

TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B or equivalent) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5. If the Power of Attorney by Applicant form is not accompanied by this transmittal form or an equivalent, the Power of Attorney will not be recognized in the application.

Application Number	Filed herewith
Filing Date	June 1, 2016
First Named Inventor	HYUN LEE
Title	MEMORY MODULE CAPABLE OF HANDSHAKING WITH A MEMORY CONTROLLER OF A HOST SYSTEM
Art Unit	Unknown
Examiner Name	Unknown
Attorney Docket Number	NETL.062C3

SIGNATURE of Applicant or Patent Practitioner

Signature	/Jamie J. Zheng/	Date	May 31, 2016
Name	Jamie J. Zheng	Telephone	650-521-4828
Registration Number	51,167		

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications.

☐ *Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: PA..

Document Description: Power of Attorney

PTO/AIA/82B(07-12)

Approved for use through 11/30/2014. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in the attached transmittal letter.

- ☐ I hereby appoint Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent):

--

OR

- ☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent):

Name	Registration Number		Name	Registration Number

Please recognize or change the correspondence address for the application identified in the attached transmittal letter to:

- ☐ The address associated with the above-mentioned Customer Number.

OR

- ☐ The address associated with Customer Number:

--

OR

☐ Firm or Individual Name				
Address				
City		State		Zip
Country				
Telephone		Email		

I am the Applicant:

- ☐ Inventor or Joint Inventor
☐ Legal Representative of a Deceased or Legally Incapacitated Inventor
☐ Assignee or Person to Whom the Inventor is Under an Obligation to Assign
☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document)

SIGNATURE of Applicant for Patent

Signature		Date	
Name		Telephone	
Title and Company			

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms for more than one signature, see below *.

- ☐ *Total of _____ forms are submitted.

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If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Samsung Electronics Co., Ltd.

Ex. 1038, p. 2

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

**GENERAL POWER OF ATTORNEY BY APPLICANT
FOR UNITED STATES PATENT**

I hereby revoke all previous powers of attorney given in the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent).

I hereby appoint the practitioner associated with the following Customer Number
:

79141

as my/our attorney or agent, and to transact all business in the United States Patent and Trademark Office in connection with the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent).

Please recognize or change the **correspondence address** for the application referenced in the attached transmittal letter to the address associated with the above-mentioned **Customer Number**.

I am the Applicant:

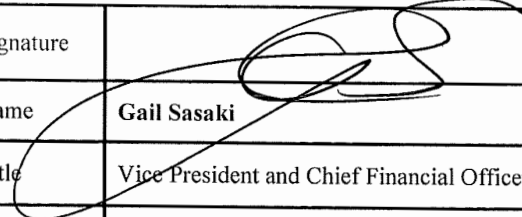
☐ Inventor or Joint Inventor

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor

☒ Assignee or Person to Whom the Inventor is Under an Obligation to Assign

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is currently being filed in this document)

SIGNATURE of Applicant for Patent

Signature		Date: January 9, 2013
Name	Gail Sasaki	
Title	Vice President and Chief Financial Officer	
Company	Netlist, Inc.	

Note: Signature - this form must be signed by the Applicant or a person authorized to act on behalf of Applicant.

Submit multiple forms for more than one signature

Total of ___ forms are submitted.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NETL.062C3
		Application Number	
Title of Invention	MEMORY MODULE CAPABLE OF HANDSHAKING WITH A MEMORY CONTROLLER OF A HOST SYSTEM		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)
--

Inventor Information:

Inventor	1				Remove	
Legal Name						
Prefix	Given Name	Middle Name	Family Name	Suffix		
	Hyun		Lee			
Residence Information (Select One) • US Residency Non US Residency Active US Military Service						
City	Ladera Ranch	State/Province	CA	Country of Residence	US	
Mailing Address of Inventor:						
Address 1		21 Thalia				
Address 2						
City	Ladera Ranch	State/Province	CA			
Postal Code	92694	Country	US			
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button.						
Add						

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).			
☐ An Address is being provided for the correspondence information of this application.			
Customer Number	79141		
Email Address	jz@jzpatent.com	Add Email	Remove Email

Application Information:

Title of the Invention	MEMORY MODULE CAPABLE OF HANDSHAKING WITH A MEMORY CONTROLLER OF A HOST SYSTEM		
Attorney Docket Number	NETL.062C3	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		Sub Class (if any)	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	3	Suggested Figure for Publication (if any)	3

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NETL.062C3
		Application Number	
Title of Invention	MEMORY MODULE CAPABLE OF HANDSHAKING WITH A MEMORY CONTROLLER OF A HOST SYSTEM		

Publication Information:

☐	Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☒	Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.			
Please Select One:			
☒	Customer Number	US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	79141		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.					
Prior Application Status	Pending	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)		
	Continuation of	15088115	2016-04-01		
Prior Application Status	Patented	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15088115	Continuation of	13942721	2013-07-16	9311116	2016-04-12
Prior Application Status	Patented	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13942721	Continuation of	12815339	2010-06-14	8489837	2013-07-16
Prior Application Status		Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12815339	non provisional of	61186799			2009-06-12
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.					

Foreign Priority Information:

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NETL.062C3
		Application Number	
Title of Invention	MEMORY MODULE CAPABLE OF HANDSHAKING WITH A MEMORY CONTROLLER OF A HOST SYSTEM		
This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).			
			Remove
Application Number	Country ¹	Filing Date (YYYY-MM-DD)	Priority Claimed
			• Yes No
Additional Foreign Priority Data may be generated within this form by selecting the Add button.			Add

Authorization to Permit Access:

Authorization to Permit Access to the Instant Application by the Participating Offices
If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application. In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application. In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.
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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NETL.062C3
		Application Number	
Title of Invention	MEMORY MODULE CAPABLE OF HANDSHAKING WITH A MEMORY CONTROLLER OF A HOST SYSTEM		

Applicant	1 Remove		
If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section. Clear			
☒ Assignee		Legal Representative under 35 U.S.C. 117	
Person to whom the inventor is obligated to assign.		Person who shows sufficient proprietary interest	
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:			
Name of the Deceased or Legally Incapacitated Inventor :			
If the Applicant is an Organization check here. ☒			
Organization Name	Netlist, Inc.		
Mailing Address Information:			
Address 1	175 Technology, #150		
Address 2			
City	Irvine	State/Province	CA
Country	US	Postal Code	92618
Phone Number	949-435-0025	Fax Number	
Email Address	gsasaki@netlist.com		
Additional Applicant Data may be generated within this form by selecting the Add button. Add			

Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee	1
Complete this section only if non-applicant assignee information is desired to be included on the patent application publication in accordance with 37 CFR 1.215(b). Do not include in this section an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest), as the patent application publication will include the name of the applicant(s). Remove	
If the Assignee is an Organization check here. ☐	

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NETL.062C3
		Application Number	
Title of Invention	MEMORY MODULE CAPABLE OF HANDSHAKING WITH A MEMORY CONTROLLER OF A HOST SYSTEM		

Prefix	Given Name	Middle Name	Family Name	Suffix

Mailing Address Information:

Address 1				
Address 2				
City		State/Province		
Country i		Postal Code		
Phone Number		Fax Number		
Email Address				

Additional Assignee Data may be generated within this form by selecting the Add button.

Add

Signature:

Remove

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications

Signature	/Jamie J. Zheng/		Date (YYYY-MM-DD)	2016-05-31
First Name	Jamie	Last Name	Zheng	Registration Number
			51167	

Additional Signature may be generated within this form by selecting the Add button.

Add

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		MEMORY MODULE CAPABLE OF HANDSHAKING WITH A MEMORY CONTROLLER OF A HOST SYSTEM		
First Named Inventor/Applicant Name:		Hyun Lee		
Filer:		Jamie Jie Zheng		
Attorney Docket Number:		NETL.062C3		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720
Pages:				
Claims:				
Claims in Excess of 20	1202	17	80	1360
Miscellaneous-Filing:				
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				2960

Electronic Acknowledgement Receipt	
EFS ID:	25931534
Application Number:	15169745
International Application Number:	
Confirmation Number:	6558
Title of Invention:	MEMORY MODULE CAPABLE OF HANDSHAKING WITH A MEMORY CONTROLLER OF A HOST SYSTEM
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.062C3
Receipt Date:	01-JUN-2016
Filing Date:	
Time Stamp:	02:07:09
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$2960
RAM confirmation Number	8318
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		2016-05-31_Spec_NETL062C3.pdf	233588 e0d46a5450020388e231c7750c78673d2d4279d1	yes	29
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	21	
	Claims		22	28	
	Abstract		29	29	
Warnings:					
Information:					
2	Drawings-only black and white line drawings	2016-05-31_Drawings_NETL062C3.pdf	315345 2c98f39e9915747c0e51480c91f3023d4534c727	no	3
Warnings:					
Information:					
3	Oath or Declaration filed	2013-10-09_Declaration_NETL062C1.pdf	286314 ac827f939d7ed2eef5ec73035d1f3c9f0f8c509d	no	2
Warnings:					
Information:					
4	Power of Attorney	2016-05-31_AIA82A_transmittal_POA_NETL062C3.pdf	195967 5865a77c37c60893a305f3023be7eeaa550ca382	no	3
Warnings:					
Information:					
5	Power of Attorney	AIA_General_POA_Netlist.pdf	133545 f8258889ee9edc63b1cc17705b3158faaed49e9e	no	1
Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					

6	Application Data Sheet	2016-05-31_ApplicationDataSheet_NETL062C3.pdf	1437494 7fe2a4d98422af858855a8d339d30848f3831c08	no	6
Warnings:					
Information:					
7	Fee Worksheet (SB06)	fee-info.pdf	37107 7a93f2e47b36d382a434ba7f476719d632372890	no	2
Warnings:					
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MEMORY MODULE CAPABLE OF HANDSHAKING WITH A MEMORY CONTROLLER OF A HOST SYSTEM

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. App. No. 15/088,115, filed April 1, 2016, entitled “SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE,” which is a continuation of U.S. App. No. 13/942,721, filed July 16, 2013, now U.S. Pat. No. 9,311,116 on April 12, 2016, which is a continuation of U.S. App. No. 12/815,339, filed June 14, 2010, now U.S. Pat. No. 8,489,837, which claims the benefit of priority from U.S. Provisional App. No. 61/186,799, filed June 12, 2009. Each of the above applications/patents is incorporated in its entirety by reference herein.

FIELD OF THE DISCLOSURE

[0002] The present disclosure relates to the operation of memory modules. Specifically, the present disclosure relates to a memory module capable of handshaking with a memory controller of a host system.

BACKGROUND OF THE DISCLOSURE

[0003] Memory subsystems such as memory modules are generally involved in the initialization procedure for computer systems, including servers, personal computers, and the like. For example, during system-wide initialization, the memory subsystems may undergo internal initialization procedures, or the system memory controller may otherwise interact with the memory subsystems during the initialization procedure. As part of this interaction, the system memory controller may request that the memory subsystem perform one or more requested tasks during system initialization.

SUMMARY

[0004] According to certain aspects, a memory module is operable with a memory controller of a host computer system. The memory module includes a module controller having an open drain output. The module controller generates a parity error signal and drives the parity error signal to the memory controller of the host system via the open drain output while the memory module

operates in a first mode, the parity error signal indicating a parity error having occurred in the memory module while the memory module operates in the first mode. The module controller is configured to cause the memory module to enter a second mode in response to a command from the memory controller of the host system. The module controller generates a notification signal indicating at least one status of one or more training sequences while the memory module is in the second mode and outputs the notification signal to the memory controller of the host system via the open drain output while the memory module is in the second mode.

[0005] The memory module further includes a printed circuit board (PCB) having a first set of edge connections for communicating address and control signals from the memory controller of the host system, a second set of edge connections for communicating data signals between the memory module and the memory controller of the host system while the memory module operates in the first mode, and an error edge connection coupled to the open drain output of the module controller. The memory module communicates to the memory controller of the host system via the error edge connection the parity error signal while the memory module operates in the first mode and the notification signal while the memory module is in the second mode.

[0006] In another aspect, a memory module includes a plurality of synchronous dynamic random access memory elements, a printed circuit board (PCB), a module circuit, and a notification circuit. The PCB has a first set of edge connections for communicating address and control signals from the memory controller of the host system, and a second set of edge connections for communicating data signals between the memory module and the memory controller of the host system while the memory module operates in a first mode. The PCB further includes an error edge connection in addition to the first set of edge connections and the second set of edge connections.

[0007] In certain embodiments, the module circuit controls the plurality of dynamic random access memory elements in response to read and write commands received from the memory controller of the host system via the first set of edge connections while the memory module operates in the first mode. The module circuit generates a parity error signal indicative of a parity error having occurred in the memory module while the memory module operates in the first mode. The module circuit can cause the memory module to enter a second mode in response to a command from the memory controller of the host system. The module circuit then generates a

notification signal in response to one or more training sequences while the memory module is in the second mode, the notification signal indicating a status of the one or more training sequences.

[0008] In certain embodiments, the notification circuit has an open drain output coupled to the error edge connection of the PCB. The notification circuit drives the parity error signal to the memory controller of the host system via the open drain output and the error edge connection while the memory module operates in the first mode. The notification circuit drives the notification signal to the memory controller of the host system via the open drain output and the error edge connection while the memory module is in the second mode.

[0009] According to additional aspects, a memory module is operable with a memory controller of a host system in at least a first mode and a second mode. The memory module includes a plurality of synchronous dynamic random access memory elements, a PCB, and a module controller. The PCB has a first set of edge connections for communicating address and control signals from the memory controller of the host system, and a second set of edge connections for communicating data signals between the memory module and the memory controller of the host system while the memory module operates in the first mode. The PCB further includes an error edge connection in addition to the first set of edge connections and the second set of edge connections. The PCB is configured to fit into a corresponding slot connector of the host system.

[0010] In certain embodiments, the module controller has an open drain output coupled to the error edge connection. The module controller is configured to transmit address and control signals to the plurality of synchronous dynamic random access memory elements in response to read or write commands received from the memory controller of the host system via the first set of edge connections while the memory module operates in the first mode, to generate a parity error signal indicating a parity error having occurred in the memory module while the memory module is in the first mode, and to transmit the parity error signal to the memory controller of the host system via the open drain output and the error edge connection while the memory module is in the first mode. The module controller is further configured to cause the memory module to enter the second mode in response to a command from the memory controller of the host system, to generate a notification signal indicating a status of one or more training sequences while the memory module is in the second mode, and to transmit the notification signal to the memory

controller of the host system via the open drain output and the error edge connection while the memory module is in the second mode.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Figure 1 shows an example host computer system including an example memory module configured to perform handshaking with a memory controller of the host computer system according to certain embodiments described herein.

[0012] Figure 2 shows an example host computer system including example first and second memory modules configured to perform handshaking with a system memory controller of the host computer system according to certain embodiments described herein.

[0013] Figure 3 shows a host computer system including example first and second memory modules configured to perform handshaking with a memory controller of the host system, where the notification circuits of the first and second memory modules have another example configuration according to certain embodiments described herein.

[0014] Figure 4 and Figure 5 show example methods of using at least one memory module according to certain embodiments described herein.

DETAILED DESCRIPTION

[0015] Existing initialization schemes have certain inefficiencies which lead to wasted time and expense. Thus, there is a need to reduce the time and complexity involved in system memory controller interactions with memory subsystems during initialization. Certain embodiments described herein advantageously satisfy at least a portion of this need by providing a system and method which utilizes a feedback path from a memory subsystem such as a memory module to a system memory controller, such as a Memory Controller Hub (MCH) of a computer system during initialization.

[0016] In general, there is no existing method of handshaking between the MCH (e.g., system memory controller) and a memory subsystem (e.g., memory module) during initialization. For example, in conventional systems, the system memory controller does not monitor the error-out signal from the memory subsystem. This causes the MCH to perform blind execution. In a typical server (e.g., an Intel or AMD or other chipset based server), the lack of any handshaking

between the MCH and the memory subsystem during the server initialization period has not been a serious issue since the MCH generally has complete control over the initialization procedure. However, one possible configuration for LR-DIMM (Load Reduced DIMM) includes the MCH handing over one or more parts of the initialization operation sequence to the memory subsystem. This raises an unprecedented issue not addressed in conventional systems because, in such proposed configurations, the system can benefit from the MCH handshaking with the memory subsystem controller, as described more fully below.

[0017] Such an LR-DIMM configuration may have the MCH inserting a waiting period of predetermined length during which the MCH is idle and the memory subsystem controller undergoes initialization. However, one shortcoming of this LR-DIMM configuration would be that it requires the MCH to be in standby (idle, or wait) while the memory subsystem controller completes its task. Under such an arrangement, since the time to complete a task can be dependent on the density, speed and configuration of the memory subsystem, and these parameters may be unknown to the MCH, the MCH may have to insert a single, predetermined standby period. In addition, if there are multiple occasions that the MCH needs to hand off control to the memory subsystem controller, the required MCH wait periods can be different from one occasion to another, and it complicates the correlation between the MCH and the memory subsystem controller. For example, the MCH according to such a scheme may give control to the local memory controller of a memory subsystem (e.g., memory module) for execution of a training sequence. The MCH may wait for a pre-determined period of time and then assume that the local memory controller has completed the training sequence. However, depending on the memory subsystem parameters (e.g., memory capacity, speed, number of ranks, etc.), the time for actually completing the training sequence may vary and may be longer or shorter than predetermined period of time.

[0018] In general, handshaking can be implemented in at least two ways; polling and notifying. In the polling method, the MCH reads a status register in the memory subsystem controller to find out if the memory subsystem controller has completed the required or requested operation. For example, a status register may be read out through a serial interface such as System Management Bus (SMBus). However, a register polling method is generally inefficient because the system memory controller does not know exactly when the memory subsystem will have completed the required or requested operation. Thus, the system memory controller may wait

longer than necessary to poll the memory subsystem, thereby delaying the overall initialization process. Additionally, the problem may be compounded because multiple training sequences or other initialization sequences may be run on the memory subsystem during a particular initialization period, resulting in accumulation of such unnecessary delays. Moreover, polling generally involves scheduling polling intervals during which the system memory controller is not performing other operations, resulting in further inefficiency.

[0019] Alternatively, the notifying method is an advantageous handshaking method between the MCH and the memory subsystem controller. According to a notifying method, the memory subsystem controller sends a signal to the MCH when the memory subsystem controller completes the required or requested operation. This method allows the MCH to execute one or more independent commands while it is waiting for a notification signal from the memory subsystem controller.

[0020] Certain embodiments described herein provide a method of establishing a handshake mechanism based on notification signaling. In certain embodiments, this mechanism can be implemented by adding a new interface (notifying) signal between the MCH and the memory subsystem controller, or by adding an additional functionality to an existing, non-timing critical signal without altering the memory subsystem hardware. In either case, the interface between the MCH and the memory subsystem controller of certain embodiments can be an open drain signaling from the memory subsystem controller to the MCH, although a variety of other configurations are possible. As will be appreciated by persons skilled in the art, the terms MCH, system memory controller, and memory subsystem are used generally interchangeable throughout this disclosure, and the terms memory module, memory subsystem controller, and local memory controller are used generally interchangeably throughout this disclosure.

[0021] FIG. 1 illustrates an example host computer system 16 including an example memory module 10 according to certain embodiments described herein. The memory module 10 can comprise at least one output 12 configured to be operatively coupled to a system memory controller 14 of the host computer system 16. In certain embodiments, the memory module 10 is configured to operate in at least two modes comprising an initialization mode during which the memory module 10 executes at least one initialization sequence, and an operational mode. The memory module 10 may further include a controller circuit 18. In some embodiments, the

controller circuit 18 is configured to cause the memory module 10 to enter the initialization mode. The memory module 10 can further include a notification circuit 20 configured to drive the at least one output 12 while the memory module 10 is in the initialization mode to provide at least one notification signal to the memory controller 14 indicating at least one status of the at least one initialization sequence.

[0022] The memory module 10 may comprise a printed-circuit board (PCB) 22. In certain embodiments, the memory module 10 has a memory capacity of 512-MB, 1-GB, 2-GB, 4-GB, 8-GB, 16-GB, or higher. Other memory capacities are also compatible with certain embodiments described herein. In addition, memory modules 10 having widths of 4 bytes, 8 bytes, 16 bytes, 32 bytes, or 32 bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein. The PCB 22 can have an industry-standard form factor. For example, the PCB 22 can have a low profile (LP) form factor with a height of 30 millimeters and a width of 133.35 millimeters. In certain other embodiments, the PCB 20 has a very high profile (VHP) form factor with a height of 50 millimeters or more. In certain other embodiments, the PCB 22 has a very low profile (VLP) form factor with a height of 18.3 millimeters. Other form factors including, but not limited to, small-outline (SO-DIMM), unbuffered (UDIMM), registered (RDIMM), fully-buffered (FBDIMM), mini-DIMM, mini-RDIMM, VLP mini-DIMM, micro-DIMM, and SRAM DIMM are also compatible with certain embodiments described herein. In other embodiments, certain non-DIMM form factors are possible such as, for example, single in-line memory module (SIMM), multi-media card (MMC), and small computer system interface (SCSI).

[0023] In certain embodiments, the memory module 10 is operatively coupled to (e.g., in electrical communication with) the host computer system 16. In certain other embodiments, the memory module 10 may communicate with the host computer system 16 using some other type of communication, such as, for example, optical communication. Examples of host computer systems 16 include, but are not limited to, blade servers, 1U servers, personal computers (PCs), and other applications in which space is constrained or limited. The PCB 22 can comprise an interface (not shown) that is configured to be in electrical communication with the host computer system 16. For example, the interface can comprise a plurality of edge connections which fit into a corresponding slot connector of the host system 16. The interface of certain embodiments provides a conduit for power voltage as well as data, address, and control signals between the

memory module 10 and the host system 16. For example, the interface can comprise a standard 240-pin DDR2 edge connector. The at least one output 12 may be routed over the interface, for example.

[0024] The memory module 10 may also comprise one or more memory elements (not shown), such as dynamic random-access memory (DRAM) elements, for example. Types of DRAM elements compatible with certain embodiments described herein include, but are not limited to, DDR, DDR2, DDR3, DDR4, and synchronous DRAM (SDRAM). In addition, memory elements having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with certain embodiments described herein. Memory elements compatible with certain embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BGA), fine-pitch BGA (FBGA), micro-BGA (μ BGA), mini-BGA (mBGA), and chip-scale packaging (CSP). In certain embodiments, the memory module 10 may also include one or more non-volatile memory elements, such as one or more flash memory elements. Types of flash memory elements compatible with certain embodiments described herein include, but are not limited to, NOR flash, NAND flash, ONE-NAND flash, and multi-level cell (MLC).

[0025] The controller circuit 18 of certain embodiments generally controls the operation of the memory module 10. For example, the controller circuit 18 may control the memory elements of the memory module 10 and/or communicate with the system memory controller 14. For example, the controller circuit 18 may receive and process address and command signals (e.g., read, write commands) from the system memory controller 14 and transmit appropriate address and commands to the memory elements in response. See, e.g., U.S. Pat. Appl. Publ. Nos. 2006/0062047 A1 and 2006/0262586 A1, each of which is incorporated in its entirety by reference herein. In certain embodiments, the controller circuit 18 comprises a local memory controller. Additionally, depending on the architecture of the memory module 10, such as for an FB-DIMM, the controller circuit 18 may comprise an advanced memory buffer (AMB). The controller circuit 18 can comprise one or more of a field-programmable gate array (FPGA), a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a custom-designed semiconductor device, and a complex programmable logic device (CPLD), for example. In certain embodiments, the controller circuit 18 comprises various discrete electrical elements, while in certain other embodiments, the controller circuit 18 comprises one or more integrated

circuits.

[0026] As discussed, the memory module 10 is configured to operate in at least two modes comprising an initialization mode during which the memory module 10 executes at least one initialization sequence, and an operational mode. In one embodiment, for example, the at least one initialization sequence may comprise one or more training sequences. The initialization sequence (e.g., comprising one or more training sequences) may be initiated by the system memory controller 14. In some embodiments, the controller circuit 18 is configured to cause the memory module 10 to enter the initialization mode. For example, the controller circuit 18 may be configured to execute a routine implementing the at least one initialization sequence when the appropriate signal or command is received from the memory controller 14 or is otherwise received from the host computer system 16 (e.g., upon receipt of a reset signal).

[0027] In certain embodiments, for example, the computer system 16 is coupled to a plurality of memory modules 10, 26 including the memory module 10 and at least a second memory module 26, and the memory controller 14 (e.g., MCH) trains each module 10, 26 separately, in series. In one example scenario, the memory controller 14 issues a first command to the memory module 10, and, in response, the memory module 10 executes an initialization sequence (e.g., one or more training sequences). Upon completion of the initialization sequence, the first memory module 10 advantageously issues a notification to the memory controller 14 in accordance with embodiments described herein. In response, the memory controller 14 issues a second command, this time to the memory module 26, and, in response, the memory module 26 executes an initialization sequence (e.g., one or more training sequences). Upon completion of the initialization sequence, the second memory module 26, similar to the first memory module 10, advantageously issues a notification to the memory controller 14 in accordance with embodiments described herein. In response, where there are more than two memory modules 10, 26, the memory controller 14 issues a third command to a third memory module (not shown), and so forth. One example computer system 16 capable of implementing such a scenario is configured to execute an Intel Basic Input/Output System (BIOS), and comprises a plurality of memory modules 10, 26 having an LRDIMM configuration. In such an example system, the Intel BIOS causes the system memory controller 14 to initialize the LRDIMM memory modules 10, 26 serially.

[0028] The operational mode is the normal mode of the memory module 10. For example, during the operational mode, the memory module 10 is generally accessed by the system memory controller 14 of the host computer 16 during standard computer operation not associated with initialization. For example, the system memory controller 14 may cause the memory module 10 to perform standard operations such as memory read/write, pre-charge, refresh, etc., while in operational mode, although it will be appreciated that one or more of these operations can also be performed by the memory module 10 while in initialization mode in certain embodiments.

[0029] The notification circuit 20 can be configured to drive the at least one output 12, while the memory module 10 is in the initialization mode or after the memory module 10 completes one or more initialization sequences, to provide the at least one notification signal to the memory controller 14 indicating at least one status of the at least one initialization sequence. While shown in FIGS. 1-3 as forming a part of the controller circuit 18, the notification circuit 20 may be a physically and/or logically separate circuit in certain embodiments. While a variety of configurations are possible, the notification circuit 20 may comprise one or more transistors, one or more logic elements (e.g., AND, OR, NOR, NAND, XOR gates, and the like), or a combination thereof. In some embodiments, the notification circuit 20 may additionally or alternatively comprise one or more of an FPGA, PLD, CPLD, ASIC, custom-designed semiconductor device, discrete electrical elements, and an integrated circuit.

[0030] The at least one status of certain embodiments comprises completion of the at least one initialization sequence, such that the at least one notification signal is indicative of the completion of the at least one initialization sequence. The at least one status of certain embodiments comprises execution of the at least one initialization sequence. For example, the at least one status may indicate that the at least one initialization sequence is currently being executed. In some embodiments, the at least one status may provide an indication that a certain task has been completed by the memory module 10, such as a training task requested by the system memory controller 14. In certain embodiments, the notification circuit 20 can be configured to drive the at least one output 12 to a first state indicative of execution of the at least one initialization sequence or to a second state indicative of completion of the at least one initialization sequence. As one example, the first state may be a high or low logic level, and the second state may be a high impedance state. In another case, the first state is a high or low logic level, and the second state is the inverse logic level of the first state.

[0031] The at least one output 12 of certain embodiments is configured to be operatively coupled to at least one interrupt of the system memory controller 14, and the system memory controller 14 is responsive to the at least one notification signal indicating completion of the at least one initialization sequence. For example, the system memory controller 14 may trigger execution of an interrupt routine upon receipt of the notification signal on the output 12. The interrupt routine generally executes the appropriate operations for the at least one status indicated by the at least one notification signal. For example, if the at least one status indicates that the at least one initialization sequence is complete, execution of the interrupt routine may cause the system memory controller 14 to notify the host computer system 16 that the system initialization, or a portion thereof, is completed. In one embodiment, for example, the execution of the interrupt routine causes the system memory controller 14 to initiate a subsequent training sequence for the memory module 10 or on another memory module connected to the host system 16. For example, in one embodiment, a central processing unit (CPU) of the host system 16 (not shown) enters a “Wait” state after issuing a command to the memory module 10 to enter the initialization mode. Receipt of the at least one notification signal on the output 12 triggers execution of the interrupt routine, which interrupts the CPU, causing the “Wait” state to be aborted and allowing the host system 16 to continue operation. In this manner, generation of the interrupt on the at least one output 12 can allow completion of the at least one initialization sequence to receive generally immediate attention from the CPU and/or memory controller 14 of the host system 16. As will be appreciated, the CPU and memory controller 14 of the host system 16 may comprise separate modules, or may alternatively comprise a single integrated module, depending on the architecture of the host system 16 chip-set.

[0032] In certain embodiments, execution of the interrupt routine causes the system memory controller 14 to cause the memory module 10 to exit the initialization mode and to enter the operational mode. In another embodiment, the memory module 10 automatically enters the operational mode upon completion of the at least one initialization sequence without intervention from the memory controller 14.

[0033] In some embodiments, the at least one output 12 is operated in conformance with a standard (e.g., an industry standard) when the memory module 10 is in the operational mode, but is not operated in conformance with the standard when the memory module 10 is in the initialization mode. An example of a standard in accordance with certain embodiments described

herein is one or more of the industry standard promulgated by the Joint Electronic Devices Engineering Counsel (JEDEC). For example, the operation and behavior of the at least one output 12 may conform to an industry standard when the memory module 10 is in the operational mode, but the operation and behavior of the at least one output 12 may not conform to the industry standard when the memory module 10 is in the initialization mode. Because the at least one output 12 does not conform to the standard during initialization mode, an existing (e.g., JEDEC-specified) pin may be utilized to provide the at least one notification signal to the system memory controller 14 from the memory module 10 during the initialization mode. In one embodiment, for example, the at least one output 12 comprises an error-out pin of the memory module 10. In conventional systems, the operation of the error-out pin is undefined by the standard during initialization. However, in certain embodiments described herein, during the operational mode, the error-out pin may be used according a conventional industry standard (e.g., a JEDEC standard) to indicate a parity error has occurred in the memory module 10. During the initialization mode, the error-out pin can be used to transmit the at least one notification signal to the system memory controller 14.

[0034] It is advantageous to use the error-out pin for initialization status notification according to certain embodiments because the error-out pin can be asserted by the memory module 10 independent from system memory controller 14 requests or commands. Also, because the error-out pin is a JEDEC-specified pin, design cost and complexity are reduced because additional pin-outs and interrupt design changes can be avoided (e.g., in cases where such changes in hardware or chipset may not be feasible to provide the at least one status to the system memory controller 14). However, in certain other embodiments, providing the at least one status may be implemented by adding one or more pins to the system memory controller 14 (e.g., MCH) and to the controller circuit 18 (e.g., local memory controller), thereby utilizing changes in hardware or the chipset.

[0035] Moreover, the error-out pin may be coupled to an interrupt of the system memory controller 14 (e.g., according to the JEDEC standard). Thus, where the error-out pin is used, from the system point of view in accordance with certain embodiments, the notification of completion of the required or requested task from the memory module 10 (e.g., by the local memory controller) generates an interrupt communicated to the system during the initialization period and indicative of completion of the required or requested task. Assertion of the same pin during

normal (non-initialization) operation upon an error occurring, on the other hand, generates an interrupt communicated to the system during the normal operation indicative of the occurrence of the error condition. Thus, in certain embodiments, the error-out pin and corresponding signal memory module 10 can be used to support the notifying function and to provide the at least one status generally without changing hardware. Certain other such embodiments involve modifying the basic input/output system (BIOS) or other programming change. For example, the BIOS may be modified to indicate to the system memory controller 14 how to respond to the notification signal (e.g., to the error_out signal or the interrupt corresponding thereto).

[0036] In certain other embodiments, the at least one output 12 may include other existing (e.g., JEDEC specified) pins instead of, or in addition to, the error-out pin. In yet other configurations, at least one additional (e.g., non-JEDEC specified) pin may be employed. In general, any pin not otherwise active during the initialization mode may be used (e.g., high-order address pins, read/write pins, data pins, etc.).

[0037] The at least one output 12 can further be configured to be operatively coupled to at least one second output 24 of a second memory module 26 in some embodiments, as schematically illustrated in FIGS. 1-3. The second memory module 26 may be generally similar in structure and function to the memory module 10, and may comprise a controller circuit 28 and a notification circuit 30, for example. The second memory module 26 may be generally identical to the first memory module 10, or may have a different memory capacity, form factor, etc., than the first memory module 10. More than two such memory modules may be present in certain embodiments. As described above, the second memory module 26 can be configured to operate in at least two modes comprising an initialization mode during which the second memory module 26 executes at least one initialization sequence, and an operational mode. For example, the initialization and operational modes may be similar to those describe above in relation to the first memory module 10.

[0038] The second memory module 26 can also be configured to drive the at least one second output 24 to a third state indicative of execution of at least one initialization sequence of the second memory module 26 or to a fourth state indicative of completion of the at least one initialization sequence of the second memory module 26. Additionally, in some embodiments, the at least one first output 12 of the first memory module 10 and the at least one second output

24 of the second memory module 26 are operatively coupled together by a bus 32 which is also operatively coupled to at least one input 34 of the system memory controller 14. In other embodiments (not shown), the at least one first output 12 and the at least one second output 24 are not coupled together, and are coupled to two separate inputs of the system memory controller 14.

[0039] FIG. 2 shows an example host computer system 16 including example first and second memory modules 10, 26. As shown, the notification circuits 20, 30 of the first and second memory modules 10, 26 each comprise at least one transistor 36, 38. The at least one transistor 36, 38 can be in an open-drain configuration, as shown, although other configurations are possible. In certain such embodiments, the first state of the at least one first output 12 is a first logic level, the second state of the at least one first output 12 is a high-impedance state, the third state of the at least one second output 24 is the first logic level, and the fourth state of the at least one second output 24 is the high-impedance state. In the illustrated example, while the at least one initialization sequence is in progress, the first and second memory modules 10, 26 drive the gates of the respective transistors 36, 38 high. Thus, the transistors 36, 38 are respectively low impedance while the memory modules 10, 26 are executing each section of the initialization sequence, thereby pulling the first and second outputs 12, 24 low. Thus, the first state and the third state are low logic levels (ground) in the example configuration. Also, because the first and second outputs 12, 24 are coupled together by the bus 32, if the at least one initialization sequence of either one of the first and second memory modules 10, 26 are in progress, the bus 32 will be pulled to a low logic level.

[0040] As each of the two memory modules 10, 26 completes its at least one initialization sequence, it can drive the corresponding at least one first and second outputs 12, 24 respectively to a high impedance state. For example, once the at least one initialization sequence on each of the first and second memory modules 10, 26 is completed, the first and second memory modules 10, 26 can drive the gates of the respective transistors 36, 38 low, resulting in a high-impedance state on the at least one first and second outputs 12, 24 causing the bus 32 to be pulled high by the system memory controller 14. Accordingly, only once the at least one initialization sequence of both the first and second memory modules 10, 26 are complete, the bus 32 will be pulled high by the internal pull-up configuration 40 of the system memory controller 14. The second state and the fourth state are therefore high-impedance values in the example embodiment. Thus, the

system memory controller 14 can monitor the value on the bus 32 via the first input 34 to determine when both of the memory modules 10, 26 have completed the at least one initialization sequence. As discussed, in other configurations the at least one first and second outputs 12, 24 may be received on separate inputs of the system memory controller 14, and the status of the at least one initialization sequence of each memory module 10, 26 may be monitored independently.

[0041] As discussed above, in certain embodiments in which more than one memory module 10, 26 is connected to the system memory controller 14, each memory module 10, 26 or associated controller circuit 18 (e.g., local memory controller) causes the corresponding notification circuit 20, 30 to drive the at least one output 12, 24 to the high impedance state from the low impedance state when it completes the requested or required operation. Thus, in certain such embodiments, the system memory controller 14 (e.g., MCH) can only pull the notifying signal high when all memory modules 10, 26 or associated controller circuits (e.g., local memory controllers) have completed the required or requested operation (e.g., initialization sequence). This configuration allows the system memory controller 14 (e.g., MCH) to work with a non-homogenous memory subsystem. For example, the system memory controller 14 may be able to monitor the progress of multiple memory modules 10, 26 including a mix of DIMMs or other memory modules having differing characteristics, such as DIMM density, rank configurations, DRAM density, speed, DRAM configuration, etc.

[0042] Additionally, the at least one output 12 of the first memory module 10 and the at least one second output 24 of the second memory module 26 are configured to be operatively coupled to at least one interrupt of the system memory controller 14 in certain embodiments. In certain such embodiments, the system memory controller 14 can be responsive to the second state of the first memory module 10 and the fourth state of the second memory module 26 by triggering execution of an interrupt routine by a processor of the system memory controller 14. For example, in the example system of FIG. 2, when the bus 32 is pulled high by the pull-up configuration 40 indicating the second state of the first memory module 10 and the fourth state of the second memory module 26, the system memory controller 14 triggers execution of the interrupt routine.

[0043] In some embodiments, in which the at least one first output 12 and the at least one second

output 24 are operatively coupled to separate inputs of the system memory controller 14, the at least one first output 12 and the at least one second output 24 may be operatively coupled to two separate interrupts. For example, the system memory controller 14 may be responsive to the second state of the first memory module 10 by triggering execution of a first interrupt routine associated with a first interrupt, and may be responsive to the fourth state of the second memory module 26 by triggering execution of a second interrupt routine associated with the second interrupt. In yet other embodiments, the separate inputs of the memory controller 14 are internally operatively coupled to the same interrupt, or are operatively coupled to separate interrupts which trigger the same interrupt routine.

[0044] FIG. 3 shows a host computer system 16 including an example memory module 10 where the notification circuit 20 of the memory module 10 has another example configuration in accordance with certain embodiments described herein. In the example configuration of FIG. 3, the at least one first output 12 is operatively coupled to an error-out pin of the memory module 10, and a multiplexor 42 drives the transistor 36 with either of a task_in_progress signal 44 or an error signal 46 (e.g., parity error signal). In one embodiment, for example, the multiplexor 42 may be configured to drive the transistor 36 with the task_in_progress signal 44 when the memory module 10 is in the initialization mode or is executing the at least one initialization sequence, and with the error signal 46 when the memory module 10 is in the operational mode. Thus, the memory module 10 can be advantageously configured to both perform the standard (e.g., JEDEC-specified) error reporting functionality via the error-out pin during the operational mode and provide the status notification functionality during the system initialization mode, as described herein. As shown in FIG. 3, a second memory module 26 including a similar configuration can also be operatively coupled to the host computer system 16. In certain embodiments, the at least one second output 24 of the second memory module 26 can be operatively coupled to the at least one first output 12 by the bus 32, as described above (e.g., with respect to FIG. 2).

[0045] FIG. 4 shows an example method 100 of using the at least one memory module 10 in accordance with certain embodiments described herein. While the description below of the method 100 refers to structure shown in FIGS. 1-3, other structures may also be used in accordance with certain embodiments described herein. At block 102, the method 100 of certain embodiments comprises providing a first memory module 10 comprising at least one first output

12 operatively coupled to a memory controller 14 of a host computer system 16. The first memory module 10 can be configured to operate in at least two modes comprising an initialization mode during which the first memory module 10 executes at least one initialization sequence, and an operational mode. For example, the at least one initialization sequence may comprise one or more steps of a series of steps associated with an initialization procedure of the host computer system 16.

[0046] At block 104, the method 100 in some embodiments comprises causing the first memory module 10 to enter the initialization mode. At block 106, the method 100 of certain embodiments comprises driving the at least one first output 12 to a first state while the memory module 10 executes the at least one initialization sequence. Upon completion of the at least one initialization sequence, the method of certain embodiments comprises driving the at least one first output 12 to a second state different than the first state. In certain embodiments, the first state is a first logic level and the second state is a high impedance state. Additionally, in certain embodiments, the at least one first output 12 is operatively coupled to at least one interrupt of the memory controller 14 such that driving the at least one output 12 to the second state triggers the memory controller to execute an interrupt routine.

[0047] In certain embodiments, the at least one output 12 is operated in conformance with JEDEC standard when the first memory module 10 is in the operational mode, but is not operated in conformance with the JEDEC standard when the first memory module 10 is in the initialization mode. The at least one first output 12 of certain embodiments include an error-out pin of the first memory module, for example.

[0048] The method 100 can further include providing a second memory module 26 comprising at least one second output 24 operatively coupled to the memory controller 14. The second memory module 26 can be configured to operate in one of at least two modes comprising an initialization mode, during which the second memory module 26 executes at least one initialization sequence, and an operational mode. The method 100 can further include causing the second memory module 26 to enter the initialization mode. In certain embodiments, the method 100 also includes driving the at least one second output 24 of the second memory module 26 to a third state while the second memory module 26 executes the at least one initialization sequence. Upon completion of the at least one initialization sequence, the method 100 can further include

driving the at least one second output 24 of the second memory module 26 to a fourth state different from the third state.

[0049] In certain embodiments, the at least one first output 12 of the first memory module 10 and the at least one second output 24 of the second memory module 26 are operatively coupled together by a bus 32 which is also operatively coupled to at least one input 34 of the memory controller 14. In certain other embodiments, the at least one first output 12 of the first memory module 10 is operatively coupled to a first input 34 of the memory controller 14 and the at least one second output 24 of the second memory module 26 is operatively coupled to a second input (not shown) of the memory controller 14.

[0050] FIG. 5 shows another example method 200 of using at least one memory module 10 in accordance with certain embodiments described herein. At block 202, the method 200 may include providing a memory module 10 comprising at least one output 12 operatively coupled to a memory controller 14 of a host computer system 16. The memory module 10 may be configured to operate in at least two modes comprising an initialization mode, during which the memory module 10 executes at least one initialization sequence, and an operational mode.

[0051] The method 200 can further include causing the memory module 10 to enter the initialization mode at block 204. At block 206, the method 200 can include receiving a notification signal from the at least one output 12 of the memory module 10. The notification signal may indicate that the memory module 10 has completed the initialization sequence, for example. In certain embodiments, the method 200 further comprises executing an interrupt routine by the memory controller 14 in response to the notification signal.

TERMINOLOGY/ALTERNATIVE EMBODIMENTS

[0052] Embodiments have been described in connection with the accompanying drawings. However, it should be understood that the figures are not drawn to scale. Distances, angles, etc. are merely illustrative and do not necessarily bear an exact relationship to actual dimensions and layout of the devices illustrated. In addition, the foregoing embodiments have been described at a level of detail to allow one of ordinary skill in the art to make and use the devices, systems, etc. described herein. A wide variety of variation is possible. Components, elements, and/or steps can be altered, added, removed, or rearranged. While certain embodiments have been explicitly described, other embodiments will become apparent to those of ordinary skill in the art based on

this disclosure.

[0053] Conditional language used herein, such as, among others, “can,” “could,” “might,” “may,” “e.g.,” and the like, unless specifically stated otherwise, or otherwise understood within the context as used, is generally intended to convey that certain embodiments include, while other embodiments do not include, certain features, elements and/or states. Thus, such conditional language is not generally intended to imply that features, elements and/or states are in any way required for one or more embodiments or that one or more embodiments necessarily include logic for deciding, with or without author input or prompting, whether these features, elements and/or states are included or are to be performed in any particular embodiment.

[0054] Depending on the embodiment, certain acts, events, or functions of any of the methods described herein can be performed in a different sequence, can be added, merged, or left out all together (e.g., not all described acts or events are necessary for the practice of the method). Moreover, in certain embodiments, acts or events can be performed concurrently, e.g., through multi-threaded processing, interrupt processing, or multiple processors or processor cores, rather than sequentially.

[0055] The various illustrative logical blocks, modules, circuits, and algorithm steps described in connection with the embodiments disclosed herein can be implemented as electronic hardware, computer software, or combinations of both. To clearly illustrate this interchangeability of hardware and software, various illustrative components, blocks, modules, circuits, and steps have been described above generally in terms of their functionality. Whether such functionality is implemented as hardware or software depends upon the particular application and design constraints imposed on the overall system. The described functionality can be implemented in varying ways for each particular application, but such implementation decisions should not be interpreted as causing a departure from the scope of the disclosure.

[0056] The various illustrative logical blocks, modules, and circuits described in connection with the embodiments disclosed herein can be implemented or performed with a general purpose processor, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general purpose processor can be a microprocessor, but in the

alternative, the processor can be any conventional processor, controller, microcontroller, or state machine. A processor can also be implemented as a combination of computing devices, e.g., a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration.

[0057] The blocks of the methods and algorithms described in connection with the embodiments disclosed herein can be embodied directly in hardware, in a software module executed by a processor, or in a combination of the two. A software module can reside in RAM memory, flash memory, ROM memory, EPROM memory, EEPROM memory, registers, a hard disk, a removable disk, a CD-ROM, or any other form of computer-readable storage medium known in the art. An exemplary storage medium is coupled to a processor such that the processor can read information from, and write information to, the storage medium. In the alternative, the storage medium can be integral to the processor. The processor and the storage medium can reside in an ASIC. The ASIC can reside in a user terminal. In the alternative, the processor and the storage medium can reside as discrete components in a user terminal.

[0058] Certain embodiments described herein are compatible with a memory system including memory devices with various attributes (see, e.g., FIGS. 2 and 3). For example, the memory system of certain embodiments may include various data slice sizes (e.g., two, four, eight, or 16 bit data slices) and corresponding memories (e.g., memories having two, four, eight, or 16 bit data widths).

[0059] Although certain embodiments and examples are discussed above, it is understood that the inventive subject matter extends beyond the specifically disclosed embodiments to other alternative embodiments and/or uses of the invention and obvious modifications and equivalents thereof. It is intended that the scope of the inventions disclosed herein should not be limited by the particular disclosed embodiments. Thus, for example, in any method or process disclosed herein, the acts or operations making up the method/process may be performed in any suitable sequence and are not necessarily limited to any particular disclosed sequence.

[0060] Various aspects and advantages of the embodiments have been described where appropriate. It is to be understood that not necessarily all such aspects or advantages may be achieved in accordance with any particular embodiment. Thus, for example, it should be recognized that the various embodiments may be carried out in a manner that achieves or

optimizes one advantage or group of advantages as taught herein without necessarily achieving other aspects or advantages as may be taught or suggested herein.

WHAT IS CLAIMED IS:

1. A memory module configured to fit into a corresponding slot of a host system to operate with a memory controller of the host system, the memory module comprising:
 - a module controller having an open drain output, the module controller generating a parity error signal and driving the parity error signal to the memory controller of the host system via the open drain output while the memory module operates in a first mode, the parity error signal indicating a parity error having occurred in the memory module while the memory module operates in the first mode, wherein the module controller is configured to cause the memory module to enter a second mode in response to a command from the memory controller of the host system, the module controller generating a notification signal indicating at least one status of one or more training sequences while the memory module is in the second mode and outputting the notification signal to the memory controller of the host system via the open drain output while the memory module is in the second mode; and
 - a printed circuit board having a first set of edge connections for communicating address and control signals from the memory controller of the host system, a second set of edge connections for communicating data signals between the memory module and the memory controller of the host system while the memory module operates in the first mode, and an error edge connection coupled to the open drain output of the module controller, the memory module communicating to the memory controller of the host system via the error edge connection the parity error signal while the memory module operates in the first mode and the notification signal while the memory module is in the second mode.
2. The memory module of Claim 1, further comprising:
 - a plurality of synchronous dynamic random access memory elements, wherein, while the memory module is in the first mode, the module controller receives and processes address and control signals corresponding to read or write commands from the memory controller of the host system and transmits appropriate address and control signals to the plurality of synchronous dynamic random access memory elements.

3. The memory module of Claim 1, wherein, while the memory module is in the second mode, the module controller drives the notification signal to a logic low level via the open drain output to indicate a status of the one or more training sequences.
4. The memory module of Claim 1, wherein the first mode is an operational mode of the memory module, and the second mode is a training mode of the memory module.
5. The memory module of Claim 1, wherein the one or more training sequences are initiated by the memory controller of the host system while the memory module is in the second mode.
6. The memory module of Claim 5, wherein the notification signal causes a subsequent training sequence to be initiated by the memory controller of the host system while the memory module is in the second mode.
7. The memory module of Claim 1, wherein the one or more training sequences are part of at least one initialization sequence executed by the module controller in response to a command or a signal received from the memory controller of the host system.
8. The memory module of Claim 1, wherein the module controller comprises one or more integrated circuit.
9. The memory module of Claim 1, wherein the module controller includes a notification circuit comprising one or more transistors each having an open drain coupled to the open drain output.
10. The memory module of Claim 9, wherein the notification circuit generates the notification signal by driving a gate of each of the one or more transistors to a logic high level such that the open drain of each of the one or more transistors provides a low impedance path to ground.
11. The memory module of Claim 9, wherein the notification circuit generates the parity error signal by driving a gate of each of the one or more transistors to a logic high level

such that the open drain of each of the one or more transistors provides a low impedance path to ground.

12. The memory module of Claim 9, wherein the notification circuit generates the notification signal using one or more OR logic elements.

13. The memory module of Claim 1, wherein the module controller implements the one or more training sequences in response to a signal or a command received from the memory controller of the host system while the memory module is in the second mode.

14. A memory module to be coupled to a memory controller of a host system, the memory module comprising:

- a plurality of synchronous dynamic random access memory elements;
- a printed circuit board (PCB) having a first set of edge connections for communicating address and control signals from the memory controller of the host system, and a second set of edge connections for communicating data signals between the memory module and the memory controller of the host system while the memory module operates in a first mode, the PCB further including an error edge connection in addition to the first set of edge connections and the second set of edge connections;

- a module circuit controlling the plurality of dynamic random access memory elements in response to read and write commands received from the memory controller of the host system via the first set of edge connections while the memory module operates in the first mode, the module circuit generating a parity error signal indicative of a parity error having occurred in the memory module while the memory module operates in the first mode, the module circuit causing the memory module to enter a second mode in response to a command from the memory controller of the host system, the module circuit generating a notification signal in response to one or more training sequences while the memory module is in the second mode, the notification signal indicating a status of the one or more training sequences; and

- a notification circuit having an open drain output coupled to the error edge connection of the PCB, the notification circuit driving the parity error signal to the memory controller of the host system via the open drain output and the error edge connection while

the memory module operates in the first mode, the notification circuit driving the notification signal to the memory controller of the host system via the open drain output and the error edge connection while the memory module is in the second mode.

15. The memory module of Claim 14, wherein the one or more training sequences are initiated by a signal or a command received from the memory controller of the host system.

16. The memory module of Claim 14, wherein the memory module executes the one or more training sequences in response to a signal or a command from the memory controller of the host system.

17. The memory module of Claim 14, wherein the first mode is an operational mode of the memory module, and the second mode is a training mode of the memory module.

18. The memory module of Claim 14, wherein the notification signal causes the memory controller of the host system to initiate a subsequent training sequence in response to the notification signal.

19. The memory module of Claim 14, wherein the notification circuit generates the notification signal using one or more OR logic elements.

20. The memory module of Claim 14, wherein the notification circuit is a physically separate circuit from the module circuit.

21. The memory module of Claim 14, wherein the module circuit includes the notification circuit.

22. The memory module of Claim 14, wherein the notification circuit includes one or more transistors each having an open drain coupled to the open drain output.

23. The memory module of Claim 22, wherein the notification circuit generates the notification signal by driving a gate of each of the one or more transistors to a logic high level such that the open drain of each of the one or more transistors provides a low impedance path to ground.

24. The memory module of Claim 22, wherein the notification circuit generates the parity error signal by driving a gate of each of the one or more transistors to a logic high level such that the open drain of each of the one or more transistors provides a low impedance path to ground.

25. The memory module of Claim 14, wherein the memory module is further configured to execute at least one initialization sequence in response to a command from the memory controller of the host system, the at least one initialization sequence including the one or more training sequences.

26. A memory module operable in at least a first mode and a second mode, the memory module comprising:

- a plurality of synchronous dynamic random access memory elements;
- a printed circuit board (PCB) having a first set of edge connections for communicating address and control signals from the memory controller of the host system, and a second set of edge connections for communicating data signals between the memory module and the memory controller of the host system while the memory module operates in the first mode, the PCB further including an error edge connection in addition to the first set of edge connections and the second set of edge connections, wherein the PCB is configured to fit into a corresponding slot connector of the host system; and

- a module controller having an open drain output coupled to the error edge connection, the module controller being configured to transmit address and control signals to the plurality of synchronous dynamic random access memory elements in response to read or write commands received from the memory controller of the host system via the first set of edge connections while the memory module operates in the first mode, to generate a parity error signal indicating a parity error having occurred in the memory module while the memory module is in the first mode, and to transmit the parity error signal to the memory controller of the host system via the open drain output and the error edge connection while the memory module is in the first mode, the module controller being further configured to cause the memory module to enter the second mode in response to a command from the memory controller of the host system, to generate a notification signal

indicating a status of one or more training sequences while the memory module is in the second mode, and to transmit the notification signal to the memory controller of the host system via the open drain output and the error edge connection while the memory module is in the second mode.

27. The memory module of Claim 26, wherein the first mode is an operational mode of the memory module, and the second mode is a training mode of the memory module.

28. The memory module of Claim 26, wherein the one or more training sequences are initiated in response to a signal or a command by the memory controller of the host system while the memory module is in the second mode.

29. The memory module of Claim 26, wherein a subsequent training sequence is initiated by the memory controller of the host system in response to the notification signal while the memory module is in the second mode.

30. The memory module of Claim 26, wherein the memory module executes the one or more training sequences in response to a command or a signal received from the memory controller of the host system while the memory module is in the second mode.

31. The memory module of Claim 26, wherein the module controller includes a notification circuit comprising one or more transistors, each of the one or more transistors having an open drain coupled to the open drain output.

32. The memory module of Claim 31, wherein the notification circuit is configured to generate the notification signal by driving a gate of each of the one or more transistors to a logic high level such that the open drain of each of the one or more transistors provides a low impedance path to ground.

33. The memory module of Claim 31, wherein the notification circuit is configured to generate the parity error signal by driving a gate of each of the one or more transistors to a logic high level such that the open drain of each of the one or more transistors provides a low impedance path to ground.

34. The memory module of Claim 31, wherein the notification circuit is configured to generate the notification signal using one or more OR logic elements.
35. The memory module of Claim 31, wherein the module controller comprises one or more integrated circuits.
36. The memory module of Claim 26, wherein one or more training sequences are part of at least one initialization sequence initiated by the memory controller of the host system for the memory module while the memory module is in the second mode.
37. The memory module of Claim 26, wherein the module controller is further configured to implement the one or more training sequences in response to a signal or a command received from the memory controller of the host system while the memory module is in the second mode.

MEMORY MODULE CAPABLE OF HANDSHAKING WITH A MEMORY CONTROLLER OF A HOST SYSTEM

ABSTRACT OF THE DISCLOSURE

A memory module is operable with a memory controller of a host computer system. The memory module includes a module controller having an open drain output. The module controller generates a parity error signal and drives the parity error signal to the memory controller of the host system via the open drain output while the memory module operates in a first mode, the parity error signal indicating a parity error having occurred in the memory module while the memory module operates in the first mode. The module controller is configured to cause the memory module to enter a second mode in response to a command from the memory controller of the host system. The module controller generates a notification signal indicating at least one status of one or more training sequences while the memory module is in the second mode and outputs the notification signal to the memory controller of the host system via the open drain output while the memory module is in the second mode.

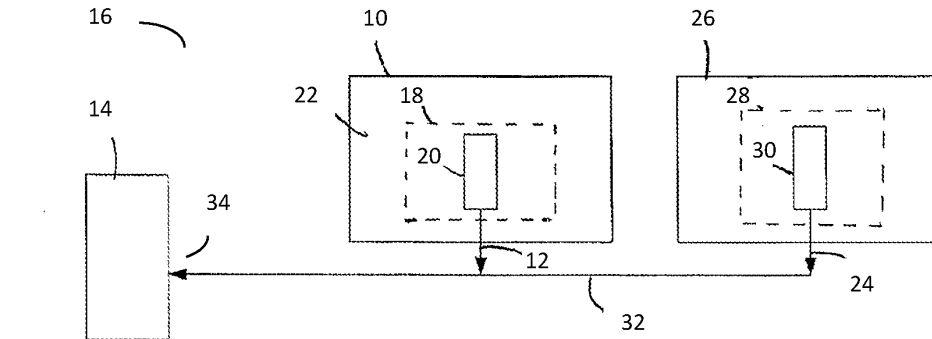


Figure 1

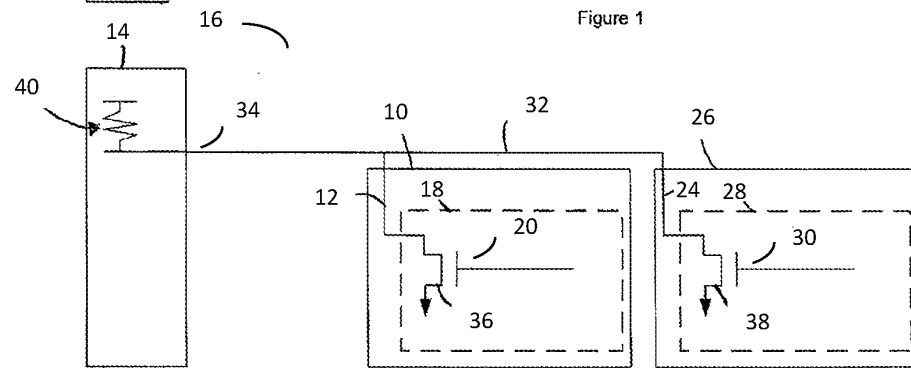


Figure 2

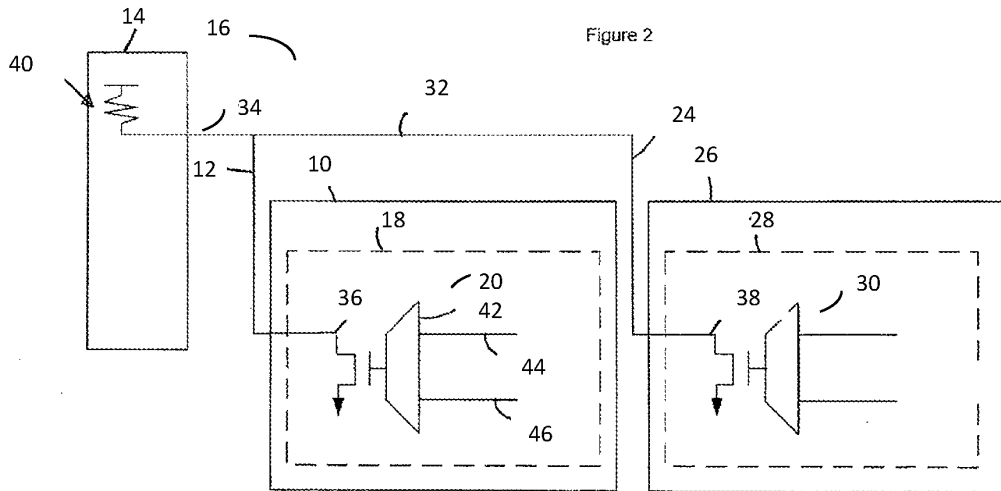


Figure 3

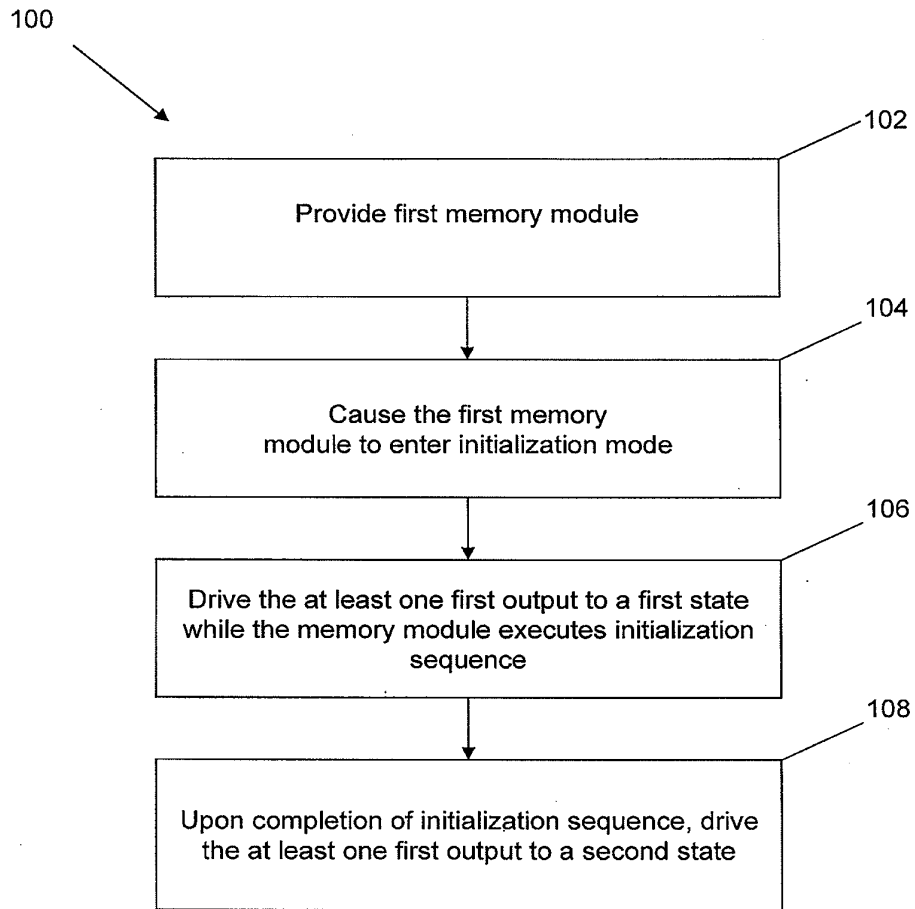


Figure 4

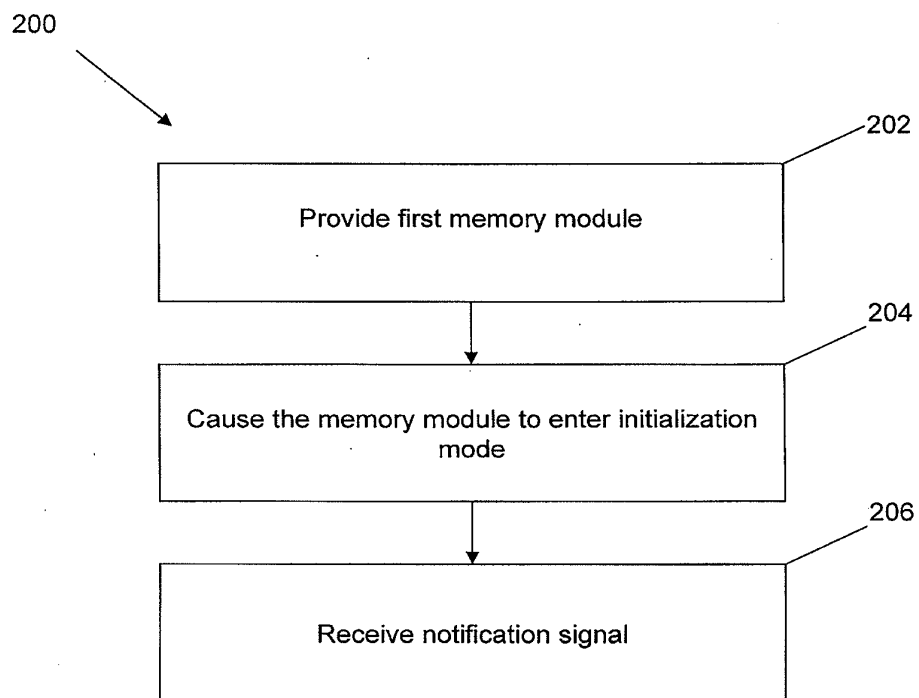


Figure 5

**COMBINED DECLARATION AND ASSIGNMENT
FOR UTILITY OR DESIGN APPLICATION**

**Title of
Invention**

SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE

DECLARATION

As a below named inventor, I hereby declare that:

This declaration
is directed to:

☐

The attached application, or

☒

United States application or PCT international application
number 13/942,721 filed on July 16, 2013 .

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

Note to Inventor: 37 C.F.R. § 1.63(c) states: "A person may not execute an oath or declaration for an application unless that person has reviewed and understands the contents of the application, including the claims, and is aware of the duty to disclose to the Office all information known to the person to be material to patentability as defined in § 1.56."

ASSIGNMENT

In consideration of the sum of One Dollar (\$1.00) and other good and valuable consideration paid, I hereby sell and assign to

Netlist, Inc.

(Name of Assignee)

of 51 Discovery, Suite #150, Irvine, CA 92618

(Address of Assignee)

(hereinafter designated as the Assignee) my entire right, title and interest for the United States as defined in 35 USC 100, for any invention set forth in the above-identified application.

I agree to execute all papers necessary in connection with this application for patent in the USPTO for the invention, and any continuation, divisional or reissue applications thereof and also to execute separate assignments in connection with such applications as the Assignee may deem necessary or expedient.

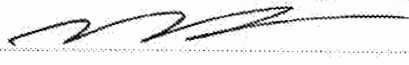
I agree to execute all papers necessary in connection with any post-grant proceeding which may occur in connection with this application or continuation, divisional or reissue thereof and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such post-grant proceeding.

I agree to execute all papers and documents and perform any act which may be necessary in connection with claims or provisions of the International Convention for Protection of Industrial Property or similar agreements.

I agree to perform all affirmative acts which may be necessary to obtain a grant of a valid United States patent to the Assignee.

I hereby authorize and request the USPTO to issue any and all Letters Patents of the United States resulting from the application or any continuation, divisional or reissue applications thereof to the Assignee, as Assignee of my entire interest, and covenant that I have not executed, and will not execute, any agreement in conflict herewith.

First Inventor (Legal Name): Hyun Lee

Signature: 

Date: 10/9/2013



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO.	TOT CLAIMS	IND CLAIMS
15/169,745	06/01/2016	2139	2960	NETL.062C3	37	3

CONFIRMATION NO. 6558

FILING RECEIPT



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79141

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Date Mailed: 06/16/2016

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

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Power of Attorney: The patent practitioners associated with Customer Number 79141

Domestic Priority data as claimed by applicant

This application is a CON of 15/088,115 04/01/2016
which is a CON of 13/942,721 07/16/2013 PAT 9311116
which is a CON of 12/815,339 06/14/2010 PAT 8489837
which claims benefit of 61/186,799 06/12/2009

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: No

Permission to Access Search Results: No

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 06/14/2016

page 1 of 3

Samsung Electronics Co., Ltd.

Ex. 1038, p. 50

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/169,745**

Projected Publication Date: Request for Non-Publication Acknowledged

Non-Publication Request: Yes

Early Publication Request: No
Title

MEMORY MODULE CAPABLE OF HANDSHAKING WITH A MEMORY CONTROLLER OF A HOST SYSTEM

Preliminary Class

711

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 15/169,745				
APPLICATION AS FILED - PART I										
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY				
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)			
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280			
SEARCH FEE (37 CFR 1.16(k), (j), or (m))	N/A	N/A	N/A			N/A	600			
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720			
TOTAL CLAIMS (37 CFR 1.16(i))	37	minus 20 = *	17			x 80 =	1360			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3	minus 3 = *				x 420 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL		TOTAL	2960			
APPLICATION AS AMENDED - PART II										
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OTHER THAN SMALL ENTITY		
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=		x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=		x	=
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE			TOTAL ADD'L FEE	
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=		x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=		x	=
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE			TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.										



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/169,745	06/01/2016	Hyun Lee	NETL.062C3	6558
79141	7590	07/29/2016	EXAMINER	
Jamie J. Zheng, Ph.D Esq. P.O. Box 60573 Palo Alto, CA 94306			CHERY, MARDOCHEE	
			ART UNIT	PAPER NUMBER
			2133	
			NOTIFICATION DATE	DELIVERY MODE
			07/29/2016	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

jz@jzpatent.com
eofficeaction@appcoll.com
infohub.j@gmail.com

Office Action Summary	Application No. 15/169,745	Applicant(s) LEE, HYUN	
	Examiner Mardochee CHERY	Art Unit 2133	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06/01/2016.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) ☒ Claim(s) 1-34 is/are pending in the application.
5a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) ____ is/are allowed.
- 7) ☒ Claim(s) 1-34 is/are rejected.
- 8) ☐ Claim(s) ____ is/are objected to.
- 9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some** c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date ____.
- 3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 4) ☐ Other: ____.

DETAILED ACTION

1. The present application is being examined under the pre-AIA first to invent provisions.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the “right to exclude” granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file

provisions of the AIA as explained in MPEP § 2159. See MPEP §§ 706.02(I)(1) - 706.02(I)(3) for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. **A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.**

3. Claims 1-37 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-20 of U.S. Patent No. 9311116. Although the claims at issue are not identical, they are not patentably distinct from each other because the claims of the instant application anticipate and/or make obvious the claims of the issued patent and vice versa. Additionally, a later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or **anticipated by**, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a

genus is anticipated by a patent claim to a species within that genus). “ ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

4. Claims 1-34 are provisionally rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-20 of copending Application No. 15/088115 (reference application). Although the claims at issue are not identical, they are not patentably distinct from each other because the claims of the instant application anticipates and/or make obvious the claims of the copending application and vice versa. Additionally, a later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or **anticipated by**, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). “ ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

This is a provisional nonstatutory double patenting rejection because the patentably indistinct claims have not in fact been patented.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mardochee CHERY whose telephone number is (571)272-4246. The examiner can normally be reached on 8:30A-5:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jared Ian Rutz can be reached on (571)272-5535. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

July 25, 2016

/Mardochee CHERY/
Primary Examiner, Art Unit 2133

Notice of References Cited	Application/Control No. 15/169,745	Applicant(s)/Patent Under Reexamination LEE, HYUN	
	Examiner Mardochee CHERY	Art Unit 2133	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2001/0034246 A1	10-2001	Hutchison, James A. IV	H04M11/06	455/557
	B	US-				
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<i>Search Notes</i> 	Application/Control No. 15169745	Applicant(s)/Patent Under Reexamination LEE, HYUN
	Examiner MARDOCHEE CHERY	Art Unit 2133

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
711	170	7/25/16	MC

SEARCH NOTES		
Search Notes	Date	Examiner
EAST Search	7/25/16	MC

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

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<i>Index of Claims</i> 	Application/Control No. 15169745	Applicant(s)/Patent Under Reexamination LEE, HYUN
	Examiner MARDOCHEE CHERY	Art Unit 2133

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47										
CLAIM		DATE								
Final	Original	07/25/2016								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
	9	✓								
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	27	✓								
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	29	✓								
	30	✓								
	31	✓								
	32	✓								
	33	✓								
	34	✓								

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Netlist, Inc.
App. No.	:	15/169,745
Filed	:	June 1, 2016
For	:	MEMORY MODULE CAPABLE OF HANDSHAKING WITH A MEMORY CONTROLLER OF A HOST SYSTEM
Examiner	:	CHERY, MARDOCHEE
Art Unit	:	2133
Conf. No.	:	6558
Docket No.	:	NETL.062C3

REPONSE TO NON-FINAL OFFICE ACTION DATED JULY 29, 2016**Mail Stop Amendment**

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Dear Sir:

This submission is in response to the Non-Final Office Action dated July 29, 2016.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 50-5963.

Amendments to the Claims: Begin on page 2 of this paper.

Remarks: Begin on page 9 of this paper.

In the Claims:

1. (Original) A memory module configured to fit into a corresponding slot of a host system to operate with a memory controller of the host system, the memory module comprising:

a module controller having an open drain output, the module controller generating a parity error signal and driving the parity error signal to the memory controller of the host system via the open drain output while the memory module operates in a first mode, the parity error signal indicating a parity error having occurred in the memory module while the memory module operates in the first mode, wherein the module controller is configured to cause the memory module to enter a second mode in response to a command from the memory controller of the host system, the module controller generating a notification signal indicating at least one status of one or more training sequences while the memory module is in the second mode and outputting the notification signal to the memory controller of the host system via the open drain output while the memory module is in the second mode; and

a printed circuit board having a first set of edge connections for communicating address and control signals from the memory controller of the host system, a second set of edge connections for communicating data signals between the memory module and the memory controller of the host system while the memory module operates in the first mode, and an error edge connection coupled to the open drain output of the module controller, the memory module communicating to the memory controller of the host system via the error edge connection the parity error signal while the memory module operates in the first mode and the notification signal while the memory module is in the second mode.

2. (Currently Amended) The memory module of Claim 1, further comprising:

a plurality of synchronous dynamic random access memory elements, wherein, while the memory module is in the first mode, the module controller receives and processes address and control signals corresponding to read or write commands from the memory controller of the host system and transmits processed ~~appropriate~~ address and control signals to the plurality of synchronous dynamic random access memory elements.

3. (Original) The memory module of Claim 1, wherein, while the memory module is in the second mode, the module controller drives the notification signal to a logic low level via the open drain output to indicate a status of the one or more training sequences.
4. (Original) The memory module of Claim 1, wherein the first mode is an operational mode of the memory module, and the second mode is a training mode of the memory module.
5. (Cancelled)
6. (Cancelled)
7. (Currently Amended) The memory module of Claim 1, wherein the one or more training sequences are ~~part of at least one initialization sequence~~ executed by the module controller in response to a command or a signal received from the memory controller of the host system.
8. (Original) The memory module of Claim 1, wherein the module controller comprises one or more integrated circuit.
9. (Original) The memory module of Claim 1, wherein the module controller includes a notification circuit comprising one or more transistors each having an open drain coupled to the open drain output.
10. (Original) The memory module of Claim 9, wherein the notification circuit generates the notification signal by driving a gate of each of the one or more transistors to a logic high level such that the open drain of each of the one or more transistors provides a low impedance path to ground.
11. (Original) The memory module of Claim 9, wherein the notification circuit generates the parity error signal by driving a gate of each of the one or more transistors to a logic high level such that the open drain of each of the one or more transistors provides a low impedance path to ground.

12. (Original) The memory module of Claim 9, wherein the notification circuit generates the notification signal using one or more OR logic elements.
13. (Currently Amended) The memory module of Claim 1, wherein the module controller implements the one or more training sequences in response to a signal or a command received from the memory controller of the host system ~~while the memory module is in the second mode.~~
14. (Currently Amended) A memory module to be coupled to a memory controller of a host system, the memory module comprising:
- a plurality of synchronous dynamic random access memory elements;
 - a printed circuit board (PCB) having a first set of edge connections for communicating address and control signals from the memory controller of the host system, and a second set of edge connections for communicating data signals between the memory module and the memory controller of the host system while the memory module operates in a first mode, the PCB further including an error edge connection in addition to the first set of edge connections and the second set of edge connections;
 - a module circuit controlling the plurality of synchronous dynamic random access memory elements in response to read and write commands received from the memory controller of the host system via the first set of edge connections while the memory module operates in the first mode, the module circuit generating a parity error signal indicative of a parity error having occurred in the memory module while the memory module operates in the first mode, the module circuit causing the memory module to enter a second mode in response to a command from the memory controller of the host system, the module circuit generating a notification signal in response to one or more training sequences while the memory module is in the second mode, the notification signal indicating a status of the one or more training sequences; and
 - a notification circuit having an open drain output coupled to the error edge connection of the PCB, the notification circuit driving the parity error signal to the memory controller of the host system via the open drain output and the error edge connection while the memory module operates in the first mode, the notification circuit driving the notification signal to the memory controller of the host system via the open

drain output and the error edge connection while the memory module is in the second mode.

15. (Cancelled)

16. (Original) The memory module of Claim 14, wherein the memory module executes the one or more training sequences in response to a signal or a command from the memory controller of the host system.

17. (Original) The memory module of Claim 14, wherein the first mode is an operational mode of the memory module, and the second mode is a training mode of the memory module.

18. (Cancelled)

19. (Original) The memory module of Claim 14, wherein the notification circuit generates the notification signal using one or more OR logic elements.

20. (Original) The memory module of Claim 14, wherein the notification circuit is a physically separate circuit from the module circuit.

21. (Original) The memory module of Claim 14, wherein the module circuit includes the notification circuit.

22. (Original) The memory module of Claim 14, wherein the notification circuit includes one or more transistors each having an open drain coupled to the open drain output.

23. (Original) The memory module of Claim 22, wherein the notification circuit generates the notification signal by driving a gate of each of the one or more transistors to a logic high level such that the open drain of each of the one or more transistors provides a low impedance path to ground.

24. (Original) The memory module of Claim 22, wherein the notification circuit generates the parity error signal by driving a gate of each of the one or more transistors to

a logic high level such that the open drain of each of the one or more transistors provides a low impedance path to ground.

25. (Cancelled)

26. (Original) A memory module operable in at least a first mode and a second mode, the memory module comprising:

- a plurality of synchronous dynamic random access memory elements;

- a printed circuit board (PCB) having a first set of edge connections for communicating address and control signals from the memory controller of the host system, and a second set of edge connections for communicating data signals between the memory module and the memory controller of the host system while the memory module operates in the first mode, the PCB further including an error edge connection in addition to the first set of edge connections and the second set of edge connections, wherein the PCB is configured to fit into a corresponding slot connector of the host system; and

- a module controller having an open drain output coupled to the error edge connection, the module controller being configured to transmit address and control signals to the plurality of synchronous dynamic random access memory elements in response to read or write commands received from the memory controller of the host system via the first set of edge connections while the memory module operates in the first mode, to generate a parity error signal indicating a parity error having occurred in the memory module while the memory module is in the first mode, and to transmit the parity error signal to the memory controller of the host system via the open drain output and the error edge connection while the memory module is in the first mode, the module controller being further configured to cause the memory module to enter the second mode in response to a command from the memory controller of the host system, to generate a notification signal indicating a status of one or more training sequences while the memory module is in the second mode, and to transmit the notification signal to the memory controller of the host system via the open drain output and the error edge connection while the memory module is in the second mode.

27. (Original) The memory module of Claim 26, wherein the first mode is an operational mode of the memory module, and the second mode is a training mode of the memory module.
28. (Cancelled)
29. (Cancelled)
30. (Currently Amended) The memory module of Claim 26, wherein the memory module executes the one or more training sequences in response to a command or a signal received from the memory controller of the host system ~~while the memory module is in the second mode.~~
31. (Original) The memory module of Claim 26, wherein the module controller includes a notification circuit comprising one or more transistors, each of the one or more transistors having an open drain coupled to the open drain output.
32. (Original) The memory module of Claim 31, wherein the notification circuit is configured to generate the notification signal by driving a gate of each of the one or more transistors to a logic high level such that the open drain of each of the one or more transistors provides a low impedance path to ground.
33. (Original) The memory module of Claim 31, wherein the notification circuit is configured to generate the parity error signal by by driving a gate of each of the one or more transistors to a logic high level such that the open drain of each of the one or more transistors provides a low impedance path to ground.
34. (Original) The memory module of Claim 31, wherein the notification circuit is configured to generate the notification signal using one or more OR logic elements.
35. (Original) The memory module of Claim 31, wherein the module controller comprises one or more integrated circuits.
36. (Cancelled)

37. (Currently Amended) The memory module of Claim 26, wherein the module controller is further configured to implement the one or more training sequences in response to a signal or a command received from the memory controller of the host system ~~while the memory module is in the second mode.~~

REMARKS

This amendment responds to the Non-Final Office Action dated July 29, 2016. In the Office Action, the Examiner:

- rejected claims 1-37 on the ground of nonstatutory double patenting as being unpatentable over claims 1-20 of U.S. Patent No. 9,311,116; and
- provisionally rejected claims 1-34 on the ground of nonstatutory double patenting as being unpatentable over claims 1-20 of copending Application No. 15/088,115.

I. CLAIM AMENDMENTS

Claims 5, 6, 15, 18, 25, 28, 29, and 36 are cancelled without prejudice. Claims 2, 7, 13, 14, 30, and 37 are amended for minor issues. No new matter is added.

I. REJECTION OF CLAIMS ON THE GROUND OF NONSTATUTORY DOUBLE PATENTING

Applicant files herewith a terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) to overcome the nonstatutory double patenting rejections.

Applicant submits that claims 1-4, 7-14, 16-17, 19-24, 26-27, 30-35, and 37 are in condition for allowance, and respectfully requests such action. The Examiner is invited to call the undersigned at (650) 521-4828 if such phone call would help resolve any remaining issues.

Respectfully submitted,

Date: August 2, 2016

/Jamie J. Zheng/

51167

Jamie J. Zheng
Customer No. 79141

(Reg. No.)

Electronic Patent Application Fee Transmittal				
Application Number:		15169745		
Filing Date:		01-Jun-2016		
Title of Invention:		MEMORY MODULE CAPABLE OF HANDSHAKING WITH A MEMORY CONTROLLER OF A HOST SYSTEM		
First Named Inventor/Applicant Name:		Hyun Lee		
Filer:		Jamie Jie Zheng		
Attorney Docket Number:		NETL.062C3		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
Total in USD (\$)				180

Electronic Acknowledgement Receipt	
EFS ID:	26528886
Application Number:	15169745
International Application Number:	
Confirmation Number:	6558
Title of Invention:	MEMORY MODULE CAPABLE OF HANDSHAKING WITH A MEMORY CONTROLLER OF A HOST SYSTEM
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.062C3
Receipt Date:	03-AUG-2016
Filing Date:	01-JUN-2016
Time Stamp:	02:53:46
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$180
RAM confirmation Number	6976
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	2016-08-02_IDS_Cover_NETL062C3.pdf	48519	no	2
			5b0f7087eba08326b52a794ce54edf9ded981c54		
Warnings:					
Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	2016-08-02_IDS_NETL062C3.pdf	69164	no	1
			d4ea7fca69eb7af1e5b7b40df0258b5e96ebb67d		
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3		2016-08-02_Rsps_NFOA_NETL062C3.pdf	100893	yes	9
			69399559092c63e80e7890627da8b944e09d9c53		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Amendment/Req. Reconsideration-After Non-Final Reject		1	1	
	Claims		2	8	
	Applicant Arguments/Remarks Made in an Amendment		9	9	
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	30931	no	2
			f769418a9adb898121607072a64b35b848b2c20		
Warnings:					
Information:					
Total Files Size (in bytes):			249507		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT

Applicant	: Netlist, Inc.
App. No.	: 15/169,745
Filed	: June 1, 2016
For	: MEMORY MODULE CAPABLE OF HANDSHAKING WITH A MEMORY CONTROLLER OF A HOST SYSTEM
Examiner	: CHERY, MARDOCHEE
Art Unit	: 2133
Conf. No.	: 6558
Docket No.	: NETL.062C3

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed for filing in the above-identified application is a Form PTO/SB/08a/b Equivalent listing 11 references. Copies of foreign documents and/or their translation and non-patent literature are submitted herewith.

The applicant would appreciate the Examiner initialing and returning the Form PTO/SB/08a/b Equivalent indicating that the information has been considered and made of record herein.

The information contained in this Information Disclosure Statement is not to be construed as a representation that: (i) a complete search has been made; (ii) additional information material to this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the above information constitutes prior art to the subject invention.

Application No.: 15/169,745
Filing Date: June 1, 2016

The Commissioner is authorized to charge the fee set forth in 37 C.F.R. § 1.17(p) to
Deposit Account No. 50-5963.

Respectfully submitted,

Dated: August 2, 2016

/Jamie J. Zheng/

Jamie J. Zheng
Customer No. 79141
(650) 521-4828

51167
(Reg. No.)

Doc Code: DIST.E.FILE Document Description: Electronic Terminal Disclaimer - Filed		PTO/SB/25 PTO/SB/26 U.S. Patent and Trademark Office Department of Commerce
Electronic Petition Request	TERMINAL DISCLAIMER TO OBVIATE A PROVISIONAL DOUBLE PATENTING REJECTION OVER A PENDING "REFERENCE" APPLICATION AND TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	
Application Number	15169745	
Filing Date	01-Jun-2016	
First Named Inventor	Hyun Lee	
Attorney Docket Number	NETL.062C3	
Title of Invention	MEMORY MODULE CAPABLE OF HANDSHAKING WITH A MEMORY CONTROLLER OF A HOST SYSTEM	
☒ Filing of terminal disclaimer does not obviate requirement for response under 37 CFR 1.111 to outstanding Office Action ☒ This electronic Terminal Disclaimer is not being used for a Joint Research Agreement.		
Owner	Percent Interest	
Netlist, Inc.	100 %	
The owner(s) of percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of any patent granted on pending reference Application Number(s)		
15088115 filed on 04/01/2016 as the term of any patent granted on said reference application may be shortened by any terminal disclaimer filed prior to the grant of any patent on the pending reference application. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and any patent granted on the reference application are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns. In making the above disclaimer, the owner does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full statutory term of any patent granted on said reference application, "as the term of any patent granted on said reference application may be shortened by any terminal disclaimer filed prior to the grant of any patent on the pending reference application," in the event that any such patent granted on the pending reference application: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321, has all claims canceled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term as shortened by any terminal disclaimer filed prior to its grant.		
The owner(s) with percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent number(s)		

9311116

as the term of said prior patent is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later:

- expires for failure to pay a maintenance fee;
- is held unenforceable;
- is found invalid by a court of competent jurisdiction;
- is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
- has all claims canceled by a reexamination certificate;
- is reissued; or
- is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

☒ Terminal disclaimer fee under 37 CFR 1.20(d) is included with Electronic Terminal Disclaimer request.

☐ I certify, in accordance with 37 CFR 1.4(d)(4), that the terminal disclaimer fee under 37 CFR 1.20(d) required for this terminal disclaimer has already been paid in the above-identified application.

Applicants claims the following fee status:

☐ Small Entity

☐ Micro Entity

☒ Regular Undiscounted

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES

I certify, in accordance with 37 CFR 1.4(d)(4) that I am:

☒ An attorney or agent registered to practice before the Patent and Trademark Office who is of record in this application

Registration Number 51167

☐ A sole inventor

☐ A joint inventor; I certify that I am authorized to sign this submission on behalf of all of the inventors as evidenced by the power of attorney in the application

☐ A joint inventor; all of whom are signing this request

Signature

/Jamie J. Zheng/

Name

Jamie J. Zheng

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

Electronic Patent Application Fee Transmittal				
Application Number:		15169745		
Filing Date:		01-Jun-2016		
Title of Invention:		MEMORY MODULE CAPABLE OF HANDSHAKING WITH A MEMORY CONTROLLER OF A HOST SYSTEM		
First Named Inventor/Applicant Name:		Hyun Lee		
Filer:		Jamie Jie Zheng		
Attorney Docket Number:		NETL.062C3		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Statutory or Terminal Disclaimer	1814	1	160	160
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				160

Doc Code: DISQ.E.FILE

Document Description: Electronic Terminal Disclaimer – Approved

Application No.: 15169745

Filing Date: 01-Jun-2016

Applicant/Patent under Reexamination: Lee et al.

Electronic Terminal Disclaimer filed on August 3, 2016

☒ APPROVED

This patent is subject to a terminal disclaimer

☐ DISAPPROVED

Approved/Disapproved by: Electronic Terminal Disclaimer automatically approved by EFS-Web

U.S. Patent and Trademark Office

Electronic Acknowledgement Receipt	
EFS ID:	26528876
Application Number:	15169745
International Application Number:	
Confirmation Number:	6558
Title of Invention:	MEMORY MODULE CAPABLE OF HANDSHAKING WITH A MEMORY CONTROLLER OF A HOST SYSTEM
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.062C3
Receipt Date:	03-AUG-2016
Filing Date:	01-JUN-2016
Time Stamp:	02:44:03
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$160
RAM confirmation Number	6967
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Electronic Terminal Disclaimer-Filed	eTerminal-Disclaimer.pdf	36106	no	3
			3a6fb8bb9cae4c203dd8ef7736e60cd33035f2d7		
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30739	no	2
			cb7d456a49bfb43f3c15c69a5a4e7eae6a93c37		
Warnings:					
Information:					
Total Files Size (in bytes):			66845		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Complete if Known	
				Application Number	15/169,745
				Filing Date	June 1, 2016
				First Named Inventor	Hyun Lee
				Art Unit	2133
				Examiner Name	CHERY, MARDOCHEE
Sheet	1	of	1	Attorney Docket Number	NETL.062C3

US PATENT DOCUMENTS					
Examiner Initials *	Cite No. ¹	Document Number	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	1.	US 4672570	06-09-1987	The United States Of America As Represented By The Secretary Of The Air Force	
	2.	US 5511152	04-23-1996	Digital Equipment Corporation	
	3.	US 6763437	07-13-2004	Maxtor Corporation	
	4.	US 7586350	09-08-2009	Hynix Semiconductor Inc.	
	5.	US 20030115427	06-19-2003	Micron Technology, Inc	
	6.	US 20070091702	04-26-2007	Andrey Nikitin	
	7.	US 20080256281	10-16-2008	International Business Machines Corporation	
	8.	US 20090119464	05-07-2009	Grundy Kevin P	
	9.	US 20100042778	02-18-2010	Advanced Micro Devices, Inc.	
	10.	US 20100202240	08-12-2010	Stec, Inc.	
	11.	US 20110022789	01-27-2011	Kabushiki Kaisha Toshiba	

EXAMINER

DATE CONSIDERED

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patents Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document and WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 15/169,745		Filing Date 06/01/2016		☐ To be Mailed				
ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO													
APPLICATION AS FILED – PART I													
(Column 1)		(Column 2)											
FOR		NUMBER FILED		NUMBER EXTRA		RATE (\$)		FEE (\$)					
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A		N/A		N/A							
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))		N/A		N/A		N/A							
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A		N/A		N/A							
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 =		*		X \$ =							
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =		*		X \$ =							
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).											
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))													
* If the difference in column 1 is less than zero, enter "0" in column 2.						TOTAL							
APPLICATION AS AMENDED – PART II													
(Column 1)		(Column 2)		(Column 3)									
AMENDMENT	08/03/2016		CLAIMS REMAINING AFTER AMENDMENT			HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA		RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))		* 29		Minus	** 37		= 0		X \$80 =		0	
	Independent (37 CFR 1.16(h))		* 3		Minus	*** 3		= 0		X \$420 =		0	
	☐ Application Size Fee (37 CFR 1.16(s))												
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))												
						TOTAL ADD'L FEE		0					
(Column 1)		(Column 2)		(Column 3)									
AMENDMENT			CLAIMS REMAINING AFTER AMENDMENT			HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA		RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))		*		Minus	**		=		X \$ =			
	Independent (37 CFR 1.16(h))		*		Minus	***		=		X \$ =			
	☐ Application Size Fee (37 CFR 1.16(s))												
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))												
						TOTAL ADD'L FEE							
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.										LIE /STELLA LITTLE/			

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Complete if Known	
				Application Number	15/169,745
				Filing Date	June 1, 2016
				First Named Inventor	Hyun Lee
				Art Unit	2133
				Examiner Name	CHERY, MARDOCHEE
Sheet	1	of	1	Attorney Docket Number	NETL.062C3

US PATENT DOCUMENTS					
Examiner Initials *	Cite No. ¹	Document Number	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	1.	US 7266633	09-04-2007	Micron Technology, Inc.	
	2.	US 7539909	05-26-2009	Intel Corporation	
	3.	US 7065688	06-20-2006	Advanced Micro Devices, Inc.	
	4.	US 5450576	09-12-1995	Ast Research, Inc.	
	5.	US 5684979	11-04-1997	IBM Corporation	
	6.	US 6886109	04-26-2005	Hewlett-Packard Development Company, L.P.	
	7.	US 7024518	04-04-2006	Intel Corporation	
	8.	US 7093115	08-15-2006	Intel Corporation	
	9.	US 7489163	02-10-2009	IBM Corporation	
	10.	US 8429493	04-23-2013	Apple Inc.	
	11.	US 20050071580	03-31-2005	Intel Corporation	
	12.	US 2007/0214347	09-13-2007	Rothman et al.	
	13.	US 20100005218	01-07-2010	IBM Corporation	

EXAMINER

DATE CONSIDERED

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patents Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document and WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

Electronic Patent Application Fee Transmittal				
Application Number:		15169745		
Filing Date:		01-Jun-2016		
Title of Invention:		MEMORY MODULE CAPABLE OF HANDSHAKING WITH A MEMORY CONTROLLER OF A HOST SYSTEM		
First Named Inventor/Applicant Name:		Hyun Lee		
Filer:		Jamie Jie Zheng		
Attorney Docket Number:		NETL.062C3		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
Total in USD (\$)				180

Electronic Acknowledgement Receipt	
EFS ID:	26609679
Application Number:	15169745
International Application Number:	
Confirmation Number:	6558
Title of Invention:	MEMORY MODULE CAPABLE OF HANDSHAKING WITH A MEMORY CONTROLLER OF A HOST SYSTEM
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.062C3
Receipt Date:	10-AUG-2016
Filing Date:	01-JUN-2016
Time Stamp:	23:58:27
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$180
RAM confirmation Number	6785
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	2016-08-10_IDS_Cover_NETL062C3.pdf	48411	no	2
			695e2b88fc575735b0f07a26fd209328ccce5c4b		
Warnings:					
Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	2016-08-10_IDS_NETL062C3.pdf	67036	no	1
			c9a13ad7d4c938c25dd289cd5a624f39fe7dc2a9e		
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3	Fee Worksheet (SB06)	fee-info.pdf	30930	no	2
			7d1db77f388ab1ae3021ace26cef28740e78abcf		
Warnings:					
Information:					
Total Files Size (in bytes):			146377		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

INFORMATION DISCLOSURE STATEMENT

Applicant	: Netlist, Inc.
App. No.	: 15/169,745
Filed	: June 1, 2016
For	: MEMORY MODULE CAPABLE OF HANDSHAKING WITH A MEMORY CONTROLLER OF A HOST SYSTEM
Examiner	: CHERY, MARDOCHEE
Art Unit	: 2133
Conf. No.	: 6558
Docket No.	: NETL.062C3

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed for filing in the above-identified application is a Form PTO/SB/08a/b Equivalent listing 13 references. Copies of foreign documents and/or their translation and non-patent literature are submitted herewith.

The applicant would appreciate the Examiner initialing and returning the Form PTO/SB/08a/b Equivalent indicating that the information has been considered and made of record herein.

The information contained in this Information Disclosure Statement is not to be construed as a representation that: (i) a complete search has been made; (ii) additional information material to this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the above information constitutes prior art to the subject invention.

Application No.: 15/169,745
Filing Date: June 1, 2016

The Commissioner is authorized to charge the fee set forth in 37 C.F.R. § 1.17(p) to
Deposit Account No. 50-5963.

Respectfully submitted,

Dated: August 10, 2016

/Jamie J. Zheng/

Jamie J. Zheng
Customer No. 79141
(650) 521-4828

51167
(Reg. No.)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Netlist, Inc.
App. No.	:	15/169,745
Filed	:	June 1, 2016
For	:	MEMORY MODULE CAPABLE OF HANDSHAKING WITH A MEMORY CONTROLLER OF A HOST SYSTEM
Examiner	:	CHERY, MARDOCHEE
Art Unit	:	2133
Conf. No.	:	6558
Docket No.	:	NETL.062C3

AUTHORIZATION TO COMMUNICATE VIA EMAIL

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with the undersigned and practitioners in accordance with 37 CFR 1.33 and 37 CFR 1.34 concerning any subject matter of this application by video conferencing, instant messaging, or electronic mail. I understand that a copy of these communications will be made of record in the application file.

The undersigned can be reached at (650) 521-4828 or jz@jzpatent.com for any questions regarding the above-reference patent application.

Respectfully submitted,

Date: August 19, 2016

/Jamie J. Zheng/
Jamie J. Zheng
Customer No. 79141

51167
(Reg. No.)

Electronic Acknowledgement Receipt	
EFS ID:	26693449
Application Number:	15169745
International Application Number:	
Confirmation Number:	6558
Title of Invention:	MEMORY MODULE CAPABLE OF HANDSHAKING WITH A MEMORY CONTROLLER OF A HOST SYSTEM
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL062C3
Receipt Date:	19-AUG-2016
Filing Date:	01-JUN-2016
Time Stamp:	14:13:00
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Internet Communications Authorized	2016-08-19_Email_Authorization_NETL062C3.pdf	65276 1cc0b3dd0e01d043fdd98fe12d556b728dd61553a	no	2

Warnings:

Information:	
Total Files Size (in bytes):	65276
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.	



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

79141 7590 11/23/2016
Jamie J. Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

EXAMINER

CHERY, MARDOCHEE

ART UNIT

PAPER NUMBER

2133

DATE MAILED: 11/23/2016

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/169,745	06/01/2016	Hyun Lee	NETL062C3	6558

TITLE OF INVENTION: MEMORY MODULE CAPABLE OF HANDSHAKING WITH A MEMORY CONTROLLER OF A HOST SYSTEM

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	02/23/2017

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

79141 7590 11/23/2016
Jamie J. Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/169,745	06/01/2016	Hyun Lee	NETL062C3	6558

TITLE OF INVENTION: MEMORY MODULE CAPABLE OF HANDSHAKING WITH A MEMORY CONTROLLER OF A HOST SYSTEM

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	02/23/2017

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHERY, MARDOCHEE	2133	711-170000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/169,745	06/01/2016	Hyun Lee	NETL.062C3	6558
79141	7590	11/23/2016	EXAMINER	
Jamie J. Zheng, Ph.D Esq. P.O. Box 60573 Palo Alto, CA 94306			CHERY, MARDOCHEE	
			ART UNIT	PAPER NUMBER

2133

DATE MAILED: 11/23/2016

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 15/169,745	Applicant(s) LEE, HYUN	
	Examiner Mardochee CHERY	Art Unit 2133	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 8/3/16.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1-4,7-14,16,17,19-24,26,27,30-35 and 37. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:
a) ☐ All b) ☐ Some *c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)	5. ☐ Examiner's Amendment/Comment
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date <u>8/10/16</u>	6. ☒ Examiner's Statement of Reasons for Allowance
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	7. ☐ Other _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.	

/Mardochee CHERY/ Primary Examiner, Art Unit 2133	11/14/16
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DETAILED ACTION

1. The present application is being examined under the pre-AIA first to invent provisions.

Allowable Subject Matter

2. Claims 1-4, 7-14, 16-17, 19-24, 26-27, 30-35 and 37 are allowed.
3. The following is an examiner's statement of reasons for allowance: the closest prior art does not teach: "a module controller having an open drain output, the module controller generating a parity error signal and driving the parity error signal to the memory controller of the host system via the open drain output while the memory module operates in a first mode, the parity error signal indicating a parity error having occurred in the memory module while the memory module operates in the first mode, wherein the module controller is configured to cause the memory module to enter a second mode in response to a command from the memory controller of the host system, the module controller generating a notification signal indicating at least one status of one or more training sequences while the memory module is in the second mode and outputting the notification signal to the memory controller of the host system via the open drain output while the memory module is in the second mode; and a printed circuit board having a first set of edge connections for communicating address and control signals from the memory controller of the host system, a second set of edge connections for communicating data signals between the memory module and the memory controller of the host system while the memory module operates in the first mode, and an error edge connection coupled to the open drain output of the module controller, the memory

module communicating to the memory controller of the host system via the error edge connection the parity error signal while the memory module operates in the first mode and the notification signal while the memory module is in the second mode.”

4. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mardochee CHERY whose telephone number is (571)272-4246. The examiner can normally be reached on 8:30A-5:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Jared Ian Rutz can be reached on (571)272-5535. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

November 14, 2016

/Mardochee CHERY/
Primary Examiner, Art Unit 2133



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BIB DATA SHEET

CONFIRMATION NO. 6558

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
15/169,745	06/01/2016 RULE	711	2133	NETL.062C3		
APPLICANTS Netlist, Inc., Irvine, CA; INVENTORS Hyun Lee, Ladera Ranch, CA; ** CONTINUING DATA ***** This application is a CON of 15/088,115 04/01/2016 which is a CON of 13/942,721 07/16/2013 PAT 9311116 which is a CON of 12/815,339 06/14/2010 PAT 8489837 which claims benefit of 61/186,799 06/12/2009 ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 06/14/2016						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and /MARDOCHEE Acknowledged CHERY/ Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY CA	SHEETS DRAWINGS 3	TOTAL CLAIMS 37	INDEPENDENT CLAIMS 3
ADDRESS Jamie J. Zheng, Ph.D Esq. P.O. Box 60573 Palo Alto, CA 94306 UNITED STATES						
TITLE MEMORY MODULE CAPABLE OF HANDSHAKING WITH A MEMORY CONTROLLER OF A HOST SYSTEM						
FILING FEE RECEIVED 2960	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.C./

PTO/SB/08a/b(07-09)

Approved for use through 7/31/2012. OMB 0651-0031

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Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Complete if Known	
				Application Number	15/169,745
				Filing Date	June 1, 2016
				First Named Inventor	Hyun Lee
				Art Unit	2133
				Examiner Name	CHERY, MARDOCHEE
Sheet	1	of	1	Attorney Docket Number	NETL.062C3

US PATENT DOCUMENTS					
Examiner Initials *	Cite No. ¹	Document Number	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	1.	US 4672570	06-09-1987	The United States Of America As Represented By The Secretary Of The Air Force	
	2.	US 5511152	04-23-1996	Digital Equipment Corporation	
	3.	US 6763437	07-13-2004	Maxtor Corporation	
	4.	US 7586350	09-08-2009	Hynix Semiconductor Inc.	
	5.	US 20030115427	06-19-2003	Micron Technology, Inc	
	6.	US 20070091702	04-26-2007	Andrey Nikitin	
	7.	US 20080256281	10-16-2008	International Business Machines Corporation	
	8.	US 20090119464	05-07-2009	Grundy Kevin P	
	9.	US 20100042778	02-18-2010	Advanced Micro Devices, Inc.	
	10.	US 20100202240	08-12-2010	Stec, Inc.	
	11.	US 20110022789	01-27-2011	Kabushiki Kaisha Toshiba	

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DATE CONSIDERED 11/14/2016

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patents Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document and WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

Samsung Electronics Co., Ltd.

Ex. 1038, p. 109

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		Number-Kind Code ² (if known)			
	1.	US 7266633	09-04-2007	Micron Technology, Inc.	
	2.	US 7539909	05-26-2009	Intel Corporation	
	3.	US 7065688	06-20-2006	Advanced Micro Devices, Inc.	
	4.	US 5450576	09-12-1995	Ast Research, Inc.	
	5.	US 5684979	11-04-1997	IBM Corporation	
	6.	US 6886109	04-26-2005	Hewlett-Packard Development Company, L.P.	
	7.	US 7024518	04-04-2006	Intel Corporation	
	8.	US 7093115	08-15-2006	Intel Corporation	
	9.	US 7489163	02-10-2009	IBM Corporation	
	10.	US 8429493	04-23-2013	Apple Inc.	
	11.	US 20050071580	03-31-2005	Intel Corporation	
	12.	US 2007/0214347	09-13-2007	Rothman et al.	
	13.	US 20100005218	01-07-2010	IBM Corporation	

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Ex. 1038, p. 110

Issue Classification 	Application/Control No. 15169745	Applicant(s)/Patent Under Reexamination LEE, HYUN	
	Examiner MARDOCHEE CHERY	Art Unit 2133	

CPC						
Symbol					Type	Version
G06F		3		0632	F	2013-01-01
G06F		3		0619	I	2013-01-01
G06F		3		0659	I	2013-01-01
G06F		3		0673	I	2013-01-01
G06F		11		1068	I	2013-01-01
G11C		29		52	I	2013-01-01

CPC Combination Sets						
Symbol			Type	Set	Ranking	Version

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	29	
/MARDOCHEE CHERY/ Primary Examiner.Art Unit 2133	11/14/16	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

Issue Classification 	Application/Control No. 15169745	Applicant(s)/Patent Under Reexamination LEE, HYUN
	Examiner MARDOCHEE CHERY	Art Unit 2133

US ORIGINAL CLASSIFICATION						INTERNATIONAL CLASSIFICATION												
CLASS			SUBCLASS			CLAIMED					NON-CLAIMED							
711			170			G	0	6	F	12 / 00 (2006.01.01)								
CROSS REFERENCE(S)																		
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																	

NONE		Total Claims Allowed:	
		29	
(Assistant Examiner)	(Date)		
/MARDOCHEE CHERY/ Primary Examiner.Art Unit 2133	11/14/16	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

☒ **Claims renumbered in the same order as presented by applicant** ☐ **CPA** ☐ **T.D.** ☐ **R.1.47**

EAST Search History**EAST Search History (Interference)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
		((controller circuit configured cause memory module enter\$3 initialization mode in response command host computer system memory module execut\$3 at least one initialization sequence during initialization mode) and (at least one output\$3 defin\$3 function operational mode according to industry standard but undefined industry standard initialization mode) and (notification circuit output\$3 notification signal indicat\$3 status initialization mode memory controller via least output\$4)).clm.	USPAT	OR	ON	2016/11/14 13:10
		((controller circuit configured cause memory module enter\$3 initialization mode in response command host computer system memory module execut\$3 at least one initialization sequence during initialization mode) and (at least one output\$3 defin\$3 function operational mode according to industry standard but undefined industry standard initialization mode) and (notification circuit output\$3 notification signal indicat\$3 status initialization mode memory controller via least output\$4)).clm.	USPAT	OR	ON	2016/02/18 00:06

11/ 14/ 2016 1:13:06 PM**C:\ Users\ mchery\ Documents\ EAST\ Workspaces\ 13942721.wsp**

<i>Search Notes</i> 	Application/Control No. 15169745	Applicant(s)/Patent Under Reexamination LEE, HYUN
	Examiner MARDOCHEE CHERY	Art Unit 2133

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
711	170	7/25/16	MC

SEARCH NOTES		
Search Notes	Date	Examiner
EAST Search	7/25/16	MC
EAST Updated	11/14/16	MC

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
	See attached	11/14/16	MC

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PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Customer No. 79141

The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15169745	06/01/2016	Hyun Lee	NETL.063C3	6558

TITLE OF INVENTION:

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	undiscounted	\$960	\$0	\$0	\$960	02/23/2017
EXAMINER	ART UNIT	CLASS-SUBCLASS				

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 JAMIE J. ZHENG, Ph.D, Esq.
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE
Netlist, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY)
Irvine, CA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 50-5863 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Jamie J. Zheng/
Typed or printed name Jamie J. Zheng

Date November 23, 2016
Registration No. 51,167

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal				
Application Number:		15169745		
Filing Date:		01-Jun-2016		
Title of Invention:		MEMORY MODULE CAPABLE OF HANDSHAKING WITH A MEMORY CONTROLLER OF A HOST SYSTEM		
First Named Inventor/Applicant Name:		Hyun Lee		
Filer:		Jamie Jie Zheng		
Attorney Docket Number:		NETL.062C3		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				960

Electronic Acknowledgement Receipt	
EFS ID:	27607095
Application Number:	15169745
International Application Number:	
Confirmation Number:	6558
Title of Invention:	MEMORY MODULE CAPABLE OF HANDSHAKING WITH A MEMORY CONTROLLER OF A HOST SYSTEM
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.062C3
Receipt Date:	23-NOV-2016
Filing Date:	01-JUN-2016
Time Stamp:	16:13:00
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$960
RAM confirmation Number	112516INTEFSW16141000
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	2016-11-23_Issue_Fee_Transmittal_NETL062C3.pdf	74223	no	2
			18dba67af780484ea05399f153b47be8e5c440f		
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30596	no	2
			384572983e460251d0d3ec3def20361f4b96888e		
Warnings:					
Information:					
Total Files Size (in bytes):			104819		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

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	2.	US 7539909	05-26-2009	~~Intel Corporation~~	LeClerc et al.
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	6.	US 6886109	04-26-2005	~~Hewlett-Packard Development Company, L.P.~~	Olarig et al.
	7.	US 7024518	04-04-2006	~~Intel Corporation~~	Halbert et al.
	8.	US 7093115	08-15-2006	~~Intel Corporation~~	Poisner et al.
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	10.	US 8429493	04-23-2013	~~Apple Inc.~~	Sokolov et al.
	11.	US 20050071580	03-31-2005	~~Intel Corporation~~	LeClerc et al.
	12.	US 2007/0214347	09-13-2007	Rothman et al.	
	13.	US 20100005218	01-07-2010	~~IBM Corporation~~	Gower et al.

Change(s) applied

to document,

/N.D.W./

11/30/2016

EXAMINER

/Mardochée Chery/

DATE CONSIDERED

11/14/2016

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patents Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document and WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

Samsung Electronics Co., Ltd.

Ex. 1038, p. 122

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		Number-Kind Code ² (if known)			
Change(s) applied to document, A.D.W./ 11/30/2016	1.	US 4672570	06-09-1987	~~The United States Of America As Represented By The Secretary Of The Air Force~~	Benken
	2.	US 5511152	04-23-1996	~~Digital Equipment Corporation~~	Lai et al.
	3.	US 6763437	07-13-2004	~~Maxtor Corporation~~	Nguyen et al.
	4.	US 7586350	09-08-2009	~~Hynix Semiconductor Inc.~~	Chung et al.
	5.	US 20030115427	06-19-2003	~~Micron Technology, Inc.~~	Roohparvar
	6.	US 20070091702	04-26-2007	~~Andrey Nikitin~~	
	7.	US 20080256281	10-16-2008	~~International Business Machines Corporation~~	Fahr et al.
	8.	US 20090119464	05-07-2009	~~Grundy Kevin P~~	
	9.	US 20100042778	02-18-2010	~~Advanced Micro Devices, Inc.~~	Grundy et al.
	10.	US 20100202240	08-12-2010	~~Steep, Inc.~~	Moshagedi et al.
	11.	US 20110022789	01-27-2011	~~Kabushiki Kaisha Toshiba~~	Fujimoto

EXAMINER /Mardochée Chery/

DATE CONSIDERED 11/14/2016

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patents Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document and WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

Samsung Electronics Co., Ltd.

Ex. 1038, p. 123



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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/169,745	01/03/2017	9535623	NETL.062C3	6558

79141 7590 12/14/2016
Jamie J. Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Hyun Lee, Ladera Ranch, CA;
Netlist, Inc., Irvine, CA;

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AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court For the Central District of California, Southern Division on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO. 8:17-cv-1030	DATE FILED 6/14/2017	U.S. DISTRICT COURT Central District of California, Southern Division
PLAINTIFF NETLIST, INC.		DEFENDANT SK HYNIX INC., SK HYNIX AMERICA INC., and SK HYNIX MEMORY SOLUTIONS INC.
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 9,535,623	January 3, 2017	Netlist, Inc.
2 9,606,907	March 28, 2017	Netlist, Inc.
3		
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

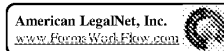
DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading		
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK	
1			
2			
3			
4			
5			

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
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Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy



UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC., SK HYNIX AMERICA, INC., and
SK HYNIX MEMORY SOLUTIONS, INC.
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case IPR2018-00303
Patent 9,535,623 B1

Before STEPHEN C. SIU, MATTHEW R. CLEMENTS, and
SHEILA F. McSHANE, *Administrative Patent Judges*.

CLEMENTS, *Administrative Patent Judge*.

DECISION
Instituting *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

SK Hynix Inc., SK Hynix America Inc., and SK Hynix Memory Solutions Inc. (“Petitioner”) filed a Petition requesting *inter partes* review of claims 1–29 (“the challenged claims”) of U.S. Patent No. 9,535,623 B2 (Ex. 1001, “the ’623 patent”). Paper 1 (“Pet.”). Netlist, Inc. (“Patent Owner”) filed a Preliminary Response. Paper 7 (“Prelim. Resp.”). We review the Petition pursuant to 35 U.S.C. § 314, which provides that an *inter partes* review may be authorized only if “the information presented in the petition . . . and any [preliminary] response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a); 37 C.F.R. § 42.4(a).

Upon consideration of the Petition and the Preliminary Response, we determine that the information presented by Petitioner establishes that there is a reasonable likelihood that Petitioner would prevail in showing the unpatentability of at least one of the challenged claims of the ’623 patent. Accordingly, pursuant to 35 U.S.C. § 314, we institute an *inter partes* review of claims 1–29 of the ’623 patent.

A. Related Proceedings

The ’623 patent is involved in *Netlist, Inc. v. SK Hynix Inc., SK Hynix America Inc., and SK Hynix Memory Solutions Inc.*, Case No. 8:17-cv-01030 (C.D. Ca.) and *In the Matter of Certain Memory Modules and Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1089 (Int’l Trade Comm’n). Pet. 2; Paper 6, 1. The ’623 patent is a continuation of U.S. Patent 8,489,837, which is the subject of, *inter alia*, *SK Hynix Inc. v. Netlist, Inc.*, Case IPR2017-00548, in which a Final Written Decision holding claims

unpatentable over a combination of LeClerg and Lee, and of LeClerg, Lee, and Kim, issued on May 3, 2018. Case IPR2017-00548, Paper 25 (PTAB May 3, 2018).

B. The '623 patent

The '623 patent, titled “Memory Module Capable of Handshaking with a Memory Controller of a Host System,” issued January 3, 2017, from U.S. Patent Application No. 15/169,745. Ex. 1001 at [54], [45], [21]. The '623 patent generally relates to “a memory module capable of handshaking with a memory controller of a host system.” *Id.* at 1:24–26. Figure 3 is reproduced below.

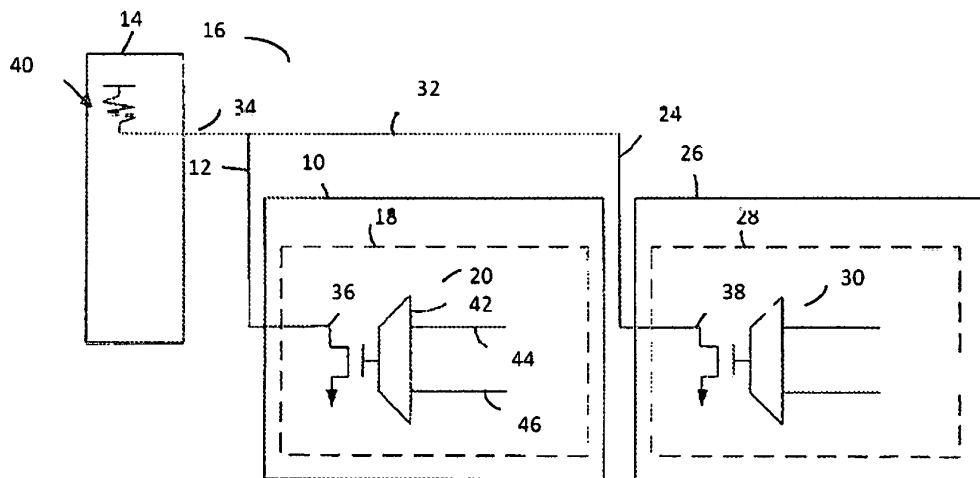


Figure 3

Figure 3 shows a host computer system including first and second memory modules configured to perform handshaking with a memory controller of the host system. *Id.* at 3:27–32. As shown in Figure 3, host computer system 16 includes memory controller 14, which is coupled to memory module 10 and to memory module 26. *Id.* at 5:8–25. “[M]emory module 10 is

configured to operate in at least two modes comprising an initialization mode during which the memory module 10 executes at least one initialization sequence, and an operational mode.” *Id.* Memory module 10 includes controller circuit 18 configured to cause memory module 10 to enter the initialization mode and notification circuit 20 configured to provide a notification signal to memory controller 14 on output 12 while memory module 10 is in initialization mode. *Id.*

“[M]emory module 10 is configured to operate in at least two modes comprising an initialization mode during which the memory module 10 executes at least one initialization sequence, and an operational mode. In one embodiment, for example, the at least one initialization sequence may comprise one or more training sequences.” *Id.* at 6:50–55. “The operational mode is the normal mode of the memory module 10.” *Id.* at 7:29–30.

The status indicated by the notification signal may be, in certain embodiments, execution of the initialization sequence or completion of the initialization sequence. *Id.* at 7:48–8:10.

As shown in Figure 3, output 12 is operatively coupled to an error-out pin of memory module 10 and multiplexor 42 drives transistor 36 with either task_in_progress signal 44 or error signal 46 (e.g., parity error signal). *Id.* at 12:2–6. For example, multiplexor 42 may be configured to drive transistor 36 with task_in_progress signal 44 when memory module 10 is in initialization mode or is executing the at least one initialization sequence, and with error signal 46 when memory module 10 is in operational mode. *Id.* at 12:6–12. “Thus, the memory module 10 can be advantageously configured to both perform the standard (e.g., JEDEC-specified) error reporting functionality via the error-out pin during the operational mode and

provide the status notification functionality during the system initialization mode, as described herein.” *Id.* at 12:12–17.

C. Illustrative Claim

Of the challenged claims, claims 1, 12, and 21 are independent, claims 2–11 depend, directly or indirectly, from claim 1, claims 13–20 depend, directly or indirectly, from claim 12, and claims 22–29 depend, directly or indirectly, from claim 21. Independent claim 1 is illustrative of the challenged claims and is reproduced below:

1. A memory module configured to fit into a corresponding slot of a host system to operate with a memory controller of the host system, the memory module comprising:

a module controller having an open drain output, the module controller generating a parity error signal and driving the parity error signal to the memory controller of the host system via the open drain output while the memory module operates in a first mode, the parity error signal indicating a parity error having occurred in the memory module while the memory module operates in the first mode, wherein the module controller is configured to cause the memory module to enter a second mode in response to a command from the memory controller of the host system, the module controller generating a notification signal indicating at least one status of one or more training sequences while the memory module is in the second mode and outputting the notification signal to the memory controller of the host system via the open drain output while the memory module is in the second mode; and

a printed circuit board having a first set of edge connections for communicating address and control signals from the memory controller of the host system, a second set of edge connections for communicating data signals between the memory module and the memory controller of the host system while the memory module operates in the first mode, and an error edge connection coupled to the open drain output of the module

controller, the memory module communicating to the memory controller of the host system via the error edge connection the parity error signal while the memory module operates in the first mode and the notification signal while the memory module is in the second mode.

Ex. 1001, 15:26–58.

D. Evidence Relied Upon

Petitioner relies upon the following prior art references:

Hazelzet	US 2008/0098277 A1	Apr. 24, 2008	Ex. 1014
Amidi	US 2008/0155378 A1	June 26, 2008	Ex. 1015
Talbot	US 2008/0147897 A1	June 19, 2008	Ex. 1016
Buchmann	US 8,139,430 B2	Mar. 20, 2012	Ex. 1017
Hokenmaier	US 7,525,860 B2	Apr. 28, 2009	Ex. 1018
Kim	US 8,359,521 B2	Jan. 22, 2013	Ex. 1019

Pet. 3–4. Petitioner also relies upon the Declaration of Dr. Donald Alpert (Ex. 1003). Patent Owner relies upon the Declaration of Robert J. Murphy (Ex. 2001).

E. Asserted Grounds of Unpatentability

Petitioner asserts that the challenged claims are unpatentable based on the following grounds (Pet. 4):

Reference(s)	Basis	Claims challenged
Hazelzet	§ 103	1–29
Hazelzet and Amidi	§ 103	1–29
Hazelzet and Talbot	§ 103	1–29
Hazelzet and Buchmann	§ 103	1–29
Hazelzet and Hokenmaier, with or without Amidi, Talbot, or Buchmann	§ 103	8, 9, 19, 20, 25, and 26

Hazelzet and Kim, with or without Amidi, Talbot, or Buchmann	§ 103	10, 15, and 27
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II. ANALYSIS

A. Claim Construction

In an *inter partes* review, a claim in an unexpired patent shall be given its broadest reasonable construction in light of the specification of the patent in which it appears. 37 C.F.R. § 42.100(b). Under the broadest reasonable construction standard, claim terms are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Any special definition for a claim term must be set forth in the specification with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994). We must be careful not to read a particular embodiment appearing in the written description into the claim if the claim language is broader than the embodiment. *See In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993). Only terms that are in controversy need to be construed, and then only to the extent necessary to resolve the controversy. *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

Petitioner proposes that we construe “mode,” “notification signal,” “training,” and “indicating . . . status.” Pet. 8–15. Patent Owner does not propose any constructions explicitly for any claim terms. Prelim. Resp. *passim*. On this record, we determine that no terms require express construction for purposes of this Decision.

B. Obviousness over Hazelzet and Buchmann

Petitioner argues that the claims 1–29 are unpatentable under 35 U.S.C. § 103(a) as obvious over the combination of Hazelzet and Buchmann. Pet. 57–61. In light of the arguments and evidence of record, we are persuaded that Petitioner has established a reasonable likelihood that claims 1 is unpatentable as obvious over the combination of Hazelzet and Buchmann.

1. Hazelzet (Ex. 1014)

Hazelzet is directed to a “high density high reliability memory controller/interface module.” Ex. 1014 ¶ 7. Specifically, Hazelzet “describes a unique DIMM having an enhanced 4 rank-enabled 28 bit 1:2 register with added error correction code logic (ECC) incorporated therein for correcting single bit errors while permitting continuous memory operation independent of the existence of these errors.” *Id.* ¶ 64. “A parity operating mode is also provided, in conjunction with error reporting circuitry to permit the system to interrogate the device to determine the error condition.” *Id.*

2. Buchmann (Ex. 1017)

Buchmann relates to power-on initialization and training sequences, such as using a static bit communication (SBC) mode to provide improvements in the overall training sequence. Ex. 1017, 3:50–54. Talbot describes memory module 110s, each with a memory buffer 106, arranged in a cascaded interconnect memory system. *Id.* at 4:5–8, 4:14–15, Fig. 1. Talbot teaches “training states” TS0 to TS7. *Id.* at 5:40–50. The host memory controller (“HMC”) communicates with memory buffers 106

(“MB”) regarding the status of the memory modules’ training states. For example:

[T]hen the HMC initiates a TS0b state which drives a TS0a state to MB0. When MB0 has completed the TS0a state processing it *returns a handshake (e.g., via SBC) to the HMC to let it know that TS0a has been completed and the status (e.g., successful).* Then the HMC initiates a TS0c state which drives a TS0b state to MB0, in turn MB0 drives a TS0a state to MB1. TS0 processing continues as depicted in FIG. 4 until the TS0b state has been completed on MB3 and there is no downstream MB for the TS0b to initiate a TS0a on. *When this occurs, the TS0d state is initiated on MB3 and then a handshake occurs between each MB back to the HMC.* The HMC then enters TS1 or TS2.

Id. at 6:58–7:2 (emphasis added).

3. Analysis

Claim 1 recites a “memory module configured to fit into a corresponding slot of a host system to operate with a memory controller of the host system, the memory module comprising.” Petitioner relies upon Hazelzet’s dual inline memory module (“DIMM”). Pet. 20–23.

Claim 1 also recites “a module controller having an open drain output.” Petitioner relies upon Hazelzet’s ECC/Parity Register 21 as the “module controller” and output /ERROR (UE) 121 as the “open drain output.” Pet. 23–25.

Claim 1 also recites “the module controller generating a parity error signal and driving the parity error signal to the memory controller of the host system via the open drain output while the memory module operates in a first mode.” Petitioner relies upon Hazelzet’s parity mode as the recited “first mode.” Pet. 25. According to Petitioner, “[w]hen the memory module is in the ‘parity mode,’ the ‘parity generator/checker circuit 231’ [of

SEC/DED ECC 90 of ECC/Parity Buffer chip 21] generates and sends the ‘parity error signal (PERR)’ to the ‘error logic circuit’ 100.” Pet. 27 (citing Ex. 1014 ¶¶ 70, 76, Figs. 4B, 5; Ex. 1003 ¶ 132). After that, according to Petitioner, “the ‘parity error signal (PERR)’ 111 that is fed into the ‘error logic circuit’ 100 is output to the memory controller through the output line 121 (*i.e.*, output for uncorrectable error ‘UE’),” which Petitioner identifies as the recited “open drain output” and which is coupled to the host memory controller using pin number 142. *Id.*

Claim 1 also recites “the parity error signal indicating a parity error having occurred in the memory module while the memory module operates in the first mode.” Petitioner relies upon Hazelzet’s teaching that parity error signal 111 indicates a parity error having occurred in the memory module while the module operates in parity mode. Pet. 27 (citing Ex. 1014 ¶¶ 18, 64, 70, 107, 99, Fig. 8; Ex. 1003 ¶¶ 136, 137).

Claim 1 also recites “wherein the module controller is configured to cause the memory module to enter a second mode in response to a command from the memory controller of the host system.” Petitioner relies upon Hazelzet’s ECC mode as the recited “second mode.” Pet. 28. For causing the memory module to enter ECC mode, Petitioner asserts that Hazelzet’s memory module can be in ECC mode only “when at least one of the ‘chip select’ commands from the memory controller of the host system is ‘active low.’” *Id.* at 29. Petitioner also relies, alternatively, upon Hazelzet’s teaching that its memory module is in ECC mode when the “/ECC Mode” signal goes low and is in parity mode when the “/ECC Mode” signal goes high. *Id.* (citing Ex. 1014 ¶¶ 62, 69, 70, Fig. 4B; Ex. 1003 ¶ 143).

Claim 1 also recites “the module controller generating a notification signal indicating at least one status of one or more training sequences while the memory module is in the second mode” and “outputting the notification signal to the memory controller of the host system via the open drain output while the memory module is in the second mode.” Petitioner asserts that Hazelzet teaches this limitation because, in ECC mode, the notification signal output to the host memory controller on open-drain output line 121 “indicates the status of the error correction sequence” by indicating whether an error was identified and whether the error is an uncorrectable error. Pet. 30. Petitioner asserts, however, that to the extent Hazelzet’s notification signal does not indicate the status of a “training sequence,” that element is taught by Buchmann because Buchmann teaches an “SBC mode” in which memory modules execute training and/or initialization sequences . *Id.* at 61–62. Petitioner identifies signal TS3 as “an example of Buchmann’s training,” and argues during TS3, “the memory module generates and outputs various notification signals indicating the status of the TS3 training sequence to the memory controller of the host system.” *Id.* at 62 (citing Ex. 1017, 8:24–9:18, Table 5, Table 6, Fig. 6; Ex. 1003 ¶ 169).

With respect to combining Buchmann and Hazelzet, Petitioner asserts that “Buchmann explains that ‘multi-drop bus(es) or other shared or parallel bus(es)’ can be used for such notification . . . and therefore one would have found it obvious to implement such notification using the open drain outputs in Hazelzet.” *Id.* (citation omitted). Petitioner argues that Hazelzet and Buchmann are analogous art, and that the combination would “be merely an arrangement of old elements with each performing the same function it had been known to perform and yielding no more than what one would expect

from such an arrangement.” *Id.* at 63. Petitioner also asserts that the training scheme of Buchmann would enhance reliability of the overall system of Hazelzet and because “one skilled in the art would have known that memory systems are initialized before normal operation.” *Id.* at 63–64. As a result, “one skilled in the art would have been motivated to initialize the memory system of Hazelzet using the initialization/error correction schemes of Buchmann.” *Id.* at 64.

Claim 1 also recites (emphasis added)

a printed circuit board having a first set of edge connections for communicating *address and control* signals from the memory controller of the host system, a second set of edge connections for communicating *data* signals between the memory module and the memory controller of the host system while the memory module operates in the first mode, and an error edge connection coupled to the open drain output of the module controller.

Petitioner relies upon Hazelzet’s teaching that the “DIMM of the present invention is comprised of a printed circuit board” (Ex. 1014 ¶ 15) with connectors 23 along the edge of both the back and front sides of the board. Pet. 33 (citing Ex. 1014 ¶¶ 38, 68, 72, Figs. 2, 7A–C). For an error edge connection coupled to the open drain output, Petitioner relies upon Hazelzet’s teaching of “[t]wo open-drain outputs are available to permit multiple modules to share a common signal line for reporting an error that occurred during a valid command.” Ex. 1014 ¶ 72.

Claim 1 also recites “the memory module communicating to the memory controller of the host system via the error edge connection the parity error signal while the memory module operates in the first mode and the notification signal while the memory module is in the second mode.” Petitioner relies upon Hazelzet’s teaching of communicating, in the parity

mode, parity error signal (PERR) 111 to the memory controller of the host via open-drain output line 121 (i.e., the output for uncorrectable error “UE”), and, in ECC mode, a notification signal output to the memory controller of the host via open-drain output line 121. Pet. 34.

Notwithstanding Patent Owner’s arguments, which we have considered and which we address below, we are persuaded, on this record, that claim 1 is unpatentable under 35 U.S.C. § 103(a) as obvious over the combination of Hazelzet and Buchmann.

Patent Owner argues that the details of how Hazelzet and Buchmann would be combined “were unclear in the Petition” because it is not clear whether Petitioner is proposing to incorporate Hazelzet into Buchmann or vice-versa. Prelim. Resp. 43–47. On this record, we disagree. We understand Petitioner to be relying upon the combined teachings of both references. To the extent Patent Owner is arguing that it is not clear whether the notification circuitry of Hazelzet would be bodily incorporated into Buchmann’s DIMM or the training sequences of Buchmann’s DIMM bodily incorporated into Hazelzet’s DIMM, that argument is not persuasive. “The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference Rather, the test is what the combined teachings of those references would have suggested to those of ordinary skill in the art.” *In re Keller*, 642 F.2d 413, 425 (CCPA 1981); *see also In re Sneed*, 710 F.2d 1544, 1550 (Fed. Cir. 1983) (“[I]t is not necessary that the inventions of the references be physically combinable to render obvious the invention under review.”); and *In re Nievelt*, 482 F.2d 965, 968 (CCPA 1973) (“Combining the *teachings* of references does not involve an ability to combine their specific structures.”).

Rather, “if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007).

Patent Owner also argues that a person of ordinary skill in the art would not have combined the teachings of Hazelzet and Buchmann upon which Petitioner relies because there are “fundamentally different design purposes between Hazelzet’s ECC MODE UE signal line 121 and Buchmann’s TS3 commands.” Prelim. Resp. 47. Specifically, Patent Owner argues that the former is for error reporting, whereas the latter is for commanding operations. *Id.* at 47–48. Similarly, Patent Owner argues that there are “fundamentally different hardware implementations” because, *inter alia*, Hazelzet’s ECC MODE UE signal line 121 is a 1-bit signal, whereas Buchmann’s TS3 commands are 6-bit commands. *Id.* at 48 (citing Ex. 1017, Fig. 11, Table 11); *see also id.* at 49–53 (analogizing Hazelzet’s UE signal to a check engine light and Buchmann’s TS3 commands to diagnostic codes). On this record, these arguments are not persuasive because they go to implementation details that are not essential to the proposed combination. The relevant aspect of Buchmann is that it teaches a notification signal indicating a status of a training sequence. Although Buchmann’s TS3 commands are implemented as 6-bit signals, we are persuaded, on this record, that it was within the ordinary level of skill in the art to implement a notification signal that performs the same function using only 1-bit and to communicate that 1-bit notification signal on Hazelzet’s UE output 121.

We also have reviewed Petitioner's contentions with respect to claims 2–29 and are persuaded that the evidence, on this record, supports Petitioner's contentions. Patent Owner argues that dependent claims 3, 4, 14, and 22 are not taught by Hazelzet alone (Prelim. Resp. 19–22), but those arguments are not persuasive because they do not address the proposed combination with Buchmann.

4. Conclusion

On this record, we are persuaded that Petitioner has established a reasonable likelihood that it would prevail in showing that claims 1–29 are unpatentable as obvious over the combination of Hazelzet and Buchmann.

C. Other Grounds

Petitioner also alleges that (1) claims 1–29 are unpatentable under § 103 as obvious over Hazelzet; (2) claims 1–29 are unpatentable under § 103 as obvious over the combination of Hazelzet and Amidi; (3) claims 1–29 are unpatentable under § 103 as obvious over the combination of Hazelzet and Talbot; (4) claims 8, 9, 19, 20, 25, and 26 are unpatentable under § 103 as obvious over the combination of Hazelzet and Hokenmaier, with or without Amidi, Talbot, or Buchmann; and (5) claims 10, 15, and 27 are unpatentable under § 103 as obvious over the combination of Hazelzet and Kim, with or without Amidi, Talbot, or Buchmann.

On this record, we are not persuaded that Hazelzet alone teaches or suggests the recited “training sequence.” Specifically, we are not persuaded that “the status of the error correction sequence when the memory module is in the ‘ECC mode,’” as relied upon by Petitioner, teaches (Pet. 30) or suggests (*id.* at 31–32) the recited training sequence. As a result, Petitioner

has not established a reasonable likelihood that claims 1–29 would have been obvious over Hazelzet alone.

We are persuaded, however, that each of Amidi and Talbot teach the recited “training sequence.” Pet. 51–53 (relying upon Amidi’s second mode), 57–58 (relying upon Talbot’s training mode). As a result, Petitioner has established a reasonable likelihood that claims 1–29 would have been obvious over the combination of Hazelzet and Amidi and over the combination of Hazelzet and Talbot.

Moreover, we are persuaded that Hokenmaier teaches the additional limitations recited in claims 8, 9, 19, 20, 25, and 26, and we are persuaded that Kim teaches the additional limitation recited in claims 10, 15, and 27. As a result, Petitioner has established a reasonable likelihood that that claims 8, 9, 19, 20, 25, and 26 would have been obvious over the combination of Hazelzet, Amidi, and Hokenmaier, the combination of Hazelzet, Talbot, and Hokenmaier, and the combination of Hazelzet, Buchmann, and Hokenmaier. Similarly, Petitioner has established a reasonable likelihood that claims 10, 15, and 27 would have been obvious over the combination of Hazelzet, Amidi, and Kim, the combination of Hazelzet, Talbot, and Kim, and the combination of Hazelzet, Buchmann, and Kim.

D. Institution

On April 24, 2018, the Supreme Court held that a decision to institute under 35 U.S.C. § 314 may not institute on less than all claims challenged in the petition. *SAS Inst., Inc. v. Iancu*, 2018 WL 1914661, at *10 (U.S. Apr. 24, 2018). After considering the evidence and arguments presented in the Petition and Preliminary Response, we determine that Petitioner has demonstrated a reasonable likelihood of success in proving that at least

IPR2018-00303
Patent 9,535,623 B1

claim 1 of the '623 patent is unpatentable. Accordingly, an *inter partes* review of all challenged claims and all grounds presented in the Petition is hereby instituted.

III. CONCLUSION

For the foregoing reasons, we are persuaded that Petitioner has demonstrated that there is a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of claim 1 of the '623 patent. At this stage of the proceeding, we have not made a final determination with respect to the patentability of the challenged claims or to the construction of any claim term.

IV. ORDER

Accordingly, it is

ORDERED that pursuant to 35 U.S.C. § 314, an *inter partes* review of claims 1–29 of the '623 patent is instituted with respect to all grounds set forth in the Petition; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, *inter partes* review of the '623 patent shall commence on the entry date of this Order, and notice is hereby given of the institution of a trial.

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Patent 9,535,623 B1

For PETITIONER:

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC., SK HYNIX AMERICA INC., AND SK HYNIX MEMORY
SOLUTIONS INC.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case IPR2018-00303
Patent 9,535,623 B1

NETLIST, INC.'S NOTICE OF APPEAL

via E2E
Patent Trial and Appeal Board

via Hand Carry
Director of the United States Patent and Trademark Office
c/o Office of the General Counsel, 10B20
Madison Building East
600 Dulany Street
Alexandria, VA 22314

via CM/ECF
United States Court of Appeals for the Federal Circuit

OFFICE OF THE GENERAL COUNSEL
2019 MAY 22 PM 2:15
US PATENT AND
TRADEMARK OFFICE

la-1418438

INTRODUCTION

Netlist, Inc.'s appeal stems from the Patent Trial and Appeal Board's Final Written Decision entered on March 21, 2019 (Paper 42) (the "Final Written Decision") in the above-captioned *inter partes* review of United States Patent No. 9,535,623 B1 ("the '623 patent"). This notice is timely filed within 63 days of the Board's Final Written Decision. 37 C.F.R. § 90.3(a)(1).

NETLIST, INC.'S APPEAL

Please take notice that under 35 U.S.C. §§ 141(c), 142, 319; 37 C.F.R. §§ 90.2(a), 90.3; and Federal Rule of Appellate Procedure/Federal Circuit Rule 15, Patent Owner Netlist, Inc. hereby appeals to the United States Court of Appeals for the Federal Circuit from the Final Written Decision and all underlying decisions and orders in this action on which that decision is based.

NETLIST, INC.'S ISSUES ON APPEAL

In accordance with 37 C.F.R. § 90.2(a)(3)(ii), Netlist, Inc.'s issues on appeal include at least:

(i) the Board's finding that claims 1-29 of the '623 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over Hazelzet (U.S. Patent Application Publication No. 2008/0098277) and any one of Buchmann (U.S. Patent No. 8,139,430) or Talbot (U.S. Patent Application Publication No. 2008/0147897); claims 8, 9, 19, 20, 25 and 26 are unpatentable under 35 U.S.C. § 103(a) over

Hazelzet, Hokenmaier (U.S. Patent No 7,525,860) and any one of Buchmann or Talbot; and claims 10, 15, and 27 are unpatentable under 35 U.S.C. § 103(a) over Hazelzet, Kim (U.S. Patent No. 8,359,521) and any one of Buchmann or Talbot; and

(ii) any findings or determinations supporting or related to the aforementioned issues as well as all other issues decided adversely to Netlist, Inc. in any orders, decisions, rulings, or opinions.

Simultaneously with this submission, Netlist, Inc. is filing a true and correct copy of this Notice of Appeal with the Director of the United States Patent and Trademark Office and a true and correct copy (or copies) of the same, along with the required filing fee, with the Clerk of the United States Court of Appeals for the Federal Circuit as set forth in the accompanying Certificate of Filing.

Dated: May 22, 2019

Respectfully submitted,

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CERTIFICATE OF FILING

The undersigned hereby certifies that, in addition to being electronically filed through E2E, a true and correct copy of the above-captioned NETLIST, INC.'S NOTICE OF APPEAL is being filed by hand with the Director on May 22, 2019, at the following address:

Director of the United States Patent and Trademark Office
c/o Office of the General Counsel, 10B20
Madison Building East
600 Dulany Street
Alexandria, VA 22314

The undersigned also hereby certifies that a true and correct copy of the above-captioned NETLIST, INC.'S NOTICE OF APPEAL and the filing fee is being filed via CM/ECF with the Clerk's Office of the United States Court of Appeals for the Federal Circuit on May 22, 2019.

Dated: May 22, 2019

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CERTIFICATION OF SERVICE

The undersigned hereby certifies that the foregoing NETLIST, INC.'S
NOTICE OF APPEAL was served electronically via e-mail on May 22, 2019, by
agreement of the parties, in its entirety on the following:

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC., SK HYNIX AMERICA INC., and SK HYNIX
MEMORY SOLUTIONS INC.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case IPR2018-00303
Patent 9,535,623 B1

Before STEPHEN C. SIU, BRYAN F. MOORE, and
SHEILA F. MCSHANE, *Administrative Patent Judges*.

SIU, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a)

I. INTRODUCTION

We have jurisdiction to hear this *inter partes* review under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons discussed herein, we determine that Petitioner has shown, by a preponderance of the evidence, that claims 1–29 (“the challenged claims”) of U.S. Patent No. 9,535,623 B1 (Ex. 1001, “the ’623 patent”) are unpatentable.

BACKGROUND

SK Hynix Inc., SK Hynix America Inc., and SK Hynix Memory Solutions Inc. (collectively, “Petitioner”) filed a Petition (Paper 1), with the supporting Declaration of Dr. Donald Alpert (Ex. 1003). Netlist, Inc. (“Patent Owner”) filed a Preliminary Response (Paper 7), with the supporting Declaration of Robert J. Murphy (Ex. 2001). We instituted an *inter partes* review of all challenged claims (claims 1–29) of the ’623 patent. Paper 8. Patent Owner filed a Patent Owner Response (Paper 14, “PO Resp.”), with the Supplemental Declaration of Robert J. Murphy (Ex. 2005). Petitioner filed a Petitioner Reply (Paper 23, “Pet. Reply”).

Patent Owner filed a Motion to Exclude (Paper 30), Petitioner filed an Opposition to Patent Owner’s Motion to Exclude (Paper 33), and Patent Owner filed a Reply to Petitioner’s Opposition (Paper 36).

Petitioner filed a Motion to Exclude (Paper 25), Patent Owner filed an Opposition (Paper 34), and Petitioner filed a Reply to Patent Owner’s Opposition (Paper 35).

An oral hearing was held on February 6, 2019. A transcript of the hearing is included in the record. Paper 41.

RELATED PROCEEDINGS

The '623 patent is involved in *Netlist, Inc. v. SK Hynix Inc., SK Hynix America Inc., and SK Hynix Memory Solutions Inc.*, Case No. 8:17-cv-01030 (C.D. Cal.) and *In the Matter of Certain Memory Modules and Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1089 (Int'l Trade Comm'n). Pet. 2; Paper 6, 1. The '623 patent is a continuation of U.S. Patent No. 8,489,837, which is the subject of, *inter alia*, *SK Hynix Inc. v. Netlist, Inc.*, Case IPR2017-00548, in which a Final Written Decision holding claims unpatentable as obvious, issued on May 3, 2018. Case IPR2017-00548, Paper 25 (PTAB May 3, 2018).

THE '623 PATENT (EXHIBIT 1001)

The '623 patent, titled "Memory Module Capable of Handshaking with a Memory Controller of a Host System," issued January 3, 2017, from U.S. Patent Application No. 15/169,745. Ex. 1001 at [54], [45], [21]. The '623 patent describes a memory module and a memory controller of a host system. *Id.* at 1:25–26. Figure 3 is reproduced below.

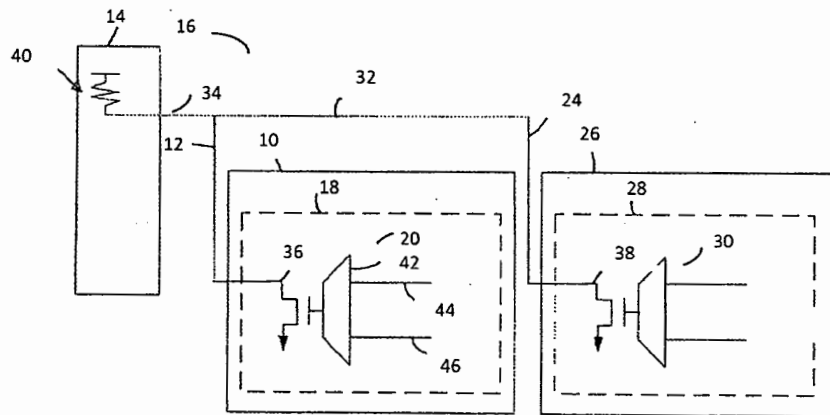


Figure 3

Figure 3 shows a host computer system including first and second memory modules configured to perform handshaking with a memory controller of the host system. Ex. 1001, 3:27–32. As shown in Figure 3, host computer system 16 includes memory controller 14, which is coupled to memory module 10 and to memory module 26. *Id.* at 5:8–25. “[M]emory module 10 is configured to operate in at least two modes comprising an initialization mode during which the memory module 10 executes at least one initialization sequence, and an operational mode.” *Id.* Memory module 10 includes controller circuit 18 configured to cause memory module 10 to enter the initialization mode and notification circuit 20 configured to provide a notification signal to memory controller 14 on output 12 while memory module 10 is in initialization mode. *Id.*

In one embodiment, for example, the at least one initialization sequence may comprise one or more training sequences.” Ex. 1001, 6:50–55. “The operational mode is the normal mode of the memory module 10.” *Id.* at 7:29–30. The status indicated by the notification signal may be, in certain embodiments, execution of the initialization sequence or completion of the initialization sequence. *Id.* at 7:48–8:10.

As shown in Figure 3, output 12 is operatively coupled to an error-out pin of memory module 10 and multiplexor 42 drives transistor 36 with either task_in_progress signal 44 or error signal 46 (e.g., parity error signal). *Id.* at 12:2–6. For example, multiplexor 42 may be configured to drive transistor 36 with task_in_progress signal 44 when memory module 10 is in initialization mode or is executing the at least one initialization sequence, and with error signal 46 when memory module 10 is in operational mode. *Id.* at 12:6–12. “Thus, the memory module 10 can be advantageously

configured to both perform the standard (e.g., JEDEC-specified) error reporting functionality via the error-out pin during the operational mode and provide the status notification functionality during the system initialization mode.” *Id.* at 12:12–17.

ILLUSTRATIVE CLAIM

Of the challenged claims, claims 1, 12, and 21 are independent; claims 2–11 depend, directly or indirectly, from claim 1; claims 13–20 depend, directly or indirectly, from claim 12; and claims 22–29 depend, directly or indirectly, from claim 21. Claim 1, reproduced below, is illustrative of the claimed subject matter:

1. A memory module configured to fit into a corresponding slot of a host system to operate with a memory controller of the host system, the memory module comprising:

a module controller having an open drain output, the module controller generating a parity error signal and driving the parity error signal to the memory controller of the host system via the open drain output while the memory module operates in a first mode, the parity error signal indicating a parity error having occurred in the memory module while the memory module operates in the first mode, wherein the module controller is configured to cause the memory module to enter a second mode in response to a command from the memory controller of the host system, the module controller generating a notification signal indicating at least one status of one or more training sequences while the memory module is in the second mode and outputting the notification signal to the memory controller of the host system via the open drain output while the memory module is in the second mode; and

a printed circuit board having a first set of edge connections for communicating address and control signals from the memory controller of the host system, a second set of edge connections for communicating data signals between the memory module and the memory controller of the host system

while the memory module operates in the first mode, and an error edge connection coupled to the open drain output of the module controller, the memory module communicating to the memory controller of the host system via the error edge connection the parity error signal while the memory module operates in the first mode and the notification signal while the memory module is in the second mode.

Id. at 15:26–58.

INSTITUTED GROUNDS

We instituted trial on the following grounds of unpatentability: claims 1–29 as unpatentable under 35 U.S.C. § 103 over Hazelzet,¹ alone or in combination with any one of Amidi² Talbot,³ or Buchmann;⁴ claims 8, 9, 19, 20, 25, and 26 as unpatentable under 35 U.S.C. § 103 over Hazelzet and Hokenmaier,⁵ with or without Amidi, Talbot, or Buchmann; and claims 10, 15, and 27 under 35 U.S.C. § 103 over Hazelzet and Kim,⁶ with or without Amidi, Talbot, or Buchmann. Pet. 3–4.

II. ANALYSIS

THE PARTIES' POST-INSTITUTION ARGUMENTS

In our Decision on Institution, we concluded that the arguments and evidence advanced by Petitioner demonstrated a reasonable likelihood that

¹ US Patent Publication 2008/0098277 A1, dated April 24, 2008 (Ex. 1014, “Hazelzet”).

² US Patent Publication 2008/0155378 A1, published June 26, 2008 (Ex. 1015, “Amidi”).

³ US Patent Publication 2008/0147897 A1, published June 19, 2008 (Ex. 1016, “Talbot”).

⁴ US Patent 8,139,430 B2, issued March 20, 2012 (Ex. 1017, “Buchmann”).

⁵ US Patent 7,525,860 B2, issued April 28, 2009 (Ex. 1018, “Hokenmaier”).

⁶ US Patent 8,359,521 B2, issued January 22, 2013 (Ex. 1019, “Kim”).

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claims 1–29 of the '623 patent would have been unpatentable under 35 U.S.C. § 103 based on certain asserted grounds of unpatentability. Dec. 6–17. We now determine whether Petitioner has established by a preponderance of the evidence that claims 1–29 are unpatentable over the asserted prior art. 35 U.S.C. § 316(e). We previously instructed Patent Owner that “any arguments for patentability not raised and fully briefed in the response will be deemed waived.” Paper 9, 3; *see also* 37 C.F.R. § 42.23(a) (“Any material fact not specifically denied may be considered admitted.”); *In re NuVasive, Inc.*, 842 F.3d 1376, 1379–82 (Fed. Cir. 2016) (holding patent owner waived an argument addressed in Preliminary Response by not raising the same argument in the Patent Owner Response). Additionally, the Board’s Trial Practice Guide states that the Patent Owner Response “should identify all the involved claims that are believed to be patentable and state the basis for that belief.” Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,766 (Aug. 14, 2012).

With a complete record before us, we note that we have reviewed all of the arguments and evidence advanced by Petitioner to support its unpatentability contentions, including arguments and evidence addressing limitations Patent Owner chose not to address in its Patent Owner Response. Based on the preponderance of the evidence before us, we conclude that certain asserted obviousness grounds render unpatentable claims 1–29 of the '623 patent.

OBVIOUSNESS OVER HAZELZET AND ONE OF BUCHMANN OR TALBOT

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that

the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness.⁷ *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

Person of Ordinary Skill in the Art

Petitioner's expert, Dr. Alpert, testifies that one of ordinary skill in the art would be someone who was familiar with computer memory systems and basic CPU architecture, which includes knowledge of techniques related to how computer components access a computer's memory, including the role of a memory controller, the basic operation of memory modules and devices, and the techniques used to couple memory, as well as applicable standards. Ex. 1003 ¶ 43; *see also* Pet. 4–5 (providing further explanation). Dr. Alpert also testifies that a person of ordinary skill in the art would have had a bachelor's degree in computer engineering, or a related field, and several years of additional experience working with computer memory systems. *Id.* Patent Owner's expert, Mr. Murphy, agrees with Petitioner's proposed qualifications. Ex. 2001 ¶¶ 18–19.

We adopt the parties' agreed-upon qualifications. In addition, we note that the art of record in this proceeding and addressed here—including,

⁷ Patent Owner has not argued that there are objective indicia of nonobviousness.

Hazelzet, Buchmann, and Talbot—is indicative of the level of ordinary skill in the art. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

Independent Claims

We will address claim 1 as representative of the independent claims. Claim 1 recites a memory module configured to fit into a corresponding slot of a host system to operate with a memory controller of the host system. Petitioner argues that the combination of Hazelzet and one of Buchmann or Talbot discloses this feature. Pet. 15–16, 18–23. For example, Petitioner explains that Hazelzet discloses “dual inline memory modules (DIMM) that are configured to operate with the ‘memory controller’ of the host system.” *Id.* at 20 (citing Ex. 1014, Fig. 2, ¶¶ [0036]–[0038]; Ex. 1003 ¶ 122). We agree with Petitioner’s showing that Hazelzet teaches this recitation.

Claim 1 recites that the module controller generates and drives “a parity error signal” to the memory controller of the host system via an open drain output when operating in a first mode. Petitioner argues that the combination of Hazelzet and one of Buchmann or Talbot discloses this feature. Pet. 23–27. For example, Petitioner explains that Hazelzet discloses “an ‘ECC/Parity register’ (*‘module controller’*) [also referred to as a “buffer device”] having an output (*‘open drain output’*)” that “operate[s] in . . . a ‘parity mode,’ which is the claimed *‘first mode (or state)’*” in which “error reporting circuitry” reports “correctable” and “uncorrectable errors.” *Id.* at 24–25 (citing Ex. 1014, Figs. 3A–3D, 4A, 4B, 5, 8, ¶¶ [0020], [0022], [0027]–[0028], [0049], [0059]–[0062], [0064], [0069]–[0070], [0072], [0075], [0081], [0101]–[0103], [0106]–[0107], [0109]; Ex. 1003 ¶¶ 127–128, 130). We agree with Petitioner that Hazelzet teaches this claim limitation.

Claim 1 recites the memory module entering “a second mode in response to a command from the memory controller of the host system.” Petitioner argues that the combination of Hazelzet and one of Buchmann or Talbot discloses this feature. Pet. 28–29. For example, as Petitioner explains, Hazelzet discloses a memory module (or “buffer device”) that operates “in (1) a ‘parity mode,’ which is the claimed ‘*first mode*,’ and (2) an ‘ECC mode,’ which is the claimed ‘*second mode*’” and that a “chip select” command “from the memory controller of the host system” “cause[s] the memory module to enter an ‘ECC mode.’” *Id.* (citing Ex. 1014 Fig. 4A, 7B, ¶¶ [0027], [0066], [0074], [0104]; Ex. 1003 ¶ 141). Hence, one of skill in the art would have understood Hazelzet to teach a memory module that operates in different “modes” based on commands from a memory controller of a host system.

As Petitioner also points out, and we agree, Buchmann discloses a memory module (or “memory buffer”) that communicates with a “memory controller” of a host system in which the memory module operates in “two modes of operation” (“SBC mode” and “high-speed mode”), and Talbot discloses “normal operation (*i.e.*, ‘read and write operations’)” and a “training mode.” Pet. 57–58, 61–62 (citing Ex. 1016 ¶¶ [0049], [0052], [0053], [0089]; Ex. 1017, Abstract, 1:39–44, 3:52–54, 3:64–67, 5:6–22, 14:1–15:15; Ex. 1003 ¶¶ 159, 165, 168). Hence, each of Buchmann and Talbot confirms that one of skill in the art would have understood memory systems containing a memory module in communication with a memory controller of a host system may operate in different “modes.”

Claim 1 recites a “second mode” in which the module controller generates and outputs a notification signal indicating a status of a training

sequence. Petitioner argues that Hazelzet in combination with any one of Buchmann or Talbot discloses this feature. Pet. 57–66. For example, as Petitioner explains, Buchmann discloses a memory system with “two modes of operation” including a mode for “training” that is “used to perform upstream data lane training” and “outputs various notification signals indicating the status of the . . . training sequence to the memory controller of the host system” and Talbot discloses a “training mode.” *Id.* at 58, 62 (citing Ex. 1016 ¶¶ [0049], [0052], [0053], [0089]; Ex. 1017, 14:1–15:15, 3:52–54, 3:64–67, 5:6–22, 5:40–12:59, 8:24–9:18, Tables 5 and 6; Ex. 1003 ¶¶ 159, 165, 168–169).

As Petitioner points out, Buchmann discloses “a memory controller (MC)” connected to “memory modules” (or “memory buffers”). Ex. 1003 ¶ 113; Ex. 1017, 4:10–15. During “power-on and initialization” of the memory modules and “memory channel initialization” (Ex. 1017, 4:29–31, 5:32), “training states [are] accomplished” including “TS3 – upstream lane training and repair” in which the “host memory controller” “initiates a [training] state . . . to [a memory module]” such that the memory module “returns a handshake . . . to the [memory controller] to let it know that [training] has been completed and the status (e.g., successful).” Pet. 62; *see* Ex. 1017, 5:40–41, 43–44; 6:54–55, 58–62. Buchmann discloses that the memory module performs “upstream lane training and repair” in which the memory module sends a “response [that] indicates that all [memory modules] have returned the TS3a_ack SBC” or a “response [that] indicates [that memory modules] are done with TS2 [i.e., “TS_done”].” Ex. 1003 ¶¶ 167, 169; Ex. 1017, 8:24, 41–44, Table 5. Also, “[t]he last [memory module] . . . sends TS3a_ack [which is] forwarded back to the host.” Ex.

1017, 8:59–61, Table 6. In other words, Buchmann discloses a memory controller connected to a memory module that operates in a mode in which the memory module executes a training sequence and notifies the memory controller of the status of the training sequence (e.g., successful). *See* Ex. 1003 ¶ 169. Likewise, we agree with Petitioner that Talbot teaches a “training mode” in which “memory controller 100 drives a training pattern” to “buffer unit 170” (or “memory module”) and receives “data patterns [or “notification signal”] on CRC path” from the buffer unit. Pet. 57–58 (citing Ex. 1016 ¶ 52).

We agree with Petitioner that Buchmann and Talbot are analogous art to Hazelzet and the ’623 patent because they are all directed to the field of error detection and correction in memory modules. Pet. 59, 63. We also agree with Petitioner that it would have been obvious to one of ordinary skill in the art to have combined the known memory system containing a memory controller connected to a memory module that may operate in more than one mode (e.g., Hazelzet, Buchmann, or Talbot), including a known mode in which the memory module performs a training sequence, to notify (send a notification signal to) the memory controller of the status of the training sequence (e.g., Buchmann or Talbot) in order to improve overall reliability. *Id.* at 59–61, 63–64. Dr. Alpert’s testimony supports that the combination of Hazelzet with Buchmann or Talbot would achieve the predictable and expected result of a known (multi-mode) memory system containing known components of a memory controller connected to a memory module performing a known function of executing a training sequence and notifying the memory controller of the status of the training sequence (e.g., Buchmann or Talbot). Ex. 1003 ¶¶ 159, 175. “The combination of familiar elements

according to known methods is likely to be obvious when it does no more than yield predictable results.” *KSR*, 550 U.S. at 416.

Petitioner further argues that the combination of Hazelzet and any one of Buchmann or Talbot discloses a printed circuit board as recited in claim 1. Pet. 32–34 (citing Ex. 1014 ¶¶ [0015], [0037]–[0039], [0059], [0068]–[0070], [0072], [0076], [0092], [0109], Figs. 2, 3A–3D, 4B, 7A–7C, 8; Ex. 1003 ¶¶ 177–186). Patent Owner does not dispute Petitioner’s contentions with respect to this issue. Based on our review of Petitioner’s argument and evidence, we find that Hazelzet teaches the printed circuit board recited in claim 1.

Notwithstanding Patent Owner’s contrary arguments, which we discuss below, we agree with Petitioner’s showing that the combination of Hazelzet and any one of Buchmann or Talbot teaches every limitation of claims 1, 12, and 21 of the ’623 patent and that a person of ordinary skill in the art would have had reason, with rational underpinning, to combine the references. Further, we credit Dr. Alpert’s supporting testimony (Ex. 1003 ¶¶ 121–150, 158–186), as it is consistent with the prior art disclosures.

Patent Owner argues that it would not have been obvious to one of ordinary skill in the art to have combined the teachings of a known memory system containing a memory module in communication with a memory controller of a host system, the memory module operating in any one of multiple modes (i.e., a system disclosed by any one of Hazelzet, Buchmann or Talbot) with the teachings of a known mode of operation of such a memory system in which the memory module sends a notification of a status of a training sequence to the memory controller (i.e., Buchmann or Talbot) because of an alleged “technological problem.” PO Resp. 11, 29. In

particular, Patent Owner argues that “[d]uring Hazelzet’s [second mode] . . . Hazelzet’s UE line . . . is busy” such that “implement[ing] Buchmann’s TS3 command signaling on Hazelzet’s UE line would run into a signal conflict with Hazelzet’s UE signaling already occurring [on] the UE line [of Hazelzet]” and that the “training pattern data” of Talbot “needs to occur ‘while [Hazelzet’s DIMM(s) 20] is in [Hazelzet’s ECC MODE]’” while “Hazelzet’s UE line . . . is busy.” *Id.* at 11–36.

In other words, Patent Owner argues that it would not be possible for one of ordinary skill in the art to perform a known mode of operation of a memory system (i.e., sending a notification signal of a status of a training sequence) while simultaneously performing a different operation using the same resources (i.e., performing Hazelzet’s “UE signal function”). We are not persuaded by Patent Owner’s argument.

Even assuming to be correct Patent Owner’s contention that sending a notification signal of a status of a training sequence over a particular bus would interfere with performing actions of a different mode of operation on the same bus at the same time, the basis of Patent Owner’s argument is nonetheless that discrete modes of operation are required to occur at the same time. For example, Patent Owner argues that the “training pattern data” of Talbot “needs to occur ‘while [Hazelzet’s DIMM(s) 20] is in [Hazelzet’s ECC MODE]’” but does not explain why transmitting “training pattern data,” in fact, “needs to occur” simultaneously with “Hazelzet’s ECC MODE.” PO Resp. 29. Given that neither Hazelzet nor Talbot discloses any specific temporal relationship between transmitting “training pattern data” and “Hazelzet’s ECC MODE,” there would be no specific requirement

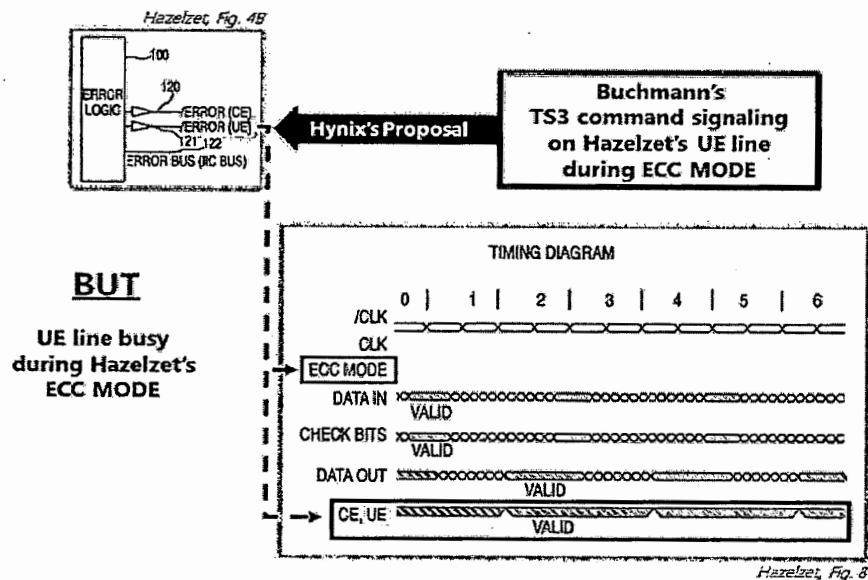
to perform the two modes of operation simultaneously using the same resources.

Similarly, as noted above, Patent Owner argues that “implement[ing] Buchmann’s TS3 command signaling on Hazelzet’s UE line would run into a signal conflict with Hazelzet’s UE signaling already occurring [on] the UE line [of Hazelzet]” but does not explain why “Buchmann’s TS3 command signaling” must be performed simultaneously “with Hazelzet’s UE signaling already occurring [on] the UE line.” PO Resp. 11–36. We also note that claim 1, for example, does not recite or require the performance of multiple modes of operation at the same time over the same bus.

To the extent that Patent Owner argues that it would not have been obvious to one of ordinary skill in the art to have bodily incorporated the teachings of either of Buchmann or Talbot (i.e., training mode) into those of Hazelzet (i.e., a mode during which training is not performed), we note that “[t]he test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference. . . . Rather, the test is what the combined teachings of those references would have suggested to those of ordinary skill in the art.” *In re Keller*, 642 F.2d 413, 425 (CCPA 1981); *see also In re Sneed*, 710 F.2d 1544, 1550 (Fed. Cir. 1983) (“[I]t is not necessary that the inventions of the references be physically combinable to render obvious the invention under review.”); *In re Nievelt*, 482 F.2d 965, 968 (CCPA 1973) (“Combining the *teachings* of references does not involve an ability to combine their specific structures.”).

Moreover, even if discrete modes of operation and associated transmissions were required to occur at the same time, we do not agree with

Patent Owner's argument that a person of ordinary skill in the art would not be motivated to combine Hazelzet with Buchmann or Talbot because of technological problems. *See* PO Resp. 10–15, 27–32. More specifically, Patent Owner argues that during Hazelzet's ECC MODE its UE line would be busy and could not accommodate, for instance, Buchmann's TS3 command signaling. *Id.* at 11–12. To illustrate the alleged understanding of one of skill of Hazelzet's UE line being busy, Patent Owner modified Hazelzet's Figure 8, as reproduced in the version below. *Id.* at 12–13.



The version of Figure 8 of Hazelzet reproduced above was modified by Patent Owner to present the alleged "exemplary operation of the UE line for a data stream of four data operation," with the four data operations on the bottom "CE, UE" line shown in different colors. PO Resp. 13. Patent Owner bases its depiction of a fully occupied UE line on Mr. Murphy's testimony that in the view of one of skill in the art, the "close packing of segments back-to-back most accurately reflects the default industry design

goal to have maximum bus utilization.” Ex. 2005 ¶ 31. Mr. Murphy acknowledges that “it could be possible to increase the spacing between Hazelzet’s UE segments in order to ‘make room’ to implement Buchmann’s TS3 command signaling on the UE line during Hazelzet’s ECC MODE,” but one of ordinary skill would be highly motivated against doing so because Buchmann’s TS3 command signaling is a secondary design feature with less priority.” *Id.* ¶ 32.

We do not credit Mr. Murphy’s testimony because it conflicts with the actual disclosure of Hazelzet and also because, absent support, it applies a broad default industry design goal to a specific application to a bus used to send uncorrectable errors. Hazelzet’s unmodified Figure 8 is reproduced below.

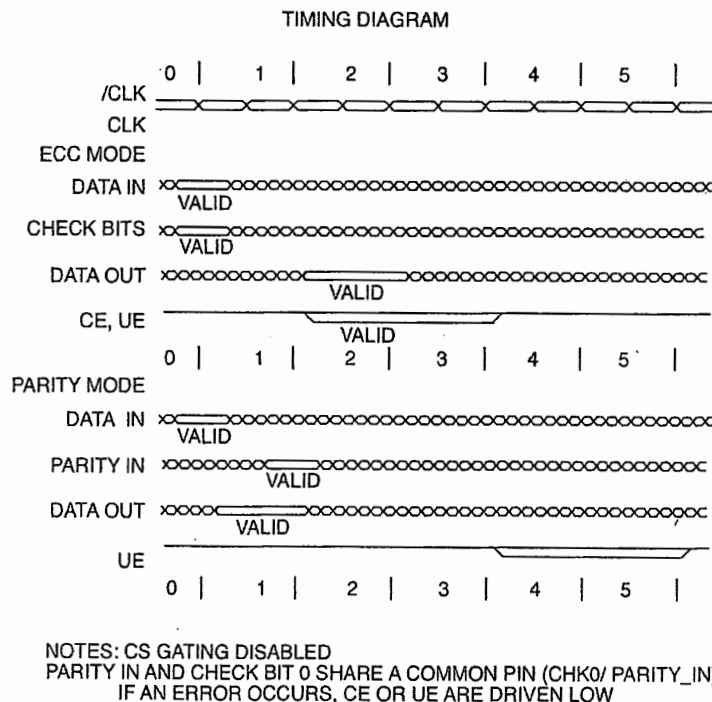


FIG. 8

Figure 8 of Hazelzet, reproduced above, depicts a timing diagram where the “ECC mode” is a mode that allows the host system to detect and/or correct correctible or uncorrectable errors. Ex. 1014 ¶ 69. As shown, the “CE, UE” signal line of the “ECC MODE” depicts more limited signaling in periods 2 and 3 compared to Patent Owner’s depiction in its modified figure that shows signals fully occupying the UE line.

Patent Owner’s justification for altering Buchmann’s TS3 command signaling disclosure is based on the premise that the default industry design goal is to have maximum bus utilization. Although that goal may generally be true, Patent Owner’s expert, Mr. Murphy fails to explain or provide support for applying this general goal to the specific transmissions of Hazelzet, which are limited to error detection. Rule 42.65(a) provides that “[e]xpert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.” We find Mr. Murphy’s testimony to be insufficient to support Patent Owner’s position because it fails to explain why an industry design goal, even if is a default, should be applied to the specific application here, namely a bus used to send uncorrectable errors, when the actual reference discloses conflicting alternative signaling.

Patent Owner further alleges that one of skill in the art would not be motivated to combine Hazelzet and Buchmann or Talbot because they have different design purposes and there would be a risk of failure if the references were combined. PO Resp. 16–27, 32–36. For instance, Patent Owner asserts that

Netlist’s point was not that their two different technical design purposes could not be combined or that doing so was beyond the skill level of a POSITA. Rather, to clarify, Netlist’s point was

that the difference at the design concept level (not implementation details) would have been recognized by a POSITA as a barrier to overcome in order to successfully accomplish the Hazelzet-Buchmann combination proposal, that barrier motivating a POSITA against doing so. For example, in the effort to combine the two fundamentally different technical design purposes, there is the risk that one or the other technical design purpose could be lost, and that risk of failure would be a significant factor leading a POSITA away from the Hazelzet-Buchmann combination proposal.

PO Resp. 17.

We do not agree with Patent Owner's arguments. Patent Owner neither asserts that the prior art would not be combinable in the view of a person of skill in the art, nor presents specific allegations of teaching away. Instead, Patent Owner's arguments are premised on alleged different design purposes and potential increased risk of failure. Petitioner's arguments focus on implementation details of the prior art based on bodily incorporation instead of what the combined teachings of those references would have suggested to those of ordinary skill in the art. *See* PO Resp. 16–27, 32–36. Patent Owner's assertions also allege tradeoffs in the combination, which we do not find persuasive in light of the Petition's demonstrated rationale to combine. *See Winner Int'l Royalty Corp. v. Wang*, 202 F.3d 1340, 1349 n.8 (Fed. Cir. 2000) (“The fact that the motivating benefit comes at the expense of another benefit . . . should not nullify its use as a basis to modify the disclosure of one reference with the teachings of another.”); *see also Polaris Indus., Inc. v. Arctic Cat, Inc.*, 882 F.3d 1056, 1069 (Fed. Cir. 2018) (reference does not teach away “if it merely expresses a general preference for an alternative invention but does not ‘criticize,

discredit, or otherwise discourage' investigation into the invention claimed").

We note that Patent Owner argues that under its proposed claim construction, Petitioner's obviousness contentions under Hazelzet alone, or Hazelzet in combination with Amidi, would fail to teach the "one or more teaching sequence" limitations of the independent claims. PO Resp. 36–37, 43–56. Patent Owner presents no arguments based on this claim construction issue on Petitioner's asserted grounds over Hazelzet in combination with Buchmann or Talbot. *See id.* at 10–36.

Dependent Claims

Claims 3, 4, 14 and 22 recite "training sequences" or "training mode." Patent Owner argues that "Dr. Alpert does not say that [Hazelzet] teaches 'training sequences' [recited in claim 3]" and that Petitioner "and Dr. Alpert add nothing new to treat claims 4, 14, and 22." PO Resp. 57–58. We are not persuaded by Patent Owner's argument at least because Petitioner relies on the combination of Hazelzet and any one of Buchmann or Talbot, not on Hazelzet alone. For reasons previously discussed, we are persuaded by Petitioner that the combination of Hazelzet and any one of Buchmann or Talbot teaches the claimed "training sequences" and, thus, renders obvious claims 3, 4, 14, and 22.

Petitioner also argues that claims 2, 5–11, 13, 15–20, and 23–29 are unpatentable over the combination of Hazelzet and any of Buchmann or Talbot; claims 8, 9, 19, 20, 25, and 26 are unpatentable over the combination of Hazelzet, Hokenmaier, and any of Buchmann or Talbot; and claims 10, 15, and 27 are unpatentable over the combination of Hazelzet, Kim, and any of Buchmann or Talbot. Pet. 57–70. Patent Owner does not dispute

Petitioner's grounds of unpatentability for these claims and references. Any arguments not raised are deemed waived.

We have reviewed the arguments and evidence presented by Petitioner for dependent claims 2–11, 13–20, and 22–29 and conclude that Petitioner demonstrates that these claims would have been obvious over these asserted combinations of prior art. Pet. 35–44, 48–39, 57–70.

Conclusion

For the reasons discussed above, Petitioner has shown by a preponderance of the evidence that claims 1–29 of the '623 patent are obvious over the combination of Hazelzet and Buchmann or Talbot; claims 8, 9, 19, 20, 25, and 26 are also obvious over the combination of Hazelzet, Hokenmaier, and Buchmann or Talbot; and claims 10, 15, and 27 are also obvious over the combination of Hazelzet, Kim, and Buchmann or Talbot.

OTHER GROUNDS

The above discussion addresses and is dispositive as to the unpatentability of all challenged claims, rendering it unnecessary to reach the propriety of any remaining contentions. *See SAS Inst. Inc. v. Iancu*, 138 S. Ct. 1348, 1359 (2018) (holding a petitioner “is entitled to a final written decision addressing all of the claims it has challenged”); *Beloit Corp. v. Valmet Oy*, 742 F.2d 1421, 1423 (Fed. Cir. 1984); *see also Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999); *In re Gleave*, 560 F.3d 1331, 1338 (Fed. Cir. 2009).

III. MOTIONS

PETITIONER'S MOTION TO EXCLUDE

Petitioner moves to exclude Exhibits 2003 and 2004 and portions of Exhibit 2001. Paper 25, 2. We did not rely on Exhibits 2003 or 2004, or the

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cited portions of Exhibit 2001. Therefore, Petitioner's motion to exclude is dismissed as moot.

PATENT OWNER'S MOTION TO EXCLUDE

Patent Owner moves to exclude Exhibits 1034 and 1036. We did not rely on Exhibits 1034 or 1036. Therefore, Patent Owner's motion to exclude is dismissed as moot.

IV. CONCLUSION

For the foregoing reasons, we conclude that Petitioner has demonstrated by a preponderance of the evidence that claims 1–29 of the '623 patent are unpatentable. Specifically, Petitioner has demonstrated by a preponderance of the evidence that claims 1–29 are unpatentable under 35 U.S.C. § 103(a) over Hazelzet and any one of Buchmann or Talbot; claims 8, 9, 19, 20, 25, and 26 are unpatentable under 35 U.S.C. § 103(a) over Hazelzet, Hokenmaier and any one of Buchmann or Talbot; and claims 10, 15, and 27 are unpatentable under 35 U.S.C. § 103(a) over Hazelzet, Kim, and any one of Buchmann or Talbot.

ORDER

ORDERED that claims 1–29 of U.S. Patent No. 9,535,623 B1 are unpatentable;

FURTHER ORDERED that Petitioner's Motion to Exclude is DISMISSED;

FURTHER ORDERED that Patent Owner's Motion to Exclude is DISMISSED; and

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FURTHER ORDERED, that because this is a final written decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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