

MB Initialization sequence

Item 142.35

6-4-09



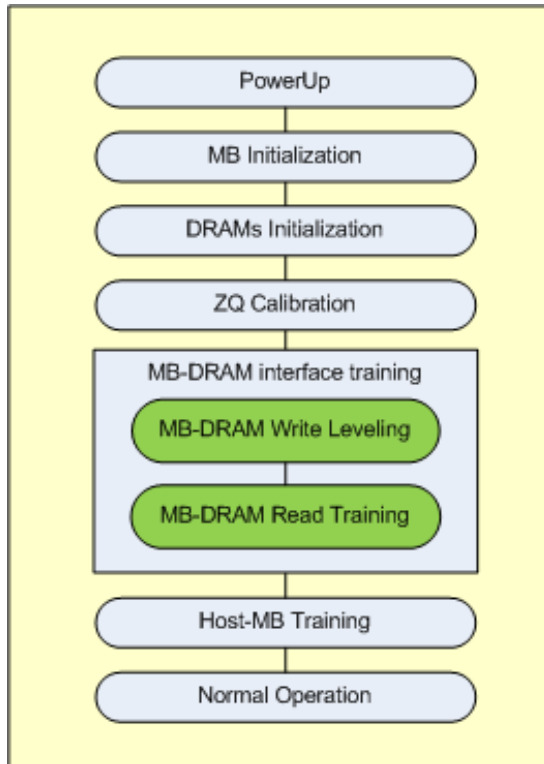
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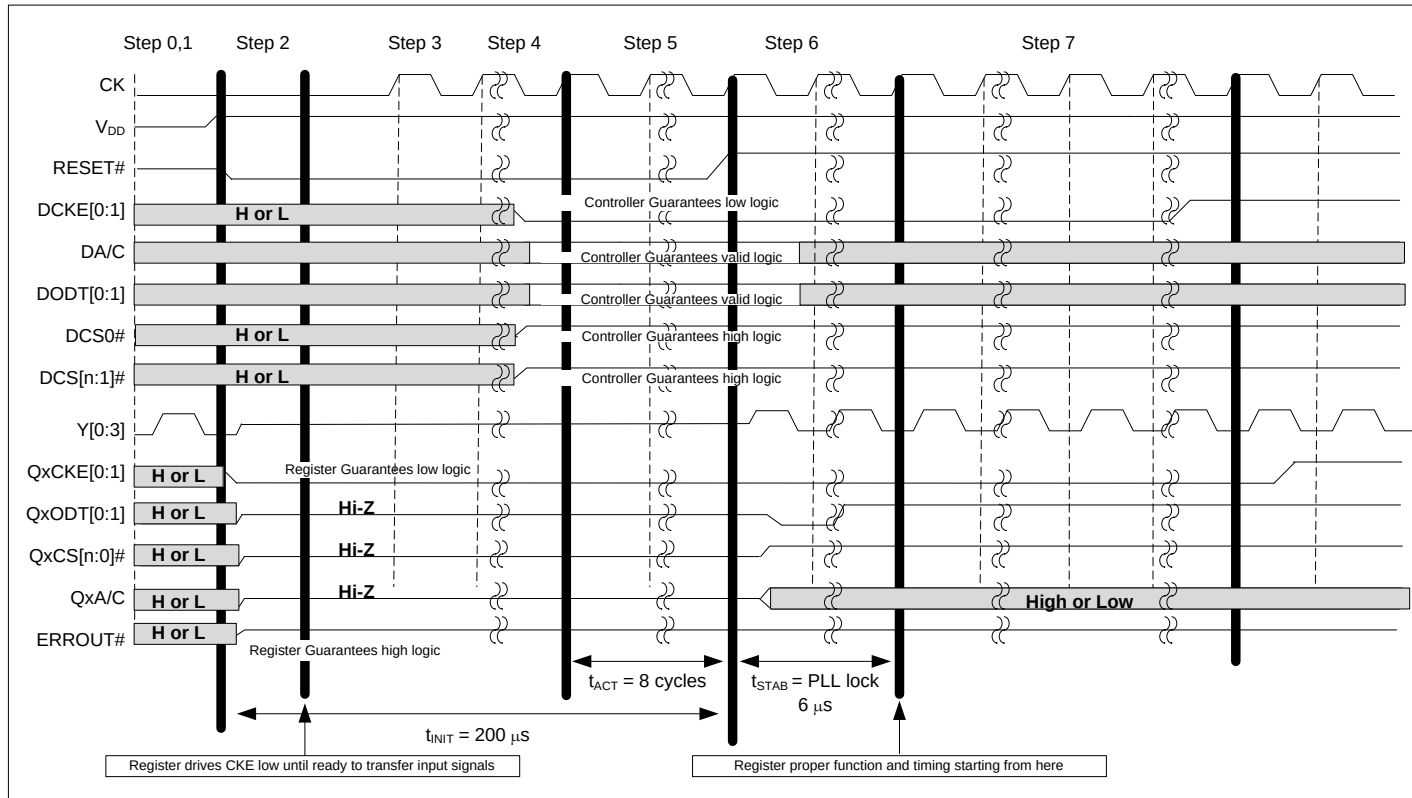
Ex. 1039, p. 1

Initialization Overview



1. Power up requirements same as 882
2. Host initializes MB CWords
3. Host initializes DRAM MRS registers
4. Host issues ZQ command to DRAM
5. Host issues CWord write to start MB-DRAM interface training
6. Host does interface training
7. Normal Operation

MB Power Up Timing



MB Power Up Table

Step	#	power	input								Outputs						
			RESET #	Vref	DCK	DCKE	DCS#	DCMD	DQ/S	DODT	QxCKE	QxCK	QxCS	QxODT	QxCMD	ERROUT #	MDQ/S
No Power	0	0	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	Z	Z	Z	Z	Z	Z	Z
Power Ramp	1	0->V _{DD}	X or Z	X or Z	L	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z
Power Adjust	2	V _{DD} 1.5→1.35 1.35→1.5	L	X or Z	L	X or Z	X or Z	X or Z	X or Z	X or Z	L	Z	Z	Z	Z	H	Z
Clock start	3	V _{DD}	L	X or Z	running	X or Z	X or Z	X or Z	Z	L	L	Z	Z	Z	Z	H	Z
Drive CKE/CS	4	V _{DD}	L	X or Z	running	L	H	X or Z	Z	L	L	Z	Z	Z	Z	H	Z
Apply Vref	5	V _{DD}	L	stable	running	L	H	X or Z	Z	L	L	Z	Z	Z	Z	H	Z
Reset release	6	V _{DD}	H	stable	running	L	H	X or Z	Z	L	L	running	H	L	X	H	Z
Normal operation	7	V _{DD}	H	stable	running	X	X	X	X or Z	X	X	running	X	X	X	X	X or Z

- ❖ Power up sequence is same as 882 device
 - ❖ MB internal circuit calibration is done within the tSTAB time
- ❖ MB doesn't forward DODT as 882, instead the QxODT is initiated by MB depending on the CMD and QxODT configuration

Host RCW to Configure MB

- ❖ Frequency and Voltage RCW to be programmed first
- ❖ No specific ordering requirements for the rest
 - ❖ Address Splitting Mode
 - ❖ Number Input Ranks and Output Ranks
 - ❖ CKE, DODT Modes
 - ❖ Mirroring Mode
 - ❖ QxODT values per rank.
 - ❖ MRS RTT Values
 - ❖ MRS Masking
- ❖ Each of these items has been specified in JEDEC TG showings

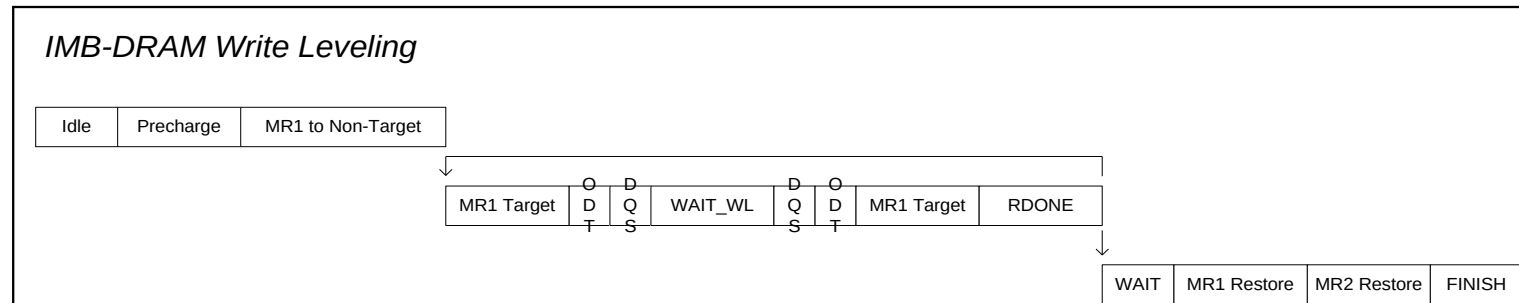
Host MRS to Configure DRAM

- ❖ Host issues ZQ commands to DRAMs
 - ❖ MB doesn't intercept nor response to ZQ command
 - ❖ ZQ command is forward to DRAMs
- ❖ Host issues MRS commands
 - ❖ MRS command is forward to DRAMs

MB-DRAM interface training

- ❖ Host writes CWord, F0RC12, to start the IMB-DRAM training and wait ...
- ❖ MB does write leveling to DRAM
- ❖ MB does RxEn training to DRAM
- ❖ MB return to idle state and ready to start normal operation

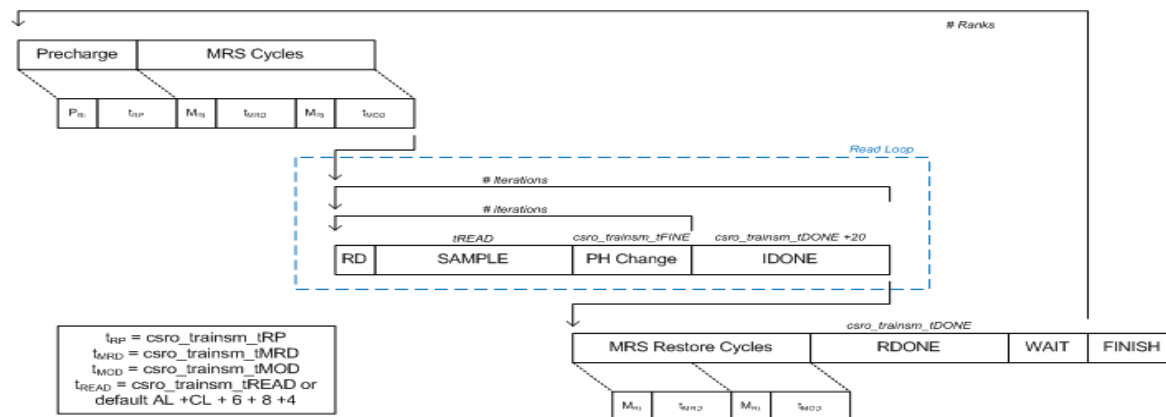
MB-DRAM Write Level Steps



- ❖ Set MR1 for non-target ranks to disable the output drivers.
- ❖ Write Level for Target Rank per DRAM spec
 1. Set MR1 A7 to 1 for target rank to enable Write Leveling
 2. Send DESELECT/NOP during Write Leveling.
 3. MB waits and assert QODT[x] for that rank.
 4. After X nCK MB generates MDQS
 5. After Y nCK, MB samples MDQ inputs.
 6. MB steps through all phases for optimal MDQS phase.
- ❖ Repeat the write level process for each physical rank.

MB-DRAM RxEn Training Steps

IMB-DRAM Read Training



- ❖ Send PREA to the physical rank under training.
- ❖ Enable DRAM to provide data to buffer
- ❖ RxEn Training Iterations
- ❖ Repeat for each physical rank defined by number of physical rank register.

MB-DRAM Complete Training Time

- ❖ After enabling the IMB-DRAM training by setting F0RC12 to 010b, the Host must wait a predetermined number of cycles before moving to next step
- ❖ $\text{Number Cycles} = \text{WL Training Time} + \text{Read Training Time}$

Host-MB Training

❖ Write Level

- MB masks Host issued DRAM WL command
- Host enables Host-MB WL by writing to MB
- MB WL Timing same as DRAM