

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC., SK HYNIX AMERICA INC., and SK HYNIX MEMORY
SOLUTIONS INC.,
Petitioners,

v.

NETLIST, INC.
Patent Owner

Patent No. 8,489,837

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Inventors: Hyun Lee

Title: Systems and Methods for Handshaking with a Memory Module
Inter Partes Review No. IPR2017-00548

PETITIONERS' REPLY TO PATENT OWNER'S RESPONSE

TABLE OF CONTENTS

I.	INTRODUCTION	1
II.	CLAIM CONSTRUCTION.....	3
	A. “Mode”	3
III.	LECLERG IN VIEW OF LEE RENDERS OBVIOUS CLAIMS 1-3 AND 6	8
	A. LeClerg discloses a “memory module configured to operate in at least two modes”	8
	B. LeClerg discloses “a controller circuit configured to cause the memory module to enter the initialization mode”	11
	C. LeClerg discloses “a notification circuit ... to provide at least one notification signal to the memory controller”	12
	D. LeClerg discloses “the at least one notification signal triggers the memory controller to execute an interrupt”	14
IV.	LECLERG IN VIEW OF LEE AND KIM RENDER CLAIM 5 OBVIOUS.....	16
	A. The Board Properly Construed Claim 5, But the Claim Is Not Patentable Even Under A Narrower Interpretation.....	16
	B. The Petition’s Proposed Modifications Are Supported By The Disclosures Of Its Cited References.....	18
V.	CONCLUSION	25

I. INTRODUCTION

The supposed invention of the 837 Patent is a memory module that provides initialization status, such as complete/not complete, using a signal line, such as an open-drain configured connection, to interrupt a memory controller. As demonstrated in the Petition, such functionality was well-known in the prior art and there were substantial reasons to combine such functionality in a single implementation.

Patent Owner seeks to avoid these amply supported facts by misconstruing the claims and mischaracterizing the prior art. Patent Owner asks, for example, for an interpretation of the claim term “mode” that departs from the ordinary meaning of that ordinary word, as its own expert admits. Ex. 1021, 77:24-25 (“So no, it's not the normal and ordinary meaning.”). Patent Owner’s proposed interpretation is also inconsistent with the patent specification, since under that interpretation the claimed “initialization mode” cannot employ the same memory operations as the claimed “operational mode,” Resp., 7; Ex. 2001, ¶48, even though the 837 Patent explicitly states that “the memory module 10 [] perform[s] standard operations such as memory read/write ... while in operational mode, **although it will be appreciated that one or more of these operations can also be performed by the memory module 10 while in initialization mode**” Ex. 1001, 6:27-33 (emphasis added).

As to the prior art, Patent Owner contends that the prior art LeClerg reference does not disclose the two claimed modes because both initialization and normal operations occur when the LeClerg memory module is operating at a normal *power level*. Resp., 7. But neither the claims nor specification of the 837 Patent say anything about power levels and, as Patent Owner's expert admitted on cross-examination, "the proper interpretation [of the claims] really shouldn't turn on power levels." Ex. 1021, 84:9-86:4.

Similarly, Patent Owner argues that LeClerg does not disclose sending initialization status messages to the memory controller, as required by the claims, but instead sends them directly to the processor. Resp., 15. But LeClerg discloses no direct connection between memory module and processor, and LeClerg explicitly discloses that information sent to the memory controller "can include initialization and/or test status messages," Ex. 1005, ¶ 34, as its expert has candidly admitted, Ex. 1021, 35:7-11 ("Q. Would you agree that the communication sent from the buffer module 202 on the upstream channel to the memory controller could include initialization status messages? A. **Based on what I've read in LeClerg, yes.**")(emphasis added).

Finally, dependent claim 5 of the 837 Patent adds only "an error-out pin" to the memory module recited in claim 1, without any recitation of functionality or more detailed structure for that pin. The Petition demonstrated that it would have

been obvious to use the error-out pin shown in the prior art Kim patent in the system of LeClerc for basic signaling of initialization status (*i.e.*, complete/not complete). Nevertheless, Patent Owner insists that such a minor modification of LeClerc – simply the addition of an error-out pin – represents a non-obvious variation and spends half of its Response attempting to explain why. But there is nothing non-obvious about including a prior art, industry standard-defined error-out pin in a system such as LeClerc’s; nor is there anything non-obvious about using the pin to communicate status information, as Kim explicitly discloses.

The claims at issue here are thus clearly unpatentable, and the Board should so rule.

II. CLAIM CONSTRUCTION

A. “Mode”

Patent Owner’s proposed construction of the claim term “*mode*” to mean “a distinct behavioral state that a system may be switched to,” Resp., 3, is inconsistent with the ordinary meaning of that term and unsupported by the intrinsic and extrinsic record.

For example, Patent Owner’s expert, Mr. Murphy, confirmed during cross-examination that the 837 Patent uses the term “mode” in its plain and ordinary sense. Ex. 1021, 9:23-10:2. Yet, Murphy also confirmed that Patent Owner’s proposed construction is not in accordance with that plain and ordinary meaning:

Q. Is it your view that the interpretation you're proposing here is just the ordinary meaning of the word "mode" to a person of ordinary skill in the art reading the '837 patent?

THE WITNESS: **No, I don't think it's the necessary -- is necessarily the ordinary meaning.** Clearly, that's what Hynix has proposed here, the plain and ordinary meaning. And in the table that's listed in page 17, I haven't listed that as being what I believe to be the correct construction. **So no, it's not the normal and ordinary meaning.**

Ex. 1021, 77:14-25 (emphasis added).

Under the broadest reasonable interpretations standard, a claim term must be given its ordinary and customary meaning, as would be understood by a person of ordinary skill in the art in the context of the entire disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Here, Patent Owner's proposal does not satisfy that standard, and Patent Owner does not even attempt to justify how the intrinsic record might support a specialized, non-ordinary meaning.

Patent Owner's construction is also inconsistent with the intrinsic record. For example, Patent Owner's construction requires a "distinct behavioral state," which according to Patent Owner means that the claimed operational and initialization modes cannot use the same memory operations. *See* Resp. at 7; Ex. 2001, ¶48. But the 837 Patent explicitly states that both the operational mode and the initialization mode can employ the same memory operations:

For example, the system memory controller 14 may cause the memory module 10 to perform standard operations such as memory read/write, pre-charge, refresh, etc., while in operational mode, **although it will be appreciated that one or more of these operations can also be performed by the memory module 10 while in initialization mode in certain embodiments.**

Ex. 1001, 6:27-33 (emphasis added); *see also* Ex. 2002, 105:8-115:9, 162:8-19.

Indeed, on cross-examination, Patent Owner's expert conceded that that the memory commands disclosed in the passage quoted above as being usable in the initialization mode would be considered "normal memory commands that a memory controller or processor would issue to read and write data out into main memory under standard or regular use of a computer[.]" Ex. 1021, 24:24-25:18, and that the proper interpretation of the "mode" language in the claims must be consistent with that passage, *id.*, 25:24-29:25. Thus, the memory module disclosed in the 837 Patent employs identical behavior in the two claimed modes, consisting of the normal memory commands typically used "under standard or regular use." Patent Owner construction is wholly at odds with this disclosure.

Patent Owner's proposed interpretation is also inconsistent with the extrinsic record Patent Owner itself has created. For example, the dictionary definition Patent Owner provides defines "mode" to mean "[a]n operational state that a system has been switched to." Ex. 2009, 624. Nothing about that definition

requires the “distinct behavior” Patent Owner asks to be read into the claim and on which it bases its main argument for patentability.¹

Finally, Patent Owner’s proposal injects several ambiguities into the analysis. As demonstrated above, Patent Owner interprets “distinct” to mean “mutually exclusive” and “behavior” to mean “memory operations,” but offers no justification for those interpretations. Neither of these words, moreover, are used in the 837 Patent, or in the extrinsic dictionary definition Patent Owner placed into the record, so it is impossible to know what sense they might apply in the context of the 837 Patent and improper to inject them into the claim. The purpose of claim construction is to remove such ambiguities, not to insert them. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 985-86 (Fed. Cir. 1995).

¹ Patent Owner’s attempt to rely on the testimony of Petitioner’s expert, Dr. Alpert, is misplaced. Dr. Alpert testified that a memory module cannot be in the “operational mode and initialization mode at the same time,” Ex. 2002, 119-21-120-5, but later clarified that “the entire module cannot be both in the initialization mode and the operational mode at the same time,” *id.*, 156:21-157:11 (emphasis added). Nowhere did Dr. Alpert say that the two modes must have distinct behaviors or employ mutually exclusive memory operations, as Patent Owner argues.

Patent Owner's "system" language is also ambiguous. As its expert conceded, a "system" can effectively be anything, depending on where one draws a line. Ex. 1021, 88:5-14. Injecting that term into the claims here therefore means that it will always be satisfied, if anything can be a system, or that it can only be satisfied by some unexplained line drawing rule. The claims of the 837 Patent already recite structural limitations, such as "memory module" and "controller circuit." There is no need to introduce new and ambiguous structural terms to apply those claims to the prior art.

Patent Owner's specialized interpretation of the simple claim term "mode" is therefore legally erroneous and particularly unhelpful. It should be rejected. Indeed, as the Board concluded in the Institution Decision, the term "mode" need not be interpreted at all. However, to the extent the Board now thinks otherwise, Petitioner agrees that the word "state" – when understood without all of the implicit limitations Patent Owner seeks to have read into the claims – is a synonym for "mode" in the context of the 837 Patent. That word is consistent with the disclosures of the 837 Patent and the dictionary Patent Owner has provided. For example, a memory module performing initialization procedures could fairly be characterized as being in a state of initialization, *i.e.* an initialization mode. Moreover, Petitioner observes that while Patent Owner's dictionary uses the phrase "operational state," Ex. 2009, 624, it is clearly using "operational" more broadly

than the 837 Patent, since the patent explicitly equates the disclosed “operational mode” with normal memory operations and the dictionary includes no such limitation. Ex. 1001, 6:22-26; Ex. 2009, 3. Construing “mode” to mean “state” therefore captures the ordinary meaning of “mode” and avoids any confusion from the inconsistent use of the word “operational.” To be clear, Petitioner does not believe interpreting “mode” to mean “state” alters the analysis set forth in the Petition one whit, since in Petitioner’s view the two words mean the same thing to a person of skill, but Petitioner has no objection to the Board adopting that portion of Patent Owner’s dictionary definition if the Board sees it as helpful.

III. LECLERG IN VIEW OF LEE RENDERS OBVIOUS CLAIMS 1-3 AND 6

A. LeClerg discloses a “memory module configured to operate in at least two modes”

Patent Owner’s main argument is that LeClerg supposedly does not disclose both an operational mode and an initialization mode. Resp., 7-13. Its contention is based, first, on the assertion that LeClerg describes only a low power mode and a normal power mode. Resp., 7. Patent Owner thus argues that because LeClerg uses the term “mode” to discuss power levels it cannot be found to disclose the claimed initialization mode. *Id.* But that is a non-sequitur. The real question is whether the operations disclosed in LeClerg constitute the claimed modes, regardless of what LeClerg calls them or what power levels his system uses.

As set forth in the Petition, LeClerc discloses a mode – a state, for example – during which initialization operations occur, such as during the boot-up state of the system, Ex. 1005, ¶¶3, 18, and also discloses a mode during which normal memory operations occur, *id.*, ¶25. Patent Owner does not dispute that these disclosures satisfy the claims under Petitioner’s interpretations. Indeed, as Patent Owner’s expert conceded, the operational state of LeClerc would not occur during boot up, Ex. 1021, 17:8-14, so LeClerc discloses distinct behavioral states for these two modes; thereby satisfying the claims even under Patent Owner’s interpretation and evidence.

The only other argument Patent Owner advances for why these differing states of LeClerc are not different “modes” is that they use the same memory commands. *See Resp.*, 7-8. But as demonstrated above, the 837 Patent explicitly discloses that both claimed modes may use the same memory commands, Ex. 1001, 6:27-33, and Patent Owner’s expert conceded as much on cross-examination, Ex. 1021, 24:24-25:18, 25:24-29:25. Patent Owner’s argument must therefore be rejected as inconsistent with the specification and unsupported by the evidence of record.

Patent Owner also complains that Petitioners’ proposed interpretations of “operational mode” and “initialization mode” use the phrase “during which” and are therefore somehow improperly linked to a time period. *Resp.*, 9-10. However,

the 837 Patent consistently characterizes the disclosed modes in terms of a time period during which certain operations occur, including in the Abstract (“... an initialization mode **during which** the memory module executes at least one initialization sequence ...”)(emphasis added); the Summary of the Invention (same at 1:38-39); the Detailed Description (same at 4:10-11) and the claims (same at 14:9-11). Thus, Petitioner’s proposed interpretations employ the same verbal formula – a time period during which certain operations occur – employed by the patent. Ex. 1001, Abstract, 1:36-40, 1:51-55, 1:67-2:4, 4:8-12, 5:43-46, 8:63-67, 11:16-19, 11:47-51, 12:10-14. Patent Owner cannot reasonably object to the form of an interpretation that tracks the disclosure of the patent so closely.²

² When confronted with this consistent use of the phrase “during which” in the patent documents, Patent Owner’s expert was unable to explain why that verbal formula was acceptable when used in the specification and claims of the patent but not in Petitioner’s claim interpretations, Ex. 1021, 99:12-109:2, but instead insisted, without any explanation, that Petitioner’s expert somehow used the phrase “during which” in his interpretation of initialization mode in a way that was “totally different” from how the 837 Patent uses that same phrase to characterize the initialization mode, *id.*, 108:5-14. Such unsupported testimony can hardly support the Board’s fact-finding.

Patent Owner also argues, without explanation, that it is improper to find that LeClerc has both an operational mode and an initialization mode based on operations that all occur while the module of LeClerc is operating at a normal power level. Resp., 11. Patent Owner further contends that Petitioner's expert should be found to lack credibility because he was unprepared to testify about power modes. *id.*, 11-13. The 837 Patent, however, says nothing about power modes or power levels. Indeed, Patent Owner's expert conceded that power modes are irrelevant to the 837 Patent, and that "the proper interpretation [of the claims] really shouldn't turn on power levels." Ex. 1021, 84:9-86:4. It is Patent Owner's power level arguments that should be given no credence.

B. LeClerc discloses "a controller circuit configured to cause the memory module to enter the initialization mode"

Patent Owner also argues that LeClerc does not disclose the claimed "controller circuit configured to cause the memory module to enter the initialization mode" because (1) it does not disclose an "initialization mode" and (2) the Controller 304 identified in the Petition as satisfying this claim element "does not cause the memory controller to enter normal power mode from low power mode." Resp., 13.

As demonstrated above, the first contention is incorrect under any interpretation, as LeClerc discloses a distinct behavioral state (such as during boot up) during which initialization operations occur. Ex. 1005, ¶¶3,18.

The second contention is simply irrelevant, since power modes have nothing to do with the claims or the patent, as even Patent Owner's expert agrees. Ex. 1021, 84:9-86:4.³

C. LeClerc discloses “a notification circuit ... to provide at least one notification signal to the memory controller”

Patent Owner also argues that LeClerc does not disclose the claimed “notification circuit ... to provide at least one notification signal to the memory controller” because (1) it does not disclose an “initialization mode” and (2) because “Hynix fails to show how LeClerc satisfies the notification circuit

³ To the extent Patent Owner may be arguing that “the initialization/test Controller 304” of LeClerc does not cause the memory module to enter the initialization mode, because it is “the registers in the initialization/test Controller 304 [that] initiate a [initialization] procedure.” Resp., 13 (citing Ex. 2001, ¶54); *see also* Ex. 2001, ¶54, that is incorrect. LeClerc discloses that it is Controller 304 that causes the initialization mode to be entered (*i.e.*, “begin[s] the process of initializing”), Ex. 1005, ¶46; Ex. 1003, ¶117, and Patent Owner's expert has admitted that the “registers” of LeClerc are merely storage devices, Ex. 1021, 95:9-13, that do not have any ability to process data, *id.* at 96:1-9. Accordingly, the “registers” cannot be the “cause” of the initialization.

providing a notification signal portion of this element” because “each channel [of LeClerg] is a parallel connection including a plurality of wires and is not a signal.” Resp., 14.

As demonstrated above, LeClerg does disclose an “initialization mode” under any interpretation, so Patent Owner’s first argument is erroneous.

Moreover, Patent Owner’s second argument mischaracterizes the analysis in the Petition by suggesting that the Petition accused LeClerg’s output 210 as satisfying the “notification signal” of the claims. Rather, the Petition accused the initialization status messages of LeClerg, which are communicated over output 210, as satisfying the claimed “notification signal.” Pet., 30-32.⁴

⁴ Patent Owner’s suggestion that it reads the Petition as accusing output connections as the claimed “notification signal,” rather than the initialization status information communicated over those connections, is also not credible.

The Preliminary Response expressly noted that “[t]he Petition maps the claimed ‘at least one notification signal’ to LeClerg’s ‘an Initialization Complete message and/or a processor interrupt,’” Prelim Resp., 8, the Board’s Institution Decision described the same mapping when rejecting one of Patent Owner’s arguments, Paper 7, 9, and Patent Owner’s expert responded to Dr. Alpert’s analysis showing

D. LeClerg discloses “the at least one notification signal triggers the memory controller to execute an interrupt”

Patent Owner also argues that “Hynix has failed to show the capability of the notification circuit to send a notification signal” to the memory controller and “[t]hus, Hynix has failed to show how LeClerg satisfies this claim element.” Resp., 14-15. Patent Owner’s reasoning appears to be that LeClerg must be read to include some type of direct connection between memory module and processor, *i.e.*, a connection that avoids or “goes around” the memory controller, such that LeClerg’s module never sends its initialization status messages to the memory controller as claimed.

Patent Owner reaches that conclusion, however, only by ignoring what is actually disclosed in LeClerg. The only connection between module and processor in LeClerg *is through the memory controller*, as shown in Figure 1 below:

that the initialization status message of LeClerg satisfied the claimed “notification signal,” Ex. 2001, ¶82; Ex. 1021, 125:21-126:1.

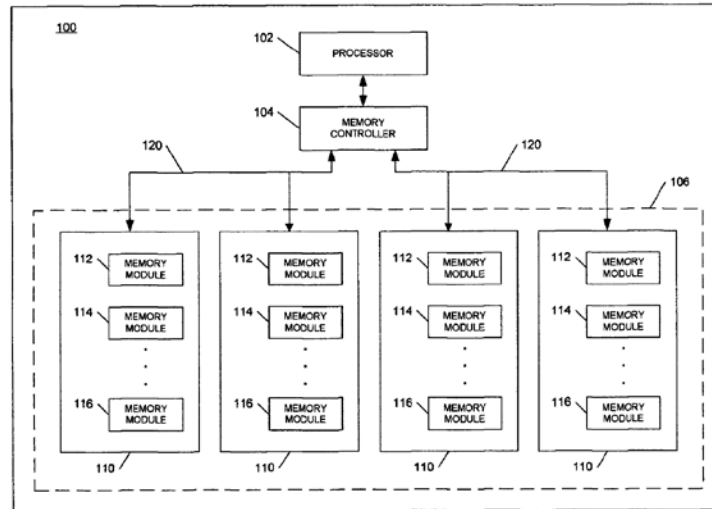


FIG. 1

Moreover, LeClerc expressly states that initialization status messages are sent from the memory modules *to the memory controller*, Ex. 1005, ¶ 34 (“Any type of information received from any memory module which is **directed toward the memory controller** 104 is referred to herein as “upstream data,” **which can include initialization and/or test status messages,...**”)(emphasis added), as Patent Owner’s expert admitted, Ex. 1021, 35:5-11.

Patent Owner’s theory to the contrary is based squarely on a misreading of ¶73 of LeClerc, which Patent Owner reads as disclosing a “direct path” and an “indirect path” between the processor and the memory modules. Resp., 15. But that paragraph does not mention any “direct path” or “indirect path.” Ex. 1005, ¶[0073]. Moreover, as Patent Owner’s expert admitted on cross-examination, this reading of ¶73 ignores FIG. 1, Ex. 1021, 56:15-60:5, which is expressly cited in ¶73 (“In an above-described embodiment, the processor (e.g., processor 102, FIG.

1) ...” and which discloses only an indirect path between processor and memory module *through the memory controller*.

IV. LECLERG IN VIEW OF LEE AND KIM RENDER CLAIM 5 OBVIOUS

A. The Board Properly Construed Claim 5, But the Claim Is Not Patentable Even Under A Narrower Interpretation

Claim 5 of the 837 Patent states, “[t]he memory module of claim 1, wherein the at least one output comprises an error-out pin of the memory module.” In its Institution Decision, the Board correctly noted that claim 5 does not recite any “specific function” of the “error-out pin.” Paper 7, 11.

Patent Owner objects to this reading of the rather simple language of claim 5, arguing that, by virtue of claim 1, “claim 5 requires a ‘notification circuit configured to drive’ the ‘error-out pin’ ‘while the memory module is in the initialization mode to provide at least one notification signal to the memory controller indicating at least one status of the at least one initialization sequence.’” Resp., 17.

The obvious problem with Patent Owner’s argument is that the plain language of claim 5 does not say that. Nor is there any reason in law or the patent that dependent claim 5 could not have been written to add an error-out pin to the module of claim 1 without also defining the function of that pin. Despite Patent Owner’s arguments to the contrary, the mere fact that claim 5 requires the error-out

pin to be part of the “at least one output” of claim 1 does not mean that the error-out pin must perform all of the functionality of the “at least one output.” Patentees have the flexibility to claim more broadly than that, and this one did so. Indeed, if Patent Owner had really desired a narrower version of claim 5, it could have drafted the claim originally with the limitations it now asks to have read in or it could have moved to amend the claim in this proceeding. It has done neither, and should not be heard to complain about the plain meaning of the words it chose to include in its claim.⁵

But the claim is unpatentable even under the narrower interpretation advanced by Patent Owner because the Petition demonstrated that the cited combination of LeClerc, Lee and Kim included the error-out pin of Kim, configured as an open drain, to communicate initialization status messages to the memory controller. The Petition’s analysis of claim 5 explicitly referenced the combination analysis of claim 3, where Kim was first analyzed in combination. Pet., 46 (“As demonstrated above, the use of the output-pin scheme of Kim in the

⁵ The testimony of Dr. Alpert, cited by Patent Owner, is not to the contrary. There is no disagreement that claim 5 requires the error-out pin to be part of the “at least one output,” which is what Dr. Alpert said, but neither the claim nor Dr. Alpert say what the error-out pin must be used for.

system of LeClerc would have been obvious....”). That combination analysis expressly noted that the error-out pin of Kim would be used in the combination to send initialization status messages. *E.g.*, Pet., 44 (“In the combination of LeClerc with the open-drain output pin scheme of Kim, an active signal on the output pin (in response **to an initialization command**) **would indicate that the initialization sequence had ‘Not Completed’** ...”); *see also id.*, 45 (“To use the output-pin scheme of Kim in the system of LeClerc would therefore have been only the use of known techniques for their known purposes to achieve predictable results, *i.e.*, using a single line **to provide status information from multiple components.**”)(emphasis added.); *see also id.*, 46. Thus, even if one were to interpret claim 5 as desired by Patent Owner, the cited combination on which trial was instituted would still render claim 5 unpatentable.

B. The Petition’s Proposed Modifications Are Supported By The Disclosures Of Its Cited References

Patent Owner also argues that “it is unclear what teachings of LeClerc, Lee and Kim correspond to the various ‘known’ things referenced above by the Board.” Resp., 20. However, as demonstrated in the Petition, a notification circuit for sending a “notification signal,” among other requirements of the claims, is disclosed by LeClerc, Pet., 30-32, a memory controller with an embedded processor and interrupt handling functionality is disclosed by Lee, Pet., 40-42, and

a shared “error-output pin” for reporting status messages is disclosed by Kim, Pet., 43-47. Patent Owner does not dispute these facts.

The Petition further provided reasons to combine the various references as set forth in the Petition, including that to do so would be simply the use of known techniques for their known purposes with no unpredictable results and that a person of skill would be motivated to make the combination for various reasons. Pet., 39-43, 45-46. Patent Owner also does not dispute these facts.

The cited combination on which trial was instituted is thus fully supported by the Petition.

C. Claim 5 Does Not Require “Initialization Error”

Despite conceding all of the above fact by not disputing them, Patent Owner argues that claim 5 is still not obvious because Kim supposedly makes no mention of “initialization errors.” Resp., 21. Were that assertion correct, it would be irrelevant. Claim 5 does not require “initialization errors” and Kim was cited in combination against claim 5 solely for its error-out pin, which Patent Owner concedes Kim discloses. See Pet., 46-47; Resp., 21.

In any event, as explained in the Petition, Kim discloses “initialization errors.” Pet., 44; Ex. 1008, 12:18-26; Ex. 1003, ¶158. For example, even Patent Owner admitted that Kim discloses “the collective information passing to and/or from Kim’s memory system” and that the “collective information” includes

“requesting or reporting status or error conditions” and also “completing memory or logic initialization.” Prelim. Resp., 12-13 (emphasis added); Ex. 1008, 12:18-26. Patent Owner provides no reason as to why one skilled in the art would have narrowly read this passage of Kim to conclude that such “collective information” taught by Kim does not include “initialization errors,” other than the fact that Kim did not specifically use the word “initialization” and “error” sequentially in a single phrase. *Id*; Resp., 21. Whether the exact same phrase is used by prior art references is not the relevant test. *In re Preda*, 401 F.2d 825, 826 (CCPA 1968).

Patent Owner further argues that “Hynix’s ‘initialization errors’ are not even actually any error, but rather initialization completion status messages of ‘Not Completed’ and ‘Completed’ messages to notify the host system of the status of memory module notification.” Resp., 21. Once again, this assertion is irrelevant. The claims do not require a notification signal indicating “initialization errors,” but instead require a “notification signal ... indicating at least one status of the at least one initialization sequence,” and Patent Owner’s expert has now conceded that LeClerc discloses sending such a signal from the memory module to the memory controller. Resp., 21.⁶

⁶ In any event, LeClerc’s status messages can include error information, so the combination of LeClerc and Kim clearly shows “initialization errors.” Ex. 1005,

Patent Owner also asserts that “Hynix’s initialization completion status messages would be reported via a ‘separate bus, such as a ‘presence detect’ bus, an I2C bus and/or an SMBus,’ which Kim already sets aside for reporting of . . . status information.’” Resp., 21-22. But the cited combination in the Petition, on which this trial was instituted, said nothing about a separate bus, and instead included the open-drain error-out pin of Kim as part of LeClerc’s output 210 directly connecting the memory modules to the system memory controller. Pet., 44-46. Patent Owner’s straw-man argument, directed as it is to a combination nobody has advanced, is thus irrelevant.

D. Claim 5 Does Not Require Multiple Memory Modules To Be Connected By A Single “Error-Out Pin”

Patent Owner next argues that Kim does not disclose using an open-drain error-out pin for multiple memory modules. Resp., 23. But Patent Owner once again ignores the Petition and the teachings of the prior art.

As to claim 5, the Petition cited Kim for its disclosure of an error-out pin. Pet., 46-47. LeClerc already disclosed an output 210 over which initialization status messages are communicated and which connects all memory modules of the

¶91; *see also* Pet., 44-45; Ex. 1003, ¶¶162, 163; Ex. 1005, ¶¶28, 35; Ex. 1008, 5:49-57, 12:18-26.

LeClerc system, Ex. 1005, ¶35, FIGS. 1 and 2, and Kim’s error-output pin scheme was proposed as part of that connection in the cited combination. Pet., 44-46. Thus, whether Kim discloses an error-out pin connecting multiple memory modules is irrelevant because the cited combination of Kim and LeClerc does. Patent Owner thus improperly attempts to argue against the combination by attacking Kim in isolation.

Moreover, Patent Owner reads Kim too narrowly. Kim discloses several exemplary “memory subsystems” in FIGS. 1-3, each of which includes multiple memory modules. Ex. 1008, 1:14-2:3, 3:8-12, FIGS. 1-3. Kim then describes one aspect of his invention as including the use of open drain signaling between the memory devices of the “memory subsystem.” Ex. 1008, 4:40-43 (“An exemplary embodiment of the present invention offers an innovative solution where a single pin is used, dotted via an open drain or related method **across memory devices in a memory subsystem ...**”)(emphasis added). There is no reason to interpret that disclosure as meaning the open drain connection connects only the memory devices of a single module. Ex. 2002, 150:12-22; *see also* Ex. 1008, 1:16-18 (explaining that Kim’s “memory subsystem” includes “one or more DIMMS”).

And while the more specific description of Kim’s FIG. 4 describes connecting memory devices that are accessed at the same time, such as those in the same rank, via an open drain connection, Ex. 1008, 5:49-57, that is described as

“an exemplary embodiment,” Ex. 1008, 5:49. Thus, Patent Owner’s overly narrow reading of Kim is both irrelevant and erroneous.

Patent Owner also argues that “Kim’s technique of a ‘single pin’ with an ‘open drain output’ would not be suitable, as a POSITA would see technical problems in the Petition’s proposed combination of LeClerc and Kim.” Resp., 27. The only supposed “technical problem” Patent Owner identifies, however, is that “when multiple memory modules of LeClerc assert a signal on the shared ‘open drain connection,’ it would not be possible to identify the specific memory module that is the source of the asserted signal.” Resp., 27-28.

But the claims at issue here do not require identification of the specific memory module that is the source of the asserted signal, as even Patent Owner’s expert has conceded. Ex. 1021, 132:6-11. Rather, they require only a notification signal indicating status of initialization (claim 1), which status can be either “Complete” or “Executing” (*i.e.*, Not Complete) (claims 2 and 3). Patent Owner does not dispute, and therefore concedes, that use of Kim’s open-drain signaling technique in the system of LeClerc could be used to achieve that functionality.

Similarly, Patent Owner’s argument that “Kim’s open drain connection would also lead to the loss of LeClerc’s intended purpose to provide full initialization completion status messages” is also irrelevant. Resp., 28. The claims

at issue here simply do not require that functionality, so the combination of Kim and LeClerc is sufficient to satisfy the requirements of the claims.

Nor does the cited combination require that the unclaimed functionality cited by Patent Owner be sacrificed from LeClerc. For example, in LeClerc the identity of “the specific memory module that is the source of the asserted signal” and complete initialization status information is stored in registers on the memory module, Ex. 1021, 137:14-25, 138:21-139:12, which LeClerc’s system memory controller can obtain either by polling or a notification signal. Ex. 1005, ¶¶55, 60, 88. Nothing in the Petition suggested that such functionality would be removed in the cited combination, and nothing in the use of Kim’s error-out pin requires its removal. The cited combination thus includes all of the functionality described in LeClerc, supplemented by Kim’s error-out pin.

Finally, Petitioner observes that nowhere does Patent Owner or its expert argue that the cited combination is not enabled, and the evidence of record would not support such an argument. Dr. Alpert, for example, explained that the cited combination was merely the use of known techniques and structures, Ex. 1003 at ¶¶160-162, and that “a person of skill in the art would readily have modified that [sic] LeClerc’s channels with the teachings of Kim to be a[n] open-drain output pin.” *Id.* at ¶162. That testimony is unrebutted.

Indeed, Patent Owner's expert admitted on cross-examination that one skilled in the art would have been knowledgeable about, among other things,

- “memory modules,”
- “initialization sequences used in memory modules,”
- “interactions between a memory controller and a memory module as they pertain to initialization,”
- “how to signal information back and forth between a memory controller and a memory module,”
- notifying and polling techniques as disclosed in the 837 Patent,
- “open drain signaling,” and
- the details of the JEDEC DDR standards (including provisions for “error-out pins”).

Ex. 1021, 73:23-77:5. Given this knowledge, one skilled in the art would have found Petitioner's proposed modifications to be supported by the disclosures of the cited references, well within the level of skill in the art, and entirely obvious.

V. CONCLUSION

For the reasons set forth above and in the Petition, Petitioner respectfully requests that claims 1-3, 5, and 6 be canceled as unpatentable.

Dated: December 13, 2017

Respectfully Submitted,

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Appendix: Updated List of Evidence and Exhibits

Exhibit #	Reference Name
1001	U.S. Patent No. 8,489,837
1002	File History of U.S. Patent No. 8,489,837
1003	Declaration of Donald Alpert
1004	Curriculum Vitae of Donald Alpert
1005	U.S. Patent Application Pub. 2005/0071580 to LeClerc et al.
1006	U.S. Provisional App. No. 61/186,799
1007	U.S. Pat. App. Pub. 2005/0193161 to Lee et al
1008	U.S. Patent No. 8,359,521 to Kim et al.
1009	U.S. Patent No. 7,155,579
1010	5400 MCH Datasheet
1011	Microsoft Computer Dictionary (5 th Ed. 2002)
1012	U.S. Patent No. 3,560,935
1013	U.S. Patent No. 7,757,101
1014	U.S. Patent No. 5,388,074
1015	U.S. Patent Application Pub. 2007/0136523
1016	U.S. Patent No. 6,754,787
1017	U.S. Patent No. 5,438,536
1018	U.S. Patent No. 6,693,840
1019	U.S. Patent No. 8,074,034
1020	U.S. Patent No. 5,835,733

Exhibit #	Reference Name
1021 [NEW]	Deposition Transcript of Murphy

CERTIFICATE OF COMPLIANCE

I hereby certify that this Petitioners' Reply To Patent Owner's Response complies with the type-volume limitations of 37 C.F.R. § 42.24, because it contains 5,460 words (as determined by the Microsoft Word word-processing system used to prepare this reply), excluding the parts of the reply exempted by 37 C.F.R. § 42.24.

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CERTIFICATE OF SERVICE

I hereby certify that on this 13th day of December, 2017, copies of this
Petitioners' Reply To Patent Owner's Response and Ex. 1021 have been served in
its entirety by electronic mail on the following counsel of record for Patent Owner:

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