

Minutes of Meeting No. 158
JC-40 Digital Logic Committee

June 4, 2009

Montreal, Canada

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1.0 JC-40 Digital Logic Plenary

The JC-40 Plenary meeting opened at 8:00 AM on June 4, 2009. Mr. Smolka led the discussion of this group.

Self-introductions were completed by the attendees.

1.1.0 Patent Policy

The patent policy was reviewed.

Netlist indicated that they would be making disclosures during the meeting related to JC-40 efforts, and asked if JC-40 was maintaining an IP Tracking list. Response: Mr. Smolka indicated that he would be making a presentation during JC-40.4 (Memory Buffer TG) which includes an IP Tracking List. He further indicated that the list is being updated to reflect recent letters sent from the JEDEC office.

Discussion:

- A discussion ensued between one or more members and committee chairmen regarding whether a disclosure need be made during each presentation – especially if the material is related to related material made earlier and/or if the disclosure is included on the IP Tracking list. Mr. Kellogg indicated that he would discuss this question with Mr. Kelly for clarification, and respond back to the committee. He further indicated that repeated disclosing of IP (disclosing the same IP for each related showing) is and should not be a concern to the membership, although this may slow meeting progress.
- A chairman clarified the member disclosure requirements, as summarized in the JC-40 agenda, JC-42 agenda, etc.

Mr. Martinez disclosed that Netlist may have IP on the ballot related to item #142.11, in addition to other possible showings.

Discussion:

- A chairman indicated that disclosures should be made in a timely manner
- prior to the ballot counting whenever possible.

1.2.0 Minutes

A motion was made by Samsung and seconded by Montage to accept the minutes of the February 2009 as written.

Discussion:

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- Mr. Martinez proposed an amendment to the motion to make a change to page 11 of 19 in the published meeting minutes, including a verbal disclosure that Netlist has IP related to item #142.11.

Mr. Kellogg reviewed the February preliminary and published minutes and did not find a statement from Netlist during the discussion on item #142.11. He then indicated that the minutes for JEDEC meetings reflect the discussions held during the meeting – changes and/or additions to the minutes should be proposed if the minutes do not correctly reflect the discussions that took place during the meeting. He asked Mr. Martinez, as well as the committee, if they could recall the disclosure being made during discussions on that item in the meeting in question, with no response.

The proposed amendment was not approved by the original first and second to the motion.

The motion was dropped.

Motion by Netlist and seconded by Montage to approve the meeting minutes as written.

The motion passed by acclamation.

1.3.0 Agenda

The agenda was reviewed.

Mr. Smolka covered several topics from the agenda material, including:

- The new member's lunch takes place on Wednesdays approximately at noon – Charles Furnweger is the focal point for the luncheon.
- The JC-40 policies were reviewed, as included in the meeting minutes.

Mr. Smolka indicated that the committee has authorized a ballot on the policies in the February meeting, as item #150.00, with no ballot issued.

Motion by Silego and seconded by TI to re-authorize the PLL/Register TG to issue one or more ballots on the JC-40 policies, as described in the JC-40 agenda material uploaded on the JEDEC server.

Discussion:

- To update policies in the future (after balloting them), members were asked to make a first and second showing (per the policies) and ballot the changes for which a motion is passed to do so.
- The purpose of balloting the policies is to ensure each committee clearly

discloses and ballots their policies for publication in JM21 such that they are well understood, with any modifications taking place using a conventional balloting process.

The motion passed by acclamation.

Mr. Gervasi summarized the JEDECworks website (the presentation was made available on the server). TGs were asked to utilize this new website.

1.4.0 BoD Ballot Review

- Committee item #104.00B (JCB-09-40, DDR3/DDR3L SSTE32882 Register) passed BoD during the current quarter.

1.5.0 BoD Update

Mr. Quddus summarized key BoD and JEDEC activities over the past quarter, with this information posted on the local server. Some key points of his presentation (previously shown in the JC-16/42/45/64 Plenary meeting) included:

- The three Flash Summits held in the first quarter of 2009 were summarized. Mr. Quddus indicated that there was significant interest in the topics covered, as well as good attendance - especially in the Far East meetings.
- An LPDDR2 Workshop is planned for June 25th in Santa Clara, relating to the recent publication of the LPDDR2 standard by JEDEC. Mr. Quddus highlighted the extensive press coverage on the new standard.
- JEDEC efforts in China and Taiwan were summarized.
- New BoD members were identified, including Sean Fan (IDT) and Dinesh Maheshwari (Cypress).
- An updated copy of the JEDEC meeting location policy was shown – with discussion delayed until later in the meeting.
- An MOU was signed between JEDEC and SFF (Small Form Factor). Work is underway regarding an MOU with SNIA (to be discussed in August).
- The JEDEC marketing report was reviewed.
- The JEDEC website activities were reviewed.

1.6.0 Ballot Review

There were no ballots for review in this committee.

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2.0 JC-40.1 CMOS/BiCMOS Digital Logic

The JC-40.1 meeting opened at 8:32 AM on June 4, 2009. Mr. Williams led the discussion of this group.

2.1.0 Agenda

The agenda was reviewed.

2.2.0 Ballot Review

There were no ballots for review in this sub-committee.

2.3.0 Second Presentations

There were no second presentations in this sub-committee.

2.4.0 First Presentations

There were no first presentations in this sub-committee.

2.5.0 Task Group Update

2.5.1.0 #121.00 TG	JEDEC Instrumentation Chip Status
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The TG logistics were shown, with calls occurring on select Thursdays at 4:30 PM (PST). The TG is comprised of 15 member companies, with 6 members generally participating. Other committee members were asked to attend if interested in this topic.

Recent topics covered in the TG included discussions with two possible silicon vendors, in addition to work on updates to resolve known “holes” in the specification related to such items as the I2C command table, the block diagram and updates to the pin count and ballout.

Activities planned for the next quarter are related to the completion of updates to the device specification – with plans to show the presentation at the 3Q ‘2009 meeting.

Discussion:

- Has the SMBus been considered as an interface bus rather than the I2C bus? Response: the TG can consider this option.
- A comment was made that the SMBus is quite different than the I2C bus, running slower than the I2C bus. Making this change would be a significant modification to the design.
- A suggestion was made to ask Intel to bring the SMBus into JEDEC. A suggestion was made to ask the JEDEC office to draft a letter to Intel requesting that they bring the SMBus to JEDEC for standardization.
- Intel commented that it is not their specification.
- The suggestion was modified to ask the JEDEC office to draft a letter to the SMBus organization to ask that they make a JEDEC showing and consider standardization. It was further suggested that a letter be sent to NXP in regard to the I2C specification. NXP rep indicated that they already have sent a letter to JEDEC on I2C.

Secr. note: No I2C letter was located at the JEDEC office by the time the minutes were approved by Mr. Kelly. A follow-up will be required on this item.

Mr. Smolka agreed to work with Mr. Williams and the JEDEC office to request that the SMBus be brought to JEDEC for possible standardization.

3.0 JC-40.3 RDIMM Support Devices

The JC-40.3 meeting opened at 8:39 AM on June 4, 2009. Mr. Ammar led the discussion of this group.

3.1.0 Agenda

The agenda was reviewed and updated.

3.2.0 BoD Ballot Review

Mr. Ammar indicated that the sub-committee BoD ballot was covered in the JC-40 Plenary.

3.3.0 Ballot Review

3.3.1.0 #104.64 JC-40.3-09-79 DDR3/DDR3L SSTE32882 Co Parameter Update

The vote count was 18 yes, 0 no and 7 abstentions.

Yes comments:

- Intel: A design target for Co is still needed. Intel recommended that the TG continue to work on this and authorize a ballot.

Motion by Intel and seconded by Montage to re-visit the Co spec and authorize the TG to issue a ballot on the material.

The motion passed by acclamation.

The ballot was left on pass/hold.

3.3.2.0 #104.63 JC-40.3-09-80 DDR3 Register (SSTE32882) – Output Slew Update

The vote count was 11 yes, 2 no and 6 abstentions.

No Votes:

- Inphi: Note 1 should include all the drive strength settings. Inphi indicated that they agreed with Silego's comments as discussed in the May 27th TG call. Inphi indicated that their comment was addressed.
- Smart Modular: The change in the slew rate definition changes the ring-back characteristics of the modules, which will require module manufacturers to re-characterize RTT values for modules currently qualified and in production. Smart Modular indicated that their "no" vote was addressed.

Yes comments:

- IDT: Output CL test loads should be adjusted for moderate and strong settings.

- Silego: Silego made a showing (item #104.70), including the following comments (see the showing for more details):

 - An inconsistency in the specification was reviewed, with a proposed editorial change which had been agreed upon by the TG.

 - Note 1 on table 2 says "measured into test load at default register setting". The default setting results in light drive - still need to measure at moderate and strong. Silego proposed to change the note to add "except for RC3, RC4 and RC5 which are set according to the drive strength to be

measured.”

Motion by Silego and seconded by Inphi to editorially modify the SSTE32882 specification (not yet published) to editorially add the text for note 1 (slide 6 of their presentation), and to include the editorially modified text proposed by Silego in the current specification revision prior to publication.

The motion passed by acclamation.

3.3.3.0 #104.65 JC-40.3-09-85 SSTE32882 IDD and IID Max Limits

The vote count was 12 yes, 0 no and 7 abstentions.

Yes comments:

- Inphi: Add clarification to the meaning of “IBT off”, such as “RC8 = x111” as discussed in the TG. Response: This is already addressed in errata comments to be included in the current spec revision prior to publication.

Inphi indicated that their comment was addressed.

The ballot material was left on pass/hold.

3.3.4.0 #104.00B JC-40.4-06-208B DDR3/DDR3L SSTE32882 Register

The vote count was 10 yes, 0 no and 1 abstentions.

Yes Votes:

- Elpida: Yn and Yn# need to be swapped as an editorial change.
- Smart Modular: Table 24 should include the strong drive option since most vendors support this feature. Response: Being discussed in TG, will await feedback from TG.

Mr. Smolka indicated that the ballot was a fast track ballot, was sent to BoD and passed BoD voting (as previously reported).

All comments were addressed prior to issuing the BoD ballot.

3.4.0 Second Presentations

3.4.1.0 #153.01 Silego

DDR3 SSTE32882 for DDR3U 1.25V Applications

A marked-up DDR3 SSTE32882 specification was shown to include 1.25V support. Silego indicated that the specification is a draft document – the specification values need to be discussed in the TG. Other possible changes were verbally summarized.

Discussion:

- In response to a question, Silego indicated that the values in the specification include both estimates and copy/paste values. The specification is intended as a template for the final specification.

Motion by Silego and seconded by HP to authorize the PLL/Reg TG to work on the specification proposal and to issue one or more ballots on the specification.

Discussion items included the following:

- A question was asked as to whether the showing was a second showing. Response: Related item number #137.00 was previously shown by HP – this showing is intended to build on that material.
- A concern was raised that the material has not yet been discussed in the TG. Response: This is not a committee requirement.
- Are there any functional changes? Response: Expect that changes will relate to values, not functions.
- Do the values change from the 1.5V spec? Response: Driver strength is expected to remain the same.
- No simulation data has been completed in the RDIMM TG – this information is required prior to ballot authorization to determine if the proposal will meet the application requirements. Response: Let the TG work on the details and if a consensus is achieved, issue a ballot on the material.
- This is a template, built on a specification already completed and standardized by the committee.
- AMD indicated that they have completed extensive simulations but not yet shown results in the TG – the results can be shown if needed.

The motion passed by acclamation.

3.4.2.0 #137.00 HP

DDR3U Ultra Low Voltage Memory

The sponsors of the material was shown – including nine member companies. HP indicated that the material was shown earlier in the week (in JC-42 and JC-45). A special TG was previously formed, sponsored by AMD, to define the modules affected by 1.25V.

The proposed standardization of 1.25V is due to requests from customers to reduce power. Memory now represents 40% of power consumed in systems, with the memory percentage increasing.

With the expected DDR4 standardization and broad adoption schedule, there is too long of a gap from 1.5 and 1.35V memory devices to DDR4. A 1.25V transition device is needed. The current proposal is for a part that has a nominal voltage of 1.25V and is 1.35V tolerant (this topic will be discussed in the TG). The proposal is scaled from 1.35V, with proposed bus speeds of 800 – 1333 Mb/s.

Discussion:

- It would be good to see DRAM producers as sponsors as well.

3.4.3.0 #104.69 Silego

**DDR3 RCD/RDIMM tQSK
Consideration**

Silego indicated that the material was previously shown in the JC-45 RDIMM committee, with authorization to ballot in that committee. Additional work is required in this committee.

With the measurement procedure defined for tQsk, it is time to fine-tune the DDR3 RCD spec, which assumes ideal output clock. The Intent is not to make technical changes but to make changes that may be considered as editorial or close to that.

Table 38 of the current register specification was shown – output clock jitter not included in the tQsk specifications. Table 65 (Note b) of the DRAM specification was then shown. Every instantaneous setup and/or hold should satisfy the DRAM input specification values.

The table “Example of DDR3 Timing Budget for Post Register...” timing budget was then shown with areas of concern highlighted in red (relating to jitter).

Concerns included:

- There is a need for addition of tjit(hper) in the RDIMM timing budget.

- The current approach in the RDIMM specification does not appropriately account for the jitter.
- The specification is unclear in regard to a $\frac{3}{4}$ pre-launch case.

A copy of the consensus from validation TG was shown for tQsk. It was noted that the "Measurement procedure includes output clock jitter". Recommended specification changes were reviewed for the DDR3 RCD specification, followed by the proposed RDIMM specification changes and the proposed changes to table 38 of the buffer specification. A future JEP specification will emerge from the validation TG. Siligo indicated that there is no impact on the DIMM timings – this is just a different means of specifying the timings.

Discussion:

- A question was asked in regard to correlation between clock jitter and input jitter. Response: Because there is no input specification, devices will tend to meet the output specification.

Motion by Siligo and seconded by Micron to authorize the TG to issue a ballot on tQsk modifications as suggested by the presentation.

Discussion:

- As clarification, Siligo indicated that the Intention is that the PLL/Register TG will discuss the material and issue a ballot if a consensus is reached.

The motion passed by acclamation.

3.4.4.0 #104.68 Inphi

DDR3 Register SSTE32882 IBT Parameter Definition

The presentation was intended to clarify the IBT parameter. A new defined parameter to replace the mismatch tolerance parameter was proposed to make it easier to measure the mismatch on test equipment (automated and bench). The showing was in ballot form.

A modified version of table 37 in the SSTE32882 specification was shown, including the new parameter, applicable notes and a figure. The TG has considered this proposal.

Motion by Inphi and seconded by TI to authorize the TG to issue a ballot on this material.

The motion passed by acclamation.

3.4.5.0 #104.56A Intel

**CKE Power-Down Mode Footnote
Update**

Intel made a proposal to change the register CKE power down mode footnote – with the existing and proposed text reviewed. Associated timing diagrams were shown with the modified footnote.

Motion by Intel and seconded by Montage to authorize this re-ballot including the proposed modifications as shown.
The motion passed by acclamation.

3.5.0 First Presentations

There were no first presentations in this sub-committee.

3.6.0 Task Group Update

3.6.1.0 #122.00 TG

PLL/Reg TG Status Update

The TG logistics were shown, with calls held every Wednesday. The TG is now utilizing the JEDECworks website.

TG activities since the last committee meeting were summarized, including compilation of an updated specification revision (on server), discussions and ballots on Co, output slew rates and IDD/IID, discussions related to the IBT tolerance measurement and consideration of a new register package (8.5 mm x 11.0 mm).

Consensus votes were reviewed, primarily related to the TG activities previously summarized. A list of proposed editorial changes to the DDR3 SSTE32882 specification were then reviewed, as delineated on page 5 of the presentation, including:

- Correct the narrow package row “Y” name in tables 7, 8, 9 and 10 from “W” to “Y”
- Swap Yn# and Yn in figure 25
- Add RC8=x111, turning off all IBTs, to the IDD static operating current for clarification.
- Note 2 table 33: Need to add DCAS# to the list
- Change “J11” ball assignment name in table 6, page 23, from QABA2 to “QBBA2”

Ballot results were shown for this meeting. Future discussion topics were

then summarized; including DDR3 slew rate measurement, tQSKx clarification, Co specification discussion, DDR3 1866/2133 specification discussion, DDR3 1.2V discussion and DDR4 specifications.

Motion by Silego and seconded by Montage to authorize the TG to arrange and clean up fonts and tables and include the proposed editorial changes listed on page 5 of the presentation in the DDR3 pass/hold spec as editorial changes and to include them in the specification that has passed the BoD prior to publication of that specification if a 100% consensus vote is achieved that the changes are editorial.
The motion passed by acclamation.

Motion by Silego and seconded by Montage to authorize the TG to issue one or more ballots on the DDR3 and DDR3L register specification operating at 1866.
The motion passed by acclamation.

4.0 JC-40.4 FBDIMM Support Devices

The JC-40.4 meeting opened at 10:06 AM on June 4, 2009. Mr. Chung led the discussion of this group.

4.1.0 Agenda

The agenda was reviewed and updated.

4.2.0 Ballot Review

4.2.1.0 #142.24 JC-40.4-09-118 DDR3 Memory Single Buffer Ballout 0.65mm Pitch

Secr. note: A prior version of this material was balloted under item #142.14. This material is a re-ballot of that material.

The vote count was 16 yes, 1 no and 5 abstentions.

No votes:

- IDT: 8 DCS inputs are needed, 4 QODT pins are missing on the A and B sides, Test [2:0] should be defined as I/O, Aout should be defined as I/O, SMBus need not be on outer edge of pinout, corner pins should not be

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populated with pins, etc.

IDT indicated that they would be making a presentation in relation to their comment. IDT asked to have the ballot taken back to the TG for re-ballot.

Yes comments:

- Elpida: Need to consider 8 DCS inputs.
- IBM: IBM requires 8 DCS inputs (was "no" vote, changed to "yes" vote on voting machine based on sponsor indicating support for 8 DCS pins). IBM concurred that they accepted the response and their vote is now included as a "Yes" in the tally.
- Micron: Reverse the order of A-AV (numbering appears to be backward relative to JEDEC convention).
Micron indicated that their comment is incorrect, indicating that their comment is addressed.

Motion by IDT and second by Montage to send the ballot back to the TG and authorize the TG to re-ballot the material considering all voting comments and including 4 additional DCS inputs.

Discussion:

- IP Disclosure: Netlist indicated they have IP that may read on this material. Patent numbers were identified as 7532537 and 7289386.
- The sponsor indicated that their objective is to place the current ballot material on pass/hold, understanding that changes may occur.
- What is the benefit to leave on pass/hold as is if "no vote" comments have not been addressed? Response: By leaving on pass/hold, the current material provides some guidance to designers, albeit at some risk.
- A concern was raised in regard to making the addition of 4 DCS pins as an editorial change. Response: IBM indicated that they would be OK with enabling the TG to add the addition 4 chip selects as an editorial change.

Discussion continued regarding whether the 4 DCS addition is editorial as well as the rationale for leaving the ballot on pass/hold while authorizing the committee to do further work on the ballot.

The motion failed with a vote count of 5 against and 6 in favor.

Motion by Inphi and seconded by FormFactor to leave the ballot on pass/hold and authorize the TG to consider all comments and issue a re-ballot on this material.

The motion passed by acclamation.

4.2.2.0 #142.05A JC40.4-09-44A

**DDR3 LRDIMM Memory Twin
Buffer Ballout**

The vote count was 4 yes, 6 no and 11 abstentions.

The ballot failed by count. The voting results were quickly reviewed to determine if any feedback was included that was not already under consideration.

No votes:

- AMD: Single buffer consensus achieved.
- FormFactor: Single buffer is now the TG consensus.
- IBM: Require 4 additional chip selects.
- Inphi: The ballot has errors - several of which were listed in the voting response.
- Intel: Prefer single buffer.
- Samsung: The TG has agreed to a single buffer solution.

Discussion:

- Who decided on a single buffer? Response: The determination was made in the LR-DIMM TG by consensus. The TG information was reviewed in the JC-45 committee meeting.
- A comment was made that the JC-40/JC-45 committees did not make the determination to use single buffer. Response: Mr. Kellogg indicated that JC-40 can elect to standardize products not requested by a specific JEDEC committee.

IP Disclosure: Netlist indicated they have IP that may read on this material. Patent numbers were identified as 7532537 and 7289386.

4.2.3.0 #142.23 JC-40.4-09-110

**DDR3 MB Control Word Update –
CKE and ODT**

The vote count was 14 yes, 0 no and 6 abstentions.

Yes comments:

- Intel: Should clarify that “disabled” means that the outputs are Hi-Z (footnote #1). Response: The proposed change was accepted as an editorial change.
- Silego: Add two “reserved” rows for DBA1=0 and 1.

IP Disclosure: Netlist indicated they have IP that may read on this material. Patent numbers were identified as 7532537 and 7289386.

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Motion by IBM and seconded by Samsung to place the ballot material on pass/hold with the editorial changes defined in the voting comments by Intel and Silego, awaiting completion of the specification and sending the complete specification to the BoD.

The motion passed by acclamation.

4.2.4.0 #142.25 JC-40.4-09-127

**DDR3 MB FORC15 Rank
Multiplication Control Word**

The vote count was 15 yes, 0 no and 4 abstentions.

Yes comments:

- Hynix: Subject is in error. Response: Initially was incorrect but was later fixed. Ballot content was correct.
- Silego: Several typos were identified. Response: Accepted as editorial.

IP Disclosure: Netlist indicated they have IP that may read on this material. Patent numbers were identified as 7532537 and 7289386.

Discussion:

- Still using “#” signal for low active signals. Recommend changing this by using “_” to delineate low active signals.

Motion by AMD and seconded by Silego to leave the ballot material on pass/hold with the editorial changes covered in the voting responses, awaiting publication of the MB specification.

The motion passed by acclamation.

4.2.5.0 #142.26 JC-40.4-09-126

**DDR3 MB F0RC14 DRAM
Command Control Word**

The vote count was 15 yes, 0 no and 5 abstentions.

Yes comments:

- FormFactor: Correct spelling of “Mirrors”. Response: Accepted as editorial.
- Micron: Same as above.
- Silego: Several editorial changes were proposed, including typos and clarifications.

The ballot material was reviewed. Response: Accepted as editorial.

IP Disclosure: Netlist indicated they have IP that may read on this material.

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Patent numbers were identified as 7532537 and 7289386.

Motion by AMD and seconded by FormFactor to accept all proposed editorial changes and place the editorially modified ballot on pass/hold awaiting publication of the MB specification.
The motion passed by acclamation.

**4.2.6.0 #142.27 JC-40.4-09-123 DDR3 MB F0RC12 DRAM Interface
Training Control Word**

The vote count was 13 yes, 0 no and 7 abstentions.

Yes comments:

- Inphi: "Context" tends to confuse the meaning of this function. An alternate word is needed.

Motion by AMD and seconded by Silego to discuss clarification wording in the TG and if 100% consensus is achieved on the wording change, to place the editorially modified ballot material on pass/hold pending the completion of the MB specification.

Discussion:

IP Disclosure: Netlist indicated they have IP that may read on this material.
Patent numbers were identified as 7532537 and 7289386.

The motion passed by acclamation.

**4.2.7.0 #142.28 JC-40.4-09-124 DDR3 MB F0RC11 Parity Control
Word**

The vote count was 15 yes, 0 no and 5 abstentions.

Yes comments:

- Silego: Add (Default) after "OFF". Response: Accepted as editorial.

Motion by AMD and seconded by Silego to leave the editorially modified ballot material on pass/hold pending completion of the MB specification.

Discussion:

IP Disclosure: Netlist indicated they have IP that may read on this material.

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Patent numbers were identified as 7532537 and 7289386.

The motion passed by acclamation.

**4.2.8.0 #142.29 JC-40.4-09-125 DDR3 MB F[3-11]RC6 Connector
Interface Control Word**

The vote count was 14 yes, 0 no and 7 abstentions.

The ballot passed by acclamation.

Motion by AMD and seconded by FormFactor to leave the ballot material on pass/hold pending completion of the MB specification.

IP Disclosure: Netlist indicated they have IP that may read on this material. Patent numbers were identified as 7532537 and 7289386.

The motion passed by acclamation.

**4.2.9.0 #142.32 JC-40.4-09-116 DDR3 MB Control Word – Pre/Post
Launch Update**

The vote count was 12 yes, 0 no and 8 abstentions.

Yes comments:

- FormFactor: Not sure timing accuracy is good to so many significant digits. Response: The committee has not decided the number of significant digits (e.g. 3 to 4 digits) to the right of the decimal point. This question on accuracy should be considered in the TG. Is there a JEDEC standard on this (a hard metric on timing accuracy)?

Comments were made that the accuracy is determined by the application and that test devices are generally accurate within about 5%.

Mr. Keller indicated that he would consider having presentations in the DDR3 validation committee which can be brought to this committee regarding appropriate timing specification accuracy. He indicated that Agilent will also bring a presentation describing conventional processes.

- Silego: Two editorial changes were proposed - change "Delay Y" to "Y Delay" in Table 1 and in table 2, is the "2" after "Control Word" intentional? Remove this text.

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IP Disclosure: Netlist indicated they have IP that may read on this material.
Patent numbers were identified as 7532537 and 7289386.

Motion by IDT and seconded by FormFactor to place the ballot material on pass/hold with the editorial changes proposed by Silego.
The motion passed by acclamation.

4.2.10.0 #142.33 JC-40.4-09-117

**DDR3 MB Control Word – 3T
Update**

The vote count was 14 yes, 1 no and 6 abstentions.

No votes:

- FormFactor: The voting response included a request for clarification of a portion of the ballot material. Response: Mr. Chung provided a verbal clarification of the ballot text. Suggested moving “control signals” portion of the subject text into a note for clarification. Response: Accepted as editorial.

Yes comments:

- Silego: A typo was identified. Response: Accepted as editorial.

Motion by IDT and seconded by Montage to place the editorially modified material on pass/hold.

The motion passed by acclamation.

Discussion:

- A member commented that the agenda, on page 37, has several incorrect numbers and/or names.

IP Disclosure: Netlist indicated they have IP that may read on this material.
Patent numbers were identified as 7532537 and 7289386.

4.3.0 Second Presentations

4.3.1.0 #137.00 HP

DDR3 Ultra Low Voltage Memory

The sub-committee agreed that the material need not be re-shown in this sub-committee as it was already shown earlier in the committee meeting.

4.3.2.0 #142.31 IBM

MB 8CS Inputs

IBM indicated that an electronic first showing was made greater than 30 days prior to the committee meeting

The MB TG has achieved a consensus that the buffer will support 8 chip selects. A control word needs to be defined. Proposed updates to the F0RC13 (control word) table were shown.

Motion by IBM and seconded by Montage to authorize the TG to issue one or more ballots on the material.

The motion passed by acclamation.

IP Disclosure: Netlist indicated they have IP that may read on this material. Patent numbers were identified as 7532537 and 7289386.

4.3.3.0 #142.24A Inphi

**DDR3 Memory Single Buffer
Ballout (0.65 mm Pitch)**

Secr. note: The item number and filename on the JEDEC server reflect a showing of this material under prior item #142.14. Item #142.24 was subsequently assigned to this material.

Inphi indicated that the ballout was discussed during the ballot reviews earlier in the meeting. The proposed ballout includes all items on the TG consensus list up to this meeting, such as the 4 additional CS pins (IBM).

Inphi indicated that ballot authorization was granted earlier in the meeting.

4.3.4.0 #142.35 Inphi

MB Initialization Sequence

A high-level overview of the initialization sequence was shown, covering host operations prior to normal operation. The MB power-up timing was then shown and was described as being fundamentally the same as the SSTE32882 device.

The MB power-up table was reviewed, followed by the host configuration of the MB control words, the host MRS to configure the DRAM (the buffer simply forwards these commands), the MB-DRAM interface training (MB write-leveling to DRAM, read training, etc), after which normal operation can begin. The MB-DRAM write leveling steps and read training were then shown in greater detail – the TG will work the details.

Discussion:

- A request was made to change the text from "iMB" to "MB" where this shows up in the presentation.

4.3.5.0 #142.36 Inphi

MB Transparent Mode

Inphi indicated that the material was previously shown in JC-45. A request was made as to whether the material need be re-shown - no members asked to have this re-shown.

The material was not shown in the committee but was loaded on the server.

4.3.6.0 #142.38 Inphi

Scalability of SB-Based LR-DIMMs

Inphi indicated that the material was previously shown in JC-45. A request was made as to whether the material need be re-shown - no members asked to have this re-shown.

The material was not shown in the committee but was loaded on the server.

4.3.7.0 #142.40 IDT

SB Ballout Considerations

IDT indicated that the material was previously shown in JC-45 – the TG was asked consider these proposals to the single buffer ballout.

A request was made as to whether the material need be re-shown - no members asked to have this re-shown.

The material was not shown in the committee but was loaded on the server.

4.4.0 First Presentations

4.4.1.0 #142.42 IDT

**Memory Buffer SMBus CSR MAP
for LR-DIMM**

Consensus list items were reviewed:

- Eight functions (4 for JEDEC-use, 4 for vendor-specific use) were added to the consensus list (2/16/09)
- Each function is 256 bytes deep (2/16/09).
- A function map overview (FN0 – FN7) was added 2/16/09.

IDT indicated that the vendor-specific registers need not be defined as “host bus” or “DRAM bus” registers.

Motion by Montage and seconded by IDT to elevate the showing to be a second showing.
The motion passed by acclamation.

Motion by IDT and seconded by Intel to authorize the MB TG to issue one or more ballots on the material.
The motion passed by acclamation.

4.4.2.0 #142.43 IDT

Memory Buffer Membist for LR-DIMM

The MB TG consensus list was shown including items related to Membist. The rationale for including Membist was summarized, including the fact that the DRAM interface is fully hidden behind the buffer, the memory buffer does not have boundary scan of JTAG, Membist exercise all pins between the buffer and DRAM, etc. Membist exercises/stresses the DIMM with system-level timings – using the same settings the host uses, the DRAM interface must be fully trained before running Membist, etc.

Membist can further run data patterns, address patterns, include failure locators, determine margin at various operational corners, clear and check memory in boot phase.

Membist is started through SMBus or RCW (BIOS-level access). The memory buffer needs to know the number of rows and columns (through the host or other means). Can use an error indicator or the SMBus to report errors.

The presentation included the proposed use of Function 3 and Function 5 for Membist.

Motion by Montage and seconded by IDT to elevate the showing to be a second showing.
The motion passed by acclamation.

Motion by IDT and seconded by Montage to authorize the MB TG to issue one or more ballots on DFX features in the MB.

Discussion:

- SMBus is a very slow bus – consider use of I2C bus? Will affect effectiveness of the DFX features. Response: Will consider I2C in TG discussions.

IP disclosures

- Cray verbally disclosed IP related to US patent #7184916. A RAND letter is in place which may relate to this material - the RAND letter was not limited to the FB-DIMM.
- Netlist verbally disclosed that they may have IP that may apply to this proposal – Netlist will follow-up with the JEDEC office on this IP.
- Which committee will review this ballot? Response: To be counted in JC-40.4 as this is an MB function/feature.

The motion passed by acclamation.

4.4.3.0 #142.44 AMD

DDR3 LRDIMM Control Word Clarification

Table 14 F0RC7 was shown. AMD proposed deleting the wording associated with the buffer number. AMD indicated that similar changes should be made throughout the control word ballots (e.g. table 23, table 24, etc) to remove any reference to dual buffer cases.

Motion by AMD and seconded by Samsung to empower the TG to editorially make changes to the memory buffer control word ballots previously passed to reflect the use of a single buffer if a 100% consensus is achieved on the editorial modifications.
The motion passed by acclamation.

4.5.0 Task Group Update

4.5.1.0 #142.10 TG

DDR3 MB TG

The TG mission and goal was reviewed, followed by the ballots issued this quarter. The TG consensus list was then shown, including the recent decision in the TG to develop a single buffer solution.

The new JEDEC website information used by the TG was shown.

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Motion by Silego and seconded by Inphi to authorize the MB TG to issue one or more ballots based on the existing DDR3 register spec currently on pass/hold.

The motion passed by acclamation.

Mr. Chung indicated that this action empowers the MB TG to work on all aspects of the MB.

The TG logistics were shown, followed by the TG activity now underway, including straw polls related to several AMD proposals regarding memory refresh. Planned TG activity was reviewed for the next quarter, including two possible motions (not made during this presentation).

The consensus list was shown (50 items), followed by the IP tracking list. Mr. Smolka agreed to add to the list the new IP disclosures made during this meeting.

4.5.2.0 #154.00 TG

DDR4 VRD TG Report

The TG logistics were shown – the TG is currently a JC-45 TG, with 196 members over 60 companies and 10-15 members on each call. The scope is to consider of a voltage regulator on DIMM as proposed by HP's JC-45 item #2208.01.

A list of TG discussions and associated presentations was shown. The TG consensus list was shown, comprising one item.

The presenter requested that the JC-45 TG work jointly with JC-40.4 on this proposal.

Mr. Chung authorized that JC-40.4 participate with JC-45 and that the TG operate as a joint TG.

Motion by Inphi and seconded by (no second) to authorize the VRD logic device TG to issue one or more ballots on a VRD logic device.

Discussion:

- A concern was indicated that there have been no presentations made in this committee on a VRD device.
- An observation was made that the JC-40 committee requires 2 showings – the showing would need to be elevated to a second showing.

The TG report included a request for authorization to issue one or more ballots, as included on page 8 of the presentation.

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Discussion:

- Consider sending out a survey ballot on the 5 items listed.
- An observation was made that the listed items appear to be DIMM topics (JC-45).

The motion was withdrawn.

The chairman authorized a newly formed VRD Logic Device TG to issue one or more survey ballots as required.

Discussion continued in regard to the TG showing:

- The material presented related to Item #122.08, which was previously shown.
- Item #152.01 was shown in the February '2009 meeting, related to a voltage regulator on a DIMM in this committee.

The chairman empowered the TG to issue a survey ballot on item #2 on page 8 of the current showing.

Motion by Montage and seconded by Intel to authorize the VRD Logic Device TG to issue 4 ballots on items 1, 3, 4 and 5 on page 8 of 8 in the current presentation (JC-45 item #2208.00), based on the first showing on item #152.01 from the February '2009 meeting.

Discussion:

- A concern was raised that these items, as worded, are not JC-40 work items. JC-40 can't issue DIMM ballots from this committee – just device ballots.

An amendment was proposed to modify the motion to empower the TG to issue one or more ballots on component-related aspects to support the VRD.

The amendment was accepted by the first and second to the original motion.

The amended motion passed by acclamation.

5.0 JC-40.5 Logic Verification and Validation

The JC-40.5 meeting opened at 2:24 PM on June 4, 2009. Mr. Keller led the discussion of this group.

5.1.0 Agenda

The agenda was reviewed, after which the scope was reviewed.

5.2.0 Ballot Review

There were no ballots for review in this sub-committee.

5.3.0 Second Presentations

5.3.1.0 #149.02 Agilent/IDT/Inphi/Montage/TI MB Test Boards for Characterization, Validation and Failure Analysis

The motivation is to establish a means to do accurate and repeatable measurement of MB parametrics, power and protocol behavior - in and out of the system, under varying operating conditions, etc.

The proposed fixturing and probing was reviewed –including an MB parametric test fixture, a DIMM parametric test, a protocol test, a parametric DIMM system probe, device and DIMM probes.

A proposed LR-DIMM in-system test was described – including where testing may be done, the use of a DIMM parametric test board, etc. The DIMM parametric test board objectives and a block diagram were shown, followed by the MB component parametric test board objectives and block diagram. A protocol test board was then described, followed by a possible structure.

A request was made to form an LR-DIMM validation TG to further define and promote development of these tools for industry enablement.

Discussion:

- This topic should be brought up in JC-45 as well, since the proposal includes DIMM test platforms and test probing.
- A company indicated that any test fixtures, adapters and/or other test devices developed within the JEDEC committee must be made available to all (e.g. no discrimination) – preferably through a third party supplier.

The sub-committee chairman formed the requested TG with Victor Cai and Jeffrey Chung appointed by Mr. Keller as the TG chair and vice-chair respectively.

5.3.2.0 #133.03 Agilent

**DDR3 Register/PLL Validation
Procedure**

The presentation covered a tSTAOFF/tDYNOFF update – with procedure simplifications based on TG inputs

The test procedure draft was briefly shown – the document was loaded on the server for later review by members.

Motion by Agilent and seconded by (company name not captured) to authorize the DDR3 Register/PLL Validation TG to issue one or more ballots on the DDR3 Register/PLL test procedures, including input from Mr. Kelly.

Discussion:

- Clarification questions were asked regarding the test procedures.
 - In response to a question Mr. Keller indicated that the procedures do not require specific non-JEDEC equipment. Is there anything in the spec that is not readily available? Response: The proposed procedures do not require a specific platform or equipment. At this time, test platforms developed by Inphi, IDT, TI are included in the specification.
 - TI was asked if the RVB Lite test platform is available to everyone in a non-discriminatory manner. Response: Yes – provided by 3rd party supplier.
 - IDT was asked if the RVB test platform is available to everyone in a non-discriminatory manner. Response: Yes – provided by 3rd party supplier. - -
 - Inphi was asked if the CRB test platform is available to everyone in a non-discriminatory manner. Response: The CRB is an Inphi product (no RAND commitment was provided to the committee).
 - Mr. Kellogg indicated that he would speak to Mr. Kelly in regard to referencing a platform, in a JEDEC document, that is not available to everyone under RAND terms.
 - What if a customer says a device does not meet the specification on a test platform not available to the device manufacturer? If not available to all, then the test platform should not be referenced.
 - Mr. Keller indicated that the validation procedure would be balloted for publications as a JEP document (as an application note).
- Discussion continued consistent with earlier comments.

Mr. Keller indicated that the TG should consider feedback from Mr. Kelly in preparation of any such ballots.

The motion passed by acclamation.

5.4.0 First Presentations

5.4.1.0 #142.41 Inphi

LR-CTC Concept for MB

Inphi reviewed a test platform having a fully configurable environment for the MB, supporting 3 DIMMs per channel and requiring minimal external equipment.

The hardware feature set was summarized, including memory access to all ranks/slots, a user configurable memory-testing engine, MB control register access (read/write), configuration of memory controller via SPD, Vref and VDD margining, etc.

The software feature set was then summarized, including an easy to use GUI interface, GPIB and LAN access to external equipment, fully programmable test vector development, GUI access to all testing features, compiler for customized memory testing, etc.

The design methodology was shown, including a block diagram of what the solution would look like as well as a representative photo.

An initial list of tests was reviewed, including single bit and SSO delay testing, parity functionality testing, GND/VDD bounce due to SSO, signal integrity, protocol testing, parametric testing, etc.

5.4.2.0 #133.04 Silego

DDR3 RCD tQsk Measurement Procedure

Silego indicated that the material was previously shown to the TG on May 28th. The TG has reached a consensus, with the material almost in ballot ready form on the server.

The proposed document was shown to the committee, with the committee asked to review the proposed document in more detail as time permits. The document references all 3 test platforms – thereby potentially have the same concerns regarding platform availability as discussed earlier in the meeting. The TG will await and consider feedback from Mr. Kelly.

The test setup and test procedure were reviewed with examples of clock/data capture waveforms shown. The document described how to calculate tQsk from the measurement example.

Silego indicated that the document is pretty much ready to go except for the board availability concern.

Motion by Silego and seconded by Sun to elevate the material to be considered as a second showing.
The motion passed by acclamation.

Motion by Silego and seconded by Netlist to authorize the TG to issue a ballot on this test procedure, with the same criteria as item #133.03.

An amendment was proposed to modify motion to remove reference to the CRB.

Discussion:

- A comment was made that a JEP document may be different than a JESD document as related test board references and availability.

The proposed amendment was not accepted by the first and second to the original motion.

Discussion:

- The RVB and RVB-lite boards are readily available whereas the CRB does not appear to be. The document should not reference the CRB if it is not readily available.

The motion passed by acclamation.

5.4.3.0 #133.05 Silego

**DDR3 RCD Plug-In Test Card
Errata**

A signal integrity issue was observed on the JEDEC DDR3 RCD plug-in test card when running an SSO pattern. The QAxx (left side) was found to be worse than the QB (right side).

The optimal solution would be a new design, adding decoupling capacitance on the VTT and VDD planes near the termination resistors.

The existing test cards can be modified by adding capacitance between VTT and GND. The proposed changes were described and shown. The optimal solution was found to add four 0.01uF caps (waveform examples were shown with 0 caps, 2 caps and 4 caps at two conditions). Information shown indicated that far-end (long) signal traces do not require added caps.

Two options were then summarized:

- 1) Issue an errata to customers of the DDR3 RCD PIC through CST (the board supplier)

2) Re-design the DDR3 RCD PIC for proper referencing/decoupling (reference VDD, add decoupling caps between VDD and VTT).

Discussion:

- It was observed that some slides show 0.1uF, others show 0.01uF.

Response: Silego will check to see which is correct.

- Do using companies need help to do the re-work Silego is suggesting?

Response: They should not need help as the re-work is relatively easy.

- CST indicated that there is no inventory of unsold boards and indicated a willingness to send out a letter with proposed errata to purchasers.

Mr. Keller indicated that work will be done to initiate a design modification should new boards be ordered, and that the TG will review the design modification. In addition, errata will be prepared such that CST can issue it. The errata will be prepared by Silego.

5.5.0 Task Group Update

5.5.1.0 #133.00 TG

DDR3 Register/PLL Validation TG Report

The TG logistics were shown, with meetings every week held after the Register/PLL TG call. About 34 companies and 140 members are included on the TG roster, with 6 – 12 participating in a typical call.

Showings and discussions summarized were summarized including tDYNOFF/tSTAOFF, tQSK, low voltage register/PLL measurements, slew rate and instrument performance requirements, etc. Remaining TG work was also summarized.

The TG consensus list was shown, which included a consensus that procedures should support all 3 test platforms (RVB, CRB and RVB-lite) where possible. Other consensus items included parameters to be measured, 200 cycle TJ model is normative (10K cycles used previously), 1E-12 BER method is informative, etc.

Two proposed jitter specification methodologies were shown – The “N-Cycle” (more traditional) approach does tend to be optimistic. Companies were asked to provide input. The specification methodology may require modification in the future for higher speeds to maintain closure.

6.0 Other Committee Business

- Inphi indicated that any test boards, related hardware and source code developed by them for such test boards would be turned over to a 3rd party for sale and distribution. In addition, the design would be made available as an open source design (FPGA code made available). As clarification, Inphi indicated that this would apply to the CRB, with the CRB BoM and all related materials to be provided to CST for distribution.

- A member asked the committee chairman, Mr. Smolka, to adopt the JC-42/45 Excel spreadsheet format for the showings and ballots. Mr. Smolka agreed that this would be done.

- A clarification question was asked regarding the meeting date and start time for JC-40, given that the JC-16/42/45/63 plenary session agreed to change the 3Q '2009 meeting start date to Tuesday, September 8th (Monday is Labor Day in the U.S.).

Discussion:

- Can the meeting week be compressed to 4 days? Response: Unless agreed upon by the committee chairmen (some of which were not present), it was recommended that reserve a meeting room for Saturday.

- Mr. Smolka indicated that if JC-40 can start by 10 AM on Friday, and run long on Friday if needed, the committee would complete their activities on Friday. Mr. Rhoden agreed to contact the other committee chairmen to determine if those meetings will end such that JC-40 will start no later than 10 AM Friday (each meeting day may need to run long).

Motion by Silego and seconded by TI to modify any related prior motions made during this meeting to permit inclusion of the CRB in the ballot material

The motion passed with a vote count of 1 opposed and 4 in favor.

7.0 Adjournment

Motion by Intel and seconded by Google to adjourn the meeting.
The motion passed by acclamation.

The meeting adjourned at 4:07 PM on June 4, 2009

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**THIS MEETING WAS CONDUCTED IN ACCORDANCE WITH JEDEC
LEGAL GUIDES, JM5, AND THE JEDEC MANUAL OF ORGANIZATION
AND PROCEDURE, JM21-N.**

REVIEWED/CORRECTED AND AUTHORIZED FOR RELEASE BY:

Approved on: June 24, 2009
JC-40 Chairman, John Smolka

The following individuals did review/approve the minutes:

Approved on: June 24, 2009
JC-40.1 Sub-Committee Chairman, Rick Williams

Approved on: June 30, 2009
JC-40.3 Sub-Committee Chairman, Ramzi Ammar

Approved on: June 20, 2009
JC-40.4 Sub-Committee Chairman, Jeffrey Chung

Approved on: July 1, 2009
JC-40.5 Sub-Committee Chairman, Perry Keller

Approved on: June 17, 2009
Legal Approval, John Kelly

Approved on: June 16, 2009
Secretary, Mark Kellogg