

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner

Patent No. 10,474,595

Issued: November 12, 2019

Filed: December 28, 2017

Inventors: Hyun Lee

Title: Memory Module Having An Open-Drain Output Pin For Parity Error
 In a First Mode and For Training Sequences In A Second Mode

Inter Partes Review No. IPR2022-00064

DECLARATION OF JULIE CARLSON

I, Julie Carlson, declare as follows:

1. I have personal knowledge of the facts set forth herein, and if called to testify, I could and would competently testify to the same.
2. I have been involved in semiconductor standardization and publication services for over twenty years. For nearly all of this time, I have worked at JEDEC, a standards-setting organization for the microelectronics industry, to edit, publish, and maintain JEDEC business records and standards developed by its numerous committees and subcommittees.
3. I have been involved with the standardization and publication activities of JEDEC continuously since 1997. I was the Manager of Standards and Publications at JEDEC from February 1997 through June 2005. Since June 2005, I have continued to work for JEDEC as a Consultant where my responsibilities include the maintenance and publication of JEDEC documents and standards. In addition, I am familiar with JEDEC's historical record-keeping and publication practices since at least 1992, based on my review of

JEDEC's business records since that time and my regular discussions with JEDEC employees and members.

4. For over 50 years, JEDEC has been the global leader in developing and publishing open standards for the microelectronics industry. JEDEC's membership consists of more than 3,000 volunteers representing nearly 300 member companies, and includes key technical individuals from most device, assembly, system and testing companies. JEDEC publications and standards are adopted worldwide. JEDEC is accredited by ANSI and maintains liaisons with numerous standards bodies throughout the world.
5. JEDEC membership is open to any company or organization, or one of its related entities, that manufactures electronic equipment or electronic-related products or related services. Anyone interested can join JEDEC online, at JEDEC.org. When joining, any interested person can join any committee, including JC-40: Digital Logic (which includes its subcommittees, such as JC-40.4: Registered & Fully Buffered Memory Support Logic) and JC-45: DRAM Modules (which includes its subcommittee, such as JC-45.4: Fully Buffered DRAM Modules). The joining members would have access to documents available to the committees and subcommittees the members join, such as

Exhibits A-J attached hereto, available to any such members who joined JC-40.4 and JC-45.4.

6. JEDEC maintains business records to document when standards are modified, balloted, and approved, and when its standards are published. Through my work at JEDEC, I am familiar with these business records and standardization practices. JEDEC employees and members generate and keep these records, which are routinely generated at or around the time of the event that they describe, and keep them.
7. Committee Item Number 142.35 (hereinafter “Item Number 142.35”), attached as Exhibit A, with the Subject “LRDIMM DDR3 Memory Initialization Chapter Proposal” is a proposal to the JC-40.4 committee for ballot approval. Ex. A. On November 9, 2009, Item Number 142.35 was approved by DDR3 MB TG (“Task Group”) and referred to JC-40.4 to vote for ballot approval. See Ex. A at 1; *see also* Ex. B at 1. After approval, Committee Letter Ballot JC-40.4-09-320 (hereinafter “Letter Ballot for Item Number 142.35”), attached as Exhibit B, was distributed to the members of JEDEC JC-40.4 on November 11, 2009. Ex. B. Letter Ballot for Item Number 142.35 itself distributes Item Number 142.35 to JC-40.4, in the link labeled “Download NB09320-.pdf.” Ex. B. A true and

correct copy of Item Number 142.35 is attached as Exhibit A, and a true and correct copy of Letter Ballot for Item Number 142.35 is attached as Exhibit B. As I noted above, JEDEC maintains all item numbers and letter ballots, such as Exhibits A and B, as business records, and it is the general practice of JEDEC employees and members to generate them at or around the time of the event they describe, and to keep them.

8. “JEDEC Compilation of Tallies for JC-40 CMOS Digital Logic and point committees” (hereinafter, “JEDEC Tally for Item Number 142.35”), attached as Exhibit C, records JEDEC member votes for, among others, Letter Ballot for Item Number 142.35 on page 21. See Ex. C at 1, 21 (identifying “Committee Letter Ballot, JC-40.4-09-320, 142.35”). JEDEC Tally for Item Number 142.35 also confirms that Letter Ballot for Item Number 142.35 was distributed on November 11, 2009 to JC-40.4. Ex. C at 21. JEDEC Tally for Item Number 142.35 itself also provides a link to Item Number 142.35, in the link labeled “Click here for NB09320-.pdf.” Ex. C at 21. Letter Ballot for Item Number 142.35 was posted to JEDEC’s Voting Machine, and the Voting Machine produced JEDEC Tally for Item Number 142.35. JEDEC Tally for Item Number 142.35 records that 20 companies voted on Letter Ballot for Item Number 142.35, and identifies those companies and their votes. Ex. C at 21.

Those companies include Advanced Micro Devices Inc. (AMD), Cray Inc., Dell Inc., Elpida Memory Inc., Hynix Semiconductor, IBM Corp., Inphi Corp., Integrated Device Technology Inc., Intel Corp, Kingston Technology Co. Inc., Legacy Electronics Inc., Micron Technology Inc., Netlist Inc., Nvidia Corp., NXP Semiconductors, Samsung Semiconductor, Silego Technology, Smart Modular Technologies, Inc., Sun Microsystems Inc., and Texas Instruments Inc. Ex. C at 21.

9. JEDEC Tally for Item Number 142.35 records in the “DoV” column that those companies voted between November 13, 2009 and December 3, 2009. Ex. C at 21. The compilation of votes was generated on December 4, 2009, one day after the expiration date of the ballots. Ex. C at 1. A true and correct copy of the JEDEC Tally for Item Number 142.35 is attached as Exhibit C. As I noted above, JEDEC maintains all vote tallies, such as those contained in Exhibit C, as business records, and it is the general practice of JEDEC employees and members to generate them at or around the time of the event they describe, and to keep them.

10. Committee Item Number 2192.44 (hereinafter “Item Number 2192.44”), attached as Exhibit D, with the Subject “DDR3 LRDIMM Design Specification

Body” is a proposal to the JC-45.4 committee. Ex. D at 1. Ex. D at 1. After approval, Committee Letter Ballot JC-45.4-09-321 (hereinafter “Letter Ballot for Item Number 2192.44”), attached as Exhibit E, was distributed to the members of JEDEC JC-45.4, on November 16, 2009. Ex. E at 1. Letter Ballot for Item Number 2192.44 distributes the Item Number 2192.44, in the link labeled “Download HB09321-.pdf.” Ex. E at 1. Item Number 2192.44 notes that, although the DDR3 LRDIMM Design Specification Body has changes that are highlighted in the document, the “entire specification is being balloted.” *Id.* A true and correct copy of Item Number 2192.44 is attached as Exhibit D. A true and correct copy of Letter Ballot for Item Number 2192.44 is attached as Exhibit E. As I noted above, JEDEC maintains all item numbers and letter ballots, such as Exhibits D and E, as business records, and it is the general practice of JEDEC employees and members to generate them at or around the time of the event they describe, and to keep them.

11. “Tally of Votes, Committee Letter Ballot JC-45.4-09-321, 2192.44” (hereinafter, “JEDEC Tally for Item Number 2192.44”), attached as Exhibit F, records JEDEC JC-45.4 votes for Letter Ballot for Item Number 2192.44. Ex. F at 1-2. Letter Ballot for Item Number 2192.44 was posted to JEDEC’s Voting Machine, and the Voting Machine produced JEDEC Tally for Item Number

2192.44. JEDEC Tally for Item Number 2192.44 provides that 22 members voted on Letter Ballot for Item Number 2192.44, identifies those companies and their vote and any comment they made. Ex. F at 1-4. Those companies include Advanced Micro Devices Inc., Buffalo Inc., Cray Inc., Elpida Memory Inc., FormFactor Inc., Hynix Semiconductor, I-O Data Device Inc., IBM Corp., Inphi Corp., Integrated Device Technology Inc., Intel Corp., Kingston Technology Co. Inc., Legacy Electronics Inc., Micron Technology Inc., Nanya Technology Corp., Netlist Inc., Nvidia Corp., PNY Technologies Inc., Samsung Semiconductor, Sun Microsystems Inc., Tyco Electronics Corp. Ex. F at 1-2.

12. JEDEC Tally for Item Number 2192.44 records that those companies voted between November 16, 2009 and December 3, 2009 on Letter Ballot for Item Number 2192.44. Ex. F at 1-3. JEDEC Tally for Item Number 2192.44 confirms that Item Number 2192.44 was distributed to JEDEC committee JC-45.4 on November 16, 2009, in the link labeled "Attachment: HB09321-.pdf." Ex. F at 1. A true and correct copy of the JEDEC Tally for Item Number 2192.44 is attached as Exhibit F. As I noted above, JEDEC maintains all vote tallies, such as Exhibit F, as business records, and it is the general practice of JEDEC employees and members to generate them at or around the time of the event they describe, and to keep them.

13. Exhibit G identifies Inphi Corp. as making the presentation “MB Initialization sequence Item 142.35,” (hereinafter, “142.35 Presentation”). Ex. G at 1. The 142.35 Presentation is dated June 4, 2009, and was presented to JC-40, as discussed as noted hereafter. Ex. G at 1. A true and correct copy of the 142.35 Presentation is attached as Exhibit G. As I noted above, JEDEC maintains specification proposals, such as Exhibit G, as business records, and it is the general practice of JEDEC employees and members to generate them at or around the time of the event they describe, and to keep them.
14. JEDEC’s “Minutes of Meeting No. 158, JC-40 Digital Logic Committee” (hereinafter “158 Meeting Minutes”) is attached as Exhibit H. The 158 Meeting Minutes provide that the 142.35 Presentation by Inphi Corp. was discussed at the June 4, 2009 JEDEC JC-40 meeting in Montreal, Canada as agenda number 4.3.4.0. See Ex. H at 21. Exhibit H includes a full list of the JC-40 member attendees at the June 4, 2009 meeting. See Ex. H at 1-2. A true and correct copy of the 158 Meeting Minutes is attached as Exhibit H identifying this disclosure. As I noted above, JEDEC maintains meeting minutes, such as Exhibit H, as business records, and it is the general practice of JEDEC employees and members to generate them at or around the time of the event they describe, and

to keep them.

15. Attached as Exhibit I is a true and correct copy of the JEDEC Manual of Organization and Procedure JM21N (hereinafter “JM21N”) in effect commencing May 2008. Attached as Exhibit J is a true and correct copy JEDEC Manual of Organization and Procedure JM21P, which revises JM21N, that went into effect commencing May 2010.

I, Julie Carlson, do hereby declare and state, that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

Executed on June 3, 2020.


_____ (signature)

Julie D. Carlson (name printed)

Exhibit A



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COMMITTEE LETTER BALLOT

COMMITTEE: JC-40.4

Committee Item Number: 142.35

Subject: LRDIMM DDR3 Memory Initialization Chapter Proposal

Background: At September '09 JEDEC meeting in San Jose, "motion by Intel and seconded by Montage to authorize the TG to issue one or more ballots on the items listed on pages 3 and 4 of the presentation that have item numbers, have been shown in the committee and for which the TG has reached a consensus".

The motion passed by acclamation.

This ballot proposal is to specify LRDIMM DDR3 Memory Initialization, and has been approved by DDR3 MB TG on 11/09/2009.

Keywords: DDR3, MB, Memory Buffer, LRDIMM, Initialization

PROPOSED

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6 Initialization

6.1 Initialization Overview

The sequence of steps below is an overview of the power-up initialization of the Memory Buffer. Figure 1 shows a graphical representation of the same steps. Detailed requirements for each step are provided in the following sections. Note that the sequence below does not distinguish between host HW and host SW (i.e. BIOS).

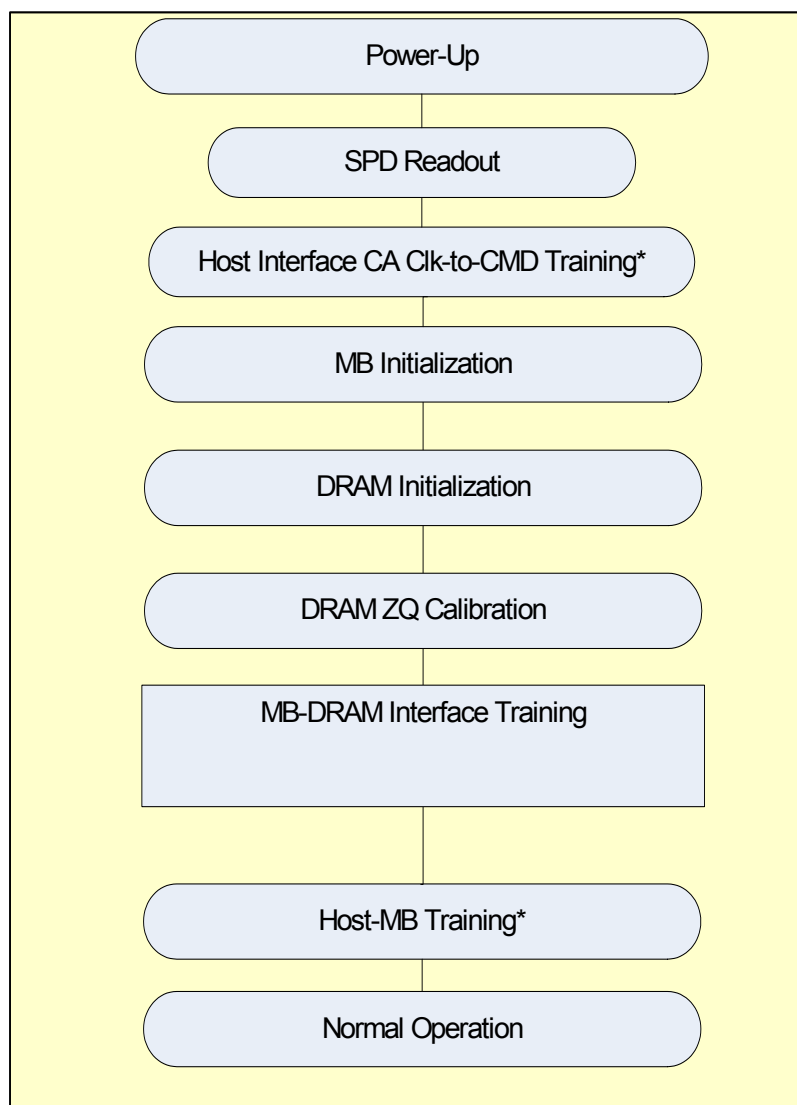
1. Power-Up (Same requirements as 882)
 - a. Ramp of voltage rails
 - b. Generation of stable clock
 - c. De-assertion of RESET#
 2. Determination of DIMM configuration via SPD read out
 3. CA Clock to CMD Training¹
 - a. Sets the optimal phase of the clock to CA and Ctrl signals.
 4. Memory Buffer Initialization
 - a. Host initializes buffer control words
 5. DRAM Initialization
 - a. Host initializes DRAM MRS registers
 6. DRAM ZQ Calibration
 - a. Host issues ZQCAL command to DRAM
 7. Memory Buffer to DRAM Interface Training
 - a. Done by the buffer, triggered by host RCW write
 - b. Write Leveling
 - c. Read Enable training
 - d. Read/Write DQ/DQS training²
- Host can wait for a per-physical rank time-out of tCAL=10ms or periodically poll the buffer via SMBus CSR read or wait for ERROUT#.
8. Host to Memory Buffer Interface Training³
 - a. Done by host
 9. Normal Operation

1. This step is optional for the MB but may be done by some platforms. No special support by the MB is required.

2. This step is optional for the MB but may be required for stable DIMM operation.

3. This step is optional for the MB but may be done by some platforms.

Figure 1 — Initialization Overview



* This step is optional for the MB but may be done by some platforms

6.2 Power-on Initialization

The Memory Buffer can be powered-on at 1.5V or 1.35V. After the voltage ramp, stable power is provided for a minimum of 200 μ S with RESET# asserted. When the reset input RESET# is LOW, all input receivers are disabled, and can be left floating. The MB output pin QRST# follows the MB input pin RESET#. Therefore the reference voltage (V_{REF}) doesn't need to be stable. In addition, when RESET# is LOW, all control registers are restored to their default states. The outputs QACKE[3:0] and QBCKE[3:0] must drive LOW during reset. All other outputs must float. As long as the RESET# input is pulled LOW the register is in low power state and input termination is not present. A certain period of time (t_{ACT}) before the RESET# input is pulled HIGH the reference voltage needs to be stable within specification, the clock input signal must be stable, the register inputs DCS[1:0]# must be pulled HIGH to prevent accidental access to the control registers and DCKE[2:0] as well as DCKE3/DODT[1] must be pulled LOW.

6.2.1 Clock Stabilization Time t_{STAB}

During PLL stabilization time t_{STAB} the memory buffer is not fully operational. In order to avoid invalid commands being sent to the DRAMs some rules apply to the inputs of the buffer:

- All DCS signals need to be kept high. No DRAM command or control word write¹ may take place.
- All DCKE signals don't change their state.
- DODT[0] or DODT[1:0] signals (depending on F0RC6 setting) are kept at a stable valid logic level.

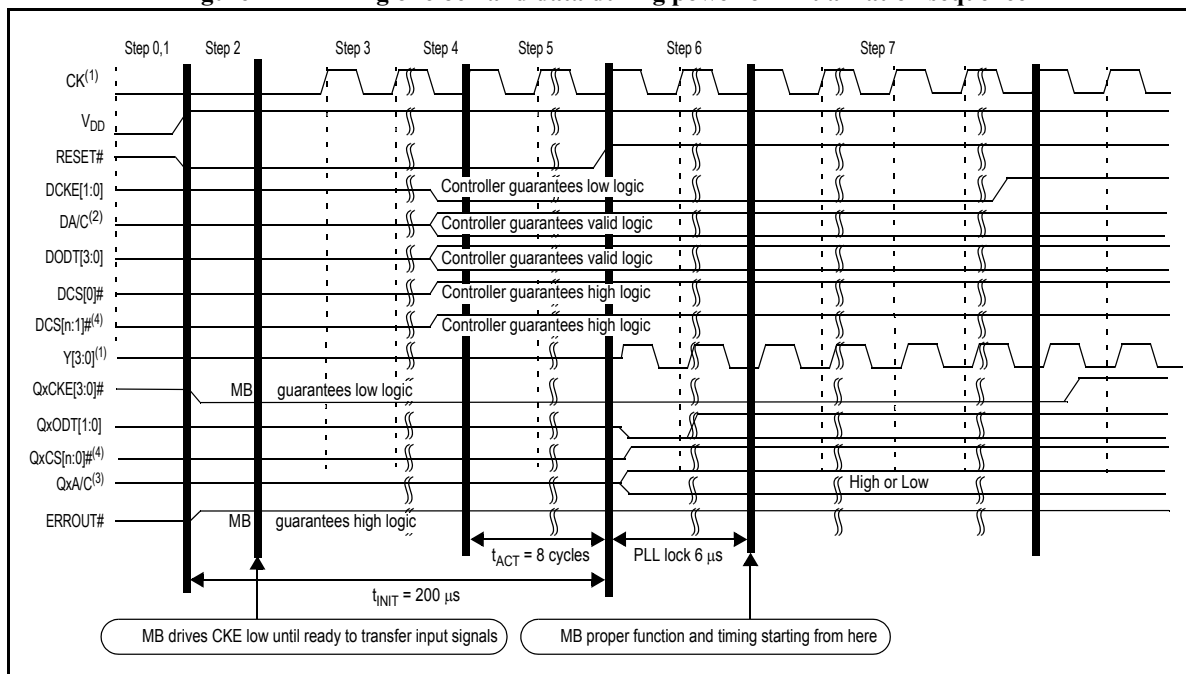
These rules apply to any instance where stabilization time t_{STAB} is required:

- Exit from Reset
- Exit from clock stop power down
- Changing clocking related registers (F0RC2, F0RC10, F0RC11, F1RC8, F1RC11-F1RC15)²
- Changing input clock frequency during boot or run time

Since the buffer has not reached a stable state the termination on the host interface will be undefined before the end of the stabilization time.

After reset and after the PLL stabilization time (t_{STAB}) the device must meet the input setup- and hold specification, as well as accept and transfer input signals to the corresponding outputs. The RESET# input must always be held at a valid logic level once the input clock is present.

Figure 2 — Timing of clock and data during power-on initialization sequence



1. No control word writes are allowed during t_{STAB} after reset/frequency change/clock stop. Control word writes are allowed during t_{STAB} after clocking related register write.

2. These requirements mean that we have to wait two t_{STAB} times during every initialization, one after RESET# de-assertion and one after all the clocking related control words have been written.

- (1) CK# and Y[3:0]# left out for better visibility
 (2) DCKE[2:0], DCKE[3]/DODT[1], DODT[0] and DCS0[3:0]# are not included in this range
 (3) QxCKE[3:0], QxODT[1:0], QxCS[7:0]# are not included in this range
 (4) n = JEDEC standard DIMMs, n = 7 for non-JEDEC applications
 (5) n = 3 for dual or quad rank DIMMs, n = 7 for octal rank DIMMs

From a device perspective, the initialization sequence must be as shown in Table 1

Table 1 — MB Device Initialization Sequence^a

Step	Power	Inputs: Signals provided by the controller								Outputs: Signals provided by the device					
		RESET#	Vref	DCS# [n:0] ^b	DODT [1:0]	DCKE [3:0]	DA/C	PAR_IN	CK CK#	QCS# [n:0] ^c	QODT [1:0]	QCKE [3:0]	QxA/C	ERR OUT#	Y[3:0] Y#[3:0]
0	0V	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	Z	Z	Z	Z	Z	Z
1	0-->V _{DD}	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	L	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z
2 ^d	V _{DD} 1.5V-->1.35V 1.35V-->1.5V	L	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	L	Z	Z	L ^e	Z	H ⁴	Z
3	V _{DD}	L	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	running	Z	Z	L	Z	H	Z
4	V _{DD}	L	X or Z	H	X or Z	L	X or Z	X or Z	running	Z	Z	L	Z	H	Z
5	V _{DD}	L	stable voltage	H	X	L	X	X	running	Z	Z	L	Z	H	Z
6	V _{DD}	H	stable voltage	H	X	L	X	X	running	H	L ^f	L	X	H	running
7 ^g	V _{DD}	H	stable voltage	H	X	X	X	X	running	After Step 6 (Step 7 and beyond), the device outputs are as defined in the device Function Tables (see Table 12, Table 14 and Table 16).					

a. X = Logic LOW or logic HIGH. Z = floating.

b. n = 3 for JEDEC standard DIMM, n = 7 for non-JEDEC application

c. n = 3 for dual or quad rank DIMMs, n = 7 for octal rank DIMMs.

d. The system may power up using either 1.5V or 1.35V. The BIOS reads the SPD and adjusts the voltage if needed from 1.35V to 1.5V or from 1.5V to 1.35V. After the voltage transition, stable power is provided for a minimum of 200 uS with RESET# asserted.

e. QxCKE[3:0] and ERR0UT# will be driven to these logic states by the register after RESET# is driven LOW and VDD is 1.5V or 1.35V (nominal).

f. This indicates the state of QxODT[1:0] after RESET# switches from LOW-to-HIGH and before the rising CK edge (falling CK# edge).

g. Step 7 is a typical usage example and is not a MB requirement.

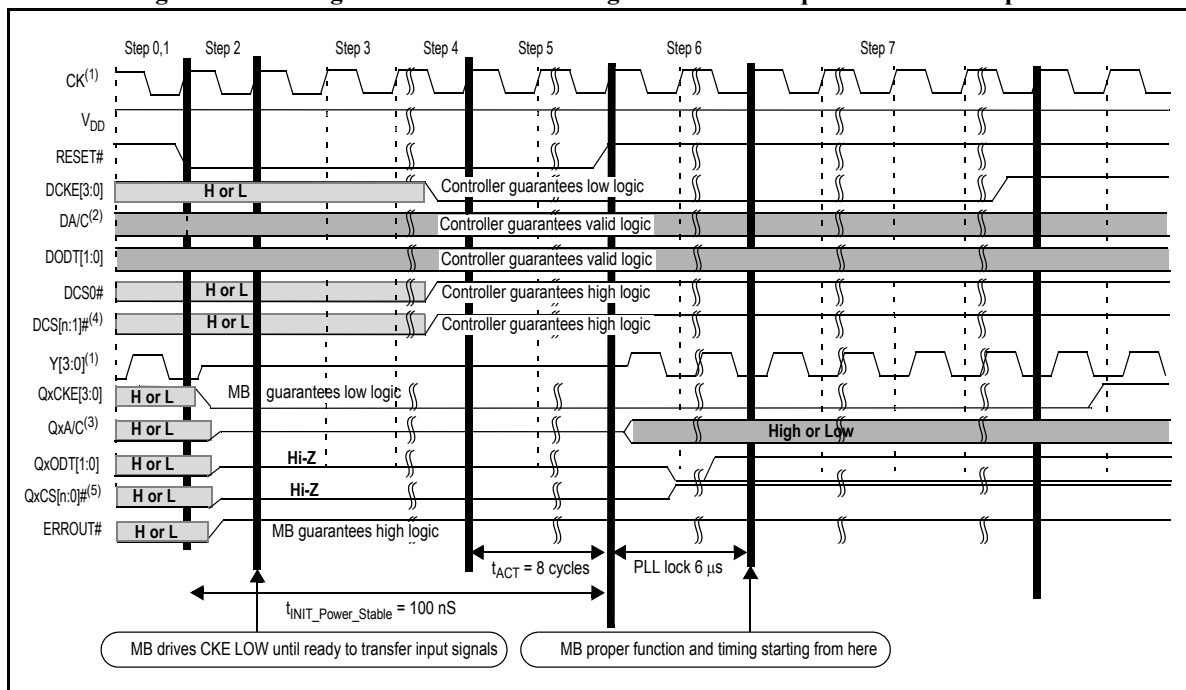
To ensure defined outputs from the register before a stable clock has been supplied, the memory buffer must enter the reset state during power-up. It may leave this state only after a LOW to HIGH transition on RESET# while a stable clock signal is present on CK and CK#. In the DDR3 LRDIMM application, RESET# is specified to be completely asynchronous with respect to CK and CK#. Therefore, no timing relationship can be guaranteed between the two.

As part of the initialization all control words are reset to their default state which is "0", except when explicitly defined otherwise. After initialization, the host only needs to write to those control registers whose contents need to be changed.

6.3 Initialization with Stable Power (Soft Reset)

The timing diagram in Figure 3 depicts the initialization sequence with stable power and clock. This will apply to the situation when we have a soft reset in the system. RESET# will be asserted for minimum 100ns. This RESET# timing is based on DDR3 DRAM Reset Initialization with Stable Power requirement, and is a minimum requirement. Actual RESET# timing can vary base on specific system requirement, but it cannot be less than 100ns as required by JESD79-3 Specification.

Figure 3 — Timing of clock and data during initialization sequence with stable power



(1) CK# and Y[3:0]# left out for better visibility

(2) DCKE[2:0], DCKE[3]/DODT[1], DODT[0] and DCS0[3:0]# are not included in this range

(3) QxCKE[3:0], QxODT[1:0], QxCS[7:0]# are not included in this range

(4) n = JEDEC standard DIMMs, n = 7 for non-JEDEC applications

(5) n = 3 for dual or quad rank DIMMs, n = 7 for octal rank DIMMs.

Table 2 — MB Device Initialization Sequence^a when Power and Clock are Stable

Step	Power	Inputs: Signals provided by the controller								Outputs: Signals provided by the device					
	VDD, AVDD, PVDD	RESET#	Vref	DCS# [n:0] ^b	DODT [1:0]	DCKE [3:0]	DA/C	PAR_IN	CK CK#	QCS# [n:0] ^c	QODT [1:0]	QCKE [3:0]	QxA/C	ERR OUT#	Y[3:0] Y# [3:0]
0	V _{DD}	H	stable voltage	X	X	X	X	X	running	X	X	X	X	X	running
1	V _{DD}	H	stable voltage	X	X	X	X	X	running	X	X	X	X	X	running
2	V _{DD}	L	stable voltage	X	X	X	X	X	running	Z	Z	L ^d	Z	H ⁴	Z
3	V _{DD}	L	stable voltage	X	X	X	X	X	running	Z	Z	L	Z	H	Z
4	V _{DD}	L	stable voltage	H	X	L	X	X	running	Z	Z	L	Z	H	Z
5	V _{DD}	L	stable voltage	H	X	L	X	X	running	Z	Z	L	Z	H	Z
6	V _{DD}	H	stable voltage	H	X	L	X	X	running	H	L ^e	L	X	H	running
7	V _{DD}	H	stable voltage	H	X	X	X	X	running	After Step 6 (Step 7 and beyond), the device outputs are as defined in the device Function Tables (see Table 12, Table 14 and Table 16).					

a. X = Logic LOW or logic HIGH. Z = floating.

b. n = 3 for JEDEC standard DIMM, n = 7 for non-JEDEC application

c. n = 3 for dual or quad rank DIMMs, n = 7 for octal rank DIMMs.

- d. QxCKE[3:0] and ERROUT# will be driven to these logic states by the register after RESET# is driven LOW and V_{DD} is nominal
 e. This indicates the state of QxODT[1:0] after RESET# switches from LOW-to-HIGH and before the rising CK edge (falling CK# edge)

6.4 Host RCW to Configure MB

After the MB is ready to receive commands and addresses without error, the host needs to configure the MB with register control word writes and/or SMBUS writes (step 4). At reset all RCWs had been reset to their default state (which is '0' except when explicitly noted otherwise). Therefore the host only needs to write those control words whose contents need to be changed.

6.5 Host MRS to Configure DRAM

The host sends MRS commands to the DRAM mode registers to configure proper DRAM operation for all ranks behind the MB. The host can utilize either the MB broadcast mode to send MRS commands to all physical ranks associated with a logical rank or the MB physical rank mode to target MRS commands to specific physical ranks by programming the corresponding mode to the F0RC14 DRAM MRS Control bits.

6.6 Host MRS to DRAM ZQ Calibration

The host sends ZQCL (ZQ Calibration Long) commands to all ranks behind the MB. The MB broadcasts ZQ calibration commands (both ZQCL and ZQCS) to all physical ranks associated with a logical rank. The host may issue ZQ calibration commands sequentially to each logical rank (i.e. wait for tZQinit, tZQoper or tZQCS after each ZQ calibration command before issuing the next one) or it may overlap the ZQ calibration commands to all ranks.

The MB may or may not perform any calibration for its own I/O circuits on receipt of ZQCL or ZQCS calibration commands.

6.7 MB-DRAM Training

After all the DRAMs are fully operational, the host triggers the DRAM interface training by setting the control bit DA4 in F0RC12. Once enabled, the MB assumes autonomous control of the Command/Address, Control and Data/Strobe signals to the DRAMs, without any further assistance from the host.

The MB performs 'Write Leveling' to the DRAMs to ensure successful writes, and 'Read Enable Training' to ensure it can capture read data from the DRAMs correctly, as part of the DRAM interface training.

No DRAM commands or control word writes (either over the Command/Address and Control buses or via SMBus) can be issued to the MB until the MB-DRAM Interface training is complete and the DODTn inputs must be kept low. The MB responds to SMBus CSR read accesses whether or not DRAM interface training is active. To determine DRAM interface training completion the host may either wait for a time 'tCAL * number of physical ranks' (which is the maximum amount of time that the MB-DRAM Interface training is allowed to take) or it may periodically poll the content of the MB CSR 'Training Completion' (see 'Configuration Registers' chapter) over the SMBus.

In addition, training completion can be signaled by the assertion of ERROUT#. This is not the power-up default but can be enabled by setting the DBA1 bit in the F3RC14 Training Completion Control Word.

6.8 Host-MB Training

Now the host can train the MB host interface. The host sets the 'Connector DQ interface write leveling'

PROPOSED

bits in F0RC12 (=0bx001) in order to perform host interface write leveling. Optionally a MB may support RDIMM backward compatible host interface write leveling by intercepting 'Write leveling enable' (MR1 A7) and 'Qoff' (MR1 A12) commands to the DRAMs. The MB asynchronously feeds back CK/CK#, sampled with the rising edge of DQS/DQS#, through the DQ bus (in the same way as a DDR3 DRAM does). Since write leveling requests from the host terminate at the MB, multiple write leveling requests to the MB (i.e. one per rank) will give the same result and are optional. It is sufficient to perform host interface write leveling only once regardless of how many logical or physical ranks are supported by the MB.

MB DRAM interface training must be completed before any MB host interface read training to reflect the correct read round trip delay to and from an LRDIMM. This delay consists of

- (1) Host to MB delay for command
- (2) Command delay through the MB¹
- (3) MB command to DRAM delay
- (4) DRAM latency
- (5) DRAM data/strobe return time to MB
- (6) Data/strobe delay through the MB
- (7) MB to host delay for data/strobe

MB DRAM interface training must be completed before any MB host interface read or write training to ensure that the MB DRAM interface is configured optimally for DRAM reads and writes. The host performs normal writes to DRAM for write DQ/DQS margining, with failure occurring through incorrect strobing of write data through the MB. The host performs read DQ/DQS margining by using normal reads from DRAM or by using the DRAM multi purpose register (MPR) with failure occurring through invalid DQ/DQS alignment at the host I/O pins. No special support by the MB is required for host interface read training.

¹.Note that the data/strobe delay through the MB during writes can be different than the command delay through the MB.

Exhibit B



Committee Letter Ballot
JC-40.4-09-320
Item 142.35
Distributed: 11 Nov 2009
Expiring: 03 Dec 2009



SPONSOR: Super Micro Computer Inc., represented by John Smolka, johns@supermicro.com,
(408) 390-8302 N/A

DISTRIBUTION: Formal Vote: JC-404
Non voting committees: JC-40 (Information and Comments)

Eng. No.: AS 90577

Item No.: 142.35

SUBJECT: [LRDIMM DDR3 Memory Initialization Chapter Proposal](#)

BACKGROUND: At September 09 JEDEC meeting in San Jose, motion by Intel and seconded by Montage to authorize the TG to issue one or more ballots on the items listed on pages 3 and 4 of the presentation that have item numbers, have been shown in the committee and for which the TG has reached a consensus.

The motion passed by acclamation.

This ballot proposal is to specify LRDIMM DDR3 Memory Initialization, and has been approved by DDR3 MB TG on 11/09/2009.

PATENTS: No known patent issues on the sponsor's part

ATTACHMENT: [Download NB09320-.pdf](#)

KEYWORDS: DDR3, MB, Memory Buffer, LRDIMM, Initialization

[\[Top\]](#)



Exhibit C

December 04 2009 at 09:31:09



JEDEC
Compilation of Tallies
for JC-40 CMOS Digital Logic and
point committees



The following compilation was generated on 12-04-09, one day after expiration date of the ballot(s). These tallies are not deemed final.

Please attend the meeting or read the minutes of the relevant meeting to learn the final decision on any ballot.

Tallies can change in many significant ways, including, but not restricted to, the following common situations:

- votes can be added by the sponsor upon voters' request (even after the ballot is closed);
- voters can send postcards thereby adding comments;
- voters can send postcards and change a "No" vote to a "Yes";
- sponsors may further address comments;
- etc.

The list of ballots contains not only those ballots that the committee voted but also those that were distributed on a "For information and Comments" or "Information only" basis.

Committee Letter Ballot JC-40.3-09-282 Item 104.75

Subject: DDR3 Register (SSTE32882) -- DDR3 1866 Specification

PATENTS: No known patent issues on the sponsor's part

[Clik here for NB09282-.pdf](#)

Ballot distributed: 09 Nov 2009, Expired: 03 Dec 2009

Sponsor: Mr. Ramzi Ammar **Silego Technology** [e-mail \(rammar@silego.com\)](mailto:rammar@silego.com)

NON FINAL REPORT/ Attend meeting or read minutes for final results.								
Company / voter	Y*	N*	A*	P*	C*	PC*	DoV*	DoR*
20 companies voted	15	0	5	0	0			
Advanced Micro Devices Inc. Patel	Y						12/02/09	
Cray Inc. Grossmeier			A				11/16/09	
Dell Inc. Berke	Y						12/01/09	
Elpida Memory Incorporated Ono	Y						11/26/09	
Hynix Semiconductor Kim			A				12/02/09	
IBM Corporation Stout	Y						11/20/09	
Inphi Corporation Washkewicz	Y						12/02/09	
Integrated Device Technology Inc. Franklin	Y						12/03/09	
Intel Corporation Tsang	Y						12/03/09	
Kingston Technology Company Inc. Cheng			A				11/23/09	
Legacy Electronics Inc. Mecker	Y						12/01/09	
Micron Technology Inc. Graham	Y						11/30/09	
Netlist Inc. Martinez	Y						12/01/09	
Numonyx B.V. Abdulla			A				11/30/09	
Nvidia Corporation Wagner			A				12/01/09	
NXP Semiconductors Roozeboom	Y						12/01/09	
Samsung Semiconductor Park	Y						12/02/09	
Silego Technology Chung	Y						12/03/09	
Smart Modular Technologies, Inc. Marino	Y						12/02/09	
Texas Instruments Inc. Frank	Y						12/03/09	
* Y = Yes, N = No, A = Abstain, P = Patent(s), C = Comments PC: Postcard, Y = approved response, N = did not approve response, N/A: not available, sponsor and / or voter did not respond, DoV: Date of Vote								

JEDEC compilation of tallies (non final) expiring on December 03 2009. The minutes of the relevant meeting(s) will contain the final decision on any ballot.

Committee Letter Ballot JC-40.4-09-255 Item 142.12

Subject: Transparent Mode Functionality

PATENTS: No known patent issues on the sponsor's part

[Clik here for NB09255-.pdf](#)

Ballot distributed: 22 Oct 2009, Expired: 03 Dec 2009

Sponsor: Mr. Christian Harrieder Texas Instruments Inc. [e-mail \(christian.harrieder@ti.com\)](mailto:christian.harrieder@ti.com)

NON FINAL REPORT/ Attend meeting or read minutes for final results.								
Company / voter	Y*	N*	A*	P*	C*	PC*	DoV*	DoR*
19 companies voted	11	0	8	1	1_Y			
Advanced Micro Devices Inc. Patel			A				12/03/09	
Agilent Technologies Keller			A				10/27/09	
Cray Inc. Grossmeier	Y						10/27/09	
Elpida Memory Incorporated Ono	Y						11/26/09	
Hynix Semiconductor Kim	Y						12/02/09	
IBM Corporation Stout			A				11/20/09	
Inphi Corporation Washkewicz	Y						12/02/09	
Integrated Device Technology Inc. Franklin	Y						12/02/09	
Intel Corporation Tsang	Y						12/03/09	
Kingston Technology Company Inc. Cheng			A				10/27/09	
Legacy Electronics Inc. Mecker			A				12/01/09	
Micron Technology Inc. Graham	Y				X	N/A	11/30/09	
Netlist Inc. Martinez			A	P			12/01/09	
Nvidia Corporation Wagner			A				12/01/09	
NXP Semiconductors Roozeboom	Y						12/01/09	
Samsung Semiconductor Park	Y						12/02/09	
Silego Technology Chung	Y						12/03/09	
Smart Modular Technologies, Inc. Marino			A				11/30/09	
Texas Instruments Inc. Harrieder	Y						10/26/09	
* Y = Yes, N = No, A = Abstain, P = Patent(s), C = Comments PC: Postcard, Y = approved response, N = did not approve response, N/A: not available, sponsor and / or voter did not respond, DoV: Date of Vote								

Comments from **Micron Technology Inc.**

No where in the ballot is it identified that this pertains to the Memory Buffer except the keywords.

Postcard Response (for above discussion) / if any present:"

PATENT ISSUE:

Netlist may have IP that applies to this ballot.

Committee Letter Ballot JC-40.4-09-297 Item 142.51

Subject: Transparent Mode CA timing

PATENTS: No known patent issues on the sponsor's part

[Clik here for NB09297-.pdf](#)

Ballot distributed: 10 Nov 2009, Expired: 03 Dec 2009

Sponsor: Mr. Christian Harrieder Texas Instruments Inc. [e-mail \(christian.harrieder@ti.com\)](mailto:christian.harrieder@ti.com)

NON FINAL REPORT/ Attend meeting or read minutes for final results.								
Company / voter	Y*	N*	A*	P*	C*	PC*	DoV*	DoR*
20 companies voted	14	0	6	1	0			
Advanced Micro Devices Inc. Patel			A				12/03/09	
Cray Inc. Grossmeier			A				11/16/09	
Elpida Memory Incorporated Ono	Y						11/26/09	
FormFactor Inc. Gervasi	Y						12/02/09	
Hynix Semiconductor Kim	Y						12/02/09	
IBM Corporation Stout			A				11/20/09	
Inphi Corporation Washkewicz	Y						12/02/09	
Integrated Device Technology Inc. Franklin	Y						12/02/09	
Intel Corporation Tsang	Y						12/03/09	
Kingston Technology Company Inc. Cheng	Y						11/23/09	
Legacy Electronics Inc. Mecker			A				12/01/09	
Micron Technology Inc. Graham	Y						11/30/09	
Netlist Inc. Martinez			A	P			12/01/09	
Nvidia Corporation Wagner			A				12/01/09	
NXP Semiconductors Roozeboom	Y						12/01/09	
Samsung Semiconductor Park	Y						12/02/09	
Silego Technology Chung	Y						12/03/09	
Smart Modular Technologies, Inc. Marino	Y						12/02/09	
Sun Microsystems Inc. Lee	Y						11/13/09	
Texas Instruments Inc. Harrieder	Y						11/19/09	
* Y = Yes, N = No, A = Abstain, P = Patent(s), C = Comments PC: Postcard, Y = approved response, N = did not approve response, N/A: not available, sponsor and / or voter did not respond, DoV: Date of Vote								

PATENT ISSUE:

Netlist may have IP that applies towards this ballot

Committee Letter Ballot JC-40.4-09-299 Item 142.54

Subject: LR-DIMM DDR3 Memory Buffer Pin Description Proposal

PATENTS: No known patent issues on the sponsor's part

[Clik here for NB09299-.pdf](#)

Ballot distributed: 10 Nov 2009, Expired: 03 Dec 2009

Sponsor: Mr. John Smolka **Silego Technology** [e-mail \(jsmolka@silego.com\)](mailto:jsmolka@silego.com)

NON FINAL REPORT/ Attend meeting or read minutes for final results.								
Company / voter	Y*	N*	A*	P*	C*	PC*	DoV*	DoR*
21 companies voted	18	0	3	1	5Y			
Advanced Micro Devices Inc. Patel	Y				X	N/A	12/03/09	
Cray Inc. Grossmeier	Y						11/16/09	
Dell Inc. Berke	Y						12/01/09	
Elpida Memory Incorporated Ono	Y				X	N/A	11/26/09	
FormFactor Inc. Gervasi	Y				X	N/A	12/02/09	
Hynix Semiconductor Kim	Y						12/02/09	
IBM Corporation Stout	Y						11/20/09	
Inphi Corporation Washkewicz	Y				X	N/A	12/02/09	
Integrated Device Technology Inc. Franklin	Y				X	N/A	12/02/09	
Intel Corporation Tsang	Y						12/03/09	
Kingston Technology Company Inc. Cheng	Y						11/23/09	
Legacy Electronics Inc. Mecker			A				12/01/09	
Micron Technology Inc. Graham	Y						11/30/09	
Netlist Inc. Martinez			A	P			12/01/09	
Nvidia Corporation Wagner			A				12/01/09	
NXP Semiconductors Roozeboom	Y						12/01/09	
Samsung Semiconductor Park	Y						12/02/09	
Silego Technology Chung	Y						12/03/09	
Smart Modular Technologies, Inc. Marino	Y						11/30/09	
Sun Microsystems Inc. Lee	Y						11/13/09	
Texas Instruments Inc. Harrieder	Y						11/30/09	
* Y = Yes, N = No, A = Abstain, P = Patent(s), C = Comments PC: Postcard, Y = approved response, N = did not approve response, N/A: not available, sponsor and / or voter did not respond, DoV: Date of								

Comments from **Advanced Micro Devices Inc.**

TG has unanimously agreed to remove QAECC[9,6,2] pins from the buffer and hence should be removed from this ballot. Postcard Response (for above discussion) / if any present:"

Comments from **Elpida Memory Incorporated**

How should the QAECC2,6,9 be treated ? Changing to NC or RFU ? Postcard Response (for above discussion) / if any present:"

Comments from **FormFactor Inc.**

ERROUT_n should include statement about being an open drain output and that a pull-up is required on the main board. Postcard Response (for above discussion) / if any present:"

Comments from **Inphi Corporation**

Inphi approves material in red text. Postcard Response (for above discussion) / if any present:"

Comments from **Integrated Device Technology Inc.**

QAECC 9, 6, and 2 are shown in this Ballot but in MB TG discussion they should all be renamed RFU as there was no usage model for them. Postcard Response (for above discussion) / if any present:"

PATENT ISSUE:

Netlist may have IP that may apply towards this ballot

Committee Letter Ballot JC-40.4-09-300 Item 142.53

Subject: LR-DIMM DDR3 Memory Buffer Ballout Proposal

PATENTS: No known patent issues on the sponsor's part

[Clik here for NB09300-.pdf](#)

Ballot distributed: 10 Nov 2009, Expired: 03 Dec 2009

Sponsor: Mr. John Smolka **Silego Technology** [e-mail \(jsmolka@silego.com\)](mailto:jsmolka@silego.com)

NON FINAL REPORT/ Attend meeting or read minutes for final results.								
Company / voter	Y*	N*	A*	P*	C*	PC*	DoV*	DoR*
20 companies voted	14	0	6	1	2Y			
Advanced Micro Devices Inc. Patel	Y						12/02/09	
Cray Inc. Grossmeier	Y						11/16/09	
Dell Inc. Berke			A				12/01/09	
Elpida Memory Incorporated Ono	Y				X	N/A	11/26/09	
Hynix Semiconductor Kim	Y						12/02/09	
IBM Corporation Stout	Y						11/20/09	
Inphi Corporation Washkewicz	Y						12/02/09	
Integrated Device Technology Inc. Franklin	Y				X	N/A	12/02/09	
Intel Corporation Tsang	Y						12/03/09	
Kingston Technology Company Inc. Cheng			A				11/23/09	
Legacy Electronics Inc. Mecker			A				12/01/09	
Micron Technology Inc. Graham	Y						11/30/09	
Netlist Inc. Martinez			A	P			12/01/09	
Nvidia Corporation Wagner			A				12/01/09	
NXP Semiconductors Roozeboom	Y						12/01/09	
Samsung Semiconductor Park	Y						12/02/09	
Silego Technology Chung	Y						12/03/09	
Smart Modular Technologies, Inc. Marino			A				11/30/09	
Sun Microsystems Inc. Lee	Y						11/13/09	
Texas Instruments Inc. Harrieder	Y						11/30/09	
* Y = Yes, N = No, A = Abstain, P = Patent(s), C = Comments PC: Postcard, Y = approved response, N = did not approve response, N/A: not available, sponsor and / or voter did not respond, DoV: Date of Vote								

Comments from Elpida Memory Incorporated

How should the QAECC2,6,9 be treated ? Changing to NC or RFU ? Postcard Response (for above discussion) / if any present:"

Comments from Integrated Device Technology Inc.

QAECC 9, 6, and 2 are shown in this Ballot but in MB TG discussions they should all be renamed RFU as there was no usage model for them Postcard Response (for above discussion) / if any present:"

PATENT ISSUE:

Netlist may have IP that may apply towards this ballot.

Committee Letter Ballot JC-40.4-09-316 Item 142.46

Subject: LRDIMM DDR3 Memory Buffer Host Interface Protocol and Requirements

PATENTS: No known patent issues on the sponsor's part

[Clik here for NB09316-.pdf](#)

Ballot distributed: 11 Nov 2009, Expired: 03 Dec 2009

Sponsor: Mr. John Smolka **Silego Technology** [e-mail \(jsmolka@silego.com\)](mailto:jsmolka@silego.com)

NON FINAL REPORT/ Attend meeting or read minutes for final results.								
Company / voter	Y*	N*	A*	P*	C*	PC*	DoV*	DoR*
20 companies voted	15	0	5	1	3Y			
Advanced Micro Devices Inc. Patel	Y				X	N/A	12/03/09	
Cray Inc. Grossmeier	Y						11/16/09	
Dell Inc. Berke	Y						12/01/09	
Elpida Memory Incorporated Ono	Y						11/26/09	
Hynix Semiconductor Kim	Y						12/02/09	
IBM Corporation Stout	Y						11/20/09	
Inphi Corporation Washkewicz	Y				X	N/A	12/02/09	
Integrated Device Technology Inc. Franklin	Y						12/02/09	
Intel Corporation Tsang	Y						12/03/09	
Kingston Technology Company Inc. Cheng			A				11/23/09	
Legacy Electronics Inc. Mecker			A				12/01/09	
Micron Technology Inc. Graham	Y						11/30/09	
Netlist Inc. Martinez			A	P			12/01/09	
Nvidia Corporation Wagner			A				12/01/09	
NXP Semiconductors Roozeboom	Y						12/01/09	
Samsung Semiconductor Park	Y						12/02/09	
Silego Technology Chung	Y						12/03/09	
Smart Modular Technologies, Inc. Marino			A				12/01/09	
Sun Microsystems Inc. Lee	Y						11/13/09	
Texas Instruments Inc. Harrieder	Y				X	N/A	11/30/09	
* Y = Yes, N = No, A = Abstain, P = Patent(s), C = Comments PC: Postcard, Y = approved response, N = did not approve response, N/A: not available, sponsor and / or voter did not respond, DoV: Date of Vote								

Comments from **Advanced Micro Devices Inc.**

section 4.2.2.3.6.4 should be part of the ballot.

Add a statement which indicates it is not allowed by the buffer to put half the ranks in self refresh mode while other half the ranks on a dimm in power down mode to help reduce the test/validation combinations. Postcard Response (for above discussion) / if any present:"

Comments from **Inphi Corporation**

Inphi approves material in red text Postcard Response (for above discussion) / if any present:"

PATENT ISSUE:

Netlist may have IP that may apply to this ballot

Comments from **Texas Instruments Inc.**

page 7; Table 6, Section "2 Way Rank Multiplication using A[15]", Subsection "Nr. DCS=4", First Row, Column A16/DCS[2]_n:
is 'x' should be '1'

page 15; Table 10, row NOP

"Command is not passed to the DRAM bus." contradicts chapter 4.2.2.3.9 "The MB will pass a NOP onto the DRAM bus, broadcasting to all sub-ranks." Postcard Response (for above discussion) / if any present:"

Committee Letter Ballot JC-40.4-09-317 Item 142.47

Subject: LRDIMM DDR3 Memory Buffer DRAM Interface Protocol and Requirements

PATENTS: No known patent issues on the sponsor's part

[Clik here for NB09317-.pdf](#)

Ballot distributed: 11 Nov 2009, Expired: 03 Dec 2009

Sponsor: Mr. John Smolka **Silego Technology** [e-mail \(jsmolka@silego.com\)](mailto:jsmolka@silego.com)

NON FINAL REPORT/ Attend meeting or read minutes for final results.								
Company / voter	Y*	N*	A*	P*	C*	PC*	DoV*	DoR*
21 companies voted	16	0	5	1	4Y			
Advanced Micro Devices Inc. Patel	Y				X	N/A	12/03/09	
Cray Inc. Grossmeier	Y						11/16/09	
Dell Inc. Berke	Y						12/01/09	
Elpida Memory Incorporated Ono	Y				X	N/A	11/26/09	
Hynix Semiconductor Kim	Y						12/02/09	
IBM Corporation Stout	Y						11/20/09	
Inphi Corporation Washkewicz	Y						12/02/09	
Inphi Corporation Raghavan	Y						12/02/09	
Integrated Device Technology Inc. Franklin	Y				X	N/A	12/02/09	
Intel Corporation Tsang	Y				X	N/A	12/03/09	
Kingston Technology Company Inc. Cheng			A				11/23/09	
Legacy Electronics Inc. Mecker			A				12/01/09	
Micron Technology Inc. Graham	Y						11/30/09	
Netlist Inc. Martinez			A	P			12/01/09	
Nvidia Corporation Wagner			A				12/01/09	
NXP Semiconductors Roozeboom	Y						12/01/09	
Samsung Semiconductor Park	Y						12/02/09	
Silego Technology Chung	Y						12/03/09	
Smart Modular Technologies, Inc. Marino			A				12/02/09	
Sun Microsystems Inc. Lee	Y						11/13/09	
Texas Instruments Inc. Harrieder	Y						11/30/09	
* Y = Yes, N = No, A = Abstain, P = Patent(s), C = Comments PC: Postcard, Y = approved response, N = did not approve response, N/A: not available, sponsor and / or voter did not respond, DoV: Date of								

Comments from **Advanced Micro Devices Inc.**

TG has unanimously agreed to remove all references related to QAECC[2,6,9] from the buffer spec. This ballot should editorially update it accordingly. Postcard Response (for above discussion) / if any present:"

Comments from **Elpida Memory Incorporated**

How should the QAECC 2,6,9 part be treated ?

Removing the QAECC 2,6,9 part? Postcard Response (for above discussion) / if any present:"

Comments from **Integrated Device Technology Inc.**

QAECC 9, 6, and 2 are shown in this Ballot but in MB TG discussion they should all be renamed RFU as there was no useage model for them Postcard Response (for above discussion) / if any present:"

Comments from **Intel Corporation**

Editorial changes: Table 2: QAECC should be deleted. The ECC DRAM columns should also be deleted. Page 12, 4.2.2.3.4.3 The Targeted Refresh mode is used the Refresh Control bit .. should be The Targeted Refresh mode is used if the Refresh Control bit ..
Page 14, 4.2.2.3.8 When Broadcast to All Sub-ranks is spiced, & should probably be When Broadcast to All Sub-ranks is specified, & Postcard Response (for above discussion) / if any present:"

PATENT ISSUE:

Netlist may have IP that applies towards this ballot

Committee Letter Ballot JC-40.4-09-318 Item 142.11c

Subject: DDR3 MB Control Word Definition

PATENTS: No known patent issues on the sponsor's part

[Clik here for NB09318-.pdf](#)

Ballot distributed: 11 Nov 2009, Expired: 03 Dec 2009

Sponsor: Mr. John Smolka **Silego Technology** [e-mail \(jsmolka@silego.com\)](mailto:jsmolka@silego.com)

Parent ballot: JC-40.4-09-216

NON FINAL REPORT/ Attend meeting or read minutes for final results.								
Company / voter	Y*	N*	A*	P*	C*	PC*	DoV*	DoR*
21 companies voted	14	0	7	1	5Y 1A			
Advanced Micro Devices Inc. Patel	Y				X	N/A	12/03/09	
Cray Inc. Grossmeier			A				11/16/09	
Dell Inc. Berke	Y						12/01/09	
Elpida Memory Incorporated Ono	Y				X	N/A	11/26/09	
FormFactor Inc. Gervasi					X	N/A	12/02/09	
Hynix Semiconductor Kim	Y						12/02/09	
IBM Corporation Stout	Y						11/20/09	
Inphi Corporation Washkewicz	Y				X	N/A	12/02/09	
Integrated Device Technology Inc. Franklin	Y						12/02/09	
Intel Corporation Tsang	Y				X	N/A	12/03/09	
Kingston Technology Company Inc. Cheng			A				11/23/09	
Legacy Electronics Inc. Mecker			A				12/01/09	
Micron Technology Inc. Graham	Y						11/30/09	
Netlist Inc. Martinez			A	P			12/01/09	
Nvidia Corporation Wagner			A				12/01/09	
NXP Semiconductors Roozeboom	Y						12/01/09	
Samsung Semiconductor Park	Y						12/02/09	
Silego Technology Chung	Y						12/03/09	
Smart Modular Technologies, Inc. Marino			A				12/01/09	
Sun Microsystems Inc. Lee	Y						11/13/09	
Texas Instruments Inc. Harrieder	Y				X	N/A	11/30/09	
* Y = Yes, N = No, A = Abstain, P = Patent(s), C = Comments								

PC: Postcard, Y = approved response, N = did not approve response, N/A: not available, sponsor and / or voter did not respond, DoV: Date of Vote

Comments from Advanced Micro Devices Inc.

-- Table 25 should have reverse the mapping as following: 00 - default - 8 rank; 01 - 4 rank; 10 - 2 rank; 11 - 1 rank
-- Footnote 2 for table 18 should be included part of the ballot
-- There are several other editorial changes that has been suggested. Will show the updated draft. Postcard Response (for above discussion) / if any present:"

Comments from Elpida Memory Incorporated

1) Definition of table 40: "Total QODT delay = Y Delay (F[1]RC14)+QODDextended (" should be changed to "Total QODT delay = QODT delay (F[1]RC14) + QODT Dextended"
2) Encoding of table 40: "to Delay Y " should be changed to " to QODT delay " 3) Bottom two row of Table 68, Definition: "Reserved" should be changed to "Vref for MDQ to MB" , and corresponding "Encoding" should be changed from "Reserved to "TBD" Postcard Response (for above discussion) / if any present:"

Comments from FormFactor Inc.

DCS[n:0]# should be DCS[n:0]_n

Postcard Response (for above discussion) / if any present:"

Comments from Inphi Corporation

--Footnote 2 for Table 18 should be included as part of the ballot.

--Table 25 F0RC13 - mapping should be updated as following for bits DA4, DA3.

00b - Default - 8 Ranks; QCS[7:0]_n

01b - 4 Ranks; QCS[3:0]_n

10b - 2 Ranks; QCS[1:0]_n

11b - 1 rank; QCS[0]_n

--Table 27. Footnote for Self Refresh Entry and Self Refresh exit should be included as part of the ballot. Postcard Response (for above discussion) / if any present:"

Comments from Intel Corporation

As DDR3U is not part of JEDEC standard currently, DDR3U reference should be removed from the following tables:

Table 22 F[0]RC10: Encoding for LRDIMM Operating Speed

Table 23 F[0]RC11: Operating Voltage & Parity Calculation Control Word Postcard Response (for above discussion) / if any present:"

PATENT ISSUE:

Netlist may have IP that apply towards this ballot.

Comments from Texas Instruments Inc.

page 8 table 13: DA3 encoding needs update from F1RC12 to F1RC8, F1RC11-F1RC15 |

page 12 table 20: Footnote 2 this text belongs to footnote 1 |

page 19 Table 30: Section "2 Way Rank Multiplication using A[15]", Subsection "Nr. DCS=4", First Row, Column A16/DCS[2]_n:

Typo: This should be 1 and not x |

page 27 Table 40: Definition: QOD-Dextended -> QODT-Dextended
Postcard Response (for above discussion) / if any present:"

Committee Letter Ballot JC-40.4-09-319 Item 142.09

Subject: LRDIMM DDR3 Memory Power Management Chapter Proposal

PATENTS: No known patent issues on the sponsor's part

[Clik here for NB09319-.pdf](#)

Ballot distributed: 11 Nov 2009, Expired: 03 Dec 2009

Sponsor: Mr. John Smolka **Silego Technology** [e-mail \(jsmolka@silego.com\)](mailto:jsmolka@silego.com)

NON FINAL REPORT/ Attend meeting or read minutes for final results.								
Company / voter	Y*	N*	A*	P*	C*	PC*	DoV*	DoR*
21 companies voted	15	0	6	1	3Y			
Advanced Micro Devices Inc. Patel	Y				X	N/A	12/03/09	
Cray Inc. Grossmeier	Y						11/16/09	
Dell Inc. Berke	Y						12/01/09	
Elpida Memory Incorporated Ono	Y						11/26/09	
Hewlett Packard Company Gharaibeh	Y						11/17/09	
Hynix Semiconductor Kim	Y						12/02/09	
IBM Corporation Stout			A				11/20/09	
Inphi Corporation Washkewicz	Y				X	N/A	12/02/09	
Integrated Device Technology Inc. Franklin	Y						12/02/09	
Intel Corporation Tsang	Y				X	N/A	12/03/09	
Kingston Technology Company Inc. Cheng			A				11/23/09	
Legacy Electronics Inc. Mecker			A				12/01/09	
Micron Technology Inc. Graham	Y						11/30/09	
Netlist Inc. Martinez			A	P			12/01/09	
Nvidia Corporation Wagner			A				12/01/09	
NXP Semiconductors Roozeboom	Y						12/01/09	
Samsung Semiconductor Park	Y						12/02/09	
Silego Technology Chung	Y						12/03/09	
Smart Modular Technologies, Inc. Marino			A				12/01/09	
Sun Microsystems Inc. Lee	Y						11/13/09	
Texas Instruments Inc. Harrieder	Y						11/30/09	
* Y = Yes, N = No, A = Abstain, P = Patent(s), C = Comments PC: Postcard, Y = approved response, N = did not approve response, N/A: not available, sponsor and / or voter did not respond, DoV: Date of								

Comments from **Advanced Micro Devices Inc.**

-- Section 8.1.3 - A note should be added which indicates it is not allowed to put half the ranks of a dimm in self refresh while other remaining half ranks in power down mode to simplify buffer test and verification combination. Postcard Response (for above discussion) / if any present:"

Comments from **Inphi Corporation**

--Section 8.1.3 - A note should be added to indicate that it is not allowed to put half the ranks of LRDIMM in self refresh mode while remaining half ranks of LRDIMM in power down mode.
Postcard Response (for above discussion) / if any present:"

Comments from **Intel Corporation**

Attached is the editorial change (ure: sing correct convention for # signals) that TG agreed
Postcard Response (for above discussion) / if any present:"

PATENT ISSUE:

Netlist may have IP that applies towards this ballot

Committee Letter Ballot JC-40.4-09-320 Item 142.35

Subject: LRDIMM DDR3 Memory Initialization Chapter Proposal

PATENTS: No known patent issues on the sponsor's part

[Clik here for NB09320-.pdf](#)

Ballot distributed: 11 Nov 2009, Expired: 03 Dec 2009

Sponsor: Mr. John Smolka **Silego Technology** [e-mail \(jsmolka@silego.com\)](mailto:jsmolka@silego.com)

NON FINAL REPORT/ Attend meeting or read minutes for final results.								
Company / voter	Y*	N*	A*	P*	C*	PC*	DoV*	DoR*
20 companies voted	15	0	5	1	1Y			
Advanced Micro Devices Inc. Patel	Y						12/03/09	
Cray Inc. Grossmeier	Y						11/16/09	
Dell Inc. Berke	Y						12/01/09	
Elpida Memory Incorporated Ono	Y						11/26/09	
Hynix Semiconductor Kim	Y						12/02/09	
IBM Corporation Stout			A				11/20/09	
Inphi Corporation Washkewicz	Y						12/02/09	
Integrated Device Technology Inc. Franklin	Y						12/02/09	
Intel Corporation Tsang	Y				X	N/A	12/03/09	
Kingston Technology Company Inc. Cheng	Y						11/23/09	
Legacy Electronics Inc. Mecker			A				12/01/09	
Micron Technology Inc. Graham	Y						11/30/09	
Netlist Inc. Martinez			A	P			12/01/09	
Nvidia Corporation Wagner			A				12/01/09	
NXP Semiconductors Roozeboom	Y						12/01/09	
Samsung Semiconductor Park	Y						12/02/09	
Silego Technology Chung	Y						12/03/09	
Smart Modular Technologies, Inc. Marino			A				12/02/09	
Sun Microsystems Inc. Lee	Y						11/13/09	
Texas Instruments Inc. Harrieder	Y						11/30/09	
* Y = Yes, N = No, A = Abstain, P = Patent(s), C = Comments PC: Postcard, Y = approved response, N = did not approve response, N/A: not available, sponsor and / or voter did not respond, DoV: Date of Vote								

Comments from **Intel Corporation**

Attached is the editorial change (re: using correct convention for # signals) that TG agreed Postcard Response (for above discussion) / if any present."

PATENT ISSUE:

Netlist may have IP which may apply to this ballot

End of Compilation of Tallies (PDF Format)



December 04 2009 at 09:31:22

Exhibit D



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COMMITTEE LETTER BALLOT

Committee: 45.4

Committee Item Number: 2192.44

Subject: DDR3 LRDIMM Design Specification Body

Background: At the September 2009 Committee meeting the DDR3 LRDIMM TG was given authorization for 1 or more ballots on the LRDIMM Design Specification body and Appendices.

The following LRDIMM Design Specification has Change bars and Highlighted text however the **entire specification is being balloted**. The change bars and Highlighted areas are difference from the RDIMM specification.

Keywords: LRDIMM, DIMM, DDR3, MB, Memory Buffer, DRAM, SDRAM, Design, Specification

PC3 Load Reduced DIMM (LRDIMM)

Design Specification

Revision 0.16

November 4, 2009

The following draft contains general sections for DDR3 LRDIMMs.

Proposed

Contents

1. Product Description.....	4
Product Family Attributes.....	4
2. Environmental Requirements.....	5
3. Pinout and Description.....	6
Pin Description.....	6
Input/Output Functional Description.....	7
DDR3 240-pin DIMM Pinout.....	9
Pinout Comparison.....	10
4. Component Details.....	11
Pin Assignments for 512Mb to 8Gb; DDR3 SDRAM.....	12
PACB Pad Array Options for SDRAM Placements.....	16
Pin Assignments for Registering Clock Driver.....	22
Critical Registering Clock Driver Specifications (Reference Only).....	23
Pin Assignments for Serial Presence Detect.....	25
5. DDR3 Registered DIMM Wiring Details.....	26
Signal Groups.....	26
General Net Structure Routing Guidelines.....	26
Test Point.....	28
Explanation of Net Structure Diagrams.....	29
6. Timing Budget.....	30
Example of DDR3 Timing Budget.....	31
7. On Dimm Thermal Sensor.....	32
8. Serial Presence Detect Definition.....	33
9. DDR3 DIMM Label Format.....	36
10. DIMM Mechanical Specifications.....	38
11. Design File Naming Convention.....	39
11. Revision Log.....	40
12. Appendix A.....	Appendix A
13. Raw Card B.....	Appendix B
14. Raw Card C.....	Appendix C

Proposed

15. Raw Card D.....	Appendix D
16. Raw Card E.....	Appendix E
17. Raw Card F.....	Appendix F
18. Raw Card G.....	Appendix G
20. Raw Card J	Appendix J
21. Raw Card K	Appendix K

Proposed

Product Description

This specification defines the electrical and mechanical requirements for 240-pin, 72 bit-wide, Load Reduced Double Data Rate Synchronous DRAM Dual In-Line Memory Modules (DDR3 SDRAM DIMMs). These SDRAM DIMMs are intended for use as main memory when installed in systems such as servers and workstations.

PC3-6400/PC3-8500/PC3-10600/PC3-12800/PC3-14900/PC3-17000 refers to the JEDEC standard DIMM naming convention in which PC3-6400/PC3-8500/PC3-10600/PC3-12800/PC3-14900/PC3-17000 indicates a 240-pin DIMM running at 400/533/666/800/933/1066 MHz clock speed and offering 6400/8500/10600/12800/14900/17000 MB/s bandwidth.

Reference design examples are included which provide an initial basis for Load Reduced DIMM designs. Modifications to these reference designs may be required to meet all system timing, signal integrity, and thermal requirements. All load reduced DIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

The LRDIMM differs from RDIMMs in that the SDRAMs do not connect directly to the edge connector with the exception of VDD and VSS (ground). The Memory Buffer (MB) buffers both address and data. Increased performance is achieved based on the LRDIMM presenting only one load to the system. Increased capacity is achieved since the MB drives only the SDRAMs on the module and therefore a well defined topology and load. The maximum number of SDRAM die is 144. The LRDIMM is intended to function in all RDIMM platforms with appropriate BIOS changes. Systems designed to function with LRDIMMs will be better able to take advantage of LRDIMM features.

While four chip selects are possible at the edge connector the MB provides a "address multiplication" feature. The MB uses one or two of the address lines not directly useable by the SDRAM to generate additional chip selects to the SDRAM. This feature is completely configurable in the MB. There are 2 additional address lines (A16 and A17) defined that will typically only be used with the address multiplication feature. With address multiplication refresh and mode register access become more difficult. This is because the system sees the LRDIMM as fewer logical ranks than the true physical ranks. Rank based commands like refresh and mode register access must accommodate this in some fashion. The MB provides several methods. See the MB Design Specification for more information on the MB features and programming.

The LRDIMM has the option of using ODT0 only or both ODT0 and ODT1.

The VREF_DQ and VREF_CA pins on the edge connector provide the reference for the MB. The MB has additional VREF generators that may be used for the SDRAM reference and as the reference for the MB interfaces.

LRDIMMs can use an address mirroring feature. This is exactly as defined in the UDIMM Design Specification with the exception that all odd ranks are mirrored when this feature is used. There is an SPD bit that provides the information to the system on whether the specific LRDIMM requires the use of address mirroring. Since the wiring on the LRDIMM is different to support this feature it must be used when the LRDIMM is wired to use address mirroring. As defined the controller must have the capability to do address mirroring.

The LRDIMMs are defined to require an integrated thermal sensor with the SPD. Additionally the MB is defined to have an internal thermal sensor.

Proposed

Product Family Attributes

DIMM organization	x72 ECC
DIMM dimensions : height (nom.) x width(nom.) x thickness(max.) / MO-number, Variation	30.35 mm x 133.35 mm x 4.00 mm / MO-269, Variation TBD 30.35 mm x 133.35 mm x 6.75 mm / MO-269, Variation TBD 30.35 mm x 133.35 mm x 7.55 mm / MO-269, Variation TBD 18.75 mm x 133.35 mm x 4.00 mm / MO-269. Variation DB 18.75 mm x 133.35 mm x 4.00 mm / MO-269. Variation EB 18.75 mm x 133.35 mm x 4.00 mm / MO-269. Variation FB
Pin count	240
SDRAMs supported	1 Gb, 2 Gb, 4 Gb
Capacity	4 GB, 8 GB, 16 GB, 32 GB, 64 GB
Serial PD	Consistent with JC 45
Voltage options	1.35 and 1.5 volt (V_{DD}), 3.3 volt (V_{DDSPD})
Interface	1.35 and 1.5 volt signal switching based on reference voltage at $V_{DD}/2$. See DRAM specification for more detail.

Environmental Parameters

DDR3 SDRAM Registered DIMMs are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating temperature	See Note		3
H_{OPR}	Operating humidity (relative)	10 to 90	%	1
T_{STG}	Storage temperature	-50 to +100	°C	1
H_{STG}	Storage humidity (without condensation)	5 to 95	%	1
P_{BAR}	Barometric pressure (operating & storage)	105 to 69	K Pascal	1, 2
1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. 2. Up to 9850 ft. 3. The designer must meet the case temperature specifications for individual module components.				

Proposed

Pinout and Description

Pin Description

Pin Name	Description	Number	Pin Name	Description	Number
CK0_t	Clock Input, positive line	1	Par_In	Parity bit for the Address and Control bus	1
CK0_c	Clock Input, negative line	1	ErrOut_n	Parity error found on the Address and Control bus	1
CK1_t	Clock Input, positive line	1	ODT[0]	On Die Termination Input	1
CK1_c	Clock Input, negative line	1	DQ[63:0]	Data Input/Output	64
CKE[1:0]	Clock Enables	2	CB[7:0]	Data check bits Input/Output	8
CKE[3:2], ODT[1], TEST	Clock Enables On Die Termination Memory bus tool (Not Connected and Not Useable on DIMMs)	2	DQS[8:0]_t	Data strobes	9
RAS_n	Row Address Strobe	1	DQS[8:0]_c	Data strobes, negative line	9
CAS_n	Column Address Strobe	1	DM[8:0]/ DQS[17:9]_t, TDQS[17:9]_t	Data Masks / Data strobes, Termination data strobes	9
WE_n	Write Enable	1	DQS[17:9]_c TDQS[17:9]_c	Data strobes, negative line, Termination data strobes	9
S[1:0]_n	Chip Selects	2	EVENT_n	Reserved for optional hardware temperature sensing	1
S[3:2]_n, A17, A16	Chip Selects Address Inputs	2	TEST	Memory bus test tool (Not Connected and Not Useable on DIMMs)	1
A[9:0],A11, A[15:13]	Address Inputs	14	RESET_n	Register and SDRAM control pin	1
A10/AP	Address Input/Autoprecharge	1	V _{DD}	Power Supply	22
A12/BC_n	Address Input/Burst chop	1	V _{SS}	Ground	59
BA[2:0]	SDRAM Bank Addresses	3	V _{REFDQ}	Reference Voltage for DQ	1
SCL	Serial Presence Detect (SPD) Clock Input	1	V _{REFCA}	Reference Voltage for CA	1
SDA	SPD Data Input/Output	1	V _{TT}	Termination Voltage	4
SA[2:0]	SPD Address Inputs	3	V _{DDSPD}	SPD Power	1

Proposed

Load Reduced DIMM Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0_t	IN	Positive Line	Positive line of the differential pair of system clock inputs that drives input to the on-DIMM Clock Driver.
CK0_c	IN	Negative Line	Negative line of the differential pair of system clock inputs that drives the input to the on-DIMM Clock Driver.
CK1_t	IN	Positive Line	Terminated but not used on RDIMMs.
CK1_c	IN	Negative Line	Terminated but not used on RDIMMs.
CKE[3:0]	IN	Active High	CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers of the SDRAMs. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank)
S[3:0]_n	IN	Active Low	Enables the command decoders for the associated rank of SDRAM when low and disables decoders when high. When decoders are disabled, new commands are ignored and previous operations continue. Other combinations of these input signals perform unique functions, including disabling all outputs (except CKE and ODT) of the register(s) on the DIMM or accessing internal control words in the register device(s). For modules with two registers, S[3:2]_n operate similarly to S[1:0]_n for the second set of register outputs or register control words.
ODT[1:0]	IN	Active High	On-Die Termination control signals
RAS_n, CAS_n, WE_n	IN	Active Low	When sampled at the positive rising edge of the clock, CAS_n, RAS_n, and WE_n define the operation to be executed by the SDRAM.
V _{REFDQ}	Supply		Reference voltage for DQ0-DQ63 and CB0-CB7.
V _{REFCA}	Supply		Reference voltage for A0-A17, BA0-BA2, RAS_n, CAS_n, WE_n, S0_n, S1_n, S2_n, S3_n, CKE0, CKE1, CKE2, CKE3, Par_In, ODT0 and ODT1.
BA[2:0]	IN	—	Selects which SDRAM bank of eight is activated. BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines mode register is to be accessed during an MRS cycle.
A[17:13, 12/BC_n,11, 10/AP_n,9:0]	IN	—	Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA. A12 is also utilized for BL 4/8 identification for "BL on the fly" during CAS_n command. The address inputs also provide the op-code during Mode Register Set commands.
DQ[63:0], CB[7:0]	I/O	—	Data and Check Bit Input/Output pins
DM[8:0]	IN	Active High	Masks write data when high, issued concurrently with input data.
V _{DD} , V _{SS}	Supply		Power and ground for the DDR SDRAM input buffers and core logic.
V _{TT}	Supply		Termination Voltage for Address/Command/Control/Clock nets.
DQS[17:0]_t	I/O	Positive Edge	Positive line of the differential data strobe for input and output data.
DQS[17:0]_c	I/O	Negative Edge	Negative line of the differential data strobe for input and output data.

Proposed

Load Reduced DIMM Input/Output Functional Description (Continued)

Symbol	Type	Polarity	Function
TDQS[17:9]_t TDQS[17:9]_c	OUT		TDQS_t/TDQS_c is applicable for X8 DRAMs only. When enabled via Mode Register A11=1 in MR1, DRAM will enable the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via mode register A11=0 in MR1, DM/TDQS_t will provide the data mask function and TDQS_c is not used. X4/X16 DRAMs must disable the TDQS function via mode register A11=0 in MR1
SA[2:0]	IN	—	These signals are tied at the system planar to either V_{SS} or V_{DDSPD} to configure the serial SPD EEPROM address range.
SDA	I/O	—	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DDSPD} on the system planar to act as a pullup.
SCL	IN	—	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus line to V_{DDSPD} on the system planar to act as a pullup.
EVENT_n	OUT (open drain)	Active Low	This signal indicates that a thermal event has been detected in the thermal sensing device. The system should guarantee the electrical level requirement is met for the EVENT_n pin on TS/SPD part. No pull-up resistor is provided on DIMM.
V_{DDSPD}	Supply		Serial EEPROM positive power supply wired to a separate power pin at the connector which supports from 3.0 Volt to 3.6 Volt (nominal 3.3V) operation.
RESET_n	IN	Active Low	The RESET_n pin is connected to the RESET_n pin on the register and to the RESET_n pin on the DRAM.
Par_In	IN		Parity bit for the Address and Command bus. ("1 ": Odd, "0 ": Even)
ErrOut_n	OUT (open drain)		Parity error detected on the Address and Command bus. A resistor may be connected from ErrOut_n bus line to V_{DD} on the system planar to act as a pull up.
TEST			Used by memory bus analysis tools (unused (NC) on memory DIMMs)

Proposed

DDR3 240-pin LRDIMM, RDIMM and UDIMM Pinout

Pin#	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin#	Front Side	Pin#	Back Side
1	V _{REFDQ}	121	V _{SS}	31	DQ25	151	V _{SS}	61	A2	181	A1	91	DQ41	211	V _{SS}
2	V _{SS}	122	DQ4	32	V _{SS}	152	DM3, DQS12_t, TDQS12_t	62	V _{DD}	182	V _{DD}	92	V _{SS}	212	DM5, DQS14_t, TDQS14_t
3	DQ0	123	DQ5	33	DQS3_c	153	NC,DQS12_c, TDQS12_c	63	NC, CK1_t	183	V _{DD}	93	DQS5_c	213	NC, DQS14_c, TDQS14_c
4	DQ1	124	V _{SS}	34	DQS3_t	154	V _{SS}	64	NC, CK1_c	184	CK0_t	94	DQS5_t	214	V _{SS}
5	V _{SS}	125	DM0,DQS9_t, TDQS9_t	35	V _{SS}	155	DQ30	65	V _{DD}	185	CK0_c	95	V _{SS}	215	DQ46
6	DQS0_c	126	NC,DQS9_c, TDQS9_c	36	DQ26	156	DQ31	66	V _{DD}	186	V _{DD}	96	DQ42	216	DQ47
7	DQS0_t	127	V _{SS}	37	DQ27	157	V _{SS}	67	V _{REFCA}	187	EVENT_n, NC	97	DQ43	217	V _{SS}
8	V _{SS}	128	DQ6	38	V _{SS}	158	CB4,NC	68	Par_In, NC	188	A0	98	V _{SS}	218	DQ52
9	DQ2	129	DQ7	39	CB0,NC	159	CB5,NC	69	V _{DD}	189	V _{DD}	99	DQ48	219	DQ53
10	DQ3	130	V _{SS}	40	CB1,NC	160	V _{SS}	70	A10 / AP	190	BA1	100	DQ49	220	V _{SS}
11	V _{SS}	131	DQ12	41	V _{SS}	161	NC, DM8, DQS17_t, TDQS17_t	71	BA0	191	V _{DD}	101	V _{SS}	221	DM6, DQS15_t, TDQS15_t
12	DQ8	132	DQ13	42	DQS8_c	162	NC,DQS17_c, TDQS17_c	72	V _{DD}	192	RAS_n	102	DQS6_c	222	NC, DQS15_c, TDQS15_c
13	DQ9	133	V _{SS}	43	DQS8_t	163	V _{SS}	73	WE_n	193	S0_n	103	DQS6_t	223	V _{SS}
14	V _{SS}	134	DM1, DQS10_t, TDQS10_t	44	V _{SS}	164	CB6,NC	74	CAS_n	194	V _{DD}	104	V _{SS}	224	DQ54
15	DQS1_c	135	NC, DQS10_c, TDQS10_c	45	CB2,NC	165	CB7,NC	75	V _{DD}	195	ODT0	105	DQ50	225	DQ55
16	DQS1_t	136	V _{SS}	46	CB3,NC	166	V _{SS}	76	S1_n, NC	196	A13	106	DQ51	226	V _{SS}
17	V _{SS}	137	DQ14	47	V _{SS}	167	NC(TEST), CKE2	77	ODT1, CKE3, NC	197	V _{DD}	107	V _{SS}	227	DQ60
18	DQ10	138	DQ15	48	VTT, NC	168	RESET_n	78	V _{DD}	198	S3_n, A17, NC	108	DQ56	228	DQ61
19	DQ11	139	V _{SS}	KEY				79	S2_n, A16, NC	199	V _{SS}	109	DQ57	229	V _{SS}
20	V _{SS}	140	DQ20	49	VTT, NC	169	CKE1, NC	80	V _{SS}	200	DQ36	110	V _{SS}	230	DM7, DQS16_t, TDQS16_t
21	DQ16	141	DQ21	50	CKE0	170	V _{DD}	81	DQ32	201	DQ37	111	DQS7_c	231	NC, DQS16_c, TDQS16_c
22	DQ17	142	V _{SS}	51	V _{DD}	171	A15	82	DQ33	202	V _{SS}	112	DQS7_t	232	V _{SS}
23	V _{SS}	143	DM2, DQS11_t, TDQS11_t	52	BA2	172	A14	83	V _{SS}	203	DM4, DQS13_t, TDQS13_t	113	V _{SS}	233	DQ62
24	DQS2_c	144	NC, DQS11_c, TDQS11_c	53	ErrOut_n NC	173	V _{DD}	84	DQS4_c	204	NC, DQS13_c, TDQS13_c	114	DQ58	234	DQ63
25	DQS2_t	145	V _{SS}	54	V _{DD}	174	A12 / BC_n	85	DQS4_t	205	V _{SS}	115	DQ59	235	V _{SS}
26	V _{SS}	146	DQ22	55	A11	175	A9	86	V _{SS}	206	DQ38	116	V _{SS}	236	VDDSPD
27	DQ18	147	DQ23	56	A7	176	V _{DD}	87	DQ34	207	DQ39	117	SA0	237	SA1
28	DQ19	148	V _{SS}	57	V _{DD}	177	A8	88	DQ35	208	V _{SS}	118	SCL	238	SDA
29	V _{SS}	149	DQ28	58	A5	178	A6	89	V _{SS}	209	DQ44	119	SA2	239	V _{SS}
30	DQ24	150	DQ29	59	A4	179	VDD	90	DQ40	210	DQ45	120	V _{TT}	240	V _{TT}
				60	V _{DD}	180	A3								

See Notes on following page for differences of RDIMMs and UDIMMs and LRDIMMs

Proposed

Pinout Comparison Between UDIMM Type and LRDIMM Type

Pin #	UDIMM		LRDIMM	
	Signal	Notes	Signal	Notes
48, 49	NC	Not used on UDIMMs	VTT	Termination Voltage for Address/Command/Control/Clock nets.
120, 240	VTT	Termination Voltage for Address/Command/Control/Clock nets.	VTT	Termination Voltage for Address/Command/Control/Clock nets.
53	NC	Not used on UDIMMs	ERROut_n	Parity error output of Memory Buffer
63	CK1_t	Used for 2 rank UDIMMs, not used on single-rank UDIMMs, but terminated	CK1_t	Terminated but not used
64	CK1_c		CK1_c	
68	NC	Not used on UDIMMs	Par_In	Parity input to Memory Buffer (MB). This signal is required for MB functionality.
76	S1_n	Used for dual-rank UDIMMs, not connected on single-rank UDIMMs	S1_n	Chip select for the second logical rank. Required for programming the Memory Buffer. SMBus can be used for programming the MB.
77	ODT1, NC	Used for dual-rank UDIMMs, not connected on single-rank UDIMMs	ODT1, CKE3	Provides 4th CKE signal. Not used on JEDEC standard LRDIMMs but may be used on custom LRDIMMs. Connected to MB.
79	NC	Not used on UDIMMs	S2_n, A16	May be used as third chip select or address A16. Use is system dependent. MB can be programmed to use it as chip select 2 or address A16.
167	NC	TEST input used only on bus analysis probes	CKE2	Not used on JEDEC standard LRDIMMs but may be used on custom LRDIMMs.
169	CKE1, NC	Used for dual-rank UDIMMs, not connected on single-rank UDIMMs	CKE1	2nd CKE.
171	A15, NC	Depending on device density, may not be connected to SDRAMs on UDIMMs. However, these signals are terminated on UDIMMs. A15 not routed on some RCs	A15	Always used on LRDIMMs
172	A14		A14	
196	A13		A13	
198	NC	Not used on UDIMMs	S3_n, A17	May be used as either a 4th chip select or address A17. Use is system dependent. MB can be programmed to use it as chip select 3 or address A17.
39, 40, 45, 46, 158, 159, 164, 165	NC, CBn	Used on x72 UDIMMs, (n = 0...7); not used on x64 UDIMMs	CBn	ECC byte. Always used on LRDIMM.
125, 134, 143, 152, 161, 203, 212, 221, 230	DMn	Connected to DM on x8 DRAMs, UDM or LDM on x16 DRAMs on UDIMMs; (n = 0...8)	DQS [9:17]_t	Always connected to MB. Typically used for LRDIMMs with x4 SDRAMs. Not used for LRDIMMs with x8 SDRAMs.
126, 135, 144, 153, 162, 204, 213, 222, 231	NC	Not used on UDIMMs	DQS [9:17]_c	Always connected to MB. Typically used for LRDIMMs with x4 SDRAMs. Not used for LRDIMMs with x8 SDRAMs.
187	EVENT_n NC	Connected to the thermal sensing component on ECC DIMMs. No connection on non-ECC DIMMs.	EVENT_n	Connected to the thermal sensing component and MB.

NC = no internal connection

Proposed

Pinout Comparison Between RDIMM Type and LRDIMM Type

Pin #	RDIMM		LRDIMM	
	Signal	Notes	Signal	Notes
77	ODT1, NC	ODT1 is connected to the register on dual- and quad- rank RDIMMs; NC on single-rank RDIMMs, CKE3 is not available for RDIMMs	ODT1, NC, CKE3	ODT1, CKE3 is connected to the Memory Buffer. It has no defined functionality in normal use but is available for custom applications.
79	S2_n, NC	S2_n is connected to the register on quad-rank RDIMMs, not connected on single or dual rank RDIMMs. A16 is not available for RDIMMs	S2_n, NC, A16	S2_n, A16 is connected to the Memory Buffer. Based on system configuration it may be used as an additional chip select or an addition address input.
167	NC	TEST input used only on bus analysis probes. CKE2 is not available for RDIMMs	NC, CKE2	TEST input used only on bus analysis probes. The CKE2 function is only available on custom modules.
198	S3_n, NC	Connected to the register on quad-rank RDIMMs, not connected on single-or dual-rank RDIMMs	S3_n, NC, A17	S3_n, A17 is connected to the Memory Buffer. Based on system configuration it may be used as an additional chip select or an addition address input.
NC = no internal connection				

Proposed

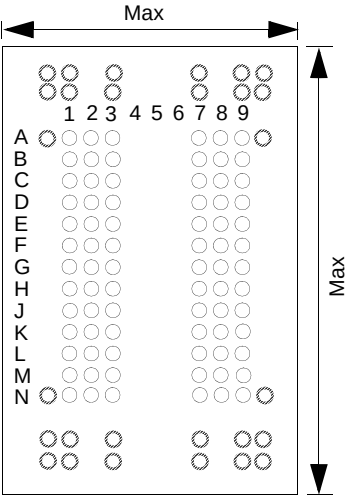
Component Details

Supported SDRAM Components Maximum size for 1Gb to 4Gb; DDR3 SDRAM

This table is for reference only. Please see appropriate raw card appendix for more information.

Raw Card	Supported DRAM Outline (Width x Length) max.	Configuration	SDRAM Placement	Package Type	Module Height (mm)	MO-207 variation	# of SDRAM balls supported
A	11.0 mm x 12.0 mm	2 rank x4	2 row vertical	Planar	30.35	DW-z	82
B	11.0 mm x 12.0 mm	4 rank x8	2 row vertical	Planar	30.35	DW-z	82
C	11.0 mm x 11.6 mm	4 rank x4	2 row vertical	DDP	30.35	DW-z	82
D	11.0 mm x 12.0 mm	8 rank x8	2 row vertical	DDP	30.35	DW-z	82
E	11.0 mm x 12.0 mm	8 rank x4	2 row vertical	QDP	30.35	DW-z	82
F	11.0 mm x 12.0 mm	2 rank x4	1 row vertical	DDP	18.75	DW-z	82
G	11.0 mm x 12.0 mm	4 rank x8	1 row vertical	DDP	18.75	DW-z	82
H	11.0 mm x 12.0 mm	4 rank x4	1 row vertical	QDP	18.75	DW-z	82
J	11.0 mm x 12.0 mm	8 rank x8	1 row vertical	QDP	18.75	DW-z	82
K	10.0 mm x 13.0 mm	4 rank x4	2 row flower	DDP	30.35	DW-z	82
	11.0 mm x 12.0 mm						

Note: 1. DDP refers to a 2 die stack. QDP refers to a 4 die stack.



Proposed

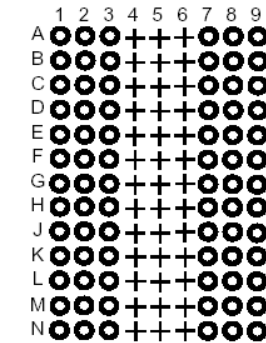
Pin Assignments for 1Gb to 4Gb; DDR3 SDRAM

(MO-207 Variation DT-z/DW-z, FBGA 0.8mm x 0.8 mm pitch)

x4 Ballout of DDR3 SDRAMs (Top view)

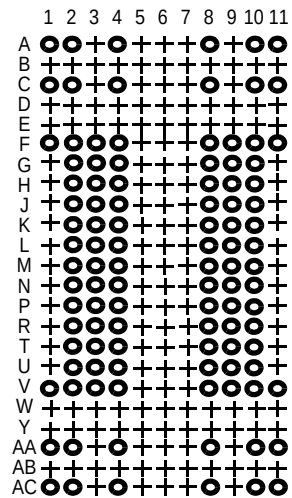
	1	2	3	4	8	9	10	11	
A	NC	NC		NC	NC		NC	NC	
B									
C	NC	NC		NC	NC		NC	NC	
D									
E									
F	NC	VSS	VDD	NC	NC	VSS	VDD	NC	A
G		VSS	VSSQ	DQ0	DM	VSSQ	VDDQ		B
H		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ		C
J		VSSQ	NC	DQS_c	VDD	VSS	VSSQ		D
K		V _{REFDQ}	VDDQ	NC	NC	NC	VDDQ		E
L		NC	VSS	RAS_n	CK_t	VSS	NC		F
M		ODT	VDD	CAS_n	CK_c	VDD	CKE		G
N		NC	CS	WE_n	A10/AP	ZQ	NC		H
P		VSS	BA0	BA2	A15	V _{REFCA}	VSS		J
R		VDD	A3	A0	A12/BC_n	BA1	VDD		K
T		VSS	A5	A2	A1	A4	VSS		L
U		VDD	A7	A9	A11	A6	VDD		M
V	NC	VSS	RESET_n	A13	A14	A8	VSS	NC	N
W									
Y									
AA	NC	NC		NC	NC		NC	NC	
AB									
AC	NC	NC		NC	NC		NC	NC	
		1	2	3	7	8	9		

MO-207 Variation DT-z



● Populated ball
+ Ball not populated

MO-207 Variation DW-z
with support balls



Proposed

Note: 1. Above coordinates of ball out corresponds to footprint on PCB (page 16).

Note: 2. "NC" means that the ball is present and is not connected to any signal in the SDRAM package.

Note: 3. NC balls may be mated with any solder pad on PCB.

Note: 4. This figure is valid for SDRAM specification as defined by JESD79-3. Refer to that specification for any later revisions

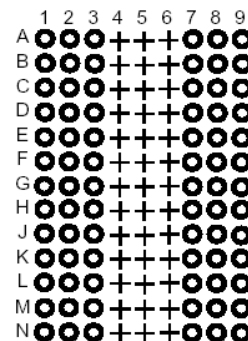
Pin Assignments for 1Gb to 4Gb; DDR3 SDRAM

(MO-207 Variation DT-z/DW-z, FBGA 0.8 mm x 0.8 mm pitch)

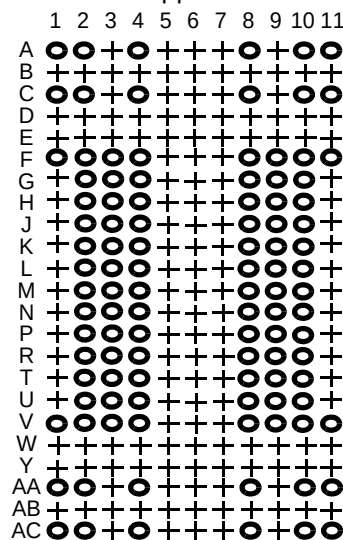
x8 Ballout of DDR3 SDRAMs (Top view)

	1	2	3	4	8	9	10	11	
A	NC	NC		NC	NC		NC	NC	
B									
C	NC	NC		NC	NC		NC	NC	
D									
E									
F	NC	VSS	VDD	NC	NU/ TDQS_c	VSS	VDD	NC	A
G		VSS	VSSQ	DQ0	DM/ TDQS_t	VSSQ	VDDQ		B
H		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ		C
J		VSSQ	DQ6	DQS_c	VDD	VSS	VSSQ		D
K		V _{REFDQ}	VDDQ	DQ4	DQ7	DQ5	VDDQ		E
L		NC	VSS	RAS_n	CK_t	VSS	NC		F
M		ODT	VDD	CAS_n	CK_c	VDD	CKE		G
N		NC	CS#	WE_n	A10/AP	ZQ	NC		H
P		VSS	BA0	BA2	A15	V _{REFCA}	VSS		J
R		VDD	A3	A0	A12/ BC_n	BA1	VDD		K
T		VSS	A5	A2	A1	A4	VSS		L
U		VDD	A7	A9	A11	A6	VDD		M
V	NC	VSS	RESET_n	A13	A14	A8	VSS	NC	N
W									
Y									
AA	NC	NC		NC	NC		NC	NC	
AB									
AC	NC	NC		NC	NC		NC	NC	
		1	2	3	7	8	9		

MO-207 Variation DT-z



MO-207 Variation DW-z
with support balls



Proposed

Note: 1. Above coordinates of ball out corresponds to footprint on PCB (page 21).

Note: 2. "NC" means that the ball is present and is not connected to any signal in the SDRAM package.

Note: 3. NC balls may be mated with any solder pad on PCB.

Note: 4. "NU" means that the ball is present and may or may not be electrically connected a an active signal in the SDRAM package.

Note: 5. NU balls may only be mated with NC solder pads on PCB.

Note: 6. This figure is valid for SDRAM specification as defined by JESD79-3. Refer to that specification for any later revisions.

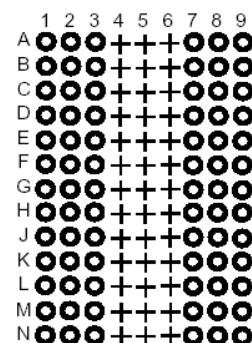
Pin Assignments for 1Gb to 4Gb; DDR3 SDRAM

MO-207 Variation DW-z, FBGA 0.8 mm x 0.8 mm pitch)

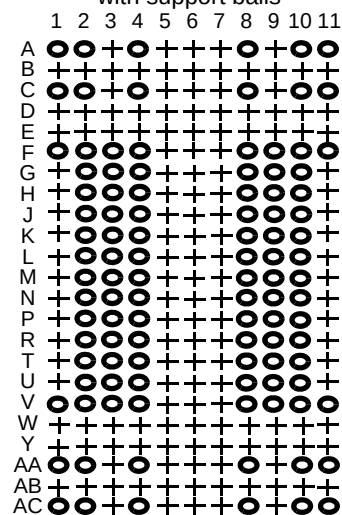
x4 Ballout of DDR3 SDRAMs for DDP Stacked DIMM (Top view)

	1	2	3	4	8	9	10	11	
A	NC	NC		NC	NC		NC	NC	
B									
C	NC	NC		NC	NC		NC	NC	
D									
E									
F	NC	VSS	VDD	NC	NC	VSS	VDD	NC	A
G		VSS	VSSQ	DQ0	DM	VSSQ	VDDQ		B
H		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ		C
J		VSSQ	NC	DQS_c	VDD	VSS	VSSQ		D
K		V _{REFDQ}	VDDQ	NC	NC	NC	VDDQ		E
L		ODT1	VSS	RAS_n	CK_t	VSS	CKE1		F
M		ODT0	VDD	CAS_n	CK_c	VDD	CKE0		G
N		CS1_n	CS0_n	WE_n	A10/AP	ZQ0	ZQ1		H
P		VSS	BA0	BA2	A15	V _{REFCA}	VSS		J
R		VDD	A3	A0	A12/BC_n	BA1	VDD		K
T		VSS	A5	A2	A1	A4	VSS		L
U		VDD	A7	A9	A11	A6	VDD		M
V	NC	VSS	RESET_n	A13	A14	A8	VSS	NC	N
W									
Y									
AA	NC	NC		NC	NC		NC	NC	
AB									
AC	NC	NC		NC	NC		NC	NC	
		1	2	3	7	8	9		

MO-207 Variation DT-z



MO-207 Variation DW-z with support balls



Proposed

Note: 1. Above coordinates of ball out corresponds to footprint on PCB (page 22).

Note: 2. "NC" means that the ball is present and is not connected to any signal in the SDRAM package.

Note: 3. NC balls may be mated with any solder pad on PCB.

Note: 4. This figure is valid for SDRAM specification as defined by JESD79-3. Refer to that specification for any later revisions.

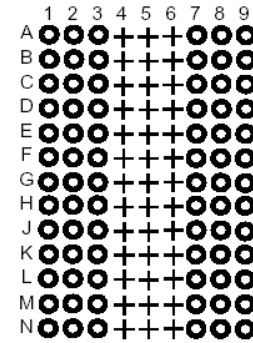
Pin Assignments for 1Gb to 4Gb; DDR3 SDRAM

MO-207 Variation DW-z, FBGA 0.8 mm x 0.8 mm pitch)

x8 Ballout of DDR3 SDRAMs for Stacked DDP DIMM (Top view)

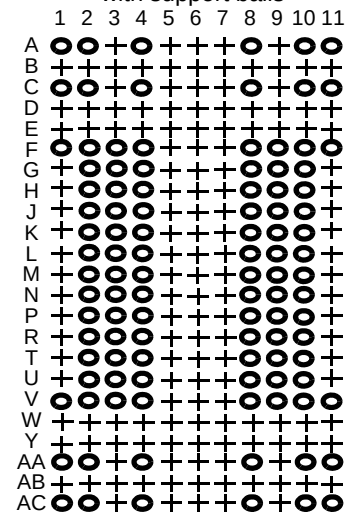
	1	2	3	4	8	9	10	11	
A	NC	NC		NC	NC		NC	NC	
B									
C	NC	NC		NC	NC		NC	NC	
D									
E									
F	NC	VSS	VDD	NC	NU/ TDQS_c	VSS	VDD	NC	A
G		VSS	VSSQ	DQ0	DM/ TSDQS_t	VSSQ	VDDQ		B
H		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ		C
J		VSSQ	DQ6	DQS_c	VDD	VSS	VSSQ		D
K		V _{REFDQ}	VDDQ	DQ4	DQ7	DQ5	VDDQ		E
L		ODT1	VSS	RAS_n	CK_t	VSS	CKE1		F
M		ODT0	VDD	CAS_n	CK_c	VDD	CKE0		G
N		CS1_n	CS0_n	WE_n	A10/AP	ZQ0	ZQ1		H
P		VSS	BA0	BA2	A15	V _{REFCA}	VSS		J
R		VDD	A3	A0	A12/BC_n	BA1	VDD		K
T		VSS	A5	A2	A1	A4	VSS		L
U		VDD	A7	A9	A11	A6	VDD		M
V	NC	VSS	RESET_n	A13	A14	A8	VSS	NC	N
W									
Y									
AA	NC	NC		NC	NC		NC	NC	
AB									
AC	NC	NC		NC	NC		NC	NC	
		1	2	3	7	8	9		

MO-207 Variation DT-z



● Populated ball
+ Ball not populated

MO-207 Variation DW-z
with support balls



Proposed

Note: 1. Above coordinates of ball out corresponds to footprint on PCB (page 22).

Note: 2. "NC" means that the ball is present and is not connected to any signal in the SDRAM package.

Note: 3. NC balls may be mated with any solder pad on PCB.

Note: 4. This figure is valid for SDRAM specification as defined by JESD79-3. Refer to that specification for any later revisions.

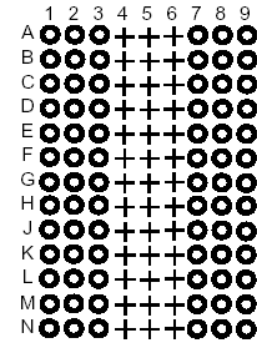
Pin Assignments for 1Gb to 4Gb; DDR3 SDRAM

MO-207 Variation DW-z, FBGA 0.8 mm x 0.8 mm pitch)

x4 Ballout of DDR3 SDRAMs for Stacked QDP DIMM (Top view)

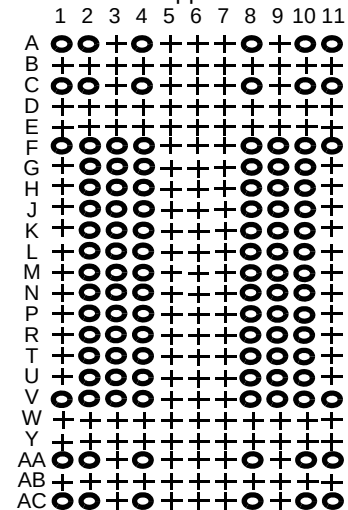
	1	2	3	4	8	9	10	11	
A	NC	NC		NC	NC		NC	NC	
B									
C	NC	NC		NC	NC		NC	NC	
D									
E									
F	NC	VSS	VDD	NC	NU/ TDQS_c	VSS	VDD	NC	A
G		VSS	VSSQ	DQ0	DM/ TSDQS_t	VSSQ	VDDQ		B
H		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ		C
J		VSSQ	DQ6	DQS_c	VDD	VSS	VSSQ		D
K		V _{REFDQ}	VDDQ	DQ4	DQ7	DQ5	VDDQ		E
L		ODT1	VSS	RAS_n	CK_t	VSS	CKE1		F
M		ODT0	VDD	CAS_n	CK_c	VDD	CKE0		G
N		CS1_n	CS0_n	WE_n	A10/AP	ZQ0	ZQ1		H
P		VSS	BA0	BA2	A15	V _{REFCA}	VSS		J
R		VDD	A3	A0	A12/BC_n	BA1	VDD		K
T		VSS	A5	A2	A1	A4	VSS		L
U		VDD	A7	A9	A11	A6	VDD		M
V	NC	VSS	RESET_n	A13	A14	A8	VSS	NC	N
W									
Y									
AA	NC	NC		NC	NC		NC	NC	
AB									
AC	NC	NC		NC	NC		NC	NC	
		1	2	3	7	8	9		

MO-207 Variation DT-z



● Populated ball
+ Ball not populated

MO-207 Variation DW-z
with support balls



Proposed

Note: 1. Above coordinates of ball out corresponds to footprint on PCB (page 16).

Note: 2. "NC" means that the ball is present and is not connected to any signal in the SDRAM package.

Note: 3. NC balls may be mated with any solder pad on PCB.

Note: 4. This figure is valid for SDRAM specification as defined by JESD79-3. Refer to that specification for any later revisions

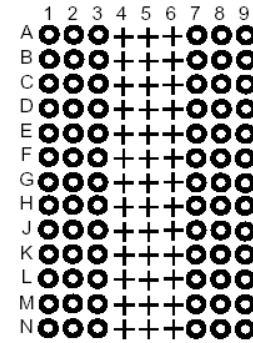
Pin Assignments for 1Gb to 4Gb; DDR3 SDRAM

MO-207 Variation DW-z, FBGA 0.8 mm x 0.8 mm pitch)

x8 Ballout of DDR3 SDRAMs for Stacked QDP DIMM (Top view)

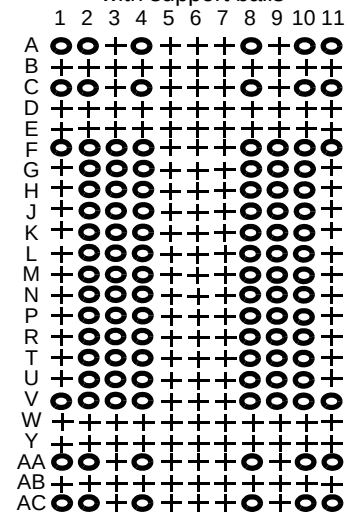
	1	2	3	4	8	9	10	11	
A	NC	NC		NC	NC		NC	NC	
B									
C	NC	NC		NC	NC		NC	NC	
D									
E									
F	NC	VSS	VDD	NC	NU/ TDQS_c	VSS	VDD	NC	A
G		VSS	VSSQ	DQ0	DM/ TSDQS_t	VSSQ	VDDQ		B
H		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ		C
J		VSSQ	DQ6	DQS_c	VDD	VSS	VSSQ		D
K		V _{REFDQ}	VDDQ	DQ4	DQ7	DQ5	VDDQ		E
L		ODT1	VSS	RAS_n	CK_t	VSS	CKE1		F
M		ODT0	VDD	CAS_n	CK_c	VDD	CKE0		G
N		CS1_n	CS0_n	WE_n	A10/AP	ZQ0	ZQ1		H
P		VSS	BA0	BA2	A15	V _{REFCA}	VSS		J
R		CS2_n	A3	A0	A12/BC_n	BA1	ZQ2		K
T		CS3_n	A5	A2	A1	A4	ZQ3		L
U		VDD	A7	A9	A11	A6	VDD		M
V	NC	VSS	RESET_n	A13	A14	A8	VSS	NC	N
W									
Y									
AA	NC	NC		NC	NC		NC	NC	
AB									
AC	NC	NC		NC	NC		NC	NC	
		1	2	3	7	8	9		

MO-207 Variation DT-z



● Populated ball
+ Ball not populated

MO-207 Variation DW-z
with support balls



Proposed

Note: 1. Above coordinates of ball out corresponds to footprint on PCB (page 16).

Note: 2. "NC" means that the ball is present and is not connected to any signal in the SDRAM package.

Note: 3. NC balls may be mated with any solder pad on PCB.

Note: 4. This figure is valid for SDRAM specification as defined by JESD79-3. Refer to that specification for any later revisions

PCB Pad Array Options for SDRAM Placements

MO-207 Variation DW-z allows any of the support balls locations to be non-populated. Many raw cards use the 72-pad array and thus support DRAM with four mechanical balls attached. The number of pads actually used is dependent on the package size of the DRAMs applied to the module. The 68-pad array corresponds with MO-207 Variation DT-z.

There are five basic pad arrays: x4 pad array, x8 pad array, x4 pad array DDP stacked, x8 pad array DDP stacked and x4 pad array QDP stacked. Each of these pad arrays may have a ball count variation. Below is a description of these 2 variations found on currently established raw card reference designs:

- 78-pad array (Variation DT-z, or DW-z with no support balls)
- 82-pad array (Variation DW-z with 4 support balls)

Proposed

x4 SDRAM Pad Array

(Top view)

		1	2	3	7	8	9	
	NC	NC		NC	NC		NC	NC
	NC	NC		NC	NC		NC	NC
A	NC	VSS	VDD	NC	NC	VSS	VDD	NC
B		VSS	VSSQ	DQ0	DM	VSSQ	VDDQ	
C		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ	
D		VSSQ	NC	DQS_c	VDD	VSS	VSSQ	
E		V _{REFDQ}	VDDQ	NC	NC	NC	VDDQ	
F		NC	VSS	RAS_n	CK_t	VSS	NC	
G		ODT	VDD	CAS_n	CK_c	VDD	CKE	
H		NC	CS_n	WE_n	A10/AP	ZQ	NC	
J		VSS	BA0	BA2	A15	V _{REFCA}	VSS	
K		VDD	A3	A0	A12/ BC_n	BA1	VDD	
L		VSS	A5	A2	A1	A4	VSS	
M		VDD	A7	A9	A11	A6	VDD	
N	NC	VSS	RESET_n	A13	A14	A8	VSS	NC
	NC	NC		NC	NC		NC	NC
	NC	NC		NC	NC		NC	NC

106-pad array (black outline)
(See MO-207, Variation DW-z)
(Includes all mechanical support balls)

78-pad array (yellow background)
(See MO-207, Variation DT-z)
(Includes no mechanical support balls)

82-pad array (light blue background)
(See MO-207, Variation DW-z)
(Includes 4 mechanical support balls)

Proposed

Note: 1. Above coordinates of footprint corresponds to previous ballout of DDR3 SDRAMs.

Note: 2. "NC" means that a solder pad is present and is not connected to any signal on the PCB.

Note: 3. NC solder pads may be mated with any balls of an SDRAM.

x8 SDRAM Pad Array

(Top view)

		1	2	3	7	8	9	
	NC	NC		NC	NC		NC	NC
	NC	NC		NC	NC		NC	NC
A	NC	VSS	VDD	NC	NU/ TDQS_c	VSS	VDD	NC
B		VSS	VSSQ	DQ0	DM/ TDQS_t	VSSQ	VDDQ	
C		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ	
D		VSSQ	DQ6	DQS_c	VDD	VSS	VSSQ	
E		V _{REFDQ}	VDDQ	DQ4	DQ7	DQ5	VDDQ	
F		NC	VSS	RAS_n	CK_t	VSS	NC	
G		ODT	VDD	CAS_n	CK_c	VDD	CKE	
H		NC	CS_n	WE_n	A10/AP	ZQ	NC	
J		VSS	BA0	BA2	A15	V _{REFCA}	VSS	
K		VDD	A3	A0	A12/BC_n	BA1	VDD	
L		VSS	A5	A2	A1	A4	VSS	
M		VDD	A7	A9	A11	A6	VDD	
N	NC	VSS	RESET_n	A13	A14	A8	VSS	NC
	NC	NC		NC	NC		NC	NC
	NC	NC		NC	NC		NC	NC

106-pad array (black outline)
(See MO-207, Variation DW-z)
(Includes all mechanical support balls)

78-pad array (yellow background)
(See MO-207, Variation DT-z)
(Includes no mechanical support balls)

82-pad array (light blue background)
(See MO-207, Variation DW-z)
(Includes 4 mechanical support balls)

Proposed

Note: 1. Above coordinates of footprint corresponds to previous ballout of DDR3 SDRAMs.

Note: 2. "NC" means that a solder pad is present and is not connected to any signal on the PCB.

Note: 3. NC solder pads may be mated with any balls of an SDRAM.

x4 SDRAM Pad Array DDP Stacked

(Top view)

		1	2	3	7	8	9	
	NC	NC		NC	NC		NC	NC
	NC	NC		NC	NC		NC	NC
A	NC	VSS	VDD	NC	NC	VSS	VDD	NC
B		VSS	VSSQ	DQ0	DM	VSSQ	VDDQ	
C		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ	
D		VSSQ	NC	DQS_c	VDD	VSS	VSSQ	
E		V _{REFDQ}	VDDQ	NC	NC	NC	VDDQ	
F		ODT1	VSS	RAS_n	CK_t	VSS	CKE1	
G		ODT0	VDD	CAS_n	CK_c	VDD	CKE0	
H		CS1_n	CS0_n	WE_n	A10/AP	ZQ0	ZQ1	
J		VSS	BA0	BA2	A15	V _{REFCA}	VSS	
K		VDD	A3	A0	A12/BC_n	BA1	VDD	
L		VSS	A5	A2	A1	A4	VSS	
M		VDD	A7	A9	A11	A6	VDD	
N	NC	VSS	RESET_n	A13	A14	A8	VSS	NC
	NC	NC		NC	NC		NC	NC
	NC	NC		NC	NC		NC	NC

106-pad array (black outline)
(See MO-207, Variation DW-z)
(Includes all mechanical support balls)

78-pad array (yellow background)
(See MO-207, Variation DT-z)
(Includes no mechanical support balls)

82-pad array (light blue background)
(See MO-207, Variation DW-z)
(Includes 4 mechanical support balls)

Proposed

Note: 1. Above coordinates of footprint corresponds to previous ballout of DDR3 SDRAMs.

Note: 2. "NC" means that a solder pad is present and is not connected to any signal on the PCB.

Note: 3. NC solder pads may be mated with any balls of an SDRAM.

x8 SDRAM Pad Array DDP Stacked

(Top view)

		1	2	3	7	8	9	
	NC	NC		NC	NC		NC	NC
	NC	NC		NC	NC		NC	NC
A	NC	VSS	VDD	NC	NU/ TDQS_c	VSS	VDD	NC
B		VSS	VSSQ	DQ0	DM/ TDQS_t	VSSQ	VDDQ	
C		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ	
D		VSSQ	DQ6	DQS_c	VDD	VSS	VSSQ	
E		V _{REFDQ}	VDDQ	DQ4	DQ7	DQ5	VDDQ	
F		ODT1	VSS	RAS_n	CK_t	VSS	CKE1	
G		ODT0	VDD	CAS_n	CK_c	VDD	CKE0	
H		CS1_n	CS0_n	WE_n	A10/AP	ZQ0	ZQ1	
J		VSS	BA0	BA2	A15	V _{REFCA}	VSS	
K		VDD	A3	A0	A12/BC_n	BA1	VDD	
L		VSS	A5	A2	A1	A4	VSS	
M		VDD	A7	A9	A11	A6	VDD	
N	NC	VSS	RESET_n	A13	A14	A8	VSS	NC
	NC	NC		NC	NC		NC	NC
	NC	NC		NC	NC		NC	NC

106-pad array (black outline)
(See MO-207, Variation DW-z)
(Includes all mechanical support balls)

78-pad array (yellow background)
(See MO-207, Variation DT-z)
(Includes no mechanical support balls)

82-pad array (light blue background)
(See MO-207, Variation DW-z)
(Includes 4 mechanical support balls)

Note: 1. Above coordinates of footprint corresponds to previous ballout of DDR3 SDRAMs.

Note: 2. "NC" means that a solder pad is present and is not connected to any signal on the PCB.

Note: 3. NC solder pads may be mated with any balls of an SDRAM.

Proposed

x4 SDRAM Pad Array QDP Stacked

(Top view)

		1	2	3	7	8	9	
	NC	NC		NC	NC		NC	NC
	NC	NC		NC	NC		NC	NC
A	NC	VSS	VDD	NC	NU/ TDQS_c	VSS	VDD	NC
B		VSS	VSSQ	DQ0	DM/ TDQS_t	VSSQ	VDDQ	
C		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ	
D		VSSQ	DQ6	DQS_c	VDD	VSS	VSSQ	
E		V _{REFDQ}	VDDQ	DQ4	DQ7	DQ5	VDDQ	
F		ODT1	VSS	RAS_n	CK_t	VSS	CKE1	
G		ODT0	VDD	CAS_n	CK_c	VDD	CKE0	
H		CS1_n	CS0_n	WE_n	A10/AP	ZQ0	ZQ1	
J		VSS	BA0	BA2	A15	V _{REFCA}	VSS	
K		VDD	A3	A0	A12/BC_n	BA1	VDD	
L		VSS	A5	A2	A1	A4	VSS	
M		VDD	A7	A9	A11	A6	VDD	
N	NC	VSS	RESET_n	A13	A14	A8	VSS	NC
	NC	NC		NC	NC		NC	NC
	NC	NC		NC	NC		NC	NC

106-pad array (black outline)
(See MO-207, Variation DW-z)
(Includes all mechanical support balls)

78-pad array (yellow background)
(See MO-207, Variation DT-z)
(Includes no mechanical support balls)

82-pad array (light blue background)
(See MO-207, Variation DW-z)
(Includes 4 mechanical support balls)

Proposed

x8 SDRAM Pad Array QDP Stacked

(Top view)

		1	2	3	7	8	9	
	NC	NC		NC	NC		NC	NC
	NC	NC		NC	NC		NC	NC
A	NC	VSS	VDD	NC	NU/ TDQS_c	VSS	VDD	NC
B		VSS	VSSQ	DQ0	DM/ TDQS_t	VSSQ	VDDQ	
C		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ	
D		VSSQ	DQ6	DQS_c	VDD	VSS	VSSQ	
E		V _{REFDQ}	VDDQ	DQ4	DQ7	DQ5	VDDQ	
F		ODT1	VSS	RAS_n	CK_t	VSS	CKE1	
G		ODT0	VDD	CAS_n	CK_c	VDD	CKE0	
H		CS1_n	CS0_n	WE_n	A10/AP	ZQ0	ZQ1	
J		VSS	BA0	BA2	A15	V _{REFCA}	VSS	
K		CS2_n	A3	A0	A12/BC_n	BA1	ZQ2	
L		CS3_n	A5	A2	A1	A4	ZQ3	
M		VDD	A7	A9	A11	A6	VDD	
N	NC	VSS	RESET_n	A13	A14	A8	VSS	NC
	NC	NC		NC	NC		NC	NC
	NC	NC		NC	NC		NC	NC

106-pad array (black outline)
(See MO-207, Variation DW-z)
(Includes all mechanical support balls)

78-pad array (yellow background)
(See MO-207, Variation DT-z)
(Includes no mechanical support balls)

82-pad array (light blue background)
(See MO-207, Variation DW-z)
(Includes 4 mechanical support balls)

Proposed

Pin Assignments for Memory Buffer

Memory Buffer (Top View)

588-Ball TFBGA 0.65 x 0.65 mm pitch [MO-XXX Variation X]

Left Side (1 of 3)

	A	B	C	D	E	F	G	H	J	K	L	M	N
20	NB	NB	VSS	DQ7	DQS9_t	DQ2	DQ3	VDD	DQ68	DQS17_t	DQ70	VSS	DQ66
19	NB	VSS	DQ4	DQ6	DQS9_c	VSS	DQ1	VSS	DQ69	DQS17_c	DQ71	VSS	DQ67
18	VSS	VDD	VSS	DQ5	DQS0_c	DQ0	NB	NB	NB	NB	NB	DQS8_t	DQ64
17	MDQ5	MDQ4	MDQ0	VSS	DQS0_t	VSS	NB	NB	NB	NB	NB	DQS8_c	DQ65
16	MDQS9_t	MDQS9_c	MDQS0_c	MDQS0_t	VDD	QACAS_n	NB	NB	NB	NB	NB	VDD	VDD
15	MDQ6	MDQ7	MDQ2	MDQ1	VDD	QARAS_n	NB	NB	NB	NB	NB	QAEC2	QAEC6
14	VSS	VSS	VSS	MDQ3	VDD	QAA15	NB	NB	NB	NB	NB	VDD	VDD
13	DQS1_t	DQS1_c	VSS	VDD	QAA10	QACKE1	NB	NB	NB	NB	NB	QAWEn	VDD
12	VDD	VSS	DQ8	VDD	QACKE0	QAA12	NB	NB	NB	NB	NB	QABA0	QABA2
11	DQ11	DQ10	DQ9	VDD	QABA1	QACKE2	NB	NB	NB	NB	NB	QAA0	VDD
10	DQ15	DQ14	DQ13	VDD	QACKE3	QAA4	NB	NB	NB	NB	NB	QAA3	QACS0_n QCS0_n
9	VDD	VSS	DQ12	VDD	QAA1	QAA5	NB	NB	NB	NB	NB	QACS3_n QCS3_n	QACS2_n QCS2_n
8	DQS10_t	DQS10_c	VSS	VDD	VDD	QAA11	NB	NB	NB	NB	NB	QAA5	QAA2
7	VSS	VSS	VSS	MDQ9	VDD	QAA8	NB	NB	NB	NB	NB	QA13	QAA9
6	MDQ12	MDQ13	MDQ8	MDQ11	VDD	QAA14	NB	NB	NB	NB	NB	QAA7	VDD
5	MDQS10_t	MDQS10_c	MDQS1_c	MDQS1_t	VSS	VDD	NB	NB	NB	NB	NB	VDD	VSS
4	MDQ14	MDQ15	MDQ10	VSS	DQS2_t	DQ16	NB	NB	NB	NB	NB	MDQS2_c	VSS
3	VSS	VDD	VSS	DQ19	DQS2_c	DQ17	NB	NB	NB	NB	NB	MDQS2_t	VSS
2	NB	VSS	DQ18	DQ22	DQS11_c	DQ20	VSS	MDQ20	MDQS11_c	MDQ22	VSS	MDQ16	MDQ18
1	NB	NB	VSS	DQ23	DQS11_t	DQ21	VSS	MDQ21	MDQS11_t	MDQ23	VSS	MDQ17	MDQ19
	A	B	C	D	E	F	G	H	J	K	L	M	N

Proposed

Middle (2 of 3)

	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE
20	VDD	Y3_c	Y3_t	Y1_t	Y1_c	Y2_c	Y2_t	Y0_t	Y0_c	VDD	ZQ	SCL
19	VDD	VSS	PVDD	VSS	PVDD	VSS	PVDD	VSS	PVDD	VSS	ZQVSS	SDA
18	VSS	MDQ68	MDQS17_t	MDQ70	MDQ64	MDQS8_c	MDQ66	VSS	CK_t	CK_c	VSS	VDD
17	VSS	MDQ69	MDQS17_c	MDQ71	MDQ65	MDQS8_t	MDQ67	TEST(0)	AVSS	AVDD	AOUT	TEST(2)
16	VDD	VSS	VDD	VSS	VDD	VSS	VDD	TEST(1)	VDD	VSS	VDD	VSS
15	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD
14	QAECC9	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS
13	QAODT1	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	QBCKE1
12	QAODT0	VSS	RESET_n	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	QBCKE0
11	VSS	VDD	DCKE2	VDD	DA1	VDD	VSS	DCS2_n	DCS4_n	DCS3_n	VSS	QBCKE3
10	QACS1_n QSC1_n	QRST_n	DCKE1	DA12	DA6	DA4	DA2	DA13	DCS0_n	DCS5_n	DBA1	VDD
9	VDD	DCKE0	DBA2	DA11	DA3	DA5	PAR_IN	DODT0	DA0	DBA0	DODT1 DCKE3	VSS
8	VDD	DA15	DA14	DA9	DA8	DA7	DCS1_n	DCAS_n	DRAS_n	DA10	DCS6_n	DCS7_n
7	VDD	VDD	ERROUT_n	VDD	VDD	VDD	VDD	VDD	VDD	DWE_n	VDD	VDD
6	DQ24	DQ25	VSS	MDQ29	MDQS12_t	VSS	MDQ36	MDQS13_t	MDQ37	VSS	DQ32	DQ33
5	DQS3_t	DQS3_c	VSS	MDQ30	MDQS12_c	MDQ28	VSS	MDQS13_c	MDQ38	VSS	DQS4_t	DQS4_c
4	DQ26	DQ27	VSS	MDQ31	MDQS3_c	VSS	MDQ32	MDQS4_c	MDQ39	VSS	DQ34	DQ35
3	VDD	DQ28	DQ29	VSS	MDQS3_t	MDQ24	VSS	MDQS4_t	VSS	DQ36	DQ37	VDD
2	VSS	DQS12_t	DQS12_c	VSS	MDQ25	VSS	MDQ33	MDQ34	VSS	DQS13_t	DQS13_c	VSS
1	VSS	DQ30	DQ31	VSS	MDQ26	MDQ27	VSS	MDQ35	VSS	DQ38	DQ39	VSS
	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE

Proposed

Right Side (3 of 3)

	AF	AG	AH	AJ	AK	AL	AM	AN	AP	AR	AT	AU	AV
20	SA2	SA0	QVREF CA	VDD	QVREF DQ	VDD	DQ59	DQ58	DQS7_t	DQ63	VSS	NB	NB
19	VCCSPD	SA1	VREFCA	VSS	VREF DQ	VSS	DQ57	VSS	DQS7_c	DQ62	DQ60	VSS	NB
18	EVENT_n	BFUNC	NB	NB	NB	NB	NB	DQ56	DQS16_c	DQ61	VSS	VDD	VSS
17	VSS	VDD	NB	NB	NB	NB	NB	VSS	DQS16_t	VSS	MDQ58	MDQ63	MDQ62
16	VDD	VSS	NB	NB	NB	NB	NB	QBWE_n	VDD	MDQS7_t	MDQS7_c	MDQS16_c	MDQS16_t
15	QBCAS_n	QBRAS_n	NB	NB	NB	NB	NB	QBBA0	VDD	MDQ59	MDQ57	MDQ61	MDQ60
14	VDD	VDD	NB	NB	NB	NB	NB	QBA0	VDD	MDQ56	VSS	VSS	VSS
13	QBA10	QBA15	NB	NB	NB	NB	NB	QBA3	QBODT1	VDD	VSS	DQS6_c	DQS6_t
12	VDD	VDD	NB	NB	NB	NB	NB	QBA2	QBBA2	VDD	DQ48	VSS	VDD
11	QBBA1	QBA12	NB	NB	NB	NB	NB	QBA5	QBODT0	VDD	DQ49	DQ50	DQ51
10	QBCKE2	QBA4	NB	NB	NB	NB	NB	QBCS1_n QCS5_n	QBCS0_n QCS4_n	VDD	DQ53	DQ54	DQ55
9	QBA1	QBA6	NB	NB	NB	NB	NB	QBCS3_n QCS7_n	QBCS2_n QCS6_n	VDD	DQ52	VSS	VDD
8	VDD	VDD	NB	NB	NB	NB	NB	QBA9	VDD	VDD	VSS	DQS15_c	DQS15_t
7	QBA11	QBA8	NB	NB	NB	NB	NB	QBA13	VDD	MDQ51	VSS	VSS	VSS
6	VDD	QBA14	NB	NB	NB	NB	NB	QBA7	VDD	MDQ49	MDQ50	MDQ55	MDQ54
5	VSS	VDD	NB	NB	NB	NB	NB	VDD	VSS	MDQS6_t	MDQS6_c	MDQS15_c	MDQS15_t
4	VSS	MDQS5_c	NB	NB	NB	NB	NB	DQ40	DQS5_t	VSS	MDQ48	MDQ53	MDQ52
3	VSS	MDQS5_t	NB	NB	NB	NB	NB	DQ41	DQS5_c	DQ45	VSS	VDD	VSS
2	MDQ40	MDQ43	VSS	MDQ44	MDQS14_t	MDQ47	VSS	DQ42	DQS14_c	DQ46	DQ44	VSS	NB
1	MDQ41	MDQ42	VSS	MDQ45	MDQS14_c	MDQ46	VSS	DQ43	DQS14_t	DQ47	VSS	NB	NB
	AF	AG	AH	AJ	AK	AL	AM	AN	AP	AR	AT	AU	AV

Proposed

Pin Assignments for Serial Presence Detect

(MO-229 Variation V/WCED-3, 2x3 mm package, 8 lead DFN 0.5 mm pitch)

(MO-229 Variation V/WEED-7, 3x3 mm package, 8 lead DFN 0.5 mm pitch)

256-byte Serial Presence Detect device, TSE2002 with thermal sensor

SPD Pinout (Top view)

TSE2002			
1	SA0	VDDSPD	8
2	SA1	EVENT	7
3	SA2	SCL	6
4	VSSSPD	SDA	5

Note: 1. Above rotations of leads correspond to footprints on PCB.

Note: 2. Refer to *JESD21C-4.1.2 -- SERIAL PRESENCE DETECT STANDARD*, General Standard for landing pattern details.

Proposed

DDR3 Load Reduced DIMM Wiring Details

Signal Groups

This specification categorizes timing-critical signals into eight groups. The following table summarizes the signals contained in each group.

Signal Group	Signals In Group
Clock Driver Input / Unused Clocks	CK0_t, CK0_c / CK1_t, CK1_c
Clock Driver Output	Yx_t, Yx_c
Pre-MB Data, DQS_t, DQS_c	DQ[63:0], CB[7:0], DQS[17:0_t], DQS[17:0]_c, DM[8:0]/ TDQS[17:9]_t, TDQS[17:9]_c
Post-MB Data, MDQS_t, MDQS_c	MDQ[71:0], MDQS[17:0_t], MDQS[17:0]_c,
Pre-MB Address and Control (Chip Select, Clock Enable, Parity, ODT)	A[15:0], BA[2:0], RAS_n, CAS_n, WE_n CS[3:0]_n, CKE[1:0], Par_In, ODT[1:0]
Post-MB Address and Control	QA[15..0], QBA[2..0], QRAS_n, QCAS_n, QWE_n, QCS[3:0]_n, QCKE[1:0], QODT[1:0]
Address and Command Parity	ErrOut_n
RESET_n	RESET_n

General Net Structure Routing Guidelines

Net structures and lengths must satisfy signal quality and setup/hold time requirements for the memory interface. Net structure diagrams for each signal group are shown in the following sections. Each diagram is accompanied by a trace length table that lists the minimum and maximum allowable lengths for each trace segment and/or net.

The general routing guidelines are as follows

- Route all signal traces except clocks using minimum of 0.075/0.1 rules, i.e., 0.075 mm traces and 0.1 mm minimum spacing between adjacent traces. But spacing should be as wide as possible to prevent crosstalk.
- Route clocks using minimum of 0.075 mm lines and 0.1 mm spaces between differential clock pairs and differential DQS_t, DQS_c.
- Route clocks using at least 90% of the total trace length in the inner layers. Maximize use of internal layers for routing clocks. Surface routing should be minimized and limited to what is necessary to connect to component.
- Signals are referenced to Vss or Vdd on adjacent layers. Data signals are referenced to Vss. Address and Command signals are referenced to VDD.
-

Signal referencing information

Signal groups	Referencing	Signal groups	Referencing
Pre-MB DQ/DQS pair	Ground layer	Pre-MB address and command net	Vdd shape
Post-MB MDQ/MDQS pair	Ground layer	Post-MB address and command net	Vdd shape
Clock nets	Vdd shape		

Differential Clock Net Structures

CK0_t, CK0_c, Yx_t, Yx_c

DDR3 SDRAM clock signals must be carefully routed to meet the following requirements:

- Signal quality
- Rise/Fall time
- Cross point of the differential pair into the SDRAM and register
- JEDEC-compatible reference delays
- Minimal segment length differences (less than 2.54 mm total) between clocks of the same function

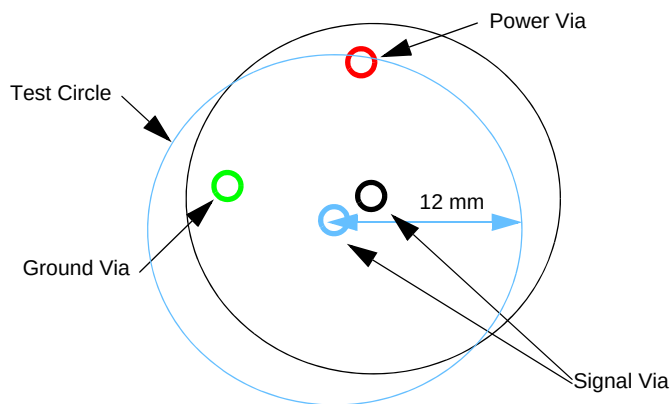
Clock Driver input net segment length is newly defined and optimized for high speed DDR3 Load Reduced DIMMs.

Proposed

Test Points

All DDR3 components are in BGA packages which makes the package pads inaccessible for probing during system development. The DDR3 Registered DIMMs have test points identified to make initial evaluation easier. In some cases test pads have been added and in other cases existing vias are used as test points. An effort has been made to provide testability on some signals in all signal groups but 100% coverage is not possible. All test points must have a power and/or ground via within 12 mm. Test point location and /or availability are indicated for each raw card in the corresponding appendices.

Test Point Location



Proposed

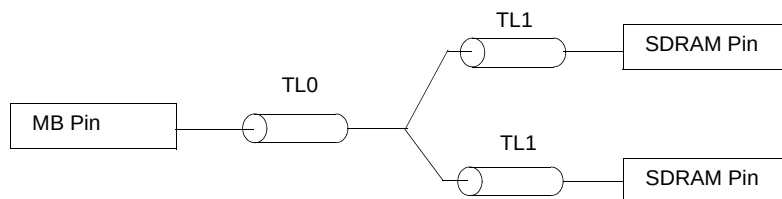
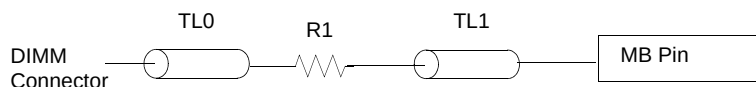
Explanation of Net Structure Diagrams

The net structure routing diagrams provide a reference design example for each raw card version. These designs provide an initial basis for registered DIMM designs. The diagrams should be used to determine individual signal wiring on a DIMM for any supported configuration. Only transmission lines (represented as cylinders and labeled with trace length designators “TL”) represent physical trace segments. All other lines are zero in length. To verify DIMM functionality, a full simulation of all signal integrity and timing is required. **The given net structures and trace lengths are not inclusive for all solutions.**

Once the net structure has been determined, the permitted trace lengths for the net structure can be read from the table below each net structure routing diagram. Some configurations require the use of multiple net structure routing diagrams to account for varying load quantities on the same signal. All diagrams define one load as one SDRAM input. **It is highly recommended that the net structure routing data in this document be simulated by the user.**

Net Structure Example

A 4 GB double-sided x72 DIMM using 1 Gbit, 128Mx8 SDRAM devices would have a data net structures as shown in the following diagrams.



Proposed

Timing Budgets

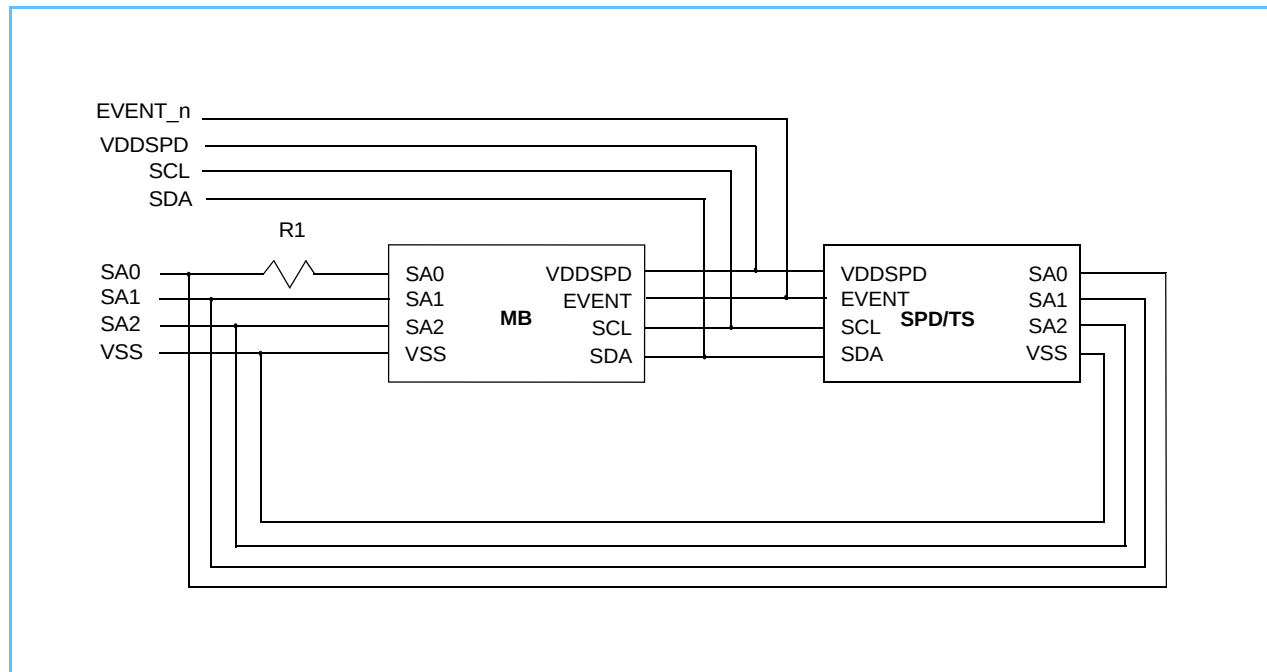
This section will be added following further definition of the Memory Buffer Specifications

Proposed

Wiring for SMBus

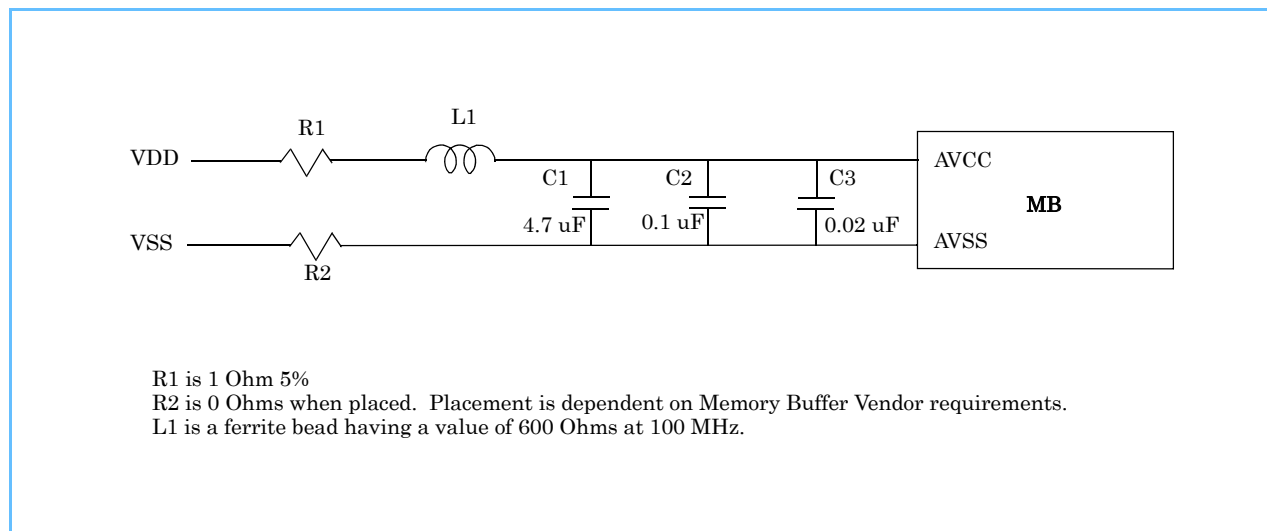
Schematic of SPD/Thermal Sensor and MB

The following schematic illustrates the required wiring of the SPD/TS and MB



This specific wiring is required. The value of R1 is typically 1K, 5% but this is a guideline. The SA0 pin may have 12 Volts applied to it for programming the SPD. Under these conditions the current into the MB must be limited. R1 serves the purpose of limiting the current into the MB.

The following schematic defines the required wiring for AVCC.



DIMM Wiring Requirements

These are requirements for compatibility. If deviations are required they must be identified and explained in the appropriate appendix.

All SDRAM components must have separate ZQ resistors for each pin on the SDRAM component.

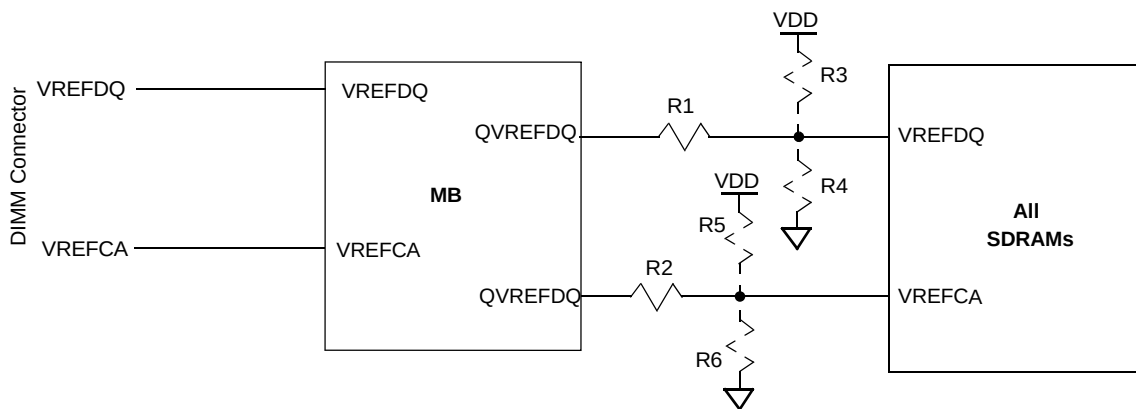
The ECC byte lane as defined by the edge connector must connect to MB pins identified as DQ63 to DQ71. For the ECC byte lane there must be a one to one match in the pin ordering between the connector and the MB, CB0 to DQ63, etc. The associated strobes must also be connected one to one.

For all other byte lanes, the strobes must match the routing as defined in the table. The bits must be kept with the associated strobes. For non-ECC byte lanes and modules with x8 SDRAM components swapping bits within the byte is allowed. For non-ECC byte lanes and modules with x4 SDRAM components swapping bits within the nibble is allowed. For non-ECC byte lanes and modules with x4 SDRAM components swapping bits between nibbles is not allowed.

Gold Finger to Memory Buffer Mapping Table

DIMM Gold Finger Connector Pin Name	Horizontal MB MB Pin Name	Vertical MB MB Pin Name	DIMM Gold Finger Connector Pin Name	Horizontal MB MB Pin Name	Vertical MB MB Pin Name
DQS0	DQS0	DQS5	DQS9	DQS9	DQS14
DQS1	DQS1	DQS2	DQS10	DQS10	DQS11
DQS2	DQS2	DQS3	DQS11	DQS11	DQS12
DQS3	DQS3	DQS4	DQS12	DQS12	DQS13
DQS4	DQS4	DQS7	DQS13	DQS13	DQS16
DQS5	DQS5	DQS1	DQS14	DQS14	DQS10
DQS6	DQS6	DQS0	DQS15	DQS15	DQS9
DQS7	DQS7	DQS6	DQS16	DQS16	DQS15
DQS8	DQS8	DQS8	DQS17	DQS17	DQS17

Proposed



As illustrated in the figure VREFCA from the edge connector must be wired to VREFCA of the MB. VREFDQ from the edge connector must be wired to VREFDQ of the MB. VREFCA and VREFDQ for the SDRAMs components must be wired to resistor dividers as illustrated with R3/R4 and R5/R6. The values of R3, R4, R5

and R6 are TBD. These are not placed on the JEDEC standard DIMM. QVREFDQ and QVREFCA from the MB must be wired to the SDRAMs through series resistors as illustrated with R1 and R2. These resistors are zero Ohms and will be placed on JEDEC standard DIMMs.

Pin 77 of the edge connector is defined as ODT1 or CKE3. It will be wired to the MB through a TBD Ohm resistor.

Pin 167 of the edge connector is defined as CKE2. For the JEDEC standard LRDIMM it is not used. It will be wired to the MB through a TBD Ohm resistor.

All LRDIMMs will provide some feature to reduce capacitance at the edge connector for the DQ bus. The details of how this is done will be defined by each raw card and included in the appendix.

Proposed

Serial Presence Detect Definition

Removed for now. Will request the JEDEC office add once the SPD spec is complete.

Proposed

DDR3 DIMM Label Format

This material is provided as reference only.

DDR3 "End-User" DIMM Label Format:

The following label shall be applied to all DDR3 memory modules targeted at end-user type products to fully describe the key attributes of the module. The label can be in the form of a stick-on label, silk screened onto the assembly, or marked using an alternate customer-readable format. A readable point size should be used, and the number can be printed in one or more rows on the label. Hyphens may be dropped when lines are split, or when font changes sufficiently separate fields. Unused letters in each field, such as ggggg, are to be omitted when not needed.

Voltage options in field 'v' describe the nominal voltage VDD of the SDRAMs and support components (excluding the SPD). Values for these voltages are 'operable' which means the device characteristics such as timing are supported at this voltage, or 'endurant' which means that the device may be powered to that voltage level without damage, however should not be used as operation is not guaranteed at the higher voltage.

ggggg eRxff PC3v-wwwwwm-aa-bb-ccd

Where:

- ggggg = Module total capacity, in bytes
256MB, 512MB, 1GB, 2GB, 4GB, etc.
- eR = Number of ranks of memory installed
1R = 1 rank of DDR3 SDRAM installed
2R = 2 ranks
4R = 4 ranks
- xff = Device organization (bit width) of DDR3 SDRAMs used on this assembly
x4 = x4 organization (4 DQ lines per SDRAM)
x8 = x8 organization
x16 = x16 organization
- v = SDRAM and support component supply voltage (VDD)
Blank = 1.5 V operable
L = 1.35 V operable, 1.5 V operable
U = 1.TBD V operable, 1.TBD V endurant
- wwwww = Module bandwidth in MB/s
6400 = 6.40 GB/s (DDR3-800 SDRAMs, 8 byte primary data bus)
8500 = 8.53 GB/s (DDR3-1066 SDRAMs, 8 byte primary data bus)
10600 = 10.66 GB/s (DDR3-1333 SDRAMs, 8 byte primary data bus)
12800 = 12.80 GB/s (DDR3-1600 SDRAMs, 8 byte primary data bus)
14900 = 14.93 GB/s (DDR3-1866 SDRAMs, 8 byte primary data bus)
17000 = 17.06 GB/s (DDR3-2133 SDRAMs, 8 byte primary data bus)
- m = Module Type
E = Unbuffered DIMM ("UDIMM"), with ECC (x72 bit module data bus)
F = Fully Buffered DIMM ("FB-DIMM")
L = Load Reduction DIMM ("LRDIMM")
M = Micro-DIMM
N = Mini-RDIMM
R = Registered DIMM ("RDIMM")
S = Small Outline DIMM ("SO-DIMM")
U = Unbuffered DIMM ("UDIMM"), no ECC (x64 bit module data bus)
- aa = DDR3 SDRAM CAS Latency in clocks at maximum operating frequency

Proposed

bb = JEDEC SPD Revision Encoding and Additions level used on this DIMM
cc = Reference design file used for this design (if applicable)
 A = Reference design for raw card 'A' is used for this assembly
 B = Reference design for raw card 'B' is used for this assembly
 AC = Reference design for raw card 'AC' is used for this assembly
 ZZ = None of the reference designs were used for this assembly
d = Revision number of the reference design used
 0 = Initial release
 1 = First revision
 2 = Second revision
 P = Pre-release or Engineering sample
 Z = To be used when field cc = ZZ

Examples:

2GB 2Rx4 PC3-10600R-7-10-D2

is a 2 GB DDR3 RDIMM using 2 ranks of x4 SDRAMs operational to DDR3-1333 performance with CAS Latency = 7 using JEDEC DDR3 SPD revision 1.0, raw card reference design file D revision 2 used for the assembly

1GB 1Rx4 PC3L-10600R-8-10-C1

is a 1 GB DDR3 RDIMM using 1 rank of x4 low voltage SDRAMs, operable at 1.35 V and 1.5 V operable, operational to DDR3-1333 performance with CAS Latency = 8 using JEDEC DDR3 SPD revision 1.0, raw card reference design file C revision 1 used for the assembly

1GB 2Rx8 PC3-12800E-10-10-BP

is a 2 GB DDR3 UDIMM with x72 data bus (ECC) using 2 ranks of x8 SDRAMs operational to DDR3-1600 performance with CAS Latency = 10 using JEDEC DDR3 SPD revision 1.0, raw card reference design file B pre-release revision used for the assembly

4GB 2Rx8 PC3-8500N-8-10-ZZZ

is a 4 GB DDR3 Mini-RDIMM using 2 ranks of x8 SDRAMs operational to DDR3-1066 performance with CAS Latency = 8 using JEDEC DDR3 SPD revision 1.0, no JEDEC standard raw card reference design file used for the assembly

Proposed

DIMM Mechanical Specifications

JEDEC has standardized detailed mechanical information for the 240Pin DIMM family. This material is included as reference and may be out of date. Download the latest version of MO-269 for any later updates. This information can be accessed on the worldwide web as follows:

1. Go to JEDEC official site; <http://www.jedec.org>.
2. Click on 'Free Standards' and enter the free download area.
3. Search by document number: 'MO-269' and download the PDF for this product family.
4. Or search by 'JEP95'; 'JEDEC Publication 95.' and open entire document, scroll down and select 'MO-269' to download the PDF for this product family.

Within MO-269, several DIMM thickness variations are defined. These variations are summarized in the table below, in conjunction with examples of the types of LRDIMM components and assemblies that may be associated with each DIMM thickness range:

Maximum LRDIMM Thickness	Comments
Less than or equal to 4.00 mm	Generally associated with DIMMs produced with devices that are 1.35 mm thick or less
> 4.00 mm and less than or equal to 6.75 mm	Generally associated with DIMMs produced with devices that are greater than 1.35 mm and less than or equal to 2.70 mm thick
> 6.75 mm and less than or equal to 7.55 mm	Generally associated with DIMMs produced with devices that are greater than 2.70 mm and less than or equal to 3.10 mm thick
> 7.55 mm	Intended to cover DIMMs produced with non-standard package thicknesses, card-on-card structures or alternate solutions

Proposed

Note: Maximum DIMM thickness can be a measured maximum value, or can be calculated using the maximum component, card, label, and assembly process adders.

Design File Naming Convention

“DIMM spec”_Vrrr_RC_LLn_YYYYMMDD.zip

Where:

DIMM spec = DIMM Specification
PC3-LRDIMM

V = Constant representing “Version”.

rrr = First revision of raw card Appendix at time of first ballot

RC = Constant representing “Raw Card”

LL = Raw Card letter(s)

n = Raw card registration number. Only to be incremented if the file is actually posted.

YYYYMMDD = Year, month and day of release if posted or last changes if under consideration.

Notes regarding release date:

1. Date will always reflect the date of the last change. Renaming of a file does not constitute a change.
2. If for example the BOM is updated, the BOM, readme and design (zip) files all receive new dates, but the brd file remains unchanged.

Notes regarding speed upgrades:

1. If for example a new BOM is needed to upgrade a design file that accomodates a new speed such as PC3-12800 then the BOM file may be named as follows:
“DIMMspec”_Vrrr_RC_LLn_YYYYMMDD_ **BOM-12800**.xls
2. BOMs may be changed or added to an existing design (zip) file without incrementing the raw card registration number. However, in this case the date designation of the design file would be incremented as shown in the following examples:

Example Filename: PC3-LRDIMM_V100_RC_B0_20080912.zip

Proposed

Revision Log

Revision Info	Page of Revision	Description of Change
Revision 0.10 20090916	ALL	Initial draft
Revision 0.11 20090930	9	Update pinout table from ballot
	11	Add table for pinout comparison between LRDIMM and RDIMM. Content of table requires review.
	17	Add QDP ballout table. Content of table requires review.
	23	Add x4 QDP Pad Array table. Content of table requires review.
	24, 25, 26	Add MB pin out table. Content of table requires review.
Revision 0.12 20091005 20091008	35	Add place holder for AVCC schematic.
	4	Added dimensions and variations to table
	11	Modified table to show only pins with differences
	12	Modified # of DRAM balls column from 72 to 82
	13-17	Change component densities in title from "512Mb to 8Gb" to "1Gb to 4Gb".
	18	Change "68-pad array" to "78 pad array"
	24-26	Updated pin assignment table
	31	Update densities in title of Net Structure Example
	35	Update schematic for AVCC
	37	Update densities in label format
	5	Removed 128 GB
Revision 0.13 20091010	10	Updated table to reflect comparing UDIMM with LRDIMM.
	12	Removed RC K entry
Revision 0.13 20091010	38	Add Data Bus Wiring Requirements
	10	Additional changes to table comparing UDIMM to LRDIMM.
Revision 0.14 20091030	10, 11, 30, 40	Corrected typos and references
	TOC, 12	Added information for RC K
	38, 39	DIMM label updated based on latest spec with hyphen removed for LRDIMM
	36	DIMM wiring requirements updated.
Revision 0.15 20091104	6,8,9,30	Changed Err_Out_n to ErrOut_n
	4	Adjusted wording for address mirroring
	30	Chnaged placement of brackets [] in signal names
	36	Corrected table for Gold finger to Memory buffer mapping
	36	Changed text regarding required wiring of QVREF_DQ
	36	Change 22 Ohms to TBD Ohms
Revision 0.16 20091104	36/37	Changed description of VTT connection to be more clear.
	4	Adjusted wording related to ODT1
	29	Incorporated latest SPD pinout, text and figure
	30	Added figure for VREFDQ and VREFCA. Adjusted wording for VREFCA and VREFDQ.
Revision 0.16 20091104	30/31	Removed text discussing VTT connections.
Revision 0.16 20091104		
Revision 0.16 20091104		

Proposed

Revision Info	Page of Revision	Description of Change

Proposed

Exhibit E



Committee Letter Ballot
JC-45.4-09-321
Item 2192.44
Distributed: 16 Nov 2009
Expiring: 07 Dec 2009



SPONSOR: Avant Technology Inc., represented by Paul Goodwin,
paul_goodwin@avanttechnology.com, (512) 719-6303 413

DISTRIBUTION: Formal Vote: JC-454
Non voting committees: JC-45 (Information and Comments)

Eng. No.: AS 90578

Item No.: 2192.44

SUBJECT: [DDR3 LRDIMM Design Specification Body](#)

BACKGROUND: At the September 2009 Committee meeting the DDR3 LRDIMM TG was given authorization for 1 or more ballots on the LRDIMM Design Specification body and Appendices.
The following LRDIMM Design Specification has Change bars and Highlighted text however the entire specification is being balloted. The change bars and Highlighted areas are difference from the RDIMM specification.

PATENTS: No known patent issues on the sponsor's part

ATTACHMENT: [Download HB09321-.pdf](#)

KEYWORDS: LRDIMM, DIMM, DDR3, MB, Memory Buffer, DRAM, SDRAM, Design, Specification

[\[Top\]](#)



Exhibit F

Tally of Votes



Committee Letter Ballot
JC-45.4-09-321
2192.44



Tally Date: Wed, December 09, 2009 at 16:40:13
 (US Eastern Time)

Ballot distributed: 16 Nov 2009

Expiration date: 07 Dec 2009

Sponsor: Avant Technology L.P. Mr. Paul Goodwin Email: paul_goodwin@avanttechnology.com Phone: 512-719-6303

Subject: DDR3 LRDIMM Design Specification Body

Attachment: [HB09321-.pdf](#)

PATENTS: No known patent issues on the sponsor's part

Summary:

17 Yes

5 Abstention

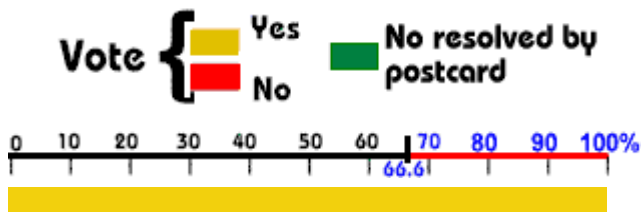
22 companies voted (including abstention)

Non voting companies are not tallied,
and are not considered to abstain.

Attention: Percentages are rounded.

Abstentions are excluded from percentage calculation.

Only Yes votes (ballot may pass by acclamation)



Company / voter	Y	N	A	P	C	PC	DoV	DoR
22 companies voted	17	0	5	1	6Y		22	
Advanced Micro Devices Inc. Patel	<u>Y</u>				<u>X</u>	N/A	12/03/09	
Buffalo Inc. Tsukada	Y						11/17/09	
Cray Inc. Grossmeier	Y						11/16/09	
Elpida Memory Incorporated Ono	<u>Y</u>				<u>X</u>	N/A	11/26/09	
FormFactor Inc. Gervasi	<u>Y</u>				<u>X</u>	N/A	12/02/09	
Hynix Semiconductor im	Y						12/02/09	
I-O Data Device Inc. Miyagoshi			A				12/01/09	
IBM Corporation ilmer	Y						11/25/09	
Inphi Corporation Washkewicz	<u>Y</u>				<u>X</u>	N/A	12/02/09	
Inphi Corporation Raghavan	Y						12/02/09	

Integrated Device Technology Inc. Franklin	Y						12/02/09	
Intel Corporation Mrdjan	Y						11/30/09	
Kingston Technology Company Inc. Cheng	Y						11/23/09	
Legacy Electronics Inc. Mecker			A				12/01/09	
Micron Technology Inc. Graham	Y						11/30/09	
Nanya Technology Corporation Linder	Y				X	N/A	12/02/09	
Netlist Inc. Martinez			A	P			12/01/09	
Nvidia Corporation Wagner			A				12/01/09	
PNY Technologies Inc. Socci	Y						12/02/09	
Samsung Semiconductor Park	Y				X	N/A	12/02/09	
Sun Microsystems Inc. Jeffrey	Y						12/01/09	
Tyco Electronics Corporation Leidy			A				11/19/09	
* Y ☐ Yes, N ☐ No, A ☐ Abstain, P ☐ Patent(s), C ☐ Comments PC: Postcard, Y ☐ approved response, N ☐ did not approve response, N/A: not available, sponsor and / or voter did not respond, DoV: Date of Vote								

Advanced Micro Devices Inc. represented by Sam Patel, email: sam.patel@amd.com voted ☐ **Approve content with comments** on 12/03/09

Comments: Would like to see CS, C_E and ODT routing for all configuration documented in this body of the lrdimm spec.

[Respond to original comments](#) Sponsor, please submit your response to voter.

[\[Top\]](#) [\[Summary table\]](#)

Elpida Memory Incorporated represented by Takao Ono, email: t.ono.gz@elpida.com voted ☐ **Approve content with comments** on 11/26/09

Comments: page 26-27, How should the QAECC2,6,9 be treated ☐ Changing to NC or RFU ☐
 page 35 AVCC should be changed to AVDD,
 page 36 one of QVREFDQ should be changed to QVREFCA

[Respond to original comments](#) Sponsor, please submit your response to voter.

[\[Top\]](#) [\[Summary table\]](#)

FormFactor Inc. represented by Bill Gervasi, email: bilge@discobolusdesigns.com voted ☐ **Approve content with comments** on 12/02/09

Comments: pg 1: andd should be and

pg 1: configureable should be configurable

[Respond to original comments](#) Sponsor, please submit your response to voter.

[\[Top\]](#) [\[Summary table\]](#)

Inphi Corporation represented by Paul Washkewicz, email: pwashkewicz@inphi-corp.com voted ☐ **Approve content with comments** ☐ on 12/02/09

Comments: Inphi approves material in red text.

[Respond to original comments](#) Sponsor, please submit your response to voter.

[\[Top\]](#) [\[Summary table\]](#)

Nanya Technology Corporation represented by Peter Linder, email: jedec@tx.nanya.com voted ☐ **Approve content with comments** ☐ on 12/02/09

Comments: Suggest to change Raw-Card-C to 11x12mm dram pkg to match the other raw cards as discussed in TG

[Respond to original comments](#) Sponsor, please submit your response to voter.

[\[Top\]](#) [\[Summary table\]](#)

Netlist Inc. represented by Mario Martinez, email: mmartinez@netlist.com voted ☐ **Abstain from voting** ☐ on 12/01/09

Comments:

[Respond to original comments](#) Sponsor, please submit your response to voter.

PATENT ISSUE:
Netlist may have IP that applies to this ballot

[\[Top\]](#) [\[Summary table\]](#)

Samsung Semiconductor represented by Sung Joo Park, email: sjoo@sec.samsung.com voted ☐ **Approve content with comments** ☐ on 12/02/09

Comments: Table of contents should be updated. And Max DRAM size of the Raw Card C (on page13) is 11.0 x 12.0.

[Respond to original comments](#) Sponsor, please submit your response to voter.

[\[Top\]](#) [\[Summary table\]](#)

End of Web Report

EXTRA OPTIONS:



Text file ready to import
in a spreadsheet



email tally to voting committee



Add vote, on your honor

PLEASE BE VERY PATIENT. Processing any of above query takes well over one minute.



Return to the main voting page

Exhibit G

MB Initialization sequence

Item 142.35

6-4-09



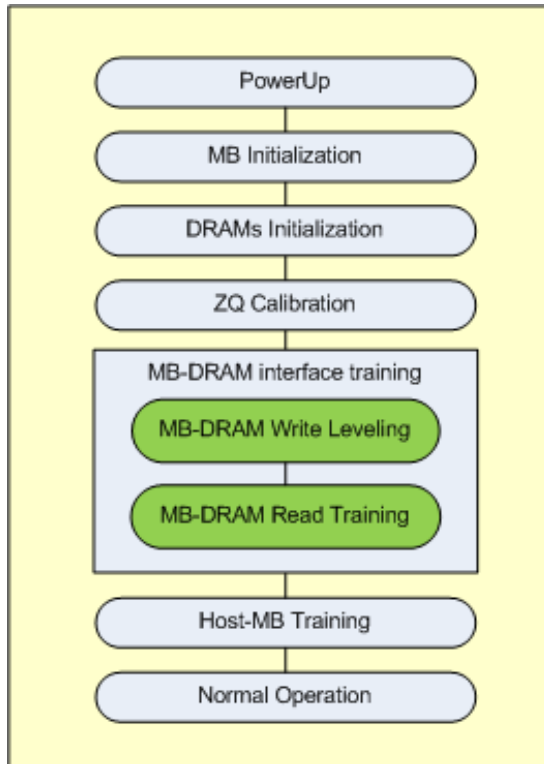
Where Semiconductor Leaders Set
Standards for the World!



Think fast.

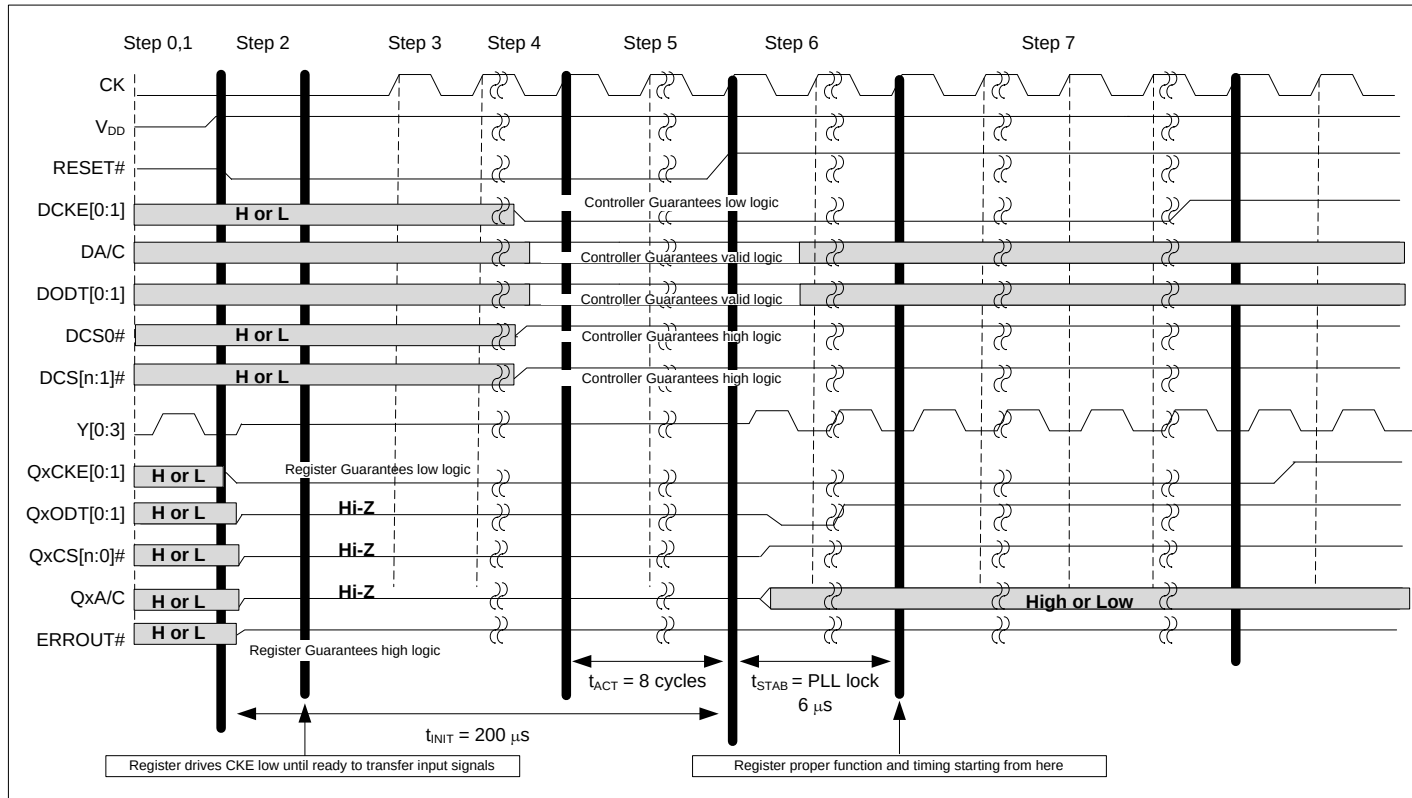
Samsung Electronics Co., Ltd.
Ex. 1050, p. 99

Initialization Overview



1. Power up requirements same as 882
2. Host initializes MB CWords
3. Host initializes DRAM MRS registers
4. Host issues ZQ command to DRAM
5. Host issues CWord write to start MB-DRAM interface training
6. Host does interface training
7. Normal Operation

MB Power Up Timing



MB Power Up Table

Step	#	power	input								Outputs						
			RESET #	Vref	DCK	DCKE	DCS#	DCMD	DQ/S	DODT	QxCKE	QxCK	QxCS	QxODT	QxCMD	ERROUT #	MDQ/S
No Power	0	0	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	Z	Z	Z	Z	Z	Z	Z
Power Ramp	1	0->V _{DD}	X or Z	X or Z	L	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z
Power Adjust	2	V _{DD} 1.5→1.35 1.35→1.5	L	X or Z	L	X or Z	X or Z	X or Z	X or Z	X or Z	L	Z	Z	Z	Z	H	Z
Clock start	3	V _{DD}	L	X or Z	running	X or Z	X or Z	X or Z	Z	L	L	Z	Z	Z	Z	H	Z
Drive CKE/CS	4	V _{DD}	L	X or Z	running	L	H	X or Z	Z	L	L	Z	Z	Z	Z	H	Z
Apply Vref	5	V _{DD}	L	stable	running	L	H	X or Z	Z	L	L	Z	Z	Z	Z	H	Z
Reset release	6	V _{DD}	H	stable	running	L	H	X or Z	Z	L	L	running	H	L	X	H	Z
Normal operation	7	V _{DD}	H	stable	running	X	X	X	X or Z	X	X	running	X	X	X	X	X or Z

- ❖ Power up sequence is same as 882 device
 - ❖ MB internal circuit calibration is done within the tSTAB time
- ❖ MB doesn't forward DODT as 882, instead the QxODT is initiated by MB depending on the CMD and QxODT configuration

Host RCW to Configure MB

- ❖ Frequency and Voltage RCW to be programmed first
- ❖ No specific ordering requirements for the rest
 - ❖ Address Splitting Mode
 - ❖ Number Input Ranks and Output Ranks
 - ❖ CKE, DODT Modes
 - ❖ Mirroring Mode
 - ❖ QxODT values per rank.
 - ❖ MRS RTT Values
 - ❖ MRS Masking
- ❖ Each of these items has been specified in JEDEC TG showings

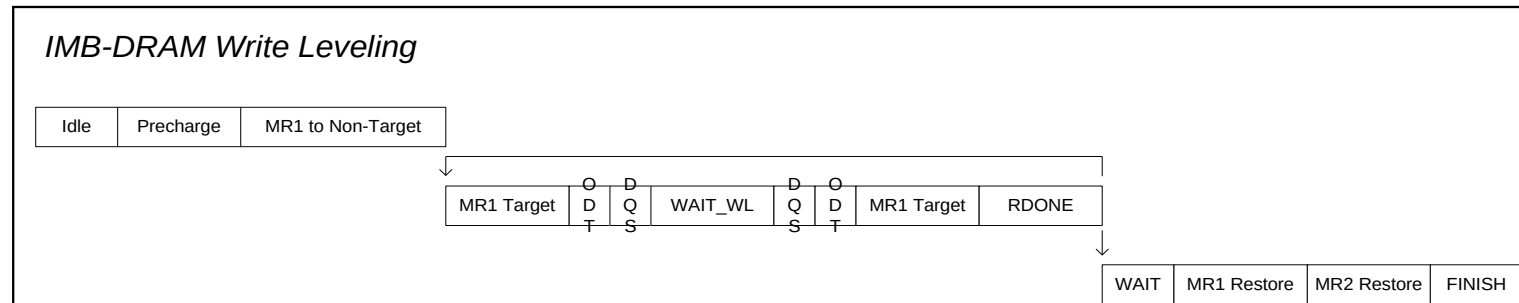
Host MRS to Configure DRAM

- ❖ Host issues ZQ commands to DRAMs
 - ❖ MB doesn't intercept nor response to ZQ command
 - ❖ ZQ command is forward to DRAMs
- ❖ Host issues MRS commands
 - ❖ MRS command is forward to DRAMs

MB-DRAM interface training

- ❖ Host writes CWord, F0RC12, to start the IMB-DRAM training and wait ...
- ❖ MB does write leveling to DRAM
- ❖ MB does RxEn training to DRAM
- ❖ MB return to idle state and ready to start normal operation

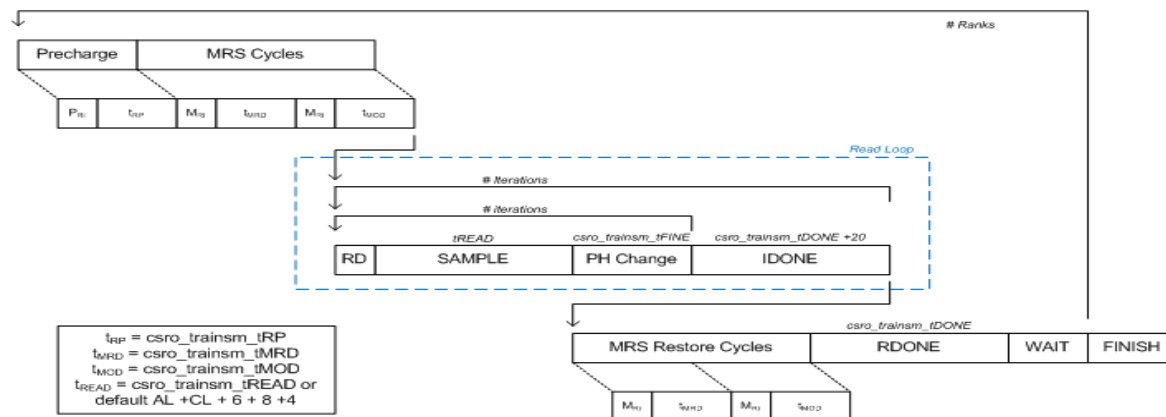
MB-DRAM Write Level Steps



- ❖ Set MR1 for non-target ranks to disable the output drivers.
- ❖ Write Level for Target Rank per DRAM spec
 1. Set MR1 A7 to 1 for target rank to enable Write Leveling
 2. Send DESELECT/NOP during Write Leveling.
 3. MB waits and assert QODT[x] for that rank.
 4. After X nCK MB generates MDQS
 5. After Y nCK, MB samples MDQ inputs.
 6. MB steps through all phases for optimal MDQS phase.
- ❖ Repeat the write level process for each physical rank.

MB-DRAM RxEn Training Steps

IMB-DRAM Read Training



- ❖ Send PREA to the physical rank under training.
- ❖ Enable DRAM to provide data to buffer
- ❖ RxEn Training Iterations
- ❖ Repeat for each physical rank defined by number of physical rank register.

MB-DRAM Complete Training Time

- ❖ After enabling the IMB-DRAM training by setting F0RC12 to 010b, the Host must wait a predetermined number of cycles before moving to next step
- ❖ $\text{Number Cycles} = \text{WL Training Time} + \text{Read Training Time}$

Host-MB Training

❖ Write Level

- MB masks Host issued DRAM WL command
- Host enables Host-MB WL by writing to MB
- MB WL Timing same as DRAM

Exhibit H

Minutes of Meeting No. 158
JC-40 Digital Logic Committee

June 4, 2009

Montreal, Canada

<u>Members Present</u>	<u>Company</u>	<u>Telephone</u>	<u>E-mail</u>
John Smolka, Chairman	Silego Technology	408-466-0412	jsmolka@silego.com
Mark Kellogg, Secretary	JEDEC Consultant	(c) 585-455-3545	mkellogg@kcdservices.com
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Paul Goodwin	Avant Technology L.P.	512-719-6303	paul_goodwin@avanttechnology.com
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Howard Sussman	Sanyo Semiconductor Corporation	978-562-9660	sanyo.hs@ix.netcom.com

Minutes of Meeting No. 158
JC-40 Digital Logic Committee

June 4, 2009

Montreal, Canada

Jeffrey Chung	Silego Technology	408-327-8807	jchung@silego.com
Kelvin Marino	Smart Modular Technologies, Inc.	949-788-3833	kelvin.marino@smartm.com
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Ricki Williams	Sun Microsystems Inc.	858-876-3042	ricki.williams@sun.com
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1.0 JC-40 Digital Logic Plenary

The JC-40 Plenary meeting opened at 8:00 AM on June 4, 2009. Mr. Smolka led the discussion of this group.

Self-introductions were completed by the attendees.

1.1.0 Patent Policy

The patent policy was reviewed.

Netlist indicated that they would be making disclosures during the meeting related to JC-40 efforts, and asked if JC-40 was maintaining an IP Tracking list. Response: Mr. Smolka indicated that he would be making a presentation during JC-40.4 (Memory Buffer TG) which includes an IP Tracking List. He further indicated that the list is being updated to reflect recent letters sent from the JEDEC office.

Discussion:

- A discussion ensued between one or more members and committee chairmen regarding whether a disclosure need be made during each presentation – especially if the material is related to related material made earlier and/or if the disclosure is included on the IP Tracking list. Mr. Kellogg indicated that he would discuss this question with Mr. Kelly for clarification, and respond back to the committee. He further indicated that repeated disclosing of IP (disclosing the same IP for each related showing) is and should not be a concern to the membership, although this may slow meeting progress.
- A chairman clarified the member disclosure requirements, as summarized in the JC-40 agenda, JC-42 agenda, etc.

Mr. Martinez disclosed that Netlist may have IP on the ballot related to item #142.11, in addition to other possible showings.

Discussion:

- A chairman indicated that disclosures should be made in a timely manner
- prior to the ballot counting whenever possible.

1.2.0 Minutes

A motion was made by Samsung and seconded by Montage to accept the minutes of the February 2009 as written.

Discussion:

**Minutes of Meeting No. 158
JC-40 Digital Logic Committee**

June 4, 2009

Montreal, Canada

- Mr. Martinez proposed an amendment to the motion to make a change to page 11 of 19 in the published meeting minutes, including a verbal disclosure that Netlist has IP related to item #142.11.

Mr. Kellogg reviewed the February preliminary and published minutes and did not find a statement from Netlist during the discussion on item #142.11. He then indicated that the minutes for JEDEC meetings reflect the discussions held during the meeting – changes and/or additions to the minutes should be proposed if the minutes do not correctly reflect the discussions that took place during the meeting. He asked Mr. Martinez, as well as the committee, if they could recall the disclosure being made during discussions on that item in the meeting in question, with no response.

The proposed amendment was not approved by the original first and second to the motion.

The motion was dropped.

Motion by Netlist and seconded by Montage to approve the meeting minutes as written.

The motion passed by acclamation.

1.3.0 Agenda

The agenda was reviewed.

Mr. Smolka covered several topics from the agenda material, including:

- The new member's lunch takes place on Wednesdays approximately at noon – Charles Furnweger is the focal point for the luncheon.

- The JC-40 policies were reviewed, as included in the meeting minutes.

Mr. Smolka indicated that the committee has authorized a ballot on the policies in the February meeting, as item #150.00, with no ballot issued.

Motion by Silego and seconded by TI to re-authorize the PLL/Register TG to issue one or more ballots on the JC-40 policies, as described in the JC-40 agenda material uploaded on the JEDEC server.

Discussion:

- To update policies in the future (after balloting them), members were asked to make a first and second showing (per the policies) and ballot the changes for which a motion is passed to do so.

- The purpose of balloting the policies is to ensure each committee clearly

discloses and ballots their policies for publication in JM21 such that they are well understood, with any modifications taking place using a conventional balloting process.

The motion passed by acclamation.

Mr. Gervasi summarized the JEDECworks website (the presentation was made available on the server). TGs were asked to utilize this new website.

1.4.0 BoD Ballot Review

- Committee item #104.00B (JCB-09-40, DDR3/DDR3L SSTE32882 Register) passed BoD during the current quarter.

1.5.0 BoD Update

Mr. Quddus summarized key BoD and JEDEC activities over the past quarter, with this information posted on the local server. Some key points of his presentation (previously shown in the JC-16/42/45/64 Plenary meeting) included:

- The three Flash Summits held in the first quarter of 2009 were summarized. Mr. Quddus indicated that there was significant interest in the topics covered, as well as good attendance - especially in the Far East meetings.
- An LPDDR2 Workshop is planned for June 25th in Santa Clara, relating to the recent publication of the LPDDR2 standard by JEDEC. Mr. Quddus highlighted the extensive press coverage on the new standard.
- JEDEC efforts in China and Taiwan were summarized.
- New BoD members were identified, including Sean Fan (IDT) and Dinesh Maheshwari (Cypress).
- An updated copy of the JEDEC meeting location policy was shown – with discussion delayed until later in the meeting.
- An MOU was signed between JEDEC and SFF (Small Form Factor). Work is underway regarding an MOU with SNIA (to be discussed in August).
- The JEDEC marketing report was reviewed.
- The JEDEC website activities were reviewed.

1.6.0 Ballot Review

There were no ballots for review in this committee.

**Minutes of Meeting No. 158
JC-40 Digital Logic Committee**

June 4, 2009

Montreal, Canada

2.0 JC-40.1 CMOS/BiCMOS Digital Logic

The JC-40.1 meeting opened at 8:32 AM on June 4, 2009. Mr. Williams led the discussion of this group.

2.1.0 Agenda

The agenda was reviewed.

2.2.0 Ballot Review

There were no ballots for review in this sub-committee.

2.3.0 Second Presentations

There were no second presentations in this sub-committee.

2.4.0 First Presentations

There were no first presentations in this sub-committee.

2.5.0 Task Group Update

2.5.1.0 #121.00 TG	JEDEC Instrumentation Chip Status
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The TG logistics were shown, with calls occurring on select Thursdays at 4:30 PM (PST). The TG is comprised of 15 member companies, with 6 members generally participating. Other committee members were asked to attend if interested in this topic.

Recent topics covered in the TG included discussions with two possible silicon vendors, in addition to work on updates to resolve known “holes” in the specification related to such items as the I2C command table, the block diagram and updates to the pin count and ballout.

Activities planned for the next quarter are related to the completion of updates to the device specification – with plans to show the presentation at the 3Q '2009 meeting.

Discussion:

- Has the SMBus been considered as an interface bus rather than the I2C bus? Response: the TG can consider this option.
- A comment was made that the SMBus is quite different than the I2C bus, running slower than the I2C bus. Making this change would be a significant modification to the design.
- A suggestion was made to ask Intel to bring the SMBus into JEDEC. A suggestion was made to ask the JEDEC office to draft a letter to Intel requesting that they bring the SMBus to JEDEC for standardization.
- Intel commented that it is not their specification.
- The suggestion was modified to ask the JEDEC office to draft a letter to the SMBus organization to ask that they make a JEDEC showing and consider standardization. It was further suggested that a letter be sent to NXP in regard to the I2C specification. NXP rep indicated that they already have sent a letter to JEDEC on I2C.

Secr. note: No I2C letter was located at the JEDEC office by the time the minutes were approved by Mr. Kelly. A follow-up will be required on this item.

Mr. Smolka agreed to work with Mr. Williams and the JEDEC office to request that the SMBus be brought to JEDEC for possible standardization.

3.0 JC-40.3 RDIMM Support Devices

The JC-40.3 meeting opened at 8:39 AM on June 4, 2009. Mr. Ammar led the discussion of this group.

3.1.0 Agenda

The agenda was reviewed and updated.

3.2.0 BoD Ballot Review

Mr. Ammar indicated that the sub-committee BoD ballot was covered in the JC-40 Plenary.

3.3.0 Ballot Review

**3.3.1.0 #104.64 JC-40.3-09-79 DDR3/DDR3L SSTE32882 Co
Parameter Update**

The vote count was 18 yes, 0 no and 7 abstentions.

Yes comments:

- Intel: A design target for Co is still needed. Intel recommended that the TG continue to work on this and authorize a ballot.

Motion by Intel and seconded by Montage to re-visit the Co spec and authorize the TG to issue a ballot on the material.

The motion passed by acclamation.

The ballot was left on pass/hold.

**3.3.2.0 #104.63 JC-40.3-09-80 DDR3 Register (SSTE32882) –
Output Slew Update**

The vote count was 11 yes, 2 no and 6 abstentions.

No Votes:

- Inphi: Note 1 should include all the drive strength settings. Inphi indicated that they agreed with Silego's comments as discussed in the May 27th TG call. Inphi indicated that their comment was addressed.
- Smart Modular: The change in the slew rate definition changes the ring-back characteristics of the modules, which will require module manufacturers to re-characterize RTT values for modules currently qualified and in production. Smart Modular indicated that their "no" vote was addressed.

Yes comments:

- IDT: Output CL test loads should be adjusted for moderate and strong settings.
- Silego: Silego made a showing (item #104.70), including the following comments (see the showing for more details):
 - An inconsistency in the specification was reviewed, with a proposed editorial change which had been agreed upon by the TG.
 - Note 1 on table 2 says "measured into test load at default register setting". The default setting results in light drive - still need to measure at moderate and strong. Silego proposed to change the note to add "except for RC3, RC4 and RC5 which are set according to the drive strength to be

measured.”

Motion by Silego and seconded by Inphi to editorially modify the SSTE32882 specification (not yet published) to editorially add the text for note 1 (slide 6 of their presentation), and to include the editorially modified text proposed by Silego in the current specification revision prior to publication.

The motion passed by acclamation.

3.3.3.0 #104.65 JC-40.3-09-85 SSTE32882 IDD and IID Max Limits

The vote count was 12 yes, 0 no and 7 abstentions.

Yes comments:

- Inphi: Add clarification to the meaning of “IBT off”, such as “RC8 = x111” as discussed in the TG. Response: This is already addressed in errata comments to be included in the current spec revision prior to publication.

Inphi indicated that their comment was addressed.

The ballot material was left on pass/hold.

3.3.4.0 #104.00B JC-40.4-06-208B DDR3/DDR3L SSTE32882 Register

The vote count was 10 yes, 0 no and 1 abstentions.

Yes Votes:

- Elpida: Yn and Yn# need to be swapped as an editorial change.
- Smart Modular: Table 24 should include the strong drive option since most vendors support this feature. Response: Being discussed in TG, will await feedback from TG.

Mr. Smolka indicated that the ballot was a fast track ballot, was sent to BoD and passed BoD voting (as previously reported).

All comments were addressed prior to issuing the BoD ballot.

3.4.0 Second Presentations

3.4.1.0 #153.01 Silego

DDR3 SSTE32882 for DDR3U 1.25V Applications

A marked-up DDR3 SSTE32882 specification was shown to include 1.25V support. Silego indicated that the specification is a draft document – the specification values need to be discussed in the TG. Other possible changes were verbally summarized.

Discussion:

- In response to a question, Silego indicated that the values in the specification include both estimates and copy/paste values. The specification is intended as a template for the final specification.

Motion by Silego and seconded by HP to authorize the PLL/Reg TG to work on the specification proposal and to issue one or more ballots on the specification.

Discussion items included the following:

- A question was asked as to whether the showing was a second showing. Response: Related item number #137.00 was previously shown by HP – this showing is intended to build on that material.
- A concern was raised that the material has not yet been discussed in the TG. Response: This is not a committee requirement.
- Are there any functional changes? Response: Expect that changes will relate to values, not functions.
- Do the values change from the 1.5V spec? Response: Driver strength is expected to remain the same.
- No simulation data has been completed in the RDIMM TG – this information is required prior to ballot authorization to determine if the proposal will meet the application requirements. Response: Let the TG work on the details and if a consensus is achieved, issue a ballot on the material.
- This is a template, built on a specification already completed and standardized by the committee.
- AMD indicated that they have completed extensive simulations but not yet shown results in the TG – the results can be shown if needed.

The motion passed by acclamation.

3.4.2.0 #137.00 HP

DDR3U Ultra Low Voltage Memory

The sponsors of the material was shown – including nine member companies. HP indicated that the material was shown earlier in the week (in JC-42 and JC-45). A special TG was previously formed, sponsored by AMD, to define the modules affected by 1.25V.

The proposed standardization of 1.25V is due to requests from customers to reduce power. Memory now represents 40% of power consumed in systems, with the memory percentage increasing.

With the expected DDR4 standardization and broad adoption schedule, there is too long of a gap from 1.5 and 1.35V memory devices to DDR4. A 1.25V transition device is needed. The current proposal is for a part that has a nominal voltage of 1.25V and is 1.35V tolerant (this topic will be discussed in the TG). The proposal is scaled from 1.35V, with proposed bus speeds of 800 – 1333 Mb/s.

Discussion:

- It would be good to see DRAM producers as sponsors as well.

3.4.3.0 #104.69 Silago

**DDR3 RCD/RDIMM tQsk
Consideration**

Silago indicated that the material was previously shown in the JC-45 RDIMM committee, with authorization to ballot in that committee. Additional work is required in this committee.

With the measurement procedure defined for tQsk, it is time to fine-tune the DDR3 RCD spec, which assumes ideal output clock. The Intent is not to make technical changes but to make changes that may be considered as editorial or close to that.

Table 38 of the current register specification was shown – output clock jitter not included in the tQsk specifications. Table 65 (Note b) of the DRAM specification was then shown. Every instantaneous setup and/or hold should satisfy the DRAM input specification values.

The table “Example of DDR3 Timing Budget for Post Register...” timing budget was then shown with areas of concern highlighted in red (relating to jitter).

Concerns included:

- There is a need for addition of tjit(hper) in the RDIMM timing budget.

- The current approach in the RDIMM specification does not appropriately account for the jitter.
- The specification is unclear in regard to a $\frac{3}{4}$ pre-launch case.

A copy of the consensus from validation TG was shown for tQsk. It was noted that the "Measurement procedure includes output clock jitter". Recommended specification changes were reviewed for the DDR3 RCD specification, followed by the proposed RDIMM specification changes and the proposed changes to table 38 of the buffer specification. A future JEP specification will emerge from the validation TG. Silago indicated that there is no impact on the DIMM timings – this is just a different means of specifying the timings.

Discussion:

- A question was asked in regard to correlation between clock jitter and input jitter. Response: Because there is no input specification, devices will tend to meet the output specification.

Motion by Silago and seconded by Micron to authorize the TG to issue a ballot on tQsk modifications as suggested by the presentation.

Discussion:

- As clarification, Silago indicated that the Intention is that the PLL/Register TG will discuss the material and issue a ballot if a consensus is reached.

The motion passed by acclamation.

3.4.4.0 #104.68 Inphi

DDR3 Register SSTE32882 IBT Parameter Definition

The presentation was intended to clarify the IBT parameter. A new defined parameter to replace the mismatch tolerance parameter was proposed to make it easier to measure the mismatch on test equipment (automated and bench). The showing was in ballot form.

A modified version of table 37 in the SSTE32882 specification was shown, including the new parameter, applicable notes and a figure. The TG has considered this proposal.

Motion by Inphi and seconded by TI to authorize the TG to issue a ballot on this material.

The motion passed by acclamation.

3.4.5.0 #104.56A Intel

**CKE Power-Down Mode Footnote
Update**

Intel made a proposal to change the register CKE power down mode footnote – with the existing and proposed text reviewed. Associated timing diagrams were shown with the modified footnote.

Motion by Intel and seconded by Montage to authorize this re-ballot including the proposed modifications as shown.
The motion passed by acclamation.

3.5.0 First Presentations

There were no first presentations in this sub-committee.

3.6.0 Task Group Update

3.6.1.0 #122.00 TG

PLL/Reg TG Status Update

The TG logistics were shown, with calls held every Wednesday. The TG is now utilizing the JEDECworks website.

TG activities since the last committee meeting were summarized, including compilation of an updated specification revision (on server), discussions and ballots on Co, output slew rates and IDD/IID, discussions related to the IBT tolerance measurement and consideration of a new register package (8.5 mm x 11.0 mm).

Consensus votes were reviewed, primarily related to the TG activities previously summarized. A list of proposed editorial changes to the DDR3 SSTE32882 specification were then reviewed, as delineated on page 5 of the presentation, including:

- Correct the narrow package row “Y” name in tables 7, 8, 9 and 10 from “W” to “Y”
- Swap Yn# and Yn in figure 25
- Add RC8=x111, turning off all IBTs, to the IDD static operating current for clarification.
- Note 2 table 33: Need to add DCAS# to the list
- Change “J11” ball assignment name in table 6, page 23, from QABA2 to “QBBA2”

Ballot results were shown for this meeting. Future discussion topics were

then summarized; including DDR3 slew rate measurement, tQSKx clarification, Co specification discussion, DDR3 1866/2133 specification discussion, DDR3 1.2V discussion and DDR4 specifications.

Motion by Silego and seconded by Montage to authorize the TG to arrange and clean up fonts and tables and include the proposed editorial changes listed on page 5 of the presentation in the DDR3 pass/hold spec as editorial changes and to include them in the specification that has passed the BoD prior to publication of that specification if a 100% consensus vote is achieved that the changes are editorial.
The motion passed by acclamation.

Motion by Silego and seconded by Montage to authorize the TG to issue one or more ballots on the DDR3 and DDR3L register specification operating at 1866.
The motion passed by acclamation.

4.0 JC-40.4 FBDIMM Support Devices

The JC-40.4 meeting opened at 10:06 AM on June 4, 2009. Mr. Chung led the discussion of this group.

4.1.0 Agenda

The agenda was reviewed and updated.

4.2.0 Ballot Review

4.2.1.0 #142.24 JC-40.4-09-118 DDR3 Memory Single Buffer Ballout 0.65mm Pitch

Secr. note: A prior version of this material was balloted under item #142.14. This material is a re-ballot of that material.

The vote count was 16 yes, 1 no and 5 abstentions.

No votes:

- IDT: 8 DCS inputs are needed, 4 QODT pins are missing on the A and B sides, Test [2:0] should be defined as I/O, Aout should be defined as I/O, SMBus need not be on outer edge of pinout, corner pins should not be

**Minutes of Meeting No. 158
JC-40 Digital Logic Committee**

June 4, 2009

Montreal, Canada

populated with pins, etc.

IDT indicated that they would be making a presentation in relation to their comment. IDT asked to have the ballot taken back to the TG for re-ballot.

Yes comments:

- Elpida: Need to consider 8 DCS inputs.
- IBM: IBM requires 8 DCS inputs (was "no" vote, changed to "yes" vote on voting machine based on sponsor indicating support for 8 DCS pins). IBM concurred that they accepted the response and their vote is now included as a "Yes" in the tally.
- Micron: Reverse the order of A-AV (numbering appears to be backward relative to JEDEC convention).
Micron indicated that their comment is incorrect, indicating that their comment is addressed.

Motion by IDT and second by Montage to send the ballot back to the TG and authorize the TG to re-ballot the material considering all voting comments and including 4 additional DCS inputs.

Discussion:

- IP Disclosure: Netlist indicated they have IP that may read on this material. Patent numbers were identified as 7532537 and 7289386.
- The sponsor indicated that their objective is to place the current ballot material on pass/hold, understanding that changes may occur.
- What is the benefit to leave on pass/hold as is if "no vote" comments have not been addressed? Response: By leaving on pass/hold, the current material provides some guidance to designers, albeit at some risk.
- A concern was raised in regard to making the addition of 4 DCS pins as an editorial change. Response: IBM indicated that they would be OK with enabling the TG to add the addition 4 chip selects as an editorial change.

Discussion continued regarding whether the 4 DCS addition is editorial as well as the rationale for leaving the ballot on pass/hold while authorizing the committee to do further work on the ballot.

The motion failed with a vote count of 5 against and 6 in favor.

Motion by Inphi and seconded by FormFactor to leave the ballot on pass/hold and authorize the TG to consider all comments and issue a re-ballot on this material.

The motion passed by acclamation.

4.2.2.0 #142.05A JC40.4-09-44A

**DDR3 LRDIMM Memory Twin
Buffer Ballout**

The vote count was 4 yes, 6 no and 11 abstentions.

The ballot failed by count. The voting results were quickly reviewed to determine if any feedback was included that was not already under consideration.

No votes:

- AMD: Single buffer consensus achieved.
- FormFactor: Single buffer is now the TG consensus.
- IBM: Require 4 additional chip selects.
- Inphi: The ballot has errors - several of which were listed in the voting response.
- Intel: Prefer single buffer.
- Samsung: The TG has agreed to a single buffer solution.

Discussion:

- Who decided on a single buffer? Response: The determination was made in the LR-DIMM TG by consensus. The TG information was reviewed in the JC-45 committee meeting.
- A comment was made that the JC-40/JC-45 committees did not make the determination to use single buffer. Response: Mr. Kellogg indicated that JC-40 can elect to standardize products not requested by a specific JEDEC committee.

IP Disclosure: Netlist indicated they have IP that may read on this material. Patent numbers were identified as 7532537 and 7289386.

4.2.3.0 #142.23 JC-40.4-09-110

**DDR3 MB Control Word Update –
CKE and ODT**

The vote count was 14 yes, 0 no and 6 abstentions.

Yes comments:

- Intel: Should clarify that “disabled” means that the outputs are Hi-Z (footnote #1). Response: The proposed change was accepted as an editorial change.
- Silego: Add two “reserved” rows for DBA1=0 and 1.

IP Disclosure: Netlist indicated they have IP that may read on this material. Patent numbers were identified as 7532537 and 7289386.

Motion by IBM and seconded by Samsung to place the ballot material on pass/hold with the editorial changes defined in the voting comments by Intel and Silego, awaiting completion of the specification and sending the complete specification to the BoD.

The motion passed by acclamation.

4.2.4.0 #142.25 JC-40.4-09-127

**DDR3 MB FORC15 Rank
Multiplication Control Word**

The vote count was 15 yes, 0 no and 4 abstentions.

Yes comments:

- Hynix: Subject is in error. Response: Initially was incorrect but was later fixed. Ballot content was correct.
- Silego: Several typos were identified. Response: Accepted as editorial.

IP Disclosure: Netlist indicated they have IP that may read on this material. Patent numbers were identified as 7532537 and 7289386.

Discussion:

- Still using “#” signal for low active signals. Recommend changing this by using “_” to delineate low active signals.

Motion by AMD and seconded by Silego to leave the ballot material on pass/hold with the editorial changes covered in the voting responses, awaiting publication of the MB specification.

The motion passed by acclamation.

4.2.5.0 #142.26 JC-40.4-09-126

**DDR3 MB F0RC14 DRAM
Command Control Word**

The vote count was 15 yes, 0 no and 5 abstentions.

Yes comments:

- FormFactor: Correct spelling of “Mirrors”. Response: Accepted as editorial.
- Micron: Same as above.
- Silego: Several editorial changes were proposed, including typos and clarifications.

The ballot material was reviewed. Response: Accepted as editorial.

IP Disclosure: Netlist indicated they have IP that may read on this material.

Patent numbers were identified as 7532537 and 7289386.

Motion by AMD and seconded by FormFactor to accept all proposed editorial changes and place the editorially modified ballot on pass/hold awaiting publication of the MB specification.
The motion passed by acclamation.

**4.2.6.0 #142.27 JC-40.4-09-123 DDR3 MB F0RC12 DRAM Interface
Training Control Word**

The vote count was 13 yes, 0 no and 7 abstentions.

Yes comments:

- Inphi: "Context" tends to confuse the meaning of this function. An alternate word is needed.

Motion by AMD and seconded by Silego to discuss clarification wording in the TG and if 100% consensus is achieved on the wording change, to place the editorially modified ballot material on pass/hold pending the completion of the MB specification.

Discussion:

IP Disclosure: Netlist indicated they have IP that may read on this material.
Patent numbers were identified as 7532537 and 7289386.

The motion passed by acclamation.

**4.2.7.0 #142.28 JC-40.4-09-124 DDR3 MB F0RC11 Parity Control
Word**

The vote count was 15 yes, 0 no and 5 abstentions.

Yes comments:

- Silego: Add (Default) after "OFF". Response: Accepted as editorial.

Motion by AMD and seconded by Silego to leave the editorially modified ballot material on pass/hold pending completion of the MB specification.

Discussion:

IP Disclosure: Netlist indicated they have IP that may read on this material.

**Minutes of Meeting No. 158
JC-40 Digital Logic Committee**

June 4, 2009

Montreal, Canada

Patent numbers were identified as 7532537 and 7289386.

The motion passed by acclamation.

**4.2.8.0 #142.29 JC-40.4-09-125 DDR3 MB F[3-11]RC6 Connector
Interface Control Word**

The vote count was 14 yes, 0 no and 7 abstentions.

The ballot passed by acclamation.

Motion by AMD and seconded by FormFactor to leave the ballot material on pass/hold pending completion of the MB specification.

IP Disclosure: Netlist indicated they have IP that may read on this material. Patent numbers were identified as 7532537 and 7289386.

The motion passed by acclamation.

**4.2.9.0 #142.32 JC-40.4-09-116 DDR3 MB Control Word – Pre/Post
Launch Update**

The vote count was 12 yes, 0 no and 8 abstentions.

Yes comments:

- FormFactor: Not sure timing accuracy is good to so many significant digits. Response: The committee has not decided the number of significant digits (e.g. 3 to 4 digits) to the right of the decimal point. This question on accuracy should be considered in the TG. Is there a JEDEC standard on this (a hard metric on timing accuracy)?

Comments were made that the accuracy is determined by the application and that test devices are generally accurate within about 5%.

Mr. Keller indicated that he would consider having presentations in the DDR3 validation committee which can be brought to this committee regarding appropriate timing specification accuracy. He indicated that Agilent will also bring a presentation describing conventional processes.

- Silego: Two editorial changes were proposed - change "Delay Y" to "Y Delay" in Table 1 and in table 2, is the "2" after "Control Word" intentional? Remove this text.

**Minutes of Meeting No. 158
JC-40 Digital Logic Committee**

June 4, 2009

Montreal, Canada

IP Disclosure: Netlist indicated they have IP that may read on this material.
Patent numbers were identified as 7532537 and 7289386.

Motion by IDT and seconded by FormFactor to place the ballot material on
pass/hold with the editorial changes proposed by Silego.
The motion passed by acclamation.

4.2.10.0 #142.33 JC-40.4-09-117

**DDR3 MB Control Word – 3T
Update**

The vote count was 14 yes, 1 no and 6 abstentions.

No votes:

- FormFactor: The voting response included a request for clarification of a
portion of the ballot material. Response: Mr. Chung provided a verbal
clarification of the ballot text. Suggested moving “control signals” portion of
the subject text into a note for clarification. Response: Accepted as editorial.

Yes comments:

- Silego: A typo was identified. Response: Accepted as editorial.

Motion by IDT and seconded by Montage to place the editorially modified
material on pass/hold.

The motion passed by acclamation.

Discussion:

- A member commented that the agenda, on page 37, has several incorrect
numbers and/or names.

IP Disclosure: Netlist indicated they have IP that may read on this material.
Patent numbers were identified as 7532537 and 7289386.

4.3.0 Second Presentations

4.3.1.0 #137.00 HP

DDR3 Ultra Low Voltage Memory

The sub-committee agreed that the material need not be re-shown in this
sub-committee as it was already shown earlier in the committee meeting.

4.3.2.0 #142.31 IBM

MB 8CS Inputs

IBM indicated that an electronic first showing was made greater than 30 days prior to the committee meeting

The MB TG has achieved a consensus that the buffer will support 8 chip selects. A control word needs to be defined. Proposed updates to the F0RC13 (control word) table were shown.

Motion by IBM and seconded by Montage to authorize the TG to issue one or more ballots on the material.
The motion passed by acclamation.

IP Disclosure: Netlist indicated they have IP that may read on this material. Patent numbers were identified as 7532537 and 7289386.

4.3.3.0 #142.24A Inphi

**DDR3 Memory Single Buffer
Ballout (0.65 mm Pitch)**

Secr. note: The item number and filename on the JEDEC server reflect a showing of this material under prior item #142.14. Item #142.24 was subsequently assigned to this material.

Inphi indicated that the ballout was discussed during the ballot reviews earlier in the meeting. The proposed ballout includes all items on the TG consensus list up to this meeting, such as the 4 additional CS pins (IBM).

Inphi indicated that ballot authorization was granted earlier in the meeting.

4.3.4.0 #142.35 Inphi

MB Initialization Sequence

A high-level overview of the initialization sequence was shown, covering host operations prior to normal operation. The MB power-up timing was then shown and was described as being fundamentally the same as the SSTE32882 device.

The MB power-up table was reviewed, followed by the host configuration of the MB control words, the host MRS to configure the DRAM (the buffer simply forwards these commands), the MB-DRAM interface training (MB write-leveling to DRAM, read training, etc), after which normal operation can begin. The MB-DRAM write leveling steps and read training were then shown in greater detail – the TG will work the details.

Discussion:

- A request was made to change the text from “iMB” to “MB” where this shows up in the presentation.

4.3.5.0 #142.36 Inphi

MB Transparent Mode

Inphi indicated that the material was previously shown in JC-45. A request was made as to whether the material need be re-shown - no members asked to have this re-shown.

The material was not shown in the committee but was loaded on the server.

4.3.6.0 #142.38 Inphi

Scalability of SB-Based LR-DIMMs

Inphi indicated that the material was previously shown in JC-45. A request was made as to whether the material need be re-shown - no members asked to have this re-shown.

The material was not shown in the committee but was loaded on the server.

4.3.7.0 #142.40 IDT

SB Ballout Considerations

IDT indicated that the material was previously shown in JC-45 – the TG was asked consider these proposals to the single buffer ballout.

A request was made as to whether the material need be re-shown - no members asked to have this re-shown.

The material was not shown in the committee but was loaded on the server.

4.4.0 First Presentations

4.4.1.0 #142.42 IDT

**Memory Buffer SMBus CSR MAP
for LR-DIMM**

Consensus list items were reviewed:

- Eight functions (4 for JEDEC-use, 4 for vendor-specific use) were added to the consensus list (2/16/09)
- Each function is 256 bytes deep (2/16/09).
- A function map overview (FN0 – FN7) was added 2/16/09.

IDT indicated that the vendor-specific registers need not be defined as “host bus” or “DRAM bus” registers.

Motion by Montage and seconded by IDT to elevate the showing to be a second showing.
The motion passed by acclamation.

Motion by IDT and seconded by Intel to authorize the MB TG to issue one or more ballots on the material.
The motion passed by acclamation.

4.4.2.0 #142.43 IDT

Memory Buffer Membist for LR-DIMM

The MB TG consensus list was shown including items related to Membist. The rationale for including Membist was summarized, including the fact that the DRAM interface is fully hidden behind the buffer, the memory buffer does not have boundary scan of JTAG, Membist exercise all pins between the buffer and DRAM, etc. Membist exercises/stresses the DIMM with system-level timings – using the same settings the host uses, the DRAM interface must be fully trained before running Membist, etc.

Membist can further run data patterns, address patterns, include failure locators, determine margin at various operational corners, clear and check memory in boot phase.

Membist is started through SMBus or RCW (BIOS-level access). The memory buffer needs to know the number of rows and columns (through the host or other means). Can use an error indicator or the SMBus to report errors.

The presentation included the proposed use of Function 3 and Function 5 for Membist.

Motion by Montage and seconded by IDT to elevate the showing to be a second showing.
The motion passed by acclamation.

Motion by IDT and seconded by Montage to authorize the MB TG to issue one or more ballots on DFX features in the MB.

Discussion:

- SMBus is a very slow bus – consider use of I2C bus? Will affect effectiveness of the DFX features. Response: Will consider I2C in TG discussions.

IP disclosures

- Cray verbally disclosed IP related to US patent #7184916. A RAND letter is in place which may relate to this material - the RAND letter was not limited to the FB-DIMM.

- Netlist verbally disclosed that they may have IP that may apply to this proposal – Netlist will follow-up with the JEDEC office on this IP.

- Which committee will review this ballot? Response: To be counted in JC-40.4 as this is an MB function/feature.

The motion passed by acclamation.

4.4.3.0 #142.44 AMD

DDR3 LRDIMM Control Word Clarification

Table 14 F0RC7 was shown. AMD proposed deleting the wording associated with the buffer number. AMD indicated that similar changes should be made throughout the control word ballots (e.g. table 23, table 24, etc) to remove any reference to dual buffer cases.

Motion by AMD and seconded by Samsung to empower the TG to editorially make changes to the memory buffer control word ballots previously passed to reflect the use of a single buffer if a 100% consensus is achieved on the editorial modifications.

The motion passed by acclamation.

4.5.0 Task Group Update

4.5.1.0 #142.10 TG

DDR3 MB TG

The TG mission and goal was reviewed, followed by the ballots issued this quarter. The TG consensus list was then shown, including the recent decision in the TG to develop a single buffer solution.

The new JEDEC website information used by the TG was shown.

Motion by Silego and seconded by Inphi to authorize the MB TG to issue one or more ballots based on the existing DDR3 register spec currently on pass/hold.

The motion passed by acclamation.

Mr. Chung indicated that this action empowers the MB TG to work on all aspects of the MB.

The TG logistics were shown, followed by the TG activity now underway, including straw polls related to several AMD proposals regarding memory refresh. Planned TG activity was reviewed for the next quarter, including two possible motions (not made during this presentation).

The consensus list was shown (50 items), followed by the IP tracking list. Mr. Smolka agreed to add to the list the new IP disclosures made during this meeting.

4.5.2.0 #154.00 TG

DDR4 VRD TG Report

The TG logistics were shown – the TG is currently a JC-45 TG, with 196 members over 60 companies and 10-15 members on each call. The scope is to consider of a voltage regulator on DIMM as proposed by HP's JC-45 item #2208.01.

A list of TG discussions and associated presentations was shown. The TG consensus list was shown, comprising one item.

The presenter requested that the JC-45 TG work jointly with JC-40.4 on this proposal.

Mr. Chung authorized that JC-40.4 participate with JC-45 and that the TG operate as a joint TG.

Motion by Inphi and seconded by (no second) to authorize the VRD logic device TG to issue one or more ballots on a VRD logic device.

Discussion:

- A concern was indicated that there have been no presentations made in this committee on a VRD device.
- An observation was made that the JC-40 committee requires 2 showings – the showing would need to be elevated to a second showing.

The TG report included a request for authorization to issue one or more ballots, as included on page 8 of the presentation.

**Minutes of Meeting No. 158
JC-40 Digital Logic Committee**

June 4, 2009

Montreal, Canada

Discussion:

- Consider sending out a survey ballot on the 5 items listed.
- An observation was made that the listed items appear to be DIMM topics (JC-45).

The motion was withdrawn.

The chairman authorized a newly formed VRD Logic Device TG to issue one or more survey ballots as required.

Discussion continued in regard to the TG showing:

- The material presented related to Item #122.08, which was previously shown.
- Item #152.01 was shown in the February '2009 meeting, related to a voltage regulator on a DIMM in this committee.

The chairman empowered the TG to issue a survey ballot on item #2 on page 8 of the current showing.

Motion by Montage and seconded by Intel to authorize the VRD Logic Device TG to issue 4 ballots on items 1, 3, 4 and 5 on page 8 of 8 in the current presentation (JC-45 item #2208.00), based on the first showing on item #152.01 from the February '2009 meeting.

Discussion:

- A concern was raised that these items, as worded, are not JC-40 work items. JC-40 can't issue DIMM ballots from this committee – just device ballots.

An amendment was proposed to modify the motion to empower the TG to issue one or more ballots on component-related aspects to support the VRD.

The amendment was accepted by the first and second to the original motion.

The amended motion passed by acclamation.

5.0 JC-40.5 Logic Verification and Validation

The JC-40.5 meeting opened at 2:24 PM on June 4, 2009. Mr. Keller led the discussion of this group.

5.1.0 Agenda

The agenda was reviewed, after which the scope was reviewed.

5.2.0 Ballot Review

There were no ballots for review in this sub-committee.

5.3.0 Second Presentations

5.3.1.0 #149.02 Agilent/IDT/Inphi/Montage/TI MB Test Boards for Characterization, Validation and Failure Analysis

The motivation is to establish a means to do accurate and repeatable measurement of MB parametrics, power and protocol behavior - in and out of the system, under varying operating conditions, etc.

The proposed fixturing and probing was reviewed –including an MB parametric test fixture, a DIMM parametric test, a protocol test, a parametric DIMM system probe, device and DIMM probes.

A proposed LR-DIMM in-system test was described – including where testing may be done, the use of a DIMM parametric test board, etc. The DIMM parametric test board objectives and a block diagram were shown, followed by the MB component parametric test board objectives and block diagram. A protocol test board was then described, followed by a possible structure.

A request was made to form an LR-DIMM validation TG to further define and promote development of these tools for industry enablement.

Discussion:

- This topic should be brought up in JC-45 as well, since the proposal includes DIMM test platforms and test probing.
- A company indicated that any test fixtures, adapters and/or other test devices developed within the JEDEC committee must be made available to all (e.g. no discrimination) – preferably through a third party supplier.

The sub-committee chairman formed the requested TG with Victor Cai and Jeffrey Chung appointed by Mr. Keller as the TG chair and vice-chair respectively.

5.3.2.0 #133.03 Agilent

**DDR3 Register/PLL Validation
Procedure**

The presentation covered a tSTAOFF/tDYNOFF update – with procedure simplifications based on TG inputs

The test procedure draft was briefly shown – the document was loaded on the server for later review by members.

Motion by Agilent and seconded by (company name not captured) to authorize the DDR3 Register/PLL Validation TG to issue one or more ballots on the DDR3 Register/PLL test procedures, including input from Mr. Kelly.

Discussion:

- Clarification questions were asked regarding the test procedures.
 - In response to a question Mr. Keller indicated that the procedures do not require specific non-JEDEC equipment. Is there anything in the spec that is not readily available? Response: The proposed procedures do not require a specific platform or equipment. At this time, test platforms developed by Inphi, IDT, TI are included in the specification.
 - TI was asked if the RVB Lite test platform is available to everyone in a non-discriminatory manner. Response: Yes – provided by 3rd party supplier.
 - IDT was asked if the RVB test platform is available to everyone in a non-discriminatory manner. Response: Yes – provided by 3rd party supplier. - -
 - Inphi was asked if the CRB test platform is available to everyone in a non-discriminatory manner. Response: The CRB is an Inphi product (no RAND commitment was provided to the committee).
 - Mr. Kellogg indicated that he would speak to Mr. Kelly in regard to referencing a platform, in a JEDEC document, that is not available to everyone under RAND terms.
 - What if a customer says a device does not meet the specification on a test platform not available to the device manufacturer? If not available to all, then the test platform should not be referenced.
 - Mr. Keller indicated that the validation procedure would be balloted for publications as a JEP document (as an application note).
- Discussion continued consistent with earlier comments.

Mr. Keller indicated that the TG should consider feedback from Mr. Kelly in preparation of any such ballots.

The motion passed by acclamation.

5.4.0 First Presentations

5.4.1.0 #142.41 Inphi LR-CTC Concept for MB

Inphi reviewed a test platform having a fully configurable environment for the MB, supporting 3 DIMMs per channel and requiring minimal external equipment.

The hardware feature set was summarized, including memory access to all ranks/slots, a user configurable memory-testing engine, MB control register access (read/write), configuration of memory controller via SPD, Vref and VDD margining, etc.

The software feature set was then summarized, including an easy to use GUI interface, GPIB and LAN access to external equipment, fully programmable test vector development, GUI access to all testing features, compiler for customized memory testing, etc.

The design methodology was shown, including a block diagram of what the solution would look like as well as a representative photo.

An initial list of tests was reviewed, including single bit and SSO delay testing, parity functionality testing, GND/VDD bounce due to SSO, signal integrity, protocol testing, parametric testing, etc.

5.4.2.0 #133.04 Silego DDR3 RCD tQsk Measurement Procedure

Silego indicated that the material was previously shown to the TG on May 28th. The TG has reached a consensus, with the material almost in ballot ready form on the server.

The proposed document was shown to the committee, with the committee asked to review the proposed document in more detail as time permits. The document references all 3 test platforms – thereby potentially have the same concerns regarding platform availability as discussed earlier in the meeting. The TG will await and consider feedback from Mr. Kelly.

The test setup and test procedure were reviewed with examples of clock/data capture waveforms shown. The document described how to calculate tQsk from the measurement example.

Silego indicated that the document is pretty much ready to go except for the board availability concern.

Motion by Silego and seconded by Sun to elevate the material to be considered as a second showing.
The motion passed by acclamation.

Motion by Silego and seconded by Netlist to authorize the TG to issue a ballot on this test procedure, with the same criteria as item #133.03.

An amendment was proposed to modify motion to remove reference to the CRB.

Discussion:

- A comment was made that a JEP document may be different than a JESD document as related test board references and availability.

The proposed amendment was not accepted by the first and second to the original motion.

Discussion:

- The RVB and RVB-lite boards are readily available whereas the CRB does not appear to be. The document should not reference the CRB if it is not readily available.

The motion passed by acclamation.

5.4.3.0 #133.05 Silego

**DDR3 RCD Plug-In Test Card
Errata**

A signal integrity issue was observed on the JEDEC DDR3 RCD plug-in test card when running an SSO pattern. The QAxx (left side) was found to be worse than the QB (right side).

The optimal solution would be a new design, adding decoupling capacitance on the VTT and VDD planes near the termination resistors.

The existing test cards can be modified by adding capacitance between VTT and GND. The proposed changes were described and shown. The optimal solution was found to add four 0.01uF caps (waveform examples were shown with 0 caps, 2 caps and 4 caps at two conditions). Information shown indicated that far-end (long) signal traces do not require added caps.

Two options were then summarized:

- 1) Issue an errata to customers of the DDR3 RCD PIC through CST (the board supplier)

2) Re-design the DDR3 RCD PIC for proper referencing/decoupling (reference VDD, add decoupling caps between VDD and VTT).

Discussion:

- It was observed that some slides show 0.1uF, others show 0.01uF.

Response: Silego will check to see which is correct.

- Do using companies need help to do the re-work Silego is suggesting?

Response: They should not need help as the re-work is relatively easy.

- CST indicated that there is no inventory of unsold boards and indicated a willingness to send out a letter with proposed errata to purchasers.

Mr. Keller indicated that work will be done to initiate a design modification should new boards be ordered, and that the TG will review the design modification. In addition, errata will be prepared such that CST can issue it. The errata will be prepared by Silego.

5.5.0 Task Group Update

5.5.1.0 #133.00 TG

DDR3 Register/PLL Validation TG Report

The TG logistics were shown, with meetings every week held after the Register/PLL TG call. About 34 companies and 140 members are included on the TG roster, with 6 – 12 participating in a typical call.

Showings and discussions summarized were summarized including tDYNOff/tSTAOFF, tQSK, low voltage register/PLL measurements, slew rate and instrument performance requirements, etc. Remaining TG work was also summarized.

The TG consensus list was shown, which included a consensus that procedures should support all 3 test platforms (RVB, CRB and RVB-lite) where possible. Other consensus items included parameters to be measured, 200 cycle TJ model is normative (10K cycles used previously), 1E-12 BER method is informative, etc.

Two proposed jitter specification methodologies were shown – The “N-Cycle” (more traditional) approach does tend to be optimistic. Companies were asked to provide input. The specification methodology may require modification in the future for higher speeds to maintain closure.

**Minutes of Meeting No. 158
JC-40 Digital Logic Committee**

June 4, 2009

Montreal, Canada

6.0 Other Committee Business

- Inphi indicated that any test boards, related hardware and source code developed by them for such test boards would be turned over to a 3rd party for sale and distribution. In addition, the design would be made available as an open source design (FPGA code made available). As clarification, Inphi indicated that this would apply to the CRB, with the CRB BoM and all related materials to be provided to CST for distribution.

- A member asked the committee chairman, Mr. Smolka, to adopt the JC-42/45 Excel spreadsheet format for the showings and ballots. Mr. Smolka agreed that this would be done.

- A clarification question was asked regarding the meeting date and start time for JC-40, given that the JC-16/42/45/63 plenary session agreed to change the 3Q '2009 meeting start date to Tuesday, September 8th (Monday is Labor Day in the U.S.).

Discussion:

- Can the meeting week be compressed to 4 days? Response: Unless agreed upon by the committee chairmen (some of which were not present), it was recommended that reserve a meeting room for Saturday.

- Mr. Smolka indicated that if JC-40 can start by 10 AM on Friday, and run long on Friday if needed, the committee would complete their activities on Friday. Mr. Rhoden agreed to contact the other committee chairmen to determine if those meetings will end such that JC-40 will start no later than 10 AM Friday (each meeting day may need to run long).

Motion by Silego and seconded by TI to modify any related prior motions made during this meeting to permit inclusion of the CRB in the ballot material

The motion passed with a vote count of 1 opposed and 4 in favor.

7.0 Adjournment

Motion by Intel and seconded by Google to adjourn the meeting.
The motion passed by acclamation.

The meeting adjourned at 4:07 PM on June 4, 2009

**Minutes of Meeting No. 158
JC-40 Digital Logic Committee**

June 4, 2009

Montreal, Canada

**THIS MEETING WAS CONDUCTED IN ACCORDANCE WITH JEDEC
LEGAL GUIDES, JM5, AND THE JEDEC MANUAL OF ORGANIZATION
AND PROCEDURE, JM21-N.**

REVIEWED/CORRECTED AND AUTHORIZED FOR RELEASE BY:

Approved on: June 24, 2009
JC-40 Chairman, John Smolka

The following individuals did review/approve the minutes:

Approved on: June 24, 2009
JC-40.1 Sub-Committee Chairman, Rick Williams

Approved on: June 30, 2009
JC-40.3 Sub-Committee Chairman, Ramzi Ammar

Approved on: June 20, 2009
JC-40.4 Sub-Committee Chairman, Jeffrey Chung

Approved on: July 1, 2009
JC-40.5 Sub-Committee Chairman, Perry Keller

Approved on: June 17, 2009
Legal Approval, John Kelly

Approved on: June 16, 2009
Secretary, Mark Kellogg

Exhibit I

JEDEC MANUAL

JEDEC Manual of Organization and Procedure

JM21N

(Revision of JM21M, December 2006)

MAY 2008

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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JEDEC MANUAL OF ORGANIZATION AND PROCEDURE

Contents

	Page
1 JEDEC	1
1.1 Mission	1
1.2 Scope	1
1.3 Membership	1
1.4 Board of Directors	2
1.4.1 Eligibility	2
1.4.2 Election of Directors	2
1.4.3 Member Company and Director resignation	3
1.4.4 Officers of the Board of Directors	4
1.4.5 Board of Directors meetings	4
1.4.5.1 Board of Directors Executive session	4
1.4.5.2 Board of Directors voting	4
1.4.5.3 Emergency action by the Board of Directors	4
1.4.6 Board of Directors guest policy	5
1.5 Governance/Interpretation	5
1.6 Scope of participation	5
1.7 Limits and restrictions	5
1.8 Modifications to the Manual of Organization and Procedure	6
2 Committees	6
2.1 Committee responsibilities	7
2.2 Executive committee	7
2.3 Election of Officers	8
2.4 Representation on the EIA Board of Governors	8
3 Meetings	9
3.1 General requirements	9
3.2 Notices	9
3.3 Agendas	9
3.4 Meeting attendance	9
3.5 Quorum	10
3.6 Recording devices	10
3.7 Minutes	10
3.7.1 Policy statement on JEDEC sign-in/attendance rosters	11
3.8 Regular meetings	11
3.9 Special (Limited Scope)	11
3.10 Joint meetings	12
3.10.1 Between JEDEC Committees	12
3.10.2 Between JEDEC and any non-JEDEC organization	12
3.10.3 Memorandum of Understanding (MoU)	12
3.11 Task groups	13
3.11.1 Joint task groups between JEDEC committees	13
3.11.2 Joint task groups between a JEDEC committee and other organizations	13
4 Document development procedure	14
4.1 Copyrights	14
5 Voting	15
5.1 Ballot voting	15
5.2 Ballot approval by acclamation	16

JEDEC MANUAL OF ORGANIZATION AND PROCEDURE**Contents (cont'd)**

	Page
6 Ballots	16
6.1 Editorial changes	16
6.2 Ballot lobbying	16
6.3 Copyrights (see 4.1)	16
6.4 Regular committee ballot	17
6.5 Limited committee ballot	17
6.6 Board of Directors ballot	17
6.6.1 Committee ballots sent to the Board of Directors	17
6.7 Survey ballots	18
7 JEDEC documents	19
7.1 Interpretation	
7.2 Document Maintenance	
7.3 Document Types	
7.3.1 Standards (JESD)	19
7.3.2 Publications (JEP)	19
7.3.3 Specifications (JES)	19
7.3.4 Registered Outlines (TO, MO, CO, PO, etc.)	19
7.3.5 Registration Data Formats (RDF)	19
7.3.6 Manuals (JM)	19
7.3.7 Joint Documents (J-STD, JP, and JS)	19
7.3.8 ANSI/JEDEC Standards	19
8 Legal Guidelines	20
8.1 JEDEC documents and publications	20
8.2 Reference to patented products in JEDEC standards and publications	20
8.3 Special legal disclaimer	21
8.4 Committee responsibility concerning intellectual property	22
9 Appeals	22
9.1 Right of appeal	22
9.2 Criteria for appeals mechanism	22
9.3 Appeals procedures	23
9.3.1 Complaints	23
9.3.2 Response	23
9.3.3 Hearing	23
9.3.4 Conduct of the Hearing	23
9.3.5 Decision	23
9.4 Further appeal	24
10 External publicity	24
11 JEDEC ethics rules for electronic communications	25
Annex A (normative) Legal Guidelines Summary	26
A.1 EIA/JEDEC patent policy summary	26
A.2 Copyright material	26
Annex B (informative) Patent policy application guidelines	27
Annex C (informative) ANSI Standardization Procedures	28

JEDEC MANUAL OF ORGANIZATION AND PROCEDURE

(From JEDEC Board Ballot JCB-02-31A, JCB-04-75, JCB-04-89, JCB-05-60, JCB-05-103, JCB-05-124, JCB-05-99C, JCB-06-02, JCB-06-36, and JCB-08-11, formulated under the cognizance of the JEDEC Board of Directors.)

1 JEDEC

JEDEC is an independent incorporated Association governed by a Board of Directors (Board). The Association facilitates standardization within the solid state technology industry and other related activities through special purpose committees.

The Association and its members are committed to foster open competition in the development of products and services.

JEDEC is a founding sector of the Electronic Industries Alliance (EIA).

1.1 Mission

The mission of JEDEC is to serve the solid state industry by creating, publishing, and promoting global acceptance of standards, and by providing a forum for technical exchange on leading industry topics.

1.2 Scope

The scope of JEDEC includes but is not necessarily limited to areas relating to (1) discrete solid state devices, (2) integrated circuits, (3) electronic modules, and (4) various manufacturing support functions.

1.3 Membership

Any company, organization, or individual conducting business that itself or through a related entity manufactures electronic equipment or electronics-related products, or provides electronics or electronics-related services, shall¹ be eligible for membership in JEDEC. Membership on a given committee shall be open to any JEDEC member company in good standing dependent solely on the dues structure defined by the Board².

Each member company, organization, or individual shall be entitled to appoint one member and multiple alternates for each committee it joins. The member and alternates should be capable of making a technical contribution to the standards-setting process of the committee. To preserve the “one-company one-vote” concept within JEDEC, wholly-owned or majority-owned subsidiaries shall not be granted separate voting privileges within any single committee or subcommittee. The JEDEC office shall maintain a list of all member companies and representatives for each committee.

¹ Special word usage. The word "shall" indicates a requirement; see JM7, annex J.

² JEDEC membership is not a prerequisite to committee participation. Non-member participation fees will be charged. Before attending a JEDEC meeting, guests and non-members must agree to comply with all JEDEC rules and procedures, including the rules and procedures set forth in this Manual. Further details are available from the JEDEC office. See 3.4.

1 JEDEC (cont'd)

1.3 Membership (cont'd)

All changes in committee membership shall be the responsibility of the member company, who shall so advise the JEDEC office and the committee chairperson in writing or by electronic means.

NOTE Government regulations restrict the participation of non-U.S. Nationals at certain meetings. Every effort shall be made to notify member companies, well in advance, when a meeting will cover restricted topics.

1.4 Board of Directors

The governing body of JEDEC is the JEDEC Board of Directors (Board) which is comprised of individual Directors (or their alternates) representing JEDEC member companies.

1.4.1 Eligibility

Any maximum dues paying Member Company of JEDEC, having an identified representative in two or more committees for at least the past two consecutive years, may nominate one candidate for Board membership. The nomination consists of the nominee's resume accompanied by a letter from a company executive to the Board chairperson (in care of the JEDEC office). The support letter is to request that the nominee be considered for Board membership and committing that if elected the member company will support the nominee's active attendance and participation in JEDEC Board meetings and affairs. If the application meets the above requirements, the JEDEC Office will hold the application on file with other (qualified) nominees. The JEDEC Office will maintain an official list of nominations to the Board. A list of the current Board Committees with a brief description and the membership of each will be sent to the nominee with an invitation for the nominee to participate where he/she has interest.

Seats on the Board are occupied by Directors representing individual JEDEC Member Companies. Once elected to a Seat on the Board, the Member Company maintains its position until the seat is voluntarily relinquished or forfeited due to other events as outlined in 1.4.3. Mergers, divestitures, acquisitions and other corporate changes that do not substantially alter the nature of a member company will not be grounds to forfeit a seat on the Board so long as the new entity continues to meet all Board Eligibility Requirements.

The total number of Directors shall not exceed thirty (30).

1.4.2 Election of Directors

The Membership Committee (chaired by appointment of the Chairman of the Board with membership open to any Board Member) shall review with the Board circumstances of a vacated seat and recommend qualified nominees from the official nominations list. In order to choose an appropriate nominee to fulfill objectives of the Board, the Membership Committee will review activities that are being conducted in active Board Committees with their respective Chairs.

1.4 Board of Directors (cont'd)

1.4.2 Election of Directors (cont'd)

The following process will occur:

- Board Committee Chairs will be informed of the vacant seat by the Membership Committee.
- It will be the responsibility of the Membership Committee to qualify the level of support required to achieve ongoing Board Committee objectives.
- The Membership Committee will compile inputs and prepare a review to the Board at the next Board meeting including a recommendation on how to fill any vacated seats.

The following procedures and guidelines will be employed by the Membership Committee during the preparation of its Director recommendations:

- Gathering of Board Committee Chair inputs on current activities and resource requirements. Chairs will have an opportunity to review with the Membership Committee special requirements, shortcomings, etc. that should be made evident during the election process.
- Identification of the nominee's JEDEC experience and previous contributions. Tenure and amount of activity within a Committee or Task group will be identified.
- Identification of Board demographics in regards to representation of committees.
- Identification of the leadership qualities the candidate will bring to the Board.
- Identification of the unique value of the individual and the member company. (Value based on Committee Objectives identified to properly support JEDEC.)
- Identification of the individual's education and professional background (Engineering, Management, Finance, Marketing, Business development, etc.) and the balance the candidate will bring to the Board.

The Board will act on the recommendations of the Membership Committee. New Directors are elected to the Board by a 75% majority of the Board members voting at the meeting. There is no requirement that the maximum of 30 Seats be filled. The Membership Committee will send a response letter to the elected candidate/company and inform them of their responsibilities as outlined in this section. The elected Director's qualifications will be presented in regards to support as an active member on one or more of the Board Committees. The Board may stipulate a contingency period during which the newly-elected Director is required to serve on one or more Board Committees.

1.4.3 Member company and Director resignation

The Director will relinquish a position on the Board in the instance of any of the following events:

- 1) The Member Company formally resigns the position. This includes a statement from the Member Company that confirms the Director and Member Company resignation.
- 2) The Member Company which the Director represents is no longer eligible as defined in 1.4.1.
- 3) The Member Company is removed by a majority vote of the Board for gross violation of JEDEC policy.
- 4) The Director is absent from and not represented by a Member Company's approved alternate at two consecutive Board meetings within a calendar year. Participation via teleconference is allowed only once per calendar year.

1.4 Board of Directors (cont'd)

1.4.3 Member company and Director resignation (cont'd)

In the event that a Director no longer represents the Member Company for which the individual was elected (including but not limited to retirement or change of employment) or should the Director be removed due to gross violation of JEDEC policy outside of the control of the Member Company, then the Board seat shall not be considered vacated and the Member Company shall have the right to maintain its position on the Board by nominating a replacement Director. The replacement Director must meet all nomination requirements as set forth in 1.4.1 and be elected by the full Board by a 75% majority of the Board members voting at the meeting. Should the replacement Director fail to be elected, the Member Company may submit a second candidate and repeat the process.

1.4.4 Officers of the Board of Directors

The officers of the Board shall follow the same guidelines as the officers of a committee with the following exceptions: There shall be at least one Vice Chairperson on the Board. The number of Vice Chairpersons on the Board shall be determined by regular vote at any regularly scheduled Board meeting.

1.4.5 Board of Directors meetings

All meetings of the Board shall follow the same procedures and guidelines as outlined for regular committee meetings, with exceptions per 1.4.5.1, 1.4.5.2, and 1.4.5.3..

1.4.5.1 Board of Directors executive session

The needs of the Association occasionally require the Board to meet in executive session. Such executive sessions are to be defined as closed meetings of Board member company representatives and guests invited for specific purposes only.

1.4.5.2 Board of Directors voting

All actions within the Board require an affirmative vote of at least 75%; members abstaining shall not be considered for determination of the 75% criterion. When defined and agreed to by a duly recorded vote of the Board, specific action may require polling of all members whether present or not and/or may require a higher percentage affirmative vote.

1.4.5.3 Emergency action by the Board of Directors

If action normally requiring Board consideration must be taken, and a meeting cannot be reasonably convened, then the following modifications apply to the approval process: 1) A reasonable attempt must be made to notify 100% of Board members, and 2) The decision shall become binding only upon receipt by the JEDEC office of affirmative votes from 75% of the members of the Board.

1.4 Board of Directors (cont'd)

1.4.6 Board of Directors guest policy

All guests must be approved by the chairman and must have a purpose related to the topics of discussions at the Board meeting. The guest must be introduced to the Board at the meeting and the purpose of the guest's visit should be stated in the agenda for that meeting.

At the discretion of the Board, a guest may be allowed to stay beyond the allotted time slot if the Board feels there is a need for that guest's continued attendance. Otherwise, all guests may only attend the portion of the Board meeting that is directly related to their purpose in the meeting. At no time may a guest speak to the Board beyond the intended purpose of he/she invitation without the explicit approval of the Board.

At anytime, any member of the Board may request that the chairman, at his discretion, ask a guest to leave the meeting.

1.5 Governance/Interpretation

The Board shall have the sole authority to interpret, in whole or in part, these operating procedures. In any case where conflict arises from ambiguity, or lack of specificity, or misunderstanding within or related to this document, the officers of the Board of the Association may make temporary rulings to be confirmed or modified at or before the next regularly scheduled Board meeting by vote of the Directors. In any case where there is not agreement between 100% of the officers of the Board concerning an interpretation, then the matter must be referred to the entire Board for resolution.

1.6 Scope of participation

The standards development process shall not be dominated by any single interest category, individual, or organization. Dominance means a position or exercise of dominate authority, leadership, or influence by reason of superior leverage, strength, or representation to the exclusion of fair and equitable consideration of other viewpoints.

The standards development process should have a balance of interests. Participants from diverse interest categories shall be sought with the objective of achieving balance.

1.7 Limits and restrictions

The Members (particularly where they are direct competitors in certain lines of business, and including their employees and representatives), shall, when engaged in the activities and affairs of the Association, act in a manner that does not violate any state, federal or international laws or regulations.

Member companies must abide by all applicable export control regulations of their respective countries while attending a JEDEC meeting, irrespective of where the meeting is actually held. It is recommended that the member seek guidance from his or her company if involved in "state of the art" engineering work, as significant changes are made to the export control regulations from time to time.

1.7 Limits and restrictions (cont'd)

The Association prohibits any discussion on specific costs, prices, quantity or yield of production levels, methods or channels of distribution, markets, customers or any other topic, or any conduct, that may be construed as a violation of antitrust laws. Each respective member company shall advise its respective participant representatives and employees on the importance of compliance with applicable state, federal or international antitrust laws or regulations and require the scope of any discussions or exchanges amongst representatives of Members and/or the Association, be limited to the mission and scope of the Association stated above.

1.8 Modifications to the Manual of Organization and Procedure

Modifications to this manual may be made in whole or in part, upon approval by the Board by the normal ballot process. Any changes to this Manual shall be distributed to the JEDEC membership at the earliest possible time upon adoption.

2 Committees

The Board shall have the authority to establish committees to perform any task(s) for the association. JEDEC committees (main and sub) shall be authorized only by the Board, and the Board shall approve the scope of each³. A main committee shall be designated by the prefix JC- plus a two-digit designator, such as committee JC-11. Main committees are separated into two types: (1) service committees, whose scope is limited to a specific subject that may impact several product types, and (2) product committees, whose scope is limited to a specific type product. For service committees, the first digit of the two-digit designator shall be the number 1, and for product committees, the first digit shall be the number 2 or higher.

When the main committee finds it necessary to divide its work into parts, subcommittees may be formed under the scope of the main committee and such subcommittees shall be designated by adding a period to the main committee number followed by a number or a number-and-letter designator (e.g., JC-42.3 or JC-42.3B).

Subcommittees shall have all the same authority and responsibilities as committees herein defined, except that a subcommittee scope shall be a subset of a committee scope, to be authorized, reviewed, and approved by the Board.

NOTE Participation shall be open to all persons who are directly and materially affected by the activity in question.

³ The committee scope shall go through the standard balloting process and must be completed within a reasonable timeframe and prior to any publication of a JEDEC document authored by the committee.

2 Committees (cont'd)

2.1 Committee responsibilities

Each committee shall have the authority to consider all matters within its approved scope, including but not limited to the following actions:

- a) Develop proposed standards, guidelines, registrations, and related technical publications for committee ballot.
- b) Authorize committee ballots on all matters within the committee's defined scope.
- c) Initiate proposals for Board ballots of previously approved committee ballots.
- d) Evaluate the results of all committee ballots, as well as comments on related Board ballots.
- e) Request approval of the Board to convert standards or publications into ANSI or IEC standards.
- f) Maintain liaison with other national and international organizations.
- g) Initiate press releases to announce a significant advancement in the work of solid state technology covered within the committee scope such as: registrations, standardization, or publication. All press releases are to be issued by the JEDEC office after review and concurrence by the JEDEC Legal Counsel.

2.2 Executive committee

A JEDEC committee or subcommittee may form an executive committee to manage its administrative work. The executive committee shall meet the following criteria:

- a) The executive committee should be chaired by the committee or subcommittee chairperson and shall include as a minimum all chairpersons and vice chairpersons of that committee and its subcommittees.
- b) Meetings of the executive committee shall be open to any committee member who gives reasonable advance notice to the executive committee chairperson or secretary.
- c) Actions of the executive committee shall be limited to handling administrative matters dealing with such items as meeting schedule, meeting agenda, future meeting dates and locations, personnel requirements, proposed work priorities, and the like. Any decision made by the executive committee is subject to review and modification by the full committee at the request of any committee member or alternate. Decisions on the final disposition of all technical matters shall be made only by the overseeing committee. Recommendations concerning future meeting dates and locations should be presented to the overseeing committee.

2 Committees (cont'd)

2.3 Election of officers

All JEDEC committee officers shall be members or alternates of their respective committees. All JEDEC committees shall have a chairperson and may also have a vice chairperson as officer(s) of the committee. All officers shall be directly elected either by secret vote of the committee members present during a regular meeting or by ballot as determined by vote of the committee. Committee officers shall serve a term of two (2) years. The JEDEC staff shall count the secret ballot and announce the result at the meeting.

At least two meetings prior to the end of a chairperson's term, he/she shall appoint a nominating committee to propose candidates to fill the next term of office(s) for the committee. The committee's candidates must be presented to the full committee at the next meeting and nominations from the floor shall also be accepted. All nominees must agree to accept the additional responsibilities before they can be considered.

If any of the officers cannot fulfill his/her term then elections shall be held at the earliest opportunity of the committee members. Similarly, if a new committee is formed, then the chairperson shall be selected by vote of the members attending the first meeting as a first order of business of the committee. These special case elections shall become effective immediately.

2.4 Representation on the EIA Board of Governors

As a sector of the Electronic Industries Alliance (EIA), JEDEC is entitled to elect members to the EIA Board of Governors. The EIA Executive Committee determines the number and allocation of sector seats on the Board of Governors.

JEDEC members of the EIA Board of Governors are nominated by the Nominations Committee of the JEDEC Board and elected by the JEDEC Board for three-year terms. To be elected, an individual must be a senior executive, officer, director, or similar level of a JEDEC member company. The individual does not need to be a member of the Board.

The Board may remove a JEDEC member of the EIA Board of Governors at any time. Grounds for removal include repeated failure to attend meetings or any other behavior that reflects unfavorably on JEDEC. The Board, at its sole discretion, will determine the adequacy of the grounds for removal. The decision of the Board is final.

When the seat of a JEDEC member on the Board of Governors becomes vacant due to resignation, removal, or any other reason, the Nominations Committee of the JEDEC Board will propose the names of one or more individuals to fill the unexpired term. The Board will elect the successor member of the Board of Governors.

3 Meetings

Communication between JEDEC member companies is essential for the work within the Association. All committees shall hold regular meetings for the purpose of conducting JEDEC business.

The use of teleconference or other electronic conferencing equipment is permitted for any type of JEDEC meeting.

3.1 General requirements

Every JEDEC meeting, regardless of type, shall be held in accordance with the directives contained within this manual and in accordance with all applicable laws.

All meeting notices, agendas, ballots, and minutes shall be distributed only by the JEDEC office. All correspondence from the JEDEC office shall only be by electronic means unless otherwise required by law. If a company requests distribution by other means, the JEDEC office will charge a fee for such additional service as directed by the JEDEC Board. The JEDEC website, www.jedec.org, shall be the primary method of electronic communication.

3.2 Notices

Notices of regular meetings shall be distributed solely by the JEDEC office no less than 28 calendar days prior to the start of such meeting, unless a “special” meeting is authorized by committee vote and the date and agenda for such meeting is fixed at a regularly scheduled meeting. Notices of such special meetings shall be distributed as soon as possible after said regular meeting and in no case less than 10 calendar days prior to the start of such special meeting.

3.3 Agendas

All meetings shall have prepared agendas distributed as soon as possible, but in no case less than 10 days prior to a meeting and should be included with the meeting notice if possible. All special meeting notices shall include the agenda at time of distribution of such notice.

3.4 Meeting attendance

All JEDEC committee and subcommittee meetings are open to members, their designated alternates, and guests invited by the committee or subcommittee chairperson.

A JEDEC staff member or a designated alternate must be in attendance at every committee meeting. The duties of the staff person shall include but not be limited to taking minutes, advising the chairperson regarding the content of this manual and JEDEC legal policies and guidelines, and distributing the minutes. JEDEC staff attendance is not required at every subcommittee meeting.

A potential new member company may be a guest for one meeting with prior approval of the chairperson. A timely submission of such a request stating the purpose of attendance shall be given so that appropriate accommodations can be made. If there are any issues to be raised by a guest, those issues must be specified in the purpose statement.

3 Meetings (cont'd)

3.4 Meeting attendance (cont'd)

Nonmembers may participate in committee meetings if they pay a nonmember participation fee. Nonmembers do not have the right to vote. Nonmembers should contact the JEDEC office prior to the meeting date for further details.

Before attending a JEDEC meeting, guests and non-members must agree to comply with all JEDEC rules and procedures, including the rules and procedures set forth in this Manual.

3.5 Quorum

The JEDEC office shall maintain a list of active members for the sole purpose of determining the quorum requirements for a committee meeting. An active member is defined as a member company that has been represented at either or both of the previous two consecutive regular meetings of the committee. Special meetings shall not be considered for the purpose of determining “active” member status. The quorum requirements shall be 50% by count of a committee’s active member list, but in no case shall the quorum requirement be greater than 20 member companies regardless of committee size. All committee member companies present at a meeting are counted toward quorum requirement.

3.6 Recording devices

Voice or video recording devices of any kind are forbidden at any type of JEDEC meeting.

3.7 Minutes

The principal activities and attendees at all JEDEC meetings shall be duly recorded in meeting minutes. Meeting minutes shall be taken by the assigned JEDEC staff for that committee or by a substitute designated by the JEDEC staff. In the absence of a JEDEC staff person at a committee meeting, a temporary secretary may be assigned by the committee chairperson.

Minutes shall be termed “unconfirmed” until reviewed and confirmed by the committee chairperson and JEDEC Legal Counsel. In the interest of member company needs, minutes should be distributed to members and alternates within 14 calendar days after a meeting. If the chairperson is unable to review and confirm the minutes within that time, the JEDEC office should distribute the unconfirmed minutes clearly labeled as unconfirmed minutes. Unconfirmed minutes shall be approved by JEDEC Legal Counsel prior to distribution. Confirmed meeting minutes from regular meetings shall be distributed no later than 28 days prior to the next regular meeting. Confirmed minutes from “special” meetings should be distributed as soon as possible after such special meeting and in no case less than 10 days prior to the next regular meeting.

3 Meetings (cont'd)

3.7 Minutes (cont'd)

At the end of each set of minutes the following statements shall appear:

“Reviewed/corrected and authorized for release” followed by the Chairperson’s and Secretary’s name and date.

Chairperson, Name / date

Secretary, Name / date

Confirmed Legal Approval Date

“This meeting was conducted in accordance with JEDEC Legal Guides and the JEDEC Manual of Organization and Procedure.”

For those situations where a report from an independent group is included in the minutes, for information purposes, then the following disclaimer may be added to the minutes:

“Disclaimer: All liaison, government, technical, and task group reports contained herein are believed to be accurate but the accuracy or completeness thereof is not guaranteed.”

Minutes of a task group meeting shall include a list of the attendees, the meeting agenda, a status review of the agenda items, and any final proposals including discussion related to the proposals. The time, the place, and any required follow-up should be included. Task group minutes are reported and approved as part of the minutes for the next meeting of the sponsoring committee.

3.7.1 Policy statement on JEDEC sign-in/attendance rosters

The policy statements reproduced on the reverse side of the JEDEC sign-in/attendance rosters shall become an integral part of the minutes of all committee, subcommittee, and task group meetings; and a statement shall be included in the minutes indicating compliance with the foregoing policy.

3.8 Regular meetings

Every JEDEC committee shall set up an annual calendar for regular meetings at which any item covered under the scope of the committee may be discussed. Under the JEDEC guidelines, committees must hold at least one (1) regular meeting each year to retain status as an active committee.

3.9 Special (Limited Scope)

All JEDEC committees shall have the authority to approve meetings of limited scope. Schedule for the meeting and specific agenda items must be approved by formal vote during a regular committee meeting. During a limited scope meeting, no other committee business shall be conducted outside of the specific items on the previously agreed to agenda. Items shall not be added to the agenda of a special meeting.

3 Meetings (cont'd)

3.10 Joint meetings

3.10.1 Between JEDEC committees

Joint meetings between two or more JEDEC committees may be authorized by agreement of the committees by vote. Selection of the joint meeting chairperson shall occur by vote of the committees' attendees. The joint chairperson shall ensure that all meeting notices, agendas, and minutes are distributed to the relevant JEDEC committees.

3.10.2 Between JEDEC and any non-JEDEC organization

Joint meetings between a JEDEC committee and any non-JEDEC organization are subject to the same requirements as 3.10.1. In addition, JEDEC Legal Counsel shall establish a Memorandum of Understanding (MoU), see 3.10.3, between the organizations and review all release of information from the meetings to any outside person or organization.

JEDEC committees may meet jointly with other organizations or agencies for the purpose of permanent or ongoing liaison. In these cases, those nonmembers attending the committee meeting are expected to pay their proportionate part of the total meeting costs. Apportionment of the meeting costs shall be agreed upon between the committee chair and the representatives of those groups participating in the meeting(s), subject to the approval of the JEDEC Board.

3.10.3 Memorandum of Understanding (MoU) with any non-JEDEC organization

Prior to the formation of a joint meeting/task group with a non-JEDEC committee, a Memorandum of Understanding (MoU) must be in effect between JEDEC and the other organization covering the following items:

- a) Balloting procedure (acceptance criteria, resolution of comments, and disapprovals),
- b) Patents procedure (including joint ownership),
- c) Distribution rights (copyright, use of association logos, available on JEDEC website without charge),
- d) Procedures for future revisions of the document(s),
- e) Selection of chairperson(s) and appointment of task group membership, and
- f) Meetings and related legal requirements (notices, agendas, motions, minutes, costs, etc.).

3 Meetings (cont'd)

3.11 Task groups

A task group may be authorized by any committee chairperson for a specific non-continuing objective. The task group chairperson, appointed by the committee chairperson, shall be a member or alternate of the overseeing committee. Membership within a task group is open to any member or alternate of the committee within which the task group is formed. In addition, members of the task group may also be appointed by the task group chairperson from nonmember JEDEC companies with approval of the overseeing committee chairperson; appointment shall be based solely on ability to contribute to the work; however, all members of a task group shall conduct their work in accordance with this manual.

A task group is not permitted to hold any formal votes or establish any final results relative to standards, publications, or ballots. All task group activities shall be presented to the overseeing committee for review, modification, and approval in the form of reports generated from every task meeting. By duly recorded committee vote, committees may authorize a task group to issue ballots or other specific tasks as required, the specific exception being that committees cannot authorize a task group to conduct a formal vote. A task group must be dissolved upon completion of its objectives.

Scheduling of task group meetings is subject to approval of the sponsoring committee's chairperson, in order to avoid conflict with regularly scheduled meetings.

3.11.1 Joint task groups between JEDEC committees

Joint task groups between two or more JEDEC committees may be authorized by agreement of the committee chairpersons. Selection of the task group chairperson shall be part of this agreement and that chairperson must be a member or alternate of one or more committees involved in the task group. The task group chairperson shall keep all sponsoring committees on the distribution list for all meeting notices, agendas, and reports. Joint task groups between JEDEC committees shall comply with all other requirements for task groups.

3.11.2 Joint task groups between a JEDEC committee and other organizations

Joint task groups between a JEDEC committee and other non-JEDEC organizations are subject to the same requirements as task groups per 3.11. Unless otherwise authorized by the Board and approved by JEDEC Legal Counsel, such joint task groups shall establish a Memorandum of Understanding (MoU), see 3.10.3, in the same manner as joint committees covered in 3.10.2.

4 Document development procedure

The development of all JEDEC documents shall follow the minimum sequential procedure outlined herein.

- 1) Presentation – initial showing or distribution of material proposed for publication. Presentations may occur at any regular meeting or special meeting if the limited scope and agenda include such information. Presentations may also occur entirely electronically without being at a meeting. An additional showing of material proposed for publication may be required.
- 2) Motion for ballot – may occur at any time after a presentation. The motion must have a second before being considered for vote. The company agreeing to second the motion for ballot should be willing to accept responsibility for sponsoring the material should the original sponsor be unable or unwilling to do so. The motion for ballot should be discussed after receiving a second and then a formal vote shall be taken.
- 3) All committee ballots shall be subjected to the committee’s editorial process prior to being posted on the JEDEC voting machine.
- 4) Committee ballot – if approved, material shall be sent out to ballot through the JEDEC voting machine. Details of balloting procedure are covered in section 6.
- 5) Motion to Board ballot – if a ballot passes and all comments are addressed then a motion may be made to send the material on to the Board for further consideration and approval. Alternatively, the motion to forward the ballot to the Board is unnecessary if the ballot passes by acclamation, see 5.2.
- 6) Board ballot – when approved, the committee material shall be sent out to ballot through the JEDEC voting machine. Board ballots follow the same procedures as committee ballots, see 6.6.1(c). When reviewing material passed by committee, the Board primarily considers whether due process has been followed.
- 7) Publication – once proposed material has successfully completed all the above steps and obtained approval through the appropriate balloting processes, it is approved for publication.
- 8) All JEDEC documents shall be published by the JEDEC office.

NOTE 1 Steps may be repeated as many times as required to satisfy the wishes of the member companies participating in the process.

NOTE 2 JEDEC Registrations are special-case publications that do not have to be reviewed by the JEDEC Board of Directors, and the registration procedure ends upon the completion of step 4 above.

4.1 Copyrights

JEDEC owns the copyright to all documents created through JEDEC, and use of that copyrighted material is at the sole discretion of the JEDEC Board.

For the protection of member companies, all JEDEC publications and standards shall be copyrighted. As a precaution, draft proposals circulated for comment and/or vote shall display the symbol ©, followed by the year and “JEDEC”. Stapled or bound documents require this designation only on the first page or title page; short documents that may be distributed unstapled shall be so labeled on every page. When final documents are ready for publication, the JEDEC office shall register the copyright and maintain all appropriate records.

4 Document development procedure (cont'd)

4.1 Copyrights (cont'd)

JEDEC member companies may reproduce any JEDEC document for internal use, without restriction. Use of JEDEC material outside of member companies is at the discretion of the Board. Generally, all JEDEC documents are available on the JEDEC website: www.jedec.org.

If, in developing a standard, a publication, or a specification, a committee proposes to incorporate verbatim material from a publication copyrighted by another organization, the committee shall obtain written permission from the owner of the copyright for JEDEC to copy the material. The letter granting permission shall be sent to the JEDEC office, and the standard or publication shall include a reference to such permission as a footnote.

5 Voting

JEDEC shall formally operate under the rule of “One company, one vote” wherein all formal, binding votes will be restricted to one vote per company. Nonbinding fact-finding “straw” or survey votes are not considered formal votes. Unless specifically authorized by the Board, all approval vote counts within JEDEC shall be a minimum of 2/3 of votes cast. All Board approval vote counts shall be a minimum of $\frac{1}{2}$ of votes cast. Abstention votes shall not be considered in the calculation.

Votes taken during committee meetings shall be duly recorded in the meeting minutes, and, except for unanimous votes, the vote count shall be included in those same meeting minutes.

In order to maintain fairness within every committee, the committee chairperson shall refrain from voting during a meeting for all but secret votes. If a chairperson has a specific company position on a topic being discussed, then control of the meeting should be turned over to the vice chairperson or other less biased member. Chairpersons may vote on any ballot to represent his/her company position.

5.1 Ballot voting

The period for voting on committee ballots shall be at least 21 calendar days from the date of issuance, and shall not exceed 90 days. In any case, the ballot closes at midnight, Eastern Time, on the final day of the voting period. All committee ballots shall be processed through the JEDEC electronic voting machine, and shall include the following vote options:

- a) approve, comments are optional with approval
- b) disapprove, comment is required and shall include a full explanation of the reason(s) for the disapproval
- c) abstain, comments are optional with abstain

NOTE All committee ballots shall contain the following patent statement:

“If anyone receiving this ballot is aware of any patents (granted or pending) involving in this ballot, check here and notify the committee, citing the applicable patent numbers.”

5 Voting (cont'd)

5.2 Ballot approval by acclamation

A committee ballot is considered approved by acclamation in either of the following two cases:

- a) The ballot is approved unanimously with no comment at the close of the voting period.
- b) The ballot is approved by count at the end of the voting period, and all comments whether from approve, disapprove, or abstain votes are resolved to the satisfaction of the sponsor and the commenting company. If any company is not satisfied with the proposed resolution of a comment, then resolution of the ballot must await committee action.

Any ballot approved by acclamation shall automatically advance to the next level in the publication process (i.e., committee ballots are automatically submitted to the Board, or Board ballots automatically become approved for publication). At the discretion of the committee chairperson, ballots that otherwise meet the requirement for approval by acclamation may be referred back to committee for further action if special conditions exist (e.g., uncharacteristically low vote count for the committee).

6 Ballots

All committee ballots shall be distributed ONLY by the JEDEC office with Board-approved electronic distribution methods to all committee members and alternates for vote and to all related committees for information and comment. A submission for ballot shall be made through the JEDEC office ONLY by Board approved editable and non-editable “soft copy” format of the complete ballot content.

Reference to any individual(s) and/or member company name(s) is prohibited from appearing on any committee ballot unless it is part of a return address.

In order to facilitate document identification and retrieval, keywords shall be submitted with all ballots. A keyword is defined as a word, term, or acronym that is descriptive of the essential contents of the ballot or a major portion thereof.

6.1 Editorial changes

During a committee meeting, provided there is no disagreement within the committee that the changes are editorial, these changes may be incorporated into committee-approved balloted material without reballoting.

6.2 Ballot lobbying

Member companies should not lobby or coerce other member companies to approve or disapprove ballots. Open discussion of balloted material is permitted and encouraged, but such discussions should focus on the technical aspects of balloted material.

6.3 Copyrights

See 4.1

6 Ballots (cont'd)

6.4 Regular committee ballot

A “regular” ballot is one in which the entire standard, publication, registration, guideline, or specification is open for comment.

Prompt consideration shall be given to the written comments and objections of all participants during the committee balloting process. An effort to resolve all expressed objections accompanied by comments related to the proposal under consideration shall be made, and the disposition of each such comment or objection and the reasons therefore shall be documented in writing (including electronic minutes and ballot material).

6.5 Limited committee ballot

If a limited number of revisions to an existing document are being proposed, a “limited” ballot may be issued. Limited ballots may be restricted to considering only the proposed areas for modification, addition, or deletion. In the cases of limited ballots both the original material and the proposed revisions thereto shall be clearly shown in the ballot material. Examples of appropriate occasions for using limited ballots are (1) a proposal to add a new definition to a long list of definitions or (2) a new package outline to JEDEC Publication No. 95.

On occasion, after a committee ballot has been approved, the committee may wish to propose minor technical changes to the ballot before forwarding the approved material on to the Board for final consideration. In such cases, a motion may be made for a limited ballot in which only these technical changes may be addressed. If the limited ballot is passed, these changes shall be incorporated. If it fails, the original material stands as approved.

6.6 Board of Directors ballot

In general, all ballots originating at the Board level shall follow the same guidelines outlined in 6.4. Board ballots are restricted in scope to non-technical Association business and specifically may not include new technical for publication creation as such material must first be submitted by the appropriate technical committee.

6.6.1 Committee ballots sent to the Board of Directors

All passed committee ballots relating to proposed JEDEC standards, guidelines, or specifications must be reviewed and approved by the JEDEC Board before becoming official JEDEC publications. Upon approval by acclamation or by committee vote⁴, the originating committee shall submit such passed committee ballot to the JEDEC office for distribution as a Board ballot.

⁴ Unless the committee ballot passes by acclamation, a formal committee vote must be taken and recorded in the minutes to send the committee ballot to the Board for further action.

6.6 Board of Directors ballot (cont'd)

6.6.1 Committee ballots sent to the Board of Directors (cont'd)

All ballots submitted to the JEDEC Board must include the committee ballot material, and:

- a) a brief description of the recent committee background regarding the material.
- b) the complete voting report including the names and votes of the member companies voting and all comments on the material.
- c) a description of the resolution of all of the comments on the material. Negative votes must be addressed, however if they cannot be resolved, the ballot can be submitted to the Board with the approval of the committee.

The Board may make only editorial modifications to any material proposed by committee for further action. Any technical modifications of committee material must be referred back to the originating committee for possible action.

6.7 Survey ballots

Surveys may be issued to determine whether a proposal warrants further action. A survey may ask for information or for a support/nonsupport position. No committee vote is required for the distribution of a survey ballot; however, every survey must be approved by the committee chairperson and issued by the JEDEC office following legal approval. The JEDEC office shall monitor every survey to ensure adherence to JEDEC legal guidelines. Surveys that contain company-sensitive material that must remain confidential shall be stripped of any reference to a company by the JEDEC office prior to use of the material. In all cases, survey results shall be presented to the full committee at the first meeting following the voting period expiration date.

Survey ballots are for gathering information or further clarifying member positions and survey votes are strictly nonbinding. All surveys should contain the following background statement:

“Companies are under no obligation to respond to this survey.”

The committee shall determine the method of data collection to ensure company confidentiality if required. In the case of anonymous surveys, the names of respondents shall be deleted by the JEDEC office. The survey shall specify the method of data-collection.

7 JEDEC documents

JEDEC documents are available from the JEDEC website: www.jedec.org. JEDEC documents may not be sold without written authorization from JEDEC.

7.1 Interpretation

Official interpretations involving technical matters pertaining to JEDEC and/or ANSI/JEDEC standards and publications shall be made by the formulating committee of the document in question.

7.2 Document Maintenance

JEDEC documents shall be reviewed by the formulating committee within five years of the last publication date, after which the committee shall take one of the following actions with respect to the standards material:

- a) Reaffirm it as a JEDEC document
- b) Recommend its revision and reissuance as a JEDEC document
- c) Recommend its rescission
- d) Recommend its consideration as an ANSI or IEC document proposal.

7.3 Document Types**7.3.1 Standards (JESD)**

Documents that are intended to represent a sound approach to product specification and application.

7.3.2 Publications (JEP)

Documents containing general engineering information on products, procedures, or services, that are not necessarily appropriate for standardization.

7.3.3 Specifications (JES)

Documents prepared specifically to facilitate procurement, that clearly and accurately describe the essential technical requirements for purchased material or services.

7.3.4 Registered Outlines (TO, MO, CO, PO, etc.)

Mechanical package outline drawings that have been registered and assigned a JEDEC registration number.

7.3.5 Registration Data Formats (RDF)

Engineering information in the form of a list of specific electrical and mechanical parameters necessary for the characterization of a particular class of solid state devices.

7.3 Document Types (cont'd)

7.3.6 Manuals (JM)

Documents that describe internal JEDEC policies and procedures.

7.3.7 Joint Documents (J-STD, JP, and JS)

Documents created in cooperation between JEDEC and another organization.

7.3.8 ANSI/JEDEC Standards

At the request of the sponsoring committee and after approval by Board ballot, JEDEC standards and publications may be submitted to ANSI through the JEDEC office for processing as an ANSI National Standard. The JEDEC office will be responsible for providing appropriate documentation to ANSI. All policies and procedures set forth by ANSI per the “ANSI Essential Requirements: Due Process Requirements for American National Standards” shall be followed. See Annex C for more details.

8 Legal guidelines

All meetings of the JEDEC Board and its associated committees, subcommittees, task groups, and other units shall comply with JEDEC Legal Guidelines incorporated herein by reference. JEDEC Legal Counsel may advise the Board and committees from time to time concerning interpretation of Legal Guidelines.

8.1 JEDEC documents and publications

Prior to publication, the following documents including, but not limited to, all JEDEC standards, publications, specifications, manuals, minutes, surveys, questionnaires, press releases, registration data formats, and workshop proceedings, formulated by the Board, committees, and subcommittees, must be approved by JEDEC Legal Counsel.

8.2 Reference to patented products in JEDEC standards and publications

JEDEC standards and non-product registrations (e.g., package outline drawings) that require the use of patented items should be considered with great care. (For the purpose of this policy, the term “patented items” includes items and processes for which a patent has been applied.) While there is no restriction against drafting a proposed standard in terms that include the use of a patented item if technical reasons justify the inclusion, committees should avoid standardization that refers to a product on which there is a known patent unless all the relevant technical information covered by the patent is known to the formulating committee, subcommittee, or task group.

If the committee member indicates a reasonable belief that the proposed standard may require the use of patented items, then the committee chairperson must promptly request a written assurance from the patent owner or applicant. The written assurance must state that, in the event that the patent or patent application is required, licenses will be made available to applicants desiring to implement (e.g., including to use) the proposed standard, either with or without compensation, under reasonable terms and conditions that are demonstrably free of any unfair discrimination.

8 Legal guidelines (cont'd)

8.2 Reference to patented products in JEDEC standards and publications (cont'd)

If the committee chairperson does not receive the written assurance from the patent owner or applicant within a reasonable time after the request is made (generally not to exceed three (3) months), the committee may refer the matter to the Board, in the form of a Board ballot, refer to 8.3⁵.

Additionally, when a known patent item is referred to in a JEDEC standard, a cautionary note, as outlined in this document, shall appear in the JEDEC standard.

All correspondence between the patent holder and the formulating committee, including a copy of the written assurance from the patent holder discussed above, shall be transmitted to the JEDEC office and JEDEC Legal Counsel at the earliest possible time and, in any case, before the standard is otherwise ready for committee ballot circulation. (See JEDEC Style Manual, JM7, for the required language in a JEDEC standard that cites a product with a known patent.)

The following notice shall be included inside the front cover of all JEDEC documents or publications in which patents are or may be involved:

“The user’s attention is called to the possibility that compliance with this document may require use of an invention covered by patent rights.”

“By publication of this document, no position is taken with respect to the validity of this claim or of any patent rights in connection therewith. The patent holder has, however, filed a statement of willingness to grant a license under these rights on reasonable nondiscriminatory terms and conditions to applicants desiring to obtain such a license. Details may be obtained from the publisher.”

In addition, a footnote should be included on each page that has a reference to a patented item as follows:

“Compliance with this section of the document requires the use of patent No. □□□□□□, □□□□”

or

“The formulating committee believes that a patent covering elements involved in this section has been applied for. The applicant, □Y□ Association, has agreed to (license without royalty) (license under reasonable terms demonstrably free of discrimination).”

8.3 Special legal disclaimer

In exceptional situations, the Board has the discretion to approve the issuance of a standard for which a patent owner or applicant has not provided written assurance that the relevant patent or patent application will be licensed, subject to special legal disclaimers.

When determining whether to approve the issuance of a standard, the Board shall consider whether the committee used diligent efforts, if appropriate under the circumstances, to develop a standard or specification that does not require the use of the patented item.

⁵ A referral by a committee under 8.2 triggers the review by the Board under 8.3.

8 Legal guidelines (cont'd)

8.3 Special legal disclaimer (cont'd)

A special legal disclaimer might include the following language: “Notice: JEDEC has received information that certain patents or patent applications may be relevant to this standard. However, as of the publication date of this standard, no statements regarding an assurance or refusal to license such patents or patent applications have been provided. JEDEC does not make any determination as to the validity or relevancy of such patents or patent applications. Prospective users of the standard should act accordingly.”

If the Board determines that:

- 1) a claim of a patent or patent application may be required to implement a standard, and
- 2) there is a credible indication that the patent owner or applicant is unwilling or unable to grant licenses, with or without compensation, on reasonable and nondiscriminatory (RAND) terms,

then the Board shall not approve the issuance of the standard.

8.4 Committee responsibility concerning intellectual property

The chairperson of any JEDEC committee must call to the attention of all those present the requirements contained in the JEDEC Legal Guides and the obligation of all participants to inform the meeting of any knowledge they may have of any patents, or pending patents, that might be involved in the work they are undertaking. Annex A provides information to be displayed at the beginning of the meeting to satisfy the requirement. Additionally, all participants must be asked to read the statement on the back of each JEDEC sign-in/attendance roster; see Annex B for patent policy application guidelines.

9 Appeals

All appeals related to standard or bulletin development are initially directed to the JEDEC office. The provision for appeals is important for the protection of all parties involved within the JEDEC standards development process. An appeals mechanism safeguards both those who are directly and or materially affected by the process and the standards developing organization. The following appeals procedures shall be used for actions taken within the JEDEC standards process for the development of ANSI/JEDEC standards and publications.

9.1 Right of appeal

Persons who have directly and or materially affected interests and who have been or will be adversely affected by a standard or publication within ANSI jurisdiction have the right to appeal substantive or procedural actions or inactions of JEDEC formulating groups.

The burden of proof to show an adverse effect shall be on the appellant. Appeals shall be directed to the JEDEC office in accordance with the appeals procedures as defined in this section.

9 Appeals (cont'd)

9.2 Criteria for appeals mechanism

The following general criteria are encompassed in these appeals procedures:

- a) Appeals shall be addressed promptly and a decision made expeditiously;
- b) The right of the involved parties to present their cases shall not be denied;
- c) These procedures shall provide for participation by all parties concerned without imposing an undue burden on them;
- d) Consideration of appeals shall be fair and unbiased and shall fully address the concerns expressed; and
- e) Records of appeals shall be kept and made available upon request. The JEDEC office may levy an appropriate charge to cover the cost of reproduction, handling, and distribution of materials.

9.3 Appeals procedures

The following subsections outline the JEDEC Appeals Procedures. In the case of an appeal to ANSI of a JEDEC action or inaction on an ANSI/JEDEC standard, the appellant may waive the right of the JEDEC appeals process, see 9.4.

9.3.1 Complaints

The appellant shall file a written complaint with the JEDEC office within 30 calendar days after the date of the action being appealed or at any time with respect to inaction. The complaint shall state the nature of the objection(s) including any adverse effects, the section(s) of these procedures or the standard(s) that are at issue, action(s) or instances of inaction that are at issue, and the specific remedial action(s) that would satisfy the appellant's concerns. Previous efforts to resolve the objection(s) and the outcome of each shall be noted.

9.3.2 Response

Within 30 calendar days after receipt of the complaint, the respondent (formulating group chairman or JEDEC representative) shall respond in writing to the appellant, specifically addressing each allegation of fact in the complaint to the extent of the respondent's knowledge. Complaints that are technical in nature shall be referred to the appropriate JEDEC formulating committee having jurisdiction over the material for review and possible action. Complaints that are procedural in nature shall be referred to the JEDEC Board for review and possible action.

9.3.3 Hearing

If the appellant and the respondent are unable to resolve the written complaint informally in a manner consistent with these procedures within 15 calendar days, the JEDEC office shall schedule a hearing with an appeals panel on a date agreeable to all participants but within 30 calendar days, giving at least 10 calendar days notice. Hearing on the complaint will take place at the next regular meeting of the JEDEC formulating committee or the JEDEC Board depending on the nature of the complaint.

9.3 Appeals procedures (cont'd)

9.3.4 Conduct of the hearing

The appellant has the burden of demonstrating adverse effects, improper actions or inactions, and the efficacy of the requested remedial action.

9.3.5 Decision

The appeal disposition shall be documented by the formulating committee for technical matters and by the JEDEC Board for procedural matters. A record of the appeals shall be kept by JEDEC and made available to the involved parties.

If, for whatever reason(s), the appellant chooses to forego the process detailed above, the JEDEC office shall maintain all documents pertaining to JEDEC attempts to resolve the matter at hand. These documents may be used in any further appeals proceedings.

9.4 Further appeal

If the matter under appeal relates to a JEDEC standard that has been or is expected to be recognized as an American National Standard, subsequent further appeal may be made directly to ANSI. If the appellant gives notice to the JEDEC office that further appeal to ANSI is intended, a full record of the complaint, response and decision shall be submitted by the JEDEC office to ANSI.

NOTE ANSI will not normally hear an appeal of an action or inaction by JEDEC until the procedures have been completed. Such appeals shall be directed to ANSI in accordance with the procedures of the appropriate ANSI entity (e.g., Board of Standards Review, Executive Standards Council, etc.).

10 External publicity

All articles, presentations, news releases, or other publicity must be approved by JEDEC Legal Counsel prior to release.

Articles, speeches, and other presentations for publication or delivery by members of the Board, its committees, or JEDEC staff that cover specific JEDEC work or JEDEC policy or purports to speak on behalf of JEDEC must be approved by the Board, if time permits; otherwise by the Board chairperson who shall be responsible for ensuring that the content is accurate and reflects current JEDEC policy. Any publicity that speaks for the Board shall require similar approval.

The committee chairperson may talk to the press and approve technical and tradeshow presentations about ongoing committee work when it is appropriate to promote a particular standard or the work of the committee. This public disclosure should be limited to the goal of the standard under development and any details of the standard that have been approved by committee ballot(s).

Companies may not advertise or give press releases stating that their products comply with a JEDEC standard, publication, or registration prior to Board approval of the documents.

11 JEDEC ethics rules for electronic communications

No JEDEC member or alternate shall post to an e-mail reflector, bulletin board, or Web site owned or sponsored by JEDEC, any of the following:

- a) any advertising or marketing information,
- b) any cost or pricing information,
- c) any proprietary information,
- d) any non-JEDEC copyright information or material that is in excess of that allowed under current USA copyright laws,
- e) any technical information that requires a USA government export license before it is transferred outside of the United States,
- f) information covered by USA secrecy laws,
- g) solicitations, or requests for contributions to “for profit” or “non-profit” (charitable) organizations,
- h) chain letters,
- i) job search or hiring information,
- j) computer games or other software products,
- k) files with known software viruses,
- l) offensive material covering:
 - 1) libel (i.e., false or malicious statements),
 - 2) threats, retaliation, or intimidation,
 - 3) use of language that is obscene or in poor taste, including jokes,
 - 4) sexual harassment or inappropriate sexual content, such as pictures, images, messages, or cartoons,
 - 5) discriminatory communication relating to race, color, national origin, sex, marital status, sexual orientation, age, veteran’s status, disability, religious or political beliefs.

All electronic communications and posting must comply with this JEDEC Manual and the JEDEC Legal Guides.

Annex A (normative) Legal guidelines summary

A.1 EIA/JEDEC patent policy summary

Standards that call for use of a patented item or process may not be considered by a JEDEC committee unless all of the relevant technical information covered by the patent or pending patent is known. In addition, the chairperson must have received written notice from the patent holder or applicant that one of the following conditions prevails:

- A license shall be made available without compensation to all applicants desiring to utilize the patent for the purpose of implementing the standard(s),

or

- A license shall be made available to all applicants under reasonable terms and conditions that are demonstrably free of any unfair discrimination.

However see, JM21M, 8.3 for additional information.

A.2 Copyright material

If, in developing a standard, a publication, or a specification, a committee proposes to incorporate verbatim material from a publication copyrighted by another organization, it shall obtain written permission from the owner of the copyright for JEDEC to copy the material. The letter granting permission shall be sent to the JEDEC office, and the standard or publication shall include a reference to such permission as a footnote.

Annex B (informative) Patent policy application guidelines

The following points describe the application of the JEDEC patent policy:

B.1 Committee discussion of pending or existing patents is a permissible activity and is encouraged when the committee feels that the patented item or process represents the best technical basis for a standard.

B.2 Discussion of a pending or existing patent does not constitute an acknowledgment of the validity of the patent, because validity is based on prior art and determination of the company/individual that first made the invention or applied for the patent. The committee's concern is only with the technical merits of the patent and whether the technical proposal is a sound basis for standardization.

B.3 By its terms, the JEDEC patent policy applies with equal force to situations involving:

- a) the discovery of patents that may be required for use of a standard subsequent to its adoption, and
- b) the initial issuance of a patent after the adoption of a standard.

Once disclosure is made, the holder is obligated to provide the same assurances to EIA/JEDEC as are required in situations where patents exist or are known prior to approval of a proposed standard.

Thus, if notice is given of a patent that may be required for use of an already approved JEDEC standard, a standards developer may wish to make it clear to other standards-making participants that the JEDEC procedures require the patent holder to provide the assurances contained in the patent policy or suffer the withdrawal of JEDEC's approval of the standard as a JEDEC standard.

Annex C (informative) ANSI Standardization Procedures

For those documents that are intended for publication as an American National Standard (ANS), the provisions set forth in this annex apply.

C.1 Submission to ANSI for Public Review

Following approval of the standard, responsible JEDEC Standards staff shall submit the proposed ANS to ANSI to initiate public review. JEDEC Standards staff shall provide appropriate documentation to ANSI. Responsible JEDEC Standards staff shall receive, collect and acknowledge receipt of public review comments. In addition, responsible JEDEC Standards staff shall forward all public review comments to the formulating group for review and response. The response to each commenter shall include a notation of the JEDEC and ANSI appeals process.

NOTE—A proposed ANS is subject to comment only (not for vote) during public review and by any and all materially or directly affected parties.

C.2 Public Review Comments

JEDEC Standards staff shall acknowledge receipt of a public review comment, regardless of its nature. The only comments normally addressed by a working group or formulating group are editorial or technical in nature. Technical comments should be accompanied with wording that would aid the formulating group in addressing the comments.

Other comments may be handled in the following manner on behalf of the formulating group:

- * The JEDEC Legal Counsel shall respond to comments relating to legal concerns;
- * JEDEC Standards staff shall respond to comments relating to concerns regarding the standards development process;
- * The formulating group with input from JEDEC staff shall address scope concerns;
- * The reason for non-acceptance shall be sent regarding editorial or technical concerns;
- * Vague comments shall be returned to the respondent requesting expeditious clarification.

JEDEC Standards staff shall retain copies of response to commenters.

C.3 Public Review Commenter Response

The commenter shall have 14 calendar days after response to acknowledge the acceptance or rejection of that reply. If no response is received, the responsible JEDEC Standards staff shall send a reminder notice to the commenter requesting response. If no response is received within an additional 5 calendar days, the responsible JEDEC Standards staff will send a registered letter to the commenter noting the lack of response. The commenter's comments are then recorded as unresolved and circulated to the formulating group per the provisions of C.2.

All correspondence showing the formulating group's effort to address the comments, noting a lack of response when appropriate, shall be included in any package of materials provided to ANSI.

C.4 Results Scenarios

Results scenario #1: If no comments are received after the close of public review, the document shall be forwarded to ANSI with a request for approval.

Results scenario #2: If editorial comments are received by the close of public review, the document editor, editing group, or chair shall address the comments. The document, with edits, if any, shall be forwarded to ANSI for approval.

Results scenario #3: If substantive comments are received from public review, the working group or formulating group shall review these comments, and attempt to resolve them, and notify each commenter of said action (see C.3), along with a notification of the JEDEC and ANSI appeals process.

- a) If no substantive changes are made, the document is forwarded to ANSI for approval.
- b) If substantive changes are made, the formulating group shall conduct a recirculation vote/ballot and “second” public review (see C.3).
- c) If negative, substantive comments remain unresolved from public review, the formulating group shall conduct a recirculation vote/ballot, and, if necessary, a “second” public review (see C.3).

C.5 Voting on a American National Standard

When a vote in a formulating group is for the purpose of approving a document for publication as an American National Standard, a Ballot Summary (Tally of votes) shall be prepared and included in the minutes. The Interest Category is normally self-selected by the voting member.

Action Required	Method (all calendar days)	Approval Criteria
Meeting Vote	At the meeting	Two-thirds voting
Ballot	30 day ballot	Two-thirds voting
ANSI BSR8 (Public review)	Initial 60 day comment period [30 or 60 day subsequent comment period(s)] (or other ANSI designated time period where applicable)	Comments addressed by formulating group

C.6 Legal Approval

All ANSI/JEDEC standards shall receive JEDEC legal approval before publication.

C.7 ANSI Approval

If ANSI/BSR is approved, responsible JEDEC Standards staff is notified and in turn publishes the document.

If ANSI/BSR does not approve, comment resolution issues will be dealt with by the formulating group and process-related issues will be dealt with by JEDEC Standards staff. If the ANSI/BSR comments are resolved and the document is approved, responsible JEDEC Standards staff publishes the document.

If the comments cannot be resolved, the document is returned to the formulating group for further resolution or cancellation. The formulating group may appeal the actions of the ANSI/BSR.

C.8 ANSI Patent Policy

If a JEDEC standard is intended for an American National Standard, then the standard must comply with the current ANSI patent policy.



Exhibit J

JEDEC MANUAL

JEDEC Manual of Organization and Procedure

JM21P

(Revision of JM21N, May 2008)

MAY 2010

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or call (703) 907-7559 or www.jedec.org

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JEDEC MANUAL OF ORGANIZATION AND PROCEDURE**Contents**

	Page
1 JEDEC	1
1.1 Mission	1
1.2 Scope	1
1.3 Membership	1
1.4 Board of Directors	2
1.4.1 Eligibility	2
1.4.2 Election of Directors	2
1.4.3 Member Company and Director resignation	3
1.4.4 Officers of the Board of Directors	4
1.4.5 Board of Directors meetings	4
1.4.5.1 Board of Directors Executive session	4
1.4.5.2 Board of Directors voting	4
1.4.5.3 Emergency action by the Board of Directors	4
1.4.6 Board of Directors guest policy	5
1.5 Governance/Interpretation	5
1.6 Scope of participation	5
1.6.1 Interest categories	5
1.6.1.1 Producer	5
1.6.1.2 User	6
1.6.1.3 General Interest	6
1.7 Limits and restrictions	6
1.8 Modifications to the Manual of Organization and Procedure	6
2 Committees	7
2.1 Committee responsibilities	7
2.2 Executive committee	8
2.3 Election of Officers	8
2.4 Government entities	9
3 Meetings	9
3.1 General requirements	9
3.2 Notices	9
3.3 Agendas	9
3.4 Meeting attendance	10
3.5 Quorum	10
3.6 Recording devices	10
3.7 Minutes	11
3.7.1 Policy statement on JEDEC sign-in/attendance rosters	12
3.8 Regular meetings	12
3.9 Special (Limited Scope)	12
3.10 Joint meetings	12
3.10.1 Between JEDEC Committees	12
3.10.2 Between JEDEC and any non-JEDEC organization	12
3.10.3 Memorandum of Understanding (MoU)	13
3.11 Task groups	13
3.11.1 Joint task groups between JEDEC committees	13
3.11.2 Joint task groups between a JEDEC committee and other organizations	14
4 Document development procedure	14
4.1 Copyrights	15

JEDEC MANUAL OF ORGANIZATION AND PROCEDURE**Contents (cont'd)**

	Page
5 Voting	15
5.1 Ballot voting	16
5.2 Ballot approval by acclamation	16
6 Ballots	17
6.1 Editorial changes	17
6.2 Ballot lobbying	17
6.3 Copyrights (see 4.1)	17
6.4 Regular committee ballot	17
6.5 Limited committee ballot	18
6.6 Board of Directors ballot	18
6.6.1 Committee ballots sent to the Board of Directors	18
6.7 Survey ballots	19
7 JEDEC documents	19
7.1 Interpretation	19
7.2 Document Maintenance	19
7.3 Document Types	20
7.3.1 Standards (JESD)	20
7.3.2 Publications (JEP)	20
7.3.3 Specifications (JES)	20
7.3.4 Registered Outlines (TO, MO, CO, PO, etc.)	20
7.3.5 Registration Data Formats (RDF)	20
7.3.6 Manuals (JM)	20
7.3.7 Joint Documents (J-STD, JP, and JS)	20
7.3.8 ANSI/JEDEC Standards	20
8 Legal Guidelines	21
8.1 JEDEC documents and publications	21
8.2 Patent policy	21
8.2.1 Terms and definitions	21
8.2.2 General provisions	23
8.2.2.1 Committee members	23
8.2.2.2 Committees	23
8.2.3 Disclosure of potentially essential patents	24
8.2.3.1 Disclosure of unwillingness to license work of a committee	24
8.2.4 RAND patent licensing commitment	25
8.2.5 Licensing assurance/disclosure form	25
8.2.6 Reference to patented products in JEDEC standards and publications	26
8.2.7 Special legal disclaimer	26
8.2.8 Miscellaneous	27
8.2.9 Violations	27
8.2.10 Interpretation and governing law	27

JEDEC MANUAL OF ORGANIZATION AND PROCEDURE

Contents (cont'd)

	Page
9 Appeals	28
9.1 Appeals related to ANSI/JEDEC standards and publications	28
9.1.1 Right of appeal	28
9.1.2 Criteria for appeals mechanism	29
9.1.3 Appeals procedures	29
9.1.3.1 Complaints	29
9.1.3.2 Response	29
9.1.3.3 Hearing	29
9.1.3.4 Conduct of the Hearing	29
9.1.3.5 Decision	29
9.1.4 Further appeal	30
9.2 Appeals not related to ANSI/JEDEC standards and publications	30
9.2.1 Right of appeal	30
9.2.2 Criteria for appeals mechanism	30
9.2.3 Appeals procedures	31
9.2.3.1 Complaints	31
9.2.3.2 Response	31
9.2.3.3 Hearing	31
9.2.3.4 Conduct of the Hearing	31
9.2.3.5 Decision	31
10 External publicity	32
11 JEDEC ethics rules for electronic communications	32
Annex A (normative) Legal Guidelines Summary	34
A.1 JEDEC patent policy summary	34
A.2 Copyright material	34
A.3 License assurance/disclosure form	34
A.4 Notice of refusal to offer license and RAND terms	37
Annex B (informative) Patent policy application guidelines	39
Annex C (informative) ANSI Standardization Procedures	40
Annex D (normative) Committee specific additional policies	44
D.1 JC-11 Committee	44
D.2 JC-16, JC-42, JC-45, and JC-63 Committees	49
D.3 JC-40 Committee	51
D.4 JC-64 Committee	54

JEDEC MANUAL OF ORGANIZATION AND PROCEDURE

(From JEDEC Board Ballot JCB-02-31A, JCB-04-75, JCB-04-89, JCB-05-60, JCB-05-103, JCB-05-124, JCB-05-99C, JCB-06-02, JCB-06-36, JCB-08-11, JCB-09-65, JCB-09-73, JCB-09-82, JCB-09-86, JCB-10-15, and JCB-10-21, formulated under the cognizance of the JEDEC Board of Directors.)

1 JEDEC

JEDEC is an independent incorporated Association governed by a Board of Directors (Board). The Association facilitates standardization within the solid state technology industry and other related activities through special purpose committees.

The Association and its members are committed to foster open competition in the development of products and services.

JEDEC is a founding sector of the Electronic Industries Alliance (EIA).

1.1 Mission

The mission of JEDEC is to serve the solid state industry by creating, publishing, and promoting global acceptance of standards, and by providing a forum for technical exchange on leading industry topics.

1.2 Scope

The scope of JEDEC includes but is not necessarily limited to areas relating to (1) discrete solid state devices, (2) integrated circuits, (3) electronic modules, and (4) various manufacturing support functions.

1.3 Membership

Any company, organization, consumer, or individual conducting business that itself or through a related entity manufactures electronic equipment or electronics-related products, or provides electronics or electronics-related services, shall¹ be eligible for membership in JEDEC. Membership on a given committee shall be open to any JEDEC member company in good standing dependent solely on the dues structure defined by the Board². Government representatives may also participate as described in 2.4.

Each member company, organization, or individual shall be entitled to appoint one member and multiple alternates for each committee it joins. The member and alternates should be capable of making a technical contribution to the standards-setting process of the committee. To preserve the “one-company one-vote” concept within JEDEC, wholly-owned or majority-owned subsidiaries shall not be granted separate voting privileges within any single committee or subcommittee. The JEDEC Office shall maintain a list of all member companies and representatives for each committee.

¹ Special word usage. The word "shall" indicates a requirement; see JM7, Annex J.

² JEDEC membership is not a prerequisite to committee participation. Non-member participation fees will be charged. Before attending a JEDEC meeting, guests and non-members must agree to comply with all JEDEC rules and procedures, including the rules and procedures set forth in this Manual. Further details are available from the JEDEC Office. See 3.4.

1 JEDEC (cont'd)

1.3 Membership (cont'd)

All changes in committee membership shall be the responsibility of the member company, who shall so advise the JEDEC Office and the committee chairperson in writing or by electronic means.

NOTE Government regulations restrict the participation of non-U.S. Nationals at certain meetings. Every effort shall be made to notify member companies, well in advance, when a meeting will cover restricted topics.

1.4 Board of Directors

The governing body of JEDEC is the JEDEC Board of Directors (Board) which is comprised of individual Directors (or their alternates) representing JEDEC member companies.

1.4.1 Eligibility

Any maximum dues paying Member Company of JEDEC, having an identified representative in two or more committees for at least the past two consecutive years, may nominate one candidate for Board membership. The nomination consists of the nominee's resume accompanied by a letter from a company executive to the Board chairperson (in care of the JEDEC Office). The support letter is to request that the nominee be considered for Board membership and committing that if elected the member company will support the nominee's active attendance and participation in JEDEC Board meetings and affairs. If the application meets the above requirements, the JEDEC Office will hold the application on file with other (qualified) nominees. The JEDEC Office will maintain an official list of nominations to the Board. A list of the current Board Committees with a brief description and the membership of each will be sent to the nominee with an invitation for the nominee to participate where he/she has interest.

Seats on the Board are occupied by Directors representing individual JEDEC Member Companies. Once elected to a Seat on the Board, the Member Company maintains its position until the seat is voluntarily relinquished or forfeited due to other events as outlined in 1.4.3. Mergers, divestitures, acquisitions and other corporate changes that do not substantially alter the nature of a member company will not be grounds to forfeit a seat on the Board so long as the new entity continues to meet all Board Eligibility Requirements.

The total number of Directors shall not exceed thirty (30).

1.4.2 Election of Directors

The Membership Committee (chaired by appointment of the Chairman of the Board with membership open to any Board Member) shall review with the Board circumstances of a vacated seat and recommend qualified nominees from the official nominations list. In order to choose an appropriate nominee to fulfill objectives of the Board, the Membership Committee will review activities that are being conducted in active Board Committees with their respective Chairs.

1.4 Board of Directors (cont'd)

1.4.2 Election of Directors (cont'd)

The following process will occur:

- Board Committee Chairs will be informed of the vacant seat by the Membership Committee.
- It will be the responsibility of the Membership Committee to qualify the level of support required to achieve ongoing Board Committee objectives.
- The Membership Committee will compile inputs and prepare a review to the Board at the next Board meeting including a recommendation on how to fill any vacated seats.

The following procedures and guidelines will be employed by the Membership Committee during the preparation of its Director recommendations:

- Gathering of Board Committee Chair inputs on current activities and resource requirements. Chairs will have an opportunity to review with the Membership Committee special requirements, shortcomings, etc. that should be made evident during the election process.
- Identification of the nominee's JEDEC experience and previous contributions. Tenure and amount of activity within a Committee or Task group will be identified.
- Identification of Board demographics in regards to representation of committees.
- Identification of the leadership qualities the candidate will bring to the Board.
- Identification of the unique value of the individual and the member company. (Value based on Committee Objectives identified to properly support JEDEC.)
- Identification of the individual's education and professional background (Engineering, Management, Finance, Marketing, Business development, etc.) and the balance the candidate will bring to the Board.

The Board will act on the recommendations of the Membership Committee. New Directors are elected to the Board by a 75% majority of the Board members voting at the meeting. There is no requirement that the maximum of 30 Seats be filled. The Membership Committee will send a response letter to the elected candidate/company and inform them of their responsibilities as outlined in this section. The elected Director's qualifications will be presented in regards to support as an active member on one or more of the Board Committees. The Board may stipulate a contingency period during which the newly-elected Director is required to serve on one or more Board Committees.

1.4.3 Member company and Director resignation

The Director will relinquish a position on the Board in the instance of any of the following events:

- 1) The Member Company formally resigns the position. This includes a statement from the Member Company that confirms the Director and Member Company resignation.
- 2) The Member Company which the Director represents is no longer eligible as defined in 1.4.1.
- 3) The Member Company is removed by a majority vote of the Board for gross violation of JEDEC policy.
- 4) The Director is absent from and not represented by a Member Company's approved alternate at two consecutive Board meetings within a calendar year. Participation via teleconference is allowed only once per calendar year.

1.4 Board of Directors (cont'd)

1.4.3 Member company and Director resignation (cont'd)

In the event that a Director no longer represents the Member Company for which the individual was elected (including but not limited to retirement or change of employment) or should the Director be removed due to gross violation of JEDEC policy outside of the control of the Member Company, then the Board seat shall not be considered vacated and the Member Company shall have the right to maintain its position on the Board by nominating a replacement Director. The replacement Director must meet all nomination requirements as set forth in 1.4.1 and be elected by the full Board by a 75% majority of the Board members voting at the meeting. Should the replacement Director fail to be elected, the Member Company may submit a second candidate and repeat the process.

1.4.4 Officers of the Board of Directors

The officers of the Board shall follow the same guidelines as the officers of a committee with the following exceptions: There shall be at least one Vice Chairperson on the Board. The number of Vice Chairpersons on the Board shall be determined by regular vote at any regularly scheduled Board meeting.

1.4.5 Board of Directors meetings

All meetings of the Board shall follow the same procedures and guidelines as outlined for regular committee meetings, with exceptions per 1.4.5.1, 1.4.5.2, and 1.4.5.3.

1.4.5.1 Board of Directors executive session

The needs of the Association occasionally require the Board to meet in executive session. Such executive sessions are to be defined as closed meetings of Board member company representatives and guests invited for specific purposes only.

1.4.5.2 Board of Directors voting

All actions within the Board require an affirmative vote of at least 75%; members abstaining shall not be considered for determination of the 75% criterion. When defined and agreed to by a duly recorded vote of the Board, specific action may require polling of all members whether present or not and/or may require a higher percentage affirmative vote.

1.4.5.3 Emergency action by the Board of Directors

If action normally requiring Board consideration must be taken, and a meeting cannot be reasonably convened, then the following modifications apply to the approval process: 1) A reasonable attempt must be made to notify 100% of Board members, and 2) The decision shall become binding only upon receipt by the JEDEC Office of affirmative votes from 75% of the members of the Board.

1.4 Board of Directors (cont'd)

1.4.6 Board of Directors guest policy

All guests must be approved by the chairman and must have a purpose related to the topics of discussions at the Board meeting. The guest must be introduced to the Board at the meeting and the purpose of the guest's visit should be stated in the agenda for that meeting.

At the discretion of the Board, a guest may be allowed to stay beyond the allotted time slot if the Board feels there is a need for that guest's continued attendance. Otherwise, all guests may only attend the portion of the Board meeting that is directly related to their purpose in the meeting. At no time may a guest speak to the Board beyond the intended purpose of his/her invitation without the explicit approval of the Board.

At anytime, any member of the Board may request that the chairman, at his discretion, ask a guest to leave the meeting.

1.5 Governance/Interpretation

The Board shall have the sole authority to interpret, in whole or in part, these operating procedures. In any case where conflict arises from ambiguity, or lack of specificity, or misunderstanding within or related to this document, the officers of the Board of the Association may make temporary rulings to be confirmed or modified at or before the next regularly scheduled Board meeting by vote of the Directors. In any case where there is not agreement between 100% of the officers of the Board concerning an interpretation, then the matter must be referred to the entire Board for resolution.

1.6 Scope of participation

The standards development process shall not be dominated by any single interest category, individual, or organization. Dominance means a position or exercise of dominate authority, leadership, or influence by reason of superior leverage, strength, or representation to the exclusion of fair and equitable consideration of other viewpoints.

The standards development process should have a balance of interests. Participants from diverse interest categories shall be sought with the objective of achieving balance.

NOTE In the case of an ANSI American National Standard, JEDEC shall comply with the criteria for balance as contained in ANSI Essential Requirements.

1.6.1 Interest categories

For a formulating group to work effectively, all interest categories should be represented, and no interest category shall be intentionally excluded. Because standards development depends on consensus rather than the will of a majority, participation in the consensus-building process is of far greater significance than the final act of voting in a formulating group. Unless it is claimed by a directly and materially affected interest that a single interest category dominated the standards development process, no test for dominance is required.

Interest categories are defined relative to each standards activity: producer; user; and general interest. See ANSI Essential Requirements for further information.

1.6 Scope of participation (cont'd)

1.6.1 Interest categories (cont'd)

1.6.1.1 Producer

Producers are formulating group members that manufacture electronic equipment or electronics-related products covered by the standard.

1.6.1.2 User

Users are members that utilize electronic equipment or electronics-related products covered by the standard to provide services to an end user.

1.6.1.3 General interest

General Interest members are neither producers nor users. This category includes, but is not limited to, regulatory agencies (state and federal), researchers, other organizations and associations, end users and consumers.

1.7 Limits and restrictions

The Members (particularly where they are direct competitors in certain lines of business, and including their employees and representatives), shall, when engaged in the activities and affairs of the Association, act in a manner that does not violate any state, federal or international laws or regulations.

Member companies must abide by all applicable export control regulations of their respective countries while attending a JEDEC meeting, irrespective of where the meeting is actually held. It is recommended that the member seek guidance from his or her company if involved in "state of the art" engineering work, as significant changes are made to the export control regulations from time to time.

The Association prohibits any discussion on specific costs, prices, quantity or yield of production levels, methods or channels of distribution, markets, customers or any other topic, or any conduct that may be construed as a violation of antitrust laws. Each respective member company shall advise its respective participant representatives and employees on the importance of compliance with applicable state, federal or international antitrust laws or regulations and require the scope of any discussions or exchanges amongst representatives of Members and/or the Association, be limited to the mission and scope of the Association stated above.

1.8 Modifications to the Manual of Organization and Procedure

Modifications to this manual may be made in whole or in part, upon approval by the Board by the normal ballot process. Any changes to this Manual shall be distributed to the JEDEC membership at the earliest possible time upon adoption.

2 Committees

The Board shall have the authority to establish committees to perform any task(s) for the association. JEDEC committees (main and sub) shall be authorized only by the Board, and the Board shall approve the scope of each³. A main committee shall be designated by the prefix JC- plus a two-digit designator, such as committee JC-11. Main committees are separated into two types: (1) service committees, whose scope is limited to a specific subject that may impact several product types, and (2) product committees, whose scope is limited to a specific type product. For service committees, the first digit of the two-digit designator shall be the number 1, and for product committees, the first digit shall be the number 2 or higher.

When the main committee finds it necessary to divide its work into parts, subcommittees may be formed under the scope of the main committee and such subcommittees shall be designated by adding a period to the main committee number followed by a number or a number-and-letter designator (e.g., JC-42.3 or JC-42.3B).

Subcommittees shall have all the same authority and responsibilities as committees herein defined, except that a subcommittee scope shall be a subset of a committee scope, to be authorized, reviewed, and approved by the Board.

NOTE Participation shall be open to all persons who are directly and materially affected by the activity in question.

2.1 Committee responsibilities

Each committee shall have the authority to consider all matters within its approved scope, including but not limited to the following actions:

- a) Develop proposed standards, guidelines, registrations, and related technical publications for committee ballot.
- b) Authorize committee ballots on all matters within the committee's defined scope.
- c) Initiate proposals for Board ballots of previously approved committee ballots.
- d) Evaluate the results of all committee ballots, as well as comments on related Board ballots.
- e) Request approval of the Board to convert standards or publications into ANSI or IEC standards.
- f) Maintain liaison with other national and international organizations.
- g) Initiate press releases to announce a significant advancement in the work of solid state technology covered within the committee scope such as: registrations, standardization, or publication. All press releases are to be issued by the JEDEC Office after review and concurrence by the JEDEC Legal Counsel.

³ The committee scope shall go through the standard balloting process and must be completed within a reasonable timeframe and prior to any publication of a JEDEC document authored by the committee.

2 Committees (cont'd)

2.2 Executive committee

A JEDEC committee or subcommittee may form an executive committee to manage its administrative work. The executive committee shall meet the following criteria:

- a) The executive committee should be chaired by the committee or subcommittee chairperson and shall include as a minimum all chairpersons and vice chairpersons of that committee and its subcommittees.
- b) Meetings of the executive committee shall be open to any committee member who gives reasonable advance notice to the executive committee chairperson or secretary.
- c) Actions of the executive committee shall be limited to handling administrative matters dealing with such items as meeting schedule, meeting agenda, future meeting dates and locations, personnel requirements, proposed work priorities, and the like. Any decision made by the executive committee is subject to review and modification by the full committee at the request of any committee member or alternate. Decisions on the final disposition of all technical matters shall be made only by the overseeing committee. Recommendations concerning future meeting dates and locations should be presented to the overseeing committee.

2.3 Election of officers

All JEDEC committee officers shall be members or alternates of their respective committees. All JEDEC committees shall have a chairperson and may also have a vice chairperson as officer(s) of the committee. All officers shall be directly elected either by secret vote of the committee members present during a regular meeting or by ballot as determined by vote of the committee. Committee officers shall serve a term of two (2) years. The JEDEC staff shall count the secret ballot and announce the result at the meeting.

At least two meetings prior to the end of a chairperson's term, he/she shall appoint a nominating committee to propose candidates to fill the next term of office(s) for the committee. The committee's candidates must be presented to the full committee at the next meeting and nominations from the floor shall also be accepted. All nominees must agree to accept the additional responsibilities before they can be considered.

If any of the officers cannot fulfill his/her term then elections shall be held at the earliest opportunity of the committee members. Similarly, if a new committee is formed, then the chairperson shall be selected by vote of the members attending the first meeting as a first order of business of the committee. These special case elections shall become effective immediately.

2 Committees (cont'd)

2.4 Government entities

JEDEC desires and encourages the active participation in its standards-developing activities of all parties having a direct and material interest in the standards, including U.S. federal, state, and local government entities when they have such a direct and material interest via the JC-13 Committee, Government Liaison.

Contribution to the standards development process may take the form of liaison with appropriate formulating groups, participation in the ANSI public review process, and active participation in formulating groups.

3 Meetings

Communication between JEDEC member companies is essential for the work within the Association. All committees shall hold regular meetings for the purpose of conducting JEDEC business.

The use of teleconference or other electronic conferencing equipment is permitted for any type of JEDEC meeting.

3.1 General requirements

Every JEDEC meeting, regardless of type, shall be held in accordance with the directives contained within this manual and in accordance with all applicable laws.

All meeting notices, agendas, ballots, and minutes shall be distributed only by the JEDEC Office. All correspondence from the JEDEC Office shall only be by electronic means unless otherwise required by law. If a company requests distribution by other means, the JEDEC Office will charge a fee for such additional service as directed by the JEDEC Board. The JEDEC website, www.jedec.org, shall be the primary method of electronic communication.

3.2 Notices

Notices of regular meetings shall be distributed solely by the JEDEC Office no less than 28 calendar days prior to the start of such meeting, unless a “special” meeting is authorized by committee vote and the date and agenda for such meeting is fixed at a regularly scheduled meeting. Notices of such special meetings shall be distributed as soon as possible after said regular meeting and in no case less than 10 calendar days prior to the start of such special meeting.

3.3 Agendas

All meetings shall have prepared agendas distributed as soon as possible, but in no case less than 10 days prior to a meeting and should be included with the meeting notice if possible. All special meeting notices shall include the agenda at time of distribution of such notice.

3 Meetings (cont'd)

3.4 Meeting attendance

All JEDEC committee and subcommittee meetings are open to members, their designated alternates, and guests invited by the committee or subcommittee chairperson.

A JEDEC staff member or a designated alternate must be in attendance at every committee meeting. The duties of the staff person shall include but not be limited to taking minutes, advising the chairperson regarding the content of this manual and JEDEC legal policies and guidelines, and distributing the minutes. JEDEC staff attendance is not required at every subcommittee meeting.

A potential new member company may be a guest for one meeting with prior approval of the chairperson. A timely submission of such a request stating the purpose of attendance shall be given so that appropriate accommodations can be made. If there are any issues to be raised by a guest, those issues must be specified in the purpose statement.

Nonmembers may participate in committee meetings if they pay a nonmember participation fee, the fee shall be predetermined, fixed, and reasonable. A procedure for requesting a fee waiver or fee reduction shall be available. Nonmembers do not have the right to vote. Nonmembers should contact the JEDEC Office prior to the meeting date for further details.

Before attending a JEDEC meeting, guests and non-members must agree to comply with all JEDEC rules and procedures, including the rules and procedures set forth in this Manual.

3.5 Quorum

The JEDEC Office shall maintain a list of active members for the sole purpose of determining the quorum requirements for a committee meeting. An active member is defined as a member company that has been represented at either or both of the previous two consecutive regular meetings of the committee. Special meetings shall not be considered for the purpose of determining “active” member status. The quorum requirements shall be 50% by count of a committee’s active member list, but in no case shall the quorum requirement be greater than 20 member companies regardless of committee size. All committee member companies present at a meeting are counted toward quorum requirement.

3.6 Recording devices

Voice or video recording devices of any kind are forbidden at any type of JEDEC meeting.

3 Meetings (cont'd)

3.7 Minutes

The principal activities and attendees at all JEDEC meetings shall be duly recorded in meeting minutes. Meeting minutes shall be taken by the assigned JEDEC staff for that committee or by a substitute designated by the JEDEC staff. In the absence of a JEDEC staff person at a committee meeting, a temporary secretary may be assigned by the committee chairperson.

Minutes shall be termed “unconfirmed” until reviewed and confirmed by the committee chairperson and JEDEC Legal Counsel. In the interest of member company needs, minutes should be distributed to members and alternates within 14 calendar days after a meeting. If the chairperson is unable to review and confirm the minutes within that time, the JEDEC Office should distribute the unconfirmed minutes clearly labeled as unconfirmed minutes. Unconfirmed minutes shall be approved by JEDEC Legal Counsel prior to distribution. Confirmed meeting minutes from regular meetings shall be distributed no later than 28 days prior to the next regular meeting. Confirmed minutes from “special” meetings should be distributed as soon as possible after such special meeting and in no case less than 10 days prior to the next regular meeting.

At the end of each set of minutes the following statements shall appear:

“Reviewed/corrected and authorized for release” followed by the Chairperson’s and Secretary’s name and date.

Chairperson, Name / date

Secretary, Name / date

Confirmed Legal Approval Date

“This meeting was conducted in accordance with JEDEC Legal Guides and the JEDEC Manual of Organization and Procedure.”

For those situations where a report from an independent group is included in the minutes, for information purposes, then the following disclaimer may be added to the minutes:

“Disclaimer: All liaison, government, technical, and task group reports contained herein are believed to be accurate but the accuracy or completeness thereof is not guaranteed.”

Minutes of a task group meeting shall include a list of the attendees, the meeting agenda, a status review of the agenda items, and any final proposals including discussion related to the proposals. The time, the place, and any required follow-up should be included. Task group minutes are reported and approved as part of the minutes for the next meeting of the sponsoring committee.

3.7 Minutes (cont'd)

3.7.1 Policy statement on JEDEC sign-in/attendance rosters

The policy statements reproduced on the reverse side of the JEDEC sign-in/attendance rosters shall become an integral part of the minutes of all committee, subcommittee, and task group meetings; and a statement shall be included in the minutes indicating compliance with the foregoing policy.

3.8 Regular meetings

Every JEDEC committee shall set up an annual calendar for regular meetings at which any item covered under the scope of the committee may be discussed. Under the JEDEC guidelines, committees must hold at least one (1) regular meeting each year to retain status as an active committee.

3.9 Special (Limited Scope)

All JEDEC committees shall have the authority to approve meetings of limited scope. Schedule for the meeting and specific agenda items must be approved by formal vote during a regular committee meeting. During a limited scope meeting, no other committee business shall be conducted outside of the specific items on the previously agreed to agenda. Items shall not be added to the agenda of a special meeting.

3.10 Joint meetings

3.10.1 Between JEDEC committees

Joint meetings between two or more JEDEC committees may be authorized by agreement of the committees by vote. Selection of the joint meeting chairperson shall occur by vote of the committees' attendees. The joint chairperson shall ensure that all meeting notices, agendas, and minutes are distributed to the relevant JEDEC committees.

3.10.2 Between JEDEC and any non-JEDEC organization

Joint meetings between a JEDEC committee and any non-JEDEC organization are subject to the same requirements as 3.10.1. In addition, JEDEC Legal Counsel shall establish a Memorandum of Understanding (MoU), see 3.10.3, between the organizations and review all release of information from the meetings to any outside person or organization.

JEDEC committees may meet jointly with other organizations or agencies for the purpose of permanent or ongoing liaison. In these cases, those nonmembers attending the committee meeting are expected to pay their proportionate part of the total meeting costs. Apportionment of the meeting costs shall be agreed upon between the committee chair and the representatives of those groups participating in the meeting(s), subject to the approval of the JEDEC Board.

3 Meetings (cont'd)

3.10 Joint meetings (cont'd)

3.10.3 Memorandum of Understanding (MoU) with any non-JEDEC organization

Prior to the formation of a joint meeting/task group with a non-JEDEC committee, a Memorandum of Understanding (MoU) must be in effect between JEDEC and the other organization covering the following items:

- a) Balloting procedure (acceptance criteria, resolution of comments, and disapprovals),
- b) Patents procedure (including joint ownership),
- c) Distribution rights (copyright, use of association logos, available on JEDEC website without charge),
- d) Procedures for future revisions of the document(s),
- e) Selection of chairperson(s) and appointment of task group membership, and
- f) Meetings and related legal requirements (notices, agendas, motions, minutes, costs, etc.).

3.11 Task groups

A task group may be authorized by any committee chairperson for a specific non-continuing objective. The task group chairperson, appointed by the committee chairperson, shall be a member or alternate of the overseeing committee. Membership within a task group is open to any member or alternate of the committee within which the task group is formed. In addition, members of the task group may also be appointed by the task group chairperson from nonmember JEDEC companies with approval of the overseeing committee chairperson; appointment shall be based solely on ability to contribute to the work; however, all members of a task group shall conduct their work in accordance with this manual.

A task group is not permitted to hold any formal votes or establish any final results relative to standards, publications, or ballots. All task group activities shall be presented to the overseeing committee for review, modification, and approval in the form of reports generated from every task meeting. By duly recorded committee vote, committees may authorize a task group to issue ballots or other specific tasks as required, the specific exception being that committees cannot authorize a task group to conduct a formal vote. A task group must be dissolved upon completion of its objectives.

Scheduling of task group meetings is subject to approval of the sponsoring committee's chairperson, in order to avoid conflict with regularly scheduled meetings.

3.11.1 Joint task groups between JEDEC committees

Joint task groups between two or more JEDEC committees may be authorized by agreement of the committee chairpersons. Selection of the task group chairperson shall be part of this agreement and that chairperson must be a member or alternate of one or more committees involved in the task group. The task group chairperson shall keep all sponsoring committees on the distribution list for all meeting notices, agendas, and reports. Joint task groups between JEDEC committees shall comply with all other requirements for task groups.

3.11 Task groups (cont'd)

3.11.2 Joint task groups between a JEDEC committee and other organizations

Joint task groups between a JEDEC committee and other non-JEDEC organizations are subject to the same requirements as task groups per 3.11. Unless otherwise authorized by the Board and approved by JEDEC Legal Counsel, such joint task groups shall establish a Memorandum of Understanding (MoU), see 3.10.3, in the same manner as joint committees covered in 3.10.2.

4 Document development procedure

The development of all JEDEC documents shall follow the minimum sequential procedure outlined herein.

- 1) Presentation – initial showing or distribution of material proposed for publication. Presentations may occur at any regular meeting or special meeting if the limited scope and agenda include such information. Presentations may also occur entirely electronically without being at a meeting. An additional showing of material proposed for publication may be required.
- 2) Motion for ballot – may occur at any time after a presentation. The motion must have a second before being considered for vote. The company agreeing to second the motion for ballot should be willing to accept responsibility for sponsoring the material should the original sponsor be unable or unwilling to do so. The motion for ballot should be discussed after receiving a second and then a formal vote shall be taken.
- 3) All committee ballots shall be subjected to the committee's editorial process prior to being posted on the JEDEC voting machine.
- 4) Committee ballot – if approved, material shall be sent out to ballot through the JEDEC voting machine. Details of balloting procedure are covered in section 6.
- 5) Motion to Board ballot – if a ballot passes and all comments are addressed then a motion may be made to send the material on to the Board for further consideration and approval. Alternatively, the motion to forward the ballot to the Board is unnecessary if the ballot passes by acclamation, see 5.2.
- 6) Board ballot – when approved, the committee material shall be sent out to ballot through the JEDEC voting machine. Board ballots follow the same procedures as committee ballots, see 6.6.1(c). When reviewing material passed by committee, the Board primarily considers whether due process has been followed.
- 7) Publication – once proposed material has successfully completed all the above steps and obtained approval through the appropriate balloting processes, it is approved for publication.
- 8) All JEDEC documents shall be published by the JEDEC Office.

NOTE 1 Steps may be repeated as many times as required to satisfy the wishes of the member companies participating in the process.

NOTE 2 JEDEC Registrations are special-case publications that do not have to be reviewed by the JEDEC Board of Directors, and the registration procedure ends upon the completion of step 4 above.

4 Document development procedure (cont'd)

4.1 Copyrights

JEDEC owns the copyright to all documents created through JEDEC, and use of that copyrighted material is at the sole discretion of the JEDEC Board.

For the protection of member companies, all JEDEC publications and standards shall be copyrighted. As a precaution, draft proposals circulated for comment and/or vote shall display the symbol ©, followed by the year and “JEDEC”. Stapled or bound documents require this designation only on the first page or title page; short documents that may be distributed unstapled shall be so labeled on every page. When final documents are ready for publication, the JEDEC Office shall register the copyright and maintain all appropriate records.

JEDEC member companies may reproduce any JEDEC document for internal use, without restriction. Use of JEDEC material outside of member companies is at the discretion of the Board. Generally, all JEDEC documents are available on the JEDEC website: www.jedec.org.

If, in developing a standard, a publication, or a specification, a committee proposes to incorporate verbatim material from a publication copyrighted by another organization, the committee shall obtain written permission from the owner of the copyright for JEDEC to copy the material. The letter granting permission shall be sent to the JEDEC Office, and the standard or publication shall include a reference to such permission as a footnote.

5 Voting

JEDEC shall formally operate under the rule of “One company, one vote” wherein all formal, binding votes will be restricted to one vote per company. Nonbinding fact-finding “straw” or survey votes are not considered formal votes. Unless specifically authorized by the Board, all approval vote counts within JEDEC shall be a minimum of 2/3 of votes cast. All Board approval vote counts shall be a minimum of 3/4 of votes cast. Abstention votes shall not be considered in the calculation.

Votes taken during committee meetings shall be duly recorded in the meeting minutes, and, except for unanimous votes, the vote count shall be included in those same meeting minutes.

In order to maintain fairness within every committee, the committee chairperson shall refrain from voting during a meeting for all but secret votes. If a chairperson has a specific company position on a topic being discussed, then control of the meeting should be turned over to the vice chairperson or other less biased member. Chairpersons may vote on any ballot to represent his/her company position.

5 Voting (cont'd)

5.1 Ballot voting

The period for voting on committee ballots shall be at least 21 calendar days from the date of issuance, and shall not exceed 90 days. In any case, the ballot closes at midnight, Eastern Time, on the final day of the voting period. All committee ballots shall be processed through the JEDEC electronic voting machine, and shall include the following vote options:

- a) approve, comments are optional with approval
- b) disapprove, comment is required and shall include a full explanation of the reason(s) for the disapproval
- c) abstain, comments are optional with abstain

NOTE All committee ballots shall contain the following patent statement:

“If anyone receiving this ballot is aware of any patents (granted or pending) involving in this ballot, check here and notify the committee, citing the applicable patent numbers.”

5.2 Ballot approval by acclamation

A committee ballot is considered approved by acclamation in either of the following two cases:

- a) The ballot is approved unanimously with no comment at the close of the voting period.
- b) The ballot is approved by count at the end of the voting period, and all comments whether from approve, disapprove, or abstain votes are resolved to the satisfaction of the sponsor and the commenting company. If any company is not satisfied with the proposed resolution of a comment, then resolution of the ballot must await committee action.

Any ballot approved by acclamation shall automatically advance to the next level in the publication process (i.e., committee ballots are automatically submitted to the Board, or Board ballots automatically become approved for publication). At the discretion of the committee chairperson, ballots that otherwise meet the requirement for approval by acclamation may be referred back to committee for further action if special conditions exist (e.g., uncharacteristically low vote count for the committee).

6 Ballots

All committee ballots shall be distributed ONLY by the JEDEC Office with Board-approved electronic distribution methods to all committee members and alternates for vote and to all related committees for information and comment. A submission for ballot shall be made through the JEDEC Office ONLY by Board approved editable and non-editable “soft copy” format of the complete ballot content.

Reference to any individual(s) and/or member company name(s) is prohibited from appearing on any committee ballot unless it is part of a return address.

In order to facilitate document identification and retrieval, keywords shall be submitted with all ballots. A keyword is defined as a word, term, or acronym that is descriptive of the essential contents of the ballot or a major portion thereof.

6.1 Editorial changes

During a committee meeting, provided there is no disagreement within the committee that the changes are editorial, these changes may be incorporated into committee-approved balloted material without reballoting.

6.2 Ballot lobbying

Member companies should not lobby or coerce other member companies to approve or disapprove ballots. Open discussion of balloted material is permitted and encouraged, but such discussions should focus on the technical aspects of balloted material.

The use of verbal, physical or business threats, intimidation, harassment or coercion is unprofessional behavior and unacceptable conduct at or in connection with any activity sponsored by JEDEC, including committee and task group meetings.

6.3 Copyrights

See 4.1

6.4 Regular committee ballot

A “regular” ballot is one in which the entire standard, publication, registration, guideline, or specification is open for comment.

Prompt consideration shall be given to the written comments and objections of all participants during the committee balloting process. An effort to resolve all expressed objections accompanied by comments related to the proposal under consideration shall be made, and the disposition of each such comment or objection and the reasons therefore shall be documented in writing (including electronic minutes and ballot material).

6 Ballots (cont'd)

6.5 Limited committee ballot

If a limited number of revisions to an existing document are being proposed, a “limited” ballot may be issued. Limited ballots may be restricted to considering only the proposed areas for modification, addition, or deletion. In the cases of limited ballots both the original material and the proposed revisions thereto shall be clearly shown in the ballot material. Examples of appropriate occasions for using limited ballots are (1) a proposal to add a new definition to a long list of definitions or (2) a new package outline to JEDEC Publication No. 95.

On occasion, after a committee ballot has been approved, the committee may wish to propose minor technical changes to the ballot before forwarding the approved material on to the Board for final consideration. In such cases, a motion may be made for a limited ballot in which only these technical changes may be addressed. If the limited ballot is passed, these changes shall be incorporated. If it fails, the original material stands as approved.

NOTE This process is not intended for use in the development of an ANS.

6.6 Board of Directors ballot

In general, all ballots originating at the Board level shall follow the same guidelines outlined in 6.4. Board ballots are restricted in scope to non-technical Association business and specifically may not include new technical for publication creation as such material must first be submitted by the appropriate technical committee.

6.6.1 Committee ballots sent to the Board of Directors

All passed committee ballots relating to proposed JEDEC standards, guidelines, or specifications must be reviewed and approved by the JEDEC Board before becoming official JEDEC publications. Upon approval by acclamation or by committee vote⁴, the originating committee shall submit such passed committee ballot to the JEDEC Office for distribution as a Board ballot.

All ballots submitted to the JEDEC Board must include the committee ballot material, and:

- a) a brief description of the recent committee background regarding the material.
- b) the complete voting report including the names and votes of the member companies voting and all comments on the material.
- c) a description of the resolution of all of the comments on the material. Negative votes must be addressed, however if they cannot be resolved, the ballot can be submitted to the Board with the approval of the committee.

The Board may make only editorial modifications to any material proposed by committee for further action. Any technical modifications of committee material must be referred back to the originating committee for possible action.

⁴ Unless the committee ballot passes by acclamation, a formal committee vote must be taken and recorded in the minutes to send the committee ballot to the Board for further action.

6 Ballots (cont'd)

6.7 Survey ballots

Surveys may be issued to determine whether a proposal warrants further action. A survey may ask for information or for a support/nonsupport position. No committee vote is required for the distribution of a survey ballot; however, every survey must be approved by the committee chairperson and issued by the JEDEC Office following legal approval. The JEDEC Office shall monitor every survey to ensure adherence to JEDEC legal guidelines. Surveys that contain company-sensitive material that must remain confidential shall be stripped of any reference to a company by the JEDEC Office prior to use of the material. In all cases, survey results shall be presented to the full committee at the first meeting following the voting period expiration date.

Survey ballots are for gathering information or further clarifying member positions and survey votes are strictly nonbinding. All surveys should contain the following background statement:

“Companies are under no obligation to respond to this survey.”

The committee shall determine the method of data collection to ensure company confidentiality if required. In the case of anonymous surveys, the names of respondents shall be deleted by the JEDEC Office. The survey shall specify the method of data-collection.

7 JEDEC documents

JEDEC documents are available from the JEDEC website: www.jedec.org. JEDEC documents may not be sold without written authorization from JEDEC.

7.1 Interpretation

Official interpretations involving technical matters pertaining to JEDEC and/or ANSI/JEDEC standards and publications shall be made by the formulating committee of the document in question.

7.2 Document Maintenance

JEDEC documents shall be reviewed by the formulating committee within five years of the last publication date, after which the committee shall take one of the following actions with respect to the standards material:

- a) Reaffirm it as a JEDEC document
- b) Recommend its revision and reissuance as a JEDEC document
- c) Recommend its rescission
- d) Recommend its consideration as an ANSI or IEC document proposal.

7.3 Document Types

7.3.1 Standards (JESD)

Documents that are intended to represent a sound approach to product specification and application.

7.3.2 Publications (JEP)

Documents containing general engineering information on products, procedures, or services, that are not necessarily appropriate for standardization.

7.3.3 Specifications (JES)

Documents prepared specifically to facilitate procurement, that clearly and accurately describes the essential technical requirements for purchased material or services.

7.3.4 Registered Outlines (TO, MO, CO, PO, etc.)

Mechanical package outline drawings that have been registered and assigned a JEDEC registration number.

7.3.5 Registration Data Formats (RDF)

Engineering information in the form of a list of specific electrical and mechanical parameters necessary for the characterization of a particular class of solid state devices.

7.3.6 Manuals (JM)

Documents that describe internal JEDEC policies and procedures.

7.3.7 Joint Documents (J-STD, JP, and JS)

Documents created in cooperation between JEDEC and another organization.

7.3.8 ANSI/JEDEC Standards

At the request of the sponsoring committee and after approval by Board ballot, JEDEC standards and publications may be submitted to ANSI through the JEDEC Office for processing as an ANSI National Standard. The JEDEC Office will be responsible for providing appropriate documentation to ANSI. All policies and procedures set forth by ANSI per the “ANSI Essential Requirements: Due Process Requirements for American National Standards” shall be followed. See Annex C for more details.

8 Legal guidelines

All meetings of the JEDEC Board and its associated committees, subcommittees, task groups, and other units shall comply with JEDEC Legal Guidelines incorporated herein by reference. JEDEC Legal Counsel may advise the Board and committees from time to time concerning interpretation of Legal Guidelines.

8.1 JEDEC documents and publications

Prior to publication, the following documents including, but not limited to, all JEDEC standards, publications, manuals, minutes, surveys, questionnaires, press releases, registration data formats, and workshop proceedings, formulated by the Board, committees, and subcommittees, must be approved by JEDEC Legal Counsel.

8.2 Patent Policy

8.2.1 Terms and definitions

Affiliate: An entity owned or controlled by a Committee Member, or which controls or is under common control with a Committee Member for so long as such control exists.

NOTE For purposes of this definition, control means the ownership of greater than 50% of the voting securities of that Committee Member.

Committee Member: An entity that participates in a JEDEC committee and its Affiliates.

Contribution: Any submitted material, proposal or other submission offered by a Committee Member in the process of developing a Standard for the purpose of incorporating such submitted material, proposal, or other submission into a Standard, provided that such submitted material, proposal, or other submission either (a) exists in a tangible form of expression (including in electronic media); or (b) is a verbal statement that is memorialized in written documentation (such as a proposed Standard or submitted material) and is either confirmed or not objected to by such Committee Member within thirty (30) calendar days after its receipt of or access to such memorialization, including without limitation, via posting on the JEDEC website.

Disclosure of Potentially Essential Patents (to Disclose Potentially Essential Patents): Disclosure to JEDEC, in writing, in the following form:

- (a) for issued patents, disclose the patent owner, assignee (if available at time of disclosure) name, address and intellectual property rights (“IPR”) contact person; name or title of the patent; the patent number; the country or countries of issuance, and the Standard(s) on which the submitter of the disclosure believes an Essential Patent Claim may read,
- (b) for published applications, disclose the patent application owner, assignee (if available at time of disclosure) name, address and IPR contact person; name or title of the patent; the patent application number; the country or countries of filing, and the Standard(s) on which the submitter of the disclosure believes an Essential Patent Claim may read, and

8.2.1 Terms and definitions (cont'd)

- (c) for unpublished pending applications, disclose the name or title of the patent application, the patent application owner or assignee (if available at time of disclosure) name, address and the IPR contact person; the patent application number; the general subject matter of such unpublished application(s) and the Standard(s) on which the submitter of the disclosure believes an Essential Patent claim may read. Nothing herein precludes broader disclosure of unpublished patent applications on a voluntary basis or pursuant to a non-disclosure agreement.

Disclosure of a patent is deemed to include all patents claiming priority of a single filing. The listing of foreign equivalents is optional and at the discretion of the patent holder.

NOTE If any of a Committee Member's disclosed patent or patent application contains Essential Patent Claims which, if licensed, would require a payment of royalties or other material consideration to an unaffiliated third party, the Committee Member must also note this fact in its disclosure statement.

Essential Patent: A Patent containing one or more Essential Patent Claims.

Essential Patent Claims: Those Patent claims the use of which would necessarily be infringed by the use, sale, offer for sale or other disposition of a portion of a product in order to be compliant with the required portions of a final approved JEDEC Standard.

NOTE Essential Patent Claims do not include Patent claims covering aspects that are not required to comply with a JEDEC Standard, or are required only for compliance with sections that are marked "example," "non-normative," or otherwise indicated as not being required for compliance, or related to underlying enabling technologies or manufacturing techniques not specified in the standard.

Participate (Participated, Participation): (a) joining a JEDEC committee or task group involved in the development of or amendments to a Standard; or (b) attending more than one meeting of such committee or task group (in person or by telephone) within a one-year period. "Participate" includes being present at any point in a meeting of a committee or task group even if the individual or entity has not formally joined the committee or task group.

Patents: All classes or types of patents other than design patents (including, without limitation, originals, divisions, continuations, continuations-in-part, extensions or reissues), and applications for these classes or types of patents throughout the world.

Potentially Essential Patent: A Patent that is reasonably believed by a subject person to contain one or more Essential Patent Claims.

Potential Licensees: All JEDEC Committee Members and non-members.

RAND: Reasonable and non-discriminatory licensing terms and conditions.

Representative: An individual who represents a Committee Member. The term includes entities that have not formally joined the committee or task group, if they participate.

Standard: Standards include publications and package outlines, provided that they are adopted (or intended to be adopted) by the JEDEC Board of Directors and have the effect of Standards. Standards work includes activities in JEDEC committees and task groups.

NOTE Standards include both proposed and adopted JEDEC technical specifications.

8.2.2 General Provisions

8.2.2.1 Committee Members

All Committee Members, as a condition of committee membership or committee Participation, agree to abide by JEDEC rules and procedures, including this JEDEC patent policy (“Patent Policy”). This commitment also applies to entities that Participate in JEDEC Committees or task groups, whether or not they have formally joined as JEDEC members.

All Committee Members, as a condition of committee membership and participation, agree to Disclose Potentially Essential Patents, as set forth more fully in 8.2.3, and to offer to license their Essential Patent Claims to all Potential Licensees on RAND terms and conditions, if and as consistent with 8.2.3 and 8.2.4.

The disclosure and licensing obligations of Committee Members and Participants are limited to Standards developed in the particular JEDEC committees in which and while they Participate.

As JEDEC members, Committee Members and Representatives are encouraged, but not required, both to disclose their Potentially Essential Patents and to license their Essential Patent Claims on RAND terms and conditions for Standards developed in all other JEDEC committees in which they are not Committee Members. Such disclosure shall be in the format described in 8.2.3 and be made to the JEDEC Legal Department.

Committee Members and Representatives are encouraged, but not required, to disclose the Potentially Essential Patents of other entities, including other Committee Members and third-parties.

Committee Members and Representatives are encouraged, but not required; to bring Patent Policy issues or concerns with respect to the Disclosure of Potentially Essential Patents and the licensing of Essential Patent Claims to the attention of the JEDEC Board of Directors for resolution, see 9.2.

8.2.2.2 Committees

JEDEC committees and task groups shall not consider any matters or proposals that are outside the approved scope of such committees or task groups. Furthermore, JEDEC committees and task groups are encouraged to use best efforts to avoid proposals for Standards that are within the approved scope of such committees and task groups and that would be likely to cause Committee Members to terminate their membership in the committee or task group for the purpose of discontinuing their disclosure or RAND licensing obligations.

JEDEC committees and task groups shall keep track of all notices, disclosures and licensing assurances with respect to Potentially Essential Patents and to review, on a periodic basis, the list of prior disclosures of Potentially Essential Patent Claims.

JEDEC committees and task groups shall consider reasonable workarounds and technical alternatives (but are not required to implement such workarounds or alternatives) within the earlier of: a) balloting, or b) one-hundred twenty (120) calendar days of receiving Notice of Refusal to offer Licenses on RAND Terms.

8.2.2.2 Committees (cont'd)

JEDEC committees and task groups are encouraged, but not required, to resolve patent policy issues before balloting. Unresolved issues relating to Potentially Essential Patents may be submitted to the JEDEC Board of Directors for resolution, see 9.2. The sole remedy for any issues or concerns about deviations from approved scope shall be an appeal to the JEDEC Board of Directors made prior to approval of the subject draft specification for resolution, see 9.2.

8.2.3 Disclosure of Potentially Essential Patents

At each committee meeting, the chairperson should call to the attention of all those present the requirements contained in the JEDEC Legal Guides and the obligation of all Representatives to inform the committee of any personal knowledge they have of any Potentially Essential Patents that are owned or controlled by that Committee Member and to call for the Disclosure of Potentially Essential Patents by Representatives. Annex A provides information to be displayed at the beginning of the committee meeting to satisfy the requirement. Additionally, all Representatives should be asked to read the statement attached to each JEDEC sign-in/attendance roster; see Annex B for patent policy application guidelines.

All Committee Members must Disclose Potentially Essential Patents, known to their Representative(s) to be Potentially Essential Patents that are owned or controlled by that Committee Member to the personal knowledge of the Representatives. However, neither Committee Members nor Representatives shall have any obligation to conduct a search for Potentially Essential Patents.

Disclosure of Potentially Essential Patents by a Representative or the Committee Member being represented shall be made as early as reasonably possible. The Disclosure of Potentially Essential Patents shall be in accordance with the definition of Disclosure of Potentially Essential Patents, see 8.2.1. Initial disclosure by a Committee Member or Representative may be made in a meeting of the committee or task group. The Representative is responsible for ensuring that such disclosure is properly recorded in the meeting minutes.

The Representative or Committee Member shall document all known Potentially Essential Patents in either: a) License Assurance/Disclosure Forms, see Annex A.3, or b) Notice of Refusal to offer Licenses on RAND Terms forms, see Annex A.4. Such disclosures or notices of known Potentially Essential Patents shall be delivered to the JEDEC Legal Department within thirty (30) calendar days of draft specification completion in order to be effective.

8.2.3.1 Disclosure of unwillingness to license work of a committee

If a Committee Member knows that it would not be willing to offer to license Essential Patent Claims arising from the Contributions of another Committee Member on RAND terms to all Potential Licensees consistent with 8.2.4, the Committee Member shall notify the committee chair in writing as early as reasonably possible but no later than thirty (30) calendar days after completion of the draft specification in the form of a Notice of Refusal to offer Licenses on RAND Terms, see Annex A.4.

8.2.3.1 Disclosure of unwillingness to license work of a committee (cont'd)

The committee shall consider working around the material or other technical alternatives with a goal of resolving the concern if at all possible. The Committee Member may (at its own discretion) withdraw its notification of Refusal to License at any time. However, if the Committee Member wishes to maintain its position that it would refuse to License the work of the committee, the Committee Member must withdraw from the committee no later than one-hundred twenty (120) calendar days after providing notice of its unwillingness to license.

8.2.4 RAND Patent Licensing Commitment

Subject to the terms and conditions, see 8.2.4, each Committee Member, as a condition of Participation, agrees to offer to license on RAND terms, to all Potential Licensees, such Committee Member's Essential Patent Claims for the use, sale, offer for sale or other disposition of a portion of a product in order to be compliant with the required portions of a final approved JEDEC Standard issued during the period of membership in that committee. The licensing commitment does not apply to Essential Patents of a Committee Member where notice of a Refusal to License has been given by the Committee Member in accordance with 8.2.3.1.

This commitment applies to any Standard that was pending in the committee or task group while the Committee Member Participated in that committee or task group. If a Committee Member terminates its committee membership, the commitment does not apply with respect to any new proposal or Standard introduced in the committee or task group after the Committee Member provided notice to the JEDEC Legal Department terminating its committee membership. If and as necessary, questions whether or not a particular proposal is a new Standard or merely a continuation of a prior Standard will be addressed in the first instance by the JEDEC Legal Department in accordance with 8.2.10.

Certain exceptions apply to the licensing requirement. A Committee Member will not be required to license or continue to license its Essential Patent Claims to a Potential Licensee for a particular Standard if: (i) such Potential Licensee does not agree to grant a license to all other Potential Licensees under such Potential Licensee's Essential Patent Claims of that Standard on RAND terms and conditions for the approved Standard and/or (ii) such Potential Licensee has commenced or has threatened to commence patent litigation targeting such Committee Member's products that are meant to comply with that Standard.

8.2.5 Licensing Assurance/Disclosure Form

A Committee Member or Representative agrees to offer the following licensing options for an Essential Patent Claim:

For any Essential Patent Claims held or controlled by the entity, pending or anticipated to be filed, which are or may be required to implement a Standard that may result from the JEDEC Standard Activity, the entity hereby makes one of the following commitments:

- (i) A license will be offered, without compensation, under reasonable terms and conditions that are free of any unfair discrimination to applicants desiring to utilize the license for the purpose of implementing the JEDEC Standard, subject to the terms and conditions in 8.2.4; *or*
- (ii) A license will be offered, to applicants desiring to utilize the license for the purpose of implementing the JEDEC Standard under reasonable terms and conditions that are free of any unfair discrimination, subject to the terms and conditions in 8.2.4.

8.2.5 Licensing Assurance/Disclosure Form (cont'd)

If a Committee Member, at its discretion, elects not to submit a License Assurance/Disclosure Form at or before the time the ballot closes and does not otherwise provide notice of an unwillingness to license in accordance with 8.2.3.1, the Committee Member and its Affiliates will be deemed to have agreed to offer to grant licenses on RAND terms and conditions for all of its Essential Patent Claims of the balloted Standard, if and as consistent with 8.2.4.

8.2.6 Reference to patented products in JEDEC standards and publications

The following notice shall be included inside the front cover of all JEDEC Standards in which Essential Patent Claims are or may be involved:

“The user’s attention is called to the possibility that compliance with this document may implicate the use of an invention covered by patent rights.”

“By publication of this document, no position is taken with respect to the infringement or validity of any patents. However, JEDEC has received statements of a willingness to offer to license certain rights on reasonable and nondiscriminatory terms and conditions to applicants desiring to obtain such a license. Details may be obtained from JEDEC.”

8.2.7 Special legal disclaimer

The Board has the discretion to approve the issuance of a standard for which a patent owner or applicant has not provided written assurance that the Essential Patent Claims will be licensed, subject to special legal disclaimers.

When determining whether to approve the issuance of such a standard, the Board shall consider whether the committee used diligent efforts, if appropriate under the circumstances, to develop a standard that does not require the use of the Essential Patent Claim(s).

A special legal disclaimer might include the following language:

“Notice: JEDEC has received information that certain patents or patent applications may be essential to this standard. However, as of the publication date of this standard, no statements regarding an assurance or refusal to license such patents or patent applications have been provided. JEDEC does not make any determination as to the validity or relevancy of such patents or patent applications. Anyone making use of the standard assumes all liability resulting from such use. JEDEC and its members disclaim any representation or warranty, express or implied, relating to the standard and its use.”

8.2.7 Special legal disclaimer (cont'd)

If the Board determines that:

- (1) the claim by the patent owner or applicant that an identified patent or patent application may be essential to implement a Standard is a reasonable claim, and
- (2) there is a credible indication that the patent owner or applicant is unwilling or unable to grant licenses, with or without compensation, on RAND terms,

then the Board *shall not* approve the issuance of the standard except as provided in 8.2.7. In its discretion, the Board may seek the advice of an independent outside patent attorney or consultant in making the determinations in subsections (1) and/or (2) of 8.2.7.

8.2.8 Miscellaneous

The Patent Policy applies equally to situations involving the Essential Patent Claims that are discovered after adoption of the Standard.

JEDEC makes no representation as to the reasonableness of any terms or conditions of the license agreements offered by such patent rights holders, and all negotiations regarding such terms and conditions must take place between the individual parties outside the context of JEDEC.

To the extent that Potentially Essential Patent Claims are disclosed with respect to a JEDEC Standard, information regarding the parties who have asserted patent rights in the Standard may be obtained from the JEDEC Corporate Office.

It is possible that other patent rights that have not been disclosed to JEDEC may be implicated by implementation of or compliance with a JEDEC Standard. JEDEC is not responsible for identifying patent claims for which a license may be required in order to implement a JEDEC Standard, and takes no position and conducts no inquiries with respect to the legal validity or scope of those patents or patent claims that are brought to its attention.

8.2.9 Violations

If a Committee Member or Representative materially violates this Patent Policy and the violation is not cured within thirty (30) days following notification of the violation by the JEDEC Corporate Office, the JEDEC Board of Directors may in its discretion suspend the Committee Member or Representative's right to participate in JEDEC. If the Committee Member is allowed to continue participation and engages in another material violation of this Policy, the JEDEC Board of Directors may in its discretion revoke the Committee Member or Representative's right to participate in JEDEC.

8.2.10 Interpretation and Governing Law

The obligations and rights of parties to this agreement in the conduct of committee meetings and the approval of standards as set forth in this Patent Policy will be interpreted in the first instance by the JEDEC Legal Department. When specifically requested by a Committee Member or Representative, interpretations by the Legal Department will be in writing.

8.2.10 Interpretation and Governing Law (cont'd)

Written interpretations by the Legal Department can be appealed by a Committee Member or Representative to the JEDEC Board of Directors. The Board of Directors will make a final decision on appeal, as determined in their reasonable and good faith judgment. The final decision will be in writing.

In no event will JEDEC or the JEDEC Board make a determination that a Patent is or is not a Potentially Essential Patent or that a Patent Claim is or is not an Essential Patent Claim.

The Patent Policy will be interpreted and governed under the laws of the State of New York.

9 Appeals

All appeals related to standard or publication development are initially directed to the JEDEC Office. The provision for appeals is important for the protection of all parties involved within the JEDEC standards development process. An appeals mechanism safeguards both those who are directly and or materially affected by the process and the standards developing organization.

9.1 Appeals related to ANSI/JEDEC standards and publications

The following appeals procedures shall be used for actions taken within the JEDEC standards process for the development of ANSI/JEDEC standards and publications.

9.1.1 Right of appeal

Persons who have directly and or materially affected interests and who have been or will be adversely affected by a standard or publication within ANSI jurisdiction have the right to appeal substantive or procedural actions or inactions of JEDEC formulating groups.

The burden of proof to show an adverse effect shall be on the appellant. Appeals shall be directed to the JEDEC Office in accordance with the appeals procedures as defined in this section.

9.1.2 Criteria for appeals mechanism

The following general criteria are encompassed in these appeals procedures:

- a) Appeals shall be addressed promptly and a decision made expeditiously;
- b) The right of the involved parties to present their cases shall not be denied;
- c) These procedures shall provide for participation by all parties concerned without imposing an undue burden on them;
- d) Consideration of appeals shall be fair and unbiased and shall fully address the concerns expressed; and
- e) Records of appeals shall be kept and made available upon request. The JEDEC Office may levy an appropriate charge to cover the cost of reproduction, handling, and distribution of materials. The fee shall be predetermined, fixed, and reasonable. A procedure for requesting a fee waiver or fee reduction shall be available.

9.1.3 Appeals procedures

The following subsections outline the JEDEC Appeals Procedures. In the case of an appeal to ANSI of a JEDEC action or inaction on an ANSI/JEDEC standard, the appellant may waive the right of the JEDEC appeals process, see 9.1.4.

9.1.3.1 Complaints

The appellant shall file a written complaint with the JEDEC Office within 30 calendar days after the date of the action being appealed or at any time with respect to inaction. The complaint shall state the nature of the objection(s) including any adverse effects, the section(s) of these procedures or the standard(s) that are at issue, action(s) or instances of inaction that are at issue, and the specific remedial action(s) that would satisfy the appellant's concerns. Previous efforts to resolve the objection(s) and the outcome of each shall be noted.

9.1.3.2 Response

Within 30 calendar days after receipt of the complaint, the respondent (formulating group chairman or JEDEC representative) shall respond in writing to the appellant, specifically addressing each allegation of fact in the complaint to the extent of the respondent's knowledge. Complaints that are technical in nature shall be referred to the appropriate JEDEC formulating committee having jurisdiction over the material for review and possible action. Complaints that are procedural in nature shall be referred to the JEDEC Board for review and possible action.

9.1.3.3 Hearing

If the appellant and the respondent are unable to resolve the written complaint informally in a manner consistent with these procedures within 15 calendar days, the JEDEC Office shall schedule a hearing with an appeals panel* on a date agreeable to all participants but within 30 calendar days, giving at least 10 calendar days notice. Hearing on the complaint will take place at the next regular meeting of the JEDEC formulating committee or the JEDEC Board depending on the nature of the complaint.

NOTE In the case of an ANSI appeal, see Annex C.10 for clarification of an appeals panel.

9.1.3.4 Conduct of the hearing

The appellant has the burden of demonstrating adverse effects, improper actions or inactions, and the efficacy of the requested remedial action.

9.1.3.5 Decision

The appeal disposition shall be documented by the formulating committee for technical matters and by the JEDEC Board for procedural matters. A record of the appeals shall be kept by JEDEC and made available to the involved parties.

NOTE In the case of an ANSI appeal, the appeals panel shall render its decision in writing within 30 days of the hearing, based upon a preponderance of the evidence, stating its findings of fact and conclusions, with reasons therefore and citing the evidence. The Committee Secretary shall notify the appellant and the Committee of the decision of the appeals panel, which shall be binding and final on all concerned.

9.1.3.5 Decision (cont'd)

If, for whatever reason(s), the appellant chooses to forego the process detailed above, the JEDEC Office shall maintain all documents pertaining to JEDEC attempts to resolve the matter at hand. These documents may be used in any further appeals proceedings.

9.1.4 Further appeal

If the matter under appeal relates to a JEDEC Standard that has been or is expected to be recognized as an American National Standard, subsequent further appeal may be made directly to ANSI. If the appellant gives notice to the JEDEC Office that further appeal to ANSI is intended, a full record of the complaint, response and decision shall be submitted by the JEDEC Office to ANSI.

NOTE ANSI will not normally hear an appeal of an action or inaction by JEDEC until the appeals process has been completed. Such appeals shall be directed to ANSI in accordance with the procedures of the appropriate ANSI entity (e.g., Board of Standards Review, Executive Standards Council, etc.).

9.2 Appeals not related to ANSI/JEDEC standards and publications

The following appeals procedures shall be used for actions taken within the JEDEC standards process that are not related to the development of ANSI/JEDEC standards and publications.

9.2.1 Right of appeal

Committee Members or Participants who have directly and or materially affected interests and who have been or will be adversely affected by the activities of another Committee Member or Representative, a JEDEC committee, or a JEDEC standard or publication have the right to appeal technical or procedural actions or inactions.

The burden of proof to show an adverse effect shall be on the appellant. Appeals shall be directed to the JEDEC Office in accordance with the appeals procedures as defined in this section.

9.2.2 Criteria for appeals mechanism

The following general criteria are encompassed in these appeals procedures:

- a) Appeals shall be addressed promptly and a decision made expeditiously;
- b) The right of the involved parties to present their cases shall not be denied;
- c) These procedures shall provide for participation by all parties concerned without imposing an undue burden on them;
- d) Consideration of appeals shall be fair and unbiased and shall fully address the concerns expressed; and
- e) Records of appeals shall be kept and made available upon request. The JEDEC Office may levy an appropriate charge to cover the cost of reproduction, handling, and distribution of materials.

9.2.3 Appeals procedures

The following subsections outline the JEDEC Appeals Procedures for appeals that are not related to ANSI/JEDEC standards and publications.

9.2.3.1 Complaints

The appellant shall file a written complaint with the JEDEC Office within 30 calendar days after the date of the action being appealed or at any time with respect to inaction. The complaint shall state the nature of the objection(s) including any adverse effects, the section(s) of these procedures or the Standard(s) that are at issue, action(s) or instances of inaction that are at issue, and the specific remedial action(s) that would satisfy the appellant's concerns. Previous efforts to resolve the objection(s) and the outcome of each shall be noted.

9.2.3.2 Response

Within 30 calendar days after receipt of the complaint, the respondent(s) shall respond in writing to the appellant, specifically addressing each allegation of fact in the complaint to the extent of the respondent's knowledge.

Complaints that are technical in nature shall be referred to the appropriate JEDEC committee having jurisdiction over the material for review and possible action. Complaints that are non-technical or procedural in nature shall be referred to the JEDEC Board for review and possible action. Complaints that relate to the patent policy shall be referred to the JEDEC Board for review and possible action.

9.2.3.3 Hearing

If the appellant and the respondent are unable to resolve the written complaint informally in a manner consistent with these procedures within 30 calendar days, the JEDEC Office shall schedule a hearing with an impartial appeals panel consisting of three individuals appointed by the committee or the JEDEC Board, as appropriate, on a date agreeable to all parties, giving at least 10 calendar days' notice. Hearing on the complaint will take place in person or by telephone.

9.2.3.4 Conduct of the hearing

The appellant has the burden of demonstrating adverse effects, improper actions or inactions, and the efficacy of the requested remedial action.

9.2.3.5 Decision

The appeal disposition shall be documented by the JEDEC appeals panel. A record of the appeals shall be kept by JEDEC and made available to the involved parties.

Appeal dispositions on complaints that are technical in nature may be further appealed to the appropriate JEDEC committee. Appeal dispositions on complaints that are non-technical or procedural in nature may be further appealed to the JEDEC Board of Directors.

10 External publicity

All articles, presentations, news releases, or other publicity must be approved by JEDEC Legal Counsel prior to release.

Articles, speeches, and other presentations for publication or delivery by members of the Board, its committees, or JEDEC staff that cover specific JEDEC work or JEDEC policy or purports to speak on behalf of JEDEC must be approved by the Board, if time permits; otherwise by the Board chairperson who shall be responsible for ensuring that the content is accurate and reflects current JEDEC policy. Any publicity that speaks for the Board shall require similar approval.

The committee chairperson may talk to the press and approve technical and tradeshow presentations about ongoing committee work when it is appropriate to promote a particular standard or the work of the committee. This public disclosure should be limited to the goal of the standard under development and any details of the standard that have been approved by committee ballot(s).

Companies may not advertise or give press releases stating that their products comply with a JEDEC standard, publication, or registration prior to Board approval of the documents.

11 JEDEC ethics rules for electronic communications

No JEDEC member or alternate shall post to an e-mail reflector, bulletin board, or Web site owned or sponsored by JEDEC, any of the following:

- a) any advertising or marketing information,
- b) any cost or pricing information,
- c) any proprietary information,
- d) any non-JEDEC copyright information or material that is in excess of that allowed under current USA copyright laws,
- e) any technical information that requires a USA government export license before it is transferred outside of the United States,
- f) information covered by USA secrecy laws,
- g) solicitations, or requests for contributions to “for profit” or “non-profit” (charitable) organizations,
- h) chain letters,
- i) job search or hiring information,
- j) computer games or other software products,
- k) files with known software viruses,

11 JEDEC ethics rules for electronic communications

- l) offensive material covering:
 - 1) libel (i.e., false or malicious statements),
 - 2) threats, retaliation, or intimidation,
 - 3) use of language that is obscene or in poor taste, including jokes,
 - 4) sexual harassment or inappropriate sexual content, such as pictures, images, messages, or cartoons,
 - 5) discriminatory communication relating to race, color, national origin, sex, marital status, sexual orientation, age, veteran's status, disability, religious or political beliefs.

All electronic communications and posting must comply with this JEDEC Manual and the JEDEC Legal Guides.

Annex A (normative) Legal guidelines summary

A.1 JEDEC patent policy summary

- All JEDEC Member Companies and their Representatives agree to abide by the JEDEC patent policy. The commitment applies to entities that participate in JEDEC Committees but are not JEDEC members, including having a representative present at any point in a meeting of a committee or task group. It continues as long as the Committee Member or Representative is a member of or a participant in a particular JEDEC committee.
- All Member Companies and their Representatives are required to disclose all known Potentially Essential Patent Claims owned or controlled by the Member Company.
- All Member Companies agree to license their Essential Patent Claims on RAND terms and conditions.
- If a Member Company knows it would be unwilling to license its Essential Patent Claims on RAND terms, the member must notify the committee chair and withdraw from the committee within 120 days after giving the notice.
- The disclosure and licensing obligations of Member Companies and their Representatives are limited to Standards developed in the particular JEDEC committees in which they are members or in which they participate.

See, 8.2 for additional information.

A.2 Copyright material

If, in developing a standard, a publication, or a specification, a committee proposes to incorporate verbatim material from a publication copyrighted by another organization, it shall obtain written permission from the owner of the copyright for JEDEC to copy the material. The letter granting permission shall be sent to the JEDEC Office, and the standard or publication shall include a reference to such permission as a footnote.

A.3 License Assurance/Disclosure Form (See 8.2.3 and 8.2.5 of the JEDEC Patent Policy)**Part 1**

Date: _____

Entity Name: _____

Address: _____

IPR Contact: _____

Phone: _____

E-Mail: _____

A.3 License Assurance/Disclosure Form (cont'd)

Part 2

Identify the relevant JEDEC Standard:

Part 3

For Issued Patents:

Patent No: _____

Patent Name or Title: _____

Country of Issuance: _____

For Published Patent Applications:

Published Patent Application No. : _____

Patent Application Name or Title: _____

Country of Filing: _____

For Unpublished Patent Applications:

Subject Matter of Patent Application:

You must complete Part 4 if the entity holds a Patent or has applied for a Patent on an invention the use of which is or may be required to comply with a Standard that may result from the JEDEC Standard Activity.

Part 4

For any Essential Patent Claims held or controlled by the entity, pending or anticipated to be filed, the entity states:

- ____ (i) A license will be offered, without compensation, under reasonable terms and conditions that are demonstrably free of any unfair discrimination to applicants desiring to utilize the license for the purpose of implementing the JEDEC Standard; *or*
- ____ (ii) A license will be offered, with compensation, to applicants desiring to utilize the license for the purpose of implementing the JEDEC Standard under reasonable terms and conditions that are demonstrably free of any unfair discrimination.

A.3 License Assurance/Disclosure Form (cont'd)

Part 5

For any disclosed Patent or Patent Application that contains Essential Patent Claims which, if licensed, would require a payment of royalties or other material consideration to an unaffiliated third party, provide the following information:

Name of Third Party: _____

Address: _____

IPR Contact: _____

Phone: _____

E-Mail: _____

AGREED, ON BEHALF OF THE ENTITY:

(Signature)

(Name printed)

(Date)

Note: The committee or task group has the right to request additional technical information relating to the Patent or Patent Application in order to consider workarounds and other technical alternatives.

RETURN THE COMPLETED FORM BY MAIL TO
JEDEC, ATTENTION: LEGAL DEPARTMENT,
3103 NORTH 10TH STREET, SUITE 240-S, ARLINGTON, VA 22201-2107
OR BY E-MAIL TO JOHNK@JEDEC.ORG

A.4 Notice of Refusal to Offer Licenses on RAND Terms

Part 1

Date: _____

Committee Member: _____

Entity Mailing Address: _____

IPR Contact Name: _____

IPR Contact Telephone Number: _____

IPR Contact E-Mail Address: _____

Part 2

Identify the relevant JEDEC Standard:

Part 3

Pursuant to 8.2.3.1 of the JEDEC Patent Policy, the Committee Member hereby provides notice that the Committee Member is not willing to offer a license on RAND terms to the Potentially Essential Patents identified in A.4, Part 4.

Part 4

For Issued Patents (please attach additional pages as necessary):

1. Owner or assignee (if known at time of disclosure) name: _____
2. Patent Name or Title: _____
3. Patent Number: _____
4. Country of Issuance: _____
5. Portions of Proposed JEDEC Standard affected (please use reasonable efforts to identify which portions may be affected), e.g., clause, page, or any other identifiable information:

For Published Patent Applications (please attach additional pages as necessary):

1. Owner or assignee (if known at time of disclosure) name: _____
2. Published Patent Application Number: _____
3. Patent Application Name or Title: _____
4. Country of Filing: _____
5. Portions of Proposed JEDEC Standard affected (please use reasonable efforts to identify which portions may be affected), e.g., clause, page, or any other identifiable information:

A.4 Notice of Refusal to Offer Licenses on RAND Terms (cont'd)

For Unpublished Patent Applications (please attach additional pages as necessary):

1. Owner or assignee (if known at time of disclosure) name: _____
2. General Subject Matter of Patent Application: _____

3. Portions of Proposed JEDEC Standard affected (please use reasonable efforts to identify which portions may be affected), e.g., clause, page, or any other identifiable information: _____

Part 5

By signing this Notice, the IPR Contact represents that they are authorized to complete and submit this Notice on behalf of the Committee Member. Pursuant to Section 8.2.3.1 of the JEDEC Patent Policy, the IPR Representative represents that the information provided in this Notice does not include a contribution that was contributed by the Committee Member. If the Committee Member becomes aware of any other Potentially Essential Patent not already covered by a Notice and the ballot period is open, then the Committee Member may submit additional Notices.

Signature of IPR Contact

Accepted and Agreed to:

JEDEC

Date Accepted: _____

*RETURN THE COMPLETED NOTICE BY MAIL TO
JEDEC, ATTENTION: LEGAL DEPARTMENT,
3103 NORTH 10TH STREET, SUITE 240-S, ARLINGTON, VA 22201-2107
OR BY E-MAIL TO JOHNK@JEDEC.ORG*

Annex B (informative) Patent policy application guidelines

The following points describe the application of the JEDEC patent policy:

B.1 Committee discussion of pending or existing patents is a permissible activity and is encouraged when the committee feels that the patented item or process represents the best technical basis for a standard.

B.2 Discussion of a pending or existing patent does not constitute an acknowledgment of the validity of the patent, because validity is based on prior art and determination of the company/individual that first made the invention or applied for the patent. The committee's concern is only with the technical merits of the patent and whether the technical proposal is a sound basis for standardization.

B.3 By its terms, the JEDEC patent policy applies with equal force to situations involving:

- a) the discovery of patents that may be required for use of a standard subsequent to its adoption, and
- b) the initial issuance of a patent after the adoption of a standard.

Once disclosure is made, the holder is obligated to provide the same assurances to JEDEC as are required in situations where patents exist or are known prior to approval of a proposed standard.

Thus, if notice is given of a patent that may be required for use of an already approved JEDEC standard, a standards developer may wish to make it clear to other standards-making participants that the JEDEC procedures require the patent holder to provide the assurances contained in the patent policy or suffer the withdrawal of JEDEC's approval of the document as a JEDEC standard.

Annex C (normative) ANSI Standardization Procedures

For those documents that are intended for publication as an American National Standard (ANS), the provisions set forth in this annex apply.

C.1 Notification of American National Standards (ANS) development

Notification of American National Standards activity shall be announced in suitable media as appropriate to demonstrate provision of opportunity for participation by all directly and materially affected persons. At the initiation of a project to develop or revise a Standard, notification shall be transmitted to ANSI using the Project Initiation Notification System (PINS) form, or its equivalent, for listing in Standards Action. A PINS form may be submitted, but is not required, at the initiation of a project to reaffirm or withdraw a Standard. Prompt consideration shall be given to the written views and objections of all participants, including those commenting on the PINS announcement. Comments resulting from the filing of PINS will be handled in accordance with the ANSI Essential Requirements, 2.5.

C.2 Submission to ANSI for public review

Following approval of the standard, responsible JEDEC Standards staff shall submit the proposed ANS to ANSI to initiate public review. JEDEC Standards staff shall provide appropriate documentation to ANSI. Responsible JEDEC Standards staff shall receive, collect and acknowledge receipt of public review comments. In addition, responsible JEDEC Standards staff shall forward all public review comments to the formulating group for review and response. The response to each commenter shall include a notation of the JEDEC and ANSI appeals process.

NOTE A proposed ANS is subject to comment only (not for vote) during public review and by any and all materially or directly affected parties.

C.3 Public review comments

JEDEC Standards staff shall acknowledge receipt of a public review comment, regardless of its nature. The only comments normally addressed by a working group or formulating group are editorial or technical in nature. Technical comments should be accompanied with wording that would aid the formulating group in addressing the comments.

Other comments may be handled in the following manner on behalf of the formulating group:

- The JEDEC Legal Counsel shall respond to comments relating to legal concerns;
- JEDEC Standards staff shall respond to comments relating to concerns regarding the standards development process;
- The formulating group with input from JEDEC staff shall address scope concerns;
- The reason for non-acceptance shall be sent regarding editorial or technical concerns;
- Vague comments shall be returned to the respondent requesting expeditious clarification.

JEDEC Standards staff shall retain copies of response to comments.

Annex C (informative) ANSI Standardization Procedures (cont'd)**C.4 Public review commenter response**

The commenter shall have 14 calendar days after response to acknowledge the acceptance or rejection of that reply. If no response is received, the responsible JEDEC Standards staff shall send a reminder notice to the commenter requesting response. If no response is received within an additional 5 calendar days, the responsible JEDEC Standards staff will send a registered letter to the commenter noting the lack of response. The commenter's comments are then recorded as unresolved and circulated to the formulating group per the provisions of C.3.

All correspondence showing the formulating group's effort to address the comments, noting a lack of response when appropriate, shall be included in any package of materials provided to ANSI.

C.5 Results scenarios

Results scenario #1: If no comments are received after the close of public review, the document shall be forwarded to ANSI with a request for approval.

Results scenario #2: If editorial comments are received by the close of public review, the document editor, editing group, or chair shall address the comments. The document, with edits, if any, shall be forwarded to ANSI for approval.

Results scenario #3: If substantive comments are received from public review, the working group or formulating group shall review these comments, and attempt to resolve them, and notify each commenter of said action (see C.4), along with a notification of the JEDEC and ANSI appeals process.

- a) If no substantive changes are made, the document is forwarded to ANSI for approval.
- b) If substantive changes are made, the formulating group shall conduct a recirculation vote/ballot and "second" public review (see C.4).
- c) If negative, substantive comments remain unresolved from public review, the formulating group shall conduct a recirculation vote/ballot, and, if necessary, a "second" public review (see C.4).

Annex C (informative) ANSI Standardization Procedures (cont'd)

C.6 Voting on an American National Standard

When a vote in a formulating group is for the purpose of approving a document for publication as an American National Standard, a Ballot Summary (Tally of votes) shall be prepared and included in the minutes. The Interest Category is normally self-selected by the voting member.

Action Required	Method (all calendar days)	Approval Criteria
Meeting Vote*	At the meeting	Two-thirds voting
Ballot	30 day ballot	Two-thirds voting
ANSI BSR8 (Public review)	Initial 60 day comment period [30 or 60 day subsequent comment period(s)] (or other ANSI designated time period where applicable)	Comments addressed by formulating group

* Voting members not present at the time of the vote shall be given the opportunity to vote on the standard after the meeting. The JEDEC staff shall notify the absent voting members via e-mail of any substantive changes made to the standard subsequent to the 21 day ballot period and advise that they have 7 days to cast their vote via the JEDEC Voting Machine. Any absent voting members that fail to respond shall be listed as No Response on the final submittal for approval to ANSI. Response to this opportunity to vote shall not be considered as attendance at the meeting for purposes of voting maintenance.

C.7 Legal approval

All ANSI/JEDEC standards shall receive JEDEC legal approval before publication.

C.8 ANSI approval

If ANSI/BSR is approved, responsible JEDEC Standards staff is notified and in turn publishes the document.

If ANSI/BSR does not approve, comment resolution issues will be dealt with by the formulating group and process-related issues will be dealt with by JEDEC Standards staff. If the ANSI/BSR comments are resolved and the document is approved, responsible JEDEC Standards staff publishes the document.

If the comments cannot be resolved, the document is returned to the formulating group for further resolution or cancellation. The formulating group may appeal the actions of the ANSI/BSR.

C.9 ANSI patent policy

If a JEDEC standard is intended for an American National Standard, then the standard must comply with the current ANSI patent policy.

Annex C (informative) ANSI Standardization Procedures (cont'd)

C.10 Appeals panel (for an appeal of an ANS)

In the case of an ANSI appeal, the appeals panel shall consist of three individuals who have not been directly involved in the matter in dispute, and who (knowingly in good faith) will not be materially or directly affected by any decision made or to be made in the dispute. At least two members shall be acceptable to the appellant and at least two members shall be acceptable to JEDEC. In the event the appellant does not wish to select a panelist or a third panelist cannot be agreed upon, JEDEC shall appoint this individual to the panel in order to hold a hearing.

C.11 ANSI Commercial Terms and Conditions

Provisions involving business relations between buyer and seller such as guarantees, warranties, and other commercial terms and conditions shall not be included in an ANS.

Annex D (normative) Committee specific additional policies

In some cases, JEDEC Committees have established additional policies and guidelines to facilitate the operation of a particular committee. The additional policies have been approved by the originating committee and the JEDEC Board of Directors.

This annex contains the committees currently operating with supplemental policies and guidelines. Those supplemental policies and guidelines are included here in their entirety. These policies are considered to be an addition to the requirements set in JM21, and in no case shall these additions contradict or supersede the requirements set in JM21. Some formatting changes have been made for incorporation into this document.

D.1 JC-11 Committee

1 NEW BUSINESS

JC-11 and or subcommittee chairs shall be advised of any new business at least 14 calendar days prior to the next JC-11 meeting. The manner of notification is listed in order of preference: E-mail, Phone, Fax or US Mail. The JC-11 or subcommittee Chair shall determine whether the new business including the background statement (justification) is editorially correct and/or otherwise ready for consideration by the committee. If the proposal is a new outline family, samples need to be made available to the committee at the time of presentation to show that the outline proposal has been reduced to practice.

2 QUORUM

As defined in JM21: The JEDEC Office shall maintain a list of active members for the sole purpose of determining the quorum requirements for a committee meeting. An active member is defined as a member company that has been represented at either or both of the previous two consecutive regular meetings of the committee. Special meetings shall not be considered for the purpose of determining “active” member status. The quorum requirements shall be 50% by count of a committee’s active member list, but in no case shall the quorum requirement be greater than 20 member companies regardless of committee size. All committee member companies present at a meeting are counted toward quorum requirement.

3 JC-11 REGISTRATION AND STANDARDS

3.1 Publication Types and Descriptions

JC-11 has 6 types of publications that are balloted and published. The registrations are:

Registered outlines drawings (such as MO, TO, UO, etc.), and Standard drawings (MS, GS, TS, etc.): These publications contain mechanical drawings that show all of the physical characteristics and dimensions of the features present on the outside of the package. These are the features that would be considered critical in mating the package to the next level of interconnect, i.e., sockets or pc boards.

Design Registrations (DR), and Design Guide Standards: These publications contain all physical features and mechanical algorithms needed when designing a package that conforms to a particular package family, i.e., BGA, QFN, PLCC, etc.

Interim Procedures and Practices (IPP), and Standard Procedures and practices (SPP): These publications contain specific procedures or practices that may be applicable to various package families. Instead of adding this information to every design guide, it is published as a document that is considered “general” in nature and may supplement the information in various design guides. It also may be applicable to older package outlines that do not have a design guide associated with them. In some cases, an IPP or SPP may be needed prior to a Design Registration or Design Guide.

In each of the cases, the registrations and the IPP’s, once determined to be widely used and stable in content, can be balloted for elevation to “standards”.

D.1 JC-11 Committee (cont'd)

4 BALLOT VOTING PERIOD

The voting period for all survey, registration and standardization ballots shall be a minimum 21 days, unless a longer period has been authorized by the JC-11 Chair. All JC-11 ballots should have expired by midnight on the day prior to the first day of the JC-11 meeting in order to have time to address any concerns brought up in the balloting cycle.

5 SURVEY BALLOTS

There is no JC-11 Committee vote required for the distribution of a survey ballot; however all survey ballots must be approved in advance by the JC-11 Chair. The JEDEC Office will monitor all ballots for adherence to JEDEC Legal Guidelines. The sponsor is required to upload the complete, unedited survey ballot results to the JEDEC server for the FIRST meeting following expiration of the ballot (see clause 3 for restrictions on ballot consideration).

6 REGISTRATION AND STANDARDS BALLOTING PROCEDURES

Prior to consideration, the proposed outline must be clearly supported by at least two JEDEC Member companies (sponsor/co-sponsor or sponsor/ballot motion second company). An outline proposal that conforms to the JC-11 outline drawing requirements and the JEDEC Publication 95, Section 4 requirements shall be distributed (via the JC-11 upload tool) to the attendees prior to any discussion or voting.

The sponsor shall prepare the presentation using the drawing template and shall include a **cover page** using the correct ballot template, available on the JC-11 members only area. The ballot template shall state the subject, brief background, and name of sponsor. In preparation of a proposal, the requirements as outlined in the "General Guidelines for Committee and Board Ballot Proposal" and the "Check List for Sponsors" shall be followed. The sponsor shall bring 3 hard copies of the material to be presented to the meeting, 1 for each, the committee secretary, committee chair, and subcommittee chair, if hard copies are not supplied the presentation will be postponed until the 3 hard copies are provided.

A sample or other evidence of the producibility of the proposed package shall also be presented at the time the proposal is made (e.g., foreign outlines or design rules, product data sheet or a similar part that in the JC-11 Chair's opinion demonstrates the producibility of the proposed part). This is to show that the outline proposal has been reduced to practice.

Upon presentation of a new proposal, the sponsor shall make a MOTION to ballot. A 2/3 majority vote of those member companies present and voting is required before a registration or standards ballot may be issued for balloting. If approval is granted, an item number will be assigned.

All outlines must be provided to the designated JC-11 subcommittee chair for thorough review prior to being uploaded via the JEDEC Voting Machine for ballot distribution. The designated JC-11 subcommittee chair shall be the final approval authority of the conformance of the outline to the Design Guide drawing requirements and ASME Y 14.5M-1994. The committee chair will follow the guidelines as provided on the JC-11 members only area, under Check List for Committee Chairs. Limited ballots or reballots involving minor (simple) dimensional type changes may be approved at the meeting for ballot or reballot at the discretion of the designated JC-11 subcommittee chair without the normal editorial review requirement prior to being placed in the ballot cycle. JC-11 Registrations and IPP's do not have to be balloted to the BoD. All JC-11 Standards must first go through committee ballot and then submitted to the JEDEC Board of Directors for approval.

7 BALLOT RESULTS AND RESOLUTION

7.1 Known patents

The ballot sponsor and all JC-11 members are required to identify outlines that are covered by known patents or could be covered by patent applications.

7.2 Discussion of ballot results

Ballot results may not be discussed at any JC-11 meeting prior to the expiration date of the subject ballot.

D.1 JC-11 Committee (cont'd)**7.3 Duplicate voting by company**

In the unlikely event of multiple votes from the same company, only the primary member's vote will be considered and counted in the final tally of results.

7.4 Reporting ballot results

The sponsor is required to report results at the JC-11 meeting immediately following the expiration date of the subject ballot. Electronic copies that shall include the following: voting summary, a paraphrased version of all negative vote reasons and yes vote with comments with their proposed resolution, shall be uploaded to the JEDEC server prior to the meeting start time. The sponsor is required to contact the ballot respondent(s) through the voting machine and or in person and attempt to resolve all comments and negative votes prior to making the report at the JC-11 meeting. Prior to the ballot results presentation, 3 hard copies of the tally, unedited reasons, comments, and proposed resolutions shall be provided, 1 for each, the committee secretary, committee chair, and subcommittee chair, if hard copies are not supplied the presentation will be postponed until the 3 hard copies are provided. In the event of a rebalot or significant editorial changes prior to publication, the sponsor is required to present the updated outline to the committee.

7.4.1 Ballot – not passed

If the ballot does not receive the required 2/3 positive votes ("NO" votes will only be counted if they are accompanied by a full explanation of the reasons for the negative vote and abstentions are not counted), the outline shall either be reballoted or withdrawn by its sponsor.

7.4.2 Ballot – passed with comments

If the committee ballot has received the required 2/3 positive votes ("NO" votes will only be counted if they are accompanied by a full explanation of the reasons for the negative vote and abstentions are not counted) and if the no votes are addressed (responded to) in writing during the official voting period (it is required to use the voting machine) the outline may be published if it is a registration, or sent to the JEDEC Board of Directors for approval if it is a standard. Note: Submission of a standard proposal to the JEDEC Board of Directors requires a 2/3 approval vote of the member companies present at that meeting.

7.4.3 Ballot – passed by acclamation

If the committee ballot has received 100% approval, it is considered approved by acclamation. If all the "approve with comments" and negative votes have been resolved through the voting machine (i.e., voting machine acknowledges approved by acclamation), the ballot sponsor may forward the final tally of votes from the voting machine (.pdf format) and the final (editorial changes only) balloting material ready for publication to the subcommittee chair for their final review, and notification to the JEDEC Office. It is the responsibility of the sponsor to bring one hard copy of the ballot results to the next regular JC-11 meeting for the JC-11 secretary to be included as an attachment to the meeting minutes.

The sponsor will not need to provide presentation materials or copies for the remainder of the JC-11 committee. If the JC-11 or subcommittee chair does not agree with the resolution of the ballot results, or changes are required based on comments, the ballot results will need to be presented at the next JC-11 meeting like any other ballot.

7.5 Motion to rebalot

Any JC-11 member may offer a MOTION to require the outline under consideration to be revised and reballoted. After a second for the motion is secured and discussion is held, a 2/3 majority vote is required to force a rebalot.

NOTE This procedure may only be utilized to prevent the publication of an obvious error that was observed during the ballot process by less than the number needed to cause the committee ballot to fail.

7.6 Minor technical changes and editorial changes

Minor technical changes (not changes in dimension or tolerance values) may be incorporated into the proposed outline at the meeting. This action requires a 2/3 majority vote to publish or, in the case of a standard, sent on for Board of Directors ballot.

D.1 JC-11 Committee (cont'd)

7.6 Minor technical changes and editorial changes (cont'd)

The ballot sponsor is required to contact all companies that voted on the ballot not present at the meeting and offer them the opportunity to vote. All votes will be included in the final ballot totals. If the final vote is unsuccessful (less than 2/3 positive), i.e., the minor technical changes were not approved, the sponsor may either rebalot or revert back to the unchanged outline and publish it as a registered outline or send the standard to the JEDEC Board of Directors for ballot. Editorial changes may be made without any vote or rebalot required. If it is undecided whether a change is technical or editorial, a vote shall be taken at the meeting and recorded in the minutes.

7.7 Changes to dimension and/or tolerance

Any changes to dimension or tolerance values will require a rebalot.

8 PUBLICATION OF JC-11 REGISTERED OUTLINES/STANDARDS

Any ballot that has passed, as stated in 7.4.2 and 7.4.3, can be prepared for publication and sent to the appropriate chair for final review and notification to the JEDEC Office for posting. JC-11 Registered Outlines and Standards will be available on the JEDEC website.

9 IEC-JEDEC ORGANIZATION (IEC/JC-11)

The JC-11.7 chair coordinates activities between JC-11 and the IEC SC-47D committee and reports on the progress of all USA proposals through the IEC voting process. The JC-11.7 Chair shall keep an item log of all USA proposals to IEC

The USA delegation to IEC is headed by the Technical Advisor. The Technical Advisor chairs the Technical Advisory group (TAG) that consists of technical members of JC-11. The TAG normally meets as a task group in conjunction with JC-11 meetings on an as needed basis. The Technical Advisor shall report to JC -11 the USA responses to IEC ballots.

10 SUBMISSION OF JEDEC OUTLINES FOR IEC CONSIDERATION

After an outline has been issued as a committee ballot and accepted for publication as a registered outline or approved for a standards ballot, the sponsor or any member of JC-11 may propose that the outline be submitted to the appropriate IEC technical committee, subcommittee, or working group for their consideration as an IEC standard.

If 2/3 of the JC-11 members present and voting approve the outline for submission to IEC, a request will be made to the JEDEC Board of Directors for approval to submit to the appropriate IEC committee as a new work item proposal.

If the IEC agrees to consider the outline for standardization, the sponsor is required to prepare the proposed outline according to IEC procedures with assistance from the Technical Advisor.

The Technical Advisor shall ensure that the proposal is presented to the appropriate IEC committee and monitor its progress until the outline is issued as an IEC standard or it is abandoned by the IEC.

The JC-11.7 Chair shall report on all IEC ballot activity to JC-11 at each meeting.

10.1 IEC document voting procedure

- a) IEC ballots will be voted upon by the Technical Advisory Group (TAG).
- b) IEC ballots will be e-mailed to each TAG member by the JEDEC Office.
- c) Ballot responses are returned to the Technical Advisor for consolidation and preparation of the JC-11 response.
- d) If 2/3 of the voting TAG members approve and all comments and negative responses are addressed, the Technical advisor will cast a positive vote. Any obvious technical errors found will result in a negative vote and be brought to the attention of the appropriate IEC committee and reviewed again at the JC-11 meeting.

D.1 JC-11 Committee (cont'd)**10.1 IEC document voting procedure (cont'd)**

- e) The TAG shall ensure that JEDEC outlines are technically correct when converted to the IEC format and the ISO dimensioning and tolerancing system.
- f) The Technical Advisor submits the response to the JEDEC Office to be forwarded to the USA National Committee (ANSI) for formal submission to the IEC.

11 ACTION

Action (by the sponsor) on all ballots and outlines that have been approved for publication or for submittal to the Board of Directors shall occur within a 180 day period (i.e., within two meetings) or the item will be subject to termination and removal from the item log.

12 ADDITIONS TO EXISTING OUTLINES

Any sponsor that proposes to revise or add to an existing outline is required to bring the subject outline up to current JC-11 outline documentation, dimensioning and tolerancing requirements. The updating may be accomplished after approval to ballot has been obtained, but before the ballot is distributed.

13 PROCEDURE FOR EDITORIAL CORRECTION(S) TO RELEASED/ PUBLISHED JEDEC JC-11 MECHANICAL OUTLINES AND DOCUMENTS CONTAINED IN JEP95

- 13.1 Editorial changes to JEDEC JC-11 published, mechanical outlines and documents may either be accomplished in accordance with this procedure or by formal balloting. This procedure applies only to editorial errors identified in published mechanical outlines and documents that were created and/or revised by the JEDEC JC-11 committee.
- 13.2 When an editorial error is discovered in any published JEDEC JC-11 document, the person or persons discovering the error are encouraged to bring it to the attention of the JC-11 Chair.
- 13.3 Only the editorial changes identified in the proposal to change (see 13.1) are to be accomplished. There is no stated or unstated requirement that large-scale editorial updating of the entire document is required.
- 13.4 The JC-11 Chair will communicate with the appropriate JC-11 subcommittee chair regarding the identified error. The two Chairs will research the matter and determine if the error is editorial in nature and will document their findings. The designated JC-11 subcommittee chair will present the findings at the next regular or special meeting of the JC-11 Committee.
- 13.5 A 2/3 positive vote of JEDEC JC-11 members present at the meeting is required to accept the findings of the JC-11 Chair and the designated JC-11 subcommittee chair as editorial to implement the approved corrections. If the vote is less than 2/3 positive the material should be prepared for ballot in accordance with the existing JC-11 operating procedures.
- 13.6 If the proposed changes are accepted, the correction will be made under the direction of the JC-11 Chair and/or designated JC-11 subcommittee chair.
- 13.7 When the change is published, the outline will be updated to the next revision letter and the current date of publication will be shown. Or the committee may request to use the JEDEC numbering system for editorial changes, e.g., MO-###A.01.
- 13.8 An "E" will be added to the JC-11 existing item number (e.g., 11-034E) to indicate that an editorial correction has been made to the published outline.

D.2 JC-16, JC-42, JC-45, and JC-63 Committees

1 GENERAL

The general rules governing all JEDEC committees are set forth by JM21. Additional policies and guidelines are established here to facilitate the operation of the particular committees referenced above, and shall be recorded as an addendum to JM21. All policies set forth herein are in addition to the requirements set forth in JM21 and in no case shall these additions contradict or supersede the requirements set forth in JM21.

1.1 Scope

In addition to the rules set forth in JM21, the policies listed herein shall be followed by all participants in the referenced committees without exception unless and until such time as the policies and/or organization and procedures have been modified by the process or processes contained within JM21 including this addendum.

1.2 Governance/Interpretation

The JEDEC Committee Secretary in concert with JEDEC legal staff shall have the sole authority to interpret, in whole or in part, these operating policies. In any case where conflict arises from ambiguity or lack of specificity, or misunderstanding within or related to this document, the JEDEC Committee Secretary in consultation with JEDEC legal staff may make temporary rulings to be confirmed or modified by committee ballot. All temporary rulings shall be confirmed by the full committee prior to any resulting action becoming permanent.

1.3 Modifications to the Policies Addendum

Modifications to this addendum may be made in whole or in part, upon approval by the normal ballot process as extended here. The JC-42 Plenary is required to submit changes to operating policies affecting represented committees for a ballot vote. All policy ballots shall be distributed to all member companies of all the affected committees and each member company shall have one and only one vote on a policy ballot regardless of whether that member company is a member of more than one of the affected committees. Ballot approval requires a minimum of 2/3 of votes cast. Abstention votes shall not be considered in the calculation. Editorial changes may be incorporated into existing operating policies without balloting during a Plenary meeting, provided there is no disagreement within the Plenary that the changes are editorial.

1.3.1 Implementation of Modifications

Any changes to this addendum shall be distributed to the JEDEC members from the affected committees at the earliest possible time upon adoption.

2 COMMITTEE MEETING TIMES POLICY

All Regular Committee meetings shall operate in the time zone where the meeting is held and shall start at 8:00 a.m. and end at 6:00 p.m. each day unless the committee currently meeting at the time decides otherwise. A 2/3 majority vote to approve extending the start or end time must be taken and duly recorded in the minutes of the affected committee or committees.

3 COMMITTEE PRESENTATION POLICIES

Presentations must be made to the committee. Items shared in a task group shall not be considered as committee presentations in the standards process.

All presentations must be placed on the wireless server at the meeting before they can be presented to the committee.

Early notification of items to be discussed, at a regular meeting, is required by JM21 (see 3.1, 3.2, and 3.3). The Committee shall operate by a policy that accepts all currently active items (2nd presentations), plus new presentations (1st presentations) received electronically by all committee members 30 days prior to a regular meeting, and that policy shall be considered as satisfying the early notification requirement in JM21.

The terms “1st presentation” and “2nd presentation” are used to designate new (items not seen before by the committee) or old (items seen before by the committee) items respectively. A 1st presentation (new) may be elevated to the classification of 2nd (old) presentation during a meeting by a motion with unanimous affirmative vote of all members present at a meeting.

D.2 JC-16, JC-42, JC-45, and JC-63 Committees (cont'd)

A MOTION to authorize a ballot for any 2nd presentation item may occur at a regular meeting, or a special meeting that includes the presentation item in the specific agenda approved for the special meeting. 1st presentations shall not be considered for ballot.

The motion authorizing a ballot of a 2nd presentation may authorize the sponsor or a task group to issue the ballot. Task groups authorized to issue a ballot shall follow all procedures and policies for task groups contained in JM21 and this addendum.

All authorizations to issue ballots expire at the next regular meeting.

3.1 Task Group (TG) Policies

TG chairs should be non-biased facilitators.

Consensus lists of items within a TG may be set up allowing 2/3 vote to put something on the list and 2/3 vote to take something off the list.

TG authorization to issue a ballot expires at the next regular committee meeting.

Discussions in a TG should be referenced to written material (presentations or e-mail) to permit fair participation by non-native English speaking attendees (common courtesy in JEDEC).

All TGs authorized to issue a ballot shall only issue that ballot when 2/3 majority vote of the active TG members have approved the exact ballot material in ballot form excluding the cover page (**no exceptions**).

TGs shall provide a minimum 5 calendar days notice of a vote on material to be balloted. Notice must include the exact ballot material in ballot form.

When ballot material properly noticed to TG members is discussed for consensus in a real time interactive forum, numerical values indicated in the ballot material may be modified (including changes to/from TBD) in the ballot material to reach consensus. Such consensus must be documented in the TG minutes. This exception does not apply to non-numerical text, notes, descriptions, formatting or any additions/deletions. If e-mail votes have been submitted with respect to the unaltered material, the TG must consider these as 'no' votes for any modifications, unless the e-mail vote explicitly approves the modified value.

4 BALLOT POLICIES

4.1 Ballot Information

Ballots require minimum 21 day review (**no exceptions - JM21 requirement**) and must be posted to remain open for vote through the Wednesday before the meeting - exceptions require committee vote (fast track).

By duly recorded authorization vote a ballot may be approved for what the committee considers “fast track” where the ballot will remain open for only the minimum 21 day voting period. Such actions are exceptions and should only be considered when the committee believes there is an exceptional time critical nature to the standard being developed.

Material to be balloted must be provided in editable form to the committee chair for committee ballots and to the JEDEC Office for BoD ballots.

All committees require Chair, Vice-chair, and sponsor company as co-sponsors on ballots posted on the voting machine.

JC-42 and JC-45 committees require committee chairs to post ballots on the JEDEC voting machine. JC-63 permits sponsors to post ballots.

“Proposed” must be on every page of new ballot material.

D.2 JC-16, JC-42, JC-45, and JC-63 Committees (cont'd)**4.2 Ballot Handling**

Once voting is closed, ballot comments and tally results should be distributed to the entire committee by the Chair or Sponsor so discussion about comments during meetings can be minimized.

Modifications may be made to ballots without re-ballot provided all member companies present at the meeting agree the modifications are only editorial in nature.

Ballots may pass to the BoD by acclamation between committee meetings only if specifically authorized to be fast track ballots.

For these committees, "Pass by acclamation" is specifically limited to ballots that pass without any negative votes. All no votes must be discussed and addressed by the committee before further action can be taken on the material.

Ballots with open patent issues require a committee ballot addressing those issues to move the ballot to the Board.

4.3 Survey Ballots

Approval for the posting of survey ballots is given by the committee or subcommittee chairman or vice chairman prior to posting on the Voting Machine.

All survey ballots will be in editable source file format, and when possible the text of the survey questions will be copied into the Background section of the Voting Machine posting to allow easy response.

Survey ballots must be posted to the Voting Machine for a minimum of 21 days. The timing of the voting period is negotiated between the survey sponsor and the approving (vice-) chairman.

Paper survey ballots are not allowed.

The sponsor will post the ballot and receive/count votes except when confidentiality of the responses is required in which case the JEDEC Office will receive/ count votes. In all cases, survey ballots will state whether responding company names will be listed in the results and who will see the unfiltered responses.

The committee (or subcommittee) chairman shall be the "co-sponsor" of all survey ballots.

All survey ballots will include the following statement: "Companies are under no obligation to respond to this survey."

All survey ballot tallies will be distributed electronically as soon as possible after the expiration of the voting period and reviewed at the next full committee meeting.

D.3 JC-40 Committee**1 JC-40 Policies****1.1 Files**

Files must be on the wireless server or the designated electronic media before a presentation may be made.

1.2 Meeting Times

The meeting starts immediately after JC-45 as early as 8:00 a.m. on Thursday –and no later than 8:00 a.m. on Friday.

1.3 Item Log

Item log will be issued at the meeting. Items not discussed for over a year will be removed from the active log.

1.4 File Naming

Enforce JM19 File Naming Convention on wireless server.

D.3 JC-40 Committee (cont'd)**1.5 Ballots and Showings**

No ballots or showings will be issued with a JESD standard cover. Cover must be removed, or marked "PROPOSED".

1.6 Ballot Procedures

- a) All ballots shall be in .pdf format.
- b) All ballots shall remain open until Thursday prior to the meeting week.
- c) All ballots shall be submitted 30 days before the meeting in electronic format.
- d) Paper ballots are not allowed.
- e) 1st showing at least 30 days before meeting in electronic format (or at meeting).
- f) 1st showings will be available on the members only area.
- g) Sponsor will create ballot and receive/count votes.
- h) Committee ballots containing pinouts for BoD ballot must have MO number + variation or a JC-11 item number + status.
- i) Any votes received from non-JC-40 members are treated as "comment only" and are not included in the final tally.
- j) The committee (or subcommittee) chairman shall be the "co-sponsor" of all BoD ballots.
- k) A second showing is required to issue a committee ballot.
- l) Second Showing Requirements:
A committee presentation can be considered a second showing if:
 - i) A first showing was made at the previous committee meeting
 - ii) An electronic first showing was upload on the JEDEC website for distribution to the committee members, >30 days before the next committee meeting
 - iii) After a first showing, the second showing can be waived and a committee ballot can be generated, provided there is acceptance by unanimous vote.

1.7 Standard Numbers for Family Products

- a) JESD73 – Bus Switches.
- b) JESD75 – Pinouts and Package Configurations.
- c) JESD76 – Logic Family Products.
- d) JESD82 – DIMM Products.
- e) JEPxxx – Test Methods and Application Notes.

1.8 Survey Ballot Policy

- a) Approval for the posting of survey ballots is given by the committee or subcommittee chairman or vice chairman prior to posting on the Voting Machine.
- b) All survey ballots will be in editable source file format, and when possible the text of the survey questions will be copied into the Background section of the Voting Machine posting to allow easy response.
- c) Survey ballots must be posted to the Voting Machine for a minimum of 21 days. The timing of the voting period is negotiated between the survey sponsor and the approving (vice-) chairman.
- d) Paper survey ballots are not allowed.

D.3 JC-40 Committee (cont'd)

- e) The sponsor will post the ballot and receive/count votes except when confidentiality of the responses is required in which case the JEDEC Office will receive/count votes. In all cases, survey ballots will state whether responding company names will be listed in the results and who will see the unfiltered responses.
- f) The committee (or subcommittee) chairman shall be the “co-sponsor” of all survey ballots.
- g) All survey ballots will include the following statement: “Companies are under no obligation to respond to this survey.”
- h) All survey ballot tallies will be distributed electronically as soon as possible after the expiration of the voting period and reviewed at the next full committee meeting, see JC-40-07-326.

1.9 TG Policies

- a) Consensus lists of items within a TG may be set up allowing 2/3 vote to put something on the list and 2/3 vote to take something off the list.
- b) TG meetings must be held to at least establish consensus, before any ballot material is posted.

NOTE E-mail meetings are considered meetings.
- c) TG Authorization to issue a ballot expires at next regular committee meeting.
- d) All TGs authorized to issue a ballot shall only issue that ballot when 2/3 majority vote of the active TG members have approved the exact ballot material in ballot form excluding the cover page (no exceptions).
- e) TGs shall provide a minimum 5 calendar days notice of a [consensus] vote on material to be balloted. (Notice includes material being considered).
- f) Discussions in a TG should be referenced to written material (presentations or e-mail) to permit fair participation by non-native English speaking attendees (common courtesy in JEDEC).
- g) TG chairs should be non-biased facilitators.
- h) When ballot material properly noticed to TG members is discussed for consensus in a real time interactive forum, numerical values indicated in the ballot material may be modified (including changes to/from TBD) in the ballot material to reach consensus. Such consensus must be documented in the TG minutes. This exception does not apply to non-numerical text, notes, descriptions, formatting or any additions/deletions. If e-mail votes have been submitted with respect to the unaltered material, the TG must consider these as 'no' votes for any modifications, unless the e-mail vote explicitly approves the modified value, see JC-40-07-108.

1.10 Changes to Policies

The Plenary is required to submit changes to operating policies affecting represented committees for a ballot vote. Ballot approval requires a minimum of 2/3 of votes cast. Abstention votes shall not be considered in the calculation. Editorial changes may be incorporated into existing operating policies without balloting during a Plenary meeting, provided there is no disagreement within the Plenary that the changes are editorial, see JC-40-07- 107.

1.11 Item Log

- a) A JEDEC representative will be the custodian of, and has ultimate responsibility for, the item log.
- b) Item numbers will be assigned between meetings by a JEDEC representative via e-mail.
- c) Target is 24 hour response time
 - i) Desire is to minimize item number assignment during the meeting, hopefully to an exception basis only.
 - ii) Members should avoid waiting until the meeting to get item numbers as a courtesy to everyone.
 - iii) Item numbers requested during the meeting may take up to 24 hours to receive due to work load.

D.4 JC-64 Committee

1 JC-64 Policies

1.1 Files

Files must be on the wireless server or the designated electronic media before a presentation may be made.

1.2 Meeting Times

Starts immediately after JC-42.4 on Monday.

1.3 File Naming

Enforce JM19 File Naming Convention on wireless server.

1.4 Ballots and Showings

No ballots or showings will be issued with a JESD standard cover. Cover must be removed, or marked "PROPOSED".

1.5 Ballot Procedures

- a) All ballots shall be in .pdf format.
- b) All ballots shall remain open until Wednesday prior to the meeting week.
- c) All ballots shall be submitted 30 days before the meeting in electronic format.
- d) Paper ballots are not allowed.
- e) 1st showing at least 30 days before meeting in electronic format (or at meeting).
- f) 1st showings will be available on the members only area.
- g) Sponsor will create ballot and receive/count votes.
- h) Committee ballots containing pinouts for BoD ballot must have MO number + variation or a JC-11 item number + status.
- i) Any votes received from non-JC-64 members are treated as "comment only" and are not included in the final tally.
- j) The committee (or subcommittee) chairman shall be "co-sponsor" of all BoD ballots.
- k) A second showing is required to issue a committee ballot.
- l) Second Showing Requirements:
A committee presentation can be considered a second showing if:
 - i) A first showing was made at the previous committee meeting,
 - ii) An electronic first showing was upload on the JEDEC website for distribution to the committee members, >30 days before the next committee meeting,
 - iii) After a first showing, the second showing can be waived and a committee ballot can be generated, provided there is acceptance by unanimous vote.

1.6 Survey Ballot Policy

- a) Approval for the posting of survey ballots is given by the committee or subcommittee chairman or vice chairman prior to posting on the Voting Machine.
- b) All survey ballots will be in editable source file format, and when possible the text of the survey questions will be copied into the Background section of the Voting Machine posting to allow easy response.
- c) Survey ballots must be posted to the Voting Machine for a minimum of 21 days. The timing of the voting period is negotiated between the survey sponsor and the approving (vice-) chairman.

D.4 JC-64 Committee (cont'd)

- d) Paper survey ballots are not allowed.
- e) The sponsor will post the ballot and receive/count votes except when confidentiality of the responses is required in which case the JEDEC Office will receive/count votes. In all cases, survey ballots will state whether responding company names will be listed in the results and who will see the unfiltered responses.
- f) The committee (or subcommittee) chairman shall be the “co-sponsor” of all survey ballots.
- g) All survey ballots will include the following statement: “Companies are under no obligation to respond to this survey.”
- h) All survey ballot tallies will be distributed electronically as soon as possible after the expiration of the voting period and reviewed at the next full committee meeting.

1.7 TG Policies

- a) Consensus lists of items within a TG may be set up allowing 2/3 vote to put something on the list and 2/3 vote to take something off the list
- b) TG meetings must be held to at least establish consensus, before any ballot material is posted.
NOTE E-mail meetings are considered meetings.
- c) TG Authorization to issue a ballot expires at next regular committee meeting.
- d) All Task Groups authorized to issue a ballot shall only issue that ballot when 2/3 majority vote of the active TG members have approved the exact ballot material in ballot form excluding the cover page (no exceptions).
- e) TGs shall provide a minimum 5 calendar days notice of a [consensus] vote on material to be balloted. (Notice includes material being considered.),
- f) Discussions in a TG should be referenced to written material (presentations or e-mail) to permit fair participation by non-native English speaking attendees (common courtesy in JEDEC),
- g) TG chairs should be non-biased facilitators,
- h) When ballot material properly noticed to TG members is discussed for consensus in a real time interactive forum, numerical values indicated in the ballot material may be modified (including changes to/from TBD) in the ballot material to reach consensus. Such consensus must be documented in the TG minutes. This exception does not apply to non-numerical text, notes, descriptions, formatting or any additions/deletions. If e-mail votes have been submitted with respect to the unaltered material, the TG must consider these as 'no' votes for any modifications, unless the E-mail vote explicitly approves the modified value,

1.8 Changes to Policies

The Plenary is required to submit changes to operating policies affecting represented committees for a ballot vote. Ballot approval requires a minimum of 2/3 of votes cast. Abstention votes shall not be considered in the calculation. Editorial changes may be incorporated into existing operating policies without balloting during a Plenary meeting, provided there is no disagreement within the Plenary that the changes are editorial.

1.9 Maintaining Item Log

- a) A JEDEC representative will be the custodian of, and has ultimate responsibility for, the item log.
- b) Item numbers will be assigned by solely by a JEDEC representative via e-mail.
- c) Target is 24 hour response time
 - i) Desire is to minimize item number assignment during the meeting, hopefully on an exception basis only.
 - ii) Members should avoid waiting until the meeting to get item numbers as a courtesy to everyone.
 - iii) Item numbers requested during the meeting may take up to 24 hour because of work load.

