

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner

Patent No. 10,474,595

Issued: November 12, 2019

Filed: December 28, 2017

Inventors: Hyun Lee

Title: Memory Module Having An Open-Drain Output Pin For Parity Error
 In a First Mode and For Training Sequences In A Second Mode

Inter Partes Review No. IPR2022-00064

DECLARATION OF JOHN HALBERT

I, John Halbert, state and declare as follows:

1. I am over the age of 18, of sound mind, and capable of making this declaration.

2. I am submitting this declaration based on my own personal knowledge of the facts stated here.

3. I was employed by Intel Corp. from 1975 through 1985 and 1991 through April 2018, most recently as a Principal Engineer working on, among other things, future memory definitions in JEDEC. While with Intel, Intel designed and manufactured memory, components for memory modules and components for servers with which memory modules interoperate. Therefore, Intel was interested in the specifications JEDEC evaluates for such products and ensuring interoperability of memory related products.

4. Since retiring from Intel, I have been self-employed as a technical consultant, since April 2018, providing technical advice on future memory standards for a DRAM manufacturer. In addition, I have been asked to provide this declaration, which is based on my personal knowledge, as detailed herein. My CV is attached as Exhibit A, and I am being paid my standard rate of \$400 per hour for my time in preparing this declaration.

5. I have designed, defined and written test programs for DRAM memory and SRAM memory in different capacities for the last 43 years during my

career starting in 1975. I started writing test programs for the 1103, a 1-Kilobit DRAM and other DRAM memories that Intel was producing, through 64K density DRAMs, and was manager of the Product Engineering group. From Product Engineering I moved to the DRAM design group at Intel where I designed DRAMs (from 64-Kilobit through 1-Megabit densities). I hold the distinction of designing the first redundancy circuits used in a DRAM that are incorporated in all DRAMs today. After Intel left the DRAM market, I moved to designing Cache SRAM chips that were imbedded in Intel Server CPUs (giving me expertise in Intel CPUs and systems) and became the design manager. I authored and presented a paper at ISSCC in 1998 on High Speed Cache SRAM and participated on panel discussions at ISSCC and IEDM in other years.

6. After working on Cache SRAMs, I moved to the Memory Enabling group, where I participated in JEDEC Standard meetings and enabling other specialized memories for Intel that were not part of JEDEC (e.g., RAMBUS RDRAM). In JEDEC I had major contributions to DDR2, DDR3, DDR4, DDR5, 3D DDR3,4,5 and HBM memory standards from the DRAM device and including RDIMM and LRDIMM standards. I was co-chairperson for the HBM2 taskgroup that defined the HBM2 standard in JEDEC. I have authored numerous presentations and ballots in JEDEC committee meetings for various DRAM memory standards.

In acknowledgement of my work in JEDEC, I received the JEDEC Chairman award in 2016 for my work on the DDR4 and LRDIMM standard.

7. I hold 70 U.S. patents and 80 international patents on DRAMs and have 54 patents pending (at last count). The patents range from DRAM architecture, buffered DIMM cards, signaling and features currently being used in DRAM technology today.

8. When a member company is involved in developing a standard at a JEDEC committee, the member company will send one or more representatives to attend the JEDEC meetings and the company representatives who attend the meetings will be listed in the JEDEC documentation, such as meeting minutes or vote tallies.

9. I served as a representative for Intel Corp. at JEDEC from approximately 2001 to 2003 and from approximately 2010 to 2017. In my role as a representative of Intel at JEDEC, I attended the JEDEC meetings where I received, reviewed, and voted on proposals regarding JEDEC standards. Intel implemented JEDEC standards in its memory module related products. The goal of JEDEC was to standardize memory technology so the various components of the module and the server in which the module operated are interoperable and can communicate with each other. I therefore have personal knowledge of JEDEC policies and

business practices regarding the processes involved in the development of JEDEC standards within JEDEC's committees.

10. To make a proposal for technology to be included as a JEDEC standard, JEDEC's committees issue ballots, which contain the technology proposed for standardization (hereinafter "ballots"), and technology presentations during JEDEC's regular committee meetings (hereinafter "technology presentations"), which are often recorded in meeting minutes. There are other ways in which technology is proposed for standardization, but these are regular procedures for introducing technology for standardization by JEDEC.

11. While I participated in JEDEC on Intel's behalf, there was no rule or other requirement that members treat ballots, technology presentations, or meeting minutes as confidential. Rather, these documents were freely disclosed and distributed within JEDEC's committees and subcommittees between JEDEC members manufacturing memory related products. JEDEC members are expected to discuss proposed technology — such as in ballots, technology presentations or meeting minutes — within their company and among all third-parties interested in interoperability of memory related products. These disclosures are required to determine the feasibility of implementing the proposed standard and also for determining whether other technology might be preferred for standardization. Were confidentiality restrictions in place, JEDEC members would be unable to

carry out the purpose of JEDEC, which is to design products that can interoperate with each other.

I, John Halbert, do hereby declare and state, that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

Executed on September 14, 2021

DocuSigned by:
John B. Halbert
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John Halbert

Exhibit A

JOHN B. HALBERT
8784 SW Marseilles Dr
Beaverton, OR. 97007
(503) 330-6885, johnhalbert3@gmail.com

EDUCATION

Cal Poly San Luis Obispo

B.S. Engineering Technology - Electronics

Areas of Concentration: BioElectronics]

Minor: Math

[1975]

AWARDS

JEDEC Chairman Award for Technical Excellence

2016

Intel Divisional Award

1984

TECHNICAL EXPERIENCE

IP Consultant, Expert Witness

- Writing Claim charts for Memory Patents.
- Expert Witness SK Hynix Vs Netlist

2018- Present
2018-2019

SK Hynix America

2018-Present

Technical consultant for Future Memory definition

- CXL Memory definition
- Post DDR5 architecture definition
- DDR5 for cloud providers

Intel Corp. Data Center Group – Memory Technologist

2000-April 2018

Principal Engineer

- Technical lead for the definition of 3D stacked Memory Standard
- Technical lead investigating DRAM scaling in Server Memory
- 3D-DDR3/4/5, architect
- Core Architect for DDR1, DDR2, DDR3, 4E and DDR5 DRAM Memory Standards
- RDRAM cost analysis and architectural proposals for more cost effective device
 - Technical witness for Hynix/ Micron vs Rambus litigation

Intel Corp

1991-2000

Sr Engineer

- *Technical* Evaluation of external companies for investment by Intel Capitol
- Design Manager - Managed a team of ~25 design engineers
- 2+ Billion transistor designs, functional on 1st design
 - External Cache for Itanium Processor
 - External Cache for Deschutes processor
 - External Cache project on Toshiba Foundry process
- Design Engineer – SRAM array for Pentium external cache

VISIC Corp -> **VLSI Technology**

1985-1991

Sr Engineer

- *Start-up Company*
- Design lead for high speed SRAM specialty memory devices

Intel Corp

1975-1985

Production Engineer; Staff Design Engineer;

- Design engineer for 64K, 256K and 1M DRAM
- Product engineer : Responsible for product yields, cost reduction, test etc

HALBERT, JOHN

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RELATED EXPERIENCE

Private Pilot since the age of 17 - 1/2 owner of a C182 RG, instrument rated and current
2014-2016 President Hillsboro Flying Club - 36 members, 3 airplanes
2012-2014 President of HOA for our neighborhood. 67 houses
1980-1982. Treasurer Mt Hood Ski Patrol - 250 members covering 5 ski areas
1982-1984 Secretary Mt Hood Ski Patrol
National Ski Patrol Member 1972-2020
National Ski Patrol Appointment # 7869. (National recognition for Ski Patrol work)
Sr Patroller, Hill Captain (Responsible for all Volunteer Patrollers during the day at the Ski area)

PUBLICATIONS AND PAPERS

2016 Keynote Speaker JEDEC Server forum
1995 ISSCC speaker : 100Mhz 256K Cache SRAM
I hold ~70 domestic Patents and 80 International Patents in DRAM Memory Architecture

MEMBERSHIPS

National Ski Patrol
IEEE
