

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner

Patent No. 10,474,595

Issued: November 12, 2019

Filed: December 28, 2017

Inventors: Hyun Lee

Title: Memory Module Having An Open-Drain Output Pin For Parity Error
In a First Mode and For Training Sequences In A Second Mode

Inter Partes Review No. IPR2022-00064

DECLARATION OF SUNG JOO PARK

I, Sung Joo Park, state and declare as follows:

1. I am over the age of 18, of sound mind, and capable of making this declaration.
2. I am submitting this declaration based on my own personal knowledge of the facts stated here.
3. I am employed by Samsung Semiconductor, Inc. (“Samsung”).
4. I am currently a principal engineer at Samsung , and have been with the company for over 20 years. I have represented Samsung at JEDEC for over 15 years and I am still involved in JEDEC. I represented Samsung at JEDEC in 2009. Samsung has been a designer and manufacturer of components for memory modules that are compliant with DDR2, DDR3, and DDR4 JEDEC standards. Samsung participated in the JEDEC specification development and evaluation because Samsung implemented JEDEC standardized technology in these products.

5. In my role as a representative of Samsung at JEDEC, I attended JEDEC meetings where I received and reviewed technology proposals for JEDEC standards, and managed Samsung's votes for technology proposals for JEDEC standards. I was a member of various committees tasked with developing these proposals. Two of those JEDEC committees that I participated in were JC-40: Digital Logic, which included JC-40.4: Registered & Fully Buffered Memory Support Logic; and JC45: DRAM Modules, which included JC-45.4: Fully Buffered DRAM Modules. In this role, I became familiar with JEDEC's balloting procedures.

I. Letter Ballot JC-40.4-09-320

6. Because Samsung was a JC-40.4 JEDEC committee member, Samsung received Committee Letter Ballot JC-40.4-09-320 (hereinafter, "Letter Ballot JC-40.4-09-320") on or about November 11, 2009, as indicated by the "Distributed" date on this document and because, under JEDEC procedures, letter ballots were distributed to all committee members. Ex. A. Letter Ballot JC-40.4-09-320 is attached as Exhibit A.

7. Letter Ballot JC-40.4-09-320 contains as an attachment a link to “NB09320-.pdf.” Ex. A. This file, “NB09320-.pdf” contains a technology proposal, Committee Item Number 142.35, which is attached as Exhibit B. As a member of the JC-40.4 committee, Samsung and I received both Exhibits A and B on or about November 11, 2009, as indicated by the “Distributed” date on the Letter Ballot JC-40.4-09-320 and because, under JEDEC procedures, letter ballots were distributed to all committee members. Ex. A.

8. JEDEC Compilation of Tallies for JC-40 CMOS Digital Logic and point committees (hereinafter “Tally JC-40.4-09-320”) shows that I (on behalf of Samsung) voted in favor of the technology proposed by Letter Ballot JC-40.4-09-320 on December 2, 2009. Ex. C at 40 (indicating “Letter Ballot JC-40.4-09-320 Item 142.35”).

II. Letter Ballot JC-45.4-09-321

9. Because Samsung was a JC-45.4 JEDEC committee member, Samsung and I received Committee Letter Ballot JC-45.4-09-321(hereinafter, “Letter Ballot JC-45.4-09-321”) on or about

November 16, 2009, as indicated by the “Distributed” date on this document and because, under JEDEC procedures, letter ballots were distributed to all committee members. Ex. D. Letter Ballot JC-45.4-09-321 is attached as Exhibit D.

10. Letter Ballot JC-45.4-09-321 contains as an attachment a link to “HB09321-.pdf.” Ex. D. This file, “HB09321-.pdf,” contains a technology proposal, Committee Item Number 2192.44, which is attached hereto as Exhibit E. As a member of the JC-45.4 committee, Samsung received both Exhibits D and E on or about November 16, 2009, as indicated by the “Distributed” date on the Letter Ballot JC-45.4-09-321 and because, under JEDEC procedures, letter ballots were distributed to all committee members. Ex. D.

11. JEDEC Tally of Votes for JC-45.4-09-321 (hereinafter “Tally JC-45.4-09-321”) shows that I (on behalf of Samsung) voted in favor of the technology proposed by Letter Ballot JC-45.4-09-321 on December 2, 2009. Ex. F at 92.

I, Sung Joo Park, do hereby declare and state, that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

Executed on: September 13, 2021 Sung Joo Park

Sung Joo Park

DRAM Solution팀(메모리)/박성주/00121302

SAMSUNG

DRAM Solution팀(메모리)/박성주/00121302

Exhibit A



Committee Letter Ballot
JC-40.4-09-320
Item 142.35
Distributed: 11 Nov 2009
Expiring: 03 Dec 2009



SPONSOR: Super Micro Computer Inc., represented by John Smolka, johns@supermicro.com,
(408) 390-8302 N/A

DISTRIBUTION: Formal Vote: JC-404
Non voting committees: JC-40 (Information and Comments)

Eng. No.: AS 90577

Item No.: 142.35

SUBJECT: [LRDIMM DDR3 Memory Initialization Chapter Proposal](#)

BACKGROUND: At September 09 JEDEC meeting in San Jose, motion by Intel and seconded by Montage to authorize the TG to issue one or more ballots on the items listed on pages 3 and 4 of the presentation that have item numbers, have been shown in the committee and for which the TG has reached a consensus.

The motion passed by acclamation.

This ballot proposal is to specify LRDIMM DDR3 Memory Initialization, and has been approved by DDR3 MB TG on 11/09/2009.

PATENTS: No known patent issues on the sponsor's part

ATTACHMENT: [Download NB09320-.pdf](#)

KEYWORDS: DDR3, MB, Memory Buffer, LRDIMM, Initialization

[\[Top\]](#)



Exhibit B



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COMMITTEE LETTER BALLOT

COMMITTEE: JC-40.4

Committee Item Number: 142.35

Subject: LRDIMM DDR3 Memory Initialization Chapter Proposal

Background: At September '09 JEDEC meeting in San Jose, "motion by Intel and seconded by Montage to authorize the TG to issue one or more ballots on the items listed on pages 3 and 4 of the presentation that have item numbers, have been shown in the committee and for which the TG has reached a consensus".

The motion passed by acclamation.

This ballot proposal is to specify LRDIMM DDR3 Memory Initialization, and has been approved by DDR3 MB TG on 11/09/2009.

Keywords: DDR3, MB, Memory Buffer, LRDIMM, Initialization

PROPOSED

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6 Initialization

6.1 Initialization Overview

The sequence of steps below is an overview of the power-up initialization of the Memory Buffer. Figure 1 shows a graphical representation of the same steps. Detailed requirements for each step are provided in the following sections. Note that the sequence below does not distinguish between host HW and host SW (i.e. BIOS).

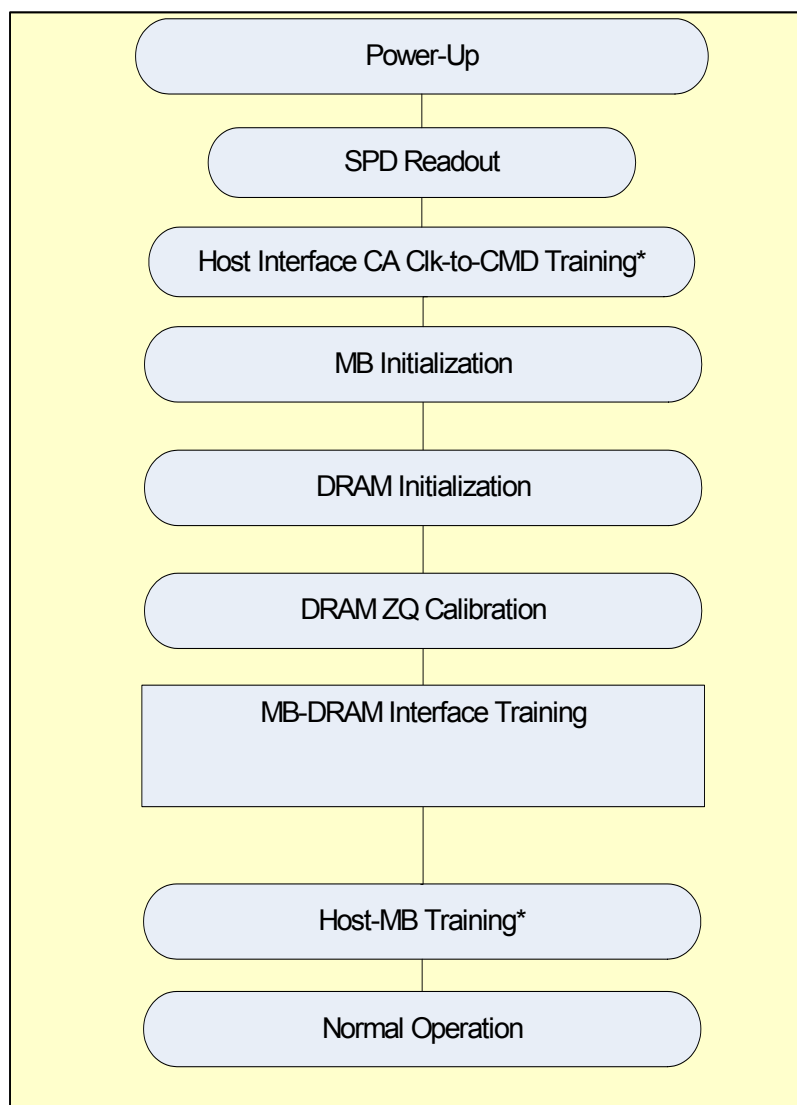
1. Power-Up (Same requirements as 882)
 - a. Ramp of voltage rails
 - b. Generation of stable clock
 - c. De-assertion of RESET#
 2. Determination of DIMM configuration via SPD read out
 3. CA Clock to CMD Training¹
 - a. Sets the optimal phase of the clock to CA and Ctrl signals.
 4. Memory Buffer Initialization
 - a. Host initializes buffer control words
 5. DRAM Initialization
 - a. Host initializes DRAM MRS registers
 6. DRAM ZQ Calibration
 - a. Host issues ZQCAL command to DRAM
 7. Memory Buffer to DRAM Interface Training
 - a. Done by the buffer, triggered by host RCW write
 - b. Write Leveling
 - c. Read Enable training
 - d. Read/Write DQ/DQS training²
- Host can wait for a per-physical rank time-out of tCAL=10ms or periodically poll the buffer via SMBus CSR read or wait for ERROUT#.
8. Host to Memory Buffer Interface Training³
 - a. Done by host
 9. Normal Operation

1. This step is optional for the MB but may be done by some platforms. No special support by the MB is required.

2. This step is optional for the MB but may be required for stable DIMM operation.

3. This step is optional for the MB but may be done by some platforms.

Figure 1 — Initialization Overview



* This step is optional for the MB but may be done by some platforms

6.2 Power-on Initialization

The Memory Buffer can be powered-on at 1.5V or 1.35V. After the voltage ramp, stable power is provided for a minimum of 200 μ S with RESET# asserted. When the reset input RESET# is LOW, all input receivers are disabled, and can be left floating. The MB output pin QRST# follows the MB input pin RESET#. Therefore the reference voltage (V_{REF}) doesn't need to be stable. In addition, when RESET# is LOW, all control registers are restored to their default states. The outputs QACKE[3:0] and QBCKE[3:0] must drive LOW during reset. All other outputs must float. As long as the RESET# input is pulled LOW the register is in low power state and input termination is not present. A certain period of time (t_{ACT}) before the RESET# input is pulled HIGH the reference voltage needs to be stable within specification, the clock input signal must be stable, the register inputs DCS[1:0]# must be pulled HIGH to prevent accidental access to the control registers and DCKE[2:0] as well as DCKE3/DODT[1] must be pulled LOW.

6.2.1 Clock Stabilization Time t_{STAB}

During PLL stabilization time t_{STAB} the memory buffer is not fully operational. In order to avoid invalid commands being sent to the DRAMs some rules apply to the inputs of the buffer:

- All DCS signals need to be kept high. No DRAM command or control word write¹ may take place.
- All DCKE signals don't change their state.
- DODT[0] or DODT[1:0] signals (depending on F0RC6 setting) are kept at a stable valid logic level.

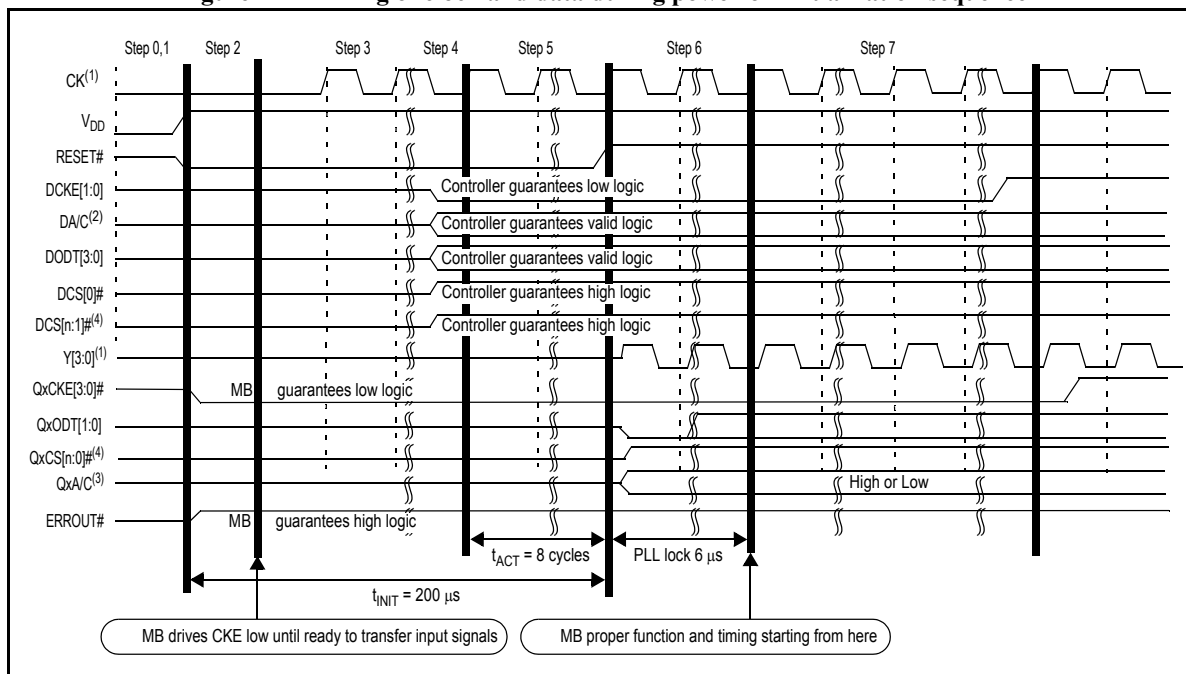
These rules apply to any instance where stabilization time t_{STAB} is required:

- Exit from Reset
- Exit from clock stop power down
- Changing clocking related registers (F0RC2, F0RC10, F0RC11, F1RC8, F1RC11-F1RC15)²
- Changing input clock frequency during boot or run time

Since the buffer has not reached a stable state the termination on the host interface will be undefined before the end of the stabilization time.

After reset and after the PLL stabilization time (t_{STAB}) the device must meet the input setup- and hold specification, as well as accept and transfer input signals to the corresponding outputs. The RESET# input must always be held at a valid logic level once the input clock is present.

Figure 2 — Timing of clock and data during power-on initialization sequence



1. No control word writes are allowed during t_{STAB} after reset/frequency change/clock stop. Control word writes are allowed during t_{STAB} after clocking related register write.

2. These requirements mean that we have to wait two t_{STAB} times during every initialization, one after RESET# de-assertion and one after all the clocking related control words have been written.

- (1) CK# and Y[3:0]# left out for better visibility
 (2) DCKE[2:0], DCKE[3]/DODT[1], DODT[0] and DCS0[3:0]# are not included in this range
 (3) QxCKE[3:0], QxODT[1:0], QxCS[7:0]# are not included in this range
 (4) n = JEDEC standard DIMMs, n = 7 for non-JEDEC applications
 (5) n = 3 for dual or quad rank DIMMs, n = 7 for octal rank DIMMs

From a device perspective, the initialization sequence must be as shown in Table 1

Table 1 — MB Device Initialization Sequence^a

Step	Power	Inputs: Signals provided by the controller								Outputs: Signals provided by the device					
		RESET#	Vref	DCS# [n:0] ^b	DODT [1:0]	DCKE [3:0]	DA/C	PAR_IN	CK CK#	QCS# [n:0] ^c	QODT [1:0]	QCKE [3:0]	QxA/C	ERR OUT#	Y[3:0] Y#[3:0]
0	0V	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	Z	Z	Z	Z	Z	Z
1	0-->V _{DD}	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	L	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z
2 ^d	V _{DD} 1.5V-->1.35V 1.35V-->1.5V	L	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	L	Z	Z	L ^e	Z	H ⁴	Z
3	V _{DD}	L	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	running	Z	Z	L	Z	H	Z
4	V _{DD}	L	X or Z	H	X or Z	L	X or Z	X or Z	running	Z	Z	L	Z	H	Z
5	V _{DD}	L	stable voltage	H	X	L	X	X	running	Z	Z	L	Z	H	Z
6	V _{DD}	H	stable voltage	H	X	L	X	X	running	H	L ^f	L	X	H	running
7 ^g	V _{DD}	H	stable voltage	H	X	X	X	X	running	After Step 6 (Step 7 and beyond), the device outputs are as defined in the device Function Tables (see Table 12, Table 14 and Table 16).					

a. X = Logic LOW or logic HIGH. Z = floating.

b. n = 3 for JEDEC standard DIMM, n = 7 for non-JEDEC application

c. n = 3 for dual or quad rank DIMMs, n = 7 for octal rank DIMMs.

d. The system may power up using either 1.5V or 1.35V. The BIOS reads the SPD and adjusts the voltage if needed from 1.35V to 1.5V or from 1.5V to 1.35V. After the voltage transition, stable power is provided for a minimum of 200 uS with RESET# asserted.

e. QxCKE[3:0] and ERR0UT# will be driven to these logic states by the register after RESET# is driven LOW and VDD is 1.5V or 1.35V (nominal).

f. This indicates the state of QxODT[1:0] after RESET# switches from LOW-to-HIGH and before the rising CK edge (falling CK# edge).

g. Step 7 is a typical usage example and is not a MB requirement.

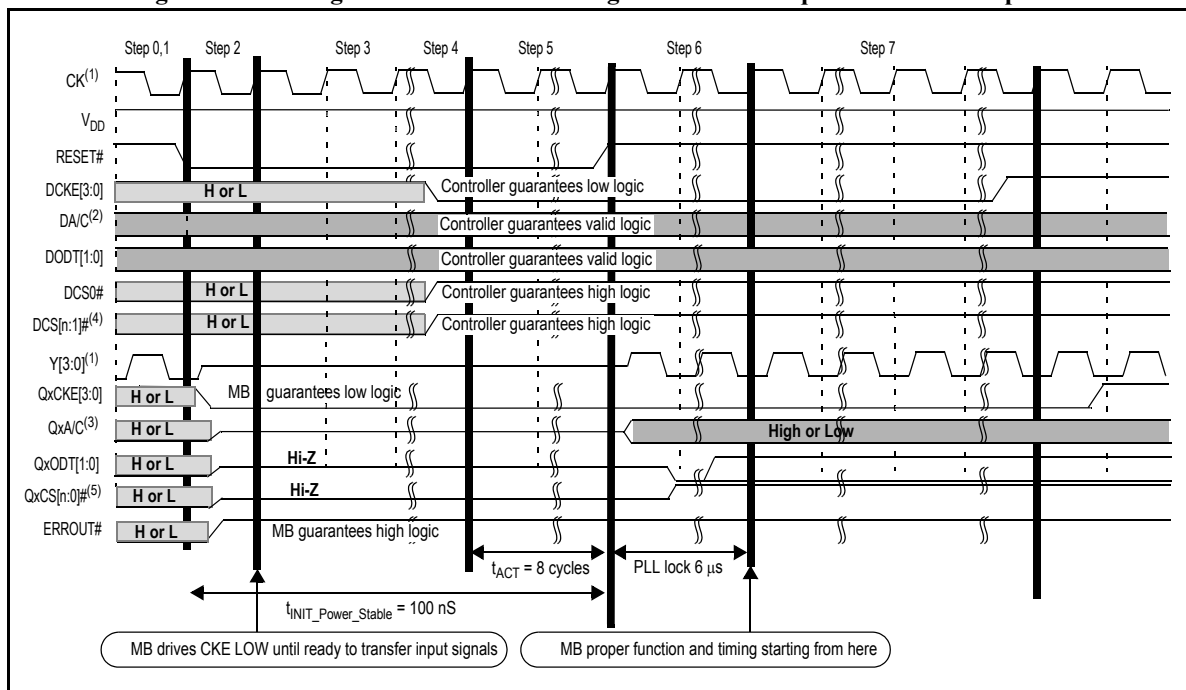
To ensure defined outputs from the register before a stable clock has been supplied, the memory buffer must enter the reset state during power-up. It may leave this state only after a LOW to HIGH transition on RESET# while a stable clock signal is present on CK and CK#. In the DDR3 LRDIMM application, RESET# is specified to be completely asynchronous with respect to CK and CK#. Therefore, no timing relationship can be guaranteed between the two.

As part of the initialization all control words are reset to their default state which is “0”, except when explicitly defined otherwise. After initialization, the host only needs to write to those control registers whose contents need to be changed.

6.3 Initialization with Stable Power (Soft Reset)

The timing diagram in Figure 3 depicts the initialization sequence with stable power and clock. This will apply to the situation when we have a soft reset in the system. RESET# will be asserted for minimum 100ns. This RESET# timing is based on DDR3 DRAM Reset Initialization with Stable Power requirement, and is a minimum requirement. Actual RESET# timing can vary base on specific system requirement, but it cannot be less than 100ns as required by JESD79-3 Specification.

Figure 3 — Timing of clock and data during initialization sequence with stable power



(1) CK# and Y[3:0]# left out for better visibility

(2) DCKE[2:0], DCKE[3]/DODT[1], DODT[0] and DCS0[3:0]# are not included in this range

(3) QxCKE[3:0], QxODT[1:0], QxCS[7:0]# are not included in this range

(4) n = JEDEC standard DIMMs, n = 7 for non-JEDEC applications

(5) n = 3 for dual or quad rank DIMMs, n = 7 for octal rank DIMMs.

Table 2 — MB Device Initialization Sequence^a when Power and Clock are Stable

Step	Power	Inputs: Signals provided by the controller								Outputs: Signals provided by the device					
	VDD, AVDD, PVDD	RESET#	Vref	DCS# [n:0] ^b	DODT [1:0]	DCKE [3:0]	DA/C	PAR_IN	CK CK#	QCS# [n:0] ^c	QODT [1:0]	QCKE [3:0]	QxA/C	ERR OUT#	Y[3:0] Y#[3:0]
0	V _{DD}	H	stable voltage	X	X	X	X	X	running	X	X	X	X	X	running
1	V _{DD}	H	stable voltage	X	X	X	X	X	running	X	X	X	X	X	running
2	V _{DD}	L	stable voltage	X	X	X	X	X	running	Z	Z	L ^d	Z	H ⁴	Z
3	V _{DD}	L	stable voltage	X	X	X	X	X	running	Z	Z	L	Z	H	Z
4	V _{DD}	L	stable voltage	H	X	L	X	X	running	Z	Z	L	Z	H	Z
5	V _{DD}	L	stable voltage	H	X	L	X	X	running	Z	Z	L	Z	H	Z
6	V _{DD}	H	stable voltage	H	X	L	X	X	running	H	L ^e	L	X	H	running
7	V _{DD}	H	stable voltage	H	X	X	X	X	running	After Step 6 (Step 7 and beyond), the device outputs are as defined in the device Function Tables (see Table 12, Table 14 and Table 16).					

a. X = Logic LOW or logic HIGH. Z = floating.

b. n = 3 for JEDEC standard DIMM, n = 7 for non-JEDEC application

c. n = 3 for dual or quad rank DIMMs, n = 7 for octal rank DIMMs.

- d. QxCKE[3:0] and ERROUT# will be driven to these logic states by the register after RESET# is driven LOW and V_{DD} is nominal
- e. This indicates the state of QxODT[1:0] after RESET# switches from LOW-to-HIGH and before the rising CK edge (falling CK# edge)

6.4 Host RCW to Configure MB

After the MB is ready to receive commands and addresses without error, the host needs to configure the MB with register control word writes and/or SMBUS writes (step 4). At reset all RCWs had been reset to their default state (which is '0' except when explicitly noted otherwise). Therefore the host only needs to write those control words whose contents need to be changed.

6.5 Host MRS to Configure DRAM

The host sends MRS commands to the DRAM mode registers to configure proper DRAM operation for all ranks behind the MB. The host can utilize either the MB broadcast mode to send MRS commands to all physical ranks associated with a logical rank or the MB physical rank mode to target MRS commands to specific physical ranks by programming the corresponding mode to the F0RC14 DRAM MRS Control bits.

6.6 Host MRS to DRAM ZQ Calibration

The host sends ZQCL (ZQ Calibration Long) commands to all ranks behind the MB. The MB broadcasts ZQ calibration commands (both ZQCL and ZQCS) to all physical ranks associated with a logical rank. The host may issue ZQ calibration commands sequentially to each logical rank (i.e. wait for tZQinit, tZQoper or tZQCS after each ZQ calibration command before issuing the next one) or it may overlap the ZQ calibration commands to all ranks.

The MB may or may not perform any calibration for its own I/O circuits on receipt of ZQCL or ZQCS calibration commands.

6.7 MB-DRAM Training

After all the DRAMs are fully operational, the host triggers the DRAM interface training by setting the control bit DA4 in F0RC12. Once enabled, the MB assumes autonomous control of the Command/Address, Control and Data/Strobe signals to the DRAMs, without any further assistance from the host.

The MB performs 'Write Leveling' to the DRAMs to ensure successful writes, and 'Read Enable Training' to ensure it can capture read data from the DRAMs correctly, as part of the DRAM interface training.

No DRAM commands or control word writes (either over the Command/Address and Control buses or via SMBus) can be issued to the MB until the MB-DRAM Interface training is complete and the DODTn inputs must be kept low. The MB responds to SMBus CSR read accesses whether or not DRAM interface training is active. To determine DRAM interface training completion the host may either wait for a time 'tCAL * number of physical ranks' (which is the maximum amount of time that the MB-DRAM Interface training is allowed to take) or it may periodically poll the content of the MB CSR 'Training Completion' (see 'Configuration Registers' chapter) over the SMBus.

In addition, training completion can be signaled by the assertion of ERROUT#. This is not the power-up default but can be enabled by setting the DBA1 bit in the F3RC14 Training Completion Control Word.

6.8 Host-MB Training

Now the host can train the MB host interface. The host sets the 'Connector DQ interface write leveling'

PROPOSED

bits in F0RC12 (=0bx001) in order to perform host interface write leveling. Optionally a MB may support RDIMM backward compatible host interface write leveling by intercepting 'Write leveling enable' (MR1 A7) and 'Qoff' (MR1 A12) commands to the DRAMs. The MB asynchronously feeds back CK/CK#, sampled with the rising edge of DQS/DQS#, through the DQ bus (in the same way as a DDR3 DRAM does). Since write leveling requests from the host terminate at the MB, multiple write leveling requests to the MB (i.e. one per rank) will give the same result and are optional. It is sufficient to perform host interface write leveling only once regardless of how many logical or physical ranks are supported by the MB.

MB DRAM interface training must be completed before any MB host interface read training to reflect the correct read round trip delay to and from an LRDIMM. This delay consists of

- (1) Host to MB delay for command
- (2) Command delay through the MB¹
- (3) MB command to DRAM delay
- (4) DRAM latency
- (5) DRAM data/strobe return time to MB
- (6) Data/strobe delay through the MB
- (7) MB to host delay for data/strobe

MB DRAM interface training must be completed before any MB host interface read or write training to ensure that the MB DRAM interface is configured optimally for DRAM reads and writes. The host performs normal writes to DRAM for write DQ/DQS margining, with failure occurring through incorrect strobing of write data through the MB. The host performs read DQ/DQS margining by using normal reads from DRAM or by using the DRAM multi purpose register (MPR) with failure occurring through invalid DQ/DQS alignment at the host I/O pins. No special support by the MB is required for host interface read training.

1. Note that the data/strobe delay through the MB during writes can be different than the command delay through the MB.

Exhibit C

December 04 2009 at 09:31:09



JEDEC
Compilation of Tallies
for JC-40 CMOS Digital Logic and
point committees



The following compilation was generated on 12-04-09, one day after expiration date of the ballot(s). These tallies are not deemed final.

Please attend the meeting or read the minutes of the relevant meeting to learn the final decision on any ballot.

Tallies can change in many significant ways, including, but not restricted to, the following common situations:

- votes can be added by the sponsor upon voters' request (even after the ballot is closed);
- voters can send postcards thereby adding comments;
- voters can send postcards and change a "No" vote to a "Yes";
- sponsors may further address comments;
- etc.

The list of ballots contains not only those ballots that the committee voted but also those that were distributed on a "For information and Comments" or "Information only" basis.

Committee Letter Ballot JC-40.3-09-282 Item 104.75

Subject: DDR3 Register (SSTE32882) -- DDR3 1866 Specification

PATENTS: No known patent issues on the sponsor's part

[Clik here for NB09282-.pdf](#)

Ballot distributed: 09 Nov 2009, Expired: 03 Dec 2009

Sponsor: Mr. Ramzi Ammar **Silego Technology** [e-mail \(rammar@silego.com\)](mailto:rammar@silego.com)

NON FINAL REPORT/ Attend meeting or read minutes for final results.								
Company / voter	Y*	N*	A*	P*	C*	PC*	DoV*	DoR*
20 companies voted	15	0	5	0	0			
Advanced Micro Devices Inc. Patel	Y						12/02/09	
Cray Inc. Grossmeier			A				11/16/09	
Dell Inc. Berke	Y						12/01/09	
Elpida Memory Incorporated Ono	Y						11/26/09	
Hynix Semiconductor Kim			A				12/02/09	
IBM Corporation Stout	Y						11/20/09	
Inphi Corporation Washkewicz	Y						12/02/09	
Integrated Device Technology Inc. Franklin	Y						12/03/09	
Intel Corporation Tsang	Y						12/03/09	
Kingston Technology Company Inc. Cheng			A				11/23/09	
Legacy Electronics Inc. Mecker	Y						12/01/09	
Micron Technology Inc. Graham	Y						11/30/09	
Netlist Inc. Martinez	Y						12/01/09	
Numonyx B.V. Abdulla			A				11/30/09	
Nvidia Corporation Wagner			A				12/01/09	
NXP Semiconductors Roozeboom	Y						12/01/09	
Samsung Semiconductor Park	Y						12/02/09	
Silego Technology Chung	Y						12/03/09	
Smart Modular Technologies, Inc. Marino	Y						12/02/09	
Texas Instruments Inc. Frank	Y						12/03/09	
* Y = Yes, N = No, A = Abstain, P = Patent(s), C = Comments PC: Postcard, Y = approved response, N = did not approve response, N/A: not available, sponsor and / or voter did not respond, DoV: Date of Vote								

JEDEC compilation of tallies (non final) expiring on December 03 2009. The minutes of the relevant meeting(s) will contain the final decision on any ballot.

Committee Letter Ballot JC-40.4-09-255 Item 142.12

Subject: Transparent Mode Functionality

PATENTS: No known patent issues on the sponsor's part

[Clik here for NB09255-.pdf](#)

Ballot distributed: 22 Oct 2009, Expired: 03 Dec 2009

Sponsor: Mr. Christian Harrieder Texas Instruments Inc. [e-mail \(christian.harrieder@ti.com\)](mailto:christian.harrieder@ti.com)

NON FINAL REPORT/ Attend meeting or read minutes for final results.								
Company / voter	Y*	N*	A*	P*	C*	PC*	DoV*	DoR*
19 companies voted	11	0	8	1	1_Y			
Advanced Micro Devices Inc. Patel			A				12/03/09	
Agilent Technologies Keller			A				10/27/09	
Cray Inc. Grossmeier	Y						10/27/09	
Elpida Memory Incorporated Ono	Y						11/26/09	
Hynix Semiconductor Kim	Y						12/02/09	
IBM Corporation Stout			A				11/20/09	
Inphi Corporation Washkewicz	Y						12/02/09	
Integrated Device Technology Inc. Franklin	Y						12/02/09	
Intel Corporation Tsang	Y						12/03/09	
Kingston Technology Company Inc. Cheng			A				10/27/09	
Legacy Electronics Inc. Mecker			A				12/01/09	
Micron Technology Inc. Graham	Y				X	N/A	11/30/09	
Netlist Inc. Martinez			A	P			12/01/09	
Nvidia Corporation Wagner			A				12/01/09	
NXP Semiconductors Roozeboom	Y						12/01/09	
Samsung Semiconductor Park	Y						12/02/09	
Silego Technology Chung	Y						12/03/09	
Smart Modular Technologies, Inc. Marino			A				11/30/09	
Texas Instruments Inc. Harrieder	Y						10/26/09	
* Y = Yes, N = No, A = Abstain, P = Patent(s), C = Comments PC: Postcard, Y = approved response, N = did not approve response, N/A: not available, sponsor and / or voter did not respond, DoV: Date of Vote								

Comments from **Micron Technology Inc.**

No where in the ballot is it identified that this pertains to the Memory Buffer except the keywords.

Postcard Response (for above discussion) / if any present:"

PATENT ISSUE:

Netlist may have IP that applies to this ballot.

Committee Letter Ballot JC-40.4-09-297 Item 142.51

Subject: Transparent Mode CA timing

PATENTS: No known patent issues on the sponsor's part

[Clik here for NB09297-.pdf](#)

Ballot distributed: 10 Nov 2009, Expired: 03 Dec 2009

Sponsor: Mr. Christian Harrieder Texas Instruments Inc. [e-mail \(christian.harrieder@ti.com\)](mailto:christian.harrieder@ti.com)

NON FINAL REPORT/ Attend meeting or read minutes for final results.								
Company / voter	Y*	N*	A*	P*	C*	PC*	DoV*	DoR*
20 companies voted	14	0	6	1	0			
Advanced Micro Devices Inc. Patel			A				12/03/09	
Cray Inc. Grossmeier			A				11/16/09	
Elpida Memory Incorporated Ono	Y						11/26/09	
FormFactor Inc. Gervasi	Y						12/02/09	
Hynix Semiconductor Kim	Y						12/02/09	
IBM Corporation Stout			A				11/20/09	
Inphi Corporation Washkewicz	Y						12/02/09	
Integrated Device Technology Inc. Franklin	Y						12/02/09	
Intel Corporation Tsang	Y						12/03/09	
Kingston Technology Company Inc. Cheng	Y						11/23/09	
Legacy Electronics Inc. Mecker			A				12/01/09	
Micron Technology Inc. Graham	Y						11/30/09	
Netlist Inc. Martinez			A	P			12/01/09	
Nvidia Corporation Wagner			A				12/01/09	
NXP Semiconductors Roozeboom	Y						12/01/09	
Samsung Semiconductor Park	Y						12/02/09	
Silego Technology Chung	Y						12/03/09	
Smart Modular Technologies, Inc. Marino	Y						12/02/09	
Sun Microsystems Inc. Lee	Y						11/13/09	
Texas Instruments Inc. Harrieder	Y						11/19/09	
* Y = Yes, N = No, A = Abstain, P = Patent(s), C = Comments PC: Postcard, Y = approved response, N = did not approve response, N/A: not available, sponsor and / or voter did not respond, DoV: Date of Vote								

PATENT ISSUE:

Netlist may have IP that applies towards this ballot

Committee Letter Ballot JC-40.4-09-299 Item 142.54

Subject: LR-DIMM DDR3 Memory Buffer Pin Description Proposal

PATENTS: No known patent issues on the sponsor's part

[Clik here for NB09299-.pdf](#)

Ballot distributed: 10 Nov 2009, Expired: 03 Dec 2009

Sponsor: Mr. John Smolka **Silego Technology** [e-mail \(jsmolka@silego.com\)](mailto:jsmolka@silego.com)

NON FINAL REPORT/ Attend meeting or read minutes for final results.								
Company / voter	Y*	N*	A*	P*	C*	PC*	DoV*	DoR*
21 companies voted	18	0	3	1	5Y			
Advanced Micro Devices Inc. Patel	Y				X	N/A	12/03/09	
Cray Inc. Grossmeier	Y						11/16/09	
Dell Inc. Berke	Y						12/01/09	
Elpida Memory Incorporated Ono	Y				X	N/A	11/26/09	
FormFactor Inc. Gervasi	Y				X	N/A	12/02/09	
Hynix Semiconductor Kim	Y						12/02/09	
IBM Corporation Stout	Y						11/20/09	
Inphi Corporation Washkewicz	Y				X	N/A	12/02/09	
Integrated Device Technology Inc. Franklin	Y				X	N/A	12/02/09	
Intel Corporation Tsang	Y						12/03/09	
Kingston Technology Company Inc. Cheng	Y						11/23/09	
Legacy Electronics Inc. Mecker			A				12/01/09	
Micron Technology Inc. Graham	Y						11/30/09	
Netlist Inc. Martinez			A	P			12/01/09	
Nvidia Corporation Wagner			A				12/01/09	
NXP Semiconductors Roozeboom	Y						12/01/09	
Samsung Semiconductor Park	Y						12/02/09	
Silego Technology Chung	Y						12/03/09	
Smart Modular Technologies, Inc. Marino	Y						11/30/09	
Sun Microsystems Inc. Lee	Y						11/13/09	
Texas Instruments Inc. Harrieder	Y						11/30/09	
* Y = Yes, N = No, A = Abstain, P = Patent(s), C = Comments PC: Postcard, Y = approved response, N = did not approve response, N/A: not available, sponsor and / or voter did not respond, DoV: Date of								

Comments from **Advanced Micro Devices Inc.**

TG has unanimously agreed to remove QAECC[9,6,2] pins from the buffer and hence should be removed from this ballot. Postcard Response (for above discussion) / if any present:"

Comments from **Elpida Memory Incorporated**

How should the QAECC2,6,9 be treated ? Changing to NC or RFU ? Postcard Response (for above discussion) / if any present:"

Comments from **FormFactor Inc.**

ERROUT_n should include statement about being an open drain output and that a pull-up is required on the main board. Postcard Response (for above discussion) / if any present:"

Comments from **Inphi Corporation**

Inphi approves material in red text. Postcard Response (for above discussion) / if any present:"

Comments from **Integrated Device Technology Inc.**

QAECC 9, 6, and 2 are shown in this Ballot but in MB TG discussion they should all be renamed RFU as there was no usage model for them. Postcard Response (for above discussion) / if any present:"

PATENT ISSUE:

Netlist may have IP that may apply towards this ballot

Committee Letter Ballot JC-40.4-09-300 Item 142.53

Subject: LR-DIMM DDR3 Memory Buffer Ballout Proposal

PATENTS: No known patent issues on the sponsor's part

[Clik here for NB09300-.pdf](#)

Ballot distributed: 10 Nov 2009, Expired: 03 Dec 2009

Sponsor: Mr. John Smolka **Silego Technology** [e-mail \(jsmolka@silego.com\)](mailto:jsmolka@silego.com)

NON FINAL REPORT/ Attend meeting or read minutes for final results.								
Company / voter	Y*	N*	A*	P*	C*	PC*	DoV*	DoR*
20 companies voted	14	0	6	1	2Y			
Advanced Micro Devices Inc. Patel	Y						12/02/09	
Cray Inc. Grossmeier	Y						11/16/09	
Dell Inc. Berke			A				12/01/09	
Elpida Memory Incorporated Ono	Y				X	N/A	11/26/09	
Hynix Semiconductor Kim	Y						12/02/09	
IBM Corporation Stout	Y						11/20/09	
Inphi Corporation Washkewicz	Y						12/02/09	
Integrated Device Technology Inc. Franklin	Y				X	N/A	12/02/09	
Intel Corporation Tsang	Y						12/03/09	
Kingston Technology Company Inc. Cheng			A				11/23/09	
Legacy Electronics Inc. Mecker			A				12/01/09	
Micron Technology Inc. Graham	Y						11/30/09	
Netlist Inc. Martinez			A	P			12/01/09	
Nvidia Corporation Wagner			A				12/01/09	
NXP Semiconductors Roozeboom	Y						12/01/09	
Samsung Semiconductor Park	Y						12/02/09	
Silego Technology Chung	Y						12/03/09	
Smart Modular Technologies, Inc. Marino			A				11/30/09	
Sun Microsystems Inc. Lee	Y						11/13/09	
Texas Instruments Inc. Harrieder	Y						11/30/09	
* Y = Yes, N = No, A = Abstain, P = Patent(s), C = Comments PC: Postcard, Y = approved response, N = did not approve response, N/A: not available, sponsor and / or voter did not respond, DoV: Date of Vote								

Comments from Elpida Memory Incorporated

How should the QAECC2,6,9 be treated ? Changing to NC or RFU ? Postcard Response (for above discussion) / if any present:"

Comments from Integrated Device Technology Inc.

QAECC 9, 6, and 2 are shown in this Ballot but in MB TG discussions they should all be renamed RFU as there was no useage model for them Postcard Response (for above discussion) / if any present:"

PATENT ISSUE:

Netlist may have IP that may apply towards this ballot.

Committee Letter Ballot JC-40.4-09-316 Item 142.46

Subject: LRDIMM DDR3 Memory Buffer Host Interface Protocol and Requirements

PATENTS: No known patent issues on the sponsor's part

[Clik here for NB09316-.pdf](#)

Ballot distributed: 11 Nov 2009, Expired: 03 Dec 2009

Sponsor: Mr. John Smolka **Silego Technology** [e-mail \(jsmolka@silego.com\)](mailto:jsmolka@silego.com)

NON FINAL REPORT/ Attend meeting or read minutes for final results.								
Company / voter	Y*	N*	A*	P*	C*	PC*	DoV*	DoR*
20 companies voted	15	0	5	1	3Y			
Advanced Micro Devices Inc. Patel	Y				X	N/A	12/03/09	
Cray Inc. Grossmeier	Y						11/16/09	
Dell Inc. Berke	Y						12/01/09	
Elpida Memory Incorporated Ono	Y						11/26/09	
Hynix Semiconductor Kim	Y						12/02/09	
IBM Corporation Stout	Y						11/20/09	
Inphi Corporation Washkewicz	Y				X	N/A	12/02/09	
Integrated Device Technology Inc. Franklin	Y						12/02/09	
Intel Corporation Tsang	Y						12/03/09	
Kingston Technology Company Inc. Cheng			A				11/23/09	
Legacy Electronics Inc. Mecker			A				12/01/09	
Micron Technology Inc. Graham	Y						11/30/09	
Netlist Inc. Martinez			A	P			12/01/09	
Nvidia Corporation Wagner			A				12/01/09	
NXP Semiconductors Roozeboom	Y						12/01/09	
Samsung Semiconductor Park	Y						12/02/09	
Silego Technology Chung	Y						12/03/09	
Smart Modular Technologies, Inc. Marino			A				12/01/09	
Sun Microsystems Inc. Lee	Y						11/13/09	
Texas Instruments Inc. Harrieder	Y				X	N/A	11/30/09	
* Y = Yes, N = No, A = Abstain, P = Patent(s), C = Comments PC: Postcard, Y = approved response, N = did not approve response, N/A: not available, sponsor and / or voter did not respond, DoV: Date of Vote								

Comments from **Advanced Micro Devices Inc.**

section 4.2.2.3.6.4 should be part of the ballot.

Add a statement which indicates it is not allowed by the buffer to put half the ranks in self refresh mode while other half the ranks on a dimm in power down mode to help reduce the test/validation combinations. Postcard Response (for above discussion) / if any present:"

Comments from **Inphi Corporation**

Inphi approves material in red text Postcard Response (for above discussion) / if any present:"

PATENT ISSUE:

Netlist may have IP that may apply to this ballot

Comments from **Texas Instruments Inc.**

page 7; Table 6, Section "2 Way Rank Multiplication using A[15]", Subsection "Nr. DCS=4", First Row, Column A16/DCS[2]_n:
is 'x' should be '1'

page 15; Table 10, row NOP

"Command is not passed to the DRAM bus." contradicts chapter 4.2.2.3.9 "The MB will pass a NOP onto the DRAM bus, broadcasting to all sub-ranks." Postcard Response (for above discussion) / if any present:"

Committee Letter Ballot JC-40.4-09-317 Item 142.47

Subject: LRDIMM DDR3 Memory Buffer DRAM Interface Protocol and Requirements

PATENTS: No known patent issues on the sponsor's part

[Clik here for NB09317-.pdf](#)

Ballot distributed: 11 Nov 2009, Expired: 03 Dec 2009

Sponsor: Mr. John Smolka **Silego Technology** [e-mail \(jsmolka@silego.com\)](mailto:jsmolka@silego.com)

NON FINAL REPORT/ Attend meeting or read minutes for final results.								
Company / voter	Y*	N*	A*	P*	C*	PC*	DoV*	DoR*
21 companies voted	16	0	5	1	4Y			
Advanced Micro Devices Inc. Patel	Y				X	N/A	12/03/09	
Cray Inc. Grossmeier	Y						11/16/09	
Dell Inc. Berke	Y						12/01/09	
Elpida Memory Incorporated Ono	Y				X	N/A	11/26/09	
Hynix Semiconductor Kim	Y						12/02/09	
IBM Corporation Stout	Y						11/20/09	
Inphi Corporation Washkewicz	Y						12/02/09	
Inphi Corporation Raghavan	Y						12/02/09	
Integrated Device Technology Inc. Franklin	Y				X	N/A	12/02/09	
Intel Corporation Tsang	Y				X	N/A	12/03/09	
Kingston Technology Company Inc. Cheng			A				11/23/09	
Legacy Electronics Inc. Mecker			A				12/01/09	
Micron Technology Inc. Graham	Y						11/30/09	
Netlist Inc. Martinez			A	P			12/01/09	
Nvidia Corporation Wagner			A				12/01/09	
NXP Semiconductors Roozeboom	Y						12/01/09	
Samsung Semiconductor Park	Y						12/02/09	
Silego Technology Chung	Y						12/03/09	
Smart Modular Technologies, Inc. Marino			A				12/02/09	
Sun Microsystems Inc. Lee	Y						11/13/09	
Texas Instruments Inc. Harrieder	Y						11/30/09	
* Y = Yes, N = No, A = Abstain, P = Patent(s), C = Comments PC: Postcard, Y = approved response, N = did not approve response, N/A: not available, sponsor and / or voter did not respond, DoV: Date of								

Comments from **Advanced Micro Devices Inc.**

TG has unanimously agreed to remove all references related to QAECC[2,6,9] from the buffer spec. This ballot should editorially update it accordingly. Postcard Response (for above discussion) / if any present:"

Comments from **Elpida Memory Incorporated**

How should the QAECC 2,6,9 part be treated ?

Removing the QAECC 2,6,9 part? Postcard Response (for above discussion) / if any present:"

Comments from **Integrated Device Technology Inc.**

QAECC 9, 6, and 2 are shown in this Ballot but in MB TG discussion they should all be renamed RFU as there was no useage model for them Postcard Response (for above discussion) / if any present:"

Comments from **Intel Corporation**

Editorial changes: Table 2: QAECC should be deleted. The ECC DRAM columns should also be deleted. Page 12, 4.2.2.3.4.3 The Targeted Refresh mode is used the Refresh Control bit .. should be The Targeted Refresh mode is used if the Refresh Control bit ..
Page 14, 4.2.2.3.8 When Broadcast to All Sub-ranks is spiced, & should probably be When Broadcast to All Sub-ranks is specified, & Postcard Response (for above discussion) / if any present:"

PATENT ISSUE:

Netlist may have IP that applies towards this ballot

Committee Letter Ballot JC-40.4-09-318 Item 142.11c

Subject: DDR3 MB Control Word Definition

PATENTS: No known patent issues on the sponsor's part

[Clik here for NB09318-.pdf](#)

Ballot distributed: 11 Nov 2009, Expired: 03 Dec 2009

Sponsor: Mr. John Smolka **Silego Technology** [e-mail \(jsmolka@silego.com\)](mailto:jsmolka@silego.com)

Parent ballot: JC-40.4-09-216

NON FINAL REPORT/ Attend meeting or read minutes for final results.								
Company / voter	Y*	N*	A*	P*	C*	PC*	DoV*	DoR*
21 companies voted	14	0	7	1	5Y 1A			
Advanced Micro Devices Inc. Patel	Y				X	N/A	12/03/09	
Cray Inc. Grossmeier			A				11/16/09	
Dell Inc. Berke	Y						12/01/09	
Elpida Memory Incorporated Ono	Y				X	N/A	11/26/09	
FormFactor Inc. Gervasi					X	N/A	12/02/09	
Hynix Semiconductor Kim	Y						12/02/09	
IBM Corporation Stout	Y						11/20/09	
Inphi Corporation Washkewicz	Y				X	N/A	12/02/09	
Integrated Device Technology Inc. Franklin	Y						12/02/09	
Intel Corporation Tsang	Y				X	N/A	12/03/09	
Kingston Technology Company Inc. Cheng			A				11/23/09	
Legacy Electronics Inc. Mecker			A				12/01/09	
Micron Technology Inc. Graham	Y						11/30/09	
Netlist Inc. Martinez			A	P			12/01/09	
Nvidia Corporation Wagner			A				12/01/09	
NXP Semiconductors Roozeboom	Y						12/01/09	
Samsung Semiconductor Park	Y						12/02/09	
Silego Technology Chung	Y						12/03/09	
Smart Modular Technologies, Inc. Marino			A				12/01/09	
Sun Microsystems Inc. Lee	Y						11/13/09	
Texas Instruments Inc. Harrieder	Y				X	N/A	11/30/09	
* Y = Yes, N = No, A = Abstain, P = Patent(s), C = Comments								

PC: Postcard, Y = approved response, N = did not approve response, N/A: not available, sponsor and / or voter did not respond, DoV: Date of Vote

Comments from Advanced Micro Devices Inc.

-- Table 25 should have reverse the mapping as following: 00 - default - 8 rank; 01 - 4 rank; 10 - 2 rank; 11 - 1 rank
-- Footnote 2 for table 18 should be included part of the ballot
-- There are several other editorial changes that has been suggested. Will show the updated draft. Postcard Response (for above discussion) / if any present:"

Comments from Elpida Memory Incorporated

1) Definition of table 40: "Total QODT delay = Y Delay (F[1]RC14)+QODDextended (" should be changed to "Total QODT delay = QODT delay (F[1]RC14) + QODT Dextended"
2) Encoding of table 40: "to Delay Y " should be changed to " to QODT delay " 3) Bottom two row of Table 68, Definition: "Reserved" should be changed to "Vref for MDQ to MB" , and corresponding "Encoding" should be changed from "Reserved to "TBD" Postcard Response (for above discussion) / if any present:"

Comments from FormFactor Inc.

DCS[n:0]# should be DCS[n:0]_n

Postcard Response (for above discussion) / if any present:"

Comments from Inphi Corporation

--Footnote 2 for Table 18 should be included as part of the ballot.

--Table 25 F0RC13 - mapping should be updated as following for bits DA4, DA3.

00b - Default - 8 Ranks; QCS[7:0]_n

01b - 4 Ranks; QCS[3:0]_n

10b - 2 Ranks; QCS[1:0]_n

11b - 1 rank; QCS[0]_n

--Table 27. Footnote for Self Refresh Entry and Self Refresh exit should be included as part of the ballot. Postcard Response (for above discussion) / if any present:"

Comments from Intel Corporation

As DDR3U is not part of JEDEC standard currently, DDR3U reference should be removed from the following tables:

Table 22 F[0]RC10: Encoding for LRDIMM Operating Speed

Table 23 F[0]RC11: Operating Voltage & Parity Calculation Control Word Postcard Response (for above discussion) / if any present:"

PATENT ISSUE:

Netlist may have IP that apply towards this ballot.

Committee Letter Ballot JC-40.4-09-319 Item 142.09

Subject: LRDIMM DDR3 Memory Power Management Chapter Proposal

PATENTS: No known patent issues on the sponsor's part

[Clik here for NB09319-.pdf](#)

Ballot distributed: 11 Nov 2009, Expired: 03 Dec 2009

Sponsor: Mr. John Smolka **Silego Technology** [e-mail \(jsmolka@silego.com\)](mailto:jsmolka@silego.com)

NON FINAL REPORT/ Attend meeting or read minutes for final results.								
Company / voter	Y*	N*	A*	P*	C*	PC*	DoV*	DoR*
21 companies voted	15	0	6	1	3Y			
Advanced Micro Devices Inc. Patel	Y				X	N/A	12/03/09	
Cray Inc. Grossmeier	Y						11/16/09	
Dell Inc. Berke	Y						12/01/09	
Elpida Memory Incorporated Ono	Y						11/26/09	
Hewlett Packard Company Gharaibeh	Y						11/17/09	
Hynix Semiconductor Kim	Y						12/02/09	
IBM Corporation Stout			A				11/20/09	
Inphi Corporation Washkewicz	Y				X	N/A	12/02/09	
Integrated Device Technology Inc. Franklin	Y						12/02/09	
Intel Corporation Tsang	Y				X	N/A	12/03/09	
Kingston Technology Company Inc. Cheng			A				11/23/09	
Legacy Electronics Inc. Mecker			A				12/01/09	
Micron Technology Inc. Graham	Y						11/30/09	
Netlist Inc. Martinez			A	P			12/01/09	
Nvidia Corporation Wagner			A				12/01/09	
NXP Semiconductors Roozeboom	Y						12/01/09	
Samsung Semiconductor Park	Y						12/02/09	
Silego Technology Chung	Y						12/03/09	
Smart Modular Technologies, Inc. Marino			A				12/01/09	
Sun Microsystems Inc. Lee	Y						11/13/09	
Texas Instruments Inc. Harrieder	Y						11/30/09	
* Y = Yes, N = No, A = Abstain, P = Patent(s), C = Comments PC: Postcard, Y = approved response, N = did not approve response, N/A: not available, sponsor and / or voter did not respond, DoV: Date of								

Comments from **Advanced Micro Devices Inc.**

-- Section 8.1.3 - A note should be added which indicates it is not allowed to put half the ranks of a dimm in self refresh while other remaining half ranks in power down mode to simplify buffer test and verification combination. Postcard Response (for above discussion) / if any present:"

Comments from **Inphi Corporation**

--Section 8.1.3 - A note should be added to indicate that it is not allowed to put half the ranks of LRDIMM in self refresh mode while remaining half ranks of LRDIMM in power down mode.
Postcard Response (for above discussion) / if any present:"

Comments from **Intel Corporation**

Attached is the editorial change (ure: sing correct convention for # signals) that TG agreed
Postcard Response (for above discussion) / if any present:"

PATENT ISSUE:

Netlist may have IP that applies towards this ballot

Committee Letter Ballot JC-40.4-09-320 Item 142.35

Subject: LRDIMM DDR3 Memory Initialization Chapter Proposal

PATENTS: No known patent issues on the sponsor's part

[Clik here for NB09320-.pdf](#)

Ballot distributed: 11 Nov 2009, Expired: 03 Dec 2009

Sponsor: Mr. John Smolka **Silego Technology** [e-mail \(jsmolka@silego.com\)](mailto:jsmolka@silego.com)

NON FINAL REPORT/ Attend meeting or read minutes for final results.								
Company / voter	Y*	N*	A*	P*	C*	PC*	DoV*	DoR*
20 companies voted	15	0	5	1	1Y			
Advanced Micro Devices Inc. Patel	Y						12/03/09	
Cray Inc. Grossmeier	Y						11/16/09	
Dell Inc. Berke	Y						12/01/09	
Elpida Memory Incorporated Ono	Y						11/26/09	
Hynix Semiconductor Kim	Y						12/02/09	
IBM Corporation Stout			A				11/20/09	
Inphi Corporation Washkewicz	Y						12/02/09	
Integrated Device Technology Inc. Franklin	Y						12/02/09	
Intel Corporation Tsang	Y				X	N/A	12/03/09	
Kingston Technology Company Inc. Cheng	Y						11/23/09	
Legacy Electronics Inc. Mecker			A				12/01/09	
Micron Technology Inc. Graham	Y						11/30/09	
Netlist Inc. Martinez			A	P			12/01/09	
Nvidia Corporation Wagner			A				12/01/09	
NXP Semiconductors Roozeboom	Y						12/01/09	
Samsung Semiconductor Park	Y						12/02/09	
Silego Technology Chung	Y						12/03/09	
Smart Modular Technologies, Inc. Marino			A				12/02/09	
Sun Microsystems Inc. Lee	Y						11/13/09	
Texas Instruments Inc. Harrieder	Y						11/30/09	
* Y = Yes, N = No, A = Abstain, P = Patent(s), C = Comments PC: Postcard, Y = approved response, N = did not approve response, N/A: not available, sponsor and / or voter did not respond, DoV: Date of Vote								

Comments from **Intel Corporation**

Attached is the editorial change (re: using correct convention for # signals) that TG agreed Postcard Response (for above discussion) / if any present."

PATENT ISSUE:

Netlist may have IP which may apply to this ballot

End of Compilation of Tallies (PDF Format)



December 04 2009 at 09:31:22

Exhibit D



Committee Letter Ballot
JC-45.4-09-321
Item 2192.44
Distributed: 16 Nov 2009
Expiring: 07 Dec 2009



SPONSOR: Avant Technology Inc., represented by Paul Goodwin,
paul_goodwin@avanttechnology.com, (512) 719-6303 413

DISTRIBUTION: Formal Vote: JC-454
Non voting committees: JC-45 (Information and Comments)

Eng. No.: AS 90578

Item No.: 2192.44

SUBJECT: [DDR3 LRDIMM Design Specification Body](#)

BACKGROUND: At the September 2009 Committee meeting the DDR3 LRDIMM TG was given authorization for 1 or more ballots on the LRDIMM Design Specification body and Appendices.
The following LRDIMM Design Specification has Change bars and Highlighted text however the entire specification is being balloted. The change bars and Highlighted areas are difference from the RDIMM specification.

PATENTS: No known patent issues on the sponsor's part

ATTACHMENT: [Download HB09321-.pdf](#)

KEYWORDS: LRDIMM, DIMM, DDR3, MB, Memory Buffer, DRAM, SDRAM, Design, Specification

[\[Top\]](#)



Exhibit E



JEDEC
Solid State Technology Association
2500 Wilson Boulevard
Arlington, Virginia 22201-3834
TEL: (703) 907-7560
FAX: (703) 907-7583
<http://www.jedec.org>



COMMITTEE LETTER BALLOT

Committee: 45.4

Committee Item Number: 2192.44

Subject: DDR3 LRDIMM Design Specification Body

Background: At the September 2009 Committee meeting the DDR3 LRDIMM TG was given authorization for 1 or more ballots on the LRDIMM Design Specification body and Appendices.

The following LRDIMM Design Specification has Change bars and Highlighted text however the **entire specification is being balloted**. The change bars and Highlighted areas are difference from the RDIMM specification.

Keywords: LRDIMM, DIMM, DDR3, MB, Memory Buffer, DRAM, SDRAM, Design, Specification

PC3 Load Reduced DIMM (LRDIMM)

Design Specification

Revision 0.16

November 4, 2009

The following draft contains general sections for DDR3 LRDIMMs.

Proposed

Contents

1. Product Description.....	4
Product Family Attributes.....	4
2. Environmental Requirements.....	5
3. Pinout and Description.....	6
Pin Description.....	6
Input/Output Functional Description.....	7
DDR3 240-pin DIMM Pinout.....	9
Pinout Comparison.....	10
4. Component Details.....	11
Pin Assignments for 512Mb to 8Gb; DDR3 SDRAM.....	12
PACB Pad Array Options for SDRAM Placements.....	16
Pin Assignments for Registering Clock Driver.....	22
Critical Registering Clock Driver Specifications (Reference Only).....	23
Pin Assignments for Serial Presence Detect.....	25
5. DDR3 Registered DIMM Wiring Details.....	26
Signal Groups.....	26
General Net Structure Routing Guidelines.....	26
Test Point.....	28
Explanation of Net Structure Diagrams.....	29
6. Timing Budget.....	30
Example of DDR3 Timing Budget.....	31
7. On Dimm Thermal Sensor.....	32
8. Serial Presence Detect Definition.....	33
9. DDR3 DIMM Label Format.....	36
10. DIMM Mechanical Specifications.....	38
11. Design File Naming Convention.....	39
11. Revision Log.....	40
12. Appendix A.....	Appendix A
13. Raw Card B.....	Appendix B
14. Raw Card C.....	Appendix C

Proposed

15. Raw Card D.....	Appendix D
16. Raw Card E.....	Appendix E
17. Raw Card F.....	Appendix F
18. Raw Card G.....	Appendix G
20. Raw Card J	Appendix J
21. Raw Card K	Appendix K

Proposed

Product Description

This specification defines the electrical and mechanical requirements for 240-pin, 72 bit-wide, Load Reduced Double Data Rate Synchronous DRAM Dual In-Line Memory Modules (DDR3 SDRAM DIMMs). These SDRAM DIMMs are intended for use as main memory when installed in systems such as servers and workstations.

PC3-6400/PC3-8500/PC3-10600/PC3-12800/PC3-14900/PC3-17000 refers to the JEDEC standard DIMM naming convention in which PC3-6400/PC3-8500/PC3-10600/PC3-12800/PC3-14900/PC3-17000 indicates a 240-pin DIMM running at 400/533/666/800/933/1066 MHz clock speed and offering 6400/8500/10600/12800/14900/17000 MB/s bandwidth.

Reference design examples are included which provide an initial basis for Load Reduced DIMM designs. Modifications to these reference designs may be required to meet all system timing, signal integrity, and thermal requirements. All load reduced DIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

The LRDIMM differs from RDIMMs in that the SDRAMs do not connect directly to the edge connector with the exception of VDD and VSS (ground). The Memory Buffer (MB) buffers both address and data. Increased performance is achieved based on the LRDIMM presenting only one load to the system. Increased capacity is achieved since the MB drives only the SDRAMs on the module and therefore a well defined topology and load. The maximum number of SDRAM die is 144. The LRDIMM is intended to function in all RDIMM platforms with appropriate BIOS changes. Systems designed to function with LRDIMMs will be better able to take advantage of LRDIMM features.

While four chip selects are possible at the edge connector the MB provides a "address multiplication" feature. The MB uses one or two of the address lines not directly useable by the SDRAM to generate additional chip selects to the SDRAM. This feature is completely configureable in the MB. There are 2 additional address lines (A16 and A17) defined that will typically only be used with the address multiplication feature. With address multiplication refresh and mode register access become more difficult. This is because the system sees the LRDIMM as fewer logical ranks than the true physical ranks. Rank based commands like refresh and mode register access must accommodate this in some fashion. The MB provides several methods. See the MB Design Specification for more information on the MB features and programming.

The LRDIMM has the option of using ODT0 only or both ODT0 and ODT1.

The VREF_DQ and VREF_CA pins on the edge connector provide the reference for the MB. The MB has additional VREF generators that may be used for the SDRAM reference and as the reference for the MB interfaces.

LRDIMMs can use an address mirroring feature. This is exactly as defined in the UDIMM Design Specification with the exception that all odd ranks are mirrored when this feature is used. There is an SPD bit that provides the information to the system on whether the specific LRDIMM requires the use of address mirroring. Since the wiring on the LRDIMM is different to support this feature it must be used when the LRDIMM is wired to use address mirroring. As defined the controller must have the capability to do address mirroring.

The LRDIMMs are defined to require an integrated thermal sensor with the SPD. Additionally the MB is defined to have an internal thermal sensor.

Proposed

Product Family Attributes

DIMM organization	x72 ECC
DIMM dimensions : height (nom.) x width(nom.) x thickness(max.) / MO-number, Variation	30.35 mm x 133.35 mm x 4.00 mm / MO-269, Variation TBD 30.35 mm x 133.35 mm x 6.75 mm / MO-269, Variation TBD 30.35 mm x 133.35 mm x 7.55 mm / MO-269, Variation TBD 18.75 mm x 133.35 mm x 4.00 mm / MO-269. Variation DB 18.75 mm x 133.35 mm x 4.00 mm / MO-269. Variation EB 18.75 mm x 133.35 mm x 4.00 mm / MO-269. Variation FB
Pin count	240
SDRAMs supported	1 Gb, 2 Gb, 4 Gb
Capacity	4 GB, 8 GB, 16 GB, 32 GB, 64 GB
Serial PD	Consistent with JC 45
Voltage options	1.35 and 1.5 volt (V_{DD}), 3.3 volt (V_{DDSPD})
Interface	1.35 and 1.5 volt signal switching based on reference voltage at $V_{DD}/2$. See DRAM specification for more detail.

Environmental Parameters

DDR3 SDRAM Registered DIMMs are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating temperature	See Note		3
H_{OPR}	Operating humidity (relative)	10 to 90	%	1
T_{STG}	Storage temperature	-50 to +100	°C	1
H_{STG}	Storage humidity (without condensation)	5 to 95	%	1
P_{BAR}	Barometric pressure (operating & storage)	105 to 69	K Pascal	1, 2
1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. 2. Up to 9850 ft. 3. The designer must meet the case temperature specifications for individual module components.				

Proposed

Pinout and Description

Pin Description

Pin Name	Description	Number	Pin Name	Description	Number
CK0_t	Clock Input, positive line	1	Par_In	Parity bit for the Address and Control bus	1
CK0_c	Clock Input, negative line	1	ErrOut_n	Parity error found on the Address and Control bus	1
CK1_t	Clock Input, positive line	1	ODT[0]	On Die Termination Input	1
CK1_c	Clock Input, negative line	1	DQ[63:0]	Data Input/Output	64
CKE[1:0]	Clock Enables	2	CB[7:0]	Data check bits Input/Output	8
CKE[3:2], ODT[1], TEST	Clock Enables On Die Termination Memory bus tool (Not Connected and Not Useable on DIMMs)	2	DQS[8:0]_t	Data strobes	9
RAS_n	Row Address Strobe	1	DQS[8:0]_c	Data strobes, negative line	9
CAS_n	Column Address Strobe	1	DM[8:0]/ DQS[17:9]_t, TDQS[17:9]_t	Data Masks / Data strobes, Termination data strobes	9
WE_n	Write Enable	1	DQS[17:9]_c TDQS[17:9]_c	Data strobes, negative line, Termination data strobes	9
S[1:0]_n	Chip Selects	2	EVENT_n	Reserved for optional hardware temperature sensing	1
S[3:2]_n, A17, A16	Chip Selects Address Inputs	2	TEST	Memory bus test tool (Not Connected and Not Useable on DIMMs)	1
A[9:0],A11, A[15:13]	Address Inputs	14	RESET_n	Register and SDRAM control pin	1
A10/AP	Address Input/Autoprecharge	1	V _{DD}	Power Supply	22
A12/BC_n	Address Input/Burst chop	1	V _{SS}	Ground	59
BA[2:0]	SDRAM Bank Addresses	3	V _{REFDQ}	Reference Voltage for DQ	1
SCL	Serial Presence Detect (SPD) Clock Input	1	V _{REFCA}	Reference Voltage for CA	1
SDA	SPD Data Input/Output	1	V _{TT}	Termination Voltage	4
SA[2:0]	SPD Address Inputs	3	V _{DDSPD}	SPD Power	1

Proposed

Load Reduced DIMM Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0_t	IN	Positive Line	Positive line of the differential pair of system clock inputs that drives input to the on-DIMM Clock Driver.
CK0_c	IN	Negative Line	Negative line of the differential pair of system clock inputs that drives the input to the on-DIMM Clock Driver.
CK1_t	IN	Positive Line	Terminated but not used on RDIMMs.
CK1_c	IN	Negative Line	Terminated but not used on RDIMMs.
CKE[3:0]	IN	Active High	CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers of the SDRAMs. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank)
S[3:0]_n	IN	Active Low	Enables the command decoders for the associated rank of SDRAM when low and disables decoders when high. When decoders are disabled, new commands are ignored and previous operations continue. Other combinations of these input signals perform unique functions, including disabling all outputs (except CKE and ODT) of the register(s) on the DIMM or accessing internal control words in the register device(s). For modules with two registers, S[3:2]_n operate similarly to S[1:0]_n for the second set of register outputs or register control words.
ODT[1:0]	IN	Active High	On-Die Termination control signals
RAS_n, CAS_n, WE_n	IN	Active Low	When sampled at the positive rising edge of the clock, CAS_n, RAS_n, and WE_n define the operation to be executed by the SDRAM.
V _{REFDQ}	Supply		Reference voltage for DQ0-DQ63 and CB0-CB7.
V _{REFCA}	Supply		Reference voltage for A0-A17, BA0-BA2, RAS_n, CAS_n, WE_n, S0_n, S1_n, S2_n, S3_n, CKE0, CKE1, CKE2, CKE3, Par_In, ODT0 and ODT1.
BA[2:0]	IN	—	Selects which SDRAM bank of eight is activated. BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines mode register is to be accessed during an MRS cycle.
A[17:13, 12/BC_n,11, 10/AP_n,9:0]	IN	—	Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA. A12 is also utilized for BL 4/8 identification for "BL on the fly" during CAS_n command. The address inputs also provide the op-code during Mode Register Set commands.
DQ[63:0], CB[7:0]	I/O	—	Data and Check Bit Input/Output pins
DM[8:0]	IN	Active High	Masks write data when high, issued concurrently with input data.
V _{DD} , V _{SS}	Supply		Power and ground for the DDR SDRAM input buffers and core logic.
V _{TT}	Supply		Termination Voltage for Address/Command/Control/Clock nets.
DQS[17:0]_t	I/O	Positive Edge	Positive line of the differential data strobe for input and output data.
DQS[17:0]_c	I/O	Negative Edge	Negative line of the differential data strobe for input and output data.

Proposed

Load Reduced DIMM Input/Output Functional Description (Continued)

Symbol	Type	Polarity	Function
TDQS[17:9]_t TDQS[17:9]_c	OUT		TDQS_t/TDQS_c is applicable for X8 DRAMs only. When enabled via Mode Register A11=1 in MR1, DRAM will enable the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via mode register A11=0 in MR1, DM/TDQS_t will provide the data mask function and TDQS_c is not used. X4/X16 DRAMs must disable the TDQS function via mode register A11=0 in MR1
SA[2:0]	IN	—	These signals are tied at the system planar to either V_{SS} or V_{DDSPD} to configure the serial SPD EEPROM address range.
SDA	I/O	—	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DDSPD} on the system planar to act as a pullup.
SCL	IN	—	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus line to V_{DDSPD} on the system planar to act as a pullup.
EVENT_n	OUT (open drain)	Active Low	This signal indicates that a thermal event has been detected in the thermal sensing device. The system should guarantee the electrical level requirement is met for the EVENT_n pin on TS/SPD part. No pull-up resistor is provided on DIMM.
V_{DDSPD}	Supply		Serial EEPROM positive power supply wired to a separate power pin at the connector which supports from 3.0 Volt to 3.6 Volt (nominal 3.3V) operation.
RESET_n	IN	Active Low	The RESET_n pin is connected to the RESET_n pin on the register and to the RESET_n pin on the DRAM.
Par_In	IN		Parity bit for the Address and Command bus. ("1 ": Odd, "0 ": Even)
ErrOut_n	OUT (open drain)		Parity error detected on the Address and Command bus. A resistor may be connected from ErrOut_n bus line to V_{DD} on the system planar to act as a pull up.
TEST			Used by memory bus analysis tools (unused (NC) on memory DIMMs)

Proposed

DDR3 240-pin LRDIMM, RDIMM and UDIMM Pinout

Pin#	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin#	Front Side	Pin#	Back Side
1	V _{REFDQ}	121	V _{SS}	31	DQ25	151	V _{SS}	61	A2	181	A1	91	DQ41	211	V _{SS}
2	V _{SS}	122	DQ4	32	V _{SS}	152	DM3, DQS12_t, TDQS12_t	62	V _{DD}	182	V _{DD}	92	V _{SS}	212	DM5, DQS14_t, TDQS14_t
3	DQ0	123	DQ5	33	DQS3_c	153	NC,DQS12_c, TDQS12_c	63	NC, CK1_t	183	V _{DD}	93	DQS5_c	213	NC, DQS14_c, TDQS14_c
4	DQ1	124	V _{SS}	34	DQS3_t	154	V _{SS}	64	NC, CK1_c	184	CK0_t	94	DQS5_t	214	V _{SS}
5	V _{SS}	125	DM0,DQS9_t, TDQS9_t	35	V _{SS}	155	DQ30	65	V _{DD}	185	CK0_c	95	V _{SS}	215	DQ46
6	DQS0_c	126	NC,DQS9_c, TDQS9_c	36	DQ26	156	DQ31	66	V _{DD}	186	V _{DD}	96	DQ42	216	DQ47
7	DQS0_t	127	V _{SS}	37	DQ27	157	V _{SS}	67	V _{REFCA}	187	EVENT_n, NC	97	DQ43	217	V _{SS}
8	V _{SS}	128	DQ6	38	V _{SS}	158	CB4,NC	68	Par_In, NC	188	A0	98	V _{SS}	218	DQ52
9	DQ2	129	DQ7	39	CB0,NC	159	CB5,NC	69	V _{DD}	189	V _{DD}	99	DQ48	219	DQ53
10	DQ3	130	V _{SS}	40	CB1,NC	160	V _{SS}	70	A10 / AP	190	BA1	100	DQ49	220	V _{SS}
11	V _{SS}	131	DQ12	41	V _{SS}	161	NC, DM8, DQS17_t, TDQS17_t	71	BA0	191	V _{DD}	101	V _{SS}	221	DM6, DQS15_t, TDQS15_t
12	DQ8	132	DQ13	42	DQS8_c	162	NC,DQS17_c, TDQS17_c	72	V _{DD}	192	RAS_n	102	DQS6_c	222	NC, DQS15_c, TDQS15_c
13	DQ9	133	V _{SS}	43	DQS8_t	163	V _{SS}	73	WE_n	193	S0_n	103	DQS6_t	223	V _{SS}
14	V _{SS}	134	DM1, DQS10_t, TDQS10_t	44	V _{SS}	164	CB6,NC	74	CAS_n	194	V _{DD}	104	V _{SS}	224	DQ54
15	DQS1_c	135	NC, DQS10_c, TDQS10_c	45	CB2,NC	165	CB7,NC	75	V _{DD}	195	ODT0	105	DQ50	225	DQ55
16	DQS1_t	136	V _{SS}	46	CB3,NC	166	V _{SS}	76	S1_n, NC	196	A13	106	DQ51	226	V _{SS}
17	V _{SS}	137	DQ14	47	V _{SS}	167	NC(TEST), CKE2	77	ODT1, CKE3, NC	197	V _{DD}	107	V _{SS}	227	DQ60
18	DQ10	138	DQ15	48	VTT, NC	168	RESET_n	78	V _{DD}	198	S3_n, A17, NC	108	DQ56	228	DQ61
19	DQ11	139	V _{SS}	KEY				79	S2_n, A16, NC	199	V _{SS}	109	DQ57	229	V _{SS}
20	V _{SS}	140	DQ20	49	VTT, NC	169	CKE1, NC	80	V _{SS}	200	DQ36	110	V _{SS}	230	DM7, DQS16_t, TDQS16_t
21	DQ16	141	DQ21	50	CKE0	170	V _{DD}	81	DQ32	201	DQ37	111	DQS7_c	231	NC, DQS16_c, TDQS16_c
22	DQ17	142	V _{SS}	51	V _{DD}	171	A15	82	DQ33	202	V _{SS}	112	DQS7_t	232	V _{SS}
23	V _{SS}	143	DM2, DQS11_t, TDQS11_t	52	BA2	172	A14	83	V _{SS}	203	DM4, DQS13_t, TDQS13_t	113	V _{SS}	233	DQ62
24	DQS2_c	144	NC, DQS11_c, TDQS11_c	53	ErrOut_n NC	173	V _{DD}	84	DQS4_c	204	NC, DQS13_c, TDQS13_c	114	DQ58	234	DQ63
25	DQS2_t	145	V _{SS}	54	V _{DD}	174	A12 / BC_n	85	DQS4_t	205	V _{SS}	115	DQ59	235	V _{SS}
26	V _{SS}	146	DQ22	55	A11	175	A9	86	V _{SS}	206	DQ38	116	V _{SS}	236	VDDSPD
27	DQ18	147	DQ23	56	A7	176	V _{DD}	87	DQ34	207	DQ39	117	SA0	237	SA1
28	DQ19	148	V _{SS}	57	V _{DD}	177	A8	88	DQ35	208	V _{SS}	118	SCL	238	SDA
29	V _{SS}	149	DQ28	58	A5	178	A6	89	V _{SS}	209	DQ44	119	SA2	239	V _{SS}
30	DQ24	150	DQ29	59	A4	179	VDD	90	DQ40	210	DQ45	120	V _{TT}	240	V _{TT}
				60	V _{DD}	180	A3								

Proposed

See Notes on following page for differences of RDIMMs and UDIMMs and LRDIMMs

Pinout Comparison Between UDIMM Type and LRDIMM Type

Pin #	UDIMM		LRDIMM	
	Signal	Notes	Signal	Notes
48, 49	NC	Not used on UDIMMs	VTT	Termination Voltage for Address/Command/Control/Clock nets.
120, 240	VTT	Termination Voltage for Address/Command/Control/Clock nets.	VTT	Termination Voltage for Address/Command/Control/Clock nets.
53	NC	Not used on UDIMMs	ERROut_n	Parity error output of Memory Buffer
63	CK1_t	Used for 2 rank UDIMMs, not used on single-rank UDIMMs, but terminated	CK1_t	Terminated but not used
64	CK1_c		CK1_c	
68	NC	Not used on UDIMMs	Par_In	Parity input to Memory Buffer (MB). This signal is required for MB functionality.
76	S1_n	Used for dual-rank UDIMMs, not connected on single-rank UDIMMs	S1_n	Chip select for the second logical rank. Required for programming the Memory Buffer. SMBus can be used for programming the MB.
77	ODT1, NC	Used for dual-rank UDIMMs, not connected on single-rank UDIMMs	ODT1, CKE3	Provides 4th CKE signal. Not used on JEDEC standard LRDIMMs but may be used on custom LRDIMMs. Connected to MB.
79	NC	Not used on UDIMMs	S2_n, A16	May be used as third chip select or address A16. Use is system dependent. MB can be programmed to use it as chip select 2 or address A16.
167	NC	TEST input used only on bus analysis probes	CKE2	Not used on JEDEC standard LRDIMMs but may be used on custom LRDIMMs.
169	CKE1, NC	Used for dual-rank UDIMMs, not connected on single-rank UDIMMs	CKE1	2nd CKE.
171	A15, NC	Depending on device density, may not be connected to SDRAMs on UDIMMs. However, these signals are terminated on UDIMMs. A15 not routed on some RCs	A15	Always used on LRDIMMs
172	A14		A14	
196	A13		A13	
198	NC	Not used on UDIMMs	S3_n, A17	May be used as either a 4th chip select or address A17. Use is system dependent. MB can be programmed to use it as chip select 3 or address A17.
39, 40, 45, 46, 158, 159, 164, 165	NC, CBn	Used on x72 UDIMMs, (n = 0...7); not used on x64 UDIMMs	CBn	ECC byte. Always used on LRDIMM.
125, 134, 143, 152, 161, 203, 212, 221, 230	DMn	Connected to DM on x8 DRAMs, UDM or LDM on x16 DRAMs on UDIMMs; (n = 0...8)	DQS [9:17]_t	Always connected to MB. Typically used for LRDIMMs with x4 SDRAMs. Not used for LRDIMMs with x8 SDRAMs.
126, 135, 144, 153, 162, 204, 213, 222, 231	NC	Not used on UDIMMs	DQS [9:17]_c	Always connected to MB. Typically used for LRDIMMs with x4 SDRAMs. Not used for LRDIMMs with x8 SDRAMs.
187	EVENT_n NC	Connected to the thermal sensing component on ECC DIMMs. No connection on non-ECC DIMMs.	EVENT_n	Connected to the thermal sensing component and MB.

NC = no internal connection

Proposed

Pinout Comparison Between RDIMM Type and LRDIMM Type

Pin #	RDIMM		LRDIMM	
	Signal	Notes	Signal	Notes
77	ODT1, NC	ODT1 is connected to the register on dual- and quad- rank RDIMMs; NC on single-rank RDIMMs, CKE3 is not available for RDIMMs	ODT1, NC, CKE3	ODT1, CKE3 is connected to the Memory Buffer. It has no defined functionality in normal use but is available for custom applications.
79	S2_n, NC	S2_n is connected to the register on quad-rank RDIMMs, not connected on single or dual rank RDIMMs. A16 is not available for RDIMMs	S2_n, NC, A16	S2_n, A16 is connected to the Memory Buffer. Based on system configuration it may be used as an additional chip select or an addition address input.
167	NC	TEST input used only on bus analysis probes. CKE2 is not available for RDIMMs	NC, CKE2	TEST input used only on bus analysis probes. The CKE2 function is only available on custom modules.
198	S3_n, NC	Connected to the register on quad-rank RDIMMs, not connected on single-or dual-rank RDIMMs	S3_n, NC, A17	S3_n, A17 is connected to the Memory Buffer. Based on system configuration it may be used as an additional chip select or an addition address input.
NC = no internal connection				

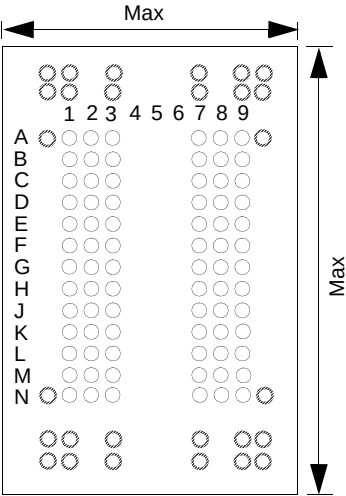
Proposed

Component Details

Supported SDRAM Components Maximum size for 1Gb to 4Gb; DDR3 SDRAM
This table is for reference only. Please see appropriate raw card appendix for more information.

Raw Card	Supported DRAM Outline (Width x Length) max.	Configuration	SDRAM Placement	Package Type	Module Height (mm)	MO-207 variation	# of SDRAM balls supported
A	11.0 mm x 12.0 mm	2 rank x4	2 row vertical	Planar	30.35	DW-z	82
B	11.0 mm x 12.0 mm	4 rank x8	2 row vertical	Planar	30.35	DW-z	82
C	11.0 mm x 11.6 mm	4 rank x4	2 row vertical	DDP	30.35	DW-z	82
D	11.0 mm x 12.0 mm	8 rank x8	2 row vertical	DDP	30.35	DW-z	82
E	11.0 mm x 12.0 mm	8 rank x4	2 row vertical	QDP	30.35	DW-z	82
F	11.0 mm x 12.0 mm	2 rank x4	1 row vertical	DDP	18.75	DW-z	82
G	11.0 mm x 12.0 mm	4 rank x8	1 row vertical	DDP	18.75	DW-z	82
H	11.0 mm x 12.0 mm	4 rank x4	1 row vertical	QDP	18.75	DW-z	82
J	11.0 mm x 12.0 mm	8 rank x8	1 row vertical	QDP	18.75	DW-z	82
K	10.0 mm x 13.0 mm	4 rank x4	2 row flower	DDP	30.35	DW-z	82
	11.0 mm x 12.0 mm						

Note: 1. DDP refers to a 2 die stack. QDP refers to a 4 die stack.



Proposed

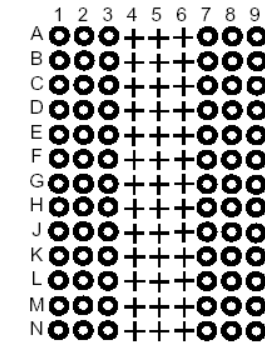
Pin Assignments for 1Gb to 4Gb; DDR3 SDRAM

(MO-207 Variation DT-z/DW-z, FBGA 0.8mm x 0.8 mm pitch)

x4 Ballout of DDR3 SDRAMs (Top view)

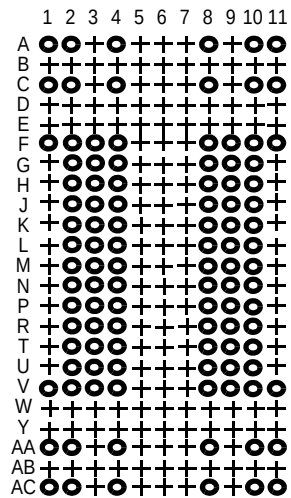
	1	2	3	4	8	9	10	11	
A	NC	NC		NC	NC		NC	NC	
B									
C	NC	NC		NC	NC		NC	NC	
D									
E									
F	NC	VSS	VDD	NC	NC	VSS	VDD	NC	A
G		VSS	VSSQ	DQ0	DM	VSSQ	VDDQ		B
H		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ		C
J		VSSQ	NC	DQS_c	VDD	VSS	VSSQ		D
K		V _{REFDQ}	VDDQ	NC	NC	NC	VDDQ		E
L		NC	VSS	RAS_n	CK_t	VSS	NC		F
M		ODT	VDD	CAS_n	CK_c	VDD	CKE		G
N		NC	CS	WE_n	A10/AP	ZQ	NC		H
P		VSS	BA0	BA2	A15	V _{REFCA}	VSS		J
R		VDD	A3	A0	A12/BC_n	BA1	VDD		K
T		VSS	A5	A2	A1	A4	VSS		L
U		VDD	A7	A9	A11	A6	VDD		M
V	NC	VSS	RESET_n	A13	A14	A8	VSS	NC	N
W									
Y									
AA	NC	NC		NC	NC		NC	NC	
AB									
AC	NC	NC		NC	NC		NC	NC	
		1	2	3	7	8	9		

MO-207 Variation DT-z



● Populated ball
+ Ball not populated

MO-207 Variation DW-z
with support balls



Proposed

Note: 1. Above coordinates of ball out corresponds to footprint on PCB (page 16).

Note: 2. "NC" means that the ball is present and is not connected to any signal in the SDRAM package.

Note: 3. NC balls may be mated with any solder pad on PCB.

Note: 4. This figure is valid for SDRAM specification as defined by JESD79-3. Refer to that specification for any later revisions

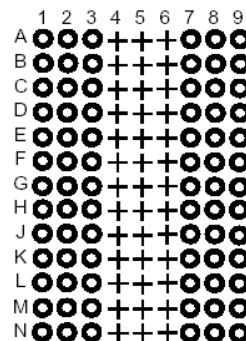
Pin Assignments for 1Gb to 4Gb; DDR3 SDRAM

(MO-207 Variation DT-z/DW-z, FBGA 0.8 mm x 0.8 mm pitch)

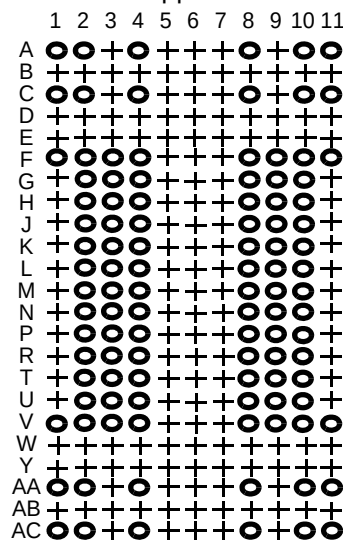
x8 Ballout of DDR3 SDRAMs (Top view)

	1	2	3	4	8	9	10	11	
A	NC	NC		NC	NC		NC	NC	
B									
C	NC	NC		NC	NC		NC	NC	
D									
E									
F	NC	VSS	VDD	NC	NU/ TDQS_c	VSS	VDD	NC	A
G		VSS	VSSQ	DQ0	DM/ TDQS_t	VSSQ	VDDQ		B
H		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ		C
J		VSSQ	DQ6	DQS_c	VDD	VSS	VSSQ		D
K		V _{REFDQ}	VDDQ	DQ4	DQ7	DQ5	VDDQ		E
L		NC	VSS	RAS_n	CK_t	VSS	NC		F
M		ODT	VDD	CAS_n	CK_c	VDD	CKE		G
N		NC	CS#	WE_n	A10/AP	ZQ	NC		H
P		VSS	BA0	BA2	A15	V _{REFCA}	VSS		J
R		VDD	A3	A0	A12/ BC_n	BA1	VDD		K
T		VSS	A5	A2	A1	A4	VSS		L
U		VDD	A7	A9	A11	A6	VDD		M
V	NC	VSS	RESET_n	A13	A14	A8	VSS	NC	N
W									
Y									
AA	NC	NC		NC	NC		NC	NC	
AB									
AC	NC	NC		NC	NC		NC	NC	
		1	2	3	7	8	9		

MO-207 Variation DT-z



MO-207 Variation DW-z
with support balls



Proposed

Note: 1. Above coordinates of ball out corresponds to footprint on PCB (page 21).

Note: 2. "NC" means that the ball is present and is not connected to any signal in the SDRAM package.

Note: 3. NC balls may be mated with any solder pad on PCB.

Note: 4. "NU" means that the ball is present and may or may not be electrically connected to an active signal in the SDRAM package.

Note: 5. NU balls may only be mated with NC solder pads on PCB.

Note: 6. This figure is valid for SDRAM specification as defined by JESD79-3. Refer to that specification for any later revisions.

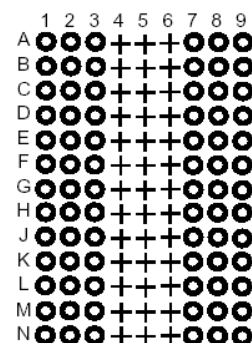
Pin Assignments for 1Gb to 4Gb; DDR3 SDRAM

MO-207 Variation DW-z, FBGA 0.8 mm x 0.8 mm pitch)

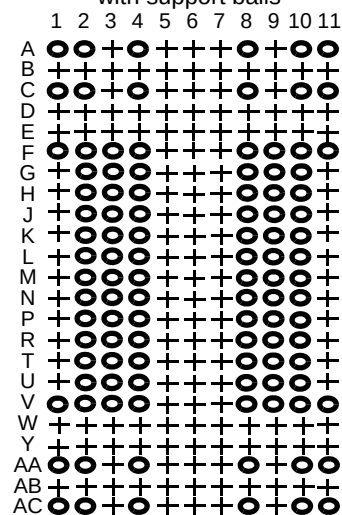
x4 Ballout of DDR3 SDRAMs for DDP Stacked DIMM (Top view)

	1	2	3	4	8	9	10	11	
A	NC	NC		NC	NC		NC	NC	
B									
C	NC	NC		NC	NC		NC	NC	
D									
E									
F	NC	VSS	VDD	NC	NC	VSS	VDD	NC	A
G		VSS	VSSQ	DQ0	DM	VSSQ	VDDQ		B
H		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ		C
J		VSSQ	NC	DQS_c	VDD	VSS	VSSQ		D
K		V _{REFDQ}	VDDQ	NC	NC	NC	VDDQ		E
L		ODT1	VSS	RAS_n	CK_t	VSS	CKE1		F
M		ODT0	VDD	CAS_n	CK_c	VDD	CKE0		G
N		CS1_n	CS0_n	WE_n	A10/AP	ZQ0	ZQ1		H
P		VSS	BA0	BA2	A15	V _{REFCA}	VSS		J
R		VDD	A3	A0	A12/BC_n	BA1	VDD		K
T		VSS	A5	A2	A1	A4	VSS		L
U		VDD	A7	A9	A11	A6	VDD		M
V	NC	VSS	RESET_n	A13	A14	A8	VSS	NC	N
W									
Y									
AA	NC	NC		NC	NC		NC	NC	
AB									
AC	NC	NC		NC	NC		NC	NC	
		1	2	3	7	8	9		

MO-207 Variation DT-z



MO-207 Variation DW-z with support balls



Proposed

Note: 1. Above coordinates of ball out corresponds to footprint on PCB (page 22).

Note: 2. "NC" means that the ball is present and is not connected to any signal in the SDRAM package.

Note: 3. NC balls may be mated with any solder pad on PCB.

Note: 4. This figure is valid for SDRAM specification as defined by JESD79-3. Refer to that specification for any later revisions.

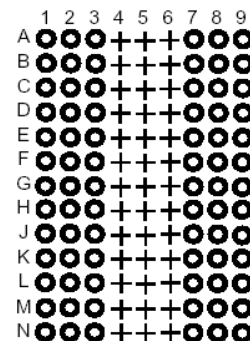
Pin Assignments for 1Gb to 4Gb; DDR3 SDRAM

MO-207 Variation DW-z, FBGA 0.8 mm x 0.8 mm pitch)

x8 Ballout of DDR3 SDRAMs for Stacked DDP DIMM (Top view)

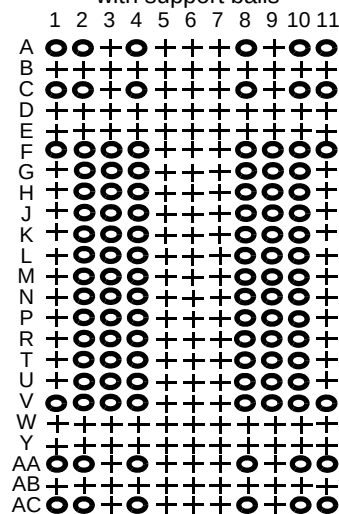
	1	2	3	4	8	9	10	11	
A	NC	NC		NC	NC		NC	NC	
B									
C	NC	NC		NC	NC		NC	NC	
D									
E									
F	NC	VSS	VDD	NC	NU/ TDQS_c	VSS	VDD	NC	A
G		VSS	VSSQ	DQ0	DM/ TSDQS_t	VSSQ	VDDQ		B
H		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ		C
J		VSSQ	DQ6	DQS_c	VDD	VSS	VSSQ		D
K		V _{REFDQ}	VDDQ	DQ4	DQ7	DQ5	VDDQ		E
L		ODT1	VSS	RAS_n	CK_t	VSS	CKE1		F
M		ODT0	VDD	CAS_n	CK_c	VDD	CKE0		G
N		CS1_n	CS0_n	WE_n	A10/AP	ZQ0	ZQ1		H
P		VSS	BA0	BA2	A15	V _{REFCA}	VSS		J
R		VDD	A3	A0	A12/BC_n	BA1	VDD		K
T		VSS	A5	A2	A1	A4	VSS		L
U		VDD	A7	A9	A11	A6	VDD		M
V	NC	VSS	RESET_n	A13	A14	A8	VSS	NC	N
W									
Y									
AA	NC	NC		NC	NC		NC	NC	
AB									
AC	NC	NC		NC	NC		NC	NC	
		1	2	3	7	8	9		

MO-207 Variation DT-z



● Populated ball
+ Ball not populated

MO-207 Variation DW-z
with support balls



Proposed

Note: 1. Above coordinates of ball out corresponds to footprint on PCB (page 22).

Note: 2. "NC" means that the ball is present and is not connected to any signal in the SDRAM package.

Note: 3. NC balls may be mated with any solder pad on PCB.

Note: 4. This figure is valid for SDRAM specification as defined by JESD79-3. Refer to that specification for any later revisions.

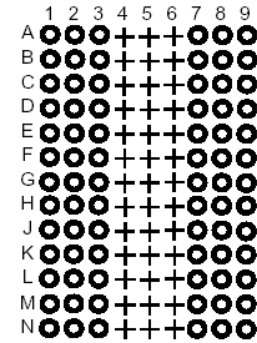
Pin Assignments for 1Gb to 4Gb; DDR3 SDRAM

MO-207 Variation DW-z, FBGA 0.8 mm x 0.8 mm pitch)

x4 Ballout of DDR3 SDRAMs for Stacked QDP DIMM (Top view)

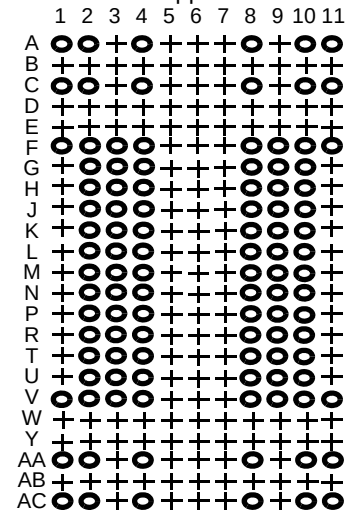
	1	2	3	4	8	9	10	11	
A	NC	NC		NC	NC		NC	NC	
B									
C	NC	NC		NC	NC		NC	NC	
D									
E									
F	NC	VSS	VDD	NC	NU/ TDQS_c	VSS	VDD	NC	A
G		VSS	VSSQ	DQ0	DM/ TSDQS_t	VSSQ	VDDQ		B
H		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ		C
J		VSSQ	DQ6	DQS_c	VDD	VSS	VSSQ		D
K		V _{REFDQ}	VDDQ	DQ4	DQ7	DQ5	VDDQ		E
L		ODT1	VSS	RAS_n	CK_t	VSS	CKE1		F
M		ODT0	VDD	CAS_n	CK_c	VDD	CKE0		G
N		CS1_n	CS0_n	WE_n	A10/AP	ZQ0	ZQ1		H
P		VSS	BA0	BA2	A15	V _{REFCA}	VSS		J
R		VDD	A3	A0	A12/BC_n	BA1	VDD		K
T		VSS	A5	A2	A1	A4	VSS		L
U		VDD	A7	A9	A11	A6	VDD		M
V	NC	VSS	RESET_n	A13	A14	A8	VSS	NC	N
W									
Y									
AA	NC	NC		NC	NC		NC	NC	
AB									
AC	NC	NC		NC	NC		NC	NC	
		1	2	3	7	8	9		

MO-207 Variation DT-z



● Populated ball
+ Ball not populated

MO-207 Variation DW-z
with support balls



Proposed

Note: 1. Above coordinates of ball out corresponds to footprint on PCB (page 16).

Note: 2. "NC" means that the ball is present and is not connected to any signal in the SDRAM package.

Note: 3. NC balls may be mated with any solder pad on PCB.

Note: 4. This figure is valid for SDRAM specification as defined by JESD79-3. Refer to that specification for any later revisions

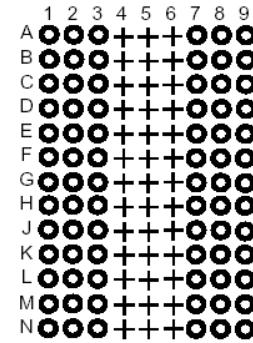
Pin Assignments for 1Gb to 4Gb; DDR3 SDRAM

MO-207 Variation DW-z, FBGA 0.8 mm x 0.8 mm pitch)

x8 Ballout of DDR3 SDRAMs for Stacked QDP DIMM (Top view)

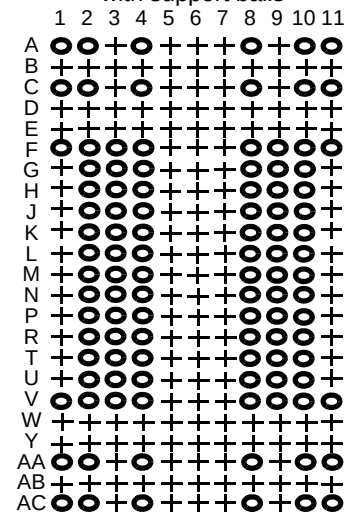
	1	2	3	4	8	9	10	11	
A	NC	NC		NC	NC		NC	NC	
B									
C	NC	NC		NC	NC		NC	NC	
D									
E									
F	NC	VSS	VDD	NC	NU/ TDQS_c	VSS	VDD	NC	A
G		VSS	VSSQ	DQ0	DM/ TSDQS_t	VSSQ	VDDQ		B
H		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ		C
J		VSSQ	DQ6	DQS_c	VDD	VSS	VSSQ		D
K		V _{REFDQ}	VDDQ	DQ4	DQ7	DQ5	VDDQ		E
L		ODT1	VSS	RAS_n	CK_t	VSS	CKE1		F
M		ODT0	VDD	CAS_n	CK_c	VDD	CKE0		G
N		CS1_n	CS0_n	WE_n	A10/AP	ZQ0	ZQ1		H
P		VSS	BA0	BA2	A15	V _{REFCA}	VSS		J
R		CS2_n	A3	A0	A12/BC_n	BA1	ZQ2		K
T		CS3_n	A5	A2	A1	A4	ZQ3		L
U		VDD	A7	A9	A11	A6	VDD		M
V	NC	VSS	RESET_n	A13	A14	A8	VSS	NC	N
W									
Y									
AA	NC	NC		NC	NC		NC	NC	
AB									
AC	NC	NC		NC	NC		NC	NC	
		1	2	3	7	8	9		

MO-207 Variation DT-z



● Populated ball
+ Ball not populated

MO-207 Variation DW-z
with support balls



Proposed

Note: 1. Above coordinates of ball out corresponds to footprint on PCB (page 16).

Note: 2. "NC" means that the ball is present and is not connected to any signal in the SDRAM package.

Note: 3. NC balls may be mated with any solder pad on PCB.

Note: 4. This figure is valid for SDRAM specification as defined by JESD79-3. Refer to that specification for any later revisions

PCB Pad Array Options for SDRAM Placements

MO-207 Variation DW-z allows any of the support balls locations to be non-populated. Many raw cards use the 72-pad array and thus support DRAM with four mechanical balls attached. The number of pads actually used is dependent on the package size of the DRAMs applied to the module. The 68-pad array corresponds with MO-207 Variation DT-z.

There are five basic pad arrays: x4 pad array, x8 pad array, x4 pad array DDP stacked, x8 pad array DDP stacked and x4 pad array QDP stacked. Each of these pad arrays may have a ball count variation. Below is a description of these 2 variations found on currently established raw card reference designs:

- 78-pad array (Variation DT-z, or DW-z with no support balls)
- 82-pad array (Variation DW-z with 4 support balls)

Proposed

x4 SDRAM Pad Array

(Top view)

		1	2	3	7	8	9	
	NC	NC		NC	NC		NC	NC
	NC	NC		NC	NC		NC	NC
A	NC	VSS	VDD	NC	NC	VSS	VDD	NC
B		VSS	VSSQ	DQ0	DM	VSSQ	VDDQ	
C		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ	
D		VSSQ	NC	DQS_c	VDD	VSS	VSSQ	
E		V _{REFDQ}	VDDQ	NC	NC	NC	VDDQ	
F		NC	VSS	RAS_n	CK_t	VSS	NC	
G		ODT	VDD	CAS_n	CK_c	VDD	CKE	
H		NC	CS_n	WE_n	A10/AP	ZQ	NC	
J		VSS	BA0	BA2	A15	V _{REFCA}	VSS	
K		VDD	A3	A0	A12/ BC_n	BA1	VDD	
L		VSS	A5	A2	A1	A4	VSS	
M		VDD	A7	A9	A11	A6	VDD	
N	NC	VSS	RESET_n	A13	A14	A8	VSS	NC
	NC	NC		NC	NC		NC	NC
	NC	NC		NC	NC		NC	NC

106-pad array (black outline)
(See MO-207, Variation DW-z)
(Includes all mechanical support balls)

78-pad array (yellow background)
(See MO-207, Variation DT-z)
(Includes no mechanical support balls)

82-pad array (light blue background)
(See MO-207, Variation DW-z)
(Includes 4 mechanical support balls)

Proposed

Note: 1. Above coordinates of footprint corresponds to previous ballout of DDR3 SDRAMs.

Note: 2. "NC" means that a solder pad is present and is not connected to any signal on the PCB.

Note: 3. NC solder pads may be mated with any balls of an SDRAM.

x8 SDRAM Pad Array

(Top view)

		1	2	3	7	8	9	
	NC	NC		NC	NC		NC	NC
	NC	NC		NC	NC		NC	NC
A	NC	VSS	VDD	NC	NU/ TDQS_c	VSS	VDD	NC
B		VSS	VSSQ	DQ0	DM/ TDQS_t	VSSQ	VDDQ	
C		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ	
D		VSSQ	DQ6	DQS_c	VDD	VSS	VSSQ	
E		V _{REFDQ}	VDDQ	DQ4	DQ7	DQ5	VDDQ	
F		NC	VSS	RAS_n	CK_t	VSS	NC	
G		ODT	VDD	CAS_n	CK_c	VDD	CKE	
H		NC	CS_n	WE_n	A10/AP	ZQ	NC	
J		VSS	BA0	BA2	A15	V _{REFCA}	VSS	
K		VDD	A3	A0	A12/BC_n	BA1	VDD	
L		VSS	A5	A2	A1	A4	VSS	
M		VDD	A7	A9	A11	A6	VDD	
N	NC	VSS	RESET_n	A13	A14	A8	VSS	NC
	NC	NC		NC	NC		NC	NC
	NC	NC		NC	NC		NC	NC

106-pad array (black outline)
(See MO-207, Variation DW-z)
(Includes all mechanical support balls)

78-pad array (yellow background)
(See MO-207, Variation DT-z)
(Includes no mechanical support balls)

82-pad array (light blue background)
(See MO-207, Variation DW-z)
(Includes 4 mechanical support balls)

Proposed

Note: 1. Above coordinates of footprint corresponds to previous ballout of DDR3 SDRAMs.

Note: 2. "NC" means that a solder pad is present and is not connected to any signal on the PCB.

Note: 3. NC solder pads may be mated with any balls of an SDRAM.

x4 SDRAM Pad Array DDP Stacked

(Top view)

		1	2	3	7	8	9	
	NC	NC		NC	NC		NC	NC
	NC	NC		NC	NC		NC	NC
A	NC	VSS	VDD	NC	NC	VSS	VDD	NC
B		VSS	VSSQ	DQ0	DM	VSSQ	VDDQ	
C		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ	
D		VSSQ	NC	DQS_c	VDD	VSS	VSSQ	
E		V _{REFDQ}	VDDQ	NC	NC	NC	VDDQ	
F		ODT1	VSS	RAS_n	CK_t	VSS	CKE1	
G		ODT0	VDD	CAS_n	CK_c	VDD	CKE0	
H		CS1_n	CS0_n	WE_n	A10/AP	ZQ0	ZQ1	
J		VSS	BA0	BA2	A15	V _{REFCA}	VSS	
K		VDD	A3	A0	A12/BC_n	BA1	VDD	
L		VSS	A5	A2	A1	A4	VSS	
M		VDD	A7	A9	A11	A6	VDD	
N	NC	VSS	RESET_n	A13	A14	A8	VSS	NC
	NC	NC		NC	NC		NC	NC
	NC	NC		NC	NC		NC	NC

106-pad array (black outline)
(See MO-207, Variation DW-z)
(Includes all mechanical support balls)

78-pad array (yellow background)
(See MO-207, Variation DT-z)
(Includes no mechanical support balls)

82-pad array (light blue background)
(See MO-207, Variation DW-z)
(Includes 4 mechanical support balls)

Proposed

Note: 1. Above coordinates of footprint corresponds to previous ballout of DDR3 SDRAMs.

Note: 2. "NC" means that a solder pad is present and is not connected to any signal on the PCB.

Note: 3. NC solder pads may be mated with any balls of an SDRAM.

x8 SDRAM Pad Array DDP Stacked

(Top view)

		1	2	3	7	8	9	
	NC	NC		NC	NC		NC	NC
	NC	NC		NC	NC		NC	NC
A	NC	VSS	VDD	NC	NU/ TDQS_c	VSS	VDD	NC
B		VSS	VSSQ	DQ0	DM/ TDQS_t	VSSQ	VDDQ	
C		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ	
D		VSSQ	DQ6	DQS_c	VDD	VSS	VSSQ	
E		V _{REFDQ}	VDDQ	DQ4	DQ7	DQ5	VDDQ	
F		ODT1	VSS	RAS_n	CK_t	VSS	CKE1	
G		ODT0	VDD	CAS_n	CK_c	VDD	CKE0	
H		CS1_n	CS0_n	WE_n	A10/AP	ZQ0	ZQ1	
J		VSS	BA0	BA2	A15	V _{REFCA}	VSS	
K		VDD	A3	A0	A12/BC_n	BA1	VDD	
L		VSS	A5	A2	A1	A4	VSS	
M		VDD	A7	A9	A11	A6	VDD	
N	NC	VSS	RESET_n	A13	A14	A8	VSS	NC
	NC	NC		NC	NC		NC	NC
	NC	NC		NC	NC		NC	NC

106-pad array (black outline)
(See MO-207, Variation DW-z)
(Includes all mechanical support balls)

78-pad array (yellow background)
(See MO-207, Variation DT-z)
(Includes no mechanical support balls)

82-pad array (light blue background)
(See MO-207, Variation DW-z)
(Includes 4 mechanical support balls)

Note: 1. Above coordinates of footprint corresponds to previous ballout of DDR3 SDRAMs.

Note: 2. "NC" means that a solder pad is present and is not connected to any signal on the PCB.

Note: 3. NC solder pads may be mated with any balls of an SDRAM.

Proposed

x4 SDRAM Pad Array QDP Stacked

(Top view)

		1	2	3	7	8	9	
	NC	NC		NC	NC		NC	NC
	NC	NC		NC	NC		NC	NC
A	NC	VSS	VDD	NC	NU/ TDQS_c	VSS	VDD	NC
B		VSS	VSSQ	DQ0	DM/ TDQS_t	VSSQ	VDDQ	
C		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ	
D		VSSQ	DQ6	DQS_c	VDD	VSS	VSSQ	
E		V _{REFDQ}	VDDQ	DQ4	DQ7	DQ5	VDDQ	
F		ODT1	VSS	RAS_n	CK_t	VSS	CKE1	
G		ODT0	VDD	CAS_n	CK_c	VDD	CKE0	
H		CS1_n	CS0_n	WE_n	A10/AP	ZQ0	ZQ1	
J		VSS	BA0	BA2	A15	V _{REFCA}	VSS	
K		VDD	A3	A0	A12/BC_n	BA1	VDD	
L		VSS	A5	A2	A1	A4	VSS	
M		VDD	A7	A9	A11	A6	VDD	
N	NC	VSS	RESET_n	A13	A14	A8	VSS	NC
	NC	NC		NC	NC		NC	NC
	NC	NC		NC	NC		NC	NC

106-pad array (black outline)
(See MO-207, Variation DW-z)
(Includes all mechanical support balls)

78-pad array (yellow background)
(See MO-207, Variation DT-z)
(Includes no mechanical support balls)

82-pad array (light blue background)
(See MO-207, Variation DW-z)
(Includes 4 mechanical support balls)

Proposed

x8 SDRAM Pad Array QDP Stacked

(Top view)

		1	2	3	7	8	9	
	NC	NC		NC	NC		NC	NC
	NC	NC		NC	NC		NC	NC
A	NC	VSS	VDD	NC	NU/ TDQS_c	VSS	VDD	NC
B		VSS	VSSQ	DQ0	DM/ TDQS_t	VSSQ	VDDQ	
C		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ	
D		VSSQ	DQ6	DQS_c	VDD	VSS	VSSQ	
E		V _{REFDQ}	VDDQ	DQ4	DQ7	DQ5	VDDQ	
F		ODT1	VSS	RAS_n	CK_t	VSS	CKE1	
G		ODT0	VDD	CAS_n	CK_c	VDD	CKE0	
H		CS1_n	CS0_n	WE_n	A10/AP	ZQ0	ZQ1	
J		VSS	BA0	BA2	A15	V _{REFCA}	VSS	
K		CS2_n	A3	A0	A12/BC_n	BA1	ZQ2	
L		CS3_n	A5	A2	A1	A4	ZQ3	
M		VDD	A7	A9	A11	A6	VDD	
N	NC	VSS	RESET_n	A13	A14	A8	VSS	NC
	NC	NC		NC	NC		NC	NC
	NC	NC		NC	NC		NC	NC

106-pad array (black outline)
(See MO-207, Variation DW-z)
(Includes all mechanical support balls)

78-pad array (yellow background)
(See MO-207, Variation DT-z)
(Includes no mechanical support balls)

82-pad array (light blue background)
(See MO-207, Variation DW-z)
(Includes 4 mechanical support balls)

Proposed

Pin Assignments for Memory Buffer

Memory Buffer (Top View)

588-Ball TFBGA 0.65 x 0.65 mm pitch [MO-XXX Variation X]

Left Side (1 of 3)

	A	B	C	D	E	F	G	H	J	K	L	M	N
20	NB	NB	VSS	DQ7	DQS9_t	DQ2	DQ3	VDD	DQ68	DQS17_t	DQ70	VSS	DQ66
19	NB	VSS	DQ4	DQ6	DQS9_c	VSS	DQ1	VSS	DQ69	DQS17_c	DQ71	VSS	DQ67
18	VSS	VDD	VSS	DQ5	DQS0_c	DQ0	NB	NB	NB	NB	NB	DQS8_t	DQ64
17	MDQ5	MDQ4	MDQ0	VSS	DQS0_t	VSS	NB	NB	NB	NB	NB	DQS8_c	DQ65
16	MDQS9_t	MDQS9_c	MDQS0_c	MDQS0_t	VDD	QACAS_n	NB	NB	NB	NB	NB	VDD	VDD
15	MDQ6	MDQ7	MDQ2	MDQ1	VDD	QARAS_n	NB	NB	NB	NB	NB	QAEC2	QAEC6
14	VSS	VSS	VSS	MDQ3	VDD	QAA15	NB	NB	NB	NB	NB	VDD	VDD
13	DQS1_t	DQS1_c	VSS	VDD	QAA10	QACKE1	NB	NB	NB	NB	NB	QAWEn	VDD
12	VDD	VSS	DQ8	VDD	QACKE0	QAA12	NB	NB	NB	NB	NB	QABA0	QABA2
11	DQ11	DQ10	DQ9	VDD	QABA1	QACKE2	NB	NB	NB	NB	NB	QAA0	VDD
10	DQ15	DQ14	DQ13	VDD	QACKE3	QAA4	NB	NB	NB	NB	NB	QAA3	QACS0_n QCS0_n
9	VDD	VSS	DQ12	VDD	QAA1	QAA5	NB	NB	NB	NB	NB	QACS3_n QCS3_n	QACS2_n QCS2_n
8	DQS10_t	DQS10_c	VSS	VDD	VDD	QAA11	NB	NB	NB	NB	NB	QAA5	QAA2
7	VSS	VSS	VSS	MDQ9	VDD	QAA8	NB	NB	NB	NB	NB	QA13	QAA9
6	MDQ12	MDQ13	MDQ8	MDQ11	VDD	QAA14	NB	NB	NB	NB	NB	QAA7	VDD
5	MDQS10_t	MDQS10_c	MDQS1_c	MDQS1_t	VSS	VDD	NB	NB	NB	NB	NB	VDD	VSS
4	MDQ14	MDQ15	MDQ10	VSS	DQS2_t	DQ16	NB	NB	NB	NB	NB	MDQS2_c	VSS
3	VSS	VDD	VSS	DQ19	DQS2_c	DQ17	NB	NB	NB	NB	NB	MDQS2_t	VSS
2	NB	VSS	DQ18	DQ22	DQS11_c	DQ20	VSS	MDQ20	MDQS11_c	MDQ22	VSS	MDQ16	MDQ18
1	NB	NB	VSS	DQ23	DQS11_t	DQ21	VSS	MDQ21	MDQS11_t	MDQ23	VSS	MDQ17	MDQ19
	A	B	C	D	E	F	G	H	J	K	L	M	N

Proposed

Middle (2 of 3)

	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE
20	VDD	Y3_c	Y3_t	Y1_t	Y1_c	Y2_c	Y2_t	Y0_t	Y0_c	VDD	ZQ	SCL
19	VDD	VSS	PVDD	VSS	PVDD	VSS	PVDD	VSS	PVDD	VSS	ZQVSS	SDA
18	VSS	MDQ68	MDQS17_t	MDQ70	MDQ64	MDQS8_c	MDQ66	VSS	CK_t	CK_c	VSS	VDD
17	VSS	MDQ69	MDQS17_c	MDQ71	MDQ65	MDQS8_t	MDQ67	TEST(0)	AVSS	AVDD	AOUT	TEST(2)
16	VDD	VSS	VDD	VSS	VDD	VSS	VDD	TEST(1)	VDD	VSS	VDD	VSS
15	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD
14	QAECC9	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS
13	QAODT1	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	QBCKE1
12	QAODT0	VSS	RESET_n	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	QBCKE0
11	VSS	VDD	DCKE2	VDD	DA1	VDD	VSS	DCS2_n	DCS4_n	DCS3_n	VSS	QBCKE3
10	QACS1_n QSC1_n	QRST_n	DCKE1	DA12	DA6	DA4	DA2	DA13	DCS0_n	DCS5_n	DBA1	VDD
9	VDD	DCKE0	DBA2	DA11	DA3	DA5	PAR_IN	DODT0	DA0	DBA0	DODT1 DCKE3	VSS
8	VDD	DA15	DA14	DA9	DA8	DA7	DCS1_n	DCAS_n	DRAS_n	DA10	DCS6_n	DCS7_n
7	VDD	VDD	ERROUT_n	VDD	VDD	VDD	VDD	VDD	VDD	DWE_n	VDD	VDD
6	DQ24	DQ25	VSS	MDQ29	MDQS12_t	VSS	MDQ36	MDQS13_t	MDQ37	VSS	DQ32	DQ33
5	DQS3_t	DQS3_c	VSS	MDQ30	MDQS12_c	MDQ28	VSS	MDQS13_c	MDQ38	VSS	DQS4_t	DQS4_c
4	DQ26	DQ27	VSS	MDQ31	MDQS3_c	VSS	MDQ32	MDQS4_c	MDQ39	VSS	DQ34	DQ35
3	VDD	DQ28	DQ29	VSS	MDQS3_t	MDQ24	VSS	MDQS4_t	VSS	DQ36	DQ37	VDD
2	VSS	DQS12_t	DQS12_c	VSS	MDQ25	VSS	MDQ33	MDQ34	VSS	DQS13_t	DQS13_c	VSS
1	VSS	DQ30	DQ31	VSS	MDQ26	MDQ27	VSS	MDQ35	VSS	DQ38	DQ39	VSS
	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE

Proposed

Right Side (3 of 3)

	AF	AG	AH	AJ	AK	AL	AM	AN	AP	AR	AT	AU	AV
20	SA2	SA0	QVREF CA	VDD	QVREF DQ	VDD	DQ59	DQ58	DQS7_t	DQ63	VSS	NB	NB
19	VCCSPD	SA1	VREFCA	VSS	VREF DQ	VSS	DQ57	VSS	DQS7_c	DQ62	DQ60	VSS	NB
18	EVENT_n	BFUNC	NB	NB	NB	NB	NB	DQ56	DQS16_c	DQ61	VSS	VDD	VSS
17	VSS	VDD	NB	NB	NB	NB	NB	VSS	DQS16_t	VSS	MDQ58	MDQ63	MDQ62
16	VDD	VSS	NB	NB	NB	NB	NB	QBWE_n	VDD	MDQS7_t	MDQS7_c	MDQS16_c	MDQS16_t
15	QBCAS_n	QBRAS_n	NB	NB	NB	NB	NB	QBBA0	VDD	MDQ59	MDQ57	MDQ61	MDQ60
14	VDD	VDD	NB	NB	NB	NB	NB	QBA0	VDD	MDQ56	VSS	VSS	VSS
13	QBA10	QBA15	NB	NB	NB	NB	NB	QBA3	QBODT1	VDD	VSS	DQS6_c	DQS6_t
12	VDD	VDD	NB	NB	NB	NB	NB	QBA2	QBBA2	VDD	DQ48	VSS	VDD
11	QBBA1	QBA12	NB	NB	NB	NB	NB	QBA5	QBODT0	VDD	DQ49	DQ50	DQ51
10	QBCKE2	QBA4	NB	NB	NB	NB	NB	QBCS1_n QCS5_n	QBCS0_n QCS4_n	VDD	DQ53	DQ54	DQ55
9	QBA1	QBA6	NB	NB	NB	NB	NB	QBCS3_n QCS7_n	QBCS2_n QCS6_n	VDD	DQ52	VSS	VDD
8	VDD	VDD	NB	NB	NB	NB	NB	QBA9	VDD	VDD	VSS	DQS15_c	DQS15_t
7	QBA11	QBA8	NB	NB	NB	NB	NB	QBA13	VDD	MDQ51	VSS	VSS	VSS
6	VDD	QBA14	NB	NB	NB	NB	NB	QBA7	VDD	MDQ49	MDQ50	MDQ55	MDQ54
5	VSS	VDD	NB	NB	NB	NB	NB	VDD	VSS	MDQS6_t	MDQS6_c	MDQS15_c	MDQS15_t
4	VSS	MDQS5_c	NB	NB	NB	NB	NB	DQ40	DQS5_t	VSS	MDQ48	MDQ53	MDQ52
3	VSS	MDQS5_t	NB	NB	NB	NB	NB	DQ41	DQS5_c	DQ45	VSS	VDD	VSS
2	MDQ40	MDQ43	VSS	MDQ44	MDQS14_t	MDQ47	VSS	DQ42	DQS14_c	DQ46	DQ44	VSS	NB
1	MDQ41	MDQ42	VSS	MDQ45	MDQS14_c	MDQ46	VSS	DQ43	DQS14_t	DQ47	VSS	NB	NB
	AF	AG	AH	AJ	AK	AL	AM	AN	AP	AR	AT	AU	AV

Proposed

Pin Assignments for Serial Presence Detect

(MO-229 Variation V/WCED-3, 2x3 mm package, 8 lead DFN 0.5 mm pitch)

(MO-229 Variation V/WEED-7, 3x3 mm package, 8 lead DFN 0.5 mm pitch)

256-byte Serial Presence Detect device, TSE2002 with thermal sensor

SPD Pinout (Top view)

TSE2002			
1	SA0	VDDSPD	8
2	SA1	EVENT	7
3	SA2	SCL	6
4	VSSSPD	SDA	5

Note: 1. Above rotations of leads correspond to footprints on PCB.

Note: 2. Refer to *JESD21C-4.1.2 -- SERIAL PRESENCE DETECT STANDARD*, General Standard for landing pattern details.

Proposed

DDR3 Load Reduced DIMM Wiring Details

Signal Groups

This specification categorizes timing-critical signals into eight groups. The following table summarizes the signals contained in each group.

Signal Group	Signals In Group
Clock Driver Input / Unused Clocks	CK0_t, CK0_c / CK1_t, CK1_c
Clock Driver Output	Yx_t, Yx_c
Pre-MB Data, DQS_t, DQS_c	DQ[63:0], CB[7:0], DQS[17:0_t], DQS[17:0]_c, DM[8:0]/ TDQS[17:9]_t, TDQS[17:9]_c
Post-MB Data, MDQS_t, MDQS_c	MDQ[71:0], MDQS[17:0_t], MDQS[17:0]_c,
Pre-MB Address and Control (Chip Select, Clock Enable, Parity, ODT)	A[15:0], BA[2:0], RAS_n, CAS_n, WE_n CS[3:0]_n, CKE[1:0], Par_In, ODT[1:0]
Post-MB Address and Control	QA[15..0], QBA[2..0], QRAS_n, QCAS_n, QWE_n, QCS[3:0]_n, QCKE[1:0], QODT[1:0]
Address and Command Parity	ErrOut_n
RESET_n	RESET_n

General Net Structure Routing Guidelines

Net structures and lengths must satisfy signal quality and setup/hold time requirements for the memory interface. Net structure diagrams for each signal group are shown in the following sections. Each diagram is accompanied by a trace length table that lists the minimum and maximum allowable lengths for each trace segment and/or net.

The general routing guidelines are as follows

- Route all signal traces except clocks using minimum of 0.075/0.1 rules, i.e., 0.075 mm traces and 0.1 mm minimum spacing between adjacent traces. But spacing should be as wide as possible to prevent crosstalk.
- Route clocks using minimum of 0.075 mm lines and 0.1 mm spaces between differential clock pairs and differential DQS_t, DQS_c.
- Route clocks using at least 90% of the total trace length in the inner layers. Maximize use of internal layers for routing clocks. Surface routing should be minimized and limited to what is necessary to connect to component.
- Signals are referenced to Vss or Vdd on adjacent layers. Data signals are referenced to Vss. Address and Command signals are referenced to VDD.
-

Signal referencing information

Signal groups	Referencing	Signal groups	Referencing
Pre-MB DQ/DQS pair	Ground layer	Pre-MB address and command net	Vdd shape
Post-MB MDQ/MDQS pair	Ground layer	Post-MB address and command net	Vdd shape
Clock nets	Vdd shape		

Differential Clock Net Structures

CK0_t, CK0_c, Yx_t, Yx_c

DDR3 SDRAM clock signals must be carefully routed to meet the following requirements:

- Signal quality
- Rise/Fall time
- Cross point of the differential pair into the SDRAM and register
- JEDEC-compatible reference delays
- Minimal segment length differences (less than 2.54 mm total) between clocks of the same function

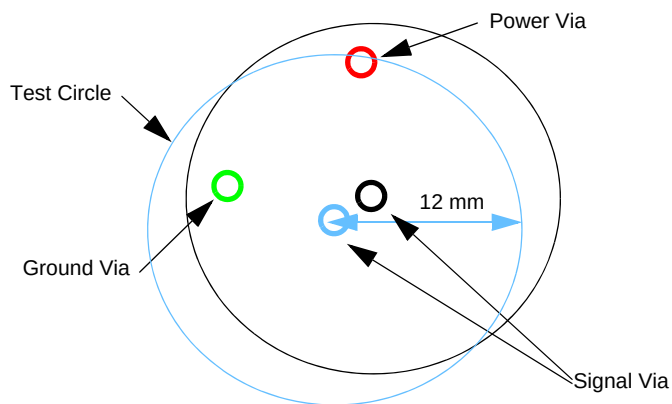
Clock Driver input net segment length is newly defined and optimized for high speed DDR3 Load Reduced DIMMs.

Proposed

Test Points

All DDR3 components are in BGA packages which makes the package pads inaccessible for probing during system development. The DDR3 Registered DIMMs have test points identified to make initial evaluation easier. In some cases test pads have been added and in other cases existing vias are used as test points. An effort has been made to provide testability on some signals in all signal groups but 100% coverage is not possible. All test points must have a power and/or ground via within 12 mm. Test point location and /or availability are indicated for each raw card in the corresponding appendices.

Test Point Location



Proposed

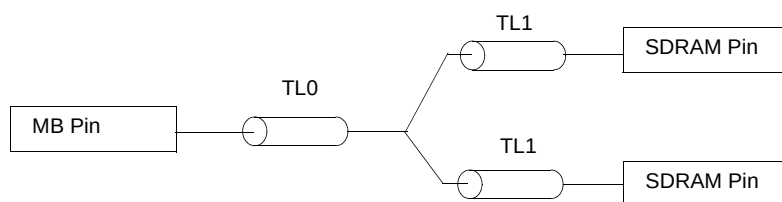
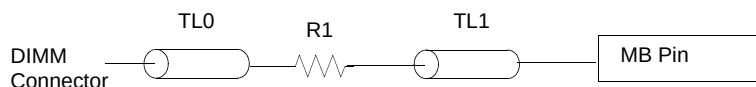
Explanation of Net Structure Diagrams

The net structure routing diagrams provide a reference design example for each raw card version. These designs provide an initial basis for registered DIMM designs. The diagrams should be used to determine individual signal wiring on a DIMM for any supported configuration. Only transmission lines (represented as cylinders and labeled with trace length designators “TL”) represent physical trace segments. All other lines are zero in length. To verify DIMM functionality, a full simulation of all signal integrity and timing is required. **The given net structures and trace lengths are not inclusive for all solutions.**

Once the net structure has been determined, the permitted trace lengths for the net structure can be read from the table below each net structure routing diagram. Some configurations require the use of multiple net structure routing diagrams to account for varying load quantities on the same signal. All diagrams define one load as one SDRAM input. **It is highly recommended that the net structure routing data in this document be simulated by the user.**

Net Structure Example

A 4 GB double-sided x72 DIMM using 1 Gbit, 128Mx8 SDRAM devices would have a data net structures as shown in the following diagrams.



Proposed

Timing Budgets

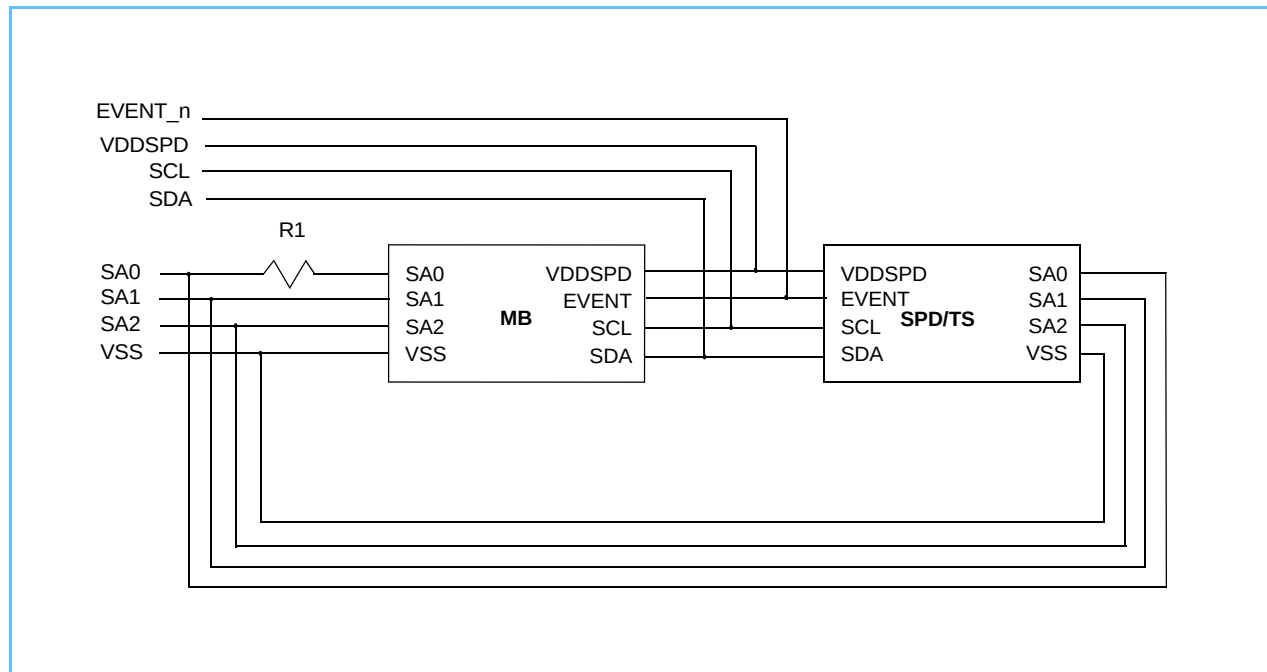
This section will be added following further definition of the Memory Buffer Specifications

Proposed

Wiring for SMBus

Schematic of SPD/Thermal Sensor and MB

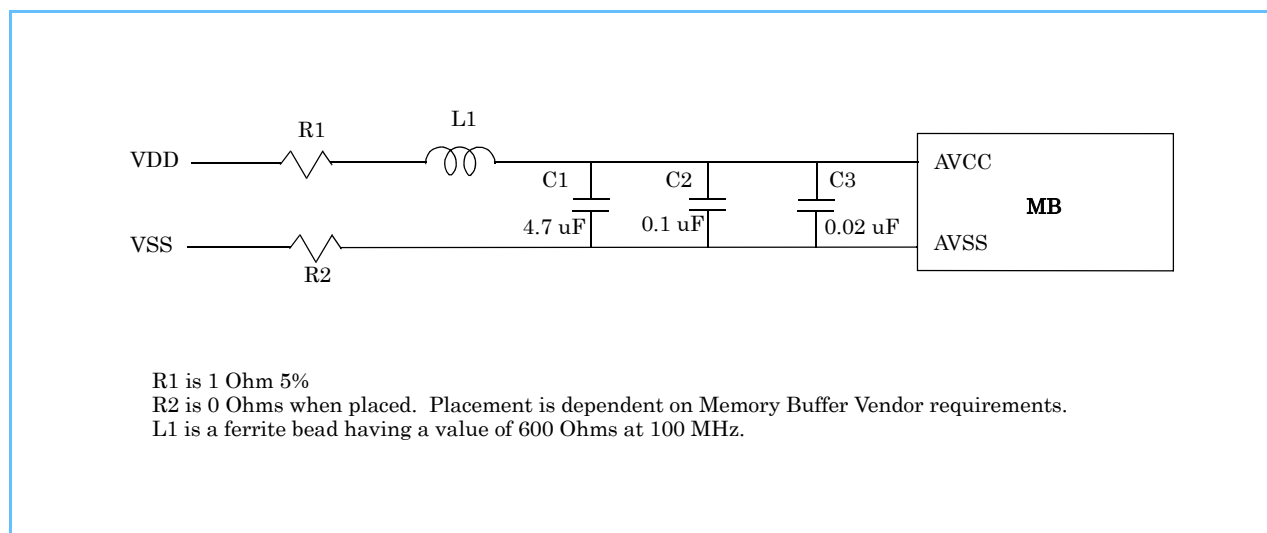
The following schematic illustrates the required wiring of the SPD/TS and MB



This specific wiring is required. The value of R1 is typically 1K, 5% but this is a guideline. The SA0 pin may have 12 Volts applied to it for programming the SPD. Under these conditions the current into the MB must be limited. R1 serves the purpose of limiting the current into the MB.

Proposed

The following schematic defines the required wiring for AVCC.



DIMM Wiring Requirements

These are requirements for compatibility. If deviations are required they must be identified and explained in the appropriate appendix.

All SDRAM components must have separate ZQ resistors for each pin on the SDRAM component.

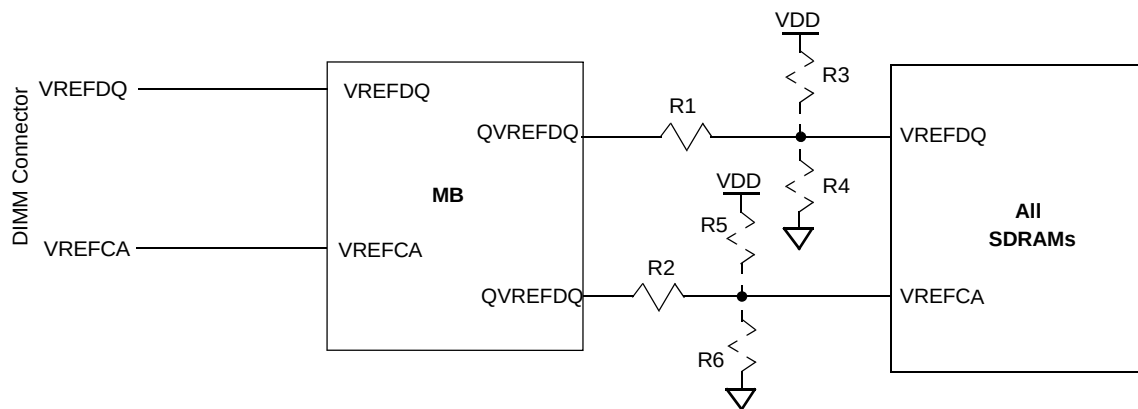
The ECC byte lane as defined by the edge connector must connect to MB pins identified as DQ63 to DQ71. For the ECC byte lane there must be a one to one match in the pin ordering between the connector and the MB, CB0 to DQ63, etc. The associated strobes must also be connected one to one.

For all other byte lanes, the strobes must match the routing as defined in the table. The bits must be kept with the associated strobes. For non-ECC byte lanes and modules with x8 SDRAM components swapping bits within the byte is allowed. For non-ECC byte lanes and modules with x4 SDRAM components swapping bits within the nibble is allowed. For non-ECC byte lanes and modules with x4 SDRAM components swapping bits between nibbles is not allowed.

Gold Finger to Memory Buffer Mapping Table

DIMM Gold Finger Connector Pin Name	Horizontal MB MB Pin Name	Vertical MB MB Pin Name	DIMM Gold Finger Connector Pin Name	Horizontal MB MB Pin Name	Vertical MB MB Pin Name
DQS0	DQS0	DQS5	DQS9	DQS9	DQS14
DQS1	DQS1	DQS2	DQS10	DQS10	DQS11
DQS2	DQS2	DQS3	DQS11	DQS11	DQS12
DQS3	DQS3	DQS4	DQS12	DQS12	DQS13
DQS4	DQS4	DQS7	DQS13	DQS13	DQS16
DQS5	DQS5	DQS1	DQS14	DQS14	DQS10
DQS6	DQS6	DQS0	DQS15	DQS15	DQS9
DQS7	DQS7	DQS6	DQS16	DQS16	DQS15
DQS8	DQS8	DQS8	DQS17	DQS17	DQS17

Proposed



As illustrated in the figure VREFCA from the edge connector must be wired to VREFCA of the MB. VREFDQ from the edge connector must be wired to VREFDQ of the MB. VREFCA and VREFDQ for the SDRAMs components must be wired to resistor dividers as illustrated with R3/R4 and R5/R6. The values of R3, R4, R5

and R6 are TBD. These are not placed on the JEDEC standard DIMM. QVREFDQ and QVREFCA from the MB must be wired to the SDRAMs through series resistors as illustrated with R1 and R2. These resistors are zero Ohms and will be placed on JEDEC standard DIMMs.

Pin 77 of the edge connector is defined as ODT1 or CKE3. It will be wired to the MB through a TBD Ohm resistor.

Pin 167 of the edge connector is defined as CKE2. For the JEDEC standard LRDIMM it is not used. It will be wired to the MB through a TBD Ohm resistor.

All LRDIMMs will provide some feature to reduce capacitance at the edge connector for the DQ bus. The details of how this is done will be defined by each raw card and included in the appendix.

Proposed

Serial Presence Detect Definition

Removed for now. Will request the JEDEC office add once the SPD spec is complete.

Proposed

DDR3 DIMM Label Format

This material is provided as reference only.

DDR3 "End-User" DIMM Label Format:

The following label shall be applied to all DDR3 memory modules targeted at end-user type products to fully describe the key attributes of the module. The label can be in the form of a stick-on label, silk screened onto the assembly, or marked using an alternate customer-readable format. A readable point size should be used, and the number can be printed in one or more rows on the label. Hyphens may be dropped when lines are split, or when font changes sufficiently separate fields. Unused letters in each field, such as ggggg, are to be omitted when not needed.

Voltage options in field 'v' describe the nominal voltage VDD of the SDRAMs and support components (excluding the SPD). Values for these voltages are 'operable' which means the device characteristics such as timing are supported at this voltage, or 'endurant' which means that the device may be powered to that voltage level without damage, however should not be used as operation is not guaranteed at the higher voltage.

ggggg eRxff PC3v-wwwwwm-aa-bb-ccd

Where:

- ggggg = Module total capacity, in bytes
256MB, 512MB, 1GB, 2GB, 4GB, etc.
- eR = Number of ranks of memory installed
1R = 1 rank of DDR3 SDRAM installed
2R = 2 ranks
4R = 4 ranks
- xff = Device organization (bit width) of DDR3 SDRAMs used on this assembly
x4 = x4 organization (4 DQ lines per SDRAM)
x8 = x8 organization
x16 = x16 organization
- v = SDRAM and support component supply voltage (VDD)
Blank = 1.5 V operable
L = 1.35 V operable, 1.5 V operable
U = 1.TBD V operable, 1.TBD V endurant
- wwwww = Module bandwidth in MB/s
6400 = 6.40 GB/s (DDR3-800 SDRAMs, 8 byte primary data bus)
8500 = 8.53 GB/s (DDR3-1066 SDRAMs, 8 byte primary data bus)
10600 = 10.66 GB/s (DDR3-1333 SDRAMs, 8 byte primary data bus)
12800 = 12.80 GB/s (DDR3-1600 SDRAMs, 8 byte primary data bus)
14900 = 14.93 GB/s (DDR3-1866 SDRAMs, 8 byte primary data bus)
17000 = 17.06 GB/s (DDR3-2133 SDRAMs, 8 byte primary data bus)
- m = Module Type
E = Unbuffered DIMM ("UDIMM"), with ECC (x72 bit module data bus)
F = Fully Buffered DIMM ("FB-DIMM")
L = Load Reduction DIMM ("LRDIMM")
M = Micro-DIMM
N = Mini-RDIMM
R = Registered DIMM ("RDIMM")
S = Small Outline DIMM ("SO-DIMM")
U = Unbuffered DIMM ("UDIMM"), no ECC (x64 bit module data bus)
- aa = DDR3 SDRAM CAS Latency in clocks at maximum operating frequency

Proposed

bb = JEDEC SPD Revision Encoding and Additions level used on this DIMM
cc = Reference design file used for this design (if applicable)
 A = Reference design for raw card 'A' is used for this assembly
 B = Reference design for raw card 'B' is used for this assembly
 AC = Reference design for raw card 'AC' is used for this assembly
 ZZ = None of the reference designs were used for this assembly
d = Revision number of the reference design used
 0 = Initial release
 1 = First revision
 2 = Second revision
 P = Pre-release or Engineering sample
 Z = To be used when field cc = ZZ

Examples:

2GB 2Rx4 PC3-10600R-7-10-D2

is a 2 GB DDR3 RDIMM using 2 ranks of x4 SDRAMs operational to DDR3-1333 performance with CAS Latency = 7 using JEDEC DDR3 SPD revision 1.0, raw card reference design file D revision 2 used for the assembly

1GB 1Rx4 PC3L-10600R-8-10-C1

is a 1 GB DDR3 RDIMM using 1 rank of x4 low voltage SDRAMs, operable at 1.35 V and 1.5 V operable, operational to DDR3-1333 performance with CAS Latency = 8 using JEDEC DDR3 SPD revision 1.0, raw card reference design file C revision 1 used for the assembly

1GB 2Rx8 PC3-12800E-10-10-BP

is a 2 GB DDR3 UDIMM with x72 data bus (ECC) using 2 ranks of x8 SDRAMs operational to DDR3-1600 performance with CAS Latency = 10 using JEDEC DDR3 SPD revision 1.0, raw card reference design file B pre-release revision used for the assembly

4GB 2Rx8 PC3-8500N-8-10-ZZZ

is a 4 GB DDR3 Mini-RDIMM using 2 ranks of x8 SDRAMs operational to DDR3-1066 performance with CAS Latency = 8 using JEDEC DDR3 SPD revision 1.0, no JEDEC standard raw card reference design file used for the assembly

Proposed

DIMM Mechanical Specifications

JEDEC has standardized detailed mechanical information for the 240Pin DIMM family. This material is included as reference and may be out of date. Download the latest version of MO-269 for any later updates. This information can be accessed on the worldwide web as follows:

1. Go to JEDEC official site; <http://www.jedec.org>.
2. Click on 'Free Standards' and enter the free download area.
3. Search by document number: 'MO-269' and download the PDF for this product family.
4. Or search by 'JEP95'; 'JEDEC Publication 95.' and open entire document, scroll down and select 'MO-269' to download the PDF for this product family.

Within MO-269, several DIMM thickness variations are defined. These variations are summarized in the table below, in conjunction with examples of the types of LRDIMM components and assemblies that may be associated with each DIMM thickness range:

Maximum LRDIMM Thickness	Comments
Less than or equal to 4.00 mm	Generally associated with DIMMs produced with devices that are 1.35 mm thick or less
> 4.00 mm and less than or equal to 6.75 mm	Generally associated with DIMMs produced with devices that are greater than 1.35 mm and less than or equal to 2.70 mm thick
> 6.75 mm and less than or equal to 7.55 mm	Generally associated with DIMMs produced with devices that are greater than 2.70 mm and less than or equal to 3.10 mm thick
> 7.55 mm	Intended to cover DIMMs produced with non-standard package thicknesses, card-on-card structures or alternate solutions

Proposed

Note: Maximum DIMM thickness can be a measured maximum value, or can be calculated using the maximum component, card, label, and assembly process adders.

Design File Naming Convention

“DIMM spec”_Vrrr_RC_LLn_YYYYMMDD.zip

Where:

DIMM spec = DIMM Specification
PC3-LRDIMM

V = Constant representing “Version”.

rrr = First revision of raw card Appendix at time of first ballot

RC = Constant representing “Raw Card”

LL = Raw Card letter(s)

n = Raw card registration number. Only to be incremented if the file is actually posted.

YYYYMMDD = Year, month and day of release if posted or last changes if under consideration.

Notes regarding release date:

1. Date will always reflect the date of the last change. Renaming of a file does not constitute a change.
2. If for example the BOM is updated, the BOM, readme and design (zip) files all receive new dates, but the brd file remains unchanged.

Notes regarding speed upgrades:

1. If for example a new BOM is needed to upgrade a design file that accomodates a new speed such as PC3-12800 then the BOM file may be named as follows:
“DIMMspec”_Vrrr_RC_LLn_YYYYMMDD_ **BOM-12800**.xls
2. BOMs may be changed or added to an existing design (zip) file without incrementing the raw card registration number. However, in this case the date designation of the design file would be incremented as shown in the following examples:

Example Filename: PC3-LRDIMM_V100_RC_B0_20080912.zip

Proposed

Revision Log

[illegible]

Proposed

Revision Info	Page of Revision	Description of Change

Proposed

Exhibit F

Tally of Votes



Committee Letter Ballot

JC-45.4-09-321

2192.44



Tally Date: Wed, December 09, 2009 at 16:40:13

(US Eastern Time)

Ballot distributed: 16 Nov 2009

Expiration date: 07 Dec 2009

Sponsor: Avant Technology L.P. Mr. Paul Goodwin Email: paul_goodwin@avanttechnology.com Phone: 512-719-6303

Subject: DDR3 LRDIMM Design Specification Body

Attachment: [HB09321-.pdf](#)

PATENTS: No known patent issues on the sponsor's part

Summary:

17 Yes

5 Abstention

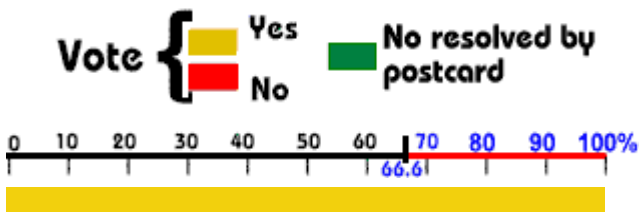
22 companies voted (including abstention)

Non voting companies are not tallied,
and are not considered to abstain.

Attention: Percentages are rounded.

Abstentions are excluded from percentage calculation.

Only Yes votes (ballot may pass by acclamation)



Company / voter	Y*	N*	A*	P*	C*	PC*	DoV*	DoR*
22 companies voted	17	0	5	1	6Y		22	
Advanced Micro Devices Inc. Patel	<u>Y</u>				<u>X</u>	N/A	12/03/09	
Buffalo Inc. Tsukada	Y						11/17/09	
Cray Inc. Grossmeier	Y						11/16/09	
Elpida Memory Incorporated Ono	<u>Y</u>				<u>X</u>	N/A	11/26/09	
FormFactor Inc. Gervasi	<u>Y</u>				<u>X</u>	N/A	12/02/09	
Hynix Semiconductor □im	Y						12/02/09	
I-O Data Device Inc. Miyagoshi			A				12/01/09	
IBM Corporation □ilmer	Y						11/25/09	
Inphi Corporation Washkewicz	<u>Y</u>				<u>X</u>	N/A	12/02/09	
Inphi Corporation Raghavan	Y						12/02/09	

Integrated Device Technology Inc. Franklin	Y						12/02/09	
Intel Corporation Mrdjan	Y						11/30/09	
Kingston Technology Company Inc. Cheng	Y						11/23/09	
Legacy Electronics Inc. Mecker			A				12/01/09	
Micron Technology Inc. Graham	Y						11/30/09	
Nanya Technology Corporation Linder	Y				X	N/A	12/02/09	
Netlist Inc. Martinez			A	P			12/01/09	
Nvidia Corporation Wagner			A				12/01/09	
PNY Technologies Inc. Socci	Y						12/02/09	
Samsung Semiconductor Park	Y				X	N/A	12/02/09	
Sun Microsystems Inc. Jeffrey	Y						12/01/09	
Tyco Electronics Corporation Leidy			A				11/19/09	
* Y ☐ Yes, N ☐ No, A ☐ Abstain, P ☐ Patent(s), C ☐ Comments PC: Postcard, Y ☐ approved response, N ☐ did not approve response, N/A: not available, sponsor and / or voter did not respond, DoV: Date of Vote								

Advanced Micro Devices Inc. represented by Sam Patel, [email: sam.patel@amd.com](mailto:sam.patel@amd.com) voted "**Approve content with comments**" on 12/03/09

Comments: Would like to see CS, C_E and ODT routing for all configuration documented in this body of the lrdimm spec.

[Respond to original comments](#) Sponsor, please submit your response to voter.

[\[Top\]](#) [\[Summary table\]](#)

Elpida Memory Incorporated represented by Takao Ono, [email: t.ono.gz@elpida.com](mailto:t.ono.gz@elpida.com) voted "**Approve content with comments**" on 11/26/09

Comments: page 26-27, How should the QAECC2,6,9 be treated ☐ Changing to NC or RFU ☐
 page 35 AVCC should be changed to AVDD,
 page 36 one of QVREFDQ should be changed to QVREFCA

[Respond to original comments](#) Sponsor, please submit your response to voter.

[\[Top\]](#) [\[Summary table\]](#)

FormFactor Inc. represented by Bill Gervasi, [email: bilge@discobolusdesigns.com](mailto:bilge@discobolusdesigns.com) voted "**Approve content with comments**" on 12/02/09

Comments: pg 1: andd should be and

pg 1: configureable should be configurable

[Respond to original comments](#) Sponsor, please submit your response to voter.

[\[Top\]](#) [\[Summary table\]](#)

Inphi Corporation represented by Paul Washkewicz, email: pwashkewicz@inphi-corp.com voted "**Approve content with comments**" on 12/02/09

Comments: Inphi approves material in red text.

[Respond to original comments](#) Sponsor, please submit your response to voter.

[\[Top\]](#) [\[Summary table\]](#)

Nanya Technology Corporation represented by Peter Linder, email: jedec@tx.nanya.com voted "**Approve content with comments**" on 12/02/09

Comments: Suggest to change Raw-Card-C to 11x12mm dram pkg to match the other raw cards as discussed in TG

[Respond to original comments](#) Sponsor, please submit your response to voter.

[\[Top\]](#) [\[Summary table\]](#)

Netlist Inc. represented by Mario Martinez, email: mmartinez@netlist.com voted "**Abstain from voting**" on 12/01/09

Comments:

[Respond to original comments](#) Sponsor, please submit your response to voter.

PATENT ISSUE:
Netlist may have IP that applies to this ballot

[\[Top\]](#) [\[Summary table\]](#)

Samsung Semiconductor represented by Sung Joo Park, email: sjoo@sec.samsung.com voted "**Approve content with comments**" on 12/02/09

Comments: Table of contents should be updated. And Max DRAM size of the Raw Card C (on page13) is 11.0 x 12.0.

[Respond to original comments](#) Sponsor, please submit your response to voter.

[\[Top\]](#) [\[Summary table\]](#)

End of Web Report

EXTRA OPTIONS:



Text file ready to import
in a spreadsheet



email tally to voting committee



Add vote, on your honor

PLEASE BE VERY PATIENT. Processing any of above query takes well over one minute.



Return to the main voting page