

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC. and SK HYNIX AMERICA INC.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2020-01042
Patent 10,474,595 B2

Before BRYAN F. MOORE, JON M. JURGOVAN, and
KARA L. SZPONDOWSKI, *Administrative Patent Judges*.

JURGOVAN, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314, 37 C.F.R. § 42.4

I. INTRODUCTION

A. *Background and Summary*

Petitioner, SK hynix Inc. and SK hynix America Inc., filed a Petition requesting *inter partes* review of claims 1–24 of U.S. Patent No. 10,474,595 B2 (Ex. 1001, the “’595 Patent”). Paper 1 (“Petition” or “Pet.”). The Petition was accorded a filed date of June 9, 2020. Paper 3. Patent Owner, Netlist, Inc., filed a Preliminary Response (“Prelim. Resp.”) on September 18, 2020. Paper 6. By Order dated October 1, 2020, we authorized the parties to brief discretionary denial and priority date issues. Petitioner filed a Reply (Paper 8) on October 8, 2020, and Patent Owner filed a Sur-Reply (Paper 9) on October 15, 2020, to address these issues.

Under 35 U.S.C. § 314(a), an *inter partes* review may not be instituted unless the information presented in a petition “shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” Upon consideration of the Petition and accompanying exhibits and evidence, we determine Petitioner has established a reasonable likelihood that it would prevail with respect to at least one challenged claim in the *inter partes* review. Therefore, we grant institution of an *inter partes* review as to all of the challenged claims of the ’595 Patent.

B. *Real Parties in Interest*

Petitioner identifies the real parties in interest as SK hynix Inc. and SK hynix America Inc. Pet. 2.

Patent Owner identifies the real party in interest as Netlist, Inc. Patent Owner’s Mandatory Notice, Paper 4, 1.

C. Related Matters

Patent Owner has asserted the '595 Patent in the following case:

Case Name	Case Number	Court
Netlist, Inc. v. SK Hynix Inc. et al. (hereafter “parallel district court litigation”)	Case No. 6:20-CV-00194	Western District of Texas

Patent Owner’s Mandatory Notices, Paper 4, 1, Pet. 2.

The '595 Patent is related to the following cases:

Case Name	Case Number	Court
Netlist, Inc. v. SK hynix Inc., et al.	Case No. 8:17-CV-01030	Central District of California
Netlist, Inc. v. SK hynix Inc., et al.	Case No. 8:16-cv-01605 (C.D. Ca.)	Central District of California
SK hynix Inc. and SK hynix America, Inc. v. Netlist, Inc.	IPR2020-01044	Patent Trial and Appeal Board
SK hynix Inc. and SK hynix America, Inc. v. Netlist, Inc.	IPR2018-00303	Patent Trial and Appeal Board
SK hynix Inc. and SK hynix America, Inc. v. Netlist, Inc.	IPR2017-00548	Patent Trial and Appeal Board
In the Matter of Certain Memory Modules and Components Thereof	Inv. No. 337-TA-1089	International Trade Commission
In the Matter of Certain Memory Modules and Components Thereof, and Products Containing Same	Inv. No. 337-TA-1023	International Trade Commission

Patent Owner’s Mandatory Notice, 1–2; Pet. 2–3.

D. The '595 Patent

The '595 Patent describes a memory module coupled to a memory controller of a host computer system. Ex. 1001, code (57). The memory module operates in two modes, one to perform normal read/write operations, and the other to receive and execute training or initialization sequences to prepare the memory module for normal read/write operation. *Id.* The memory module has an open-drain output pin which it uses to indicate a parity error in the first mode for normal read/write operations. *Id.* In the second mode of operation, however, the memory module uses the same output pin to notify the memory controller of the status of its execution of the training sequence, i.e., whether execution of the training sequence is in progress or has been completed. *Id.*, 6:57–63.

Figure 2 of the '595 Patent, below, illustrates an embodiment with multiple memory modules performing handshaking with a memory controller. *Id.* at 2:37–41.

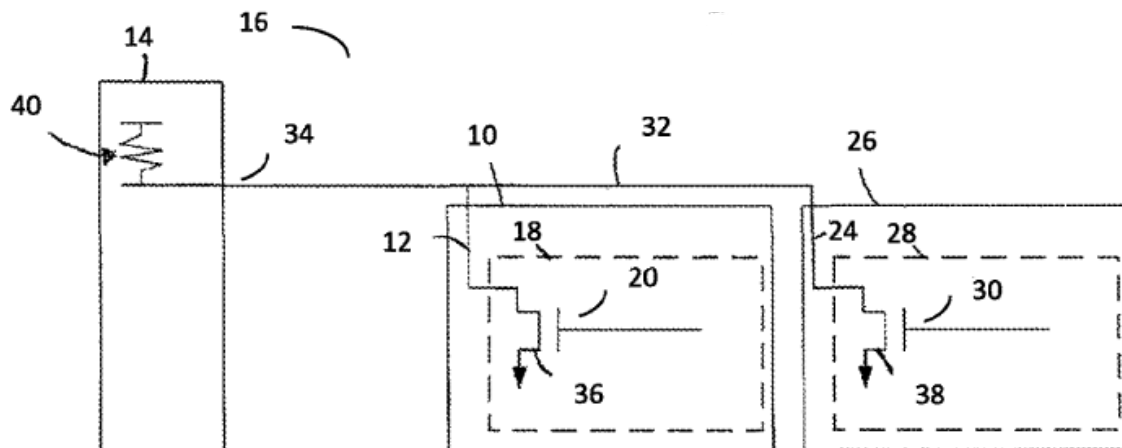


Figure 2

Specifically, Figure 2 shows host computing system 16 including memory controller 14 connected to first and second memory modules 10, 26. *Id.* at 4:24–29, 9:13–19, 47–48. The memory modules 10, 26 include respective controller circuits 18, 28 with notification circuits 20, 30. *Id.* at 9:14–23, 10:30–37. Notification circuits 20, 30 have corresponding transistors 36, 38 with open-drain configurations. *Id.* at 9:49–52. As memory modules 10, 26 carry out their training or initialization sequences, memory modules 10, 26 drive the gates of the transistors 36, 38 high, which pulls their outputs 12, 24 low, signaling to the memory controller 14 via input 34 that the initialization sequences have not been completed. *Id.* at 10:30–50. As each memory module 10, 26 completes its initialization sequence, the module drives the gate of its respective transistor 36 or 38 low, causing its output 12 or 24 to enter a high-impedance state. *Id.* When all modules' transistor outputs are in high-impedance states, input 34 draws high, notifying the system memory controller 14 that the all memory modules have completed their initialization sequences and are ready for normal read/write operation. *Id.*

The memory module may comprise a printed-circuit board (PCB) with dynamic random-access memory (DRAM) elements and a module controller. *Id.* at 4:33–34, 4:43–44. The PCB may have edge connections for data, address and control, and error signals (including parity and notification signals). *Id.* at 5:10–17, 8:26–33. The module controller may be an integrated circuit mounted on the PCB. *Id.* at 4:43–44, 13:45–49. A multiplexor may be connected to the transistor gate to provide either a parity signal or “signal related to the training sequence” (the notification signal). *Id.* at 11:15–23.

E. Challenged Claims

Claims 1, 10, 17, and 21 of the '595 Patent are independent. Claims 2–9 depend, directly or indirectly, from claim 1. Claims 11–16 depend from claim 10. Claims 18–20 depend from claim 17. Claims 22–24 depend from claim 21. Claim 1 is set forth below with annotated numbering of elements:

1. [1.a] A memory module operable with a memory controller of a host system, comprising:

[1.b] a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;

[1.c] dynamic random access memory elements on the printed circuit board;

[1.d] a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection; and

[1.e.i] wherein the memory module is configurable to operate in any of at least a first mode and a second mode;

[1.e.ii] wherein the memory module in the first mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections,

[1.e.iii] wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations, and

[1.e.iv] wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences;

[1.f.i] wherein the module controller is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations,

[1.f.ii] wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and

[1.f.iii] wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the first mode;

[1.g] wherein the module controller in the second mode is further configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection to a first state or to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.

Ex. 1001, 14:39–15:21.

F. Evidence

Petitioner relies upon the following prior art references¹:

¹ Because the claims at issue have an effective filing date prior to the effective date of the AIA's amendments to 35 U.S.C. § 112 (September 16, 2012) and 35 U.S.C. §§ 102 and 103 (March 16, 2013), we apply the pre-AIA versions of §§ 102, 103, and 112 in this Decision (pre-Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) ("AIA")). Petitioner alleges that Hazelzet is prior art under § 102(a), (b) and (e). Pet. 26. Petitioner alleges JEDEC is prior art under 35 U.S.C. § 102(a). Pet. 28. Petitioner alleges Buchmann is prior art under 35 U.S.C. § 102(e). Pet. 30. Petitioner assumes Kim is prior art, but does not identify the statutory basis for its assertion. *See* Pet. 4. Kim has a filing date of January 22, 2008, however, which is before the '595 Patent's priority date of June 12, 2009. Kim thus appears to be prior art under 35 U.S.C. § 102(e). Patent Owner does not dispute that Kim is prior art at this time.

IPR2020-01042

Patent 10,474,595 B2

Hazelzet	US 2008/0098277 A1	April 24, 2008	Ex. 1014
JEDEC	Committee Letter Ballot, Committee: JC-40.4, Committee Item Number: 142.35	Nov. 11, 2009 ²	Ex. 1015
Buchmann	US 8,139,430 B2	Mar. 20, 2012	Ex. 1016
Kim	US 8,359,521 B2	Jan. 22, 2013	Ex. 1017

Petitioner also supports its challenges with a declaration from Dr. Donald Alpert. Ex. 1003. Patent Owner does not rely on any testimony from its own expert at this time. *See generally* Prelim. Resp.

G. The Asserted Challenges

Petitioner asserts the following ground of unpatentability:

Ground #	Challenged Claims	35 U.S.C. §	References/Basis
1	1–24	103	Hazelzet, JEDEC
2	1–24	103	Hazelzet, Buchmann
3	3–7, 12–14, 20, 22, 23	103	Hazelzet, JEDEC or Buchmann, Kim

Pet. 4.

² Petitioner contends the '595 Patent is not entitled to the priority date of its provisional application under 35 U.S.C. § 119(e) because certain claimed elements were not disclosed in the provisional application. Pet. 1. Accordingly, Petitioner contends JEDEC is prior art to the '595 Patent. *Id.* Patent Owner disagrees, contending that the '595 Patent is entitled to the filing date of its provisional application as its priority date. We address this dispute in Section II.C.

II. PRELIMINARY MATTERS

A. Analysis of Discretionary Institution Under 35 U.S.C. § 314(a)

Patent Owner contends that the Board should deny institution under 35 U.S.C. § 314(a) because of the parallel district court litigation. Prelim. Resp. 1–12.

Under § 314(a), the Director has discretion to deny institution of an *inter partes* review. See 37 C.F.R. § 42.4(a) (“The Board institutes the trial on behalf of the Director.”); see also *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1367 (Fed. Cir. 2016) (“[T]he [Office] is permitted, but never compelled, to institute an [inter partes review] proceeding.”). In exercising that discretion, the Board may consider the state of a parallel district court proceeding, among other considerations, as a “factor that weighs in favor of denying the Petition under § 314(a).” *NHK Spring Co. v. Intri-Plex Techs., Inc.*, IPR2018-00752, Paper 8 at 20 (PTAB Sept. 12, 2018) (precedential) (“NHK”); *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 5–6 (PTAB Mar. 20, 2020) (precedential) (hereafter “*Fintiv*”). When considering the impact of parallel litigation, the Board seeks, among other things, to minimize the duplication of work to resolve the same issue. See *NHK*, Paper 8 at 19–20.

The Board has identified a nonexclusive list of factors “relat[ing] to whether efficiency, fairness, and the merits” favor discretionary denial in view of parallel district court litigation. *Fintiv*, Paper 11 at 6. The factors include: (1) whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted; (2) proximity of the court’s trial date to the Board’s projected statutory deadline for a final written decision; (3) investment in the parallel proceeding by the court and the parties;

(4) overlap between issues raised in the petition and in the parallel proceeding; (5) whether the petitioner and the defendant in the parallel proceeding are the same party; and (6) other circumstances that impact the Board's exercise of discretion, including the merits. *Id.* at 5–6. In evaluating the factors, we take “a holistic view of whether efficiency and integrity of the [patent] system are best served by denying or instituting review.” *Id.* at 6.

1. *Procedural Background*

On March 17, 2020, Patent Owner filed a complaint against Petitioner in the Western District of Texas. Pet. 15. Petitioner filed the present Petition on June 8, 2020. *Id.* at 71. On July 8, 2020, the District Court issued a scheduling order that set, among other things, a deadline for Petitioner to serve preliminary invalidity contentions by August 7, 2020 and a *Markman* Hearing for December 8, 2020. Ex. 2001, 2. This scheduling order stated that the District Court expected to set the trial date at the conclusion of the *Markman* Hearing, but also set a trial date of October 26, 2021. *Id.* at 3; *see also* Reply 1–2. On November 4, 2020, the District Court issued an updated scheduling order resetting the *Markman* hearing for March 19, 2021, and likewise stating that the District Court expected to set the trial date at the conclusion of the *Markman* Hearing, but also resetting the trial date to December 2021. Ex. 1073 at 3, 5; Ex. 2023 at 3, 5. On November 18, 2020, the District Court issued another updated scheduling order resetting certain deadlines, including setting the *Markman* hearing for March 19, 2021, and setting the trial date to December 6, 2021. Ex. 2023 at 3, 5.

In its Reply, Petitioner “hereby stipulate[s] that, if this IPR is instituted, they will not assert in the Texas case any ground that they would have been estopped from asserting by operation of 35 U.S.C. § 315(e)(2) had a [final written decision] in this IPR previously issued.” Reply 5–6 (hereafter “Stipulation”).

2. *Analysis*

a) *Factor 1: Whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted*

Patent Owner argues that this factor favors denying institution because the District Court has not entered a stay or given any indication that it would enter a stay if the *inter partes* review (IPR) is instituted. Prelim. Resp. 6. Patent Owner further argues that Petitioner has not moved for a stay, and has stipulated to the joint schedule and trial date. *Id.* In addition, Patent Owner argues that the District Court does not typically stay trials in these circumstances, even if an IPR was instituted. *Id.* at 6–7; *see also* Sur-Reply 1.

Petitioner asserts that it has filed a motion to transfer the parallel district court litigation to the Central District of California. Reply 2–3. According to Petitioner, if that happens, the case is likely to be stayed if IPR is instituted. *Id.*

Currently there is no stay in place. We decline to attempt to predict how the District Court would proceed should a stay be requested by either of the parties, or to attempt to predict how the District Court will decide the motion to transfer and the effects of that decision. Accordingly, in these circumstances we will not speculate as to the likelihood of a stay. Therefore,

we do not find that this factor weighs for or against exercising our discretion to deny institution.

b) Factor 2: proximity of the court's trial date to the Board's projected statutory deadline for a final written decision

As discussed above, after the parties filed their briefs in this *inter partes* review, the District Court re-scheduled the trial for December 6, 2021. Ex. 1073 at 3, 5; Ex. 2023 at 3, 5. The final written decision in this case will issue by December 18, 2021, which is approximately the same time as the currently scheduled trial date. Where, as here, the trial date and the date of our final written decision are at or around the same time, the efficiency and fairness concerns that underlie the *Fintiv* analysis are not as strong, and will instead implicate other factors, as will be discussed further below. *See Fintiv*, Paper 11 at 9 (noting that when the court's trial date is at or around the same time as the projected statutory deadline, "the decision whether to institute will likely implicate other factors," such as "the resources that have been invested in the parallel proceeding"). We take the District Court's trial schedule at face value, and decline to speculate as to whether that date will be changed. Accordingly, we find factor two weighs, at most, marginally against exercising our discretion to deny institution.

c) Factor 3: investment in the parallel proceeding by the court and the parties

Patent Owner argues that the parties and District Court will have already invested considerable resources in advancing the parallel district court litigation by the time any institution decision issues. Prelim. Resp. 9. Specifically, Patent Owner argues that: (1) the parties have already exchanged their initial infringement and invalidity contentions; (2) the

District Court will have held the *Markman* hearing and issued its claim construction order by the time of the institution decision; and (3) the parties will be in the midst of fact discovery. *Id.* Patent Owner also argues that the parties and the District Court will have “expended the time, money, and resources necessary to completely litigate and conduct a jury trial” by the time any final written decision would issue. *Id.* at 10.

Petitioner contends that it filed the Petition “as early as reasonably possible.” Reply 4–5. Petitioner also argues that by the time of institution, although claim construction briefing will be complete and the District Court may have issued constructions from the bench, the District Court’s resource investment will be “relatively minor,” and “fact discovery will have only just begun three days prior, and expert discovery will be months in the future.” *Id.* at 5.

We agree with Petitioner (Reply 5) that Factor 3 generally focuses on the investment by the District Court and the parties *at the time of the institution decision*. See *Fintiv*, Paper 11 at 9 (“The Board also has considered the amount and type of work already completed in the parallel litigation by the court and the parties *at the time of the institution decision*.”) (emphasis added)); see also *Sand Revolution II, LLC v. Continental Intermodal Grp.–Trucking LLC*, IPR2019-01393, Paper 24 at 10–11 (PTAB June 16, 2020) (informative) (analyzing the district court’s investment of time and resources prior to the institution decision).

According to the updated scheduling order in the parallel district court litigation, the *Markman* hearing is set for March 19, 2021, fact discovery opens on October 16, 2020, and closes on July 23, 2021, final infringement and invalidity contentions are due on April 16, 2021, opening expert reports

are due on July 30, 2021, and expert discovery closes on September 24, 2021, and the dispositive motion deadline is October 1, 2021. Ex. 1073 at 2–5; Ex. 2023 at 2–5. There is no evidence in the record that the District Court has substantively considered any of the invalidity arguments set forth in the Petition. Further, as noted above, the *Markman* Hearing has been rescheduled, expert discovery has not yet begun, expert reports have not been exchanged, and dispositive motions have not yet been filed. *See* Ex. 1073 at 2–5; Ex. 2023 at 2–5. Therefore, further effort remains in the case as it relates to invalidity.

The timing of filing the petition is also relevant to the analysis. *See Fintiv*, Paper 11 at 11–12. If the petitioner, “faced with the prospect of a looming trial date, waits until the district court trial has progressed significantly before filing a petition,” that decision “may impose unfair costs to a patent owner.” *Id.* at 11. On the other hand, “[i]f the evidence shows that the petitioner filed the petition expeditiously, such as promptly after becoming aware of the claims being asserted, this fact has weighed against exercising the authority to deny institution.” *Id.* Here, the Petition was filed less than three months after the Complaint was filed in the parallel district court litigation, and even before Patent Owner had served its infringement contentions. *See* Reply 4.

Weighing the facts in this particular case, including the time invested in the parallel district court litigation by the parties and the District Court, the schedule in that case, and the timing of the filing of the Petition, we find that this factor weighs against exercising our discretion to deny institution.

d) Factor 4: overlap between issues raised in the petition and in the parallel proceeding

This factor evaluates “concerns of inefficiency and the possibility of conflicting decisions” when substantially identical prior art arguments are submitted in both the district court and the *inter partes* review proceedings. *Fintiv*, Paper 11 at 12. In particular, “if the petition includes the same or substantially the same claims, grounds, arguments, and evidence as presented in the parallel proceeding, this fact has favored denial.” *Id.* (citing *Next Caller Inc. v. TRUSTID, Inc.*, IPR2019-00961, Paper 8 at 11–12 (PTAB Oct. 16, 2019) (same grounds asserted in both cases); *ZTE (USA) Inc. v. Fractus, S.A.*, IPR2018-01451, Paper 12 at 20 (PTAB Feb. 19, 2019) (same prior art and identical evidence and arguments in both cases)).

Patent Owner argues that Petitioner is “asserting the same exact prior art references” in the parallel district court litigation as in the Petition. Prelim. Resp. 10–11 (citing Ex. 2009, 2011–2014).

Petitioner stipulates “that, if IPR is instituted, they will not assert in the Texas case any ground that they would have been estopped from asserting by operation of 35 U.S.C. § 315(e)(2) had a FWD in this IPR previously issued.” Reply 5–6. Petitioner argues that based on its Stipulation, “there is no overlap between the issues to be tried in the Texas case and those raised in this IPR, if instituted.” *Id.*

Patent Owner replies that Petitioner’s Stipulation “does not change the fact that the same parties will be litigating the validity of the same patent claims simultaneously in two different forums.” Sur–Reply 2 (emphasis omitted). Patent Owner argues that Petitioner “attempt[s] to game the *Fintiv* analysis by electing to pursue different theories in each forum.” *Id.*

Petitioner's Stipulation minimizes concerns of duplicative efforts between the District Court and the Board, as well as potentially conflicting decisions. *See Sand Revolution*, Paper 24 at 11–12 (a stipulation not to pursue overlapping patentability arguments in district court may mitigate concerns of potential overlap between arguments in parallel proceedings). Petitioner's Stipulation is similar to that noted in *Sand Revolution* to address concerns regarding duplicative efforts. *See Sand Revolution*, Paper 24, 12 at n.5; *see also* Reply 6 (stating that such a Stipulation is “broader” than that in *Sand Revolution*). Petitioner's broad stipulation ensures that the PTAB proceeding is a “true alternative” to the District Court proceeding. *Sand Revolution*, Paper 24, 12 at n.5.

Accordingly, we determine the fourth factor weighs strongly against exercising our discretion to deny institution.

e) Factor 5: whether the petitioner and the defendant are the same in the parallel proceeding

Petitioner and the defendant in the parallel district court litigation are the same parties in the present case. Prelim. Resp. 11. Therefore, this factor weighs in favor of exercising our discretion to deny institution.

f) Factor 6: other circumstances that impact the Board's exercise of discretion, including the merits

The final factor is a catch-all that takes into account any other relevant circumstances. The decision whether to exercise discretion to deny institution under § 314(a) is based on “a balanced assessment of all relevant circumstances in the case, including the merits.” Patent Trial and Appeal Board Consolidated Trial Practice Guide at 58 (November 2019).

Patent Owner argues that the grounds in the Petition are “particularly weak and do not justify instituting on the merits.” Prelim. Resp. 11.

Specifically, Patent Owner argues that “the Petition wholly fails to establish any basis for concluding that ‘training’ is implemented as a new, distinct ‘mode’ in the Hazelzet reference.” *Id.* at 12.

Considering the merits of the unpatentability arguments in the Petition and Patent Owner’s arguments in the Preliminary Response, as discussed below in Sections III.D and III.E, we determine Petitioner has established a reasonable likelihood that Petitioner would prevail with respect to at least one challenged claim. As set forth below, Petitioner presents a strong showing on the merits at this preliminary stage of the proceeding. We also agree with Petitioner that the Board’s decision in IPR2018-00303 finding similar claims in the related patent unpatentable over the same prior art (Hazelzet and Buchmann) signals that the merits in this proceeding favor Petitioner. *See* Reply 6.

Accordingly, we determine the sixth factor weighs against exercising our discretion to deny institution.

3. *Conclusion on Discretionary Denial Under § 314(a)*

As noted in *Fintiv*, we consider the above six factors when taking “a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review.” *Fintiv*, Paper 11 at 6. As discussed above, factor 1 is neutral, factor 5 favors exercising our discretion to deny institution, factors 2, 3, and 6 weigh in favor not exercising our discretion to deny institution, and factor 4 weighs strongly in favor of not exercising our discretion to deny institution.

We determine that the lack of overlap in the issues that will be pursued in this proceeding and in the parallel district court litigation as a result of Petitioner’s Stipulation, the trial date in the parallel district court

litigation, the lack of investment in the parallel district court litigation as of the institution date, the expediency with which the Petition was filed, and the strength of Petitioner's preliminary showing of unpatentability favor institution of *inter partes* review. As such, we determine that, weighing these factors in a holistic analysis, these factors outweigh the fact that the same parties are involved. Therefore, we are not persuaded that the interests of efficiency and integrity of the system would be best served by invoking our authority under § 314(a) to deny institution of a potentially meritorious Petition.

B. Analysis of Discretionary Institution Under 35 U.S.C. § 325(d)

Under 35 U.S.C. § 325(d), when determining whether to institute an *inter partes* review, we “may take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments previously were presented to the Office.” 35 U.S.C. § 325(d). In deciding this issue, the Board uses the following two-part framework: (1) whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office; and (2) if either condition of the first part of the framework is satisfied, whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of the challenged claims. *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6, 7–9 (Feb. 13, 2020) (precedential).

In evaluating whether to exercise our discretion when the same or substantially the same prior art or arguments previously were presented to the Office under section 325(d), we have weighed some common non-

exclusive factors, such as: (a) the similarities and material differences between the asserted art and the prior art involved during examination; (b) the cumulative nature of the asserted art and the prior art evaluated during examination; (c) the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection; (d) the extent of the overlap between the arguments made during examination and the manner in which Petitioner relies on the prior art or Patent Owner distinguishes the prior art; (e) whether Petitioner has pointed out sufficiently how the Examiner erred in its evaluation of the asserted prior art; and (f) the extent to which additional evidence and facts presented in the Petition warrant reconsideration of the prior art or arguments. *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, Case IPR2017-01586, Paper 8, 17–18 (PTAB Dec. 15, 2017) (precedential as to § III.C.5, first paragraph).

Patent Owner states that Kim was asserted in combination with other references in IPR2017-00548, and that the combination of Hazelzet, Buchmann, and Kim was asserted in IPR2018-00303. Prelim. Resp. 14. These IPRs challenge patents related to the '595 Patent. Patent Owner's Mandatory Notice, 1; Pet. 1–3. Patent Owner states that the petitions for IPR2017-00548 and IPR2018-00303, as well as the Hazelzet, Buchmann, and Kim references, were all disclosed to the examiner of the '595 Patent on March 1, 2019, and that the examiner considered the references and petitions before issuing the '595 Patent. *Id.* at 14–15 (Ex. 1002, 194–201). Patent Owner also filed the final written decision for IPR2018-00303 in an information disclosure statement on March 21, 2019, and the Examiner issued a notice of allowance for the '595 Patent on March 29, 2019. Ex. 1002, 175, 182. The final written decision (Paper 42) for IPR2018-

00303 determined that all claims of the US 9,535,623 (“the ’623 Patent”) were unpatentable. Ex. 1034. The ’623 Patent has similar claims to those of the ’595 Patent, i.e., both sets of claims recite memory modules with a module controller with open drain output, printed circuit boards, DRAM elements, edge connections, parity error signals and notification signals output from the open drain output in different modes, etc. Ex. 1001; Ex. 1031.

Patent Owner argues that the question in *Advanced Bionics* is whether the examiner considered the same references as asserted in the petition, and does not require that the examiner consider the Board’s findings in a final written decision. Prelim. Resp. 15–16. Patent Owner contends “[a]bsent a showing that ‘the Office erred in a manner material to the patentability of challenged claims,’ the Board may properly decline to institute a petition which presents the same or substantially the same prior art or arguments previously presented to the Office.” *Id.* at 13 (citing *Advanced Bionics*, Paper 6, 7–9 (Feb. 13, 2020) (precedential)).

The first part of the *Advanced Bionics* framework is met here because Hazelzet, Buchmann, Kim, and the final written decision in IPR2018-00303, were all presented to the Office during examination. With respect to the second part of the *Advanced Bionics* framework, we agree with Petitioner that the examiner clearly erred in a manner material to the claims by overlooking the combinations of Hazelzet, Buchmann, and Kim. Pet. 17. We further find that the examiner erred in a manner material to the claims by failing to sufficiently consider the final written decision in IPR2018-00303, which explained how these references rendered obvious similar claims of the ’623 Patent. Ex. 1034. The final written decision specifically addressed

IPR2020-01042

Patent 10,474,595 B2

combinations of Hazelzet, Buchmann and Kim in relation to the '623 Patent's claims and the reasons for their combination with reasonable expectation of success, such that the Examiner erred by allowing the claims of the '595 Patent in view of that final written decision. Pet. 18. Thus, the Examiner clearly erred in material manner by overlooking the final written decision for IPR2020-00303 in connection with patentability of the '595 Patent's claims.

As to the challenges involving combinations with JEDEC, the parties do not dispute that JEDEC was never before the Examiner during prosecution of the '595 Patent. Pet. 16; *see generally* Prelim. Resp. 12–20. Accordingly, we determine that the combination of Hazelzet and JEDEC, and the combination of Hazelzet, JEDEC and Kim, were not the same or substantially the same as what was previously presented to the Office.

Thus, we determine the examiner erred in failing to consider combinations of Hazelzet, Buchmann, and Kim, and the final written decision in IPR2018-00303, in connection with examination of the '595 Patent. We further determine that JEDEC was not previously presented to the Office. Accordingly, for these reasons, we decline to exercise our discretion to deny institution under 35 U.S.C. § 325(d).

C. Priority Date of the '595 Patent Claims

Petitioner contends that “JEDEC is prior art here because the claims of the 595 Patent are not entitled to their provisional application priority date.” Pet. 1. Specifically, Petitioner contends “[t]he 595 Patent is a continuation of, *inter alia*, a utility application filed June 14, 2010, and also claims priority to U.S. Application No. 61/186,799 (EX1008), filed June 12, 2009. EX1001, Face.” *Id.* at 4. Petitioner asserts that “[t]he claims of the

[']595 Patent are not, however, entitled to the June 2009 date” because certain claim limitations are not found in the provisional application. *Id.* at 4–9.

Patent Owner argues the disputed claim limitations are present in the provisional application and that the “the ’595 patent is entitled to its stated priority date of June 12, 2009.” Prelim. Resp. 20–29.

We address the parties’ arguments in turn below for each claim limitation for which support in the provisional application is disputed by the parties.

1. “wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations”

Petitioner contends each independent claim of the ’595 Patent requires the above negative claim limitation, which allegedly is not supported by the provisional application. Pet. 4–7 (citing Ex. 1001, 14:63–65 (claim 1), 16:19–22 (claim 10), 17:41–44 (claim 17), 18:42–46 (claim 21); Ex. 1003 ¶ 44). Petitioner contends “the provisional says nothing about the memory controller not accessing the module for read and write operations in training mode” and “mentions the word ‘training’ in only one sentence fragment.” Pet. 5–7 (citing Ex. 1008, 25 stating “Error-Out pin: Low during MB training (high signal indicates that training is done).”).

Patent Owner contends “[t]he Provisional Application states that the MCH (memory controller) could be in ‘standby (idle, or wait) while the memory subsystem controller completes its task’” and that the “task is a sequence of initialization operations, which could include training.” Prelim. Resp. 22 (citing Ex. 1008, 22–23). According to Patent Owner, these

statements support that “the Provisional Application reasonably conveys to a POSITA that the memory module is not accessed for normal memory read or write operations during the second mode.” *Id.* at 23.

When a petitioner identifies a claim limitation lacking support in an earlier priority application, as alleged here, the burden shifts to Patent Owner to show that the claims are entitled to the asserted priority date. *Dynamic Drinkware, LLC v. National Graphics, Inc.*, 800 F.3d 1375, 1378–81 (Fed. Cir. 2015). “[T]he test for sufficiency is whether the disclosure of the application relied upon reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date.” *Ariad Pharmaceuticals, Inc. v. Eli Lilly and Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (internal quotations omitted). Negative limitations must have basis in the original disclosure. *In re Herz*, 537 F.2d 549, 551–52 (CCPA 1976). The absence of a positive recitation is insufficient basis for an exclusion. *In re Johnson*, 558 F.2d 1008, 1019 (CCPA 1977).

Patent Owner points to language from the provisional application describing the previous art, not the alleged improvement, as support for the claimed negative limitation. Prelim. Resp. 22; Reply 9; Ex. 1008, 22–23. Specifically, the provisional application states “[t]he shortcoming of the current the [sic] LR-DIMM proposal is that, instead of adopting the notification, the proposal requires the MCH to be in standby (idle, or wait) while the memory subsystem controller completes its task.” Ex. 1008, 22–23. Patent Owner’s reliance on the cited language from the provisional application is misplaced, however, because it does not disclose the claimed limitation. Patent Owner does not identify any statement in the provisional application indicating that the inventor was in possession of “the memory

module in the second mode is not accessed by the memory controller for normal memory read or write operations.”

Accordingly, Patent Owner’s contentions do not persuade us that the claimed phrase is supported in the provisional application on the evidence presented.

2. *“one or more training sequences”*

Petitioner contends the provisional application does not provide support for the claim limitation reciting to “perform operations related to one or more training sequences.” Pet. 7–8 (citing Ex. 1001, 14:65–67 (claim 1); 16:22–25 (claim 10); 17:41–42 (claim 17); 18:42–43 (claim 21); Ex. 1003 ¶ 49); Reply 10. Petitioner contends that the provisional only discloses “MB training” which one would understand as a generic disclosure of “training” a memory buffer in some way. Pet. 7–8 (citing Ex. 1003 ¶ 50). Specifically, Petitioner contends the provisional only discloses “MB training” and does not disclose training “sequences” or “one or more” training sequences. *Id.* at 8.

Patent Owner contends the provisional application discloses “initialization operation sequences” and that MB training is a sequence of training operations that could occur during an initialization period. Prelim. Resp. 26 (citing Ex. 1008, 22); Sur-Reply 4–5.

Reviewing the provisional application, it indeed does disclose “initialization operation sequences.” Ex. 1008, 22. Patent Owner fails, however, to show that the disclosed “initialization operation sequences” include “training sequences,” and “MB training” is mentioned only in the singular. Ex. 1008, 25. Although Patent Owner contends that “MB training” is a sequence of training operations occurring during an

initialization period (Prelim. Resp. 26; Sur-Reply 4–5), Patent Owner fails to identify any evidence to support this contention.

Accordingly, we are not persuaded the provisional application provides support for the claimed limitation on the evidence identified by Patent Owner.

3. *“one or more N-bit-wide data signals . . . where N is at least 32”*

Petitioner contends the above limitation, recited in claim 21, is not supported by the provisional application because “[t]he terms ‘data signal,’ ‘bit,’ ‘width,’ and ‘32’ are found nowhere in the provisional, much less the concept of data signals of a certain width, particularly ‘at least 32.’” Pet. 8 (citing Ex. 1003, ¶ 51); Reply 10.

Patent Owner contends that Petitioner’s expert, Dr. Alpert, acknowledges use of LRDIMMS (Load Reduced Dual Inline Memory Modules) with varying configurations. Prelim. Resp. 27 (citing Pet. 8; Ex. 1003 ¶ 52). Patent Owner contends that the provisional application discloses that the LRDIMMs may include various DRAM densities, ranks, speeds, and configurations, which would reasonably convey that a DIMM could have different bit-widths, including a bit-width of 32 bits. *Id.* (citing Ex. 1008, 23); Sur-Reply 5.

Patent Owner fails to identify any disclosure in the provisional application of DRAM elements that are configurable to communicate N-bit-wide data signals, where N is at least 32, as recited in claim 21. Furthermore, Patent Owner’s citation to Petitioner’s expert is unavailing because we do not see where the cited portion of Dr. Alpert’s testimony acknowledges use of LRDIMMs with varying configurations. In any event,

a disclosure of varying configurations would be insufficient to convey that the inventor was in possession of DRAM elements configurable to communicate data signals of at least 32 bits. Thus, we are not persuaded the provisional application provides support for the claimed limitation on the evidence identified by Patent Owner.

4. *“one or more pins that are not active”*

Petitioner contends “[c]laims 8, 15, 16, 18, and 19 require that ‘the second edge connections include one or more pins that are not active while the memory module is in the second mode,’ or substantially similar ‘pins not active’ limitations.” Pet. 8–9 (citing Ex. 1001, 15:51–53, 17:7–13 (claims 15–16), 17:49–56 (claims 18–19)). Petitioner contends “the terms ‘edge,’ ‘edge connection[s],’ ‘mode’ and ‘active’ appear nowhere in the provisional, much less the concept that certain pins on an edge connection are not active during certain modes, and those concepts are not necessarily comprehended in that disclosure.” *Id.* at 9 (citing Ex. 1003 ¶ 52); Reply 10.

Patent Owner contends the provisional application discloses that the MCH could be in “standby (idle, or wait) while the memory subsystem controller completes its task”; that the task is “an initialization operation sequence that could include training”; that the MCH in standby does not access the memory subsystem for normal memory read or write operations; and that the MCH therefore is “not communicating signals to or from the memory module’s second edge connections.” Prelim. Resp. 28 (citing Ex. 1008, 22–23). Patent Owner contends this “reasonably conveys to a POSITA that the second edge connections include one or more pins that are inactive during a second mode.” *Id.* at 29; Sur-Reply 5.

The provisional application suggests that the need for the MCH to standby while the memory subsystem controller completes a task as a “shortcoming” that its improvement is intended to overcome. Ex. 1008, 22–23. Patent Owner does not explain sufficiently why one would look to a “shortcoming” to supply the claimed feature. Also, Patent Owner relies on a chain of inferences for its contention that the provisional application supports the claimed limitation. Prelim. Resp. 28. Patent Owner does not show with evidence, however, that a person of ordinary skill in the art would have understood this disclosure in the provisional application to convey that the inventor was in possession of the claimed limitation.

Accordingly, we are not persuaded that the provisional application provides support for the claimed limitations on the evidence identified by Patent Owner. Petitioner has sufficiently shown that, since the ’595 Patent is not entitled to the priority date of its provisional application under 35 U.S.C. § 119(e), JEDEC is prior art to the ’595 Patent.

III. ANALYSIS OF CHALLENGES

A. Legal Standards

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) where present, objective

evidence of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

Petitioner contends “[a] person of ordinary skill in the art in the field of the 595 Patent in the 2009-10 time frame (a ‘Skilled Artisan’) would have had a bachelor’s degree in computer engineering, or a related field, and several years of additional experience working with computer memory systems.” Pet. 9. According to Petitioner, “[s]he would have been familiar with computer memory systems and basic CPU architecture documented in the literature, including standards, and generally available in commercial systems, including how computer components access a computer’s memory, the role of the memory controller, the basic operation of memory modules and devices, and the techniques used to couple memory devices to the other components of the computer system.” *Id.* (citing Ex. 1003 ¶ 53). Patent Owner does not dispute Petitioner’s definition of the level of ordinary skill in the art at this time.

To establish the level of ordinary skill in the art, we look to various factors including “the types of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and education level of active workers in the field.” *In re GPAC*, 57 F.3d 1573, 1579 (Fed. Cir. 1995) (citing *Custom Accessories, Inc. v. Jeffrey-Allan Indus., Inc.*, 807 F.2d 955, 962 (Fed. Cir. 1986)). Problems encountered in the art are identified in the background sections of the ’595 Patent as well as in *Hazelzet*, *Buchmann*, and *Kim*. See generally Ex. 1001, 1:20–40; Ex. 1014; Ex. 1016; Ex. 1017. Solutions proposed for these problems are also disclosed in the ’595 Patent and the

prior art references. *See generally* Ex. 1001, 1:41–2:29; Ex. 1014; Ex. 1015; Ex. 1016; Ex. 1017. On the evidence presented, the education level of active workers in the field aligns with Petitioner’s definition of a POSITA. *See* Pet. 9; Ex. 1003 ¶ 53. Considering these factors, for purposes of this decision, we agree with and adopt Petitioner’s definition of a POSITA. We apply this level of ordinary skill in the art in our obviousness analysis.

C. Claim Construction

We construe the challenged claims under the same standard used by a federal court in a civil action under 35 U.S.C. § 282(b). 37 C.F.R. § 42.100(b) (2019). This standard is articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc) and its progeny, and includes “construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” *Id.*

Only claim terms in controversy need to be construed, and only to the extent necessary to resolve the controversy. *See Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

1. “Memory Read or Write Operations”

Petitioner contends that “memory read or write operations” should be interpreted as “operations used to read from or write to memory devices in response to commands from the memory controller.” Pet. 19. Patent Owner does not dispute Petitioner’s construction at this time. *See generally* Prelim. Resp. Accordingly, there is no controversy we need to resolve for this claimed phrase.

2. *“Normal Memory Read and Write Operations”*

Petitioner contends “normal memory read and write operations” means the same as “memory read and write operations.” Pet. 20. Patent Owner does not dispute Petitioner’s interpretation. *See generally* Prelim. Resp. Accordingly, there is no controversy we need to resolve for this claimed phrase.

3. *Conclusion on Claim Construction*

As there is no controversy concerning the meaning of any claim terms and because we discern no dispositive issue implicating claim construction at this time, we provide no explicit construction for any claim terms in this decision. We instead apply the ordinary and customary meanings of the claim terms consistent with 37 C.F.R. § 42.100(b).

D. Ground 1: Asserted Obviousness of Claims 1–24 Based on Hazelzet and JEDEC

Petitioner contends claims 1–24 would have been obvious under 35 U.S.C. § 103(a) based on the combination of Hazelzet and JEDEC. Pet. 39–66.

1. *Hazelzet (Ex. 1014)*

Figure 2 of Hazelzet, reproduced below, shows an enhanced server memory arrangement. Ex. 1014 ¶ 25.

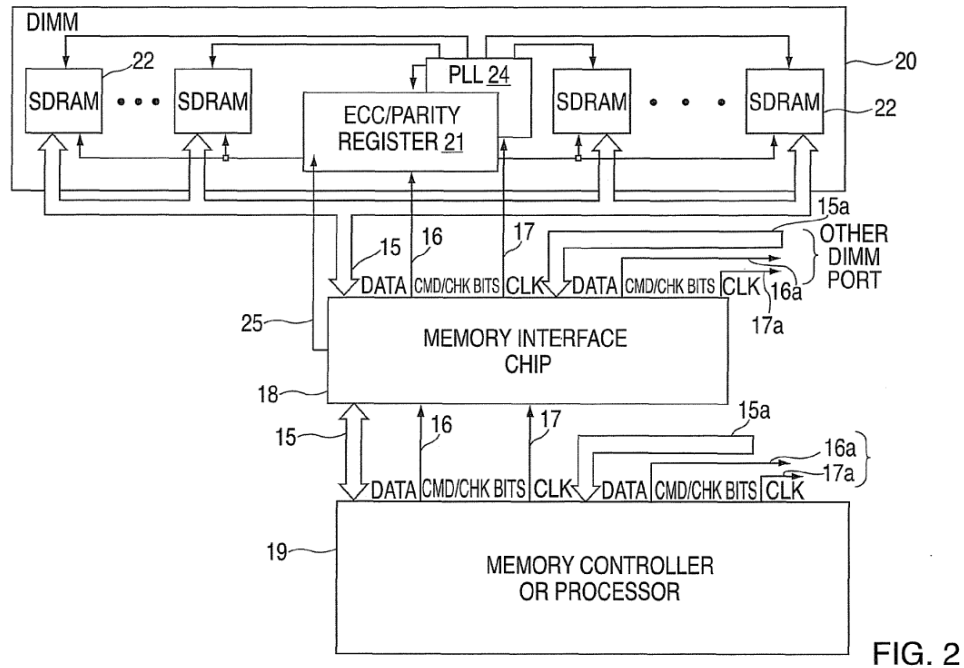


FIG. 2

Hazelzet Figure 2 comprises a DIMM 20 with an ECC/Parity buffer chip 21 coupled to a memory interface chip 18, which is in turn coupled to a memory controller or processor 19. Ex. 1014 ¶ 38. Memory interface chip 18 sends and receives data from the DIMM 20 via data line 15 and sends address and commands via line 16. *Id.* The memory interface chip 18 then sends and receives data via line 15 to the DRAMs 22 and sends address and command information to the register chip 21 via line 16. *Id.* The memory interface chip 18 further sends check bits for error correction purposes to the ECC/Parity register chip 21 via line 25. *Id.*

Hazelzet's DIMM operates in an error correction code (ECC) mode or a parity mode. Ex. 1014 ¶¶ 64, 69–70. In ECC mode, the DIMM corrects single bit errors and detects double bit errors. *Id.* ¶ 69. Correctable errors are reported on an Error (CE) output line 120 and uncorrectable errors are reported on an Error (UE) output line 121. *Id.* ¶ 59, Fig. 4B. In parity

mode, the DIMM detects and reports parity errors via uncorrectable error (UE) line 121. *Id.* ¶ 70.

2. JEDEC (*Ex. 1015*)

JEDEC discloses MB-DRAM Training triggered by a host that runs autonomously on a Memory Buffer (MB) once enabled. *Ex. 1015*, 8. The MB executes DRAM interface training including write leveling to ensure successful writes, and read enable training to ensure the MB can capture read data from the DRAMs correctly. *Id.* No DRAM commands or control word writes can be issued to the MB until the MB-DRAM Interface training is complete. *Id.* Training completion can be signaled by the assertion of *ERROUT#*. *Id.*

3. *Reasons to Combine*

Petitioner contends that the prior art are reasonably pertinent to the problem addressed by the '595 Patent—increasing memory module capacity, performance, and/or reliability by sharing an output pin/path to perform multiple functions during multiple operations/modes, including initialization/training. *Pet. 34* (citing *Ex. 1001*, code (57), 5:66–6:14, 8:4–48; *Ex. 1014*, Abstract, ¶¶ 7, 69–70, 123; *Ex. 1015* ¶¶ 1, 3, 8; *Ex. 1016*, 1:7–9, 3:49–60, 4:51–5:50, 12:60–13:41, 14:1–63, 20:20–21:19, 33:45–67; *Ex. 1017*, 1:16–22, 5:49–57, 6:8–18, 11:20–34, 12:36–53; *Ex. 1003* ¶ 158). Petitioner also contends one “would have considered each of the combinations analyzed here to be merely an arrangement of old elements with each performing the same function it had been known to perform and yielding no more than what one would expect from such an arrangement.” *Pet. 35* (citing *Ex. 1003* ¶¶ 159–160).

Petitioner contends “Hazelzet emphasizes the need for ‘improved overall system reliability.’” Pet. 35 (citing Ex. 1014 ¶¶ 1–4, 7, 42, 44). Petitioner contends “a Skilled Artisan would have been motivated to add training to Hazelzet because it was known that training improved memory module reliability.” Pet. 35 (citing Ex. 1027, 1:35–2:12; Ex. 1025, 15–18; Ex. 1014 ¶ 123; Ex. 1017, 12:36–53; Ex. 1003 ¶ 161). Because JEDEC states its training ensures successful writes, correct reads, and optimal configuration for reads and writes, Petitioner contends “[t]hese statements would have motivated a Skilled Artisan to add training to systems such as Hazelzet to ensure optimal and correct operation.” Pet. 36 (citing Ex. 1015, 3, 8–9; Ex. 1003 ¶ 162).

Petitioner further asserts that “a Skilled Artisan would have been motivated to combine these references by adding training in a mode separate from normal operation because it was known that training before normal operation was necessary to minimize errors, by ‘ensur[ing] successful writes,’ and ‘ensur[ing] [the register on the DIMM] can capture read data from the DRAMs correctly.’” Pet. 36–37 (citing Ex. 1015, 3, 8; Ex. 1025, 15–18; Ex. 1022, Fig. 4, ¶¶ 32, 52, 88–89; Ex. 1056, 18, 22, 25–26, 42–44; Ex. 1057, Fig. 5, Abstract, 2:13–34, 2:60–3:3, 9:11–10:44).

Petitioner contends “[i]t would have been further obvious to communicate training status in the new mode using the same open drain output used in other modes” because both Hazelzet and JEDEC use the same open drain output in two different modes. Pet. 37 (citing Ex. 1014, Figs. 4B, 7A, ¶¶ 44, 49, 59, 64, 69, 72, 109; Ex. 1003 ¶¶ 166–169).

Petitioner contends “[a] Skilled Artisan would also have been so motivated because such multiple use of a pin was known, and would have

been considered an efficient use of the limited number of output pins on integrated circuits. Pet. 38 (citing Ex. 1017, 1:16–22, 5:49–57, 6:8–18; Ex. 1022 ¶¶ 4, 5, 32, 33, 52; Ex. 1003 ¶¶ 170–172). Petitioner further contends “a Skilled Artisan would have been motivated to arrange the modified Hazelzet to communicate signals indicating training completion only when all memory modules have completed that training, in order to ensure that the entire memory system had been trained before proceeding to normal operation.” *Id.* at 38–39 (citing Ex. 1043, 7:30–51; Ex. 1017, Fig. 4, 5:65–6:12; Ex. 1014 ¶¶ 18, 109; Ex. 1003 ¶¶ 147–152, 172–173).

Patent Owner argues that there is no motivation to create a separate training mode in Hazelzet. Prelim. Resp. 34–36. According to Patent Owner, the Board and Petitioner agreed in IPR2018-00303 “that a POSITA would add training to Hazelzet’s ECC mode of operation, which is a normal mode of operation.” *Id.* at 34–35 (citing Ex. 2015, 62; Ex. 2017 ¶ 171). Patent Owner contends “if a POSITA would have been motivated to add training into Hazelzet’s normal mode of operation (i.e., ECC mode), they could not now be motivated to do the exact opposite by adding training to Hazelzet as a separate mode from the normal mode of operation.” *Id.* at 36.

As was the case in the final written decision for IPR2018-00303, however, Patent Owner has not demonstrated here that the prior art combination requires simultaneous, not separate, training and normal modes. *See* IPR2018-00303, Paper 42, 14–18. Dr. Alpert testified that both JEDEC and Buchmann taught that training was necessary before normal operation to ensure successful writes and capture of read data, meaning that the training mode is separate from the normal mode of operation. Pet. 36–37; Ex. 1014 ¶ 123; Ex. 1015, 3, 8; Ex. 1003 ¶¶ 164–165.

Patent Owner further argues, “discordant reconstruction of Hazelzet . . . would be required to add an entirely new mode of operation.”

Prelim. Resp. 37. Patent Owner’s argument appears to assume bodily incorporation of the prior art reference teachings disregarding what the combined teachings of the references would have suggested to those of ordinary skill in the art. *In re Keller*, 642 F.2d 413, 425 (CCPA 1981); *In re Sneed*, 710 F.2d 1544, 1550 (Fed. Cir. 1983); *In re Nievelt*, 482 F.2d 965, 968 (CCPA 1973). As noted above, Dr. Alpert testified that one of ordinary skill in the art would have added training as a separate mode from normal operations. Pet. 36–37 (citing Ex. 1015, 3, 8; Ex. 1003 ¶¶ 164–165).

Reviewing the evidence presented thus far, Petitioner has made a sufficient showing that a POSITA would have combined Hazelzet and JEDEC with a reasonable expectation of success in arriving at the claimed subject matter. On the evidence presented, we find Patent Owner’s argument does not undermine Petitioner’s persuasive showing. We proceed to examine the combination of references in connection with each limitation of claim 1. We note that, outside of motivation to combine, Patent Owner does not make specific arguments regarding the application of the prior art to the limitations of the challenged claims.

4. *Claim 1 of the ’595 Patent*

a) *Summary of Petitioner’s Contentions Regarding Claim 1*

Petitioner contends that Hazelzet discloses memory modules (DIMMs) configured to operate with a memory controller of a host system. *See, e.g.*, Pet. 40. According to Petitioner, Hazelzet’s memory modules have printed circuit boards with edge connections, DRAM elements, open drain outputs, and multiple modes of operation (ECC and parity). *See, e.g.*,

Pet. 40–52. Petitioner relies on JEDEC to disclose a training mode involving training sequences, which when combined with Hazelzet discloses all features of claim 1. *See, e.g.*, Pet. 50–52.

b) Petitioner’s Reading of Claim 1 on the Prior Art Combination

[1.a] A memory module operable with a memory controller of a host system, comprising:

At this stage of the proceeding, we need not, and do not, determine whether the preamble of claim 1 is limiting, because Petitioner shows sufficiently for purposes of institution that the asserted prior art, specifically, the combination of Hazelzet and JEDEC, teaches the preamble.

In particular, Petitioner contends “Hazelzet discloses dual inline memory modules (‘DIMMs’) configured to operate with the ‘memory controller’ of the host system.” Pet. 40 (citing Ex. 1014, Figs. 2, 3A–3D, ¶¶ 36–39; Ex. 1003 ¶ 176).

On this record, Petitioner has made a sufficient showing that Hazelzet discloses claim 1’s preamble, to the extent it is limiting.

[1.b] a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;

Petitioner contends Hazelet’s DIMM comprises a printed circuit board which fits in the slot of the host system. Pet. 42–43 (citing Ex. 1014 ¶¶ 15, 37, 39, 97, Figs. 2, 3A–3D, 9–10; Ex. 1003 ¶¶ 179–181). Petitioner further contends the printed circuit board has a first set of edge connections for communicating data signals between the module and the memory controller

(Pet. 43 (citing Ex. 1014, Figs. 7A–7C, ¶¶ 15, 35, 38, 41; Ex. 1003 ¶ 182)) and a second set of edge connections for communicating address and control signals from the memory controller (Pet. 43 (citing Ex. 1014, Figs. 7A–7C, ¶¶ 15, 35, 38, 41; Ex. 1003, ¶ 183)). Petitioner further contends Hazelzet has an error edge connection coupled to the open drain output of the module controller. Pet. 43 (citing Ex. 1014, Figs. 4B, 7A, ¶¶ 72, 109; Ex. 1003 ¶ 184).

On this record, Petitioner has made a sufficient showing that Hazelzet discloses limitation [1.b] of claim 1.

[1.c] dynamic random access memory elements on the printed circuit board;

Petitioner contends Hazelzet's memory module includes DRAMs on the printed circuit board. Pet. 44 (citing Ex. 1014 ¶ 15, Figs. 2, 3A–3D; Ex. 1003 ¶ 187).

On this record, Petitioner has made a sufficient showing that Hazelzet discloses limitation [1.c] of claim 1.

[1.d] a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection; and

Petitioner contends Hazelzet's ECC/parity register discloses a module controller, and has an uncorrectable error output 121, which is an open drain output. Pet. 44 (citing Ex. 1014, Figs. 3A–3D, 4A–4B, ¶¶ 44, 59, 72).

Petitioner contends Hazelzet's ECC/parity register is on the printed circuit board and is coupled to the DRAMs. *Id.* (citing Ex. 1014, Figs. 3A–3D, ¶¶ 39, 42; Ex. 1003 ¶ 190). Petitioner contends Hazelzet's UE 121 is

coupled to the error edge connection of the module. *Id.* (citing Ex. 1014, Figs. 4B, 7A (pin 142), ¶¶ 59, 72; Ex. 1003 ¶¶ 191–194).

On this record, Petitioner has made a sufficient showing that Hazelzet discloses limitation [1.d] of claim 1.

[1.e.i] wherein the memory module is configurable to operate in any of at least a first mode and a second mode;

Petitioner contends Hazelzet's memory module operates in the parity mode, corresponding to the claimed first mode, and an ECC mode. Pet. 44 (citing Ex. 1014, Fig. 8, ¶¶ 64, 69–72; Ex. 1003 ¶ 196. Petitioner contends JEDEC discloses a second mode in which training of the memory module would be carried out. *Id.*

On this record, Petitioner has made a sufficient showing that Hazelzet discloses that its memory module is configurable to operate in any of two modes, and that JEDEC discloses a training mode, which, when combined with Hazelzet, discloses limitation [1.e.i] in claim 1.

[1.e.ii] wherein the memory module in the first mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections,

Petitioner contends that Hazelzet's memory module is configurable to receive address and control signals via the edge connections. Pet. 45 (citing Ex. 1014, ¶¶ 15, 35, 38, 41, Figs. 2, 7A–7B; Ex. 1003 ¶ 197). Petitioner further contends Hazelzet's memory module communicates address and command information normally as a JEDEC compliant device, sending address and control to the register and data to the DRAMs. *Id.* (citing Ex. 1014 ¶¶ 44, 75, Fig. 8; Ex. 1024, 1, 14, 16; Ex. 1003 ¶¶ 198–201). Petitioner contends Hazelzet discloses that these operations occur during the

parity mode, which is a normal mode of operation. Pet. 45–46 (citing Ex. 1014, ¶¶ 64, 70, 75; Ex. 1003 ¶ 199–200).

On this record, Petitioner has made a sufficient showing that Hazelzet discloses limitation [1.e.ii] of claim 1.

[1.e.iii] wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations, and

Petitioner contends that, during the training sequences, JEDEC's memory controller communicates no data with the module and performs no operations to read or write to the memory devices, and that the training is carried out by memory buffer (module controller) itself. Pet. 32, 47–48 (citing Ex. 1015, 8; Ex. 1003 ¶¶ 154, 211).

On this record, Petitioner has made a sufficient showing that the combination of Hazelzet and JEDEC discloses limitation [1.e.iii] of claim 1.

[1.e.iv] wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences;

Petitioner contends Hazelzet's memory module can be placed into a training mode to implement JEDEC's training sequences. Pet. 48 (citing Ex. 1015, 8; Ex. 1003 ¶ 212).

On this record, Petitioner has made a sufficient showing that the combination of Hazelzet and JEDEC discloses limitation [1.e.iv] of claim 1.

[1.f.i] wherein the module controller is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations,

Petitioner contends Hazelet's memory module in parity mode receives address and control signals for performing normal memory read or write

operations over the edge connections. Pet. 48 (citing Ex. 1014, Figs. 2, 7A–7B, ¶¶ 15, 35, 38, 41, 64, 70; Ex. 1003 ¶ 214).

On this record, Petitioner has made a sufficient showing that Hazelzet discloses the limitation [1.f.i] of claim 1.

[1.f.ii] wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and

Petitioner contends Hazelzet discloses that the printed circuit board has edge connections for communicating data signals between the DRAMs and the system memory controller. Pet. 49 (citing Ex. 1014, Figs. 7A–7C, ¶¶ 15, 35, 38, 41). Petitioner contends the DRAMs communicate the data signals while the memory module is in the parity mode, and in accordance with the received address and control signals. *Id.* (citing Figs. 2, 8, ¶¶ 15, 35, 38, 41, 64, 70; Ex. 1003, ¶¶ 197–205, 215).

On this record, Petitioner has made a sufficient showing that Hazelzet discloses limitation [1.f.ii] of claim 1.

[1.f.iii] wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the first mode;

Petitioner contends Hazelzet's error edge connection (pin 142) is coupled to the open drain output (UE 121) of the module controller (ECC/parity register). Pet. 49 (citing Ex. 1014, Figs. 4B, 7A (pin 142), ¶¶ 59, 72; Ex. 1003 ¶ 216). Petitioner contends Hazelzet's SEC/DED ECC 90 includes a parity generator/checker circuit 231. *Id.* (citing Ex. 1014, Fig. 4B, Fig. 5, ¶¶ 28, 76; Ex. 1003 ¶ 217). Petitioner contends in the first mode (parity mode), the parity generator/checker circuit 231 generates and sends

the parity error signal (PERR) to the error logic circuit 100, and outputs it to the memory controller through the output line UE 121, which is an open-drain output coupled to the memory controller using pin 142. Pet. 49–50 (citing Ex. 1014, Figs. 4–5, 7A (pin 142), ¶¶ 38, 59, 70, 72, 76; Ex. 1003 ¶ 218–222).

On this record, Petitioner has made a sufficient showing that Hazelzet discloses limitation [1.f.iii] of claim 1.

[1.g] wherein the module controller in the second mode is further configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection to a first state or to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.

Petitioner contends Hazelzet's memory module modified with JEDEC's training mode outputs training status signals (ERROUT#) to the system memory controller via open drain output (UE 121). Pet. 51–52; Ex. 1014 ¶¶ 99, 123; Ex. 1015, 3, 8; Ex. 1003 ¶¶ 147–154, 156–157. Petitioner contends Hazelzet's memory system shares the open drain output so that the memory controller can receive notification signals from multiple modules using the open drain output. Pet. 50–51 (citing Ex. 1014 ¶¶ 18, 72, 109; Ex. 1003 ¶ 226). Petitioner contends the added training status signals would be at a low logic level at open drain outputs (UE121) because the gate signal of the transistors are high, until training completes for all modules, at which time all status signals would be in a high impedance state to signal completion of training. Pet. 51 (citing Ex. 1003 ¶ 227). Petitioner contends the open drain status signals change from high impedance states to low states as the gates of the transistors change from low to high to indicate

training is in progress, and change from high impedance to low logic level to indicate training operations have completed in each memory module.

Pet. 51–52 (Ex. 1014, Fig. 4B, ¶¶ 59, 70, 72; Ex. 1003 ¶ 228).

On this record, Petitioner has made a sufficient showing that the combination of Hazelzet and JEDEC discloses limitation [1.g] of claim 1.

c) Conclusion for Claim 1

In light of the foregoing discussion, we determine that the information presented in the Petition, and accompanying exhibits and testimony, shows that there is a reasonable likelihood that Petitioner would prevail with respect to claim 1 challenged in the Petition. Petitioner makes a sufficient showing that each limitation of claim 1 is taught or suggested by the combination of Hazelzet and JEDEC, and that a person of ordinary skill in the art had reason to combine the references, with a reasonable expectation of success in arriving at the memory module of claim 1.

5. Claim 10

Claim 10 is similar to claim 1 except that it requires the module controller to be “configurable to drive the open drain output from a first state to a second state and from the second state to the first state.” Ex. 1001, 16:8–11. Petitioner contends this limitation is disclosed by Hazelzet’s teaching that open drain signals would be low logic levels to indicate the training sequence (MB-DRAM) was in progress, or in a high-impedance state to indicate the training sequence has been completed in all memory modules. Pet. 59–60 (citing Ex. 1014, Figs. 4B–5, ¶¶ 59, 70, 72, 76; Ex. 1003 ¶¶ 147–152, 157, 302, 305).

On this record, Petitioner’s evidence shows that there is a reasonable likelihood that Petitioner would prevail with respect to claim 10 challenged in the Petition.

6. *Claim 17*

Claim 17 is a method claim reciting similar features as the memory module of claim 1. We have reviewed Petitioner’s evidence (Pet. 61–63) and find that it presents a reasonable likelihood that Petitioner would prevail with respect to claim 17 challenged in the Petition.

7. *Claim 21*

Claim 21 is similar to claim 1 in many respects but recites a “module controller including a transistor having a gate and an open drain output coupled to the error edge connection.” Ex. 1001, 18:17–19. Claim 21 further recites that the DRAM elements “are configurable to communicate one or more N-bit-wide data signals . . . where N is at least 32.” We find no express mention of these features in the combination of Hazelzet and JEDEC, and we decline to reach the question of whether a reasonable likelihood of unpatentability has been presented for these claims.

8. *Dependent Claims*

We find Petitioner’s evidence sufficient to establish a reasonable likelihood that Petitioner would prevail with respect to dependent claims 2, 8, 9, 11, 14, 15, and 18 on the combination of Hazelzet and JEDEC. Pet. 52 (claims 2 and 11); Pet. 57–58 (claims 8, 9, 15, 18); Pet. 56–57 (claim 14).

E. Other Grounds

For ground 2, after reviewing the Petition, and accompanying exhibits and testimony, we determine that Petitioner has presented a reasonable likelihood to prevail in showing unpatentability of claims 1, 2, 8–11, 14, 15

and 18 over the combination of Hazelzet and Buchmann. Pet. 40–52 (claim 1); Pet. 52 (claims 2, 11); Pet. 56–57 (claim 14); Pet. 57–58 (claims 8, 9, 15, 18); Pet. 58–60 (claim 10). In ground 2, Buchmann’s training sequences are used instead of JEDEC’s and the reasons for combining Buchmann with Hazelzet with a reasonable expectation of success are similar to ground 1 analyzed above. Pet. 34–39. Except for Patent Owner’s arguments regarding the motivation to combine addressed above, Patent Owner does not dispute Petitioner’s application of the prior art to the limitations of the challenged claims for ground 2.

For ground 3, after reviewing the Petition, and accompanying exhibits and testimony, we determine Petitioner has presented a reasonable likelihood to prevail in showing unpatentability of claims 3–7, 12–14, and 20 over Hazelzet, JEDEC or Buchmann, and Kim. Pet. 66–71. Kim discloses open-drain transistors and an OR gate receiving multiple error signals with output connected to the gate of an open-drain transistor. Pet. 66–67 (citing Ex. 1017, 6:13–18, Figs. 4–5; Ex. 1003 ¶ 238). Petitioner contends one of ordinary skill in the art would have combined Kim with Hazelzet and JEDEC or Buchmann because it is “merely an arrangement of old elements with each performing the same function it had been known to perform and yielding no more than what one would expect from such an arrangement.” Pet. 35 (citing Ex. 1003 ¶¶ 159–160). Petitioner also contends one of ordinary skill in the art would have been motivated to use the open-drain techniques of Kim because it represented a well-known, reliable and simple technique to provide error and status information from a number of components in different modes. Pet. 70 (citing Ex. 1014, ¶¶ 72, 122; Ex. 1017, 5:65–6:18, 12:18–23, Figs. 4–5; Ex. 1003 ¶ 141). Petitioner

further contends Kim's open-drain technique permitted a single signal line with an OR logic element to indicate error and status information, thus simplifying the design of the system and saving pins on the various integrated circuits connect to the bus. Pet. 70–71 (citing Ex. 1003 ¶¶ 233, 250–252, 312–317, 335, 354, 356). Except for Patent Owner's arguments regarding motivation to combine Hazelzet with JEDEC or Buchmann addressed above, Patent Owner does not dispute Petitioner's application of the prior art to the limitations of the challenged claims for ground 3.

IV. CONCLUSION

In light of the foregoing, Petitioner has demonstrated a reasonable likelihood of prevailing on its assertions that claims 1–24 of the '595 Patent would have been obvious under 35 U.S.C. § 103. Accordingly, we institute trial on all of claims 1–24 on the grounds of unpatentability asserted by Petitioner. *See SAS Institute, Inc. v. Iancu*, 138 S. Ct. 1348 (2018).

At this stage of the proceeding, we have not made a final determination with respect to the patentability of the challenged claims or to the construction of any claim term.

V. ORDER

For the foregoing reasons, it is

ORDERED that pursuant to 35 U.S.C. § 314(a), an *inter partes* review of claims 1–24 of the '595 Patent is hereby instituted on the grounds of unpatentability set forth in the Petition; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial will commence on the entry date of this decision.

IPR2020-01042
Patent 10,474,595 B2

For PETITIONER:

Joseph A. Micallef
Michael D. Hatcher
SIDLEY AUSTIN LLP
jmicallef@sidley.com
mhatcher@sidley.com

For PATENT OWNER:

William Meunier
Serge Subach
MINTZ, LEVIN, COHN, FERRIS, GLOVSKY AND POPEO, P.C.
wameunier@mintz.com
ssubach@mintz.com