IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

SAMSUNG ELECTRONICS CO., LTD. AND SAMSUNG SEMICONDUCTOR, INC.,	)	
Plaintiffs,	)	C.A. No. 21-1453 (RGA)
v.	)	
	)	**DEMAND FOR JURY TRIAL**
NETLIST, INC.,	)	
Defendant.	)	

FIRST AMENDED COMPLAINT FOR DECLARATORY JUDGMENT OF NON-INFRINGEMENT AND UNENFORCEABILITY; BREACH OF CONTRACT

Plaintiffs Samsung Electronics Co., Ltd. ("SEC") and Samsung Semiconductor, Inc. ("SSI" and together with SEC, "Samsung") seek a declaration that Samsung does not directly or indirectly infringe United States Patent Nos. 10,217,523 (the "'523 patent"), 10,474,595 (the "'595 patent"), 9,858,218 (the "'218 patent"), 7,619,912 (the "'912 patent"), 10,860,506 (the "'506 patent"), 10,949,339 (the "'339 patent"), and 11,016,918 (the "'918 patent") (collectively, the "Patents-in-Suit") (Exhibits 1–7), either literally or under the doctrine of equivalents; a declaration that certain of the Patents-in-Suit are unenforceable due to inequitable conduct and unclean hands; and, alternatively, a ruling that Defendant Netlist, Inc. ("Netlist") has breached contractual obligations owed to Samsung, including obligations to license its allegedly essential patents and patent applications to Samsung and its affiliates on reasonable and non-discriminatory ("RAND") terms and conditions, as follows:

NATURE OF THE ACTION

1. This is an action for a declaratory judgment and breach of contract arising under the patent laws of the United States, Title 35 of the United States Code, the Declaratory Judgment Act, 28 U.S.C. § 2201 *et seq.*, and state contract law.

2. Samsung requests this relief because Netlist has, without justification, unilaterally attempted to terminate a November 2015 Joint Development and License Agreement ("Agreement") in which Netlist granted Samsung a perpetual, paid-up, worldwide license to, among others, the Patents-in-Suit. Samsung believes that it is licensed to the Patents-in-Suit under the Agreement. Netlist, however, claims it has terminated the Agreement, and Netlist asserts that Samsung infringes the Patents-in-Suit, including in litigation against a user of Samsung products, in license demands made to Samsung, and in litigation against Samsung. Thus, Samsung seeks a declaration that it does not infringe the Patents-in-Suit and that certain of the Patents-in-Suit are unenforceable. In the alternative, Netlist has breached its commitment to license on RAND terms and conditions, as Netlist insists the Patents-in-Suit are necessarily infringed by the practice of certain standards promulgated by the Joint Electron Device Engineering Council ("JEDEC") and implemented by the accused Samsung memory modules.

3. Accordingly, for the reasons set forth herein, Samsung seeks a declaratory judgment that it does not infringe the Patents-in-Suit, a declaratory judgment that certain of the Patents-in-Suit are unenforceable due to inequitable conduct and unclean hands, and, alternatively, relief for Netlist's breaches of contractual obligations owed to Samsung, including obligations to license its allegedly essential patents and patent applications to Samsung and its affiliates on RAND terms and conditions.

THE PARTIES

4. Samsung Electronics Co., Ltd. ("SEC") is a corporation organized and existing under the laws of the Republic of Korea, with its principal place of business at 129, Samsung-ro, Yeongtong-gu, Suwon-si, Gyeonggi-do, 443-742, Republic of Korea.

5. Samsung Semiconductor, Inc. ("SSI") is a corporation organized and existing under the laws of the State of California, with its principal place of business at 3655 North First Street, San Jose, California 95134.

6. On information and belief, Netlist is a corporation organized and existing under the laws of the State of Delaware, with its principal place of business at 175 Technology Drive, Suite 150, Irvine, California 92618.

JURISDICTION AND VENUE

7. This Court has subject matter jurisdiction over the claims for declaratory judgments of non-infringement and unenforceability (Counts I–XI) under 28 U.S.C. §§ 1331, 1338(a), and 2201(a).

8. This Court has subject matter jurisdiction over the breach of contract claim (Count XII) pursuant to 28 U.S.C. § 1367. The breach of contract claim forms part of the same case or controversy as the claims for declaratory judgment of non-infringement and unenforceability asserted by Samsung in this action.

9. This Court has personal jurisdiction over Netlist, a corporation organized and existing under the laws of the State of Delaware.

10. Venue is proper in this District under 28 U.S.C. § 1391(b)–(c) because Netlist is subject to personal jurisdiction in this District.

11. An immediate, real, and justiciable controversy exists between Samsung and Netlist as to whether Samsung has infringed the Patents-in-Suit and whether certain of the Patents-in-Suit are unenforceable.

12. For example, and as discussed more fully below, shortly after Netlist unilaterally declared that Samsung was no longer licensed to Netlist's patent portfolio, Netlist issued a "Notice of Infringement" letter to SEC and SSI, in which Netlist asserted that certain Samsung memory modules infringe Netlist's patents, including the '523, '595, and '218 patents. Netlist sent this letter after filing a lawsuit against Samsung seeking a judicial declaration that Samsung's license has been terminated.

13. Moreover, Netlist previously asserted the '523, '595, and '218 patents in litigation against SK hynix, and in doing so served claim charts that purport to demonstrate infringement based on compliance with certain JEDEC memory standards. The Samsung memory modules at issue in this action implement those same standards.

14. In an ongoing patent infringement lawsuit against Google, Netlist recently amended its infringement contentions to allege that Google's servers (which include Samsung's standard-compliant memory modules) infringe the '912 patent. Netlist first provided notice to Google on May 19, 2021, in the form of a claim chart, that Netlist would assert that JEDEC standard-compliant DDR4 LRDIMM and RDIMM memory modules incorporated in Google's servers infringe claim 16 of the '912 patent. Netlist's amended infringement contentions, served on June 18, 2021, formally alleged that certain JEDEC standard-compliant DDR4 LRDIMM and RDIMM memory modules—including memory modules supplied by SSI—practice each and every limitation in claim 16. As a direct and proximate result of Netlist's patent enforcement

activities with respect to the ’912 patent, Samsung has received demands for indemnification, including from Google and Lenovo.

15. In addition, Netlist previously asserted the ’912 patent in litigation against Inphi Corporation, and in doing so served claim charts that purport to demonstrate infringement based on compliance with certain JEDEC memory standards.

16. Netlist has also accused SEC, SSI, and one of their affiliates, in a case Netlist filed on December 20, 2021, of infringing the ’506, ’339, and ’918 patents in connection with the making, sale, use, and/or importation of certain Samsung memory modules.

17. Netlist has also recently asserted patents, including patents related to the Patents-in-Suit, in multiple litigations against Micron Technology, Inc. and its affiliates (collectively, “Micron”), which are competitors of Samsung with respect to at least certain of the memory products at issue. *Netlist, Inc. v. Micron Technology, Inc. et al.*, Case No. 6:21-cv-430 (W.D. Tex.) (the “Micron -430 Litigation”); *Netlist, Inc. v. Micron Technology, Inc. et al.*, Case No. 6:21-cv-431 (W.D. Tex.) (the “Micron -431 Litigation”). In the Micron -431 Litigation, Netlist alleges that Micron’s JEDEC standard-compliant memory modules infringe three patents, two of which are related to the ’506 patent at issue in the present case. *See* Micron -431 Litigation, D.I. 1, ¶ 2. Specifically, the ’506 patent is a continuation of Application No. 15/820,076, now U.S. Patent No. 10,268,608 (the “’608 patent”), which is a continuation of Application No. 15/426,064, now U.S. Patent No. 9,824,035 (the “’035 patent”). Netlist has accused Samsung of infringement with respect to memory modules implementing the same standards to which the ’608 and ’035 patents are allegedly essential.

18. In the Micron -430 Litigation, Netlist alleges that certain Micron memory products infringe U.S. Patent No. 8,301,833 (the “’833 patent”). The ’833 patent is a parent of the

’918 patent at issue in the present case, by way of several intermediate continuation and continuation-in-part applications.

19. Furthermore, between May 2020 and the present, Netlist made demands that Samsung take a second license to Netlist’s portfolio of patents based on Netlist’s claim that it terminated the fully paid-up, worldwide patent license granted in the Agreement.

20. Accordingly, as set forth herein, Netlist has engaged in affirmative acts related to the enforcement of the Patents-in-Suit against specific Samsung products currently being sold and used throughout the United States and against third-party products that implement the same standards as the Samsung products. Because this action presents an actual controversy with respect to the Patents-in-Suit, the Court may grant the declaratory relief sought pursuant to 28 U.S.C. § 2201 *et seq*.

BACKGROUND

A. Netlist’s Extraordinary License Demand and Infringement Threats

21. On November 12, 2015, Netlist and SEC entered into a Joint Development and License Agreement (the “Agreement”). The Agreement contains cross-license, joint development, and product supply provisions.

22. In the Agreement, Netlist granted SEC and its subsidiaries, including SSI, a perpetual, paid-up, worldwide, non-exclusive license to all patents owned or controlled by Netlist or any of its subsidiaries having an effective first filing date on or prior to November 12, 2020. The license extends through the expiration of the last to expire of the licensed patents.

23. SEC similarly granted Netlist and its subsidiaries a perpetual, paid-up, worldwide, non-exclusive license to all patents owned or controlled by SEC or any of its subsidiaries having an effective first filing date on or prior to November 12, 2020.

24. The Agreement required SEC to make a payment to Netlist of $8 million subject to the terms and conditions therein. SEC made this payment to Netlist except for a portion that was remitted as tax withholding to the Korean tax authorities, which later refunded the withheld portion to Netlist.

25. Netlist is now taking extraordinary actions to back out of its grant of a patent license to Samsung.

26. On May 27, 2020, Netlist's Chief Licensing Officer, Marc J. Frechette, wrote to Mr. Seung Min Sung of SEC, and alleged that Samsung materially breached the Agreement by "repeatedly fail[ing] to fulfill Netlist's request for NAND and DRAM products throughout the term of the Agreement" and, allegedly, by improperly deducting withholding taxes. Netlist did not allege, and has never alleged, that Samsung breached the Agreement in any way related to the patent cross-license. In the same letter—which was the first time Netlist raised its breach allegations—Mr. Frechette informed Mr. Sung that Netlist had filed a complaint in U.S. District Court for the Central District of California with respect to the alleged breach by Samsung and provided a copy of the complaint for reference.

27. On May 28, 2020, the U.S. District Court for the Central District of California docketed Netlist's breach of contract complaint against SEC. *Netlist Inc. v. Samsung Electronics Co., Ltd.*, No. 8:20-cv-00993-MCS (C.D. Cal.) ("Breach Action").

28. Netlist subsequently wrote to SEC to terminate the Agreement, including the patent license to SEC and its subsidiaries. On July 15, 2020, Netlist's Chief Licensing Officer, Marc J. Frechette, wrote to Mr. Seung Min Sung of SEC and stated that "Netlist is hereby terminating, effective immediately, the Agreement including the patent license granted to Samsung . . . ."

29. One week later, on July 22, 2020, Netlist amended its complaint in the Breach Action, seeking a declaration that the license it granted Samsung, *but not the license Samsung granted Netlist*, is terminated. In the Breach Action, Netlist seeks monetary damages and a declaration "that Netlist has terminated the Agreement pursuant to Section 13.2 and that Samsung's licenses and rights under the agreement have ceased."

30. Netlist then issued a "Notice of Infringement" to Samsung and a demand that Samsung take a second license to Netlist's patents.

31. Specifically, on October 15, 2020, Netlist's outside counsel in the Breach Action wrote to SEC's outside counsel in the Breach Action and to the General Counsel of SSI, copying Netlist's Chief Licensing Officer, Marc J. Frechette, providing notice of Samsung's alleged infringement of Netlist's portfolio of patents. Netlist stated that because it had terminated the Agreement, "Samsung is no longer licensed to any of Netlist's portfolio of patents." Netlist further asserted that its patents relate to Load Reduced Dual In-Line Memory Modules ("LRDIMMs") and/or Registered Dual In-Line Memory Modules ("RDIMMs"). Netlist then alleged: "Despite the termination of the Joint Development and License Agreement, Samsung continues to unlawfully utilize Netlist's innovations and to infringe Netlist's patents, including United States Patent Nos. 10, 217,523, 10,474,595, and 9,858,218." Netlist concluded the letter by demanding that "Samsung and its subsidiaries honor third-party intellectual property rights" and engage in "formal licensing discussions." Netlist further stated that it "reserves all rights and remedies" with respect to the alleged infringement.

32. Netlist resumed its communications with Samsung in 2021. On February 2, 2021, Netlist's Chief Licensing Counsel, Mr. Marc J. Frechette, indicated by email that Samsung

must take a *second* license, coupled with the demand that Netlist "be made whole" for any alleged breach asserted in the Breach Action.

33. Accordingly, Netlist seeks to double-dip, with a demand that Samsung take a second license to Netlist's patents.

34. On October 14, 2021, the court in the Breach Action issued a confidential order granting summary judgment in favor of Netlist on Netlist's Third Claim for Relief, which seeks a declaration that Netlist terminated Samsung's license effective July 20, 2020. *See Netlist Inc. v. Samsung Electronics Co., Ltd.*, No. 8:20-cv-00993-MCS, D.I. 186 (C.D. Cal.). The court also granted summary judgment in Netlist's favor that Samsung was liable for certain alleged breaches of other provisions in the Agreement. *See id.*

35. Beginning on December 1, 2021, the court in the Breach Action held a jury trial on damages for one of the alleged breaches (the alleged failure to fulfill Netlist's orders for NAND and DRAM products). On December 3, 2021, the jury returned a verdict in Samsung's favor, finding that Netlist failed to prove that it suffered any damages for this alleged breach. *See* Breach Action, D.I. 276. The court in the Breach Action will decide whether or not Netlist is entitled to its alleged damages for the remaining alleged breach (the withholding of taxes) as a matter of law. The parties are briefing the court on this dispute. On January 10, 2022, Samsung filed a motion for entry of judgment in Samsung's favor as to Netlist's First and Second Claims for Relief and, as to Netlist's Third Claim for Relief, for entry of judgment in Samsung's favor or, in the alternative, a trial on the claim.

36. Despite losing at trial, Netlist issued a press release claiming to be "very pleased with the overall outcome of the case as it confirmed that Samsung no longer has a valid license to Netlist patents and therefore requires a licensing agreement." Netlist Provides Update

on Action in Federal Court Against Samsung, https://investors.netlist.com/websites/netlist/English/2120/us-press-release.html?airportNewsID=a661884d-0025-46ea-a055-bae8d8e4570b (last visited Jan. 18, 2022).

37. SEC intends to challenge the summary judgment ruling in the Breach Action through further proceedings in the district court and, if necessary, on appeal. SEC maintains that it did not breach the Agreement, that the Agreement has not been terminated, and that it continues to hold a paid-up, worldwide, non-exclusive license to Netlist's patents, including the Patents-in-Suit. Further, regardless of whether the Agreement was properly terminated (which Samsung disputes), Samsung, its customers, and its end users are not liable for infringement of the Patents-in-Suit for any memory modules made, used, sold, offered for sale, or imported before July 20, 2020, the date of which the purported termination became effective.

B. Netlist's Patent Infringement Lawsuits

38. Over the past decade, Netlist has engaged in a widespread litigation campaign against suppliers of JEDEC standard-compliant memory modules, component suppliers, and users of memory modules. During this campaign, Netlist has alleged infringement of each of the Patents-in-Suit based on the practice of JEDEC memory standards.

39. In Netlist's litigation against SK hynix, a competitor of Samsung, Netlist asserted the '523, '595, and '218 patents—the three patents identified in Netlist's October 2020 letter to Samsung—based on the practice of certain JEDEC memory standards. On October 15, 2021, SEC filed petitions for *Inter Partes* Review ("IPR") challenging the validity of all claims of the '523, '595, and '218 patents. *See* IPR2022-00063 ('523 patent); IPR2022-00064 ('595 patent); IPR2022-00062 ('218 patent). The Patent Trial and Appeal Board previously instituted trial on the same claims and on the same grounds based on petitions filed by SK hynix. *See* IPR2020-01421

('523 patent); IPR2020-01042 ('595 patent); IPR2020-01044 ('218 patent). The SK hynix proceedings were terminated due to settlement shortly after institution.

40. Netlist has asserted the '912 patent (at issue here and licensed to Samsung through the Agreement) in a lawsuit filed against Google. *See Netlist, Inc. v. Google Inc.*, No. 09-cv-05718 (N.D. Cal.) ("Google Infringement Action"). On June 18, 2021, Netlist amended its infringement contentions to accuse Google of infringing the '912 patent based on Google's use of DDR4 LRDIMM and RDIMM memory modules supplied by SSI in Google's computer systems and servers. Specifically, Netlist's amended infringement contentions include the contention that DDR4 LRDIMM and RDIMM memory modules infringe claim 16 of the '912 patent. On information and belief, until Netlist served a claim chart on Google in May 2021, just prior to formally serving amended infringement contentions in June 2021, Netlist had not previously accused DDR4 memory modules supplied by SSI in the Google Infringement Action.

41. On information and belief, Netlist's amended infringement contentions in the Google Infringement Action allege that JEDEC standard-compliant DDR4 memory modules—including DDR4 memory modules supplied by SSI—practice each and every limitation in claim 16. *See* Google Infringement Action, D.I. 174-1 (Ex. 8) at 2 ("[C]laim 16 reads on the DDR4 standard and later technology."); *id.* at 3 ("Netlist asserted claim 16 against Google's memory modules compliant with certain portions of the JEDEC DDR4 standards on May 19, 2021."); *id.* at 9 ("[A]s to standardized products, currently only DDR4 DIMMs that comply with certain JEDEC DDR4 standards while operating in PDA mode (or products that operate in a similar manner) infringe claim 16."); Google Infringement Action, D.I. 194 (Ex. 9) at 4 ("Netlist served Google infringement contentions explaining how memory modules compliant with certain

portions of the JEDEC standards for DDR4 infringe claim 16 when operating in PDA mode."). Netlist's infringement allegations, therefore, are based on the practice of the DDR4 standards.

42. Netlist also seeks an injunction in the Google Infringement Action, which would preclude Google from using the JEDEC compliant LRDIMM and RDIMM memory modules supplied by SSI to Google.

43. On July 6, 2021, Google made an indemnification request to SSI in connection with Netlist's assertion in the Google Infringement Action of the '912 patent against Google's use of Samsung's DDR4 LRDIMM and RDIMM memory modules.

44. On July 19, 2021, Lenovo made an indemnification request to SSI in connection with Netlist's assertion in the Google Infringement Action of claim 16 of the '912 patent against Google's use of Lenovo's "Octopod" servers, which contain Samsung's DDR4 LRDIMM and RDIMM memory modules.

45. As noted above, Netlist has also asserted the '912 patent against Inphi, a chip supplier, based on the practice of certain JEDEC memory standards.

46. On December 20, 2021, Netlist filed a lawsuit against SEC, SSI, and a related company, Samsung Electronics America, Inc. ("SEA"), in the U.S. District Court for the Eastern District of Texas alleging direct and indirect infringement of the '506, '339, and '918 patents. *Netlist, Inc. v. Samsung Electronics Co., Ltd.*, No. 2:21-cv-00463, D.I. 1 (E.D. Tex.) (the "Texas Infringement Action"). Netlist alleges that the defendants directly infringe the '506 and '339 patents in connection with the making, selling, using, and/or importing of DDR4 LRDIMM memory modules, *see id.*, ¶¶ 40, 53, and that the defendants directly infringe the '918 patent in connection with the making, selling, using, and/or importing of DDR5 LRDIMM, RDIMM,

SODIMM, and UDIMM memory modules, *see id.* ¶ 68. Netlist also alleges indirect infringement of all three patents under 35 U.S.C. § 271(b) and (c). *See id.* ¶¶ 49, 50, 64, 65, 76, 77.

47. Among other things, Netlist's prayer for relief requests "all equitable relief the Court deems just and proper as a result of Samsung's infringement." *Id.* at 48.

48. Netlist's Complaint in the Texas Infringement Action states that Netlist intends to assert against SEC, SSI, and SEA a patent resulting from pending Application No. 17/138,019 (the "'019 application"), once it issues from the United States Patent and Trademark Office ("Patent Office"). *See id.* ¶ 32. The '019 application, which is a continuation of the '918 patent, is expected to issue on January 25, 2022, as U.S. Patent No. 11,232,054.

49. Netlist filed the Texas Infringement Action the same day that it moved to dismiss the present action based on, *inter alia*, an alleged lack of any case or controversy over Samsung's declaratory judgment claims. *See* D.I. 11 at 3 (arguing that the present case does not involve a "substantial controversy of sufficient immediacy").

50. The claims in the Texas Infringement Action overlap substantially with the claims asserted in the original complaint in the present action. For example, all of the patents relate to the same area of technology—computer memory modules—and as discussed below, Netlist contends that all of the patents are essential to JEDEC standards relating to such modules. Samsung's original complaint in the present action was directed to LRDIMMs and RDIMMs—the products identified in Netlist's October 2020 notice letter—and Netlist likewise accuses both LRDIMMs and RDIMMs in the Texas Infringement Action. Moreover, all of the patents are subject to the license Netlist granted to Samsung in the Agreement and later attempted to terminate.

51. The claims asserted in the Texas Infringement Action also implicate Samsung's breach of contract claim in the present case (Count XII). As with the original patents-

in-suit in this case, Netlist contends that practice of the JEDEC standard constitutes infringement of the patents asserted in the Texas Infringement Action, and yet Netlist has failed to offer a RAND license for any of those patents. Indeed, Netlist failed to provide any notice of the alleged infringement before filing the Texas Infringement Action. This conduct violates Netlist's contractual commitments for the reasons set forth in Count XII.

52. As noted above, Netlist has asserted several patents, including three patents related to the Patents-in-Suit, against Micron, a competitor of Samsung. The cases against Micron remain ongoing. On December 23, 2021, Micron filed IPR petitions on the '035 and '608 patents, which are related to the '506 patent at issue in the present suit. *See* IPR2022-00236 ('035 patent); IPR2022-00237 ('608 patent). On January 14, 2022, Micron filed an IPR petition on the '833 patent, which is related to the '918 patent at issue in the present suit. *See* IPR2022-00418.

C. Netlist Patents and Standard Essential Allegations

53. Netlist asserts that the Patents-in-Suit are essential to one or more of (a) JEDEC standards JESD79-4C, JESD82-31, JEDEC82-31A, and JESD82-32 ("the DDR4 Standards"), which were developed by the JEDEC JC-40 committee (JESD82-31 and JESD82-32), JC-40.4 committee (JESD82-31A), and JC-42.3C committee (JESD79-4C), and (b) JESD301.1, JESD82-511, and JESD79-5 ("the DDR5 Standards"), which were developed by the JEDEC JC-40.1 committee (JESD301.1), JC-40.4 committee (JESD82-511), and JC-42.3 committee (JESD79-5). Netlist further asserts that the Patents-in-Suit are essential to one or more of the standards encompassed by JESD21-C (together with the DDR4 Standards and the DDR5 Standards, "the JEDEC Standards").

54. Netlist contends that the '523, '595, and '218 patents are essential to one or more of JEDEC Standards. In its October 15, 2020 "Notice of Infringement" letter, Netlist asserts that it owns "over 100 patents and patent applications related to memory technologies," including

LRDIMM and RDIMM, and accuses Samsung of infringing these three patents. Furthermore, Netlist contended that each of these patents is essential to certain DDR4 Standards in previous litigation against SK hynix. *See Netlist, Inc. v. SK hynix Inc.*, No. 6:20-cv-00194 (W.D. Tex.), D.I. 1 ¶¶ 27, 37, D.I. 1-5 ('218 Claim Chart for DDR4 LRDIMM), D.I. 1-6 ('218 Claim Chart for DDR4 RDIMM), D.I. 1-10 ('595 Claim Chart for DDR4 LRDIMM), D.I. 1-11 ('595 Claim Chart for DDR4 RDIMM); *Netlist, Inc. v. SK hynix Inc.*, No. 6:20-cv-00525 (W.D. Tex.), D.I. 1 ¶ 27, D.I. 1-2 ('523 Claim Chart for DDR4 LRDIMM). In asserting the '523, '595, and '218 patents against SK hynix, Netlist's complaint included claim charts for each patent, in which Netlist mapped various claim limitations to the DDR4 Standards. *See id.*

55. Netlist contends that the '912 patent is essential to one or more of the DDR4 Standards. Specifically, in the Google Infringement Action, Netlist asserts that memory modules used by Google (which include Samsung's LRDIMM and RDIMM memory modules) infringe the '912 patent based on an implementation of the JESD79-4C standard.

56. In the Texas Infringement Action, Netlist alleges that "any Samsung DDR4 LRDIMM products" infringe the '506 and '339 patents. *See* Texas Infringement Action, D.I. 1, ¶¶ 37, 40, 53. Netlist relies on the implementation of the JESD82-32A standard in alleging infringement of the '506 patent, *id.* ¶ 46, and Netlist relies on the implementation of the JESD79-4C DDR4 SDRAM, JEDEC 21C, and JESD82-32A standards in alleging infringement of the '339 patent, *id.* ¶¶ 59–63.

57. Netlist further alleges that the '918 patent and the '019 application "provide for the effective operation of DDR5 memory modules," *id.* ¶ 33, and that "any Samsung DDR5 LRDIMM and DDR5 RDIMM products . . . that are JEDEC standard-compliant memory modules" infringe the '918 patent, *id.* ¶ 38. Netlist also accuses Samsung's DDR5 SODIMM and

UDIMM memory modules of infringing the ’918 patent. *Id.* ¶ 36. Netlist relies on the implementation of the JESD301-1, JESD82-511, and JESD79-5 standards in alleging infringement of the ’918 patent. *Id.* ¶¶ 72–75.

58. In the present action, SEC and SSI seek declarations that Samsung’s LRDIMM and RDIMM memory modules that comply with the DDR4 Standards or any standard requiring materially similar functionality (“Samsung DDR4 Memory Modules”); and Samsung’s SODIMM, UDIMM, and RDIMM memory modules that comply with the DDR5 Standards or any standard requiring materially similar functionality (“Samsung DDR5 Memory Modules” and together with the Samsung DDR4 Memory Modules, the “Samsung Memory Modules”), do not infringe the Patents-in-Suit. SEC and SSI also seek a declaration that certain of the Patents-in-Suit are unenforceable due to inequitable conduct and unclean hands.

59. If, as Netlist contends, the Patents-in-Suit are essential to any of the JEDEC Standards (which they are not), Netlist is obligated to license the patents on RAND terms. As discussed below, Netlist has failed to offer such a license to Samsung.

D. Samsung Does Not Infringe the Patents-in-Suit and Netlist’s Inequitable Conduct and Unclean Hands Renders the Claims Unenforceable

1. Overview of the ’523 Patent

60. The ’523 patent relates to a self-testing memory module for testing a plurality of memory devices mounted thereon. Ex. 1 (’523 Patent) at 5:4–27. An illustrative example is shown in FIG. 2, below.

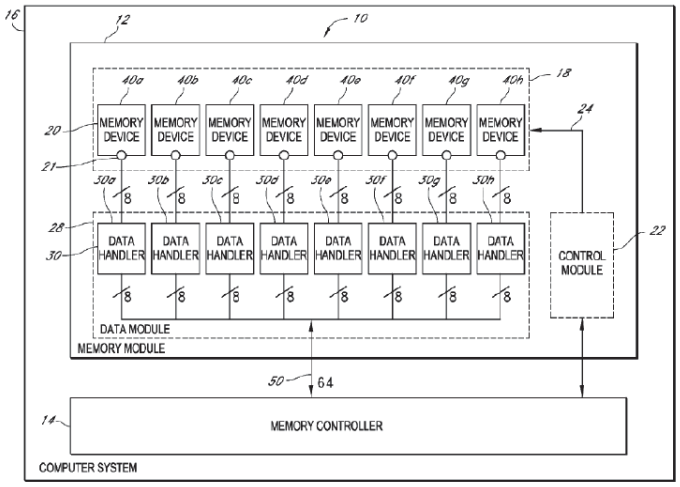


FIG. 2

61. As shown there, the memory module (12) includes a control module (22) that generates address and control signals for testing memory devices (20) and a data module (28) that includes a plurality of distributed data handlers (30) that are each located in proximity to a corresponding memory device (20) and act as a buffer between the memory device (20) and system memory controller (14). The data handlers (30) of the data module (28) generate test patterns to write to the memory devices (20) and compare test patterns read from the memory devices (20) to the written patterns to identify faults. *Id*. at 5:28–34, 9:22–42.

62. Figure 3 provides additional detail regarding the control module, data handlers and their components and interconnections:

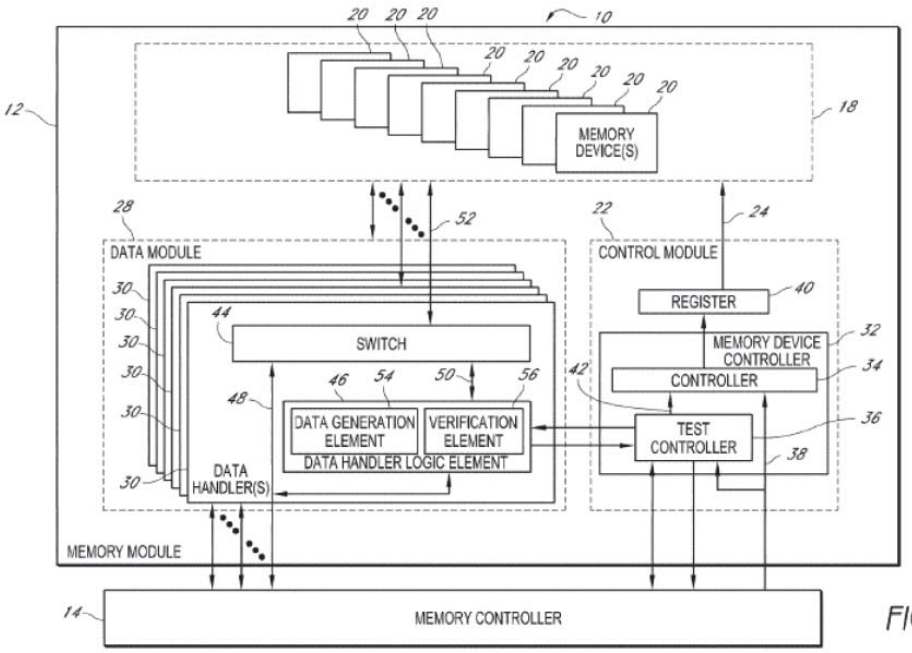


FIG. 3

63. Netlist appears to argue that the DB-to-DRAM Write Delay Training ("MWD Training"), as described in JESD82-32, practices one or more claims of the '523 patent. According to the standard, "for the DB-to-DRAM write delay training, the MDQ-MDQS delay adjustments are performed in the data buffer so that the DRAM receives the MDQ and MDQS signals with the optimal phase relationship." Ex. 10 (JESD82-32) at pg. 32. "[T]he data that is written to the DRAM comes from the data buffer's internal data control words that are written through the DDR4 register via the BCOM bus." *Id.* The Standard further explains:

> To perform DB-to-DRAM write training, the host will first enable the MDQ-MDQS write delay training mode in the Training Mode Control Word (BC0C) and it will also program the MPRs F5BC0x through F5BC3x and F6BC0x through F6BC3x. After that the host sends write commands to an arbitrary DRAM location without driving data on the host interface. The data for these write commands come from the DB MPRs.
>
> . . .
>
> To check whether the writes were successful, the host reads the data back from the same DRAM location and the data buffer performs a bit wise comparison with the data in the MPRs. If the data pattern is matched, the DQ pins are driven to "1" until the next comparison

> takes place or until the training mode is disabled. If the data pattern is not matched, the DQ pins are driven to "0."

Id.

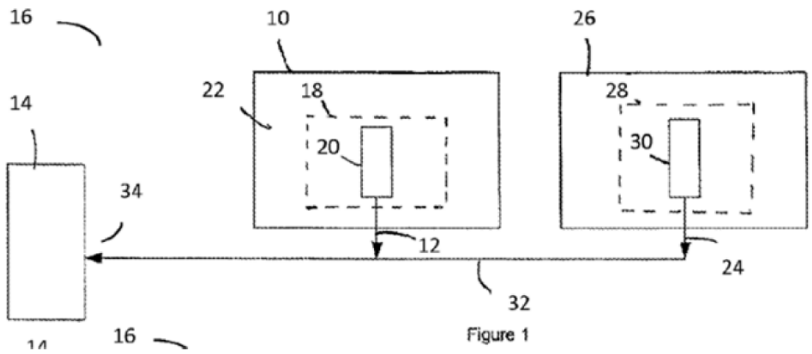
64. For at least the reasons explained in Count I, the Samsung Memory Modules do not infringe the claims of the '523 patent.

2. Overview of the '595 and '218 Patents

65. The '595 and '218 patents describe "a method of establishing a handshake mechanism based on notification signaling" that "can be implemented by adding a new interface (notifying) signal between the MCH [i.e., system memory controller] and the memory subsystem controller," Ex. 2 ('595 Patent) at 4:5–12, and this interface "can be an open drain signaling from the memory subsystem controller to the MCH." *Id*. at 4:12–16.

66. According to the '595 patent, "there [was] no existing method of handshaking between the MCH (*e.g.*, system memory controller) and a memory subsystem (*e.g.*, memory module) during initialization." *Id*. at 2:64–67. And "in conventional systems, the system memory controller does not monitor the error-out signal from the memory subsystem." *Id*. at 2:67-3:2. The '595 patent states that "[i]n a typical server (e.g., an Intel or AMD or other chipset based server), the lack of any handshaking between the MCH and the memory subsystem during the server initialization period has not been a serious issue since the MCH generally has complete control over the initialization procedure." *Id*. at 3:3–8.

67. Figure 1 shows a computer system including memory module 10, coupled to a memory controller 14 via "output 12," which is driven by notification circuit 20 of controller circuit 18.



Id. at 4:24–42, FIG. 1. Memory module 26 is also shown, and has essentially the same structure as module 10, having "output 24" driven by notification circuit 30 of controller circuit 28. *Id*. at 6:23–44.

68. In one specific example of handshaking, the interface between the memory controller (MCH) and memory subsystem controller is implemented using a technique called open drain signaling. *Id*. at 4:12–16, 9:47–53, FIGs. 2–3. Specifically, output 12 of module 10 and output 24 of module 26 are both tied to the same bus 32 using an open drain configured transistor. *Id.*

69. In that configuration, when starting an initialization procedure, each memory module will drive the gate of the transistor of its open drain output high, placing a logic level low (low impedance) signal on bus 32. When the initialization is complete, the memory module can drive the gate of the transistor, placing a logic level high (high impedance) signal on bus 32. However, because all of the outputs of multiple memory modules are tied to the same bus 32 in an open drain configuration, the state of bus 32 will remain logic level low (low impedance) until each memory module drives the gate of the transistor of its open drain output low, placing a logic level high (high impedance) on its output, which then allows "the bus 32 [to] be pulled high by the internal pull-up configuration 40 of the system memory controller 14." *Id*.

at 9:47–10:50. In this manner, the system memory controller may be provided a notification signal, notifying that the module is currently executing or has completed initialization. *Id*. at 9:47–10:50.

70. Netlist appears to allege that the Clock-to-CA training, as described in JESD82-31, practices one or more claims of the ’595 and ’218 patents. According to the standard, “[i]n Clock-to-CA training mode the DDR4RCD01 ORs all enabled Dn inputs <u>every other cycle</u> together and loops back the result to the ALERT_n output pin.” Ex. 11 (JESD82-31) at pg. 44 (emphasis in original). “In this mode, the DPAR input is sampled at the same time as the other Dn inputs,” and “[t]he ALERT_n latency relative to the DQn inputs is the same 3 cycles as in the normal parity mode.” *Id.*

71. For at least the reasons explained in Counts II and III, the Samsung Memory Modules do not infringe the claims of the ’595 and ’218 patents, respectively.

3. Overview of the ’912 Patent

72. The ’912 patent describes memory modules that purportedly have the capability of expanding the number of memory devices that can be accessed by a computer. The ’912 patent provides:

> The memory capacity of a memory module increases with the number of memory devices. The number of memory devices of a memory module can be increased by increasing the number of memory devices per rank or by increasing the number of ranks. For example, a memory module with four ranks has double the memory capacity of a memory module with two ranks and four times the memory capacity of a memory module with one rank.

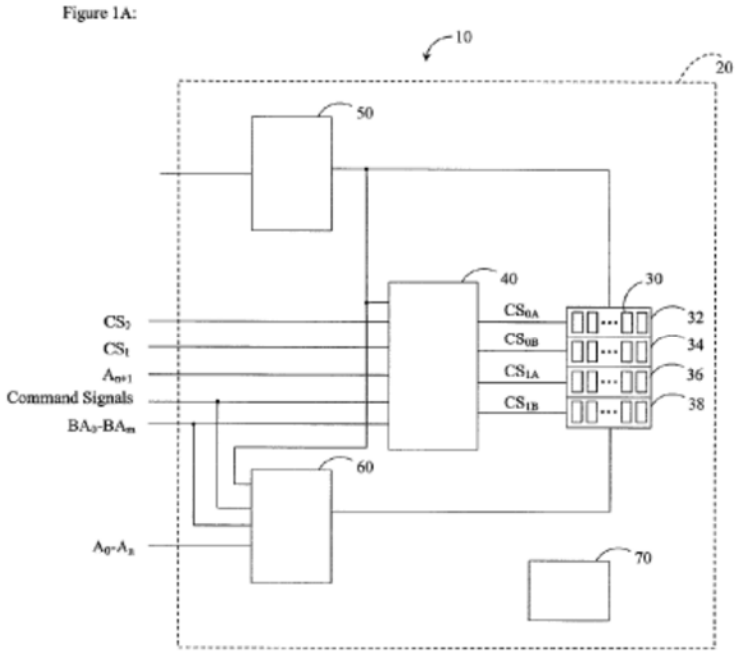
Ex. 4 (’912 Patent) at 2:23–30.

73. A given total amount of module memory (*e.g.*, 4GB) may be provided by using a small number of high-density memory devices or a large number of low-density memory devices. The ’912 patent states:

> Market pricing factors for DRAM devices are such that higher-density DRAM devices (e.g., 1Gb DRAM devices) are much more than twice the price of lower-density DRAM devices (e.g., 512 Mb DRAM devices). In other words, the price per bit ratio of the higher-density DRAM devices is greater than that of the lower density DRAM devices.

Id. at 4:59–64.

74. Figure 1A illustrates an exemplary memory module with four ranks of memory devices. The memory module 10 includes a logic element 40 and a register 60. *Id*. at 5:6–21. Input control signals, such as a row/column address signal (A_{n+1}), bank address signal (BA_o-BA_m), and chip select signals (CS_0 and CS_1), are received by logic element 40. *Id*. at 6:55–61. In response to the set of input control signals, the logic element 40 generates a set of output control signals, which includes address signals and a command signal. *Id*. at 6:61–63. Figure 1A shows a system configured for two ranks of memory per memory module (using chip select signals CS_0 and CS_1), even though the memory module 10 is arranged in four ranks of memory devices. *Id*. at 6:64–7:53. "Thus, in certain embodiments, even though the memory module 10 actually has the first number of ranks of memory devices 30, the memory module 10 simulates a virtual memory module by operating as having a second number of ranks of memory devices 30." *Id*. at 7:9–13.



Id., FIG. 1A.

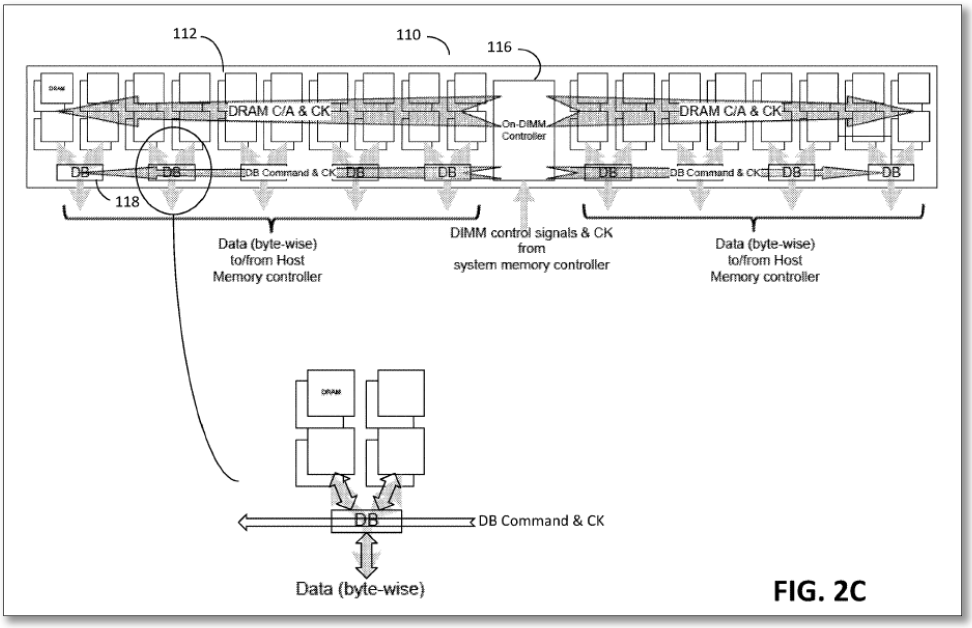
75. Netlist appears to allege that the Per DRAM Addressability ("PDA") mode, as described in JESD79-4C and JESD82-31A, practices certain limitations of claim 16 of the '912 patent. Netlist has alleged that the PDA mode allows programmability of a given device on a rank using the Mode Register Set ("MRS") function. In addition, Netlist has alleged that the Rank Multiplication Mode as described in JESD82-30 for LRDIMM DDR3 Memory Buffer (MB) Specification practices certain limitations of claims 1, 15, 28, 39, 77, 80, 82, 86, 88, and 90 of the '912 patent.

76. For at least the reasons explained in Count IV, the Samsung Memory Modules do not infringe the '912 patent.

4. Overview of the '506 Patent

77. The '506 patent relates to "multi-rank memory modules and methods of operation." Ex. 5 ('506 Patent) at 1:37–39. As shown in Figure 2C, below, "the control circuit 116

transmits registered C/A and clock signals to the memory devices 112, and transmits module control signals and a registered clock signal . . . to the isolation device 118." *Id.* at 8:22–26.



78. Figure 2C illustrates that data buffers 118 and their associated memory devices 112 are distributed across the memory module at varying distances from the module control device 116. "In some conventional memory systems, the memory controllers include leveling mechanisms for write and/or read operations to compensate for unbalanced wire lengths and memory device loading on the memory module." *Id.* at 2:28–36. The '506 patent alleges, however, that "such leveling mechanisms are also insufficient to insure [sic] proper timing of the control and/or data signals received and/or transmitted by the memory modules." *Id.* at 2:32–36.

79. The '506 patent describes "isolation devices" in which "each isolation device[] includes signal alignment circuits that determine, during a write operation, a time interval between a time when one or more module control signals are received from the module control signal 116 and a time when a write strobe or write data signal is received from the MCH 101." *Id.* at 10:7–21, 15:14–35. "This time interval is used during a subsequent read operation to time the

transmission of read data to the MCH 101, such that read data follows a read command by a read latency value associated with system 100." *Id.* at 10:11–21, 15:23–35.

80. In the Texas Infringement Action, Netlist alleges that Samsung's DDR4 LRDIMM memory modules directly infringe at least claim 1 of the '506 patent. *See* Texas Infringement Action, D.I. 1, ¶¶ 39–48. Netlist further alleges that Samsung indirectly infringes the '506 patent "by inducing infringement by others, such as Samsung's customers and end users" and by "contributing to direct infringement committed by others, such as customers and end users." *Id.* ¶¶ 49–50.

81. For at least the reasons explained in Count V, the Samsung DDR4 Memory Modules do not infringe the '506 patent.

5. Overview of the '339 Patent

82. The '339 patent relates to a "memory module" that purportedly solves the problem that prior art memory modules "require[d] that the memory system slow down operation speed if the memory subsystem is populated with more memory devices to provide high density memory cards." Ex. 6 ('339 patent) at 2:18–22. Figure 3A purports to illustrate a memory module of the '339 patent:

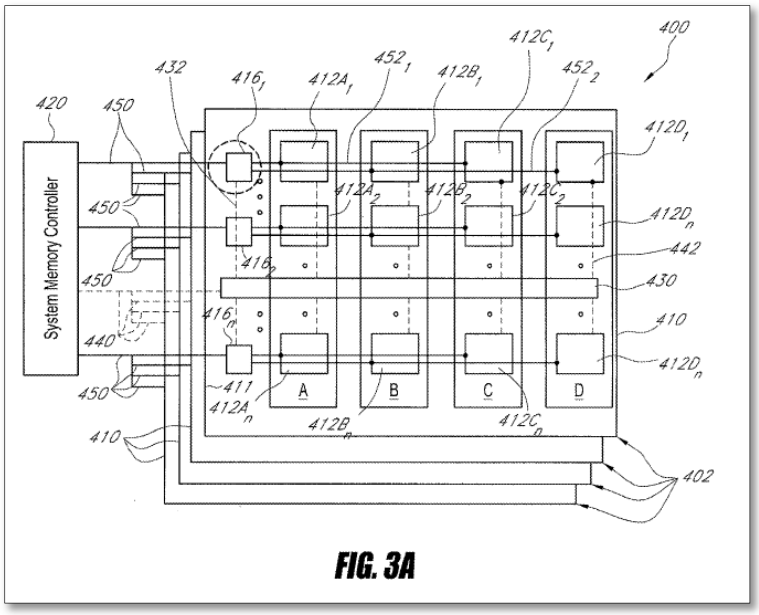


FIG. 3A

83. The memory modules (402) include a "control circuit" (430), a plurality of "memory devices" (412), and a plurality of "data transmission circuits" (416). *Id.* at 7:44–53. The claims of the '339 patent use the term "byte-wise buffer" to refer to the "data transmission circuit." *See, e.g.*, *id.* at 13:31–32 ("In certain embodiments, the data transmission circuit 416 comprises or functions as a byte-wise buffer."); *id.* at claim 1.

84. The data transmission circuit (416) is illustrated in Figure 5:

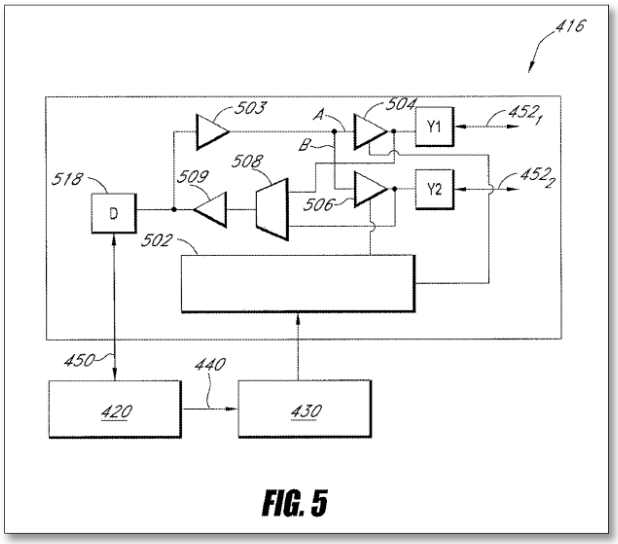


FIG. 5

85. The memory devices are arranged in a plurality of "ranks." *Id.* at 1:37–39. The data transmission circuit includes multiple data paths and includes logic to switch between different data paths depending on which rank of the memory is being accessed. *Id.* at 15:26–60. In Figure 5, the data transmission circuit has two data paths, which the '339 patent calls "path A and path B." *Id.* at 15:44–48. Path A connects the computer to ranks A and C of the memory module, while path B connects the computer to ranks B and D of the memory module. *Id.* at 15:48–58. During a write operation, for example, "the control logic circuitry 502 selects either path A or path B to direct the data." *Id.* at 16:7–11; *id.* at 17:53–18:24.

86. The '339 patent distinguishes the claimed memory modules from prior art memory modules that "combine[] chip-select signals with an address signal to increase the number of physically addressable memory spaces." *Id.* at 4:22–26. The '339 patent asserts that this approach has "several shortcomings," including that "a heavier load is presented to the output of the system controller and the outputs of the memory devices, resulting in a slower system." *Id.* at 4:27–31. According to the '339 patent, this approach also "results in higher power dissipation" and "introduc[es] uneven signal propagation delay between the data signal paths and control signal paths." *Id.* at 4:31–47.

87. In the Texas Infringement Action, Netlist alleges that Samsung's DDR4 LRDIMM memory modules directly infringe at least claim 1 of the '339 patent. *See* Texas Infringement Action, D.I. 1, ¶¶ 53–63. Netlist further alleges that Samsung indirectly infringes the '339 patent "by inducing infringement by others, such as Samsung's customers and end users" and by "contributing to direct infringement committed by others, such as customers and end users." *Id.* ¶¶ 64–65.

88. For at least the reasons explained in Count VI, the Samsung DDR4 Memory Modules do not infringe the ’339 patent.

6. Overview of the ’918 Patent

89. The ’918 patent relates to “Flash-DRAM Hybrid Memory Modules” that supply power to the memory system from a system power supply when the memory module is in the first state, and from an on-board power supply when the memory module is in a second state. Ex. 7 (’918 patent) at 25:54–58. Figure 12 illustrates a memory module disclosed in the ’918 patent:

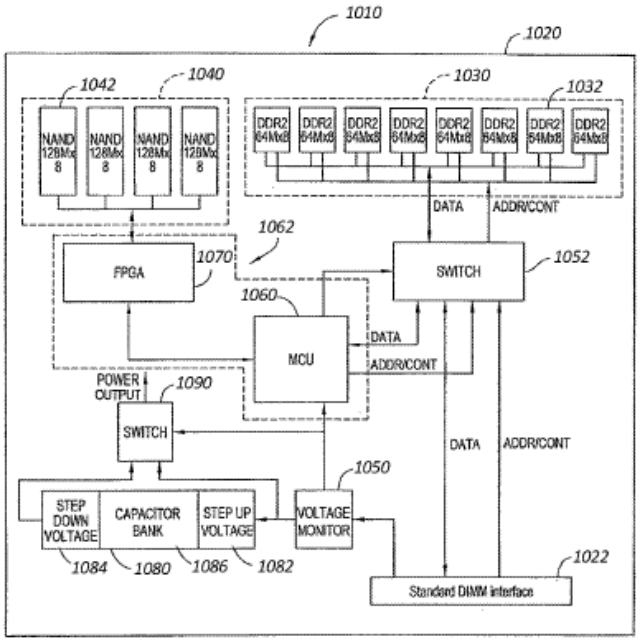


FIG. 12

90. The memory module (1010) includes a volatile memory subsystem (1030), a non-volatile memory subsystem (1040), and a controller (1062) coupled to the non-volatile memory subsystem. *Id.* at 21:14–20. The on-board power supply (1080) can be implemented as a power module (1100) that provides multiple voltages to the circuitry on the memory module. Figure 16 illustrates the power module disclosed in the ’918 patent:

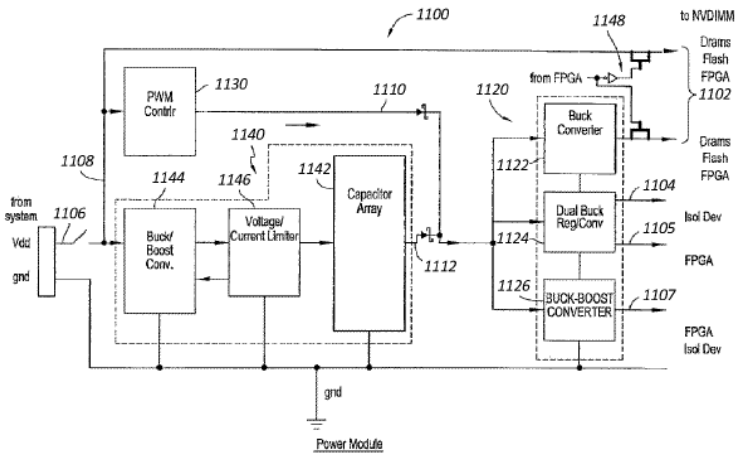


FIG. 16

91. The ’918 patent states “[t]he power module has a conversion element (1120) that can comprise at least one or more buck converters (1122, 1124) and at least one buck-boost converter (1126).” *Id.* at 29:18–19.

92. In the Texas Infringement Action, Netlist alleges that the Samsung DDR5 Memory Modules, as well as DDR5 LRDIMM memory modules, directly infringe at least one claim of the ’918 patent. *See* Texas Infringement Action, D.I. 1, ¶¶ 68–75. Netlist further alleges that Samsung indirectly infringes the ’918 patent “by inducing infringement by others, such as Samsung’s customers and end users” and by “contributing to direct infringement committed by others, such as customers and end users.” *Id.* ¶¶ 76–77.

93. For at least the reasons explained in Count VII, the Samsung DDR5 Memory Modules do not infringe the ’918 patent. Samsung does not manufacture or supply DDR5 LRDIMM memory modules.

7. Certain of the Patents-in-Suit Are Unenforceable

94. Certain of the Patents-in-Suit also are unenforceable due to inequitable conduct and unclean hands.

95. As fully set forth in Counts VIII and IX, individuals substantively involved in the prosecution of the ’523, ’595, and ’218 patents knew about material and non-cumulative

prior art by virtue of their participation in JEDEC standards meetings, the citation of the prior art against patents in the same family, and/or IPR petitions filed by SK hynix. On information and belief, these individuals specifically intended to deceive the Patent Office into believing that the claims of the ’523, ’595, and ’218 patents were patentable by withholding the relevant art from the examiner during prosecution of the patents.

96. As fully set forth in Count X, individuals substantively involved in the reexamination of the ’912 patent made false and misleading statements to the Patent Office and the Federal Circuit that were material to the patentability of the amended claims. On information and belief, these individuals specifically intended to deceive the Patent Office and the Federal Circuit into believing that the amendment of certain claims in the ’912 patent were “narrowing” in scope, thereby distinguishing those claims from the prior art. On information and belief, these individuals misrepresented the intended effect of the amendments in order to secure allowance of the amended claims, knowing that Netlist would later adopt the position in litigation that the amendments were in fact not “narrowing” at all, but rather recited “inherent functions” that were already required by the original claims.

97. As fully set forth in Count XI, individuals substantively involved in the prosecution of the ’506 patent knew about material and non-cumulative prior art by virtue of their participation in JEDEC standards meetings. On information and belief, these individuals specifically intended to deceive the Patent Office into believing that the claims of the ’506 patent were patentable by withholding the relevant art from the examiner during prosecution of the patent.

E. Netlist Has Breached Contractual Obligations Owed to Samsung

1. JEDEC and Semiconductor Memory Standards

98. JEDEC is an independent, non-profit semiconductor engineering trade association and standardization body based in the United States. Over 300 companies in the

computer and electronics industries are currently members of JEDEC, including Samsung and Netlist.

99. JEDEC has become the global leader in developing open standards and publications for a broad range of semiconductor technologies, including memory products. As relevant here, JEDEC develops standards for semiconductor memory chips and modules, including standards implemented by Samsung's products.

100. JEDEC's semiconductor memory standards enable interoperability, *i.e.*, the ability of memory products made by different manufacturers to work together with computer and electronic devices made by others. JEDEC standards are widely implemented, and, for many types of semiconductor memory products, it is imperative that they comply with JEDEC standards in order to be commercially viable.

101. Member companies participate in JEDEC's standard-setting process through over 50 committees and subcommittees that address various technological areas. Through a collaborative process, members contribute to and vote on technical proposals for incorporation into JEDEC standards. Upon committee and Board approval, new standards are promulgated and made available to the public.

102. In some cases, JEDEC members own patents covering the technology they or others seek to have included in a JEDEC standard. A patent that includes a claim or claims that would necessarily be infringed by the use, sale, offer for sale, or disposition of a portion of a product in order to be compliant with an industry standard is referred to as a "standard essential patent" or an "SEP."

103. Each owner of an SEP can, unless restrained, demand and obtain exorbitant royalties for the use of its patents, far in excess of the value, if any, that the patented technology

would command had it not been incorporated into a standard. If unwilling to pay such excessive royalties, firms wishing to implement the standard face the risk of being foreclosed from using any portion of the standard, including unpatented and public domain technologies. This threat of foreclosure, if left unchecked, puts a manufacturer's investment in developing standard-compliant products at risk and, in effect, permits the possibility that the SEP holder may capture up to the value of the standard as a whole for each unique implementer, rather than the true value of its specific contribution to the standard, independent of the incorporation of the technology into the standard. The exploitation of SEPs to extract unreasonable or discriminatory royalties is referred to as patent "hold-up."

104. The problem of "hold-up" is exacerbated in the context of standards, like those at issue here, as to which there are large numbers of SEPs and many different firms that claim to hold SEPs. The problem is likewise compounded when the products at issue, like those at issue here, may be required to implement multiple standards. The resulting problem of excessive aggregate royalties is referred to as "royalty stacking."

105. In order to mitigate these risks, JEDEC—like many other standard-setting organizations—has adopted a Patent Policy that seeks to ensure that owners of SEPs license those patents to manufacturers of standard-compliant products on RAND terms and conditions. Every firm that is a member of a JEDEC committee or a participant in a JEDEC committee meeting, including Netlist, agrees to abide by the JEDEC Patent Policy.

> *All Committee Members, as a condition of committee membership or committee Participation, agree to abide by JEDEC rules and procedures, including this JEDEC patent policy ("Patent Policy").*

Ex. 12 (JEDEC Manual No. 21T) § 8.2.2.1.

106. Pursuant to the JEDEC Patent Policy, as a condition of committee membership or participation, all JEDEC committee members agree to disclose "Potentially Essential Patents" relevant to the work of the committee:

> *All Committee Members must Disclose Potentially Essential Patents, known to their Representative(s) to be Potentially Essential Patents that are owned or controlled by that Committee Member . . . .*

Id. § 8.2.3.

107. The requirement to disclose "Potentially Essential Patents" extends to disclosing pending patent applications. *Id.* § 8.2.1.

108. JEDEC committee members also agree to license "Essential Patent Claims" on RAND terms and conditions:

> *All Committee Members, as a condition of committee membership or committee Participation, agree to Disclose Potentially Essential Patents, as set forth more fully in 8.2.3, and to offer to license their Essential Patent Claims to all Potential Licensees on RAND terms and conditions, if and as consistent with 8.2.3 and 8.2.4.*

Id. § 8.2.2.1.

109. JEDEC committee members also agree to license on RAND terms any "Essential Patent Claims" included in their patent applications:

> For any Essential Patent Claims held or controlled by the entity, *pending[,] or anticipated to be filed*, which are or may be required to implement a Standard that may result from the JEDEC Standard Activity, the entity hereby makes one of the following commitments: . . . A license will be offered . . . under reasonable terms and conditions that are free of any unfair discrimination.

Id. § 8.2.5 (emphasis added).

110. The JEDEC Patent Policy defines "Potentially Essential Patent" as a patent that is reasonably believed to contain one or more Essential Patent Claims. *Id*. § 8.2.1. "Essential Patent Claim" is further defined as those "Patent claims the use of which would necessarily be

infringed by the use, sale, offer for sale or other disposition of a portion of a product in order to be compliant with the required portions of a final approved JEDEC standard." *Id.*

111. The JEDEC Patent Policy provides that the disclosure of Potentially Essential Patents "shall be made as early as reasonably possible" and documented by submission to JEDEC of either a "License Assurance/Disclosure Form" or a "Notice of Refusal." *Id.* § 8.2.3.

112. A License Assurance/Disclosure Form (also known as a "Letter of Assurance" or "LOA") states that the committee member commits to license its SEPs to all potential licensees on RAND terms. On the contrary, a Notice of Refusal states that the member is not "willing to offer to license Essential Patent Claims . . . on RAND terms to all Potential Licensees." *Id.* § 8.2.3.1. In order to be effective, any such LOA or Notice of Refusal must be delivered to the JEDEC Legal Department within thirty (30) calendar days of a draft specification's completion. *Id.*

113. Member companies who disclose and agree to license their patents on RAND terms do so via the aforementioned "LOA" identifying the relevant JEDEC standard(s) and making one of the two following commitments specified by the JEDEC Patent Policy:

> *For any Essential Patent Claims held or controlled by the entity, pending or anticipated to be filed, which are or may be required to implement a Standard that may result from the JEDEC Standard Activity, the entity hereby makes one of the following commitments:*
>
> *(i) A license will be offered, without compensation, under reasonable terms and conditions that are free of any unfair discrimination to applicants desiring to utilize the license for the purpose of implementing the JEDEC Standard, subject to the terms and conditions in 8.2.4; or*
>
> *(ii) A license will be offered, to applicants desiring to utilize the license for the purpose of implementing the JEDEC Standard under reasonable terms and conditions that are free of any unfair discrimination, subject to the terms and conditions in 8.2.4.*

Id. § 8.2.5.

114. According to JEDEC's Patent Policy, disclosures and commitments with respect to one patent are deemed to include all patents claiming priority to the same filing. *Id*. § 8.2.1. Committee members are therefore obligated to license on RAND terms later-issuing SEPs that claim priority to patents disclosed to JEDEC.

115. If a committee member who owns or controls patents essential (or potentially essential) to JEDEC standards does not disclose and agree to license them before the ballot closes, or notify the committee of an intention not to license through a "Notice of Refusal," the committee member will be deemed to have agreed to offer licenses on RAND terms:

> *If a Committee Member, at its discretion, elects not to submit a License Assurance/Disclosure Form (see Annex A.3) at or before the time the ballot closes and does not otherwise provide notice of an unwillingness to license in accordance with 8.2.3.1, the Committee Member and its Affiliates will be deemed to have agreed to offer to grant licenses on RAND terms and conditions for all of its Essential Patent Claims of the balloted Standard, if and as consistent with 8.2.4.*

Id. § 8.2.5.

116. The JEDEC Patent Policy provides that it is to be interpreted and governed under the laws of the State of New York. *Id*. § 8.2.10. Although the JEDEC Manual 21 has been updated and amended from time to time, upon information and belief, all of the relevant provisions of the JEDEC Patent Policy have been materially the same at all times relevant hereto.

2. Netlist's RAND Commitments

117. Netlist alleges that it owns over 100 patents and patent applications related to memory technologies.

118. Netlist is also a member of JEDEC and has joined a number of JEDEC technical committees over time. After years of membership in JEDEC, Netlist withdrew from

membership in JC-40, JC-42, and JC-45 in 2015, after submitting notices of refusal for many of its patents. In May 2018, Netlist requested from the JEDEC board of directors that Netlist be reinstated in those committees. The JEDEC board of directors approved the request on the condition that Netlist would agree to be bound by the JEDEC Patent Policy regarding work conducted in JC-40, JC-42, and JC-45 during the time Netlist had not participated in the committees, since and including February 27, 2015. Netlist agreed in writing to the JEDEC board of directors' terms, and JEDEC reinstated Netlist on August 14, 2018, retroactive to February 27, 2015.

119. Upon information and belief, therefore, at the time that the JEDEC Standards were drafted and approved by JEDEC, Netlist was a member, attended the meetings, and/or was deemed a member of the JC-40, JC-42, and JC-45 committees that developed those standards.

120. To date, and on information and belief, Netlist has disclosed that at least 42 of its patents are essential or potentially essential to JEDEC standards.

121. Netlist is obligated to license the '523 patent on RAND terms to implementers of certain DDR4 Standards, to the extent it is essential to those standards. In fact, Netlist committed to license the '523 patent on RAND terms to implementers of certain DDR4 Standards. Upon information and belief, Netlist submitted a Letter of Assurance for U.S. Patent No. 8,001,434 (the "'434 patent") on April 7, 2016, related to JEDEC committee JC-40 and DDR4 LRDIMM components. Ex. 13 ('434 LOA). The '523 patent is a continuation of the '434 patent. Therefore, under the JEDEC Patent Policy, the commitments in the '434 Letter of Assurance extend to the '523 patent. Ex. 12 (JEDEC Manual No. 21T) § 8.2.1.

122. Netlist is obligated to license the ’595 and ’218 patents on RAND terms to implementers of certain DDR4 Standards, to the extent they are essential to those standards. In fact, Netlist committed to license the ’595 and ’218 patents on RAND terms to implementers of certain DDR4 Standards. Upon information and belief, Netlist submitted a Letter of Assurance for U.S. Patent No. 8,489,837 (the “’837 patent”) on April 7, 2016, related to JEDEC committee JC-40 and DDR4 LRDIMM and RDIMM components. Ex. 14 (’837 LOA). The ’595 and ’218 patents are continuations of the ’837 patent. Therefore, under the JEDEC Patent Policy, the commitments in the ’837 Letter of Assurance extend to the ’595 and ’218 patents. Ex. 12 (JEDEC Manual No. 21T) § 8.2.1.

123. Netlist is obligated to license the ’912 patent on RAND terms to implementers of certain DDR4 Standards, to the extent it is essential to those standards. Upon information and belief, Netlist wrote a letter to JEDEC on April 1, 2010, disclosing the ’912 patent in connection with the JC-40 and JC-42 committees. Ex. 15 (’912 Letter). Netlist submitted a Letter of Assurance on November 22, 2010 related to DDR2 and DDR3 technology, Ex. 16 (’912 LOA), but withdrew that commitment on December 6, 2010, when Netlist submitted a Notice of Refusal, Ex. 17 (’912 Refusal). Netlist withdrew its Notice of Refusal for the ’912 patent nine months later, on September 7, 2011. Ex. 18 (’912 LOA II).

124. Upon information and belief, Netlist never specifically disclosed the ’912 patent in connection with any of the DDR4 Standards. Netlist has alleged that a DDR4 memory module operating in PDA mode, in compliance with certain DDR4 Standards, infringes claim 16 of the ’912 patent. Netlist also acknowledges that PDA mode was not part of the earlier DDR standards and was introduced in connection with the DDR4 Standards. Upon information and belief, despite the differences between DDR4 and earlier DDR standards, Netlist never disclosed

the ’912 patent to JEDEC with respect to the standards that define PDA mode. Netlist only disclosed related patents—U.S. Patent Nos. 8,081,535 and 8,081,537—to the JC-40 and JC-42 committees in relation to DDR4. Ex. 19 (’535 and ’537 LOAs).

125. Moreover, the DDR4 standards were first published in 2014, so Netlist had seven years in which to notify the industry that the ’912 patent was allegedly essential to certain DDR4 Standards. Although, on information and belief, Netlist neglected to specifically disclose the ’912 patent in connection with the DDR4 Standards defining PDA mode throughout this time period, Netlist amended its infringement contentions in 2021 in the Google Infringement Action to assert that claim 16 of the ’912 patent is essential to those standards.

126. Notwithstanding Netlist’s failure to disclose the ’912 patent in connection with DDR4, Netlist is obligated to license the ’912 patent to implementers of the DDR4 Standards, to the extent it is essential to those standards, on the basis of the JEDEC Patent Policy and Netlist’s participation in the JEDEC committees that developed those standards. Ex. 12 (JEDEC Manual No. 21T) § 8.2.5.

127. Netlist is obligated to license the ’506 patent on RAND terms to implementers of certain DDR4 Standards, to the extent it is essential to those standards. In fact, Netlist committed to license the ’506 patent on RAND terms to implementers of certain DDR4 Standards. Upon information and belief, Netlist submitted a Letter of Assurance for U.S. Patent No. 9,128,632 (the “’632 patent”) on April 7, 2016, related to JEDEC committees JC-40 and JC-45 and DDR4 LRDIMM components. Ex. 20 (’632 LOA). The ’506 patent is a continuation of the ’632 patent. Therefore, under the JEDEC Patent Policy, the commitments in the ’632 Letter of Assurance extend to the ’506 patent. Ex. 12 (JEDEC Manual No. 21T) § 8.2.1.

128. Netlist is obligated to license the ’339 patent on RAND terms to implementers of certain DDR4 Standards, to the extent it is essential to those standards. In fact, Netlist committed to license the ’339 patent on RAND terms to implementers of certain DDR4 Standards. Upon information and belief, Netlist submitted a Letter of Assurance related to JEDEC committees JC-42.3 and JC-45 and LRDIMM on November 22, 2010, for U.S. Patent Application No. 12/761,179, which issued as U.S. Patent No. 8,516,185 (the “’185 patent”), Ex. 21 (12/761,179 LOA), and U.S. Patent Application No. 12/504,131, Ex. 22 (12/504,131 LOA), which issued as U.S. Patent No. 8,417,870 (the “’870 patent”). The ’339 patent is a continuation of the ’185 and ’870 patents.

129. Netlist also disclosed U.S. Patent Application No. 12/761,179, Ex. 23 (12/761,179 LOA II), and U.S. Patent Application No. 12/504,131, Ex. 24 (12/504,131 LOA II), to JEDEC in relation to JC-40 on September 7, 2011—after submitting a notice of refusal for a number of Netlist patents on December 6, 2010. Therefore, under the JEDEC Patent Policy, Netlist’s RAND commitments for those patent applications extend to the patents issuing therefrom and the related ’339 patent. Ex. 12 (JEDEC Manual No. 21T) § 8.2.1.

130. Netlist is obligated to license the ’918 patent on RAND terms to implementers of certain DDR5 Standards, to the extent it is essential to those standards. Upon information and belief, Netlist never specifically disclosed the ’918 patent in connection with any of the DDR5 Standards. Netlist only disclosed patents related to the ’918 patent—specifically, U.S. Patent No. 8,874,831 (the “’831 patent”) and U.S. Patent No. 8,301,833 (the “’833 patent”)—to JEDEC committees, and Netlist only did so in relation to DDR4, not DDR5. Ex. 25 (’831 LOA); Ex. 26 (’833 LOA).

131. In fact, Netlist did not file the patent application from which the ’918 patent issued until December 30, 2020—several months after the finalization of at least certain DDR5 Standards (including JESD301-1 and JESD79-5). Although Netlist was aware of the standards—and was actively pursuing patent claims that it contends are essential to the standards—Netlist never disclosed to JEDEC the patent application, or the ’918 patent once it issued, as potentially essential to the DDR5 Standards.

132. Notwithstanding Netlist’s failure to disclose the ’918 patent (or the application from which it issued) in connection with DDR5, Netlist is obligated to license the ’918 patent to implementers of the DDR5 Standards, to the extent it is essential to those standards, on the basis of the JEDEC Patent Policy and Netlist’s participation in the JEDEC committees that developed those standards. Ex. 12 (JEDEC Manual No. 21T) § 8.2.5.

133. Netlist is also obligated to license the ’019 application (and any patent issuing therefrom) on RAND terms to implementers of certain DDR5 Standards, to the extent it is essential to those standards. Upon information and belief, Netlist never specifically disclosed the ’019 application in connection with any of the DDR5 Standards. Netlist only disclosed patents related to the ’019 application—specifically, the ’831 and ’833 patents—to JEDEC committees, and Netlist only did so in relation to DDR4, not DDR5.

134. In fact, Netlist did not file the ’019 application until May 24, 2021—several months after the finalization of at least certain DDR5 Standards (including JESD301-1 and JESD79-5). Although Netlist was aware of the standards—and was actively pursuing patent claims that it apparently contends are essential to the standards—Netlist never disclosed to JEDEC the ’019 application as potentially essential to the DDR5 Standards.

135. Notwithstanding Netlist's failure to disclose the '019 application in connection with DDR5, Netlist is obligated to license the '019 application (and any patent issuing therefrom) to implementers of the DDR5 Standards, to the extent it is essential to those standards, on the basis of the JEDEC Patent Policy and Netlist's participation in the JEDEC committees that developed those standards. Ex. 12 (JEDEC Manual No. 21T) § 8.2.5.

136. The commitments that Netlist has made to license its SEPs on RAND terms constitute binding contractual obligations that may be enforced by firms seeking to implement the JEDEC standards, such as Samsung.

3. Netlist's Failure to Comply with Its RAND Obligations

137. Although Netlist accepted the benefits of its membership in JEDEC in order to induce JEDEC to incorporate technologies over which Netlist claims to have patents into JEDEC standards, Netlist has failed to fulfill its corresponding contractual commitments. Despite voluntarily undertaking the obligation to license its alleged SEPs on RAND terms, Netlist has made licensing demands of Samsung that violate its RAND commitment.

138. For instance, by email dated February 2, 2021, Netlist demanded that Samsung enter a second license to patents that Samsung previously licensed from Netlist, coupled with a demand to "be made whole" for any alleged breach under the Agreement. Specifically, Netlist stated that "Samsung will require a new license to our patent portfolio" and requested "[d]amages that Netlist has incurred as a result of Samsung's material decrease of product supply to Netlist following Q1 2017 and how Netlist might be made whole." Further, in the Google Infringement Action, Netlist has brought suit against Google based on Google's use of Samsung DDR4 Memory Modules, and Netlist seeks to enjoin Google from using those modules. Such an injunction request violates Netlist's commitment to license its alleged SEPs on RAND terms and conditions.

139. Moreover, although the infringement claims in the Texas Infringement Action are based on the alleged practice of certain JEDEC Standards, Netlist filed the lawsuit without notifying Samsung of the asserted patents, describing the alleged infringement, or making any good-faith RAND offer.

140. Accordingly, and as discussed elsewhere herein, Netlist has breached its obligations under the JEDEC Patent Policy.

COUNT I
(Declaration of Non-Infringement of the '523 Patent)

141. Samsung restates and incorporates by reference the preceding paragraphs as if fully set forth herein.

142. The Patent Office issued the '523 patent, titled "Multi-Mode Memory Module," on February 26, 2019. On information and belief, Netlist claims to own all rights, title, and interest in the '523 patent. A true and correct copy of the '523 patent is attached hereto as Exhibit 1.

143. The '523 patent has two independent claims: 1 and 19. For example, claim 1 reads as follows:

Element	Claim Language
preamble	A memory module accessible in a computer system by a system memory controller via a system memory bus, comprising:
(a)	memory devices mounted on a circuit board, the memory devices having address and control ports and data ports;
(b)	a data module mounted on the circuit board and coupled between the data ports of the memory devices and the system memory bus, the data module including data handler logic elements; and
(c)	a control module mounted on the circuit board and coupled to the data module, the address and control ports of the memory devices, and the system memory bus; and

Element	Claim Language
(d)	wherein the memory module is operable in any of a plurality of modes including a first mode and a second mode;
(e)	wherein the control module in the first mode is configured to receive system address and control signals from the system memory controller and to output first memory address and control signals to the memory devices according to the system address and control signals, and the data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller, the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals; and
(f)	wherein the control module in the second mode is configured to output second memory address and control signals to the address and control ports of the memory devices, and the data module in the second mode is configured to isolate the memory devices from being accessed by the system memory controller and to transmit one or more second data signals including data patterns provided by the data handler logic elements to the data ports of the memory devices according to one or more commands output from the control module, and wherein at least a portion of the memory devices are configured to receive the one or more second data signals according to the second memory address and control signals from the control module.

144. Netlist has alleged and continues to allege that Samsung infringes one or more claims of the ’523 patent.

145. Samsung has not directly or indirectly infringed any claim of the ’523 patent, either literally or under the doctrine of equivalents, at least because the Samsung DDR4 Memory Modules do not employ, incorporate, or otherwise make use of all of the limitations of the claims of the ’523 patent.

146. For example, claim 1 requires a “data module” that includes “data handler logic elements.” Similarly, claim 19 requires “data handlers” that include a “data handler logic element.” Thus, all of the claims of the ’523 patent require a “data module” or a “data handler” that includes a “data handler logic element.” Netlist appears to allege that LRDIMM data buffers are “data modules” or “data handlers.” Samsung’s LRDIMM products do not include any accused

data buffers. The accused LRDIMM data buffers are not "data modules" or "data handlers" that include a "data handler logic element" at least because they do not include circuitry for generating data as required by the claims of the '523 patent.

147. As another example, claims 1 and 19 require "a first mode and a second mode." Netlist appears to allege that the MWD Training in Samsung's LRDIMM products is the alleged "second mode." However, the accused MWD Training is a training and not a "second mode" as required by the claims.

148. The Samsung DDR4 Memory Modules do not infringe any of claims 2–18 and 20–34 at least because these claims depend directly or indirectly from claims 1 or 19.

149. For at least the same reasons described above, Samsung DDR5 Memory Modules do not infringe any claims of the '523 patent. In addition, Samsung, its customers, and its end users are not liable for infringement of the '523 patent for any Samsung Memory Modules made, imported, or sold under license from Netlist.

150. A substantial, immediate, and real controversy exists between Samsung and Netlist regarding whether Samsung or its customers or end users infringe the '523 patent by making, using, selling, and/or offering for sale the Samsung Memory Modules in the United States, or by importing the Samsung Memory Modules into the United States. A judicial declaration is necessary to determine the parties' respective rights regarding the '523 patent.

151. Samsung seeks a judgment declaring that Samsung and its customers and end-users do not infringe the '523 patent, either literally or under the doctrine of equivalents, by making, using, selling, and/or offering for sale the Samsung Memory Modules in the United States, or by importing the Samsung Memory Modules into the United States, either directly under 35 U.S.C. § 271(a) or indirectly under 35 U.S.C. § 271(b)–(c).

COUNT II
(Declaration of Non-Infringement of the '595 Patent)

152. Samsung restates and incorporates by reference the preceding paragraphs as if fully set forth herein.

153. The Patent Office issued the '595 patent, titled "Memory Module Having An Open-Drain Output Pin For Parity Error In A First Mode And For Training Sequences In A Second Mode," on November 12, 2019. On information and belief, Netlist claims to own all rights, title, and interest in the '595 patent. A true and correct copy of the '595 patent is attached hereto as Exhibit 2.

154. The '595 patent has four independent claims: 1, 10, 17, and 21. For example, claim 1 reads as follows:

Element	Claim Language
preamble	A memory module operable with a memory controller of a host system, comprising:
(a)	a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;
(b)	dynamic random access memory elements on the printed circuit board;
(c)	a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection; and
(d)	wherein the memory module is configurable to operate in any of at least a first mode and a second mode;
(e)	wherein the memory module in the first mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations, and wherein the

Element	Claim Language
	memory module in the second mode is configurable to perform operations related to one or more training sequences;
(f)	wherein the module controller is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the first mode;
(g)	wherein the module controller in the second mode is further configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection to a first state or to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.

155. Netlist has alleged and continues to allege that Samsung infringes one or more claims of the ’595 patent.

156. Samsung has not directly or indirectly infringed any claim of the ’595 patent, either literally or under the doctrine of equivalents, at least because the Samsung DDR4 Memory Modules do not employ, incorporate, or otherwise make use of all of the limitations of the claims of the ’595 patent.

157. For example, claim 1 requires “the memory module in the second mode is configurable to perform operations related to one or more training sequences” and “wherein the module controller in the second mode is further configurable to provide information related to the one or more training sequences.” Similarly, claim 10 requires “wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences” and “wherein the module controller in the second mode is further configurable to output to the memory controller open-drain signals related to the one or more training sequences.” Netlist appears to

allege that the Clock-to-CA training as described in the JEDEC standard is the alleged "second mode." However, any configuration of the alleged "memory module" or the alleged "memory controller" occurs prior to entering Clock-to-CA training and no further configuration can occur during the training. Thus, the accused Samsung DDR4 Memory Modules do not meet the limitations of at least claims 1–16.

158. As another example, claim 1 requires "wherein the module controller in the second mode is further configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection to a first state or to a second state." Similarly, claim 10 requires "wherein the module controller in the second mode is further configurable to output to the memory controller open-drain signals related to the one or more training sequences via the open drain output and the error edge connection while the memory module is in the second mode." Claim 21 requires "wherein the module controller is configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection from one of the first state and the second state to the other one of the first state and the second state." Netlist appears to argue that the signal on the ALERT_n output pin meets these limitations during Clock-to-CA training. The signal on the ALERT_n output pin is not "information related to the one or more training sequences" or "open-drain signals related to the one or more training sequences" as required by the claims. The signal does not indicate the status of any training, and is polled by the system memory controller during Clock-to-CA training. Thus, the accused signal on the ALERT_n output pin does not satisfy the requirements of claims 1–16 and 21–24.

159. The Samsung DDR4 Memory Modules do not infringe any of claims 2–9, 11–16, 18–20, and 22–24 at least because these claims depend directly or indirectly from claims 1, 10, or 21.

160. For at least the same reasons described above, Samsung DDR5 Memory Modules do not infringe any claims of the ’595 patent. In addition, Samsung, its customers, and its end users are not liable for infringement of the ’595 patent for any Samsung Memory Modules made, imported, or sold under license from Netlist.

161. A substantial, immediate, and real controversy exists between Samsung and Netlist regarding whether Samsung or its customers or end users infringe the ’595 patent by making, using, selling, and/or offering for sale the Samsung Memory Modules in the United States, or by importing the Samsung Memory Modules into the United States. A judicial declaration is necessary to determine the parties’ respective rights regarding the ’595 patent.

162. Samsung seeks a judgment declaring that Samsung and its customers and end-users do not infringe the ’595 patent, either literally or under the doctrine of equivalents, by making, using, selling, and/or offering for sale the Samsung Memory Modules in the United States, or by importing the Samsung Memory Modules into the United States, either directly under 35 U.S.C. § 271(a) or indirectly under 35 U.S.C. § 271(b)–(c).

COUNT III
(Declaration of Non-Infringement of the ’218 Patent)

163. Samsung restates and incorporates by reference the preceding paragraphs as if fully set forth herein.

164. The Patent Office issued the ’218 patent, titled “Memory Module And Methods For Handshaking With A Memory Controller,” on January 2, 2018. On information and

belief, Netlist claims to own all rights, title, and interest in the ’218 patent. A true and correct copy of the ’218 patent is attached hereto as Exhibit 3.

165. The ’218 patent has three independent claims: 1, 9, and 15. For example, claim 1 reads as follows:

Element	**Claim Language**
preamble	A memory module operable with a memory controller of a host system, comprising:
(a)	a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;
(b)	dynamic random access memory elements on the printed circuit board;
(c)	a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection; and
(d)	wherein the memory module is operable in at least a first mode and a second mode, wherein the memory module in the first mode is configured to be trained with one or more training sequences; wherein the memory module in the second mode is configured to perform one or more memory read or write operations not associated with the one or more training sequences by communicating data signals via the first edge connections in response to address and command signals received via the second edge connections;
(e)	wherein the module controller is configured to receive via the second edge connections the address and command signals associated with the one or more memory read or write operations and to control the dynamic random access memory elements in accordance with the address and command signals, and wherein the module controller is further configured to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the second mode;
(f)	wherein the module controller is further configured to drive a notification signal associated with the one or more training sequences to the error edge connection via the open drain output while the memory module is in the first mode.

166. Netlist has alleged and continues to allege that Samsung infringes one or more claims of the ’218 patent.

167. Samsung has not directly or indirectly infringed any claim of the ’218 patent, either literally or under the doctrine of equivalents, at least because the Samsung DDR4 Memory Modules do not employ, incorporate, or otherwise make use of all of the limitations of the claims of the ’218 patent.

168. For example, claim 1 requires “wherein the memory module in the first mode is configured to be trained with one or more training sequences.” Similarly, claim 9 requires a “memory module” “training with one or more training sequences while the first edge connections are not active.” Claim 15 requires “wherein the memory module in the second operation is configured to be trained with one or more training sequences while the first edge connections are not active.” Thus, claims 1–22 of the ’218 patent require that the “memory module” is “configured to be trained with one or more training sequences.” Netlist appears to argue that Clock-to-CA training as described in the JEDEC standard meets the “first mode” and “second operation” limitations in claims 1 and 15, respectively. However, during Clock-to-CA training, it is the system memory controller—not the accused memory module—that is being trained so that it uses the correct timing of its signals; the accused memory module is not trained during the accused mode.

169. As another example, claim 1 requires “wherein the module controller is configured . . . to control the dynamic random access memory elements in accordance with the address and command signals.” Similarly, claim 15 requires “wherein the module controller in the first operation is configured . . . to control the dynamic random access memory elements in accordance with the address and command signals.” In the accused Samsung DDR4 Memory Modules, the alleged module controller does not control the DRAMs. Rather, the DRAMs are

controlled by the system memory controller. Thus, the accused Samsung DDR4 Memory Modules do not meet the limitations of at least claims 1–8 and 16–22.

170. As another example, claim 1 requires "wherein the module controller is further configured to drive a notification signal associated with the one or more training sequences to the error edge connection via the open drain output while the memory module is in the first mode." Similarly, claim 9 requires "memory module" "driving a notification signal associated with the one or more training sequences to the memory controller." Claim 15 requires "wherein the module controller in the second operation is configured to drive a notification signal associated with the one or more training sequences to the error edge connection via the open drain output of the module controller." Netlist appears to argue that the signal on the ALERT_n output pin meets these limitations during Clock-to-CA training. The signal on the ALERT_n output pin is not "a notification signal associated with the one or more training sequences" as required by the claims. The signal on the ALERT_n output pin does not indicate the status of any training, and ALERT_n is polled by the system memory controller during Clock-to-CA training. Thus, the accused Samsung Memory Modules do not meet the limitations of at least claims 1–22.

171. The Samsung DDR4 Memory Modules do not infringe any of claims 2–8, 10–14, and 16–22 at least because these claims depend directly or indirectly from claims 1 or 15.

172. For at least the same reasons described above, Samsung DDR5 Memory Modules do not infringe any claims of the '218 patent. In addition, Samsung, its customers, and its end users are not liable for infringement of the '218 patent for any Samsung Memory Modules made, imported, or sold under license from Netlist.

173. A substantial, immediate, and real controversy exists between Samsung and Netlist regarding whether Samsung or its customers or end users infringe the '218 patent by

making, using, selling, and/or offering for sale the Samsung Memory Modules in the United States, or by importing the Samsung Memory Modules into the United States. A judicial declaration is necessary to determine the parties' respective rights regarding the '218 patent.

174. Samsung seeks a judgment declaring that Samsung and its customers and end-users do not infringe the '218 patent, either literally or under the doctrine of equivalents, by making, using, selling, and/or offering for sale the Samsung Memory Modules in the United States, or by importing the Samsung Memory Modules into the United States, either directly under 35 U.S.C. § 271(a) or indirectly under 35 U.S.C. § 271(b)–(c).

COUNT IV
(Declaration of Non-Infringement of the '912 Patent)

175. Samsung restates and incorporates by reference the preceding paragraphs as if fully set forth herein.

176. The Patent Office issued the '912 patent, titled "Memory Module Decoder," on November 17, 2009. A true and correct copy of the '912 patent is attached hereto as Exhibit D. On information and belief, Netlist claims to own all rights, title, and interest in the '912 patent. The Patent Office issued an *Inter Partes* Reexamination Certificate for the '912 patent on February 8, 2021. A true and correct copy of the '912 patent and Reexamination Certificate is included in Exhibit 4.

177. The '912 patent has eleven independent claims: 1, 15, 16, 28, 39, 77, 80, 82, 86, 88, and 90. For example, claim 16 reads as follows:

Element	Claim Language
preamble	A memory module connectable to a computer system, the memory module comprising:
(a)	a printed circuit board;

Element	Claim Language
(b)	a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;
(c)	a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and
(d)	a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,
(e)	wherein the command signal is transmitted to only one DDR memory device at a time.

178. Netlist has alleged and continues to allege that Samsung infringes one or more claims of the ’912 patent. On information and belief, in the Google Infringement Action, Netlist contends that the Samsung DDR4 Memory Modules infringe claim 16 of the ’912 patent. Specifically, in the amended infringement contentions, Netlist points to the PDA mode in JESD79-4C for DDR4 SDRAM as the infringing feature.

179. Samsung has not directly or indirectly infringed any claim of the ’912 patent, either literally or under the doctrine of equivalents, at least because the Samsung DDR4 Memory Modules do not employ, incorporate, or otherwise make use of all of the limitations of the claims of the ’912 patent.

180. For example, the Samsung DDR4 Memory Modules do not meet claim limitation 16(c) at least because there is no "set of output signals" generated in response to a set of input signals "comprising at least one row/column address signal, bank address signals, and at least one chip-select signal." The alleged set of output signals are not generated in response to a set of input signals that include all of the signals required by the claim.

181. As another example, the Samsung DDR4 Memory Modules do not meet claim limitation 16(c) at least because there is no "set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks" that are generated in response to "the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks," where "the second number of DDR memory devices [is] smaller than the first number of DDR memory devices and the second number of ranks [is] less than the first number of ranks." In litigation against Inphi Corporation ("Inphi"), *Netlist, Inc. v. Inphi Corp.*, No. 09-cv-06900 (C.D. Cal.), Netlist alleged that a claim limitation containing similar language is satisfied by the Rank Multiplication Mode in JESD82-30 for LRDIMM DDR3 Memory Buffer (MB) Specification. The DDR4 Standards do not include the Rank Multiplication Mode.

182. As another example, the Samsung DDR4 Memory Modules do not meet claim limitation 16(e) at least because, in the PDA mode, there is no "command signal [that] is transmitted to only one DDR memory device at a time." Rather, the alleged command signal is transmitted to multiple DDR memory devices at a time.

183. As another example, the Samsung DDR4 Memory Modules do not meet at least the "a plurality of double-data-rate (DDR) memory devices . . . a first number of ranks" limitation, "a circuit . . . the first number of ranks" limitation, "wherein, the register . . . by the

logic element" limitation, and "wherein the logic element . . . the PLL clock signal" limitation in claim 1. In litigation against Inphi, Netlist alleged that these claim limitations are satisfied by the Rank Multiplication Mode in JESD82-30 for LRDIMM DDR3 Memory Buffer (MB) Specification. The Samsung DDR4 Memory Modules do not meet these limitations at least because the DDR4 Standards do not include the Rank Multiplication Mode. For the same reason, the Samsung DDR4 Memory Modules do not meet at least the following limitations in claims 15, 28, 39, 77, 80, 82, 86, 88, and 90:

- the "a plurality of double-data-rate (DDR) memory devices . . . a first number of ranks" limitation, "a circuit . . . the first number of ranks" limitation, "wherein, the register . . . by the logic element" limitation, and "wherein the logic element . . . the PLL clock signal" limitation in claim 15;
- the "a plurality of double-data-rate (DDR) dynamic random-access memory (DRAM) devices . . . a first number of ranks" limitation, "a circuit . . . the selected at least one rank" limitation, "wherein, the register . . . by the logic element" limitation, and "wherein the logic element . . . the PLL clock signal" limitation in claim 28;
- the "a plurality of double-data-rate (DDR) memory devices . . . a first number of chip-select signals" limitation, "at least one integrated circuit element . . . the selected at least one rank" limitation, "wherein, the register . . . by the logic element" limitation, and "wherein the logic element . . . the PLL clock signal" limitation in claim 39;
- the "a plurality of double-data-rate (DDR) memory devices . . . a first number of ranks" limitation, "a circuit . . . the first number of ranks" limitation, "wherein, the

register . . . by the logic element" limitation, and "wherein the logic element . . . the second number of ranks" limitation in claim 77;

- the "a plurality of double-data-rate (DDR) memory devices . . . a first number of ranks" limitation, "a circuit . . . the first number of ranks" limitation, "wherein operation of the register . . . the second number of ranks" limitation, "wherein the bank address signals . . . by the logic element" limitation, "wherein a plurality of row/column address signals . . . by the logic element" limitation, and "wherein the generation of the first number of chip-select signals . . . the phase-lock loop device" limitation in claim 80;
- the "a plurality of double-data-rate (DDR) memory devices . . . a first number of ranks" limitation, "a circuit . . . the first number of ranks" limitation, "wherein, the register . . . by the logic element" limitation, and "wherein the logic element . . . the set of input control signals" limitation in claim 82;
- the "a plurality of double-data-rate (DDR) memory devices . . . a first number of ranks" limitation, "a circuit . . . the first number of ranks" limitation, "wherein, the register . . . by the logic element" limitation, and "wherein the logic element . . . the set of input signals" limitation in claim 86;
- the "a plurality of double-data-rate (DDR) dynamic random-access memory (DRAM) devices . . . a first number of ranks" limitation, "a circuit . . . the selected at least one rank" limitation, "wherein, the register . . . by the logic element" limitation, and "wherein the logic element . . . the set of input control signals" limitation in claim 88; and

- the "a plurality of double-data-rate (DDR) memory devices . . . a first number of chip-select signals" limitation, "at least one integrated circuit . . . the selected at least one rank" limitation, "wherein, the register . . . by the logic element" limitation, and "wherein the logic element . . . the plurality of input signals" limitation in claim 90.

184. The Samsung DDR4 Memory Modules do not infringe any of claims 2–14, 17–27, 29–38, 40–76, 78, 79, 81, 83–85, 87 and 91 at least because these claims depend directly or indirectly from claims 1, 15, 16, 28, 39, 77, 80, 82, 86, 88, or 90.

185. For at least the same reasons described above, Samsung DDR5 Memory Modules do not infringe any claims of the '912 patent. In addition, Samsung, its customers, and its end users are not liable for infringement of the '912 patent for any Samsung Memory Modules made, imported, or sold under license from Netlist.

186. A substantial, immediate, and real controversy exists between Samsung and Netlist regarding whether Samsung or its customers or end users infringe the '912 patent by making, using, selling, and/or offering for sale the Samsung Memory Modules in the United States, or by importing the Samsung Memory Modules into the United States. A judicial declaration is necessary to determine the parties' respective rights regarding the '912 patent.

187. As alleged in Count X below, the claims of the '912 patent were subject to reexamination. During the course of the reexamination, Netlist canceled originally issued claims 2, 5, 7, 9, 21, 23, 25, 26, 30, 33, 42, 44, and 51; amended claims 1, 15, 16, 28, 39, and 43; and added new claims 52–91. Claims 3, 4, 6, 8, 10–14, 17–20, 22, 24, 27, 29, 31, 32, 34–38, 40, 41, and 45–50 were deemed patentable because of their dependence on amended claims. These amendments and additions, as well as arguments made by Netlist during the reexamination

proceeding, substantively changed the scope of the originally issued claims of the ’912 patent. Following an appeal to the Federal Circuit, the Patent Office issued an *Inter Partes* Reexamination Certification for the ’912 patent on February 8, 2021.

188. As a consequence of those amendments and additions, as well as Netlist’s reexamination proceeding arguments, the making, using, selling, offering for sale, and/or importing of the Samsung Memory Modules are protected by absolute and/or equitable intervening rights. In particular, to the extent that Netlist’s allegations are based on Samsung Memory Modules that were made, used, offered for sale, sold, and/or imported prior to the issuance of the reexamination certificate, the defense of absolute intervening rights bars any liability for infringement with respect to such products. To the extent Netlist’s accusations are based on Samsung Memory Modules that were made, used, offered for sale, sold, and/or imported after the issuance of the reexamination certificate, the defense of equitable intervening rights applies, because Samsung made substantial preparation of those products prior to issuance of the certificate. Netlist’s infringement allegations thus are barred, in whole or in part, by absolute and/or equitable intervening rights under 35 U.S.C. §§ 252 and 307(b).

189. Samsung seeks a judgment declaring that Samsung and its customers and end-users do not infringe the ’912 patent, either literally or under the doctrine of equivalents, by making, using, selling, and/or offering for sale the Samsung Memory Modules in the United States, or by importing the Samsung Memory Modules into the United States, either directly under 35 U.S.C. § 271(a) or indirectly under 35 U.S.C. §§ 271(b) and (c).

COUNT V
(Declaration of Non-Infringement of the ’506 Patent)

190. Samsung restates and incorporates by reference the preceding paragraphs as if fully set forth herein.

191. The Patent Office issued the ’506 patent, titled “Memory Module with Timing-Controlled Data Buffering,” on December 8, 2020. On information and belief, Netlist claims to own all rights, title, and interest in the ’506 patent. A true and correct copy of the ’506 patent is attached hereto as Exhibit 5.

192. The ’506 patent has two independent claims: 1 and 14. For example, claim 1 reads as follows:

Element	**Claim Language**
preamble	A memory module operable in a computer system to communicate with a memory controller of the computer system via a memory bus including control and address (C/A) signal lines and a data bus, the memory module comprising:
(a)	a module board having edge connections to be coupled to respective signal lines in the memory bus;
(b)	a module control device on the module board configurable to receive input C/A signals corresponding to a memory read operation via the C/A signal lines and to output registered C/A signals in response to the input C/A signals and to output module control signals;
(c)	memory devices arranged in multiple ranks on the module board and coupled to the module control device via module C/A signal lines that conduct the registered C/A signals, wherein the registered C/A signals cause a selected rank of the multiple ranks to perform the memory read operation by outputting read data and read strobes associated with the memory read operation, and wherein a first memory device in the selected rank is configurable to output at least a first section of the read data and at least a first read strobe; and
(d)	data buffers on the module board and coupled between the edge connections and the memory devices, wherein a respective data buffer of the data buffers is coupled to at least one respective memory device in each of the multiple ranks and is configurable to receive the module control signals from the module control device, and wherein a first data buffer of the data buffers is coupled to the first memory device and is configurable to, in response to one or more of the module control signals:
(e)	delay the first read strobe by a first predetermined amount to generate a first delayed read strobe;
(f)	sample the first section of the read data using the first delayed read strobe; and

Element	Claim Language
(g)	transmit the first section of the read data to a first section of the data bus;
(h)	wherein the first predetermined amount is determined based at least on signals received by the first data buffer during one or more previous operations.

193. Netlist has alleged and continues to allege that Samsung infringes one or more claims of the ’506 patent.

194. Samsung has not directly or indirectly infringed any claim of the ’506 patent, either literally or under the doctrine of equivalents, at least because the Samsung DDR4 Memory Modules do not employ, incorporate, or otherwise make use of all of the limitations of the claims of the ’506 patent.

195. For example, claim 1 of the ’506 patent requires that “the first predetermined amount is based at least on signals received by the first data buffer during one or more previous operations.” Similarly, claim 14 requires “determining the first predetermined amount based at least on signals received by the first data buffer.” Thus, all of the claims of the ’506 patent include these requirements. However, the accused Samsung DDR4 Memory Modules do not determine the alleged “predetermined amount” “based at least on signals received by the first data buffer during one or more previous operations.” The accused Samsung DDR4 Memory Modules are not responsible for the alleged training, and do not receive or use any “signals received by the first data buffer” to “determine” the alleged “predetermined amount.”

196. The Samsung DDR4 Memory Modules do not infringe any of claims 2–13 and 15–20 at least because these claims depend directly or indirectly from claims 1 or 14.

197. Samsung, its customers, and its end users are not liable for infringement of the ’506 patent for any Samsung Memory Modules made, imported, or sold under license from Netlist.

198. A substantial, immediate, and real controversy exists between Samsung and Netlist regarding whether Samsung or its customers or end users infringe the ’506 patent by making, using, selling, and/or offering for sale the Samsung DDR4 Memory Modules in the United States, or by importing the Samsung DDR4 Memory Modules into the United States. A judicial declaration is necessary to determine the parties’ respective rights regarding the ’506 patent.

199. Samsung seeks a judgment declaring that Samsung and its customers and end-users do not infringe the ’506 patent, either literally or under the doctrine of equivalents, by making, using, selling, and/or offering for sale the Samsung DDR4 Memory Modules in the United States, or by importing the Samsung DDR4 Memory Modules into the United States, either directly under 35 U.S.C. § 271(a) or indirectly under 35 U.S.C. § 271(b)–(c).

COUNT VI
(Declaration of Non-Infringement of the ’339 Patent)

200. Samsung restates and incorporates by reference the preceding paragraphs as if fully set forth herein.

201. The Patent Office issued the ’339 patent, titled “Memory Module With Controlled Byte-Wise Buffers,” on March 16, 2021. A true and correct copy of the ’339 patent is attached hereto as Exhibit 6. On information and belief, Netlist claims to own all rights, title, and interest in the ’339 patent.

202. The ’339 patent has four independent claims: 1, 11, 19, 27. For example, claim 1 reads as follows:

Element	Claim Language
preamble	A N-bit-wide memory module mountable in a memory socket of a computer system and configurable to communicate with a memory controller of the computer system via address and control signal lines and N-bit wide data signal lines, the N-bit wide data signal lines including a plurality of sets of data signal lines, each set of data signal lines is a byte wide, the memory module comprising:
(a)	a printed circuit board (PCB) having an edge connector comprising a plurality of electrical contacts which are positioned on an edge of the PCB and configured to be releasably coupled to corresponding contacts of the memory socket;
(b)	double data rate dynamic random access memory (DDR DRAM) devices coupled to the PCB and arranged in multiple N-bit-wide ranks;
(c)	a module controller coupled to the PCB and operatively coupled to the DDR DRAM devices, wherein the module controller is configurable to receive from the memory controller via the address and control signal lines input address and control signals for a memory write operation to write N-bit-wide write data from the memory controller into a first N-bit-wide rank of the multiple N-bit-wide ranks, and to output registered address and control signals in response to receiving the input address and control signals, wherein the registered address and control signals cause the first N-bit-wide rank to perform the memory write operation by receiving the N-bit-wide write data, wherein the module controller is further configurable to output module control signals in response to at least some of the input address and control signals; and
(d)	a plurality of byte-wise buffers coupled to the PCB and configured to receive the module control signals, wherein each respective byte-wise buffer of the plurality of byte-wise buffers has a first side configured to be operatively coupled to a respective set of data signal lines, a second side that is operatively coupled to at least one respective DDR DRAM device in each of the multiple N-bit-wide ranks via respective module data lines, and a byte-wise data path between the first side and the second side, wherein the each respective byte-wise buffer is disposed on the PCB at a respective position corresponding to the respective set of the plurality of sets of data signal lines;
(e)	wherein the each respective byte-wise buffer further includes logic configurable to control the byte-wise data path in response to the module control signals, wherein the byte-wise data path is enabled for a first time period in accordance with a latency parameter to actively drive a respective byte-wise section of the N-bit wide write data associated with the memory operation from the first side to the second side during the first time period; and

Element	Claim Language
(f)	wherein the byte-wise data path includes first tristate buffers, and the logic in response to the module control signals is configured to enable the first tristate buffers to drive the respective byte-wise section of the N-bit wide write data to the respective module data lines during the first time period.

203. Netlist has alleged and continues to allege that Samsung infringes one or more claims of the ’339 patent.

204. Samsung has not directly or indirectly infringed any claim of the ’339 patent, either literally or under the doctrine of equivalents, at least because the Samsung DDR4 Memory Modules do not employ, incorporate, or otherwise make use of all of the limitations of the claims of the ’339 patent.

205. For example, claim 1 requires “a plurality of byte-wise buffers” and further requires that “each respective byte-wise buffer includes logic configurable to control the byte-wise data path in response to the module control signals, wherein the byte-wise data path is enabled for a first time period.” The ’339 patent identifies the data transmission circuit as the “byte-wise buffer.” Similarly, claim 11 requires “n/2 data transmission circuits” and further requires that “each respective data transmission circuit is configurable to enable the data paths for a first time period.” Claim 19 similarly requires “a plurality of buffers” and further requires that “each respective buffer further includes logic configurable to enable the data paths for a first time period” and “to enable the data paths for a second time period subsequent to the first time period.” Claim 27 requires “a plurality of n-bit-wise data buffers.” Netlist appears to allege that any circuit that complies with JEDEC Standard JESD82-32A satisfies the requirement of the “byte-wise buffer,” “data transmission circuit,” “buffers,” or “n-bit-wise data buffers.” However, the circuits defined in JEDEC Standard JESD82-32A and used in the accused Samsung DDR4 Memory Modules are not the “byte-wise buffer,” “data transmission circuit,” “buffers,” or “n-bit-wise data buffers” of the

’339 patent. For example, the circuits used in the accused Samsung DDR4 Memory Modules do not contain multiple data paths and do not select or switch between data paths. Thus, the accused Samsung DDR4 Memory Modules do not meet these limitations of claims 1–35.

206. The Samsung DDR4 Memory Modules do not infringe any of claims 2–10, 12–18, 20–26, and 28–35 at least because these claims depend directly or indirectly from claims 1, 11, 19, or 27.

207. Samsung, its customers, and its end users are not liable for infringement of the ’339 patent for any Samsung Memory Modules made, imported, or sold under license from Netlist.

208. A substantial, immediate, and real controversy exists between Samsung and Netlist regarding whether Samsung or its customers or end users infringe the ’339 patent by making, using, selling, and/or offering for sale the Samsung DDR4 Memory Modules in the United States, or by importing the Samsung DDR4 Memory Modules into the United States. A judicial declaration is necessary to determine the parties’ respective rights regarding the ’339 patent.

209. Samsung seeks a judgment declaring that Samsung and its customers and end users do not infringe the ’339 patent, either literally or under the doctrine of equivalents, by making, using, selling, and/or offering for sale the Samsung DDR4 Memory Modules in the United States, or by importing the Samsung DDR4 Memory Modules into the United States, either directly under 35 U.S.C. § 271(a) or indirectly under 35 U.S.C. § 271(b)–(c).

COUNT VII
(Declaration of Non-Infringement of the ’918 Patent)

210. Samsung restates and incorporates by reference the preceding paragraphs as if fully set forth herein.

211. The Patent Office issued the ’918 patent, titled “Flash-DRAM hybrid memory module,” on May 25, 2021. A true and correct copy of the ’918 patent is attached hereto as Exhibit 7. On information and belief, Netlist claims to own all rights, title, and interest in the ’918 patent.

212. The ’918 patent has three independent claims: 1, 16, and 23. For example, claim 1 reads as follows:

Element	Claim Language
preamble	A memory module comprising:
(a)	a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;
(b)	a first buck converter configured to provide a first regulated voltage having a first voltage amplitude;
(c)	a second buck converter configured to provide a second regulated voltage having a second voltage amplitude;
(d)	a third buck converter configured to provide a third regulated voltage having a third voltage amplitude;
(e)	a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude; and
(f)	a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, the plurality of components comprising:
(g)	a plurality of synchronous dynamic random access memory (SDRAM) devices coupled to the first regulated voltage, and
(h)	at least one circuit coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices, the at least one circuit operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices, the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage, wherein a first one of the second and fourth voltage amplitudes is less than a second one of the second and fourth voltage amplitudes.

213. Netlist has alleged and continues to allege that Samsung infringes one or more claims of the ’918 patent.

214. Samsung has not directly or indirectly infringed any claim of the ’918 patent, either literally or under the doctrine of equivalents, at least because the Samsung DDR5 Memory Modules do not employ, incorporate, or otherwise make use of all of the limitations of the claims of the ’918 patent.

215. For example, each of claims 1, 16, and 23 requires memory modules having first, second, and third buck converters that provide first, second, and third regulated voltages, respectively. Claims 1 and 16 further require that the first, second, and third regulated voltages have first, second, and third voltage amplitudes, respectively. Netlist alleges that the Samsung DDR5 Memory Modules include buck converters that provide only two regulated voltages (1.1 volts and 1.8 volts). *See* Texas Infringement Action, D.I. 1, ¶ 72. Thus, the Samsung DDR5 Memory Modules do not meet these limitations of claims 1–29. Likewise, the Samsung DDR5 Memory Modules do not include “a converter circuit” that provides “a fourth regulated voltage,” as required by claims 1, 16, and 23.

216. The Samsung DDR5 Memory Modules do not infringe any of claims 2–15, 17–22, and 24–29 at least because these claims depend directly or indirectly from claims 1, 16, or 23.

217. Moreover, Samsung does not infringe the ’918 patent with respect to Samsung DDR5 LRDIMMs because Samsung does not manufacture or supply such memory modules.

218. Samsung, its customers, and its end users are not liable for infringement of the ’918 patent for any Samsung Memory Modules made, imported, or sold under license from Netlist.

219. A substantial, immediate, and real controversy exists between Samsung and Netlist regarding whether Samsung or its customers or end users infringe the ’918 patent by making, using, selling, and/or offering for sale the Samsung DDR5 Memory Modules in the United States, or by importing the Samsung DDR5 Memory Modules into the United States. A judicial declaration is necessary to determine the parties’ respective rights regarding the ’918 patent.

220. Samsung seeks a judgment declaring that Samsung and its customers and end users do not infringe the ’918 patent, either literally or under the doctrine of equivalents, by making, using, selling, and/or offering for sale the Samsung DDR5 Memory Modules in the United States, or by importing the Samsung DDR5 Memory Modules into the United States, either directly under 35 U.S.C. § 271(a) or indirectly under 35 U.S.C. § 271(b)–(c).

COUNT VIII
(Declaration of Unenforceability of the ’523 Patent Due to Inequitable Conduct & Unclean Hands)

221. Samsung restates and incorporates by reference the preceding paragraphs as if fully set forth herein.

A. Netlist Individuals Substantively Involved in the ’523 Patent Prosecution

222. On information and belief, at least the following people associated with Netlist were substantively involved in the prosecution of the application that issued as the ’523 patent: Hyun Lee; Jayesh Bhakta; Soonju Choi; Noel Whitley; Marwan Fawal; Gail Sasaki; and patent prosecution counsel Jamie Zheng (collectively “Netlist Individuals Substantively Involved in the ’523 Patent Prosecution”).

223. Hyun Lee, Jayesh Bhakta and Soonju Choi are the named inventors of the ’523 patent and signed oaths that were submitted with the application attesting to being the inventors of the alleged invention(s) claimed in the application.

224. On information and belief, Noel Whitley was, during the prosecution of the application that issued as the ’523 patent, an employee and/or contractor for Netlist with responsibility for managing prosecution of the application that issued as the ’523 patent.

225. On information and belief, Marwan Fawal was, during the prosecution of the application that issued as the ’523 patent, a contractor for Netlist who consulted on the prosecution of the application that issued as the ’523 patent.

226. On information and belief, Gail Sasaki was, during the prosecution of the application that issued as the ’523 patent, an employee and/or contractor for Netlist who signed the power of attorney for the application that issued as the ’523 patent.

227. Jamie Zheng is the prosecuting attorney for the application that issued as the ’523 patent.

228. On information and belief, the above individuals involved in the prosecution of the application that issued as the ’523 patent, such as Noel Whitley, Marwan Fawal and/or Jamie Zheng, utilized information obtained in the litigation between Netlist and SK hynix regarding, for instance, SK hynix’s non-infringement positions for the ’434, ’501, and/or ’064 patents to which the application that issued as the ’523 patent claims priority, for purposes of assisting in drafting and/or amending the claims of the application that issued as the ’523 patent in an attempt to overcome SK hynix’s non-infringement arguments.

229. On information and belief, each of the Netlist Individuals Substantively Involved in the ’523 Patent Prosecution is an individual associated with the filing and prosecution of the application that issued as the ’523 patent.

B. The Inventors and Others Knew of Ellsberry and Jeddeloh752 Before the Application That Issued as the ’523 Patent Was Even Filed

230. The ’523 patent claims priority to the same provisional patent applications to which the ’434, ’501, and ’064 patents claim priority. All four patents share the same specification, inventors, and alleged priority dates.

1. Early Knowledge of Ellsberry

231. In addition to being a named inventor on the ’523 patent, Jayesh Bhakta is a named inventor on the ’912 patent. U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”) was cited during prosecution of the ’912 patent in 2010. On information and belief, at least Jayesh Bhakta became aware of Ellsberry at that time.

232. On information and belief, at least Hyun Lee, Noel Whitley and Jamie Zheng learned of Ellsberry during the prosecution of other Netlist patents before the application that issued as the ’523 patent was filed.

2. Early Knowledge of Jeddeloh752

233. U.S. Patent No. 7,310,752 (“Jeddeloh752”) was disclosed to JEDEC as potentially essential to JEDEC standards before 2010, and appears in many JEDEC presentations as a disclosed patent, including to the standards for DDR4 LRDIMMs that Netlist accuses of infringement.

234. Hyun Lee regularly attended JEDEC meetings for at least the JC-40 committee and the JC-45 committee from 2008 to 2010, as well as before and after that timeframe. For instance, on information and belief, Hyun Lee attended at least the following JC-40 meetings:

No. 155, Aug. 28, 2008; No. 156, Dec. 4-5, 2008; No. 158, June 4, 2009; No. 159, Sept. 10, 2009; No. 160, Dec. 10, 2009; No. 161, Mar. 4. 2010. And, on information and belief, Hyun Lee attended at least the following JC-45 meetings: No. 20, Aug 27-28, 2008; No. 21, Dec. 3-5, 2008; No. 23, June 3, 2009; No. 24, Sept 9-10, 2009; No. 25, Dec. 9, 2009; No. 26, Mar. 2-3, 2010.

235. By virtue of his attendance at those meetings, active involvement in JEDEC and otherwise, on information and belief, Hyun Lee was aware of Jeddeloh752 and its disclosure as a potentially essential patent to JEDEC standards, including DDR4 LRDIMM standards.

236. Hyun Lee, on information and belief, shared JEDEC presentations, including Jeddeloh752, with at least Noel Whitley and Jayesh Bhakta and they too learned of Jeddeloh752 and its disclosure as a potentially essential patent to JEDEC standards, including DDR4 LRDIMM standards, before the application that issued as the ’523 patent was filed.

C. ’523 Patent Prosecution and Corresponding Events

237. Netlist filed the application, No. 14/229,844, which ultimately issued as the ’523 patent, on March 29, 2014.

1. Netlist “Buries” the Examiner with Everything, Except Ellsberry and Jeddeloh752

238. Netlist submitted information disclosure statements on August 7, 2014, August 10, 2014, December 24, 2014, February 16, 2016, February 17, 2016, February 18, 2016, and July 13, 2016.

239. Netlist submitted so many references in those information disclosure statements that the examiner asked Netlist to identify the ones “which have particular significance,” and “to highlight those documents which have been specifically brought to applicant’s attention and/or are known to be of most significance.”

240. Despite submitting so many references, Netlist did not submit Ellsberry or Jeddeloh752.

241. Nor did Netlist ever do what the examiner requested with respect to the references it did submit: identify the ones "which have particular significance," and "highlight those documents which have been specifically brought to applicant's attention and/or are known to be of most significance."

242. On October 20, 2016, the examiner issued a final office action rejecting the then-pending claims. In that office action, the examiner stated (citations omitted, emphasis added):

> An applicant's duty of disclosure of material information is not satisfied by presenting a patent examiner with "a mountain of largely irrelevant data from which he is presumed to have been able, with his expertise and with adequate time, to have found the critical data. It ignores the real world conditions under which examiners work." An applicant has a duty to not just disclose pertinent prior art references but to make a disclosure in such way as not to ***"bury"*** it within other disclosures of less relevant prior art. *It is unreasonable for Examiner to review all of the cited references thoroughly. By signing the accompanying 1449 forms, Examiner is merely acknowledging the submission of the cited references and indicating that* ***only a cursory review has been made****.*

Office Action, Application No. 14/229,844 (October 20, 2016).

2. Netlist Sues SK hynix on Parent Patents, Learns SK hynix Non-Infringement and Invalidity Positions, and Relies on Jeddeloh752 in Those Suits, All While Continuing to Prosecute the '523 Patent

243. On August 31 and September 1, 2016, Netlist filed complaints against SK hynix in the Central District of California and the U.S. International Trade Commission asserting the '434, '501 and '064 patents against SK hynix.

244. On January 3-5, 2017, SK hynix filed IPR petitions against each of the ’434, ’501 and ’064 patents. *See* IPR2017-00560 (’064 IPR); IPR2017-00561 (’434 IPR); IPR2017-00562 (’501 IPR).

245. Returning to the pending application that eventually issued as the ’523 patent, on March 21, 2017, Netlist filed a request for continued examination that, among other things, amended the claims of the application.

246. On March 24, 2017, Netlist filed another information disclosure statement. Like all previous information disclosure statements, it did not include Ellsberry or Jeddeloh752.

247. On April 4, 2017, the examiner issued a non-final office action rejecting the then-pending claims.

248. On September 5, 2017, Netlist filed an amendment that, among other things, again amended the claims of the application that issued as the ’523 patent.

249. On September 5, 2017, Netlist also filed another information disclosure statement. Like all previous information disclosure statements, it did not include Ellsberry or Jeddeloh752.

250. On December 8, 2017, the examiner issued a final office action rejecting the then-pending claims.

251. During the period of time addressed above that Netlist was amending the claims in the application that issued as the ’523 patent, Netlist and SK hynix exchanged their prehearing briefs in the then-pending 1023 ITC Investigation, in which Netlist was asserting the ’434, ’501, and ’064 patents against SK hynix, conducted the full evidentiary hearing in that Investigation, submitted post-hearing briefs, and submitted petitions to the Commission seeking review of the Administrative Law Judge’s (ALJ) initial determination finding no infringement of

the ’434, ’501, and ’064 patents, all of which addressed SK hynix’s arguments for why the accused products did not infringe the ’434, ’501, and ’064 patents’ claims.

252. Netlist continued amending the claims thereafter, as set forth below.

253. Furthermore, during the 1023 ITC investigation, Netlist specifically relied on Jeddeloh752 as a patent declared essential to the DDR4 LRDIMM standards, the practice of which it alleged infringed the ’434, ’501, and ’064 patents, when arguing that Netlist had fulfilled its obligations to offer a license to the ’434, ’501, and ’064 patents on RAND terms. For instance, Netlist submitted an expert’s testimony that relied on Jeddeloh752 as support for his opinion that Netlist’s licensing offers for the ’434, ’501, and ’064 patents were reasonable and non-discriminatory.

3. Netlist Receives SK hynix’s ’907 Patent IPR Presenting Ellsberry and Arguments Based Thereon, While Prosecuting the ’523 Patent

254. On December 22, 2017, SK hynix filed an IPR petition against U.S. Patent No. 9,606,907 (the “’907 patent”) asserting that the Ellsberry prior art reference rendered all of the claims of the ’907 patent unpatentable. *See* Ex. 27, IPR2018-00362. The ’907 patent lists Hyun Lee and Jayesh Bhakta as inventors, both of whom are named as inventors on the ’523 patent. That IPR petition explained, among other things, how Ellsberry disclosed or rendered obvious claim limitations directed to memory modules with DRAMs organized in ranks on a printed circuit board with edge connectors, a control module for buffering address and control signals from a system memory controller, and distributed data buffers for buffering data signals to/from a system memory controller, as well as normal operations of that memory module.

255. Returning to the pending application that eventually issued as the ’523 patent, on February 8, 2018, Netlist filed a request for consideration under the after final

consideration pilot program 2.0 that, among other things, yet again amended the claims of the application that issued as the ’523 patent.

256. On February 15, 2018, Netlist filed a request for continued examination that, among other things, yet further amended the claims of the application that issued as the ’523 patent.

257. On April 10, 2018, the examiner issued an *Ex parte Quayle* action indicating the application was in condition for allowance, other than formal matters.

258. On May 2, 2018, Netlist filed a response to the *Ex parte Quayle* action that, among other things, amended yet again the claims of the application that issued as the ’523 patent.

259. On May 17, 2018, Netlist submitted additional information disclosure statements. Like so many before them, the information disclosure statements did not include Ellsberry or Jeddeloh752.

260. On August 28, 2018, Netlist submitted yet another information disclosure statement, this time listing the Final Written Decisions (“FWDs”) from the IPRs of the ’434, ’501, and ’064 patents. It still did not include Ellsberry or Jeddeloh752.

261. On October 16, 2018, the examiner issued a Notice of Allowance for the application that issued as the ’523 patent.

262. On November 20, 2018, the examiner filed an interview summary for an applicant-initiated interview that occurred on November 13, 2018, indicating that the substance of the interview was: “Discussed status of the application and IDS dated on 8/28/18.” The summary includes nothing regarding Ellsberry or Jeddeloh752, and they still were not disclosed.

263. On January 15, 2019, Netlist paid the issue fee for the application that issued as the ’523 patent.

264. By the time of Netlist's interview with the examiner in November 2018, before which Netlist submitted its August 2018 IDS:

1) the PTAB had issued a decision instituting SK hynix's IPR against the '907 patent based on Ellsberry;

2) Ms. Zheng has been specifically questioned about Ellsberry at a deposition;

3) a German patent cancellation proceeding against a German counterpart to the '907 patent based on Ellsberry was ongoing;

4) a Chinese counterpart to the '907 patent had been ruled invalid based on Ellsberry by a Chinese tribunal; and

5) a continuation application to the '907 patent that Ms. Zheng was prosecuting had its claims rejected based on Ellsberry.

265. Despite all of the above, Ms. Zheng did not submit Ellsberry or Jeddeloh752 to the examiner before the '523 patent issued, nor did Hyun Lee, Jayesh Bhakta, or Noel Whitley.

D. SK hynix's IPR Against the '523 Patent

266. On August 21, 2020, SK hynix filed an IPR petition against the '523 patent asserting that Ellsberry in combination with Jeddeloh752 render all the claims of the patent unpatentable, either by themselves or in combination with other references for certain dependent claims. *See* Ex. 28, IPR2020-01421.

267. In general, that petition argues that Ellsberry discloses the claimed details of a memory module with a normal mode of operation and DRAMs organized in ranks on a printed circuit board with edge connectors, a control module for buffering address and control signals from a system memory controller, and distributed data buffers for buffering data signals to/from a

system memory controller, and that Jeddeloh752 renders obvious adding a test mode to Ellsberry's memory modules and the claimed circuit functionality to implement the testing.

268. On March 16, 2021, the PTAB instituted the IPR filed against the '523 patent as to all challenged claims. *See* Ex. 29, IPR2020-01421, Paper No. 10.

E. Netlist's Failure to Disclose Ellsberry During the Prosecution of the '523 Patent

269. At least by December 22, 2017, Jamie Zheng, Hyun Lee, Jayesh Bhakta, and Noel Whitley knew of the Ellsberry prior art reference, and SK hynix's detailed explanations (set forth in SK hynix's IPR petition with respect to the '907 patent) as to why that reference disclosed or rendered obvious claim limitations directed to memory modules with DRAMs organized in ranks on a printed circuit board with edge connectors, a control module for buffering address and control signals from a system memory controller, and distributed data buffers for buffering data signals to/from a system memory controller, as well as normal operations of that memory module. On information and belief, Jamie Zheng, Hyun Lee, Jayesh Bhakta and Noel Whitley recognized the materiality of Ellsberry to the then-pending claims of the application that issued as the '523 patent, either at that time or at least by the time of the November 2018 interview with the examiner.

270. Ellsberry is material and not cumulative of other art or information before the examiner of the application that issued as the '523 patent. The pertinent disclosure in Ellsberry is described in detail in the August 21, 2020 IPR petition against the '523 patent filed by SK hynix, IPR2020-01421, which is incorporated herein by reference and attached hereto as Exhibit 28. As set forth in the IPR petition, Ellsberry discloses memory modules with distributed data buffers ("data handlers") between the memory devices and data edge connections on the module, as well as the details of conventional module components/interconnections called for by the '523 patent

claims. The references considered by the examiner did not provide the same disclosure. In its Patent Owner's Preliminary Response, Netlist did not argue that Ellsberry is cumulative of other information that was before the examiner.

271. The Patent Office would not have allowed at least one claim of the '523 patent to issue had it been aware of Ellsberry, at least because it would have found a claim obvious over that art, as explained in SK hynix's IPR petition filed against the '523 patent (Ex. 28) and in the PTAB's March 16, 2021 Decision Granting Institution (Ex. 29).

272. On information and belief, Jamie Zheng, Hyun Lee, Jayesh Bhakta, and Noel Whitley specifically intended to deceive the Patent Office into believing that the claims of the '523 patent were patentable, by withholding Ellsberry from the examiner during prosecution of the application that issued as the '523 patent. On information and belief, Jamie Zheng, Hyun Lee, Jayesh Bhakta, and Noel Whitley engaged in this conduct as part of a scheme to monetize Netlist's patents through litigation against the industry.

F. Netlist's Failure to Disclose Jeddeloh752 During the Prosecution of the '523 Patent

273. At least by December 2017, on information and belief, Hyun Lee and Noel Whitley knew of—by virtue of for instance Hyun Lee's attendance at JEDEC meetings and Noel Whitley's knowledge of Netlist's positions regarding Netlist's RAND contentions taken in the 1023 Investigation—Jeddeloh752 and its disclosure as a potentially essential patent to JEDEC standards, including DDR4 LRDIMM standards.

274. Jeddeloh752 is material and not cumulative of other art or information before the examiner of the application that issued as the '523 patent. The pertinent disclosure in Jeddeloh752 is described in detail in the August 21, 2020 IPR petition against the '523 patent filed by SK hynix, IPR2020-01421, which is incorporated herein by reference and attached hereto as

Exhibit 28. As set forth in the IPR petition, Jeddeloh752 discloses certain aspects of self-test circuitry, including a functional block diagram with elements corresponding to certain limitations in the claims of the ’523 patent. The references considered by the examiner did not provide the same disclosure. In its Patent Owner’s Preliminary Response, Netlist did not argue that Jeddeloh752 is cumulative of other information that was before the examiner.

275. The Patent Office would not have allowed at least one claim of the ’523 patent to issue had it been aware of Jeddeloh752, at least because it would have found a claim obvious over that art in combination with Ellsberry, as explained in SK hynix’s IPR petition filed against the ’523 patent (Ex. 28) and in the PTAB’s March 16, 2021 Decision Granting Institution (Ex. 29).

276. On information and belief, Hyun Lee and Noel Whitley recognized the materiality of that art and specifically intended to deceive the Patent Office into believing that the claims of the ’523 patent are patentable by withholding that art from the examiner during prosecution of the application that issued as the ’523 patent. On information and belief, Hyun Lee and Noel Whitley engaged in this conduct as part of a scheme to monetize Netlist’s patents through litigation against the industry.

* * * *

277. Inequitable Conduct: Any one or more acts set forth above are sufficient in and of itself/themselves to demonstrate that Netlist committed inequitable conduct during the prosecution of the ’523 patent that renders the ’523 patent unenforceable.

278. Unclean Hands: Furthermore, any one or more acts set forth above are sufficient in and of itself/themselves to demonstrate that Netlist has unclean hands in relation to its assertion of the ’523 patent that renders the ’523 patent unenforceable.

COUNT IX
(Declaration of Unenforceability of the ’218 and ’595 Patents Due to Inequitable Conduct & Unclean Hands)

279. Samsung restates and incorporates by reference the preceding paragraphs as if fully set forth herein.

A. Netlist Individuals Substantively Involved in the ’218 and ’595 Patent Prosecutions

280. On information and belief, at least the following people associated with Netlist were substantively involved in the prosecution of the applications that issued as the ’218 and/or ’595 patents: Hyun Lee; Noel Whitley; Marwan Fawal; Gail Sasaki; and patent prosecution counsel Jamie Zheng (collectively “Netlist Individuals Substantively Involved in the ’218 and ’595 Patent Prosecutions”).

281. Hyun Lee is the lone named inventor of the ’218 and ’595 patents, and signed oaths that were submitted with each application attesting to being the sole inventor of the alleged inventions claimed in those applications.

282. On information and belief, Noel Whitley was, during the prosecution of the applications that issued as the ’218 and ’595 patents, an employee and/or contractor for Netlist with responsibility for managing prosecution of the applications that issued as the ’218 and ’595 patents.

283. On information and belief, Marwan Fawal was, during the prosecution of the applications that issued as the ’218 and ’595 patents, a contractor for Netlist who consulted on the prosecution of the applications that issued as the ’218 and ’595 patents.

284. On information and belief, Gail Sasaki was, during the prosecution of the applications that issued as the ’218 and ’595 patents, an employee and/or contractor for Netlist

who signed the powers of attorney for each of the applications that issued as the ’218 and ’595 patents.

285. Jamie Zheng is the prosecuting attorney for the applications that issued as the ’218 and ’595 patents.

286. On information and belief, the above individuals involved in the prosecution of the applications that issued as the ’218 and ’595 patents, such as Noel Whitley, Marwan Fawal, and/or Jamie Zheng, utilized information obtained in litigation between Netlist and SK hynix regarding, for instance, SK hynix’s non-infringement positions for the ’837 patent and/or the ’623 patent to which the applications that issued as the ’218 and ’595 patents claim priority, for purposes of assisting in drafting and/or amending the claims of the applications that issued as the ’218 and ’595 patents in an attempt to overcome arguments that DDR4 memory modules are non-infringing.

287. On information and belief, each of the Netlist Individuals Substantively Involved in the ’218 and ’595 Patent Prosecutions is an individual associated with the filing and prosecution of the applications that issued as the ’218 and ’595 patents.

B. Background on the Alleged Invention, and the Prosecution of the ’218 and ’595 Patents, and Events Occurring During the Same

288. Both the ’218 and ’595 patents claim priority to the same provisional patent application to which the ’837 and ’623 patents claim priority. All four patents share the same specification, inventor, and alleged priority dates.

289. Netlist filed a terminal disclaimer for the ’623 patent over the ’837 patent, and over the application that issued as the ’218 patent. Netlist likewise filed a terminal disclaimer for the ’218 patent over the ’837 patent. Netlist likewise filed a terminal disclaimer for the ’595 patent over the ’837 patent, and over the ’218 patent.

1. Hyun Lee's Alleged Solo Conception and Reduction to Practice, and Regular Attendance at JEDEC Meetings

290. Hyun Lee regularly attended JEDEC meetings for at least the JC-40 committee and the JC-45 committee from 2008 to 2010, as well as before and after that timeframe. For instance, on information and belief, Hyun Lee attended at least the following JC-40 meetings: No. 155, Aug. 28, 2008; No. 156, Dec. 4-5, 2008; No. 158, June 4, 2009; No. 159, Sept. 10, 2009; No. 160, Dec. 10, 2009; No. 161, Mar. 4. 2010. And, on information and belief, Hyun Lee attended at least the following JC-45 meetings: No. 20, Aug 27-28, 2008; No. 21, Dec. 3-5, 2008; No. 23, June 3, 2009; No. 24, Sept 9-10, 2009; No. 25, Dec. 9, 2009; No. 26, Mar. 2-3, 2010.

291. By virtue of his attendance at those meetings, active involvement in JEDEC and otherwise, on information and belief, Hyun Lee was aware of the draft and final specifications for DDR3 RDIMMs being considered and voted upon by those committees, including JESD82-29, dated December 2009, as well as prior drafts of it, such as a draft dated May 2009 on its cover, and with notes in the headers of its pages indicating that it was last edited on June 4, 2009 at 5:43 am, and the other specifications for DDR3 RDIMM considered by those committees.

292. A true and correct copy of JESD82-29 is attached as Exhibit 30. On information and belief, this standard was circulated at or before, and discussed at and voted on at or before, JC-40 and JC-45 committee meetings that Hyun Lee attended.

293. A true and correct copy of a draft of JESD82-29, dated May 2009 on its cover and with notes in the headers of its pages indicating that it was last edited on June 4, 2009 at 5:43 am, is attached as Exhibit 31. On information and belief, this draft was circulated at or before, and discussed at, the June 3-4, 2009 JC-40 and JC-45 committee meetings that Hyun Lee attended.

294. By virtue of his attendance at those meetings, active involvement in JEDEC and otherwise, on information and belief, Hyun Lee was aware of the draft and final specifications for DDR3 LRDIMMs being considered and voted upon by those subcommittees, including the Committee Letter Ballot sent to committee members in November 2009 with the subject "LRDIMM DDR3 Memory Initialization Chapter Proposal," as well as prior drafts of it and the other specifications for DDR3 LRDIMM considered by those committees, such as another Committee Letter Ballot sent to committee members in November 2009 with the subject "DDR3 LRDIMM Design Specification Body."

295. A true and correct copy of the Committee Letter Ballot sent to committee members in November 2009 with the subject "LRDIMM DDR3 Memory Initialization Chapter Proposal" is attached as Exhibit 32.

296. A true and correct copy of the Committee Letter Ballot sent to committee members in November 2009 with the subject "DDR3 LRDIMM Design Specification Body" is attached as Exhibit 33.

297. Draft specifications, ballots and presentations distributed to the members of the JC-40 and/or JC-45 committees of JEDEC were distributed to many (20+) key members of the interested public with the expectation they would be freely disclosed to and discussed with others. As such, they are prior art under 35 U.S.C. § 102 at least as of those distribution dates.

298. Distributed specifications, such as JESD82-29, are prior art under 35 U.S.C. § 102 at least as of their release dates.

299. The provisional application to which the '837, '623, '218, and '595 patents all claim priority was filed on June 12, 2009, naming Hyun Lee as the sole inventor.

300. In a case brought by Netlist in the Central District of California, *Netlist Inc. v. SK hynix, Inc.*, No. 8:16-CV-01605, Netlist explained to the court during claim construction that the '837 patent discloses (and thus the '623, '218, and '595 patents disclose, since they all share a common specification):

> an improved configuration for memory modules which includes the system memory controller handing off portions of an initialization sequence to the memory module. *See* '837 Patent at 2:56–59 (JX-0006). … The '837 Patent discloses an apparatus and method of handshaking, in which the memory subsystem (the memory module) sends a signal to the system memory controller indicating a status of the initialization procedure.

Netlist Inc. v. SK hynix, Inc. (No. 8:16-CV-01605), D.I. 124 at 3–4.

301. Thus, according to Netlist, the '218 and '595 patents disclose an "improved" memory module that (1) executes "hand[ed] off portions of an initialization sequence" from "the system memory controller" and (2) "sends a signal to the system memory controller indicating a status of the initialization procedure."

302. The provisional application explicitly states that a "recent proposal in JEDEC for LR-DIMM (Load Reduced DIMM) requires" the system memory controller "to hand over one or more parts of the initialization operation sequences" to the memory module, "which raises an unprecedented issue" for the system memory controller because "it needs a way of handshaking with the" memory module such that the memory module notifies the system memory controller when the initialization sequence is complete.

303. Netlist has admitted that the "recent proposal" referenced in the provisional application is a June 4, 2009 presentation by Inphi entitled, "MB Initialization sequence Item 142.35," that was presented to the members of JEDEC at a JEDEC committee meeting on June 4, 2009.

304. On information and belief, Hyun Lee attended that meeting, witnessed that presentation, and was present for the discussions that occurred about it.

305. A true and correct copy of the June 4, 2009 "MB Initialization sequence Item 142.35" presentation by Inphi is attached as Exhibit 34.

306. The "MB Initialization sequence Item 142.35" presentation discloses a system memory controller handing off portions of an initialization sequence to the memory module, such as MB-DRAM interface training.

307. At that same meeting, another presentation was made, by IDT, Texas Instruments, Montage Technology, and Inphi, entitled "Memory Buffer Membist for LRDIMM DDR3 MB TG item # 142.43."

308. On information and belief, Hyun Lee witnessed that presentation and was present for the discussions that occurred about it as well.

309. A true and correct copy of the "Memory Buffer Membist for LRDIMM DDR3 MB TG item # 142.43" presentation is attached as Exhibit 35.

310. On information and belief, and based on Netlist's apparent view of the scope of the alleged invention, the "Memory Buffer Membist for LRDIMM DDR3 MB TG item # 142.43" presentation discloses a memory module sending a signal to the system memory controller indicating a status of an initialization procedure, MEMBIST testing and/or training. For instance, on information and belief and based on Netlist's apparent view of the scope of the alleged invention, the meeting minutes for the June 4, 2009 JEDEC meeting, which Hyun Lee attended, state (regarding the discussions surrounding that presentation) that the memory module "[c]an use an error indicator … to report errors."

311. On information and belief, after attending the June 4, 2009 meeting and listening to these ideas from other members of JEDEC, Hyun Lee returned to Netlist and hurriedly completed drafting the provisional application to which the ’837, ’623, ’218 and ’595 patents all claim priority, naming himself as the sole inventor, and had it filed only eight days after that meeting, on June 12, 2009.

2. ’218 Patent Prosecution and Corresponding Events

312. Netlist filed the application, No. 15/088,115, that issued as the ’218 patent on April 1, 2016.

313. On October 12, 2017, the examiner issued a Notice of Allowance for the application that issued as the ’218 patent.

314. On November 15, 2017, Netlist filed an Amendment after Allowance and an IDS, and paid the issue fee for the application that issued as the ’218 patent.

315. On December 1, 2017, the examiner accepted the Amendment.

316. On December 13, 2017, the examiner issued an issue date notification for the application that issued as the ’218 patent. That notification specified an issue date of January 2, 2018.

317. The very next day, on December 14, 2017, SK hynix filed an IPR petition against the ’623 patent asserting that U.S. Patent Application Publication No. 2008/0098277 (“Hazelzet”), alone or in combination with, for instance, U.S. Patent No. 8,139,430 (“Buchmann”), U.S. Patent Application Publication No. 2008/0155378 (“Talbot”), or U.S. Patent Application Publication No. 2008/0155378 (“Amidi”), rendered all of the claims of the ’623 patent unpatentable. *See* Ex. 36, IPR2018-00303, Paper No. 1.

318. Netlist took no action to withdraw the application that issued as the ’218 patent from issuance, or to otherwise continue prosecution of that application, and the application issued as the ’218 patent on January 2, 2018.

3. ’595 Patent Prosecution and Corresponding Events

319. On information and belief, instead of seeking to withdraw the application that issued as the ’218 patent from issuance and submit, for instance, the ’623 IPR petition, Hazelzet, Buchmann, Talbot, and/or Amidi, for consideration by the examiner, Netlist prepared the application, No. 15/857,553, that eventually issued as the ’595 patent for filing, and filed that application on December 28, 2017.

320. On information and belief, Netlist did eventually submit the ’623 IPR petition, Hazelzet, Buchmann, Talbot, and Amidi for consideration by the examiner of the application that issued as the ’595 patent.

321. On February 6, 2019, the examiner issued a Notice of Allowance for the application that issued as the ’595 patent.

322. Instead of paying the issue fee, on March 1, 2019, Netlist filed a request for continued examination that, among other things, amended the claims of the application that issued as the ’595 patent.

323. On March 29, 2019, the examiner issued another Notice of Allowance for the application that issued as the ’595 patent.

324. Instead of paying the issue fee, on July 1, 2019, Netlist filed another request for continued examination that, among other things, again amended the claims of the application that issued as the ’595 patent.

325. On August 9, 2019, the examiner issued another Notice of Allowance for the application that issued as the ’595 patent.

326. Netlist paid the issue fee on August 16, 2019.

327. Shortly before and during the period of time that Netlist was amending the claims in the application that issued as the ’595 patent after they were allowed, Netlist and SK hynix exchanged contentions and submitted extensive briefing in the then-pending ITC Investigation (*In re Certain Memory Modules*, 337-TA-1089) addressing arguments that DDR4 memory modules do not infringe the ’623 patent claims, as the ITC ultimately ruled.

4. SK hynix’s IPRs Against the ’623, ’218 and ’595 Patents

328. As noted, on December 14, 2017, SK hynix filed an IPR petition against the ’623 patent asserting that Hazelzet, alone or in combination with, for instance, Buchmann, Talbot or Amidi, rendered all the claims of the ’623 patent unpatentable. *See* Ex. 36, IPR2018-00303, Paper No. 1.

329. The PTAB instituted that IPR and, on March 21, 2019, issued FWDs finding all claims of the ’623 patent unpatentable in view of, for instance, Hazelzet in combination with Buchmann. *See* Ex. 37, IPR2018-00303, Paper No. 42.

330. In general, the PTAB found that Hazelzet discloses the claimed details of a memory module with a normal mode of operation utilizing parity error checking and notifying the system memory control of those parity errors via an open-drain output, and found that Buchmann rendered obvious adding a training mode to Hazelzet’s memory modules and notifying the system memory control about the execution and/or completion of that training via Hazelzet’s open-drain output. *See id*.

331. At least pursuant to Netlist’s apparent view of the claims, the claims of the ’218 and ’595 patents claim patentably indistinct alleged inventions compared to the ’623 patent claims, as illustrated, for example, by Netlist’s filing of terminal disclaimers for the ’218 and ’595

patents over the ’623 patent and patents for which Netlist filed terminal disclaimers for the ’623 patent.

332. On June 9, 2020, SK hynix filed IPR petitions against the ’218 and ’595 patents asserting that Hazelzet in combination with either Buchmann or the JEDEC Committee Letter Ballot sent to committee members in November 2009 with the subject “LRDIMM DDR3 Memory Initialization Chapter Proposal” (Ex. 32) rendered all the claims of the patents unpatentable, either by themselves or in combination with another reference for certain dependent claims. *See* Ex. 38, IPR2020-01042 (’595 IPR); Ex. 39 IPR-2020-01044 (’218 IPR).

333. In general, those petitions argue that Hazelzet discloses the claimed details of a memory module with a normal mode of operation utilizing parity error checking and notifying the system memory control of those parity errors via an open-drain output, and that Buchmann or “LRDIMM DDR3 Memory Initialization Chapter Proposal” (Ex. 32) render obvious adding a training mode to Hazelzet’s memory modules and notifying the system memory control about the execution and/or completion of that training via Hazelzet’s open-drain output.

334. On December 17, 2020, the PTAB instituted the IPRs filed against the ’218 and ’595 patents as to all claims. *See* Ex. 40, IPR2020-01042, Paper No. 14; Ex. 41, IPR2020-01044, Paper No. 13.

C. Netlist’s Failure to Disclose the Presentations from the June 4, 2009 JEDEC JC-40 Meeting Attended by Hyun Lee, and False Portrayal of Hyun Lee as a Sole Inventor

335. At least according to Netlist’s characterizations of the inventive aspects of the disclosure and claims of the ’218 and ’595 patents, the June 4, 2009 presentation by Inphi entitled “MB Initialization sequence Item 142.35” that was presented to the members of JEDEC at a JEDEC committee meeting on June 4, 2009 (Ex. 34), and June 4, 2009 presentation by IDT, Texas Instruments, Montage Technology and Inphi entitled “Memory Buffer Membist for

LRDIMM DDR3 MB TG item # 142.43" that was presented to the members of JEDEC at a JEDEC committee meeting on June 4, 2009 (Ex. 35), disclose the key allegedly inventive aspects of the claims of the '218 and '595 patents. Specifically, these presentations disclose a memory module that (1) executes "hand[ed] off portions of an initialization sequence" from "the system memory controller" and (2) "sends a signal to the system memory controller indicating a status of the initialization procedure." *Netlist Inc. v. SK hynix, Inc.* (No. 8:16-CV-01605), D.I. 124 at 3–4.

336. Even though Hyun Lee was present at the JEDEC meeting at which those presentations were made, witnessed those presentations, and was present for the discussions that occurred about them, and immediately thereafter drafted the provisional application to which the '218 and '595 patents claim priority, on information and belief, Hyun Lee did not disclose either of those presentations to the examiner of the applications that issued as the '218 and '595 patents.

337. Those presentations are prior art under 35 U.S.C. § 102 at least as of June 4, 2009.

338. The presentations marked as Exhibits 34 and 35 are material and not cumulative of other art or information before the examiner of the applications that issued as the '218 and '595 patents. For example, during prosecution of the '218 and '595 patents, Netlist argued that the art of record did not disclose an open drain output for both a parity error signal during normal operation and a notification signal while carrying out training sequences outside of normal operation. The June 4, 2009 presentation by Inphi entitled "MB Initialization sequence Item 142.35" describes, for example, a memory module with "training" and "normal operation," Ex. 34 at 3, and includes an "ERROUT#" bit, *id*. at 4–5. The June 4, 2009 presentation by IDT, Texas Instruments, Montage Technology and Inphi entitled "Memory Buffer Membist for LRDIMM DDR3 MB TG item # 142.43" describes, for example, a memory module with a "Membist" that

includes the use of "Data Patterns, Address Patterns, failure locators" for "Characterization, Validation, Debug and Failure Analysis." Ex. 35 at 3–4. At least these exemplary disclosures are material to the patentability of the '218 and '595 patents.

339. Those presentations also illustrate that Hyun Lee falsely portrayed himself as the sole inventor of the alleged inventions claimed in the '218 and '595 patents. At a minimum, those presentations illustrate that Hyun Lee derived at least portions of the allegedly inventive aspects of the claimed inventions from others in attendance at the June 4, 2009 meeting, who made those presentations on behalf of Inphi, IDT, Montage and TI.

340. The Patent Office would not have allowed at least one claim of each of the '218 and '595 patents to issue had it been aware of those presentations, at least because it would have found the claims obvious over those presentations (either in combination with the knowledge of one of ordinary skill, in combination with art disclosing the basic architecture and functionality of DDR2 and DDR3 RDIMMs of the time, and/or in combination with Hazelzet), that there are joint inventors that were not properly named on the applications that issued as the '218 and '595 patents, and/or that the alleged inventions claimed therein had been derived in whole or in part from another.

341. On information and belief, Hyun Lee specifically intended to deceive the Patent Office into believing that Hyun Lee was the sole inventor of the '218 and '595 patents, and/or that the claims of those patents are otherwise patentable, by withholding those presentations from the patent examiner during prosecution of the applications that issued as the '218 and '595 patents. On information and belief, Hyun Lee engaged in this conduct as part of a scheme to monetize Netlist's patents through litigation against the industry.

D. Netlist's Failure to Disclose Hazelzet, Buchmann, Talbot and/or Amidi During the Prosecution of the '218 Patent

342. At least by December 14, 2017, the day after the Patent Office issued an issue notice for the application that issued as the '218 patent, Jamie Zheng knew of the prior art references by Hazelzet, Buchmann, Talbot, and/or Amidi, and SK hynix's detailed explanations (set forth in its IPR petition) as to why those references rendered the claims of the '623 patent, which Netlist admitted were patentably indistinct from the then-pending claims of the '218 patent application, unpatentable. On information and belief, Jamie Zheng recognized the materiality of the Hazelzet, Buchmann, Talbot and/or Amidi references to the then-pending claims of the application that issued as the '218 patent.

343. Netlist and Jamie Zheng could have withdrawn the '218 patent application from issuance and submitted SK hynix's IPR petition and art, but, on information and belief, chose not to do so because she wanted the '218 patent to issue so that Netlist could attempt to assert it in litigation, including its on-going ITC investigation seeking to exclude DDR4 memory modules, as it subsequently tried to do.

344. Rather than submitting the IPR petition and art to the Patent Office, Netlist and Jamie Zheng instead filed the application that eventually issued as the '595 patent between the time the '623 patent IPR petition was filed and the date on which the '218 patent issued.

345. Hazelzet, Buchmann, Talbot, and/or Amidi are not cumulative of other art or information before the examiner of the application that issued as the '218 patent. The pertinent disclosure in these references is described in detail in the December 14, 2017 IPR petition against the '623 patent filed by SK hynix (Ex. 36), the June 8, 2020 IPR petition filed against the '218 patent filed by SK hynix (Ex. 39), and the December 17, 2020 Decision Granting Institution of the IPR petition against the '218 patent (Ex. 41), each of which is incorporated herein by reference

and attached hereto as Exhibit 36. In the IPR proceeding filed against the ’218 patent, Netlist did not argue that Hazelzet, Buchmann, Talbot, and/or Amidi are cumulative of other art or information before the examiner.

346. The Patent Office would not have allowed at least one claim of the ’218 patent to issue had it been aware of Hazelzet, Buchmann, Talbot, and/or Amidi, at least because it would have found a claim obvious over that art, consistent with the PTAB’s FWD declaring that claims 1–29 of the ’623 patent are unpatentable (Ex. 37) and the PTAB’s Decision Granting Institution of the IPR petition filed against the ’218 patent (Ex. 41).

347. On information and belief, Jamie Zheng specifically intended to deceive the Patent Office into believing that the claims of the ’218 patent were patentable, and intended to induce the Patent Office into promptly issuing those claims so that the ’218 patent could be added to the 1089 ITC Investigation, by withholding that art from the examiner during prosecution of the applications that issued as the ’218 and ’595 patents. On information and belief, Jamie Zheng engaged in this conduct as part of a scheme to monetize Netlist’s patents through litigation against the industry.

E. Netlist’s Failure to Disclose Drafts/Ballots for DDR3 LRDIMM Specifications

348. At least by November 2009, on information and belief, Hyun Lee knew of, by virtue for instance his attendance at JEDEC meetings, the Committee Letter Ballot sent to JC-40 committee members in November 2009 with the subject “LRDIMM DDR3 Memory Initialization Chapter Proposal” (Ex. 32), and the Committee Letter Ballot sent to JC-40 committee members in November 2009 with the subject “DDR3 LRDIMM Design Specification Body” (Ex. 33).

349. As explained in the IPR petitions filed against the ’218 and ’595 patents, the claims of the ’218 and ’595 patents are not entitled to claim priority to the June 12, 2009 provisional application, making the ballots marked as Exhibits 32 and 33 prior art to both patents. *See* Ex. 38, IPR2020-01042, Paper No. 1 (’595 IPR); Ex. 39, IPR-2020-01044, Paper No. 1 (’218 IPR).

350. For example, claim 1 of the ’218 patent requires the negative limitation that the memory module be “configured to perform one or more memory read or write operations *not associated with the one or more training sequences* by communicating data signals via the first edge connections in response to address and command signals received via the second edge connections.” However, the terms “read operation,” “write operation” (or just “write”), “data signals” (or just “data”), “first edge connections” (or just “edge”), “address signals” (or just “address”), “command signals,” and “second edge connections” for receiving such address and command signals appear nowhere in the provisional, much less any disclosure of how such read and write operations in the “second” (operational) mode relate to the training sequences used in the “first” (initialization) mode. As another example, each independent claim of the ’595 patent requires the negative limitation that the memory controller *not access the module for memory read and write operations* in a training mode. However, the provisional says nothing about the memory controller not accessing the module for read and write operations in training mode; indeed, it mentions the word “training” in only one sentence fragment, never explains that such training may occur in its own mode, never uses the word “mode” at all, and never says anything about what operations may or may not occur in training mode. On information and belief, at least Hyun Lee knew that the claims of the ’218 and ’595 patents are not entitled to claim priority to the June 12, 2009 provisional application.

351. The ballots marked as Exhibits 32 and 33 are material and not cumulative of other art or information before the examiner of the applications that issued as the ’218 and ’595 patents. For example, during prosecution of the ’218 and ’595 patents, Netlist argued that the art of record did not disclose an open drain output for both a parity error signal during normal operation and a notification signal while carrying out training sequences outside of normal operation. The November 2009 Committee Letter Ballot with the subject “LRDIMM DDR3 Memory Initialization Chapter Proposal” discusses, for example, initialization of prior art memory modules including an “ERROUT#” output pin, *e.g.*, Ex. 32 at 6, and “Host Interface CA Clk-to-CMD Training,” *e.g.*, *id*. at 4. The November 2009 Committee Letter Ballot with the subject “DDR3 LRDIMM Design Specification Body” discloses, for example, an “open drain” pin named “ErrOut_n” that indicates a “[p]arity error detected on the Address and Command bus.” Ex. 33 at 6, 8, 10, 30. At least these exemplary disclosures are material to the patentability of the ’218 and ’595 patents.

352. When voting on the ballots marked as Exhibits 32 and 33, Netlist abstained from voting and indicated that it held intellectual property that may be relevant to the subject matter, presumably the June 12, 2009 provisional application that Hyun Lee had hurriedly drafted and filed after he attended the June 4, 2009 JEDEC meeting discussed above.

353. The Patent Office would not have allowed at least one claim of each of the ’218 and ’595 patents to issue had it been aware of the ballots marked as Exhibits 32 and 33, at least because it would have found a claim obvious over that art in combination with Hazelzet consistent with the PTAB’s FWD in the ’623 patent IPR, as explained in the IPR petitions filed against the ’218 and ’595 patents and the PTAB’s decisions granting institution of those IPRs.

354. On information and belief, Hyun Lee recognized the materiality of that art and specifically intended to deceive the Patent Office into believing that the claims of the ’218 and ’595 patents are patentable by withholding that art from the examiner during prosecution of the applications that issued as the ’218 and ’595 patents. On information and belief, Hyun Lee engaged in this conduct as part of a scheme to monetize Netlist’s patents through litigation against the industry.

F. Netlist’s Failure to Disclose the JESD82-29 Specification and/or Drafts/Ballots Thereof

355. At least by November 2009, on information and belief, Hyun Lee knew, at least by virtue of his attendance at JEDEC meetings, of JESD82-29, dated December 2009 (Ex. 30), and, by at least June 4, 2009, knew of a draft of that specification dated May 2009 on its cover with notes in the headers of its pages that it was last edited on June 4, 2009 at 5:43 am (Ex. 31).

356. As explained in the IPR petitions filed against the ’218 and ’595 patents, the claims of the ’218 and ’595 patents are not entitled to claim priority to the June 12, 2009 provisional application, making JESD82-29, marked as Exhibit 30, prior art to both patents. The draft of the same, marked as Exhibit 31, is prior art regardless as it was publicly available before the provisional application was filed.

357. For example, claim 1 of the ’218 patent requires the negative limitation that the memory module be “configured to perform one or more memory read or write operations *not associated with the one or more training sequences* by communicating data signals via the first edge connections in response to address and command signals received via the second edge connections.” However, the terms “read operation,” “write operation” (or just “write”), “data signals” (or just “data”), “first edge connections” (or just “edge”), “address signals” (or just

"address"), "command signals," and "second edge connections" for receiving such address and command signals appear nowhere in the provisional, much less any disclosure of how such read and write operations in the "second" (operational) mode relate to the training sequences used in the "first" (initialization) mode. As another example, each independent claim of the '595 patent requires the negative limitation that the memory controller *not access the module for memory read and write operations* in a training mode. However, the provisional says nothing about the memory controller not accessing the module for read and write operations in training mode; indeed, it mentions the word "training" in only one sentence fragment, never explains that such training may occur in its own mode, never uses the word "mode" at all, and never says anything about what operations may or may not occur in training mode. On information and belief, at least Hyun Lee knew that the claims of the '218 and '595 patents are not entitled to claim priority to the June 12, 2009 provisional application.

358. JESD82-29 and the draft thereof marked as Exhibit 31 are material and not cumulative of other art or information before the examiner of the applications that issued as the '218 and '595 patents. For example, during prosecution of the '218 and '595 patents, Netlist argued that the art of record did not disclose an open drain output for both a parity error signal during normal operation and a notification signal while carrying out training sequences outside of normal operation. JESD82-29 and the draft thereof marked as Exhibit 31 disclose, for example, that the memory module included an "open-drain ERROUT# pin" that indicated "whether a parity error has occurred." *See, e.g.*, Ex. 31 at 5. At least this disclosure is material to the patentability of the '218 and '595 patents.

359. The Patent Office would not have allowed at least one claim of each of the '218 and '595 patents to issue had it been aware of JESD82-29 and the draft thereof marked as

Exhibit 31, at least because it would have found a claim obvious over that art in combination with, for instance, Buchmann, consistent with the PTAB's FWD in the '623 patent IPR, the arguments in SK hynix's IPR petitions filed against the '218 and '595 patents, and the PTAB's decisions granting institution of the IPRs filed against the '218 and '595 patents.

360. On information and belief, Hyun Lee recognized the materiality of that art and specifically intended to deceive the Patent Office into believing that the claims of the '218 and '595 patents are patentable by withholding that art from the examiner during prosecution of the applications that issued as the '218 and '595 patents. On information and belief, Hyun Lee engaged in this conduct as part of a scheme to monetize Netlist's patents through litigation against the industry.

G. Netlist's Violation of the Estoppel Rules of 37 C.F.R. § 42.73(d)

361. The PTAB, on March 21, 2019, issued an FWD finding all claims of the '623 Patent unpatentable in view of, for instance, Hazelzet in combination with Buchmann. *See* Ex. 37. Jamie Zheng received a copy of that FWD the same day it issued.

362. Netlist filed a terminal disclaimer for the '623 patent over the '837 patent, and the application that issued as the '218 patent. Netlist likewise filed a terminal disclaimer for the '218 patent over the '837 patent. Netlist likewise filed a terminal disclaimer for the '595 patent over the '837 patent, and the '218 patent. Netlist has thus terminally disclaimed the '218 and '595 patents over the '623 patent because the Patent Office found the claims of the respective patents patentably indistinct from each other, and Netlist chose not to contest those findings.

363. The issued claims of the '595 patent are not patentably distinct from the claims of the '623 patent that were held unpatentable in view of, for instance, Hazelzet in combination with Buchmann.

364. On information and belief, Jamie Zheng was aware of 37 C.F.R. § 42.73 when prosecuting the application that issued as the '595 patent.

365. Despite the issuance of the FWD finding the '623 patent claims unpatentable on March 21, 2019, which constitutes a "judgment" per 37 C.F.R. § 42.73(a), on information and belief, Jamie Zheng and Netlist continued prosecuting the application that issued as the '595 patent, submitting multiple Requests for Continued Examination and eventually paying the issue fee. All those actions are in violation of the estoppel provisions of 37 C.F.R. § 42.73(d), are *per se* material, and constitute affirmative acts of egregious misconduct.

366. But for the violation of those estoppel provisions by Jamie Zheng and Netlist, the Patent Office would not have issued the '595 patent.

367. On information and belief, Jamie Zheng specifically intended to deceive the Patent Office into issuing the '595 patent by failing to abide by the estoppel provisions of 37 C.F.R. § 42.73(d). On information and belief, Jamie Zheng engaged in this conduct as part of a scheme to monetize Netlist's patents through litigation against the industry.

* * * *

368. Inequitable Conduct: Any one or more acts set forth above are sufficient in and of itself/themselves to demonstrate that Netlist committed inequitable conduct during the prosecution of the '218 and '595 patents that renders the '218 and '595 patents unenforceable. To the extent any particular act is only found sufficient to support a finding of inequitable conduct as to one of the '218 and '595 patents, the doctrine of infectious unenforceability renders the other patent unenforceable as well.

369. Unclean Hands: Furthermore, any one or more acts set forth above are sufficient in and of itself/themselves demonstrated that Netlist has unclean hands in relation to its

assertion of the ’218 and ’595 patents that renders the ’218 and ’595 patents unenforceable. To the extent any particular act is only found sufficient to support a finding of unclean hands as to one of the ’218 and ’595 patents, the doctrine of infectious unenforceability renders the other patent unenforceable as well.

COUNT X
(Declaration of Unenforceability of the ’912 Patent Due to Inequitable Conduct & Unclean Hands)

370. Samsung restates and incorporates by reference the preceding paragraphs as if fully set forth herein.

A. Netlist Individuals Substantively Involved in the ’912 Reexamination

371. On information and belief, at least the following people associated with Netlist were substantively involved in the *inter partes* reexamination proceedings with respect to the ’912 patent: Gail Sasaki, Mehran Arjomand, and David S. Kim (collectively “Netlist Individuals Substantively Involved in the ’912 Patent Reexamination”).

372. On information and belief, Gail Sasaki was, during the reexamination proceedings for the ’912 patent, an employee and/or contractor for Netlist who signed the power of attorney appointing counsel of record to prosecute the reexamination proceeding on behalf of Netlist.

373. Mehran Arjomand and David S. Kim served as counsel of record for Netlist in connection with the *inter partes* reexamination proceedings for the ’912 patent.

374. On information and belief, the Netlist Individuals Substantively Involved in the ’912 Patent Reexamination withheld information that they knew to be material to the patentability of the ’912 patent with the specific intent to deceive the Patent Office in order to secure allowance of certain amended claims.

375. On information and belief, each of the Netlist Individuals Substantively Involved in the ’912 Reexamination is an individual associated with the prosecution of the ’912 patent during the *inter partes* reexamination proceedings, which ultimately led to the issuance of an *Inter Partes* Reexamination Certificate on February 8, 2021.

B. Netlist Made Narrowing Amendments to Claims During Reexamination

376. The ’912 patent was originally filed in the United States on September 27, 2007 by inventors Jayesh R. Bhakta and Jeffrey C. Solomon. The ’912 patent, titled “Memory Module Decoder,” issued on November 17, 2009. Netlist claims to own all rights, title, and interest in the ’912 patent.

377. On April 20, 2010, a first request for *inter partes* reexamination of claims 1–51 of the ’912 patent was filed by third party requester Inphi. The Patent Office assigned this request control No. 95/001,339 (“’339 proceeding”) and ultimately ordered the reexamination of claims 1–51 of the ’912 patent on September 1, 2010.

378. On October 20, 2010, a second request for *inter partes* reexamination of claims 1, 6, 3–4, 6–11, 15, 18–22, 24–25, 27–29, 31–34, 36–39, 41–45, and 50 of the ’912 patent was filed by third party requester SMART Modular Technologies (WWH), Inc. (“SMART”). The Patent Office assigned this request control No. 95/000,578 (“’578 proceeding”) and ordered reexamination of claims 1, 3–4, 6–11, 15, 18–22, 24–25, 27–29, 31–34, 36–39, 41–45, and 50 of the ’912 patent on January 14, 2011.

379. On October 21, 2010, a third request for *inter partes* reexamination of claims 1, 3–4, 6–11, 15, 18–22, 24–25, 27–29, 31–34, 36–39, 41–45, and 50 of the ’912 patent was filed by Google. The Patent Office assigned this request control No. 95/000,579 (“’579 proceeding”) and ordered reexamination of claims 1, 3–4, 6–11, 15, 18–22, 24–25, 27–29, 31–34, 36–39, 41–45, and 50 of the ’912 patent on January 18, 2011.

380. The Examiner in the ’578, ’579, and ’339 proceedings agreed with Inphi, SMART, and Google that the proposed combination of Micron, DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF28672 Data Sheet, 2002 (“Micron”) in view of U.S. Patent Application Publication No. 2006.0117152 (“Amidi”) presented a substantial new question of patentability and that “a reasonable examiner would consider the teaching of Micron and Amidi important in deciding the patentability of” the challenged claims. *See* January 14, 2011 Reexamination Ordered.

381. On February 25, 2011, the Patent Office *sua sponte* merged the ’578, ’579, and ’339 proceedings into a single matter, as all three proceedings were pending, had yet to be terminated, and involved overlapping claims of the same patent.

382. After the merger, Netlist argued against the pending rejections of the existing claims and added new claims 52–118. *See* Netlist’s July 5, 2011 Response to Office Action in *Inter Partes* Reexamination Communication Mailed April 4, 2011. For example, Netlist argued that the phase-lock loop device disclosed in Amidi was not “operatively coupled” to its CPLD. Netlist narrowed the scope of the “operatively coupled” feature by arguing that in the context of the ’912 patent the phrase means that “the operations of the logic element 40 are clocked either directly or indirectly (e.g., through a clock buffer) by the output of the PLL 50” and that “the output of the PLL 50 controls the operation of the logic element 40.”

383. Google responded by explaining how Micron and Amidi rendered obvious both the original and new claims. *See* August 29, 2011 Response. Google also explained how Micron, Amidi, U.S. Patent No. 5,926,827 (“Dell 2”), and Double Data Rate (DDR) SDRAM Specification, JEDEC Standard No. 79C, March 2003 (“JEDEC 79C”) rendered obvious the new claims. *Id*. The Examiner adopted some aspects of the grounds raised by Google, rejected other

aspects, and declined to adopt other grounds. *See* October 14, 2011 Non-Final Office Action. Netlist responded by canceling some of its claims, amending most of the remaining claims, and adding new claims 119–136. *See* January 14, 2012 Netlist's Response After Non-Final Action. Google again respondedby continuing to argue, among other things, that Micron, Amidi, Dell 2, and/or JEDEC 79C rendered obvious a set of the pending claims. *See* February 23, 2012 Google's Response.

384. The Examiner then adopted additional grounds for rejection and maintained certain earlier rejections. *See* November 13, 2012 Non-Final Action. Netlist responded by canceling certain claims, further amending other claims, and arguing against the rejections. *See* January 14, 2013 Netlist's Response After Non-Final Action. Google again explained why various combinations of Micron, Amidi, Dell 2, and JEDEC 79C (among other references) rendered the claims obvious. *See* February 13, 2013 Google's Response.

385. The Examiner issued an Action Closing Prosecution, which maintained several rejections, withdrew others, and found certain rejections moot due to Netlist canceling certain claims. *See* March 21, 2014 Action Closing Prosecution. The Examiner issued a Right of Appeal Notice, and Google appealed the Examiner's unadopted portions of certain grounds. *See* July 18, 2014 Google's Notice of Appeal. Netlist cross-appealed on the grounds of rejection the Examiner maintained. *See* July 30, 2014 Netlist's Notice of Cross Appeal.

386. The PTAB, in its first appeal decision, affirmed the Examiner's adoption of certain aspects of the ground involving Micron in view of Amidi, reversed the Examiner's refusal to adopt other aspects of this ground, reversed the Examiner's refusal to adopt the ground involving Micron in view of Amidi and Olarig, and declined to reach the merits on the ground involving Micron in view of Amidi, Dell 2, and JEDEC 79C. *See* June 6, 2016 Decision on Appeal.

387. Netlist then requested that the Patent Office reopen prosecution, canceling certain claims and amending most of the remaining claims. *See* July 31, 2016 Netlist's Response Requesting to Reopen Prosecution. It was in this set of amendments in which Netlist amended claim 1 and several other claims to include the following language:

- "wherein, in response to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR memory devices, the logic element, and the register" ("PLL device limitation");

- "wherein, the register (i) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices" ("register limitation"); and

- "wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output control signals in response to at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal." ("logic element limitation").

388. Netlist asserted that these three amendments were "principal amendments to overcome the new grounds of rejection" and further stated that "[t]o address the Board's rejection, Patent Owner *narrowed* the claim to include" the above identified three amendments. *Id*. (emphasis added). Netlist then referenced the above identified "claim amendments [to] highlight at least two differences between the '912 invention and the prior art." *Id*. Below are the two differences that Netlist highlighted to the PTAB:

> First, the claim amendments now require: In response to signals received from the computer system, the phase-lock loop (PLL) device transmit a PLL clock to the plurality of DDR memory devices, the logic element, and the register. Amidi transmits a PLL clock signal to the register and memory, but not the CPLD. Thus, Amidi does not disclose the PLL device transmitting the PLL clock to the logic element; the output of PLL 606 is neither directly nor indirectly transmitted to the CPLD 604. Additionally, a POSITA would not be motivated or inclined to transmit the PLL clock to CPLD 604.

> Second, the amended claims now also require that the logic element generates certain output signals (e.g., gated column access strobe (CAS) signals or chip-select signals recited in claim 1) in response to at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal. Amidi's CPLD 604 never receives bank address signals and hence Amidi's control signals cannot be generated based on bank address signals. Instead, the control signals (rcs0a, rcs0b, rcs1a, rcs1b, rcs2a, rcs2b, rcs3a, and rcs3b) are based on the row address signals and chip-select signals. Thus, Amidi does not disclose the CPLD generating the gated CAS signals or chip-select signals in response to *the bank address signals*. Moreover, since the output of PLL 606 is neither directly nor indirectly transmitted to the CPLD 604, a POSITA would understand that the PLL clock does not control the operation of CPLD 604. Thus, Amidi is further deficient by failing to disclose the CPLD generating the gated CAS signals or chip-selected signals in response to the *PLL clock signal*.

Id. (emphasis in original) (internal citations omitted).

389. Netlist went on to further explain how the specific amendments above were the distinguishing factors over Amidi:

> As amended, the claims require that the *logic element receives* at least one row address signal and *bank address signals*, and require that the *register* (i) *receives*, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and *the bank address signals*, and (iii) transmit the buffered plurality of DDR memory devices. The claims also require the plurality of row/column address signals received by the register are separate from the at least one row address signal received by the logic element. In other words, in the confirmation recited by the claims, the bank address signals are received by the logic element, the register and the plurality of memory devices. Under such circumstances, Amidi does not use bank address signals to generate control signals (and certainly not the bank address signals and the at least one row address signal.) The claims, however, require generating CAS signals or chip-select signals based on a row address signal and bank address signals.
>
> Based on the above, it would not be obvious to a POSITA to combine Amidi and Dell 2 to reach the claimed invention, as amended. For the sake of argument, however, even the proposed combination of Amidi and Dell 2 fails to disclose the claimed

> invention. Therefore, even in combination, Amidi in view of Dell 2 fails to disclose all of the claim recitations of the claims.

Id. (emphasis in original) (internal citations omitted).

390. Following Google's response to Netlist's amendments and response, the PTAB remanded the case to the Examiner and the Examiner maintained the PTAB's new grounds of rejection as well as one additional ground. *See* October 3, 2017 Examiner's Determination Under 37 C.F.R. § 41.77(d).

391. The PTAB then issued its second appeal decision, affirming several prior rejections but withdrawing many of the rejections the PTAB and the Examiner had previously maintained. *See* July 27, 2018 Decision on Appeal. The withdrawn rejections corresponded to the combination of Micron in view of Amidi and Micron in view of Amidi and Olarig. *Id*. The PTAB determined, among other things, that the addition of the "logic element" limitation distinguished the invention from the prior art of record. *See, e.g.*, *id*. at 23 ("[W]e are persuaded Micron and Amidi do not teach or suggest the newly recited 'logic element' limitation in claim 1 or similar independent claims."). Google sought rehearing, which the PTAB denied. *See* January 31, 2019 Decision on Rehearing. In the Decision on Rehearing, the PTAB again emphasized that the prior art of record, including Amidi, does not teach the "logic element" limitation recited in claim 1. *See id*. at 3–5. Google then appealed the PTAB's decision to the Federal Circuit.

392. In its responsive appeal brief to the Federal Circuit, Netlist repeatedly stated that "it *narrowed* its claims to define its precise inventive contributions over the prior art." December 12, 2019 Netlist Response Brief (emphasis added). Therefore, in statements to the PTAB and the Federal Circuit, Netlist reiterated that the amendments identified above are *narrowing*, and that it was these narrowing amendments that were Netlist's basis for arguing that

the prior art at issue does not disclose the asserted claims. It was in response to these statements that the PTAB withdrew its rejections of the asserted claims and the Federal Circuit affirmed the PTAB's decision on June 15, 2020.

393. The *Inter Partes* Reexamination Certification for the '912 patent issued on February 8, 2021.

C. After the Claims Issued with the Narrowing Amendments, Netlist Argued in Litigation that the Amendments Did Not Change the Scope of the Claims

394. After the *Inter Partes* Reexamination Certification for the '912 patent issued on February 8, 2021, Netlist resumed its litigation against Google.

395. On information and belief, Gail Sasaki is involved in overseeing Netlist's litigation against Google.

396. On July 30, 2021, Google filed a Motion for Summary Judgment on the Issue of Absolute Intervening Rights. *See Netlist, Inc. v. Google LLC*, No. 4:09-cv-05718-SBA, D.I. 155.

397. On September 3, 2021, Netlist filed its Opposition to Google's Motion for Summary Judgement on the Issue of Absolute Intervening Rights. *See id*., D.I. 196. In the opposition, Netlist argued, in direct contradiction to what it argued to the PTAB and the Federal Circuit during reexamination proceedings, that the above identified claim amendments were not narrowing. Instead, Netlist now argues that "the language added during reexamination clarified what was inherent in the original claims." D.I. 196 at 17; *see also id*. at 16–24.

398. If the above identified amendments were in fact inherent, as Netlist now contends to overcome intervening rights, then Gail Sasaki, Mehran Arjomand, and David S. Kim knowingly misled the PTAB and the Federal Circuit when it distinguished the amended claims from the prior art during reexamination.

399. Had the PTAB and the Federal Circuit known that the amendments were in fact not "narrowing" but instead just "made express the inherent functions of the [original limitation]," the PTAB and the Federal Circuit would have found these claims obvious and not allowed them to issue. For example, if the newly added functions were inherent in the original claim limitation, as Netlist now contends, these functions also would have been inherent in the prior art, thus rendering the claims obvious and invalid.

400. On information and belief, at the direction of Gail Sasaki, Mehran Arjomand and David S. Kim knowingly misrepresented the amendments in its arguments to the PTAB and the Federal Circuit. Mehran Arjomand and David S. Kim had a duty of candor and good faith in dealing with the PTAB and the Federal Circuit during reexamination of the '912 patent. That duty of candor and good faith included a duty to disclose to the PTAB and the Federal Circuit any intention *not* to narrow the claims at all in order to distinguish the prior art. Instead, Mehran Arjomand and David S. Kim chose to tell both the PTAB and the Federal Circuit the opposite to convince the PTAB and the Federal Circuit to allow the claims. This information is material to the patentability of the claims. By misrepresenting the intended effect of the above identified amendments to the claims to the PTAB and the Federal Circuit, Mehran Arjomand and David S. Kim, at the direction of Gail Sasaki, breached their duty of candor and good faith and showed specific intent to deceive the PTAB and the Federal Circuit.

401. On information and belief, Mehran Arjomand and David S. Kim, at the direction of Gail Sasaki, engaged in this conduct as part of a scheme to monetize Netlist's patents through litigation against the industry.

* * * *

402. Inequitable Conduct: Any one or more acts set forth above are sufficient in and of itself/themselves to demonstrate that Netlist committed inequitable conduct during the reexamination of the ’912 patent that renders the ’912 patent unenforceable.

403. Unclean Hands: Furthermore, any one or more acts set forth above are sufficient in and of itself/themselves to demonstrate that Netlist has unclean hands in relation to its assertion of the ’912 patent that renders the ’912 patent unenforceable.

COUNT XI
(Declaration of Unenforceability of the ’506 Patent Due to Inequitable Conduct & Unclean Hands)

404. Samsung restates and incorporates by reference the preceding paragraphs as if fully set forth herein.

A. Background on the Alleged Invention, and the Prosecution of the ’506 Patent, and Events Occurring During the Same

405. The ’506 patent issued from a series of continuation applications: U.S. Patent Application Nos. 15/820,076 (U.S. Patent No. 10,268,608); 15/426,064 (U.S. Patent No. 9,824,035); 14/846,993 (U.S. Patent No. 9,563,587); and 13/952,599 (U.S. Patent No. 9,128,632). This chain of continuation applications ultimately claims priority to U.S. Provisional Patent Application No. 61/676,883, which was filed on July 27, 2012. All of the applications name Hyun Lee and Jayesh R. Bhakta as the inventors.

406. The ’506 patent incorporates by reference a number of Netlist’s other patent applications including U.S. Patent Application Nos. 14/715,486 (U.S. Patent No. 9,858,821); 13/970,606 (U.S. Patent No. 9,606,907); 12/504,131 (U.S. Patent No. 8,417,870); 12/761,179 (U.S. Patent No. 8,516,185); 13/287,042 (U.S. Patent No. 8,756,364); and 13/287,081 (U.S. Patent No. 8,516,188).

407. Netlist filed a terminal disclaimer for the ’506 patent on April 10, 2020, over the ’608, ’035, ’587, and ’632 patents.

1. Hyun Lee’s and Jayesh Bhakta’s Alleged Conception and Reduction to Practice, and Regular Attendance at JEDEC Meetings

408. Hyun Lee continued to regularly attend JEDEC meetings for at least the JC-40 committee and the JC-45 committee in 2011 and 2012, as well as before and after that timeframe. For instance, on information and belief, Hyun Lee attended at least the following JC-40 meetings: No. 168, Dec. 8, 2011; No. 169, Mar. 5, 2012; and No. 170, June 4, 2012. And, on information and belief, Hyun Lee attended at least the following JC-45 meetings: No. 33, Dec. 7-8, 2011; No. 34, Mar. 5, 2012; and No. 35, June 4, 2012.

409. By virtue of his attendance at those meetings, active involvement in JEDEC and otherwise, on information and belief, Hyun Lee was aware of the draft and final specifications for DDR4 LRDIMMs being considered and voted upon by those committees, including JESD82-32, dated November 2016, as well as prior drafts of it. For example, Intel presented and discussed Committee Item Number 158.01 (“DDR4 LRDIMM Proposal”) at the December 8, 2011 meeting of JC-40, Committee Item Number 0311.14 (“Proposed DDR4 DB Training Modes”) at the March 25, 2012 meeting of JC-40, and Committee Item Number 0311.12 (“Proposed DDR DB Buffer Control Words”) at the June 4, 2012 meeting of JC-40.

410. A true and correct copy of JESD82-32 is attached as Exhibit 10. On information and belief, this standard was circulated at or before, and discussed at and voted on at or before, JC-40 and JC-45 committee meetings that Hyun Lee attended.

411. A true and correct copy of Committee Item Number 158.01 from the December 2011 meeting is attached as Exhibit 42. On information and belief, this draft was created

by employees of Intel Corp. and circulated at or before, and discussed at, the JC-40 committee meeting on December 8, 2011 that Hyun Lee attended.

412. A true and correct copy of Committee Item Number 0311.14 from the March 2012 meeting is attached as Exhibit 43. On information and belief, this draft was created by employees of Intel Corp. and circulated at or before, and discussed at, the JC-40 committee meeting on Mar. 5, 2012 that Hyun Lee attended.

413. A true and correct copy of Committee Item Number 0311.12 from the June 2012 meeting is attached as Exhibit 44. On information and belief, this draft was created by employees of Intel Corp. and circulated at or before, and discussed at, the JC-40 committee meeting on June 4, 2012 that Hyun Lee attended.

414. By virtue of his attendance at those meetings, active involvement in JEDEC and otherwise, on information and belief, Hyun Lee was aware of the draft and final specifications for DDR4 LRDIMMs being considered and voted upon by those subcommittees.

415. Draft specifications, ballots and presentations distributed to the members of the JC-40 and/or JC-45 committees of JEDEC were distributed to many (20+) key members of the interested public with the expectation they would be freely disclosed to and discussed with others. As such, they are prior art under 35 U.S.C. § 102 at least as of those distribution dates.

416. Distributed specifications, such as JESD82-32, are prior art under 35 U.S.C. § 102 at least as of their release dates.

417. The provisional application to which the ’506 patent claims priority was filed on July 12, 2012, naming Hyun Lee as the inventor. Jayesh R. Bhakta was named as a co-inventor after the provisional was filed.

418. On information and belief, and based on Netlist's apparent view of the scope of the alleged invention, each of the draft DDR4 LRDIMM drafts and presentations disclose materially the same structure and functionality that Netlist accuses of infringing the claims of '506 patent.

419. On information and belief, after attending the June 4, 2012 meeting and listening to these ideas from other members of JEDEC, Hyun Lee returned to Netlist and hurriedly completed drafting the provisional application to which the '506 patent claims priority, naming himself as the inventor, and had a provisional application filed on July 27, 2012. Netlist filed a request to correct inventorship on September 26, 2012, adding Jay R. Bhakta as a co-inventor.

2. '506 Patent Prosecution and Corresponding Events

420. Netlist filed the application, No. 16/391,151, that issued as the '506 patent on April 22, 2019.

421. On August 20, 2019, Netlist filed an Information Disclosure Statement (IDS) Form containing seven sheets. JEDEC DDR LRDIMM drafts and specifications were not included.

422. On January 8, 2020, Netlist filed an Information Disclosure Statement (IDS) Form containing twenty-two sheets. The cited references include numerous entire prosecution histories for other Netlist applications. JEDEC DDR LRDIMM drafts and specifications were not included.

423. On January 10, 2020, the examiner issued a Non-Final Rejection rejecting then-pending claim 1 for obviousness-type double patenting and as anticipated by U.S. Patent No. 8,565,033 ("Manoharajah").

424. On April 10, 2020, Netlist filed an Amendment and Request for Reconsideration after Non-Final Rejection. Netlist's response included a Terminal Disclaimer and canceled claim 1. Netlist added claims 2–21.

425. On July 23, 2020, the examiner issued a Notice of Allowance for the application that issued as the '506 patent.

426. On October 16, 2020, Netlist filed an Amendment after Allowance, and on October 22, 2020, Netlist paid the issue fee for the application that issued as the '506 patent.

427. On November 11, 2020, the examiner accepted the Amendment.

428. On November 18, 2020, the examiner issued an issue date notification for the application that issued as the '506 patent. That notification specified an issue date of December 8, 2020.

429. Netlist took no action to withdraw the application that issued as the '506 patent from issuance, or to otherwise continue prosecution of that application, and the application issued as the '506 patent on December 8, 2020.

B. Netlist's Failure to Disclose the Drafts and Presentations for DDR4 LRDIMMs from the Dec. 8, 2011, Mar. 5, 2012, and June 4, 2012 JEDEC JC-40 Meetings Attended by Hyun Lee, and False Portrayal of Hyun Lee and Jayesh R. Bhakta as Inventors.

430. At least according to Netlist's characterizations of the inventive aspects of the disclosure and claims of the '506 patent, the draft specifications and related presentations for DDR4 LRDIMMs that were presented at the Dec. 8, 2011, Mar. 5, 2012, and June 4, 2012 meetings disclose the key allegedly inventive aspects of the claims of the '506 patent. These draft specifications and presentations include Committee Item Number 158.01 from the December 2011 meeting (Ex. 42), Committee Item Number 0311.14 from the March 2012 meeting (Ex. 43), and Committee Item Number 0311.12 from the June 2012 meeting (Ex. 44).

431. Even though at least Hyun Lee was present at the JEDEC meeting at which those presentations were made, witnessed those presentations, and was present for the discussions that occurred about them, and immediately thereafter drafted the provisional application to which the ’506 patent claims priority, on information and belief, Hyun Lee did not disclose any of these drafts and the presentations to the examiner of the application that issued as the ’506 patent.

432. Those drafts and presentations are prior art under 35 U.S.C. § 102 at least as of the meeting in which they were presented and discussed, and are not cumulative of other art or information before the examiner of the application that issued as the ’506 patent.

433. Those drafts and presentations also illustrate that Hyun Lee falsely portrayed himself and Jayesh R. Bhakta as the inventors of the alleged inventions claimed in the ’506 patent. At a minimum, those drafts and presentations illustrate that Hyun Lee, based on Netlist’s infringement allegations, derived at least portions of the allegedly inventive aspects of the claimed inventions from others in attendance at the JC-40 meetings, who made those presentations on behalf of Intel, among others.

434. The Patent Office would not have allowed at least one claim of each of the ’506 patents to issue had it been aware of those drafts and presentations, at least because it would have found the claims obvious over those drafts and presentations (either in combination with the knowledge of one of ordinary skill, in combination with art disclosing the basic architecture and functionality of DDR4 LRDIMMs), that there are joint inventors that were not properly named on the applications that issued as the ’506 patent, and/or that the alleged inventions claimed therein had been derived in whole or in part from another.

435. The drafts and presentations that Hyun Lee failed to disclose to the Patent Office were not cumulative of other art before the examiner. The examiner stated that he allowed the claims because the art of record did not teach or suggest:

> a memory controller system with memory modules having control and address signal lines implemented to be used corresponding to memory read operations to and from memory devices of the memory module that are arranged in multiple ranks with data buffers couple to memory devices, where memory read operations output read data and read strobes associated with memory read operations, and where the data buffer implemented delaying of a first read strobe by a predetermined amount, i.e. generating a delayed read strobe, sampling the first section of read data using the delayed read strobe, and transmitting the section of read data to a data bus, where the predetermined amount of delay is based at least on signals received by the data buffer [during one or more previous operations] as claimed.

Notice of Allowability at 3–4. The withheld drafts and presentations for DDR4 LRDIMM explained the structure and operation of DDR4 LRDIMM devices, which Netlist argues practice the claims of the ’506 patent. For example, Committee Item Number 158.01 (Ex. 42), shows the accused DDR4 LRDIMM’s structure, which Netlist argues includes the claimed “memory devices of the memory module that are arranged in multiple ranks with data buffers couple to memory device.” Ex. 42 at 2. Moreover, the draft specifications explain DDR LRDIMM’s training modes including “Read Delay Training.” *See, e.g.*, Ex. 43 (Committee Item No. 311.14) at 8–9. Netlist argues that these training modes are used to determine the claimed “predetermined amount.”

436. On information and belief, Hyun Lee specifically intended to deceive the Patent Office into believing that Hyun Lee and Jayesh R. Bhakta were the sole inventors of the ’506 patent, and/or that the claims of those patents are otherwise patentable, by withholding those drafts and presentations from the patent examiner during prosecution of the application that issued as the ’506 patents. On information and belief, Hyun Lee engaged in this conduct as part of a scheme to monetize Netlist’s patents through litigation against the industry.

* * * *

437. Inequitable Conduct: Any one or more acts set forth above are sufficient in and of itself/themselves to demonstrate that Netlist committed inequitable conduct during the prosecution of the ’506 patent that renders the ’506 patent unenforceable.

438. Unclean Hands: Furthermore, any one or more acts set forth above are sufficient in and of itself/themselves demonstrated that Netlist has unclean hands in relation to its assertion of the ’506 patent that renders the ’506 patent unenforceable.

COUNT XII
(Breach of Contract)

439. Samsung restates and incorporates by reference the preceding paragraphs as if fully set forth herein.

440. Under the JEDEC Patent Policy, Netlist has a contractual commitment to offer implementers of the JEDEC Standards, including Samsung, licenses to any Essential Patent Claims (as defined in the JEDEC Patent Policy) on RAND terms and conditions. This contractual commitment is on-going. Netlist continues to have an obligation to license its SEPs to Samsung on RAND terms, notwithstanding any breach of the Agreement or any termination of the license contained therein. Having entered the Agreement, Netlist cannot dispute Samsung is a willing licensee.

441. Netlist submitted Letters of Assurance to the JC-40, JC-42, and JC-45 committees in which Netlist promised to make available to implementers of the DDR4 Standards a license to the ’434, ’837, ’632, ’185, ’870, ’831, and ’833 patents “under reasonable terms and conditions that are demonstrably free of any unfair discrimination.” Ex. 13 (’434 LOA); Ex. 14 (’837 LOA); Ex. 20 (’632 LOA); Ex. 21 (12/761,179 LOA); Ex. 22 (12/504,131 LOA); Ex. 25 (’831 LOA); Ex. 26 (’833 LOA). Under the JEDEC Patent Policy, those commitments extend to the ’523, ’595, ’218, ’506, and ’339 patents, to the extent they are essential to the DDR4 Standards.

442. On information and belief, Netlist failed to specifically disclose the ’912 patent as potentially essential to the DDR4 Standards. Notwithstanding this failure, the JEDEC Patent Policy requires Netlist, as a member of or participant in the committee that developed the DDR4 Standards, to license the ’912 patent on RAND terms to the extent it is essential to those Standards.

443. On information and belief, Netlist also failed to specifically disclose the ’918 patent as potentially essential to the DDR5 Standards. Notwithstanding this failure, the JEDEC Patent Policy requires Netlist, as a member of or participant in the committee that developed the DDR5 Standards, to license the ’918 patent on RAND terms to the extent it is essential to those Standards.

444. On information and belief, Netlist also failed to specifically disclose the ’019 application as potentially essential to the DDR5 Standards. Notwithstanding this failure, the JEDEC Patent Policy requires Netlist, as a member of or participant in the committee that developed the DDR5 Standards, to license the ’019 application, and any patent issuing therefrom, on RAND terms to the extent it is essential to those Standards.

445. The JEDEC Patent Policy and/or Letters of Assurance constitute a valid and binding contract between Netlist and JEDEC.

446. Samsung is a third-party beneficiary to the JEDEC Patent Policy and/or Letters of Assurance, and to Netlist’s RAND obligations thereunder. Participation in JEDEC committees and the standard-setting process is expressly conditioned on a commitment to license essential patents to third-party implementers on RAND terms. Ex. 12 (JEDEC Manual No. 21T) § 8.2.2.1. The JEDEC Patent Policy is therefore intended to benefit third-party implementers of JEDEC standards, such as Samsung, and the obligations under the JEDEC Patent Policy, including

the RAND obligations, are intended to be enforceable by third-party implementers of the JEDEC standards. Third-party implementers, such as Samsung, are also the only parties who could recover for Netlist's breach of its obligations under the JEDEC Patent Policy.

447. Samsung has relied on the JEDEC Patent Policy and/or Letters of Assurance, including the RAND obligations set forth therein, in designing, manufacturing, and selling standard-compliant products, including the Samsung Memory Modules, and Samsung has supported the JEDEC standard based on its understanding and expectation that JEDEC members, including Netlist, will abide by their obligations.

448. In ongoing litigation, Netlist and Samsung dispute whether Samsung has a license to Netlist's patents, including the Patents-in-Suit, under the Agreement. Netlist has taken the position that Samsung's license under the Agreement has been terminated, while Samsung maintains that the termination was not effective and that it has a license to the Patents-in-Suit. In any event, Netlist has failed to offer Samsung a license to patents that Netlist alleges are essential to the JEDEC Standards, including the Patents-in-Suit, on RAND terms and conditions. To the extent the Patents-in-Suit or any other Netlist patents are essential to any of the JEDEC Standards (which Samsung submits they are not), Netlist has breached its contractual obligations to license such patents to Samsung on RAND terms and conditions.

449. To the extent the '912 patent is essential to any of the DDR4 Standards, Netlist has also breached its RAND obligations by seeking an injunction against Google in connection with its use of certain Samsung memory modules that are alleged to infringe the '912 patent.

450. Netlist also breached its contractual obligations by filing the Texas Infringement Action without notifying Samsung of the asserted patents, describing the alleged infringement, or making any good-faith RAND offer.

451. As a result of Netlist's breaches of contract, Samsung has been injured in its business or property because it has been denied access to a license to Netlist's claimed SEPs on RAND terms, a license that can only be obtained from Netlist. Netlist's conduct threatens Samsung with imminent loss of customers and potential customers, loss of goodwill and product image, loss of sales, litigation costs, uncertainty in business planning, and uncertainty among customers and potential customers.

JURY DEMAND

Samsung demands a jury trial on all issues and claims so triable.

PRAYER FOR RELIEF

WHEREFORE, Samsung prays for judgment and relief as follows:

(a) Declare that Samsung does not directly or indirectly infringe the '523 patent, either literally or under the doctrine of equivalents, and that it is not liable for damages or injunctive relief based on any claim in the '523 patent;

(b) Declare that Samsung does not directly or indirectly infringe the '595 patent, either literally or under the doctrine of equivalents, and that it is not liable for damages or injunctive relief based on any claim in the '595 patent;

(c) Declare that Samsung does not directly or indirectly infringe the '218 patent, either literally or under the doctrine of equivalents, and that it is not liable for damages or injunctive relief based on any claim in the '218 patent;

(d) Declare that Samsung does not directly or indirectly infringe the ’912 patent, either literally or under the doctrine of equivalents, and that it is not liable for damages or injunctive relief based on any claim in the ’912 patent;

(e) Declare that Samsung does not directly or indirectly infringe the ’506 patent, either literally or under the doctrine of equivalents, and that it is not liable for damages or injunctive relief based on any claim in the ’506 patent;

(f) Declare that Samsung does not directly or indirectly infringe the ’339 patent, either literally or under the doctrine of equivalents, and that it is not liable for damages or injunctive relief based on any claim in the ’339 patent;

(g) Declare that Samsung does not directly or indirectly infringe the ’918 patent, either literally or under the doctrine of equivalents, and that it is not liable for damages or injunctive relief based on any claim in the ’918 patent;

(h) Declare that the ’523 patent is unenforceable due to inequitable conduct and unclean hands;

(i) Declare that the ’595 patent and ’218 patent are unenforceable due to inequitable conduct and unclean hands;

(j) Declare that the ’912 patent is unenforceable due to inequitable conduct and unclean hands;

(k) Declare that the ’506 patent is unenforceable due to inequitable conduct and unclean hands;

(l) Declare that Netlist is liable for breach of contract;

(m) Grant injunctive relief requiring Netlist to offer a license to the patents it asserts are essential or potentially essential to the JEDEC standards—

including the Patents-in-Suit—on reasonable terms and conditions that are demonstrably free from any unfair discrimination;

(n) Enjoin Netlist from further demanding excessive, non-RAND royalties from Samsung;

(o) Declare that Netlist is barred from seeking and/or enforcing injunctive relief against Samsung (including its affiliates) or its direct or indirect customers and end-users in any jurisdiction with respect to any alleged infringement of any patent essential to JEDEC standards;

(p) Enjoin Netlist from seeking and/or enforcing injunctive relief against Samsung (including its affiliates) or its direct or indirect customers and end-users in any jurisdiction with respect to any alleged infringement of any patents essential to JEDEC standards;

(q) Compensate Samsung for all damages caused by Netlist's breaches of contract, including breaches of its RAND obligations;

(r) Declare that judgment be entered in favor of Samsung and against Netlist on each of Samsung's claims;

(s) Find that this is an exceptional case under 35 U.S.C. § 285;

(t) Award Samsung pre-judgment and post-judgment interest;

(u) Award Samsung its costs and attorneys' fees in connection with this action; and

(v) Such further and additional relief as the Court deems just and proper.

MORRIS, NICHOLS, ARSHT & TUNNELL LLP

/s/ Rodger D. Smith II

Jack B. Blumenfeld (#1014)
Rodger D. Smith II (#3778)
1201 North Market Street
P.O. Box 1347
Wilmington, DE 19899
(302) 658-9200
jblumenfeld@morrisnichols.com
rsmith@morrisnichols.com

Attorneys for Plaintiffs

OF COUNSEL:

Brian Nester
COVINGTON & BURLING LLP
One CityCenter
850 Tenth Street, NW
Washington, DC 20001-4956
(202) 662-6000

Alice J. Ahn
COVINGTON & BURLING LLP
Salesforce Tower
415 Mission Street, Suite 5400
San Francisco, CA 94105-2533
(415) 591-6000

January 18, 2022

CERTIFICATE OF SERVICE

I hereby certify that on January 18, 2022, I caused the foregoing to be electronically filed with the Clerk of the Court using CM/ECF, which will send notification of such filing to all registered participants.

I further certify that I caused copies of the foregoing document to be served on January 18, 2022, upon the following in the manner indicated:

Karen E. Keller, Esquire
Andrew E. Russell, Esquire
Nathan R. Hoeschen, Esquire
SHAW KELLER LLP
I.M. Pei Building
1105 North Market Street, 12th Floor
Wilmington, DE 19801
Attorneys for Defendant

VIA ELECTRONIC MAIL

/s/ Rodger D. Smith II

Rodger D. Smith II (#3778)