

DECLARATION OF NATHANIEL E FRANK-WHITE

I, NATHANIEL E FRANK-WHITE, declare as follows:

1. I have personal knowledge of the facts set forth herein, and if called to testify, I could and would competently testify to the same.

2. I am a Records Request Processor at the Internet Archive. I make this declaration of my own personal knowledge.

3. The Internet Archive is a website that provides access to a digital library of Internet sites and other cultural artifacts in digital form. Like a paper library, we provide free access to researchers, historians, scholars, and the general public. The Internet Archive has partnered with and receives support from various institutions, including the Library of Congress.

4. The Internet Archive has created a service known as the Wayback Machine. The Wayback Machine makes it possible to browse more than 450 billion pages stored in the Internet Archive's web archive. Visitors to the Wayback Machine can search archives by URL (i.e., a website address). If archived records for a URL are available, the visitor will be presented with a display of available dates. The visitor may select one of those dates, and begin browsing an archived version of the Web. Links on archived files in the Wayback Machine point to other archived files (whether HTML pages or other file types), if any are found for the URL indicated by a given link. For instance, the Wayback Machine is designed such that when a visitor clicks on a hyperlink on an archived page that points to another URL, the visitor will be served the archived file found for the hyperlink's URL with the closest available date to the initial file containing the hyperlink.

5. The archived data made viewable and browseable by the Wayback Machine is obtained by use of web archiving software that automatically stores copies of files available via the Internet, each file preserved as it existed at a particular point in time.

6. The Internet Archive assigns a URL on its site to the archived files in the format http://web.archive.org/web/[Year in yyyy][Month in mm][Day in dd][Time code in hh:mm:ss]/[Archived URL] aka an "extended URL". Thus, the extended URL http://web.archive.org/web/19970126045828/http://www.archive.org/ would be the URL for the record of the Internet Archive home page HTML file (http://www.archive.org/) archived on January 26, 1997 at 4:58 a.m. and 28 seconds (1997/01/26 at 04:58:28). The date indicated by an extended URL applies to a preserved instance of a file for a given URL, but not necessarily to any other files linked therein. Thus, in the case of a page constituted by a primary HTML file and other separate files (e.g., files with images, audio, multimedia, design elements, or other embedded content) linked within that primary HTML file, the

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primary HTML file and the other files will each have their own respective extended URLs and may not have been archived on the same dates.

7. Attached hereto as Exhibit A are true and accurate copies of screenshots of the Internet Archive's records of the archived files for the URLs and the dates specified in the attached coversheet of each printout.

8. I do hereby declare and state, that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

DATE: August 5, 2022

Nathaniel E Frank-White

Nathaniel E Frank-White

EXHIBIT A

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2009 Meetings Schedule

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January, 2009

Dates	Event/Committee	Location	Accommodations	Info
Jan 8	Flash Memory, The Future of Consumer Products	Las Vegas, NV, Consumer Electronics Show		◆
Jan 12-Jan 15	JC-13	Jacksonville, FL	Crowne Plaza Jacksonville Riverfront	◆
Jan 20-Jan23	JC-14	Las Vegas, NV	Tuscany Suites & Casino	◆
Jan 21-Jan 22	JC-11	Las Vegas, NV	The Flamingo	◆

February, 2009

Dates	Event/Committee	Location	Accommodations	Info
Feb 2-Feb 3	Board of Directors	Miami, FL	Marriott Biscayne Bay	◆
Feb 23-Feb 27	JC-16, 40, 42, 45, 63, 64	Tokyo, Japan	Hilton Tokyo Online Reservations	◆

March, 2009

Dates	Event/Committee	Location	Accommodations	Info
Mar 3-Mar 5	International Lead Free Conference	Santa Clara, CA	Marriott Santa Clara	◆
Mar 17-Mar 18	JC-25	Irvine, CA	Microsemi	
Mar 20-Mar 21	JC-15	San Jose, CA	Holiday Inn San Jose	
Mar 31	Flash Storage Summit	Shanghai, China	Courtyard Marriott Shanghai-Pudong	

April, 2009

Dates	Event/Committee	Location	Accommodations	Info
Apr 2	Flash Storage Summit	Taipei, Taiwan	Grand Formosa Regent	
Apr 6-Apr 7	Flash Storage Summit	San Jose, CA	Marriott Santa Clara	
Apr 15-Apr 16	JC-11	Austin, TX	Intercontinental Austin	◆
Apr 28-Apr 29	JC-22	Scottsdale, AZ	Hilton Garden Inn Scottsdale Old Town	◆
Apr 30-May 1	JC-14	Montreal	CANCELLED	

May, 2009

Dates	Event/Committee	Location	Accommodations	Info
May 4-May 5	Board of Directors	Santa Clara, CA	Hilton Santa Clara	◆
May 18-May 21	JC-13	Kansas City, MO	Kansas City Marriott Downtown	◆
May 20	JC-14	Tampa, FL	Marriott Tampa	

June, 2009

Dates	Event/Committee	Location	Accommodations	Info
Jun1-Jun 5	JC-16, 40, 42, 45, 63, 64	Montreal, CD	Omni Mont-Royal	◆
Jun 23-Jun 25	JC-14	Williamsburg, VA	Woodlands Hotel & Suites	◆

July, 2009

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Dates	Event/Committee	Location	Accommodations	Info
Jul 22-Jul 23	JC-11	Minneapolis, MN	Millennium Minneapolis	

August, 2009

Dates	Event/Committee	Location	Accommodations	Info
Aug 3-Aug 4	Board of Directors	Vancouver, Canada	Renaissance Harbourside	

September, 2009

Dates	Event/Committee	Location	Accommodations	Info
Sep 7-Sep 11	JC-16, 40, 42, 45, 63, 64	tbd		
Sept 22- Sept 25	JC-14	Seattle, WA	Crowne Plaza Online reservations	
Sept 21-Sept 24	JC-13	Columbus, OH	The Columbus	

October, 2009

Dates	Event/Committee	Location	Accommodations	Info
Oct 7-Oct 8	JC-11	Salt Lake City, UT	Hilton Salt Lake City Center	
Oct 11	ROCS	Greensboro, NC		
Oct 13-Oct 14	JC-25	Clearwater, FL	Hilton Clearwater Beach	
Oct tbd	JC-14	Tahoe, CA	IRW	

November, 2009

Dates	Event/Committee	Location	Accommodations	Info
Nov 2-Nov	Board of Directors	Alexandria, VA	Hilton Alexandria Mark Center	
Nov 17-Nov 18	JC-22	Ft. Lauderdale, FL	Lago Mar	

December, 2009

Dates	Event/Committee	Location	Accommodations	Info
Dec 7-Dec 11	JC-16, 40, 42, 45, 63 & 64	Maui, HI	Grand Wailea	

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Document Type

NUMBER	JEDEC Engineering Bulletins (JEB)	PRICE
JEB 5-A	METHODS OF MEASUREMENT FOR SEMICONDUCTOR LOGIC GATING MICROCIRCUITS: The purpose of this bulletin is to recommend for use in the rating of semiconductor logic gating microcircuits which use the binary states to represent and process logic information. Both static and dynamic measurements are covered. January 1970; Reaffirmed February 1984 /JEDEC Committee	$63.00
JEB 6	STANDARD MEASURMENTS OF THE ELECTRICAL CHARACTERISTICS OF SEMICONDUCTOR INTEGRATED CIRCUITS December 1966; Rescinded October 1984 / Committee!33JCJEDC	
JEB 15	TERMINOLOGY AND METHODS OF MEASUREMENT FOR BISTABLE SEMICONDUCTOR MICROCIRCUITS: This bulletin explains the terminology and methods of measurement for bistable semiconductor microcircuits. It is also intended to be used with the EIA Registration Data Format for semiconductor integrated bistable logic circuits. November 1969 /JC-40 Committee	$109.00
JEB 16	USER GUIDE FOR MICROCIRCUIT FAILURE ANALYSIS: This guide defines generalized procedures for the failure analysis of monolithic integrated microelectronic circuits. Although the generalized procedural steps may apply to all microelectronic circuits, additional analysis steps unique to thin/thick film hybrid devices are not covered. July 1970; Rescinded November 2004 September 2003 /JC-14 Committee	$41.00
JEB 17	USER GUIDELINES FOR QUALITY AND RELIABILITY ASSURANCE OF LSI COMPONENTS November 1970; Rescinded April 1987 April 1987	
JEB 19	RECOMMENDED CHARACTERIZATION OF MOS SHIFT REGISTERS: This recommendation applies to MOS Shift Registers. Definitions are given for P-channel registers but are applicable to all CMOS and N-channel with changes in power supply notation. November 1972 /JC-40 Committee	$40.00
JEB 20	ACCEPTED PRACTICES FOR MAKING MICROELECTRONIC DEVICE THERMAL CHARACTERISTICS TESTS January 1975; Rescinded November 1988 /JC-11 Committee	

NUMBER	Tentative Standards (TENTSTD)	PRICE
TENTSTD 11	HANDLING AND INSTALLATION OF POWER SEMICONDUCTORS IN DISC TYPE PACKAGES: Included in JESD282 and EIA397. July 1973; Rescinded June 1992 June 1992 /JC-22.2 Subcommittee	
TENTSTD 12	STANDARD FOR SELENIUM SURGE SUPPRESSORS: The suppresser furnished under this standard shall be a product that has been tested and meets the definitions and minimum requirements specified herein. November 1973 /JC-22.5 Subcommittee	$49.00

NUMBER	JEDEC Specifications (JES)	PRICE
JES 2	TRANSISTOR, GALLIUM ARSENIDE POWER FET, GENERIC SPECIFICATION: Establishes guideline requirements and quality assurance provisions for gallium arsenide power field-effect transistors (FETs, also know as MESFETs) designed for use in high-reliability space application such as spacecraft communications transmitters. Identifies the electrical parameters, wafer acceptance tests, screening tests, qualification tests, and lot acceptance tests pertinent to power GaAs FETs. Applicable to packaged and chip-carrier parts; portions may not be applicable to unpackaged and unmounted chips. July 1992 /JC-14.7 Subcommittee	$71.00

NUMBER	JEDEC Standards (JESD)	PRICE
JESD 1	LEADLESS CHIP CARRIER PINOUTS STANDARDIZED FOR LINEARS: This standard shows how to convert existing DIP pinouts for op-amps, comparators, and D/A converters, to chip carrier packages. April 1982 / Committee!33JC41	$41.00
JESD 15	THERMAL MODELING OVERVIEW This document and the associated series of documents are intended to promote the continued development of modeling methods, while providing a coherent framework for their use by defining a common vocabulary to discuss modeling, creating requirements for what information should be included in a thermal modeling report, and specifying modeling procedures, where appropriate, and validation methods. This	

	document provides an overview of the methodology necessary for performing meaningful thermal simulations for packages containing semiconductor devices. The actual methodology components are contained in separate detailed documents. October 2008 March 2006 /JC-15.1 Subcommittee	$47.00
JESD 15-1	COMPACT THERMAL MODEL OVERVIEW This document should be used in conjunction with the master document, JESD15, and JESD15-2, and subsidiary documents as they become available. This document is intended to function as an overview to support the effective use of Compact Thermal Model (CTM) methodologies as specified in the companion methods documents. At present, there are two such documents; JESD15-3, and JESD15-4. October 2008 October 2006 /JC-15.1 Subcommittee	$51.00
JESD 15-4	DELPHI COMPACT THERMAL MODEL GUIDELINE This guideline specifies the definition and lists acceptable approaches for constructing a compact thermal model (CTM) based on the DELPHI methodology. The purpose of this document is twofold. First, it aims to provide clear guidance to those seeking to create DELPHI compact models of packages. Second, it aims to provide users with an understanding of the methodology by which they are created and validated, and the issues associated with their use. October 2008 March 2006 /JC-15 Committee	$62.00
JESD 2	DIGITAL BIPOLAR LOGIC PINOUTS FOR CHIP CARRIERS: This standard provides a chip carrier format for digital devices by defining pin functions and locations for 20, 38, 44, 52, and 68-terminal devices. December 1982 /JC-40.1 Subcommittee	$41.00
JESD 3-C	STANDARD DATA TRANSFER FORMAT BETWEEN DATA PREPARATION SYSTEM AND PROGRAMMABLE LOGIC DEVICE PROGRAMMER: This standard was developed to prevent the proliferation of data transfer formats that occurred with microprocessor development systems. The focus of the standard is on field programmable devices and their support tools. It is not intended for other types of semicustom logic devices or other types of fabrication or testing equipment. June 1994 / Committee!33JC421	$61.00
JESD 4	DEFINITION OF EXTERNAL CLEARANCE AND CREEPAGE DISTANCES OF DISCRETE SEMICONDUCTOR PACKAGES FOR THYRISTORS AND RECTIFIER DIODES: This standard defines reference distances between terminals of the device and the external package at specific voltages. November 1983; Reaffirmed January 1991, April 1999, April 2002 April 2002 /JC-22.2 Subcommittee	$38.00
JESD 5	MEASUREMENT OF TEMPERATURE COEFFICIENT OF VOLTAGE REGULATOR DIODES: This standard is designed to define voltage-temperature characteristic measurement techniques and a method of calculation. Although many methods could be defined, this method provides a desired uniformity and lends itself to production testing. Formerly JEDEC Suggested Standard No. 5A February 1982; Reaffirmed April 1999, April 2002 April 2002 /JC-22.4 Subcommittee	$38.00
JESD 6	MEASUREMENT OF SMALL VALUES OF TRANSISTOR CAPACITANCE: This standard gives a test method for measuring transistor capacitance using a three-terminal bridge which employs a guard-circuit that eliminates the effect of extraneous capacitance. February 1967; Reaffirmed September 1981, April 1999, October 2002 /JC-25 Committee	$47.00
JESD 7-A	STANDARD FOR DESCRIPTION OF 54/74HCXXXX AND 54/74HCTXXXX HIGH SPEED CMOS DEVICES: This standard provides uniformity, multiplicity of sources, eliminate confusion, and ease of device specification and design by users for HC, and HCT CMOS devices. This standard specifies electrical parameters. It also includes appendices listing part numbers. August 1986 / Committee!33JC402	$109.00
JESD 8- 1	ADDENDUM No. 1 to JESD8: INTERFACE STANDARD FOR LOW VOLTAGE TTL-COMPATIBLE (LVTTL) VLSI DIGITAL CIRCUITS June 1994; Incorporated into JESD8-A, June 1994. JESD8-A was replaced by JESD8-B, September 1999. /JC-16 Committee	
JESD 8- 1-A	INTERFACE STANDARD FOR NOMINAL 0.3 V/3.3 V SUPPLY DIGITAL INTEGRATED CIRCUITS June 1994; Incorporated into JESD8-A, June 1994. JESD8-A was replaced by JESD8-B, September 1999. /JC-16 Committee	
JESD 8- 2	ADDENDUM No. 2 to JESD8 - STANDARD FOR OPERATING VOLTAGES AND INTERFACE LEVELS FOR LOW VOLTAGE EMITTER-COUPLED LOGIC (ECL) INTEGRATED CIRCUITS: This Addendum No. 2 to JEDEC Standard No. 8 provides standard operating voltage and interface levels that can be used by designers and application engineers as they develop and introduce new products. Covers the ECL logic family designated 300K ECL. The 300K ECL family is Voltage and Temperature Compensated, with I/O interface levels compatible with the existing 100K ECL and 101K ECl families. March 1993 /JC-16 Committee	$40.00
JESD 8- 3A	ADDENDUM No. 3A to JESD8 - GUNNING TRANSCEIVER LOGIC (GTL) LOW-LEVEL, HIGH-SPEED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS: This Addendum No. 3 to JEDEC Standard No. 8 defines the dc input and output specifications for a low-level, high-speed interface for integrated devices. May 2007 December 2006 /JC-16 Committee	$40.00

JESD 8- 4	ADDENDUM No. 4 to JESD8 - CENTER-TAP-TERMINATED (CTT) INTERFACE LOW-LEVEL, HIGH-SPEED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS: This Addendum No. 4 to JEDEC Standard No. 8 defines the dc input and output specifications for a low-level, high-speed interface for integrated devices that can be a super-set of LVCMOS and LVTTL. November 1993 /JC-16 Committee	$38.00
JESD 8- 5A.01	ADDENDUM No. 5 to JESD8 - 2.5 V 0.2 V (NORMAL RANGE), AND 1.8 V TO 2.7 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUIT: This standard defines power supply voltage ranges, dc interface parameters for a high speed, low voltage family of non-terminated digital circuits driving/driven by parts of the same family. The specifications in this standard represent a minimum set of 'base line' set of interface specifications for CMOS-compatible circuits. September 2007 September 2004 /JC-16 Committee	$43.00
JESD 8- 6	ADDENDUM No. 6 to JESD8 - HIGH SPEED TRANSCEIVER LOGIC (HSTL)- A 1.5 V OUTPUT BUFFER SUPPLY VOLTAGE BASED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS: This standard is a 1.5 volt high performance CMOS-based interface document suitable for high I/O count CMOS and BiCMOS devices operating at frequencies in excess of 200 Mhz. August 1995 /JC-16 Committee	$48.00
JESD 8- 7A	ADDENDUM No. 7 to JESD8 - 1.8 V + -0.15 V (NORMAL RANGE), AND 1.2 V - 1.95 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUIT: This standard continues the voltage specification migration to the next level beyond the 2.5 V specification already established. Since this migration is driven by both process changes and performance/power, more entries can be expected in supporting required voltage levels. The rapidity of this evolution is expecting to increase because of the same feature sizes expected. June 2006 June 2004 /JC-16 Committee	$43.00
JESD 8- 8	ADDENDUM No. 8 to JESD8 - STUB SERIES TERMINATED LOGIC FOR 3.3 VOLTS (SSTL_3) A 3.3 V VOLTAGE BASED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS: This standard is a result of a major effort by the JC-16 Committee to develop a high performance CMOS-based interface suitable for high speed main memory applications in excess of 125 MHz. August 1996 /JC-16 Committee	$47.00
JESD 8- 9B	ADDENDUM No. 9B to JESD8 - STUB SERIES TERMINATED LOGIC FOR 2.5 VOLTS (SSTL_2): Includes Errata and Corrected Page 7 as of October 18, 2002. This standard defines the input, output specifications and ac test conditions for devices that are designed to operate in the SSTL_2 logic switching range, nominally 0 V to 2.5 V. The standard may be applied to ICs operating with separate VDD and VDDQ supply voltages. This standard has been developed particularly with the objective of providing a relatively simple upgrade path from MOS push-pull interface designs. The standard is particularly intended to improve operation in situations where busses must be isolated from relatively large stubs. May 2002 /JC-16 Committee	$55.00
JESD 8-11A.01	ADDENDUM No. 11A.01 to JESD8 - 1.5 V +/- 0.1 V (NORMAL RANGE) AND 0.9 - 1.6 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUITS: This new standard provides specifications that will be used by several companies in new 1.5 V products designed in 0.12-0.15 um CMOS technologies, and in components that interface with them. The specifications allow limited interoperability with products using the existing JEDEC HSTL specification (JESD8-6). This version is a minor editorial revision as noted in Annex A. September 2007 June 2004 /JC-16 Committee	$41.00
JESD 8-12A.01	1.2 V +/- 0.1 V (NORMAL RANGE) AND 0.8 - 1.3 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUITS: This standard defines power supply voltage ranges, dc interface and switching parameters for a high speed, low voltage family of nonterminated digital circuits driving/driven by parts of the same family, or mixed families which comply with the input receiver specifications. The specifications in this standard represent a minimum set of interface specifications for CMOS compatible circuits. September 2007 June 2004 /JC-16 Committee	$41.00
JESD 8-13	SCALABLE LOW-VOLTAGE SIGNALING FOR 400 MV (SLVS-400): This standard defines the input, output, and termination specifications for differential signaling in the SLVS-400 environment, nominally between 0 and 400 mV. Power supplies other than the nominal 800 mV power for the SLVS interface are not specified. October 2001 /JC-16 Committee	$41.00
JESD 8-14A.01	1.0 V +/- 0.1 V (NORMAL RANGE) AND 0.7 V - 1.1 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUITS: This new standard provides specifications that will be used by several companies in new 1.0 V products designed in 0.10-0.12 um CMOS technologies, and in components that interface with them. This standard defines power supply voltage ranges, dc interface and switching parameters for a high speed, low voltage family of nonterminated digital circuits driving/driven by parts of the same family, or mixed families which comply with the input receiver specifications. The specifications in this standard represent a minimum set of interface specifications for CMOS compatible circuits. This version is a minor editorial revision as noted in Annex A. September 2007 June 2004 /JC-16 Committee	$41.00
JESD 8-15A	STUB SERIES TERMINATED LOGIC FOR 1.8 V (SSTL_18): This standard defines the input, output specifications and ac test conditions for devices that are designed to operate in the SSTL_18 logic switching range, nominally 0	

V to 1.8 V. The standard may be applied to ICs operating with separate VDD and VDDQ supply voltages. The VDD value is not specified in this standard; however VDD and VDDQ will have the same voltage level in many cases.

September 2003 /JC-16 Committee $49.00

JESD 8-17

DRIVER SPECIFICATIONS FOR 1.8 V POWER SUPPLY POINT-TO-POINT DRIVERS This material is intended to be reflected in supplier specifications for point to point DDR devices ranging from 400 Mb/s to 800 Mb/s operation. It is a method to specify driver impedance with something other than a number that does not nec-essarily define how it operates in a real net This standard addresses this issue using net lengths and specifies how much uncertainty can exist in the data for each speed supported.

November 2004 May 2002 /JC-16 Committee $40.00

JESD 8-18A

FBDIMM SPECIFICATION: HIGH SPEED DIFFERENTIAL PTP LINK AT 1.5 V This specification defines the high-speed differential point-to-point signaling link for FBDIMM, operating at the buffer supply voltage of 1.5V that is provided at the FBDIMM DIMM connector. This specification also applies to FBDIMM host chips which may operate with a different supply voltage. The link consists of a transmitter and a receiver and the interconnect in between them. The transmitter sends serialized bits into a lane and the receiver accepts the electrical signals of the serialized bits and transforms them into a serialized bit-stream. The first generation FBDIMM link is being specified to operate from 3.2 to 4.8 Gb/s. The specifications are defined for three distinct bit-rates of operation: 3.2 Gb/s, 4.0 Gb/s and 4.8 Gb/s.

March 2008 March 2007 /JC-16 Committee $98.00

JESD 8C.01

INTERFACE STANDARD FOR NOMINAL 3.0 V/3.3 V SUPPLY DIGITAL INTEGRATED CIRCUITS: This standard (a replacement of JEDEC Standards No. 8, 8-1, 8-1-A, and 8-A) defines dc interface parameters for a family of digital circuits operating from a power supply of nominal 3.0 V/3.3. V and driving/driven by parts of the same family. The specifications in this standard represent a minimum set of 'base line' set of interface specifications for LVTTL-compatible and LVCMOS-compatible circuits.

September 2007 June 2004 /JC-16 Committee $45.00

JESD 9-A

METAL PACKAGE SPECIFICATION FOR MICROELECTRONIC PACKAGES AND COVERS: This standard establishes the general requirements and quality assurance provisions that can be specified and met in procuring microelectronics packages and covers, manufactured from matched seal with and without high thermal conductivity base materials, intended for use in fabricating hybrid microelectronics circuits. This document details those minimum requirements necessary for metal packages' use exclusively.

April 1987; Under Revision /JC-13.5 Subcommittee $71.00

JESD 10

LOW FREQUENCY POWER TRANSISTORS: This standard consists of a listing of letter symbols, terms, and definitions that are used in power transistors. It also includes information on JEDEC registration procedures, verification tests, and thermal characteristics.

January 1976; Reaffirmed September 1981, October 2002 April 1999 /JC-25 Committee $147.00

JESD 11

CHIP CARRIER PINOUTS STANDARDIZED FOR CMOS 4000, HC AND HCT SERIES OF LOGIC CIRCUITS: This standard indicates the procedures used to convert existing DIP and flat packages for digital parts (SSI & MSI) to chip carrier packages.

December 1984 / Committee!33JC402 $41.00

JESD 12

SEMICUSTOM INTEGRATED CIRCUITS (FORMERLY PUBLISHED AS STANDARD FOR GATE ARRAY BENCHMARK SET): The purpose of these benchmarks is to provide a common set of high level functions which serve as vehicles for comparing the performance of gate arrays implemented in any technology using any internal structure. These benchmarks effectively provide an unbiased measure of gate array vendors' ability to implement a desired complex function on a particular gate array at a known level of performance.

June 1985 / Committee!33JC44 $43.00

JESD 12-1B

ADDENDUM No. 1 to JESD12 - TERMS AND DEFINITIONS FOR GATE ARRAYS AND CELL-BASED INTEGRATED CIRCUITS: The purpose of this standard is to promote the uniform use of abbreviations, terms, and definitions throughout the semiconductor industry. It is a useful guide for users, manufactures, educators, technical writers, and others interested in the characterization, nomenclature, and classification of semicustom integrated circuits.

August 1993 / Committee!33JC44 $48.00

JESD 12-2

ADDENDUM No. 2 to JESD12 - STANDARD FOR CELL-BASED INTEGRATED CIRCUIT BENCHMARK SET: The purpose of these benchmarks is to provide a common set of high level functions that serve as vehicles for comparing the performance of cell-based ICs implemented in any technology using any internal structure. JESD12-2 extends the gate array benchmark set (JESD12) to cell-based ICs.

February 1986 / Committee!33JC44 $61.00

JESD 12-3

ADDENDUM No. 3 to JESD12 - CMOS GATE ARRAY MACROCELL STANDARD: This standard defines a minimum set of macro cell standards for CMOS gate arrays. A total of 41 macro cell types are addressed, all of which are commonly used by gate array designers to implement Application Specific Integrated Circuits.

June 1986 / Committee!33JC44 $47.00

JESD 12-4

ADDENDUM No. 4 to JESD12 - METHOD OF SPECIFICATION OF PERFORMANCE PARAMETERS FOR CMOS SEMICUSTOM INTEGRATED CIRCUITS: This standard defines how to specify various performance parameters of semicustom ICs, including cell and interconnect propagation delays, input/output levels and capacitance, and power dissipation.

April 1987 / Committee!33JC44 $48.00

JESD 12-5	**ADDENDUM No. 5 to JESD12 - DESIGN FOR TESTABILITY GUIDELINES:** This standard is intended to provide circuit designers with the information needed to develop complex integrated circuits that can be reliably and economically tested without compromising flexibility. August 1988 / Committee!33JC44	$109.00
JESD 12-6	**ADDENDUM No. 6 to JESD12 - INTERFACE STANDARD FOR SEMICUSTOM INTEGRATED CIRCUITS:** This standard defines logic interface levels for CMOS, TTL, ECL, and BiCC inputs and outputs. This standard is intended to provide an industry-wide set of specifications, for Application Specific Integrated Circuit (ASIC) signal inputs and outputs, both necessary and sufficient to define a circuits electrical interfacing with the external environment. JESD12-6 is intended to provide the ASIC manufacturer and user with a common set of signal interface levels. The standard defines interface levels for 5 volt operation. March 1991 / Committee!33JC44	$43.00
JESD 13-B	**STANDARD SPECIFICATION FOR DESCRIPTION OF B SERIES CMOS DEVICES:** This standard provides for uniformity, multiplicity of sources, elimination of confusion, and ease of device specifications and system design by users. It gives electrical levels and timing diagrams for B Series CMOS devices. May 1980 / Committee!33JC402	$63.00
JESD 14	**SEMICONDUCTOR POWER CONTROL MODULES:** Semiconductor Power Control Modules (SPCM) are modules consisting of thyristors or transistors, or both, as the primary controlling elements. Methods of manufacture of semiconductor power control modules include the assembling of individual components and the use of semiconductor hybrids or monolithic processing technologies, or both. November 1986; Reaffirmed June 1992, April 1999, April 2002 April 2002 /JC-22.2 Subcommittee	$47.00
JESD 15-3	**TWO-RESISTOR COMPACT THERMAL MODEL GUIDELINE** This document specifies the definition and construction of a two-resistor compact thermal model (CTM) from the JEDEC junction-to-case and junction-to-board thermal metrics. The guidance provided in this document only applies to thermal metrics defined in JEDEC standards JESD51-8 and JESD51-12. The scope of this document is limited to single-die packages that can be effectively represented by a single junction temperature. July 2008 March 2006 /JC-15 Committee	$57.00
JESD 16-A	**ASSESSMENT OF AVERAGE OUTGOING QUALITY LEVELS IN PARTS PER MILLION (PPM):** This standard was revised to clarify assumptions necessary to estimate AOQ, revise the minimum sample size algorithm, address small sample size concerns, and provide methods for combining groups for AOQ estimation. Derivation of any new methods for combing groups for AOQ estimation. Derivation of any new methods introduced into this document have been provided in annexes. A statistical method is based on confidence interval statistics. A procedure was established for reporting AOQ when the minimum sample size criterion is not met. April 1995 Not all sections of EIA-554 are appropriate for use by device manufacturers therefore JEDEC wishes to continue using JESD16A. /JC-13 Committee	$61.00
JESD 17	**LATCH-UP IN CMOS INTEGRATED CIRCUITS - SUPERSEDED BY JESD78, February 1999** August 1988; Rescinded February 1999 February 1999 / Committee!33JC402	
JESD 18-A	**STANDARD FOR DESCRIPTION OF FAST CMOS TTL COMPATIBLE LOGIC:** The purpose of this standard is to provide for uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users. The standard covers specifications for description of '54/74FCTXXXX' series fast CMOS TTL compatible devices. January 1993 / Committee!33JC402	$63.00
JESD 19	**GENERAL STANDARD FOR STATISTICAL PROCESS CONTROL (SPC) - SUPERSEDED by EIA-557-A** July 1988; Rescinded July 1995 /JC-13 Committee	
JESD 20	**STANDARD FOR DESCRIPTION OF 54/74ACXXXXX AND 54/74ACTXXXXX ADVANCED HIGH-SPEED CMOS DEVICES:** This standard describes electrical parameters for this class of CMOS devices. September 1990 / Committee!33JC402	$147.00
JESD 21-C	**CONFIGURATIONS FOR SOLID STATE MEMORIES:** This revision of JESD21 is substantially different from previous issues because it reflects advancement in semiconductor technology and computer design needs. A new class of memory devices, the multiport DRAM (MPDRAM) C also know as 'Video Ram' because of the most common application for the devices C is represented. A new family of SRAMs which addresses the increasing need for high speed is introduced. Additional families of devices in the SOJ and Zip packages are included. The material in this revision is organized primarily by function (ROM, EPROM, SRAM, DRAM, etc.) rather than by technology and word length. Pinouts for SIMM and DIMM are included along with presence detect schemes. A current set of terms has also been included. JESD21-C is a compilation of all memory device standards that have been developed by the JC-42 Committee and approved by the JEDEC BoD from September 1989 to present. This latest issue has changed to a loose-leaf format and comes in a three-ring binder so that new drawings can be added without requiring a new publication. Time of publication of the material is identified by release number, i.e., if marked Release 8, this item was approved and released in 1998, if marked Release 13, this item was approved and released in 2003. May 2003; Under Revision Sections in this document may be under revision at any time. /JC-42 Committee	$150.00
JESD 21-C AUS	**ANNUAL UPDATING SERVICE:** The JEDEC Office has generated a mailing list for those who wish to subscribe to	

updates of this publication. A payment is required for subscription to this updating service.

January 2004 /JC-42 Committee $50.00

JESD 22-A100C

CYCLED TEMPERATURE HUMIDITY BIAS LIFE TEST: The Cycled Temperature-humidity-bias Life Test is performed for the purpose of evaluating the reliability of nonhermetic packaged solid state devices in humid environments. It employs conditions of temperature cycling, humidity, and bias that accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors that pass through it. The Cycled Temperature-Humidity-Bias Life Test is typically performed on cavity packages (e.g., MQUADs, lidded ceramic pin grid arrays, etc.) as an alternative to JESD22-A101 or JESD22-A110.

October 2007 January 2007 /JC-14.1 Subcommittee $49.00

JESD 22-A101C

STEADY-STATE TEMPERATURE HUMIDITY BIAS LIFE TEST: This standard establishes a defined method and conditions for performing a temperature humidity life test with bias applied. The test is used to evaluate the reliability of non-hermetic packaged solid state devices in humid environments. It employs high temperature and humidity conditions to accelerate the penetration of moisture through external protective material or along interfaces between the external protective coating and conductors or other features which pass through it. This revision enhances the ability to perform this test on a device which cannot be biased to achieve very low power dissipation.

March 2009 January 2008 /JC-14.1 Subcommittee $51.00

JESD 22-A102-C

ACCELERATED MOISTURE RESISTANCE - UNBIASED AUTOCLAVE: This test allows the user to evaluate the moisture resistance of nonhermetic packaged solid state devices. The Unbiased Autoclave Test is performed to evaluate the moisture resistance integrity of non-hermetic packaged solid state devices using moisture condensing or moisture saturated steam environments. It is a highly accelerated test which employs conditions of pressure, humidity and temperature under condensing conditions to accelerate moisture penetration through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors passing through it. This test is used to identify failure mechanisms internal to the package and is destructive.

December 2000; Reaffirmed June 2008 /JC-14.1 Subcommittee $38.00

JESD 22-A103C

HIGH TEMPERATURE STORAGE LIFE: The test is applicable for evaluation, screening, monitoring, and/or qualification of all solid state devices. High Temperature storage test is typically used to determine the effect of time and temperature, understorage conditions, for thermally activated failure mechanisms of solid state electronic devices, includingnonvolatile memory devices (data retention failure mechanisms). During the test elevated temperatures(accelerated test conditions) are used without electrical stress applied. This test may be destructive,depending on Time, Temperature and Packaging (if any).

November 2004 June 2004 /JC-14.1 Subcommittee $40.00

JESD 22-A104D

TEMPERATURE CYCLING: This standard provides a method for determining solid state devices capability to withstand extreme temperature cycling. Changes in this revision include requirements that the worst-case load temperature must reach the specific extremes rather than just requiring that the chamber ambient temperature reach the extremes. This ensures that the test specimens will reach the specified temperature extremes regardless of chamber loading. Definitions are provided for Load, Monitoring Sensor, Worst-Case Load Temperature, and Working Zone. The transfer time has been tightened from 5 minutes to 1 minute. Five new test conditions have been added as well as a caution on test conditions which exceed the glass transition temperature of plastic package solid devices.

March 2009 September 2008 /JC-14.1 Subcommittee $57.00

JESD 22-A105C

POWER AND TEMPERATURE CYCLING: The power and temperature cycling test is performed to determine the ability of a device to withstand alternate exposures at high and low temperature extremes and simultaneously the operating biases are periodically applied and removed. It is intended to simulate worst case conditions encountered in application environments. The power and temperature cycling test is considered destructive and is only intended for device qualification. This test method applies to semiconductor devices that are subjected to temperature excursions and required to power on and off during all temperatures.

January 2004 June 2003 /JC-14.1 Subcommittee $40.00

JESD 22-A106B

THERMAL SHOCK: This test is conducted to determine the resistance of a part to sudden exposure to extreme changes in temperature and to the effect of alternate exposures to these extremes.

June 2004 January 2003 /JC-14.1 Subcommittee $40.00

JESD 22-A107B

SALT ATMOSPHERE: This salt Atmosphere test is conducted to determine the resistance of solid state devices to corrosion. It is an accelerated test that simulates the effects of severe seacoast atmosphere on all exposed surfaces. The salt atmosphere test is considered destructive. It is intended for lot acceptance, process monitor, and qualification testing.

January 2004 January 2003 /JC-14.1 Subcommittee $38.00

JESD 22-A108C

TEMPERATURE, BIAS, AND OPERATING LIFE: A revised method for determining the effects of bias conditions and temperature, over time, on solid state devices is now available. Revision B of A108 includes low temperature operating life (LTOL) and high temperature gate bias (HTGB) stress conditions, revised cool down requirements for high temperature stress, and a procedure to follow if parts are not tested within the allowed time window.

June 2005 March 2004 /JC-14.1 Subcommittee $43.00

JESD 22-A109-A

HERMETICITY: This revised test method establishes a standard procedure for determining the effectiveness of

	the seal of hermetically sealed solid state devices. The objective of this revision was to modify the test parameters to reflect current practice and to eliminate the specification of fluorocarbons, banned from use due to environmental concerns. July 2001 /JC-14.1 Subcommittee	$43.00
JESD 22-A110C	**HIGHLY ACCELERATED TEMPERATURE AND HUMIDITY STRESS TEST (HAST)** The purpose of this test method is to evaluate the reliability of nonhermetic packaged solid state devices in humid environments. It employs severe conditions of temperature, humidity, and bias that accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it. January 2009 August 2008 /JC-14.1 Subcommittee	$52.00
JESD 22-A111	**EVALUATION PROCEDURE FOR DETERMINING CAPABILITY TO BOTTOM SIDE BOARD ATTACH BY FULL BODY SOLDER IMMERSION OF SMALL SURFACE MOUNT SOLID STATE DEVICES:** The purpose of this test method is to identify the potential wave solder classification level of small plastic Surface Mount Devices (SMDs) that are sensitive to moisture-induced stress so that they can be properly packaged, stored, and handled to avoid subsequent mechanical damage during the assembly wave solder attachment and/or repair operations. This test method also provides a reliability preconditioning sequence for small SMDs that are wave soldered using full body immersion. This test method, may be used by users to determine what classification level should be used for initial board level reliability qualification. May 2004 June 2000 /JC-14.1 Subcommittee	$47.00
JESD 22-A112-A	**MOISTURE-INDUCED STRESS SENSITIVITY FOR PLASTIC SURFACE MOUNT DEVICES - SUPERSEDED BY J-STD-020A, April 1999.** J-STD-020 is now on revision D. November 1995; Rescinded May 2000 May 2000 /JC-14.1 Subcommittee	
JESD 22-A113F	**PRECONDITIONING OF PLASTIC SURFACE MOUNT DEVICES PRIOR TO RELIABILITY TESTING:** This Test Method establishes an industry standard preconditioning flow for nonhermetic solid state SMDs (surface mount devices) that is representative of a typical industry multiple solder reflow operation. These SMDs should be subjected to the appropriate preconditioning sequence of this document by the semiconductor manufacturer prior to being submitted to specific in-house reliability testing (qualification and reliability monitoring) to evaluate long term reliability (which might be impacted by solder reflow). October 2008 January 2008 /JC-14.1 Subcommittee	$51.00
JESD 22-A114F	**ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY TESTING HUMAN BODY MODEL (HBM):** This test method establishes a standard procedure for testing and classifying microcircuits according to their susceptibility to damage or degradation by exposure to a defined electrostatic Human Body Model (HBM) discharge (ESD). The objective is to provide reliable, repeatable HBM ESD test results so that accurate classifications can be performed. December 2008 January 2008 /JC-14.1 Subcommittee	$57.00
JESD 22-A115-A	**ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY TESTING MACHINE MODEL (MM):** This method establishes a standard procedure for testing and classifying microcircuits according to their susceptibility to damage or degradation by exposure to a defined Machine Model (MM) electrostatic discharge (ESD). The objective is to provide reliable, repeatable MM ESD test results so that accurate classifications can be performed. October 1997 This is a valid test method, however it is not currently being used in the industry, the preferred industry test methods are JESD22A114 or JESD22C101. /JC-14.1 Subcommittee	$45.00
JESD 22-A117B	**ELECTRICALLY ERASABLE PROGRAMMABLE ROM (EEPROM) PROGRAM/ERASE ENDURANCE AND DATA RETENTION TEST:** This method establishes a standard procedure for determining the data cycling endurance and data retention capability of non-volatile memory cells. It is intended as a qualification and monitor test procedure. This test is also applicable to FLASH EEPROM integrated circuits and Erasable Programmable Logic Devices (EPLD) with embedded EEPROM or FLASH memory. March 2009 September 2008 /JC-14.3 Subcommittee	$60.00
JESD 22-A118	**ACCELERATED MOISTURE RESISTANCE - UNBIASED HAST:** The Unbiased HAST is performed for the purpose of evaluating the reliability of non-hermetic packaged solid-state devices in humid environments. It is a highly accelerated test which employs temperature and humidity under non-condensing conditions to accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it. Bias is not applied in this test to ensure the failure mechanisms potentially overshadowed by bias can be uncovered (e.g. galvanic corrosion). This test is used to identify failure mechanisms internal to the package and is destructive. December 2000; Reaffirmed June 2008 /JC-14.1 Subcommittee	$41.00
JESD 22-A119	**LOW TEMPERATURE STORAGE LIFE** The test is applicable for evaluation, screening, monitoring, and/or qualification of all solid state devices. Low Temperature storage test is typically used to determine the effect of time and temperature, under storage conditions, for thermally activated failure mechanisms of solid state electronic devices, including nonvolatile memory devices (data retention failure mechanisms). During the test reduced temperatures (test conditions) are used without electrical stress applied. This test may be destructive, depending on Time, Temperature and Packaging (if any). November 2004 June 2004 /JC-14.1 Subcommittee	$40.00
JESD 22-A120A	**TEST METHOD FOR THE MEASUREMENT OF MOISTURE DIFFUSIVITY AND WATER SOLUBILITY IN ORGANIC MATERIALS USED IN INTEGRATED CIRCUITS:** This specification details the procedures for the measurement of characteristic bulk material properties of moisture diffusivity and water solubility in organic materials used in the	

packaging of IC components. These two material properties are important parameters for the effective reliability performance of plastic packaged ICs after exposure to moisture and subjected to high temperature solder reflow.

January 2008 June 2006 /JC-14.1 Subcommittee $50.00

JESD 22-A121A

MEASURING WHISKER GROWTH ON TIN AND TIN ALLOY SURFACE FINISHES The predominant terminal finishes on electronic components have been Sn-Pb alloys. As the industry moves toward Pb-free components and assembly processes, the predominant terminal finish materials will be pure Sn and alloys of Sn, including Sn-Bi and Sn-Ag. Pure Sn and Sn-based alloy electrodeposits and solder-dipped finishes may grow tin whiskers, which could electrically short across component terminals or break off the component and degrade the performance of electrical or mechanical parts.

July 2008 September 2008 /JC-14.1 Subcommittee $68.00

JESD 22-B100B

PHYSICAL DIMENSION: The standard provides a method for determining whether the external physical dimensions of the device are in accordance with the applicable procurement document. This revision includes a change in details to be specified by the procurement document.

June 2003; Reaffirmed June 2006 September 2002 /JC-14.1 Subcommittee $38.00

JESD 22-B101A

EXTERNAL VISUAL: The purpose of this inspection is to verify that the materials, design, construction, markings, and workmanship of the device are in accordance with the applicable procurement document. External visual is a nondestructive test and applicable for all package types. The test is useful for qualification, process monitor, or lot acceptance.

October 2004 January 2004 /JC-14.1 Subcommittee $43.00

JESD 22-B102E

SOLDERABILITY: This test method provides optional conditions for preconditioning and soldering for the purpose of assessing the solderability of device package terminations. It provides procedures for dip & look solderability testing of through hole, axial and surface mount devices and a surface mount process simulation test for surface mount packages. The purpose of this test method is to provide a means of determining the solderability of device package terminations that are intended to be joined to another surface using lead (Pb) containing or Pb-free solder for the attachment.

October 2007 January 2007 /JC-14.1 Subcommittee $62.00

JESD 22-B103B

VIBRATION, VARIABLE FREQUENCY: The Vibration, Variable Frequency Test Method is intended to determine the ability of component(s) to withstand moderate to severe vibration as a result of motion produced by transportation or filed operation of electrical equipment. This is a destructive test that is intended for component qualification.

June 2002; Reaffirmed June 2006 /JC-14.1 Subcommittee $43.00

JESD 22-B104C

MECHANICAL SHOCK: This test is intended to determine the suitability of component parts for use in electronic equipment that may be subjected to moderately severe shocks as a result of suddenly applied forces or abrupt changes in motion produced by rough handling, transportation, or field operation. Shock of this type may disturb operating characteristics, particularly if the shock pulses are repetitive. This is a destructive test intended for device qualification. It is normally applicable to cavity-type packages.

November 2004 - Typo found on pg.1 in title, a new version dated December 2004 has been posted. if you downloaded between 11/10/04 & 12/10/04, please download againJanuary 2004 /JC-14.1 Subcommittee $41.00

JESD 22-B105C

LEAD INTEGRITY: This test method provides various tests for determining the integrity lead/package interface and the lead itself when the lead(s) are bent due to faulty board assembly followed by rework of the part for reassembly. For hermetic packages it is rececommend that this test be followed by hermeticity tests in accordance with Test Method A109 to determine if there are any adverse effects from the stresses applied to the seals as well as to the leads. These tests, including each of its test conditions, is considered destructive and is only recommended for qualification testing. This test is applicable to all through-hole devices and surface-mount devices requiring lead forming by the user.

May 2003; Reaffirmed June 2006 /JC-14.1 Subcommittee $48.00

JESD 22-B106D

RESISTANCE TO SOLDER SHOCK FOR THROUGH-HOLE MOUNTED DEVICES: This method established a standard procedure for determining whether through-hole solid state devices can withstand the effects of the temperature to which they will be subject during soldering of their leads. This revision updates the references to currently military standards.

April 2008 November 2007 /JC-14.1 Subcommittee $49.00

JESD 22-B107C

MARKING PERMANENCY: This test method provides two tests for determining the marking permanency of ink marked integrated circuits. A new non-destructive tape test method is introduced to quickly determine marking integrity. The test method also specifies a resistance to solvents method based upon MIL Std 883 Method 2015.

September 2004 October 2002 /JC-14.1 Subcommittee $43.00

JESD 22-B108A

COPLANARITY TEST FOR SURFACE-MOUNT SEMICONDUCTOR DEVICES: The purpose of this test is to measure the deviation of the terminals (leads or solder balls) from coplanarity for surface-mount semiconductor devices.

January 2003 /JC-14.1 Subcommittee $41.00

JESD 22-B109A

FLIP CHIP TENSILE PULL: The Flip Chip Tensile Pull Test Method is performed to determine the fracture mode and strength of the solder bump interconnection between the flip chip die and the substrate. It should be used to assess the consistency of the chip join process. This test method is a destructive test.

January 2009 September 2008 /JC-14.1 Subcommittee $54.00

JESD 22-B110A	**SUBASSEMBLY MECHANICAL SHOCK:** The new test method JESD22-B110 provides guidance for in-situ testing of mechanical shock resistance of components as mounted in a subassembly. Using terms, procedures, and test levels in common with JESD22-B104B, this test method provides a range of test level options to improve test applicability and compatibility with fragility test procedures. Test procedures are detailed, including test card and fixture needs, test tolerances, test documentation, component preparation, and definition of terms. November 2004 January 2004 /JC-14.1 Subcommittee	$45.00
JESD 22-B111	**BOARD LEVEL DROP TEST METHOD OF COMPONENTS FOR HANDHELD ELECTRONIC PRODUCTS:** This Board Level Drop Test Method is intended to evaluate and compare drop performance of surface mount electronic components for handheld electronic product applications in an accelerated test environment, where excessive flexure of a circuit board causes product failure. The purpose is to standardize the test board and test methodology to provide a reproducible assessment of the drop test performance of surface mounted components while duplicating the failure modes normally observed during product level test. July 2003 /JC-14.1 Subcommittee	$48.00
JESD 22-B112	**HIGH TEMPERATURE PACKAGE WARPAGE MEASUREMENT METHODOLOGY** The purpose of this test method is to measure the deviation from uniform flatness of an integrated circuit package body for the range of environmental conditions experienced during the surface-mount soldering operation. May 2005 October 2004 /JC-14.1 Subcommittee	$49.00
JESD 22-B113	**BOARD LEVEL CYCLIC BEND TEST METHOD FOR INTERCONNECT RELIABILITY CHARACTERIZATION OF COMPONENTS FOR HANDHELD ELECTRONIC PRODUCTS** The Board Level Cyclic Bend Test Method is intended to evaluate and compare the performance of surface mount electronic components in an accelerated test environment for handheld electronic products applications. The purpose is to standardize the test methodology to provide a reproducible performance assessment of surface mounted components while duplicating the failure modes normally observed during product level test. This is not a component qualification test and is not meant to replace any product level test that may be needed to qualify a specific product and assembly. March 2006 October 2005 /JC-14.1 Subcommittee	$49.00
JESD 22-B115	**SOLDER BALL PULL** This document describes a test method only; acceptance criteria and qualification requirements are not defined. This test method applies to solder ball pull force testing prior to end-use attachment. Solder balls are pulled individually using mechanical jaws; force and failure mode data are collected and analyzed. Other specialized solder ball pull methods using a heated thermode, gang pulling of multiple solder joints, etc., are outside the scope of this document. Both low and high speed testing are covered by this document. May 2007 September 2006 /JC-14.1 Subcommittee	$49.00
JESD 22-B116	**WIRE BOND SHEAR TEST:** This test method establishes a standard procedure for determining the strength of an integrated circuit wire bond by shearing the wire from the surface it is bonded to and measuring the force required. This method serves as an alternative to pulling the wire vertically until the wire separates from one of it's two bonded surfaces. It also provides guidelines for determining an appropriate minimum shear force for gold balls on aluminum alloy bonding surfaces. July 1998 /JC-14.1 Subcommittee	$45.00
JESD 22-B117A	**SOLDER BALL SHEAR:** The purpose of this test is conducted to assess the ability of solder balls to withstand mechanical shear forces that may be applied during device manufacturing, handling, test, shipment and end-use conditions. Solder ball shear is a destructive test. October 2006 January 2006 /JC-14.1 Subcommittee	$45.00
JESD 22-C100-A	**HIGH TEMPERATURE CONTINUITY - RESCINDED, November 1999** April 1990; Rescinded November 1999 /JC-14.1 Subcommittee	
JESD 22-C101D	**FIELD-INDUCED CHARGED-DEVICE MODEL TEST METHOD FOR ELECTROSTATIC DISCHARGE WITHSTAND THRESHOLDS OF MICROELECTRONIC COMPONENTS:** This new test method describes a uniform method for establishing charged-device model electrostatic discharge withstand thresholds. The charged-device-model simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing. One of many examples is a device sliding down a shipping tube hitting a metal surface. Discharges to devices on unterminated circuit assemblies are also well-modeled by the CDM test. DM ESD events not only reduce assembly yields but can also produce device damage that goes undetected by factory test and later is the cause of a latent failure. October 2008 January 2008 /JC-14.1 Subcommittee	$54.00
JESD 22B114	**MARK LEGIBILITY** This standard describes a nondestructive test to assess solid state device mark legibility. The specification applies only to solid state devices that contain markings, regardless of the marking method. It does not define what devices must be marked or the method in which the device is marked, i.e., ink, laser, etc. The standard is limited in scope to the legibility requirements of solid state devices, and does not replace related reference documents listed in this standard. March 2008 September 2007 /JC-14.3 Subcommittee	$50.00
JESD 23	**TEST METHODS AND CHARACTER DESIGNATION FOR LIQUID CRYSTAL DEVICES:** This standard specifies a collection of procedures for testing and character designation of liquid crystal devices. May 1982	$57.00
JESD 24	**POWER MOSFETS:** This standard contains a listing of terms and definitions and letter symbols; a description of	

established procedures that are followed in the assignment of semiconductor-industry-type designations to power transistors; electrical verification test; thermal characteristics; and a user's guide.

July 1985 /JC-25 Committee $71.00

JESD 24- 1

ADDENDUM No. 1 to JESD24 - METHOD FOR MEASUREMENT OF POWER DEVICE TURN-OFF SWITCHING LOSS: Describes the method of a typical oscilloscope waveform and the basic test circuit employed in the measurement of turn off loss for bipolar, IGBT and MOSFET power semiconductors. This method can be used as a standard for evaluating power semiconductor turn-off switching loss capability and defines standard terminology that should be referenced within the electronic industry.

October 1989; Reaffirmed April 1999, October 2002 /JC-25 Committee $41.00

JESD 24- 2

ADDENDUM No. 2 to JESD24 - GATE CHARGE TEST METHOD: This addendum establishes a method for measuring power device gate charge. A gate charge test is performed by driving the device gate with a constant current and measuring the resulting gate voltage response. Constant gate current scales the gate voltage, a function of time, to a function of coulombs. The slope of the generated response reflects the active device capacitance as it varies during the switching transition . Gate charge measurements are useful for characterizing the large signal switching performance of power MOS and IGBT devices. Developed over a four year span by the JEDEC JC-25 Committee, the method defines a repeatable means of measuring the widely published Qgd charge values.

January 1991; Reaffirmed October 2002 April 1999 /JC-25 Committee $41.00

JESD 24- 3

ADDENDUM No. 3 to JESD24 - THERMAL IMPEDANCE MEASUREMENTS FOR VERTICAL POWER MOSFETS (DELTA SOURCE-DRAIN VOLTAGE METHOD): The purpose of this test method is to measure the thermal impedance of the MOSFET under the specified conditions of applied voltage, current and pulse duration. The temperature sensitivity if the forward voltage drop of the source-drain is used as the junction temperature indicator. This method is particularly suitable to enhancement mode, power MOSFETs having relatively long thermal response times. This test method may be used to measure the thermal response of junction to a heating pulse, to ensure proper die mountdown to its case, or the dc thermal resistance, by the proper choice of the pulse duration and magnitude if the heating pulse.

November 1990; Reaffirmed April 1999 /JC-25 Committee $47.00

JESD 24- 4

ADDENDUM No. 4 to JESD24 - THERMAL IMPEDANCE MEASUREMENTS FOR BIPOLAR TRANSISTORS (DELTA BASE-EMITTER VOLTAGE METHOD): The purpose of this test method is to measure the thermal impedance of the Bipolar Transistor under the specified conditions of applied voltage, current and pulse duration. The temperature sensitivity of the base-emitter voltage is used as the junction temperature indicator. This test method is used to measure the thermal response of the junction to a heating pulse. Specifically, the test may be used to measure dc thermal resistance, and to ensure proper die mountdown to its case. This is accomplished through the appropriate choice of pulse duration and heating power magnitude.

November 1990; Reaffirmed October 2002 April 1999 /JC-25 Committee $47.00

JESD 24- 5

ADDENDUM No. 5 to JESD24 - SINGLE PULSE UNCLAMPED INDUCTIVE SWITCHING (UIS) AVALANCHE TEST METHOD: This method describes a means for testing the ability of a power switching device to withstand avalanche breakdown.

August 1990; Reaffirmed october 2002 April 1999 /JC-25 Committee $38.00

JESD 24- 6

ADDENDUM No. 6 to JESD24 - THERMAL IMPEDANCE MEASUREMENTS FOR INSULATED GATE BIPOLAR TRANSISTORS: This standard describes in detail the method for thermal measurements of Insulated Gate Bipolar Transistors (IGBTs) and is suitable for use both in manufacturing and application of the devices. The method covers both thermal transient and thermal equilibrium measurements for manufacturing process control and device characterization purposes. Properly implemented, JESD24-6 provides a basis for obtaining realistic thermal parametric values that will benefit supplier's internal effectiveness and will be useful to the design and manufacturer of reliable IGBT circuits.

October 1991; Reaffirmed October 2002 April 1999 /JC-25 Committee $47.00

JESD 24- 7

ADDENDUM No. 7 to JESD24 - COMMUTATING DIODE SAFE OPERATING AREA TEST PROCEDURE FOR MEASURING dv/dt DURING REVERSE RECOVERY OF POWER TRANSISTORS: Defines methods for verifying the diode recovery stress capability of power transistors.

August 1982; Reaffirmed October 2002 April 1999 /JC-25 Committee $40.00

JESD 24- 8

ADDENDUM No. 8 to JESD24 - METHOD FOR REPETITIVE INDUCTIVE LOAD AVALANCHE SWITCHING: Determines the repetitive inductive avalanche switching capability of power switching transistors.

August 1992; Reaffirmed October 2002 April 1999 /JC-25 Committee $40.00

JESD 24- 9

ADDENDUM No. 9 to JESD24 - SHORT CIRCUIT WITHSTAND TIME TEST METHOD: Test method to determine how long a device can survive a short circuit condition with a given drive level.

August 1992; Reaffirmed October 2002 April 1999 /JC-25 Committee $40.00

JESD 24-10

ADDENDUM No. 10 to JESD24 - TEST METHOD FOR MEASUREMENT OF REVERSE RECOVERY TIME trr FOR POWER MOSFET DRAIN-SOURCE DIODES: Test method to measure the reverse recovery characteristics of the drain source diode of a power MOSFET.

August 1994; Reaffirmed October 2002 April 1999 /JC-25 Committee $41.00

JESD 24-11

ADDENDUM No. 11 to JESD24 - POWER MOSFET EQUIVALENT SERIES GATE RESISTANCE TEST METHOD: Test method to measure the equivalent resistance of the gate to source of a power MOSFET.

August 1996; Reaffirmed March 2001, October 2002 March 2001 /JC-25 Committee $38.00

JESD 24-12	**THERMAL IMPEDANCE MEASUREMENT FOR INSULATED GATE BIPOLAR TRANSISTORS - (Delta VCE(on) Method)** The purpose of this test method is to measure the thermal impedance of the IGBT (Insulated Gate Bipolar Transistor) under the specified conditions of applied voltage, current and pulse duration. The temperature sensitivity of the collector-emitter on voltage, VCE(on), is used as the junction temperature indicator. This is an alternative method to JEDEC Standard No. 24-6. June 2004 September 2002 /JC-25 Committee	$45.00
JESD 25	**MEASUREMENT OF SMALL-SIGNAL TRANSISTOR SCATTERING PARAMETERS:** This standard provides a test method and definition for small-signal conditions at microwave frequencies. November 1972; Reaffirmed September 1981, April 2000, October 2002 /JC-25 Committee	$57.00
JESD 26-A	**GENERAL SPECIFICATION FOR PLASTIC ENCAPSULATED MICROCIRCUITS FOR USE IN RUGGED APPLICATIONS - RESCINDED, July 2001** April 1990; Rescinded July 2001 /JC-13.2 Subcommittee	
JESD 27	**CERAMIC PACKAGE SPECIFICATION FOR MICROELECTRONIC PACKAGES:** The intent of this standard is to be a guide in the manufacture and procurement of ceramic packages, especially for the hybrid industry. Manufacturers or ceramic packages and procuring activities for these packages will now be able to use this document as the means for agreement in the imposition of minimum requirements in qualification, screening, and quality conformance. August 1993; Under Revision , will be merged with JESD9-A /JC-13.5 Subcommittee	$67.00
JESD 28-1	**N-CHANNEL MOSFET HOT CARRIER DATA ANALYSIS:** This addendum provides data analysis examples useful in analyzing MOSFET n-channel hot-carrier-induced degradation data. This addendum to JESD28 (Hot carrier n-channel testing standard) suggests hot-carrier data analysis techniques. September 2001 /JC-14.2 Subcommittee	$43.00
JESD 28-A	**A PROCEDURE FOR MEASURING N-CHANNEL MOSFET HOT-CARRIER-INDUCED DEGRADATION UNDER DC STRESS:** This document describes an accelerated test for measuring the hot-carrier-induced degradation of a single n-channel MOSFET using dc bias. The purpose of this document is to specify a minimum set of measurements so that valid comparisons can be made between different technologies, IC processes, and process variations in a simple, consistent and controlled way. The measurements specified should be viewed as a starting point in the characterization and benchmarking of the transistor manufacturing process. December 2001 /JC-14.2 Subcommittee	$47.00
JESD 29-A	**FAILURE-MECHANISM-DRIVEN RELIABILITY MONITORING - SUPERSEDED BY EIA/ANSI-659, July 1996.** July 1996; Superseded July 1996 /JC-14.3 Subcommittee	
JESD 30E	**DESCRIPTIVE DESIGNATION SYSTEM FOR SEMICONDUCTOR-DEVICE PACKAGES:** This standard describes a systematic method for generating universal descriptive designators for semiconductor-device packages. The descriptive designator is intended to provide a useful communication tool but has no implied control for assuring package interchangeability. August 2008 January 2008 /JC-11 Committee	$69.00
JESD 31C	**GENERAL REQUIREMENTS FOR DISTRIBUTORS OF COMMERCIAL AND MILITARY SEMICONDUCTOR DEVICES:** This publication identifies the general requirements for Distributors that supply Commercial and Military products. This document identifies the general requirements for Distributors that supply Commercial and Military products. Now updated to provide clarification, these requirements apply to all discrete semiconductors, integrated circuits and hybrids, whether packaged or in wafer/die form, manufactured by all component Manufacturers. This revision was incorporated to better define the requirements for the handling of moisture-sensitive devices in distribution. The addition of IPC/JEDEC J-STD-020 and IPC/JEDEC J-STD-033 ensure consistent requirements throughout the distribution channel. September 2003 January 2003 /JC-14.4 Subcommittee	$52.00
JESD 32	**STANDARD FOR CHAIN DESCRIPTION FILE:** This document provides a standard for describing an ISP device chain, opening up the possibility for third-party companies to provide value-added ISP software. The purpose of the Chain Description File is to describe the configuration of a programming chain made up of devices that can be connected in some serial fashion. No assumptions are made about how data is used by the device, nor about the nature or configuration of the control signals that affect programming. It will support devices configured using electrically-erasable(EE), Flash, SRAM, or any other reconfigurable cell. For devices programmed via an IEEE programmable devices in the same chain. June 1996 / Committee!33JC421	$47.00
JESD 33-B	**STANDARD METHOD FOR MEASURING AND USING THE TEMPERATURE COEFFICIENT OF RESISTANCE TO DETERMINE THE TEMPERATURE OF A METALLIZATION LINE:** This newly revised test method provides a procedure for measuring the temperature coefficient of resistance, TCR(T), of thin-film metallizations used in microelectronic circuits and devices. Procedures are also provided to use the TCR(T) to determine the temperature of a metallization line under Joule-heating conditions and to determine the ambient temperature where the metallization line is used as a temperature sensor. Originally, the method was intended only for aluminum-based metallizations and for other metallizations that satisfy the linear dependence and stability stipulations of the method. The method has been revised to make it explicitly applicable to copper-based metallizations, as well, and at temperatures beyond where the resistivity of copper is no longer linearly dependent on temperature (beyond approximately 200 °C). Using the TCR(T) measured for copper in the linear-dependent region, a factor is used to correct the calculated temperature at these higher temperatures.	

	February 2004 April 2003 /JC-14.2 Subcommittee	$61.00
JESD 34	**FAILURE-MECHANISM-DRIVEN RELIABILITY QUALIFICATION OF SILICON DEVICES:** This document applies to the reliability qualification of new or changed silicon devices, and their materials or manufacturing processes. Does not address qualification of product quality or functionality. Provides an alternative to traditional stress-driven qualification. March 1993; Rescinded November 2004 June 2004 /JC-14.2 Subcommittee	$43.00
JESD 35-1	**ADDENDUM No. 1 to JESD35 - GENERAL GUIDELINES FOR DESIGNING TEST STRUCTURES FOR THE WAFER-LEVEL TESTING OF THIN DIELECTRICS:** This addendum expands the usefulness of the Standard 35 (JESD35) by detailing the various sources of measurement error that could effect the test results obtained by the ramped tests described in JESD35. Each source of error is described and its implications on test structure design is noted. This addendum can be used as a guide when designing test structures for the qualification and characterization of thin oxide reliability, specifically, by implementing accelerated voltage or current ramp tests. September 1995 /JC-14.2 Subcommittee	$52.00
JESD 35-2	**ADDENDUM No. 2 to JESD35 - TEST CRITERIA FOR THE WAFER-LEVEL TESTING OF THIN DIELECTRICS:** This addendum includes test criteria to supplement JESD35. JESD35 describes procedures developed for estimating the overall integrity of thin oxides in the MOS Integrated Circuit manufacturing industry. Two test procedures are included in JESD35: a Voltage-Ramp (V-Ramp) and a Current-Ramp (J-Ramp). As JESD35 became implemented into production facilities on a variety of test structures and oxide attributes, a need arose to clarify end point determination and point out some of the obstacles that could be overcome by careful characterization of the equipment and test structures. February 1996 /JC-14.2 Subcommittee	$43.00
JESD 35-A	**PROCEDURE FOR WAFER-LEVEL-TESTING OF THIN DIELECTRICS:** The revised JESD35 is intended for use in the MOS Integrated Circuit manufacturing industry. It describes procedures developed for estimating the overall integrity and reliability of thin gate oxides. Three basic test procedures are described, the Voltage-Ramp (V-Ramp), the Current-Ramp (J-Ramp) and the new Constant Current (Bounded J-Ramp) test. Each test is designed for simplicity, speed and ease of use. The standard has been updated to include breakdown criteria that are more robust in detecting breakdown in thinner gate oxides that may not experience hard thermal breakdown. April 2001 /JC-14.2 Subcommittee	$67.00
JESD 36	**STANDARD DESCRIPTION OF LOW-VOLTAGE TTL-COMPATIBLE, 5 V TOLERANT CMOS LOGIC DEVICES:** This standard outlines the standard dc specifications, test conditions, and test loading for logic products that are designed to tolerate input and output voltages which exceed the device's power supply. More specifically this standardizes 5 V - tolerant logic prducts that run from 'low voltage' (2.7 V to 3.6 V) power supplies. Products that meet this standard can be used to effectively interface between LVCMOS/LVTTL and 5 V TTL buses, bridging the gap between low-voltage and 5 V TTL busses. June 1996 /JC-40 Committee	$45.00
JESD 37	**STANDARD LOGNORMAL ANALYSIS OF UNCENSORED DATA, AND OF SINGLY RIGHT -CENSORED DATA UTILIZING THE PERSSON AND ROOTZEN METHOD:** This standard details techniques for estimating the values of a two parameter lognormal distribution from complete lifetime data (all samples in an experiment have failed) or singly right-censored lifetime data (the experiment have failed) or singly right-censored lifetime data gathered from rapid stress test; however, not all types of failure data can be analyzed with these techniques. October 1992 /JC-14.2 Subcommittee	$59.00
JESD 38	**STANDARD FOR FAILURE ANALYSIS REPORT FORMAT:** This standard is to promote unification of content and format of semiconductor device failure-analysis reports so that reports from diverse laboratories may be easily read, compared, and understood by customers. Additional objectives are to ensure that reports can be easily ready by users, satisfactorily reproduced on copying machines, adequately transmitted by telefax, and conveniently stored in standard filing cabinets. December 1995 /JC-14.6 Subcommittee	$43.00
JESD 39-A	**QUALITY SYSTEM ASSESSMENT - SUPERSEDED BY ANSI/EIA-670, June 1997.** June 1997; Superseded /JC-14.4 Subcommittee	
JESD 40	**PROCUREMENT QUALITY OF SOLID STATE COMPONENTS BY GOVERNMENT CONTRACTORS - SUPERSEDED BY EIA-623, July 1994** July 1994; Superseded /JC-13 Committee	
JESD 41	**REVERSE RECOVERY CHARACTERISTICS OF SILICON DIODES: RESCINDED June 2002.** May 1995; Rescinded June 2002 /JC-22.1 Subcommittee	
JESD 42	**REQUIREMENTS FOR HANDLING ELECTROSTATIC-DISCHARGE-SENSITIVE (ESDS) DEVICES - SUPERSEDED BY EIA-625, November 1994.** March 1994; Superseded /JC-13 Committee	
JESD 43	**COMPONENT PROBLEM ANALYSIS AND CORRECTIVE ACTION REQUIREMENTS - SUPERSEDED BY EIA-671, November 1996.** November 1996; Superseded /JC-14.4 Subcommittee	

JESD 45	MEASUREMENT METHOD FOR THERMAL RESISTANCE OF BRIDGE RECTIFIER ASSEMBLIES: RESCINDED, June 2002. Replaced by JESD282-B. December 1994; Rescinded June 2002 June 2002 /JC-22.2 Subcommittee	
JESD 46C	CUSTOMER NOTIFICATION OF PRODUCT/PROCESS CHANGES BY SEMICONDUCTOR SUPPLIERS: This standard establishes procedures to notify customers of semiconductor product and process changes. Requirements include: documentation; procedures for classification, notification and customer response; content; and records.Documentation of a suppliers change notification system should set clear and understandable expectations for both the originators of the change and their end customers. October 2006 January 2006 /JC-14.4 Subcommittee	$41.00
JESD 47G	STRESS-TEST-DRIVEN QUALIFICATION OF INTEGRATED CIRCUITS: This standard describes a baseline set of acceptance tests for use in qualifying electronic components as new products, a product family, or as products in a process which is being changed. March 2009 September 2008 /JC-14.3 Subcommittee	$65.00
JESD 48B	PRODUCT DISCONTINUANCE: This standard establishes the requirements for timely customer notification of planned productdiscontinuance, which will assist customers in managing end-of-life supply, or to transition on-goingrequirements to alternate products. May 2005 January 2005 /JC-14.4 Subcommittee	$40.00
JESD 49A	PROCUREMENT STANDARD FOR KNOWN GOOD DIE (KGD): This standard was created to facilitate the procurement and use of high reliability semiconductor microcircuits or discrete devices provided in bare die form, commonly known as Known Good Die (KGD). September 2005 January 2005 /JC-13 Committee	$48.00
JESD 50B.01	SPECIAL REQUIREMENTS FOR MAVERICK PRODUCT ELIMINATION AND OUTLIER MANAGEMENT This standard applies to the identification and control of Maverick Product that can occur during fabrication, assembly, packaging, or test of any electronic component. It can be implemented for an entire product line or to segregate product that has a higher probability of adversely impacting quality or reliability. November 2008 January 2008 /JC-14.3 Subcommittee	$54.00
JESD 51	METHODOLOGY FOR THE THERMAL MEASUREMENT OF COMPONENT PACKAGES (SINGLE SEMICONDUCTOR DEVICE) This standard and its subsequent addendum's, provides a standard for thermal measurement that, if followed fully, will provide correct and meaningful data that will allow for determination of junction temperature for specific conditions. The data can be used for package design evaluation, device characterization and reliability predictions. December 1995 /JC-15.1 Subcommittee	$40.00
JESD 51- 1	INTEGRATED CIRCUIT THERMAL MEASUREMENT METHOD - ELECTRICAL TEST METHOD (SINGLE SEMICONDUCTOR DEVICE): The purpose of this test method is to define a standard Electrical Test Method (ETM) that can be used to determine the thermal characteristics of single integrated circuit devices housed in some form of electrical package. This method will provide a basis for comparison of different devices housed in the same electronic package or similar devices housed in different electronic packages. December 1995 /JC-15.1 Subcommittee	$61.00
JESD 51- 2A	INTEGRATED CIRCUITS THERMAL TEST METHOD ENVIRONMENTAL CONDITIONS - NATURAL CONVECTION (STILL AIR): This document outlines the environmental conditions necessary to ensure accuracy and repeatability for a standard junction-to-ambient thermal resistance measurement in natural convection. January 2007 March 2007 /JC-15.1 Subcommittee	$57.00
JESD 51- 3	LOW EFFECTIVE THERMAL CONDUCTIVITY TEST BOARD FOR LEADED SURFACE MOUNT PACKAGES: This standard describes design requirements for a single layer, leaded surface mount integrated circuit package thermal test board. The standard describes board material and geometry requirements, minimum trace lenghts, trace thickness, and routing considerations. Application includes still air and moving air thermal tests. August 1996 /JC-15.1 Subcommittee	$41.00
JESD 51- 4	THERMAL TEST CHIP GUIDELINE (WIRE BOND TYPE CHIP): This guideline describes design requirements for wire bond type semiconductor chips to be used for thermal resistance listing of IC packages. This document provides specific guidelines for chip design but allows flexibility in the materials and layout requirements. February 1997 /JC-15.1 Subcommittee	$45.00
JESD 51- 5	EXTENSION OF THERMAL TEST BOARD STANDARDS FOR PACKAGES WITH DIRECT THERMAL ATTACHMENT MECHANISMS: This extension of the thermal standards provides a standard fixture for direct attach type packages such as deep-downset of thermally tabbed packages. This specification provides additional design detail for use in developing thermal test boards with application to these package types. This document is in addition to and not replacement for the design specifications in other standards. February 1999 /JC-15.1 Subcommittee	$38.00
JESD 51- 6	INTEGRATED CIRCUIT THERMAL TEST METHOD ENVIRONMENTAL CONDITIONS - FORCED CONVECTION (MOVING AIR): This standard specifies the environmental conditions for determining thermal performance of an integrated circuit device in a forced convection environment when mounted on a standard thermal test board. March 1999 /JC-15.1 Subcommittee	$38.00

JESD 51- 7	**HIGH EFFECTIVE THERMAL CONDUCTIVITY TEST BOARD FOR LEADED SURFACE MOUNT PACKAGES:** This fixturing further defines the environment for thermal test of packaged microelectronic devices. Its function is to provide an alternate mounting surface for the analysis of heat flow in electronic components. The objective of the standard is to provide a high effective thermal conductivity mounting surface that can be compared equally against standard tests done in different laboratories with typical variations of less than or equal to 10%. February 1999 /JC-15.1 Subcommittee	$41.00
JESD 51- 8	**INTEGRATED CIRCUIT THERMAL TEST METHOD ENVIRONMENTAL CONDITIONS - JUNCTION-TO-BOARD:** This specification should be used in conjunction with the overview document JESD51, Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device) [1] and the electrical test procedures described in JESD51-1, 'Integrated Circuit Thermal Measurement Method (Single Semiconductor Device' [2. The environmental conditions described in this document are specifically designed for testing of integrated circuit devices that are mounted on standard test boards with two internal copper planes [3]. This standard is not applicable to packages that have asymmetric heat flow paths to the printed board caused by such thermal enhancements as fused leads (leads connected to the die pad) or power style packages with the exposed heat slug on one side of the package. October 1999 /JC-15.1 Subcommittee	$45.00
JESD 51- 9	**TEST BOARDS FOR AREA ARRAY SURFACE MOUNT PACKAGE THERMAL MEASUREMENTS:** This standard covers the design of printed circuit boards (PCBs) used in the thermal characterization of ball grid array (BGA) and land grid array (LGA) packages. It is intended to be used in conjunction with the JESD51 series of standards that cover the test methods and test environments. JESD51-9 was developed to give a figure-of-merit of thermal performance that allows for accurate comparisons of packages from different suppliers. It can be used to give a first order approximation of system performance and, in conjunction with the other JESD51 PCB standards, allows for comparisons of the various package families. July 2000 /JC-15.1 Subcommittee	$48.00
JESD 51-10	**TEST BOARDS FOR THROUGH-HOLE PERIMETER LEADED PACKAGE THERMAL MEASUREMENTS:** This standard covers the design of printed circuit boards (PCBs) used in the thermal characterization of Dual-Inline Packages (DIP) and Single-Inline Packages (SIP). It is intended to be used in conjunction with the JESD51 series of standards that cover the test methods and test environments. JESD51-10 was developed to give a figure-of-merit of thermal performance that allows for accurate comparisons of packages from different suppliers. It can be used to give a first order approximation of system performance and, in conjunction with the other JESD51 PCB standards, allows for comparisons of the various package families. July 2000 /JC-15.1 Subcommittee	$45.00
JESD 51-11	**TEST BOARDS FOR THROUGH-HOLE AREA ARRAY LEADED PACKAGE THERMAL MEASUREMENT:** This standard covers the design of printed circuit boards (PCBs) used in the thermal characterization of Pin Grid Array (PGA) packages. It is intended to be used in conjunction with the JESD51 series of standards that cover the test methods and test environments. JESD51-11 was developed to give a figure-of-merit of thermal performance that allows for accurate comparisons of packages from different suppliers. It can be used to give a first order approximation of system performance and, in conjunction with the other JESD51 PCB standards, allows for comparisons of the various package families. June 2001 /JC-15.1 Subcommittee	$47.00
JESD 51-31	**THERMAL TEST ENVIRONMENT MODIFICATIONS FOR MULTICHIP PACKAGES** This document specifies the appropriate modifications needed for Multi-Chip Packages to the thermal test environmental conditions specified in the JESD51 series of specifications. The data obtained from methods of this document are the raw data used to document the thermal performance of the package. The use of this data will be documented in JESD51-XX, ☐Guideline to Support Effective Use of MCP Thermal Measurements☐ which is being prepared. July 2008 November 2007 /JC-15 Committee	$54.00
JESD 52	**STANDARD FOR DESCRIPTION OF LOW VOLTAGE TTL-COMPATIBLE CMOS LOGIC DEVICES:** This standard describes dc interface specifications and test environment for these devices that operate with 2.7 V to 3.6 V power supplies. The goal is to provide a consistent set of dc specifications for reference by logic suppliers and users alike. November 1995 /JC-40 Committee	$45.00
JESD 53	**MANAGEMENT OF COMPONENT OBSOLESCENCE BY GOVERNMENT CONTRACTORS: RESCINDED, October 2002** January 1996; Rescinded October 2002 October 2002 /JC-13.2 Subcommittee	
JESD 54	**STANDARD FOR DESCRIPTION OF 54/74ABTXXX AND 74BCXXX TTL-COMPATIBLE BiCMOS LOGIC DEVICES:** The purpose is to provide a standard of BiCMOS Logic series specifications to provide for uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users. February 1996 /JC-40 Committee	$61.00
JESD 55	**STANDARD FOR DESCRIPTION OF LOW-VOLTAGE TTL-COMPATIBLE BiCMOS LOGIC DEVICES:** The purpose is to provide a standard of BiCMOS Logic series specifications for uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users. May 1996 /JC-40 Committee	$49.00
JESD 57	**TEST PROCEDURE FOR THE MANAGEMENT OF SINGLE-EVENT EFFECTS IN SEMICONDUCTOR DEVICES FROM HEAVY ION IRRADIATION:** This test method defines requirements and procedures for ground simulation and single	

event effects (SEE) and implementation of the method in testing integrated circuits. This standard is valid when using a cyclotron or Van de Graaff accelerator. Microcircuits under test must be delidded. The ions used at the facilities have an atomic number Z > 2. It does not apply to SEE testing that uses protons, neutrons, or other lighter particles. This standard is designed to eliminate any misunderstanding between users of the method and test facilities, to minimize delays, and to promote standardization of testing and test data.

December 1996; Under Revision September 2003 /JC-13.4 Subcommittee $67.00

JESD 59

BOND WIRE MODELING STANDARD: This standard describes the modeling of a bond wire from an integrated circuit (IC) die to a package lead in a ball or wedge type wire bond configuration.

June 1997 /JC-15.2 Subcommittee $45.00

JESD 60A

A PROCEDURE FOR MEASURING P-CHANNEL MOSFET HOT-CARRIER-INDUCED DEGRADATION AT MAXIMUM GATE CURRENT UNDER DC STRESS: This method establishes a standard procedure for accelerated testing of the hot-carrier-induced change of a p-channel MOSFET. The objective is to provide a minimum set of measurements so that accurate comparisons can be made between different technologies. The measurements specified should be viewed as a starting pint in the characterization and benchmarking of the trasistor manufacturing process.

September 2004 August 2002 /JC-14.2 Subcommittee $52.00

JESD 61A.01

ISOTHERMAL ELECTROMIGRATION TEST PROCEDURE: This standard describes an algorithm for the execution of the isothermal test, using computer-controlled instrumentation. The primary use of this test is for the monitoring of microelectronic metallization lines at wafer level (1) in process development, to evaluate process options, (2) in manufacturing, to monitor metallization reliability and (3) to monitor/evaluate process equipment. While it is developed as a fast WLR test, it can also be an effective tool for complementing the reliability data obtained through the standard package level electromigration test.

October 2007 June 2006 /JC-14.2 Subcommittee $67.00

JESD 62-A

OUTLIER IDENTIFICATION AND MANAGEMENT SYSTEM FOR ELECTRONIC COMPONENTS, RESCINDED January 2009. Replaced by JESD50. Relevant JESD62 content has been consolidated into JESD50B, published October 2008 - Special Requirments for Maverick Product Elimination-.

May 2002; Rescinded January 2009 /JC-14.3 Subcommittee $45.00

JESD 63

STANDARD METHOD FOR CALCULATING THE ELECTROMIGRATION MODEL PARAMETERS FOR CURRENT DENSITY AND TEMPERATURE: This method provides procedures to calculate sample estimates and their confidence intervals for the electromigration model parameters of current density and temperature. The model parameter for current density is the exponent (n) to which the current density is raised in Black's equation. The parameter for temperature is the activation energy for the electromigration failure process.

February 1998 /JC-14.2 Subcommittee $61.00

JESD 64-A

STANDARD FOR DESCRIPTION OF 2.5 V CMOS LOGIC DEVICES WITH 3.6 V CMOS TOLERANT INPUTS AND OUTPUTS: The purpose is to provide a standard for 2.5 V nominal supply voltage logic devices for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. This specification provides for compatibility between devices operating between either the Standard Range of 1.8 V to 2.7 V or the optional Extended Range of 1.65 V to 2.7 V supply voltages, as well as over-voltage tolerance with devices operating at 3.6 V.

October 2000 /JC-40 Committee $40.00

JESD 65B

DEFINITION OF SKEW SPECIFICATIONS FOR STANDARD LOGIC DEVICES: This standard defines skew specifications and skew testing for standard logic devices. The purpose is to provide a standard for specifications to achieve uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users.

September 2003 /JC-40 Committee $48.00

JESD 66

TRANSIENT VOLTAGE SUPPRESSOR STANDARD FOR THYRISTOR SURGE PROTECTIVE DEVICE: This standard is applicable to Thyristor Surge Protective Devices. It describes terms and definitions and explains methods for verifying device ratings and measuring device characteristics. The intended users of this standard are those interested in Thyristor Surge Protective Device characterization and rating verification. These devices are used primarily by the telecommunications industry to protect circuits from harmful overvoltages. The Thyristor Surge Protective Device (TSPD) is a semiconductor device that is finding widespread application in the telecommunication industry. The intent of this stand is to provide information on test methods that will reduce the possibility of disagreement and misunderstanding between TSPD vendors and users, and facilitate the determination of device interchangeability.

November 1999; Reaffirmed November 2006 /JC-22.5 Subcommittee $91.00

JESD 67

I/O DRIVERS AND RECEIVERS WITH CONFIGURABLE COMMUNICATION VOLTAGE, IMPEDANCE, AND RECEIVER THRESHOLD: This standard attempts to aid in the design of electronic systems comprised of components that operate at several different supply voltages. This document covers respectively configurable I/O voltage, receiver type and switchpoint, and driver impedance.

February 1999 /JC-16 Committee $45.00

JESD 68.01

COMMON FLASH INTERFACE (CFI): The Common Flash Interface (CFI) specification outlines a device and host system software interrogation handshake that allows specific software algorithms to be used for entire families of devices. This allows device-independent, JEDEC ID-independent, and forward- and backward-compatible software support for the specific flash families. It allows flash vendors to standardize their existing interfaces for long-term compatibility. The changes for this minor revision are indicated in Annex A on page 11.

September 2003 December 2002 /JC-42.4 Subcommittee $48.00

JESD 69B	**INFORMATION REQUIREMENTS FOR THE QUALIFICATION OF SILICON DEVICES:** This standard establishes the information required by semiconductor users from IC manufacturers and distributors in order to judge whether a semiconductor component is fit for use in their particular application. It establishes a set of data elements that describes the component and defines what each element means. It does not define the quality and reliability requirements that the component must satisfy. This standard can be used in conjunction with other reliability qualification standards, such as JESD34 'Failure Mechanism-Driven Reliability Qualification of Silicon Devices' and JESD47 'Stress Test Driven Qualification of Integrated Circuits'. October 2007 June 2007 /JC-14.3 Subcommittee	$50.00
JESD 70	**2.5 V BiCMOS LOGIC DEVICE FAMILY SPECIFICATION WITH 5 V TOLERANT INPUTS AND OUTPUTS:** The purpose is to provide a standard for 2.5 V nominal supply voltage logic devices, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use, thus providing compatibility between devices operating between 2.3 V and 2.7 V supply voltages, as well as overvoltage tolerance with devices operating at 3.3 V, or 5 V. June 1999 /JC-40 Committee	$41.00
JESD 71	**STANDARD TEST AND PROGRAMMING LANGUAGE (STAPL):** STAPL is a vendor- and platform-independent language for programming and testing devices via the IEEE standard 1149.1 interface, commonly known as JTAG. STAPL enables programming of designs into programmable logic devices (PLDs) offered by a variety of PLD vendors. STAPL is also suitable for testing 1149.1-compliant devices. August 1999 / Committee!33JC421	$67.00
JESD 72	**TEST METHODS AND ACCEPTANCE PROCEDURES FOR THE EVALUATION OF POLYMERIC MATERIALS:** This Test Method covers the minimum requirements that should be in effect for the evaluation and acceptance of polymeric materials for use in industrial, military, space, and other special-condition products which may require capabilities beyond standard commercial microelectronics applications. It is not the intent of this Publication to specify a material, but to evaluate the material to assure that the quality and reliability of the microelectronic devices are not compromised. This document replaces JEP105, JEP107 and JEP112. June 2001; Reaffirmed January 2007 January 2001 /JC-13.5 Subcommittee	$52.00
JESD 73	**DESCRIPTION OF 5 V BUS SWITCH WITH TTL-COMPATIBLE CONTROL INPUTS:** This standard covers specifications for a family of 5 V NMOS FET bus switch devices with 5 V TTL compatible control inputs. Not included in this document are device-specific parameters and performance levels that the vendor must also apply for full device description. June 1999 /JC-40 Committee	$40.00
JESD 73-1	**STANDARD FOR DESCRIPTION OF 3.3 V NFET BUS SWITCH DEVICES:** This standard covers specifications for a family of 3.3 V NMOS FET bus switch devices. Not included in this document are device specific parameters and performance levels that the vendor must also supply for full device description. The purpose of this document is to provide a set of uniform data sheet parameters for the description of bus switch devices. This standard includes required parameters, test conditions, test levels, and measurement methods for data sheet descriptions of bus switch devices. August 2001 /JC-40 Committee	$40.00
JESD 73-2	**STANDARD FOR DESCRIPTION OF 3.3 V NFET BUS SWITCH DEVICES WITH INTEGRATED CHARGE PUMPS:** This standard covers specifications for a family of 3.3 V NMOS FET bus switch devices with integrated charge pumps. Not included in this document are device specific parameters and performance levels that the vendor must also supply for full device description. The purpose of this standard is to provide a set of uniform data sheet parameters for the description of bus switch devices. This standard includes required parameters, test conditions, test levels, and measurement methods for data sheet descriptions of bus switch devices. August 2001 /JC-40 Committee	$40.00
JESD 73-3	**STANDARD FOR DESCRIPTION OF 3867 - 2.5 V, SINGLE 10-BIT, 2-PORT, DDR FET SWITCH:** This standard provides a set of uniform data sheet parameters for the description of a single 10-bit, 2.5 V FET transmission-gate bus switch device for DDR memory module and motherboard applications. This bus switch device has a low ON resistance allowing inputs to be connected directly to outputs, with near zero propagation delay. November 2001 / Committee!33JC402	$40.00
JESD 73-4	**STANDARD FOR DESCRIPTION OF 3877 - 2.5 V, DUAL 5-BIT, 2-PORT, DDR FET SWITCH:** This standard provides a set of uniform data sheet parameters for the description of a dual 5-bit, 2.5 V FET transmission-gate bus switch device for DDR memory module and motherboard applications. This bus switch device has a low ON resistance allowing inputs to be connected directly to outputs, with near zero propagation delay. November 2001 / Committee!33JC402	$40.00
JESD 74A	**EARLY LIFE FAILURE RATE CALCULATION PROCEDURE FOR SEMICONDUCTOR COMPONENTS:** This standard defines methods for calculating the early life failure rate of a product, using accelerated testing, whose failure rate is constant or decreasing over time. For technologies where there is adequate field failure data, alternative methods may be used to establish the early life failure rate. The purpose of this standard is to define a procedure for performing measurement and calculation of early life failure rates. Projections can be used to compare reliability performance with objectives, provide line feedback, support service cost estimates, and set product test and screen strategies to ensure that the ELFR meets customers' requirements. February 2007 September 2006 /JC-14.3 Subcommittee	$61.00

JESD 75	**BALL GRID ARRAY PINOUTS STANDARDIZED FOR 32-BIT LOGIC FUNCTIONS:** The purpose of this standard is to provide a pinout standard for dual-die 32-bit logic devices offered in a 96- and 144-ball grid array package for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease use. This standard defines device output for 32-bit wide buffer, driver and transceiver functions. This pinout specifically applies to the conversion of DIP-packaged 16-bit logic devices to LFBGA-packaged dual-die 32-bit logic devices. November 1999 /JC-40 Committee	$38.00
JESD 75-1	**BALL GRID ARRAY PINOUTS STANDARDIZED FOR 16, 18, AND 20-BIT LOGIC FUNCTIONS USING A 54 BALL PACKAGE:** This standard establishes a 54 Ball Grid Array pinout for 16, 18 and 20-bit standard logic devices that are currently being produced in 48 and 56 Pin SSOP and TSSOP packages. The 54 Ball Grid Array Package is organized as a 6 x 9 array with balls on a .8mm x .8mm grid pitch. October 2001 /JC-40 Committee	$38.00
JESD 75-2	**BALL GRID ARRAY PINOUTS STANDARDIZED FOR 16-BIT LOGIC FUNCTIONS:** This standard provides a pinout standard for 16-bit wide logic devices offered in a 56-ball areagrid array package to provide for uniformity, multiplicity of sources, elimination of confusion,ease of device specification, and ease of use. July 2001 /JC-40 Committee	$38.00
JESD 75-3	**BALL GRID ARRAY PINOUTS STANDARDIZED FOR 8-BIT LOGIC FUNCTIONS:** This standard provides a pinout standard for 8-bit logic devices offered in a 20-ball area gridarray package to provide for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. July 2001 /JC-40 Committee	$37.00
JESD 75-4	**BALL GRID ARRAY PINOUT FOR 1-, 2-, AND 3-BIT LOGIC FUNCTIONS:** This standard defines device pinout for 1-, 2- and 3-bit wide logic functions. This pinout specifically applies to the conversion of Dual-Inline-Packaged (DIP) 1-, 2- and 3-bit logic devices to DSBGA-packaged 1-, 2- and 3-bit logic devices. March 2004 June 2003 /JC-40 Committee	$41.00
JESD 75-5	**SON/QFN PACKAGE PINOUTS STANDARDIZED FOR 1-, 2-, AND 3-BIT LOGIC FUNCTIONS** This standard defines device pinout for 1-, 2- and 3-bit wide logic functions. This pinout specifically applies to the conversion of Dual-Inline-Packaged (DIP) 1-, 2- and 3-bit logic devices to SON/QFN packaged 1-, 2- and 3-bit logic devices. The purpose of this document is to provide a pinout standard for 1-, 2- and 3-bit logic devices offered in 5-, 6- or 8-land SON/QFN packages for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. July 2004 December 2003 /JC-40.1 Subcommittee	$41.00
JESD 75-6	**PSO-N/PQFN PINOUTS STANDARDIZED FOR 14-, 16-, 20-, AND 24-LEAD LOGIC FUNCTIONS:** This standard defines device pinouts for 14-, 16-, 20-, and 24-lead logic functions. This pinout standard specifically applies to the conversion of DIP-packaged logic devices to PSO-N/PQFN packages logic devices. The purpose of this standard is to provide a pinout standard for 14-, 16-, 20-, and 24-lead logic devices offered in 14-, 16-, 20-, and 24-lead PSO-N/PQFN packages for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. March 2006 September 2005 /JC-40.1 Subcommittee	$41.00
JESD 76	**DESCRIPTION OF 1.8 V CMOS LOGIC DEVICES:** This standard continues the voltage specification migration to the next level beyond the 2.5 V specification already established in JESD80. In this standard, the input and output conditions are described for CMOS Logic products in a 1.8 V (Normal Range) application. April 2000 /JC-40.1 Subcommittee	$38.00
JESD 76-1	**STANDARD DESCRIPTION OF 1.2 V CMOS LOGIC DEVICES (WIDE RANGE OPERATION):** This standard defines dc interface, switching parameters and test loading for digital logic devices based on 1.2 V (nominal) power supply levels. The purpose is to provide a standard specification for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. June 2001 /JC-40 Committee	$38.00
JESD 76-2	**STANDARD DESCRIPTION OF 1.2 V CMOS LOGIC DEVICES (NORMAL RANGE OPERATION):** This standard defines dc interface, switching parameters and test loading for digital logic devices based on 1.2 V (normal range) power supply levels. The purpose is to provide a standard specification for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. June 2001 /JC-40 Committee	$38.00
JESD 76-3	**STANDARD DESCRIPTION OF 1.5 V CMOS LOGIC DEVICES:** This standard continues the voltage specification migration to the next level beyond the 1.8 V specification already established. The purpose is to provide a standard for 1.5 V nominal supply voltage CMOS logic devices, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. August 2001 /JC-40.1 Subcommittee	$38.00
JESD 77B.01	**TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR DISCRETE SEMICONDUCTOR AND OPTOELECTRONIC DEVICES:** A revised and significantly expanded reference for technical writers and educators, manufacturers, buyers and users of discrete semiconductor and optoelectronic devices, is now available. Revision B of JEDEC Standard No. 77 includes extensive information on: letter symbol conventions; diodes and rectifiers (including signal, rectifier, microwave, tunnel and backward, voltage-regulator, voltage-reference, current regulator, and varactor diodes); transistors (including FETs, JFETs, and IGBTs); photosensitive devices, photoemitters, and optocouplers; thyristors and PUTs; and transient voltage suppressors. Terms and symbols, with their definitions, are arranged alphabetically by product type. Where applicable, graphical symbols are also included.	

alphabetically by product type. Where applicable, graphical symbols are also included.

July 2006 /JC-10 Committee $162.00

JESD 78B

IC LATCH-UP TEST: This standard has been adopted by the Defense Logistics Agency (DLA) as project 5962-1880. This standard establishes a defined method for latch-up testing of ICs. It defines Classes and Levels for a device's latch-up capability so that both the user and supplier understand a device's latch-up capabilities. It is applicable to NMOS, CMOS, Bipolar, and all variations and combinations of these technologies. Latch-up is an extremely important factor in determining product reliability. This document contains the corrected figure 4 to include T6 on page 12, this change was made in January 1998.

December 2008 January 2008 /JC-14.1 Subcommittee $66.00

JESD 79-2E

DDR2 SDRAM SPECIFICATION This comprehensive standard defines all required aspects of 256Mb through 4Gb DDR2 SDRAMs with x4/x8/x16 data interfaces, including pinout, addressing, functional description, features, ac and dc parametrics, truth tables, and packages. Standard JESD79-2 uses a SSTL_18 interface, which is described in another JEDEC standard called JESD8-15. The purpose of this Standard is to define the minimum set of requirements for compliant devices 256Mb through 4Gb, x4/x8/x16 DDR2 SDRAMs. System designs based on the required aspects of this specification will be supported by all DDR2 SDRAM vendors providing compliant devices. Changes between versions is indicated in Annex A.

April 2008 June 2007 /JC-42.3 Subcommittee $177.00

JESD 79-3C

DDR3 SDRAM STANDARD This document defines the DDR3 SDRAM specification, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this Specification is to define the minimum set of requirements for JEDEC compliant 512 Mb through 8 Gb for x4, x8, and x16 DDR3 SDRAM devices. This specification was created based on the DDR2 specification (JESD79-2) and some aspects of the DDR specification (JESD79). Each aspect of the changes for DDR3 SDRAM operation were considered and approved by committee ballots). The accumulation of these ballots were then incorporated to prepare this JESD79-3 specification, replacing whole sections and incorporating the changes into Functional Description and Operation.

November 2008 March 2008 /JC-42.3 Subcommittee $229.00

JESD 79F

DOUBLE DATA RATE (DDR) SDRAM SPECIFICATION: This comprehensive standard defines all required aspects of 64Mb through 1Gb DDR SDRAMs with X4/X8/X16 data interfaces, including features, functionality, ac and dc parametrics, packages and pin assignments. This scope will subsequently be expanded to formally apply to x32 devices, and higher density devices as well. The purpose of this Standard is to define the minimum set of requirements for JEDEC compliant 64Mb through 1Gb, X4/X8/X16 DDR SDRAMs. System designs based on the required aspects of this specification will be supported by all DDR SDRAM vendors providing JEDEC compliant devices.

February 2008 /JC-42.3 Subcommittee $109.00

JESD 8-16A

BUS INTERCONNECT LOGIC (BIC) FOR 1.2 V This standard defines the electrical parameters for high-speed interfaces for use in the 1.2V electrical environment. Included in the standard are a single ended signaling interface suitable for parallel busses, and a differential signaling interface suitable for clock applications or parallel differential buses. JEDEC ?BIC? Standard JESD8-16A continues the tradition of the JESD8-xx standards, defining electrical interfaces for the industry as new technologies and bus requirements develop. Previously, JEDEC defined standard JESD8-6, the ?HSTL? standard, for use in 1.5V electrical environments. BIC is similar to HSTL, except the power supply voltage has dropped from 1.5V to 1.2V, and interface requirements are tightened to allow much higher speeds.

November 2004 June 2004 /JC-16 Committee $52.00

JESD 80

STANDARD FOR DESCRIPTION OF 2.5 V CMOS LOGIC DEVICES: The purpose of this standard is to provide a standard for 2.5 V nominal supply-voltage CMOS logic devices, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. This standard defines dc interface parameters and test loading for CMOS digital logic family based on 2.5 V (nominal) power supply levels at 2.5 V input tolerance.

November 1999 /JC-40 Committee $38.00

JESD 82

DEFINITION OF CDCV857 PLL CLOCK DRIVER FOR REGISTERED DDR DIMM APPLICATIONS: This specification is a reference for Registered DDR DIMM designers. JESD82 defines the physical, electrical, interface and timing requirements of a 1:10 PLL clock driver for DDR Registered DIMMs from DDR200 to DDR266 as refined in revision C of JEDEC Standard 21-C (JESD21-C). JESD82 was also written to meet the future performance requirements of Registered DIMMs for DDR300 and DDR333.

July 2000 /JC-40 Committee $47.00

JESD 82-10A

DEFINITION OF THE SSTU32866 1.8 V CONFIGURABLE REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTU32866 registered buffer with parity test for DDR2 RDIMM applications. The purpose is to provide a standard for the SSTU32866 (see Note) logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

May 2007 September 2006 /JC-40.4 Subcommittee $63.00

JESD 82-11

DEFINITION OF 'CU878 PLL CLOCK DRIVER FOR REGISTERED DDR2 DIMM APPLICATIONS This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of a ? CU878 PLL clock device for registered DDR2 DIMM applications. The purpose is to provide a standard for a ? CU878 PLL clock device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

September 2004 February 2004 /JC-40.3 Subcommittee $48.00

JESD 82-12A	**DEFINITION OF THE SSTU32S869 & SSTU32D869 REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS** This standard defines standard specifications of DC interface parameters, switching parameters, and test loading for definition of the SSTU32S869 and SSTU32D869 registered buffer with parity for driving heavy load on high-density DDR2 RDIMM applications. A typical application would be a 36 SDRAM planar DIMM. The purpose is to provide a standard for the SSTU32S869 and SSTU32D869 logic devices, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. April 2007 September 2006 /JC-40 Committee	$57.00
JESD 82-13A	**DEFINITION OF THE SSTVN16859 2.5-2.6 V 13-BIT TO 26-BIT SSTL_2 REGISTERED BUFFER FOR PC1600, PC2100, PC2700 AND PC3200 DDR DIMM APPLICATIONS** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTVN16859 13-bit to 26-bit SSTL_2 registered buffer for PC1600, PC2100, PC2700 and PC3200 DDR DIMM applications. The SSTVN16859 is a speed upgrade of the SSTV16859 (JESD82-4) for use in PC3200 DDR DIMMs. It is fully backward compatible with SSTV16859 for all speed grades. May 2005 September 2004 /JC-40 Committee	$48.00
JESD 82-14A	**DEFINITION OF THE SSTUB32868 1.8 V CONFIGURABLE REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTUB32868 registered buffer with parity test for DDR2 RDIMM applications. SSTU32S2868 denotes a single-die implementation and SSTU32D868 denotes a dual-die implementation. October 2006 June 2005 /JC-40 Committee	$57.00
JESD 82-15	**STANDARD FOR DEFINITION OF CUA878 PLL CLOCK DRIVER FOR REGISTERED DDR2 DIMM APPLICATIONS** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of a CUA878 PLL clock device for registered DDR2 DIMM applications. The purpose is to provide a standard for a CUA878 PLL clock device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. November 2005 September 2004 /JC-40 Committee	$49.00
JESD 82-16A	**DEFINITION OF THE SSTUA32866 1.8 V CONFIGURABLE REGISTERED BUFFER WITH PARITY TEST FOR DDR2 RDIMM APPLICATIONS** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTUA32866 registered buffer with parity test for DDR2 RDIMM applications. The purpose is to provide a standard for the SSTUA32866 (see Note) logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. May 2007 June 2006 /JC-40 Committee	$63.00
JESD 82-17	**DEFINITION OF THE SSTUA32S868 AND SSTUA32D868 REGISTERED BUFFER WITH PARITY FOR 2R X 4 DDR2 RDIMM APPLICATIONS** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTUA32S868 and SSTUA32D868 registered buffer with parity test for DDR2 RDIMM applications. November 2005 June 2004 /JC-40.3 Subcommittee	$57.00
JESD 82-18A	**STANDARD FOR DEFINITION OF THE CUA877 AND CU2A877 PLL CLOCK DRIVERSFOR REGISTERED DDR2 DIMM APPLICATIONS** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the CUA877 and CU2A877 PLL clock devices for registered DDR2 DIMM applications.The purpose is to provide a standard for the CUA877 and CU2A877 PLL clock devices, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. January 2007 June 2006 /JC-40 Committee	$49.00
JESD 82-19A	**DEFINITION OF THE SSTUA32S865 AND SSTUA32D865 28-BIT 1:2 REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTUA32S865 and SSTUA32D865 registered buffer with parity for 2 rank by 4 or similar high-density DDR2 RDIMM applications. May 2007 June 2006 /JC-40 Committee	$55.00
JESD 82-1A	**DEFINITION OF CVF857 PLL CLOCK DRIVER FOR REGISTERED PC1600, PC2100, PC2700, AND PC3200 DIMM APPLICATIONS:** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of a CV857 PLL clock device for registered PC1600, PC2100, PC2700 and PC3200 DIMM applications. The purpose is to provide a standard for a CV857 PLL clock device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. May 2004 /JC-40 Committee	$52.00
JESD 82-2	**STANDARD FOR DESCRIPTION OF A 3.3 V, 18-BIT, LVTTL I/O REGISTER FOR PC133 REGISTERED DIMM APPLICATIONS:** This standard defines the register support devices needed for standard height and low profile registered PC133 SDRAM DIMM modules. The objective of the standard is to clearly define the functionality, pinout and electrical characteristics required for this type of SDRAM module. July 2001 /JC-40 Committee	$45.00
JESD 82-20A	**FBDIMM: ADVANCED MEMORY BUFFER (AMB)** This document is a core specification for a Fully Buffered DIMM (FBD) memory system. This document, along with the other core specifications, must be treated as a whole. Information critical to a Advanced Memory Buffer design appears in the other specifications, with specific cross-references provided. March 2009 August 2007 /JC-40 Committee	$221.00

JESD 82-21	**STANDARD FOR DEFINITION OF CUA845 PLL CLOCK DRIVER FOR REGISTERED DDR2 DIMM APPLICATIONS** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of a CUA845 PLL clock device for registered DDR2 DIMM applications.The purpose is to provide a standard for a CUA845 PLL clock device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. January 2007 March 2006 /JC-40 Committee	$48.00
JESD 82-22	**INSTRUMENTATION CHIP DATA SHEET FOR FBDIMM DIAGNOSTIC SENSELINES** This device is a one-chip spectrum analyzer that operates in the frequency range from 1 to 2 GHz. It requires no external components except some filtering of the voltage supply (one inductor, one bypass capacitor). The frequency of the VCO is adjusted by an internal DAC. No PLL loop is used to lock the VCO to a reference frequency. A counter is used to determine the VCO frequency. The device has a serial I2C data interface. The device is available in a 28 pin TQFN package and is specified over the extended industrial (-40 C to +85 C) temperature range. November 2006 March 2006 /JC-40.4 Subcommittee	$47.00
JESD 82-23	**DEFINITION OF the SSTUA32S869 AND SSTUA32D869 REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS** This standard defines standard specifications of DC interface parameters, switching parameters, and test loading for definition of the SSTUA32S869 and SSTUA32D869 registered buffer with parity for driving heavy load on high-density DDR2 RDIMM applications. A typical application would be a 36 SDRAM planar DIMM. The SSTUA32S869 and SSTUA32D869 are identical in functionality to the SSTU32S869 and SSTU32D869 devices respectively but specify tighter timing characteristics and a higher application frequency of up to 410MHz. May 2007 June 2006 /JC-40 Committee	$59.00
JESD 82-24	**DEFINITION OF the SSTUB32865 28-bit 1:2 REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTUB32865 registered buffer with parity for 2 rank by 4 or similar high-density DDR2 RDIMM applications. The SSTUB32865 is identical in functionality to the SSTU32865 but specifies tighter timing characteristics and a higher application frequency of up to 410MHz. May 2007 September 2006 /JC-40 Committee	$55.00
JESD 82-25	**DEFINITION OF the SSTUB32866 1.8 V CONFIGURABLE REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTUB32866 registered buffer with parity test for DDR2 RDIMM applications. May 2007 September 2006 /JC-40 Committee	$63.00
JESD 82-26	**DEFINITION OF THE SSTUB32868 REGISTERED BUFFER WITH PARITY FOR 2R x 4 DDR2 RDIMM APPLICATIONS** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTUB32868 registered buffer with parity test for DDR2 RDIMM applications. May 2007 September 2006 /JC-40 Committee	$57.00
JESD 82-27	**DEFINITION OF THE SSTUB32869 REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS:** This standard defines standard specifications of DC interface parameters, switching parameters, and test loading for definition of the SSTUB32869 registered buffer with parity for driving heavy load on high-density DDR2 RDIMM applications. A typical application would be a 36 SDRAM planar DIMM. May 2007 September 2006 /JC-40 Committee	$59.00
JESD 82-28A	**FULLY BUFFERED DIMM DESIGN FOR TEST, DESIGN FOR VALIDATION (DFx)** This FBDIMM DFx document covers Design for Test, Design for Manufacturing and Design for Validation (DFx) requirements and implementation guidelines for Fully Buffered DIMM technology. July 2008 March 2006 /JC-40.5 Subcommittee	$151.00
JESD 82-3B	**DEFINITION OF THE SSTV16857 2.5 V, 14-BIT SSTL_2 REGISTERED BUFFER FOR DDR DIMM APPLICATIONS:** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTV16857 14-bit SSTL_2 registered buffer for DDR DIMM applications.The purpose is to provide a standard for the SSTV16857 logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. November 2004 December 2003 JC-40.3	$48.00
JESD 82-4B	**STANDARD FOR DEFINITION OF THE SSTV16859 2.5 V, 13-BIT TO 26-BIT SSTL_2 REGISTERED BUFFER FOR STACKED DDR DIMM APPLICATIONS:** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTV16859 13-bit to 26-bit SSTL_2 registered buffer for stacked DDR DIMM applications. The purpose is to provide a standard for the SSTV16859 logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. May 2003 /JC-40 Committee	$47.00
JESD 82-5	**STANDARD FOR DESCRIPTION OF A 3.3 V, ZERO DELAY CLOCK DISTRIBUTION DEVICE COMPLIANT WITH THE JESD21-C PC133 REGISTERED DIMM SPECIFICATION** This standard defines the PLL support devices required for standard height and low profile registered PC133 SDRAM DIMM modules. The objective of the standard is to clearly define the functionality, pinout and electrical characteristics of the PLL used on JEDEC standard modules.JESD82-5 is the latest specification to be added to the JESD82 family of specifications for memory module support devices. Additional specifications are currently under development for DDR2 support devices. July 2002 /JC-40 Committee	$43.00
JESD 82-6A	**DEFINITION OF THE SSTV32852 2.5 V 24-BIT TO 48-BIT SSTL_2 REGISTERED BUFFER FOR 1U STACKED DDR**	

DIMM APPLICATIONS: This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTV32852 24-bit to 48-bit SSTL_2 registered buffer for stacked DDR DIMM applications. The purpose is to provide a standard for the SSTV32852 logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

November 2004 December 2003 /JC-40 Committee $47.00

JESD 82-7A

DEFINITION OF THE SSTU32864 1.8-V CONFIGURABLE REGISTERED BUFFER FOR DDR2 RDIMM APPLICATIONS: This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTU32864 configurable registered buffer for DDR2 RDIMM applications. The purpose is to provide a standard for the SSTU32864 logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

October 2004 /JC-40.4 Subcommittee $47.00

JESD 82-9B

DEFINITION OF SSTU32865 REGISTERED BUFFER WITH PARITY FOR 2R x 4 DDR2 RDIMM APPLICATIONS This standard provides the functional definition, ball-out configuration and package outline, signal definitions and input/output characteristics for a 28-bit 1:2 registered driver with parity suitable for use on DDR2 RDIMMs. The SSTU32865 integrates the functional equivalent of two SSTU32864 devices (as defined in JESD82-7) into a single device, thereby easing layout and board design constraints especially on high density RDIMMs such as dual rank, by four configurations. Moreover, the optional use of a parity function is provided for, permitting detection and reporting of parity errors across its 22 data inputs. JESD82-9 specifies a 160-pin Thin-profile, fine-pitch ball-grid array (TFBGA) package.

May 2007 September 2006 /JC-40.4 Subcommittee $52.00

JESD 84-A41

EMBEDDED MULTIMEDIACARD (e•MMC) PRODUCT STANDARD, STANDARD CAPACITY This document provides a definition of the Embedded MultiMediaCard product, its environment, and handling. It also provides design guidelines and defines a tool box of macro functions and algorithms intended to reduce design-in costs.

July 2007 If you downloaded this file prior to 8/23/07 please download again. May 2007 /JC-64 Committee $55.00

JESD 84-A42

EMBEDDED MULTIMEDIACARD (e•MMC) PRODUCT STANDARD, HIGH CAPACITY This document provides a definition of the Embedded MultiMediaCard product, its environment, and handling. It also provides design guidelines and defines a tool box of macro functions and algorithms intended to reduce design-in costs.

July 2007 If you downloaded this file prior to 8/23/07 please download again. June 2007 /JC-64 Committee $57.00

JESD 84-A44

EMBEDDED MULTIMEDIACARD(e•MMC) e•MMC/CARD PRODUCT STANDARD, HIGH CAPACITY, INCLUDING RELIABLE WRITE, BOOT, SLEEP MODES, DUAL DATA RATE, MULTIPLE PARTITIONS SUPPORTS AND SECURITY ENHANCEMENT (MMCA, 4.4) The purpose of this specification is the definition of the MMC/e•MMC Electrical Interface, its environment and handling. It provides guidelines for systems designers. The specification also defines a tool box (a set of macro functions and algorithms) that contributes to reducing design-in costs. Item 25.02

March 2009 August 2008 /JC-64 Committee $239.00

JESD 84-B41

MULTIMEDIACARD (MMC) ELECTRICAL STANDARD, STANDARD CAPACITY (MMCA, 4.1) This document provides a comprehensive definition of the MultiMediaCard, its environment, and handling. It also provides design guidelines and defines a tool box of macro functions and algorithms intended to reduce design-in costs.

June 2007 June 2007 /JC-64.1 Subcommittee $162.00

JESD 84-B42

MULTIMEDIACARD (MMC) ELECTRICAL STANDARD, HIGH CAPACITY (MMCA, 4.2) The purpose of the specification is the definition of the e•MMC, its environment and handling. It provides guidelines for systems designers. The specification also defines a tool box (a set of macro functions and algorithms) that contributes to reducing design-in costs.

July 2007 March 2007 /JC-64.1 Subcommittee $162.00

JESD 85

METHODS FOR CALCULATING FAILURE RATES IN UNITS OF FITS: This standard establishes methods for calculating failure rates in units of FITs by using data in varying degrees of detail such that results can be obtained from almost any data set. The objective is to provide a reference to the way failure rates are calculated.

July 2001 /JC-14.3 Subcommittee $55.00

JESD 86

ELECTRICAL PARAMETERS ASSESSMENT: This standard is intended to describe various methods for obtaining electrical variate data on devices currently produced on the manufacturing and testing process to be qualified. The intent is to assess the device?s capability to function within the specification parameters over time and the application environment (operating range of temperature, voltage, humidity, input/output levels, noise, power supply stability etc.).

August 2001 /JC-14.3 Subcommittee $38.00

JESD 87

STANDARD TEST STRUCTURE FOR RELIABILITY ASSESSMENT OF AlCu METALLIZATIONS WITH BARRIER MATERIALS This document describes design of test structures needed to assess the reliability of aluminum-copper, refractory metal barrier interconnect systems. This includes any metal interconnect system where a refractory metal barrier or other barrier material prevents the flow of aluminum and/or copper metal ions from moving between interconnect layers. This document is not intended to show design of test structures to assess aluminum or aluminum-copper alloy systems, without barriers to Al and Cu ion movement, nor for Cu only metal systems. Some total interconnect systems might not include barrier materials on all metal layers. The structures in this standard are designed for cases where a barrier material separates two Al or Al alloy metal layers. The purpose of this document is to describe the design of test structures needed to assess electromigration (EM) and stress-induced-void (SIV) reliability of AlCu barrier metal systems.

July 2001 /JC-14.2 Subcommittee $43.00

JESD 88C	**DICTIONARY OF TERMS FOR SOLID STATE TECHNOLOGY, Fourth Edition:** This reference for technical writers and educators, manufacturers, and buyers and users of discrete solid state devices is now available. It should aid the technical committees of JEDEC in the avoidance of multiple definitions and reduce the proliferation of redundant definitions. The long-term goal is to include definitions from all JEDEC publications and standards. Even in this fourth edition, that goal has been largely met. Each of the approximately two thousand entries is referenced to its source publication, and an annex listing the names of the source publications and their releases dates is included. All entries were reviewed for punctuation, grammar, and clarity, as well as accuracy, and reworded if such was considered warranted. The purpose of this dictionary is to promote the uniform use of terms, definitions, abbreviations, and symbols throughout the solid state industry. July 2007 /JC-10 Committee	$150.00
JESD 89-1A	**TEST METHOD FOR REAL-TIME SOFT ERROR RATE:** This test is used to determine the Soft Error Rate (SER) of solid state volatile memory arrays and bistable logic elements (e.g. flip-flops) for errors which require no more than re-reading or re-writing to correct and as used in terrestrial environments. It simulates the operating condition of the device and is used for qualification, characterization, or reliability monitoring. This test is intended for execution in ambient conditions without the artificial introduction of radiation sources. October 2007 February 2007 /JC-14.1 Subcommittee	$52.00
JESD 89-2A	**TEST METHOD FOR ALPHA SOURCE ACCELERATED SOFT ERROR RATE:** This test method is offered as standardized procedure to determine the alpha particle Soft Error Rate (SER) sensitivity of solid state volatile memory arrays and bistable logic elements (e.g. flipflops) by measuring the error rate while the device is irradiated by a characterized, solid alpha source. October 2007 February 2007 /JC-14.1 Subcommittee	$55.00
JESD 89-3A	**TEST METHOD FOR BEAM ACCELERATED SOFT ERROR RATE** This test is used to determine the terrestrial cosmic ray Soft Error Rate (SER) sensitivity of solid state volatile memory arrays and bistable logic elements (e.g. flip-flops) by measuring the error rate while the device is irradiated in a neutron or proton beam of known flux. The results of this accelerated test can be used to estimate the terrestrial cosmic ray induced SER for a given terrestrial cosmic ray radiation environment. This test cannot be used to project alpha-particleinduced SER. November 2007 January 2007 /JC-14.1 Subcommittee	$66.00
JESD 89A	**MEASUREMENT AND REPORTING OF ALPHA PARTICLE AND TERRESTRIAL COSMIC RAY INDUCED SOFT ERRORS IN SEMICONDUCTOR DEVICES:** This specification defines the standard requirements and procedures for terrestrial soft-error-rate (SER)testing of integrated circuits and reporting of results. Both real-time (unaccelerated) and acceleratedtesting procedures are described. At terrestrial, Earth-based altitudes, the predominant sources of radiation include both cosmic-ray radiation and alpha-particle radiation from radioisotopic impurities in the package and chip materials. An overall assessment of a device?s SER is complete, only when an unaccelerated test is done, or accelerated SER data for the alpha-particle component and the cosmic-radiation component has been obtained. October 2006 January 2006 /JC-13.4 Subcommittee	$109.00
JESD 90	**A PROCEDURE FOR MEASURING P-CHANNEL MOSFET NEGATIVE BIAS TEMPERATURE INSTABILITIES** This document describes an accelerated stress and test methodology for measuring device parameter changes of a single p-channel MOSFET after Negative Bias Temperature Instability (NBTI) stress at dc bias conditions. This document gives a procedure to investigate NBTI stress in a symmetric voltage condition with the channel inverted (VGS < 0) and no channel conduction (VDS = 0).There can be NBTI degradation during channel conduction (VGS < 0, VDS < 0), however, this document does not cover this phenomena. November 2004 August 2002 /JC-14.2 Subcommittee	$48.00
JESD 91-A	**METHOD FOR DEVELOPING ACCELERATION MODELS FOR ELECTRONIC COMPONENT FAILURE MECHANISMS:** The method described in this document applies to all reliability mechanisms associated with electronic components.The purpose of this standard is to provide a reference for developing acceleration models for defect-related and wear-out mechanisms in electronic components. August 2003 /JC-14.3 Subcommittee	$49.00
JESD 92	**PROCEDURE FOR CHARACTERIZING TIME-DEPENDENT DIELECTRIC BREAKDOWN OF ULTRA-THIN GATE DIELECTRICS:** This document defines a constant voltage stress test procedure for characterizing time-dependent dielectric breakdown or ?wear-out? of thin gate dielectrics used in integrated circuit technologies. The test is designed to obtain voltage and temperature acceleration parameters required to estimate oxide life at use conditions. The test procedure includes sophisticated techniques to detect breakdown in ultra-thin films that typically exhibit large tunneling currents and soft or noisy breakdown characteristics. This document includes an annex that discusses test structure design, methods to determine the oxide electric field in ultra-thin films, statistical models, extrapolation models, and example failure-rate calculations. August 2003 July 2002 /JC-14.2 Subcommittee	$57.00
JESD 94A	**APPLICATION SPECIFIC QUALIFICATION USING KNOWLEDGE BASED TEST METHODOLOGY:** The method described in this document applies to all application specific reliability testing for solid state components with known failure mechanisms where the test duration and conditions vary based on application variables. This document does not cover reliability tests that are characterization based or essentially go / no-go type tests, for example, ESD, latch-up, or electrical over stress. Also, it does not attempt to cover every failure mechanism or test environment, but does provide a methodology that can be extended to other failure mechanisms and test environments. July 2008 January 2008 /JC-14.3 Subcommittee	$62.00
JESD 95-1	**DESIGN REQUIRMENTS FOR OUTLINES OF SOLID STATE AND RELATED PRODUCTS: DISCONTINUED AS A SEPARATE**	

ITEM CONTAINED IN JEP95, BOOK 1, SECTION 4.

September 2000; Incorporated /JC-11 Committee

JESD 96A

RADIO FRONT END - BASEBAND (RF-BB) INTERFACE The normative information in this standard is intended to provide a technical design team to construct the interface on a FED and a BED such that they will operate correctly with each other (at the interface level), when designed to this specification. Additional informative information is provided in the appendices to help illustrate the normative material. This document addresses the following interface topics: 1) RF-BB Electrical layer: time and amplitude specifications for lines, drivers, receivers, clocks; 2)RF-BB Link layer: bits, clock-data synchronization, power modes; 3) RF-BB Transport layer: data types, data framing, data bandwidth, connection to core IC; 4) RF-BB Interface Registers. This document defines a high-speed serial link that enables the bi-directional transfer of data and control information between the FED and BED. The document does not mandate the use of specific signaling, standard framing or standard messaging needed to make this an interoperable interface standard for RF devices or BB devices.

February 2006 February 2005 /JC-61 Committee $71.00

JESD 97

MARKING, SYMBOLS, AND LABELS FOR IDENTIFICATION OF LEAD (Pb) FREE ASSEMBLIES, COMPONENTS, AND DEVICES - SUPERSEDED BY J-STD-609, August 2007

May 2004; Superseded by J-STD-609, August 2007 June 2003 /JC-14.1 Subcommittee $45.00

JESD 99-1

ADDENDUM No. 1 to JESD99 - TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR ANALOG-TO-DIGITAL AND DIGITAL-TO-ANALOG CONVERTERS: This addendum has now been incorporated into JESD99.

July 1989; Incorporated into JESD99-A, May 2000 /JC-10 Committee

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JESD 99B

TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR MICROELECTRONIC DEVICES: This standard will be useful to users, manufacturers, educators, technical writers, and others interested in the characterization, nomenclature, and classification of microelectronics devices. There are general guidelines for both letter symbols and abbreviations applicable to all integrated circuits, and detailed sections for digital ICs, linear (analog) ICs, interface ICs (including D/A and A/D converters), voltage regulators, charge-transfer devices. The standard lists and defines more than 400 of the most common physical and electrical terms applicable to these devices and shows the industry-standard symbol and abbreviations that have been established for such terms.

May 2007 /JC-10 Committee $127.00

JESD 100B.01

TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR MICROCOMPUTERS, MICROPROCESSORS, AND MEMORY INTEGRATED CIRCUITS: A revised reference for technical writers and educators, manufacturers, buyers and users of microprocessors, microcomputers, mircocontrollers, memory ICs, and other complex devices. The terms and their definitions in this standard have been updated and are in general agreement with the latest publications of the IEEE and the IEC. The companion standard for other integrated circuits is JESD99A. Also included is a system for generating symbols for time intervals found in complex sequential circuits, including memories. JESD100B.01 is the first minor revision of JESD100-B, December 1999. Annex A briefly shows entries that have changed.

December 2002 /JC-10 Committee $71.00

JESD 201A

ENVIRONMENTAL ACCEPTANCE REQUIREMENTS FOR TIN WHISKER SUSCEPTIBILITY OF TIN AND TIN ALLOY SURFACE FINISHED: The methodology described in this document is applicable for environmental acceptance testing of tin based surface finishes and mitigation practices for tin whiskers. This methodology may not be sufficient for applications with special requirements, (i.e., military, aerospace, etc.). Additional requirements may be specified in the appropriate requirements (procurement) documentation.

August 2008 September 2007 /JC-14.3 Subcommittee $71.00

JESD 202

METHOD FOR CHARACTERIZING THE ELECTROMIGRATION FAILURE TIME DISTRIBUTION OF INTERCONNECTS UNDER CONSTANT-CURRENT AND TEMPERATURE STRESS: This is an accelerated stress test method for determining sample estimates and their confidence limits of the median-time-to-failure, sigma, and early percentile of a log-Normal distribution, which are used to characterize the electromigration failure-time distribution of equivalent metal lines subjected to a constant current-density and temperature stress. Failure is defined as some pre-selected fractional increase in the resistance of the line under test. Analysis procedures are provided to analyze complete and singly, right-censored failure-time data. Sample calculations for complete and right-censored data are provided in Annex A. The analyses are not intended for the case when the failure distribution cannot be characterized by a single log-Normal distribution.

March 2006 June 2004 /JC-14.2 Subcommittee $61.00

JESD 203

STANDARD TEST LOADS FOR DUAL-SUPPLY LEVEL TRANSLATION DEVICES This standard defines ac test loads for dual-supply level translation devices. Uniform test loads enable easy comparison of electrical parameters of dual-supply level translation devices across functions, logic families and IC suppliers. This standard is only intended to apply to devices released subsequent to the publication of this document.

November 2005 June 2004 /JC-40.1 Subcommittee $40.00

JESD 204A

SERIAL INTERFACE FOR DATA CONVERTERS This specification describes a serialized interface between data converters and logic devices. It contains normative information to enable designers to implement devices that communicate with other devices covered by this specification. Informative sections are included to clarify and exemplify the specification.

April 2008 August 2007 /JC-16 Committee $130.00

JESD 205

FBDIMM STANDARD: DDR2 SDRAM FULLY BUFFERED DIMM (FBDIMM) DESIGN SPECIFICATION: This specification defines the electrical and mechanical requirements for 240-pin, PC2-4200/PC2-5300/PC2-6400, 72 bit-wide, Fully Buffered Double Data Rate Synchronous DRAM Dual In-Line Memory Modules (DDR2 SDRAM FB-

	DIMMs).These SDRAM FB-DIMMs are intended for use as main memory when installed in systems such as servers and workstations. PC2-4200/PC2-5300/PC2-6400 refers to the DIMM naming convention in which PC2-4200/PC2-5300/PC2-6400 indicates a 240-pin DDR2 DIMM running at 266/333/400 MHz DRAM clock speed and offering 4266/5333/6400 MB/s bandwidth. March 2007 March 2006 /JC-45.4 Subcommittee	$147.00
JESD 206	FBDIMM Architecture and Protocol January 2007 March 2006 /JC-40 Committee	$147.00
JESD 208	SPECIALITY DDR2-1066 SDRAM This document defines the Specialty DDR2-1066 SDRAM specification, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this Specification is to define the minimum set of requirements for JEDEC compliant 256 Mb through 4 Gb for x4, x8, and x16 Specialty DDR2-1066 SDRAM devices. November 2007 March 2007 /JC-42.3 Subcommittee	$130.00
JESD 209-2	LOW POWER DOUBLE DATA RATE 2 (LPDDR2) This document defines LPDDR2, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. This specification covers the following technologies: LPDDR2-S2A, LPDDR2-S2B, LPDDR2-S4A, LPDDR2-S4B, LPDDR2-N-A, and LPDDR2-N-B. Item 1725.01A. March 2009 August 2008 /JC-42.6 Subcommittee	$239.00
JESD 209A	LOW POWER DOUBLE DATA RATE (LPDDR) SDRAM STANDARD This standard defines the Low Power Double Data Rate (LPDDR) SDRAM, including features, functionality, AC and DC characteristics, packages, and pin assignments. This scope may be expanded in future to also include other higher density devices. The purpose of this document is to define the minimum set of requirements for JEDEC compliant 64Mb through 2Gb for x16 and x32 Low Power Double Data Rate SDRAM devices. System designs based on the required aspects of this standard will be supported by all LPDDR SDRAM vendors providing compliant devices. (JESD209 was originally numbered as JESD79-4 May 2006 to August 2007, corrected to JESD209 09/17/2007). February 2009 June 2005 /JC-42.3 Subcommittee	$112.00
JESD 209A-1	Addendum No. 1 to JESD209A - LOW POWER DOUBLE DATA RATE (LPDDR) SDRAM, 1.2 V I/O. This document defines the Low Power Double Data Rate (LPDDR) SDRAM 1.2 V I/O, including AC and DC operating conditions, extended mode register settings, and I-V characteristics. The purpose of this Standard is to define the minimum set of requirements for JEDEC compliant 64 Mb through 2 Gb for x16 and x32 Low Power Double Data Rate SDRAM devices with 1.2 V I/O. System designs based on the required aspects of this specification will be supported by all LPDDR SDRAM vendors providing compliant devices. March 2009 June 2008 /JC-42.6 Subcommittee	$51.00
JESD 210	AVALANCHE BREAKDOWN DIODE (ABD) TRANSIENT VOLTAGE SUPPRESSORS This standard is applicable to avalanche breakdown diodes when used as a surge protector or transient voltage suppressor (TVS). It describes terms and definitions and explains methods for verifying device ratings and measuring device characteristics. This standard may be applied to other surge-protection components with similar characteristics as the ABD. December 2007 April 2003 /JC-22.5 Subcommittee	$72.00
JESD 22-A122	POWER CYCLING This Test Method establishes a uniform method for performing component package power cycling stress test. This specification covers power induced temperature cycling of a packaged component, simulating the non-uniform temperature distribution resulting from a device powering on and off in the application. August 2007 January 2007 /JC-14.1 Subcommittee	$47.00
JESD 282B.01	SILICON RECTIFIER DIODES: This standard provided definitions, electrical characteristics circuit technology, letter symbols and registration format for diodes and stacks. It also covers rating and characteristics, manufacturing and performance as well as test practices to demonstrate the performance of semiconductor rectifier diodes and rectifier stacks used for the conversion and/or control of electric power. This version contains minor revisions to JESD282-B, April 2000. November 2002 /JC-22.2 Subcommittee	$177.00
JESD 284-A	TEST METHODS FOR THE COLLECTOR-BASE TIME CONSTANT AND FOR THE RESISTIVE PART OF THE COMMON-EMITTER INPUT IMPEDANCE: The test methods described in this Standard are generally applicable to alloy-like devices for which the usual simplified equivalent circuits can be employed. November 1963; Reaffirmed November 1963, June 1972, April 1981, April 1999, October 2002 /JC-25 Committee	$38.00
JESD 286-B	STANDARD FOR MEASURING FORWARD SWITCHING CHARACTERISTICS OF SEMICONDUCTOR DIODES: This method updates the standard procedure for characterizing the switching of signal or switching diodes when a step function of forward current is applied. The objective is to provide a standard so that accurate comparisons can be made. February 2000 /JC-22.4 Subcommittee	$40.00
JESD 307	VOLTAGE REGULATOR DIODE NOISE VOLTAGE MEASUREMENT: This standard is intended to cover the measurement of noise voltage in voltage regulator diodes in the reverse breakdown region. It describes noise voltage measurements at specified conditions, but may be used as a guide for making such measurements at other than specified conditions.(Formerly EIA-307) May 1965; Reaffirmed January 1992, April 1999, April 2002 April 2002 /JC-22.4 Subcommittee	$38.00

JESD 313-B	**THERMAL RESISTANCE MEASUREMENTS OF CONDUCTION COOLED POWER TRANSISTORS:** This standard provides a test method for measuring thermal resistance for conduction cooled power transistors. October 1975; Reaffirmed April 1981, April 2001 /JC-25 Committee	$45.00
JESD 320-A	**CONDITIONS FOR MEASUREMENT OF DIODE STATIC PARAMETERS:** This standard provides guidance for achieving equilibrium when measuring temperature sensitive static parameters of signal diodes. (Formerly EIA-302-A) December 1992; Reaffirmed April 1999, April 2002 (Original publication July 1965) /JC-22.4 Subcommittee	$37.00
JESD 381-A	**METHOD OF DIODE Q MEASUREMENT:** This standard was updated and revised for the purpose of clarifying the method used to measure Q of a Voltage-Variable-Capacitance Diode in the low VHF range using an RF admittance bridge. Originally published November 1981. Approved as ANSI/EIA-381-A-1992, July 1992. Became JESD381-A after ANSI expiration July 2002. November 1981; Reaffirmed April 1999, April 2002 April 1999 /JC-22.4 Subcommittee	$48.00
JESD 419-A	**STANDARD LIST OF VALUES TO BE USED IN SEMICONDUCTOR DEVICE SPECIFICATIONS AND REGISTRATION FORMAT:** This document contains standard lists of values which are recommended for use in semiconductor device specification and JEDEC Registration Formats. Good reasons should exist in those cases where values are used that are not included in these lists. October 1980; Reaffirmed March 2001 /JC-25 Committee	$37.00
JESD 482-A	**LIST OF PREFERRED VALUES FOR USE ON VARIOUS TYPES OF SMALL SIGNAL AND REGULATOR DIODES:** This standard specifies preferred values to be used on signal and regulator diodes. It will facilitate the standardization for nominal values used on small signal regulator diodes previously established in JEDEC Suggested Standard No. 2. (Formerly EIA-482-A) August 1984; Reaffirmed April 1999, April 2002 April 2002 /JC-22.4 Subcommittee	$38.00
JESD 51-12	**GUIDELINES FOR REPORTING AND USING ELECTRONIC PACKAGE THERMAL INFORMATION:** This document provides guidelines for both reporting and using electronic package thermal information generated using JEDEC JESD51 standards. By addressing these two areas, this document can be used as the common basis for discussion between electronic package thermal information suppliers and users. May 2005 October 2004 /JC-15.1 Subcommittee	$49.00
JESD 531	**THERMAL RESISTANCE TEST METHOD FOR SIGNAL AND REGULATOR DIODES (FORWARD VOLTAGE, SWITCHING METHOD):** This standard describes a test method for measuring the thermal resistance of signal and regulator diodes. The need for modification of this test method arose out of the limited description that existed earlier for both signal and regulator diode applications in testing for thermal resistance. Previously published as ID-13. ANSI/EIA-531-1986 (July) expired June 1996. Became JESD531 after reaffirmation April 2002. July 1986; Reaffirmed April 1999, April 2002 April 1999 /JC-22.4 Subcommittee	$47.00
JESD 625-A	**REQUIREMENTS FOR HANDLING ELECTROSTATIC-DISCHARGE-SENSITIVE (ESDS) DEVICES:** This standard establishes the minimum requirements for Electrostatic Discharge (ESD) control methods and materials used to protect electronic devices that are susceptible to damage or degradation from electrostatic discharge (ESD). The passage of a static charge through an electrostatic-discharge-sensitive (ESDS) device can result in catastrophic failure or performance degradation of the part. Device sensitivity to ESD is determined by test methods such as EIA/JESD22-A114. ESDS devices with human body model sensitivities of less than +200 volts may need additional protective measures beyond those specified in this standard. December 1999 /JC-14.1 Subcommittee	$55.00
JESD 659B	**FAILURE-MECHANISM-DRIVEN RELIABILITY MONITORING:** This method establishes requirements for application of Statistical Reliability Monitoring 'SRM' technology to monitor and improve the reliability of electronic components and subassemblies. The standard also describes the condition under with a monitor may be replaced or eliminated. February 2007 September 2006 /JC-14.3 Subcommittee	$45.00
JESD 671-A	**COMPONENT QUALITY PROBLEM ANALYSIS AND CORRECTIVE ACTION REQUIREMENTS (INCLUDING ADMINISTRATIVE QUALITY PROBLEMS):** This revision now encompasses administrative quality problems, in addition to the electrical and visual/mechanical quality problems that were addressed in the original release. A standard set of problem categories for each of these three types of component problems is presented for tracking and reporting purposes. A common set of customer and supplier expectations and requirements are set forth to help facilitate the successful problem analysis and corrective action of any type of component quality problem. December 1999 /JC-14.4 Subcommittee	$43.00
JESD 8-19	**POD18 - 1.8 V Pseudo Open Drain I/O** This standard defines the dc and ac single-ended (data) and differential (clock) operating conditions, I/O impedances, and the termination and calibration scheme for 1.8 V Pseudo Open Drain I/Os. The 1.8 V Pseudo Open Drain interface, also known as POD18, is primarily used to communicate with GDDR3 SGRAM devices. December 2006 December 2003 /JC-16 Committee	$43.00
JESD 8-20	**POD15 - 1.5 V Pseudo Open Drain I/O** This standard defines the dc and ac single-ended (data) and differential (clock) operating conditions, I/O impedances, and the termination and calibration scheme for 1.5 V Pseudo Open Drain I/Os. The 1.5 V Pseudo Open Drain interface, also known as POD15, is primarily used to communicate with GDDR4 SGRAM devices. December 2006 March 2006 /JC-16 Committee	$43.00

JESD 82-8.01	STANDARD FOR DEFINITION OF ?CU877 PLL CLOCK DRIVER FOR REGISTERED DDR2 DIMM APPLICATIONS This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of a ?CU877 PLL clock device for registered DDR2 DIMM applications. The purpose is to provide a standard for a ?CU877 PLL clock device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. This document includes minor editorial changes as noted in Annex A, page 16. February 2004 /JC-40 Committee	$49.00
JESD 84-A43	EMBEDDED MULTIMEDIACARD (e•MMC) e•MMC/CARD PRODUCT STANDARD, HIGH CAPACITY, INCLUDING RELIABLE WRITE, BOOT, AND SLEEP MODES (MMCA, 4.3) This document is a complete specification for embedded memory devices and removable memory cards using the MMC interface version 4.3. New features developed through the Electrical Joint Task Group include: Sleep mode, Boot mode and Reliable Write. December 2007 July 2007 /JC-64 Committee	
JESD 84-C01	MULTIMEDIACARD (MMC) MECHANICAL STANDARD This document is a mechanical product specification for a removable non-volatile flash memory device using the MMC interface version 4.2. The electrical specification for the MMC interface version 4.2 is document JESD84-B42. December 2007 August 2007 /JC-64 Committee	
JESD 84-C43	EMBEDDED MULTIMEDIACARD (e•MMC)MECHANICAL STANDARD This document is a mechanical product specification for a high capacity embedded memory device using the MMC interface version 4.2 and a BGA package. December 2007 August 2007 /JC-64.2 Subcommittee	
JESD 93	HYBRIDS/MCM This specification establishes the general requirements for hybrid microcircuits, RF/microwave hybrid microcircuits and MCMs (hereafter referred to as devices). Detailed performance requirements for a specific device are specified in the applicable device acquisition document. In the event of a conflict between this document and the device acquisition document, the device acquisition document will take precedence. September 2005 May 2002 /JC-13.5 Subcommittee	$49.00
JESD 96A-1	Addendum 1 to JESD96A - INTEROPERABILITY AND COMPLIANCE TECHNICAL REQUIREMENTS FOR JEDEC STANDARD JESD96A - RECOMMENDED PRACTICE FOR USE WITH IEEE 802.11N The normative information in this publication is intended to provide a technical design team to construct the interface on a FED and a BED such that they will operate correctly with each other (at the interface level), when designed to JESD96A. January 2007 March 2006 /JC-61 Committee	$45.00
JESD JIG-101	Material Composition Declaration Guide for Electronic Products The purpose of this guide establishes the materials and substances to be disclosed by suppliers when those materials and substances are present in products and subparts that are incorporated into EEE. It benefits suppliers and their commercial customers by providing consistency and efficiency to the material declaration process. It promotes the development of consistent data exchange formats and tools that will facilitate and improve data transfer along the entire global supply chain. June 2005 January 2003 /JC-14 Committee	

NUMBER	Joint IPC/JEDEC Standards (J-STD-)	PRICE
J-STD- 002B	SOLDERABILITY TESTS FOR COMPONENT LEADS, TERMINATIONS, LUGS, TERMINALS AND WIRES: At the request of IPC, J-STD-002B has been temporarily removed from the free download area until such time when it is revised to include lead-free. In its place, JEDEC's Test Method B102-D, Solderability, which includes lead-free, is available for free downloading. February 2003 Removed 01/21/04 /JC-14.1 Subcommittee	
J-STD- 020D.01	JOINT IPC/JEDEC STANDARD FOR MOISTURE/REFLOW SENSITIVITY CLASSIFICATION FOR NONHERMETIC SOLID STATE SURFACE-MOUNT DEVICES: This document identifies the classification level of nonhermetic solid-state surface mount devices (SMDs) that are sensitive to moisture-induced stress. It is used to determine what classification level should be used for initial reliability qualification. Once identified, the SMDs can be properly packaged, stored and handled to avoid subsequent thermal and mechanical damage during the assembly solder reflow attachment and/or repair operation. This revision now covers components to be processed at higher temperatures for lead-free assembly. A hard cop version is available for $20 each for IPC/JEDEC members and $40 for nonmembers. March 2008 September 2006 /JC-14.1 Subcommittee	
J-STD- 033B.1	JOINT IPC/JEDEC STANDARD FOR HANDLING, PACKING, SHIPPING AND USE OF MOISTURE/REFLOW SENSITIVE SURFACE-MOUNT DEVICES: NOTE - The Moisture Sensitive Caution Label (figure 3-4) has been editorially revised since originally posted 11/04/05, if you downloaded this file prior to 12/14/05 please download this revised version. This document provides SMD manufacturers and users with standardized methods for handling, packing, shipping and use of moisture/reflow sensitive SMDs. Now updated to support components that may need to be processed at higher temperatures, such as lead-free processes, these methods help avoid damage from moisture absorption and exposure to solder reflow temperatures that can result in yield and reliability degradation. IPC/JEDEC J-STD-033B helps achieve safe and damage-free reflow with the dry packing process and provides a minimum shelf life of 12 months from the seal date when using sealed dry bags. January 2007 (Available in German, www.ihs.com) October 2004 /JC-14.1 Subcommittee	
J-STD- 035	JOINT IPC/JEDEC STANDARD FOR ACOUSTIC MICROSCOPY FOR NONHERMETRIC ENCAPSULATED ELECTRONIC COMPONENTS: This test method defines the procedures for performing acoustic microscopy on non-hermetic encapsulated electronic components. This method provides users with an acoustic microscopy process reflow for	

	detecting defects non-destructively in plastic packages while achieving reproducibility. May 1999; Under Revision /JC-14.1 Subcommittee	$35.00
J-STD- 609	MARKING AND LABELING OF COMPONENTS, PCBs AND PCBAs TO IDENTIFY LEAD (Pb), Pb-FREE AND OTHER ATTRIBUTES This standard applies to boards/assemblies, to identify the type of Pb-free or Pb-containing solder used. This standard documents a method for identifying board surface finishes and Printed Circuit Board (PCB) resin systems. This standard applies to PCB base materials and for marking the type of conformal coating utilized on Printed Circuit Board Assemblies (PCBAs). Material and their containers previously marked or labeled according to JESD 97 or IPC-1066 need not be remarked unless agreed upon by the supplier and customer. May 2007 January 2007 /JC-14.4 Subcommittee	
NUMBER	**Joint Publication (JP)**	**PRICE**
JP 001.01	FOUNDRY PROCESS QUALIFICATION GUIDELINES (Wafer Fabrication Manufacturing Sites) This document provides a guideline for the minimum set of measurements to qualify a new semiconductor wafer process. It is written with particular reference to a generic silicon based CMOS logic technology. While it may be applicable to other technologies (e.g. analog CMOS, bipolar, BICMOS, GaAs, etc.), some sections apply specifically to CMOS. No effort was made in the present document to cover all the qualification requirements for specific other technologies, e.g. Cu/Low K interconnects or ultra thin gate oxide. This publication, is co-sponsored by JEDEC JC-14.2 and the FSA (Fabless Semiconductor Association). It originated at the FSA as a technology specific document, and has evolved into a generic set of qualification requirements. May 2004 /JC-14.2 Subcommittee	$67.00
JP 002	CURRENT TIN WHISKERS THEORY AND MITIGATION PRACTICES GUIDELINE This document will provide insight into the theory behind tin whisker formation as it is known today and, based on this knowledge, potential mitigation practices that may delay the onset of, or prevent tin whisker formation. The potential effectiveness of various mitigation practices will also be briefly discussed. References behind each of the theories and mitigation practices are provided. March 2006 June 2005 /JC-14.1 Subcommittee	$55.00
NUMBER	**Joint Standard (JS)**	**PRICE**
JS 9702	IPC/JEDEC-9702: MONOTONIC BEND CHARACTERIZATION OF BOARD-LEVEL INTERCONNECTS (IPC/JEDEC-9702) This publication specifies a common method of establishing the fracture resistance of board-level device interconnects to flexural loading during non-cyclic board assembly and test operations. Monotonic bend test qualification pass/fail requirements are typically specific to each device application and are outside the scope of this document. June 2004 September 2003 /JC-14.1 Subcommittee	
JS 9704	IPC/JEDEC-9704: Printed Wiring Board (PWB) Strain Gage Test Guideline This document describes specific guidelines for strain gage testing for Printed Wiring Board (PWB)assemblies. The suggested procedures enables board manufacturers to conduct required strain gage testing independently, and provides a quantitative method for measuring board flexure, and assessing risk levels. The topics covered include: Test setup and equipment; requirements; Strain measurement; Report format June 2005 January 2005 /JC-14.1 Subcommittee	
NUMBER	**JEDEC Publications (JEP)**	**PRICE**
JEP 64	SOLID STATE PRODUCTS REGISTRATION LIST(ORDER FROM TYPE ADMINISTRATION OFFICE): This publication includes addenda from 1976 to August 1986. The purpose of this list is to determine release numbers (file numbers) for JEDEC Type Designations. (See page 6 for more information.) September 1986; Reaffirmed November 2002 / Committee!33JCJEDC	$162.00
JEP 65	TEST PROCEDURES FOR VERIFICATION OF MAXIMUM RATINGS OF POWER TRANSISTORS: This publication describes tests which are intended to represent the verification of maximum ratings for data sheets; they are not tests for performance or quality level. This material is to be used in conjunction with formats developed for device registration and defining data. December 1967; Reaffirmed September 1981, April 1999 /JC-25 Committee	$52.00
JEP 69-B	PREFERRED LEAD CONFIGURATION FOR FIELD-EFFECT TRANSISTORS: This publication indicates preferred pinouts for FETs in various package designs. November 1973; Reaffirmed September 1981, April 1999 /JC-25 Committee	$38.00
JEP 70-B	QUALITY AND RELIABILITY STANDARDS AND PUBLICATIONS: Contains a listing and description of commonly used quality and reliability related standards and publications that are applicable to the semiconductor industry. It is intended to be a reference aid in finding available standards and obtaining a copy from the source of the standard. It is not intended to recommend or imply the applicability of any standard for a specific purpose. This revision has been updated to include recent releases as well as revisions, in addition, URLs have been added to the October 1999 /JC-14.4 Subcommittee	$57.00
JEP 74	STANDARD LIST OF VALUES TO BE USED IN POWER TRANSISTOR DEVICE REGISTRATION AND MINIMUM DIFFERENCES FOR DISCRETENESS OF REGISTRATIONS - SUPERSEDED BY EIA-419-A, February 1996. July 1969; Rescinded February 1996 /JC-25 Committee	$38.00

JEP 75	LETTER SYMBOLS USED WITH INFRARED DEVICES - INCORPORATED INTO JESD77-A. August 1984; Rescinded August 1984 /JC-10 Committee	
JEP 78	RELATIVE SPECTRAL RESPONSE CURVES FOR SEMICONDUCTOR INFRARED DETECTORS: The intent of this publication is to facilitate the specification of infrared detector diodes, particularly in conjunction with the preparation of data for JEDEC type registration. October 1969 /JEDEC Committee	$52.00
JEP 79	LIFE TEST METHODS FOR PHOTOCONDUCTIVE CELLS: This publication is for photoconductive cells sensitive primarily in the visible and near infrared region. September 1969	$52.00
JEP 84A	RECOMMENDED PRACTICE FOR MEASUREMENT OF TRANSISTOR LEAD TEMPERATURE: This publication covers recommended methods for measurement of transistor lead temperatures under various load conditions. The techniques described are sufficiently accurate for most applications. June 2004 September 2002 /JC-25 Committee	$41.00
JEP 86-A	RECOMMENDED PRACTICE FOR DUAL DIMENSIONING May 1976; Rescinded November 1999 /JC-11 Committee	
JEP 87	FORWARD TURN-ON TIME MEASUREMENT ON SEMI-DIODES - INCORPORATED INTO EIA-282-A. June 1992; Rescinded June 1985 /JC-22.2 Subcommittee	
JEP 88	THERMAL RESISTANCE AND THERMAL IMPEDANCE TEST METHODS FOR STUD AND BASE-MOUNTED RECTIFIER DIODES AND THYRISTORS January 1974; Rescinded June 1992 /JC-22.1 Subcommittee	
JEP 90	THERMAL RESISTANCE FOR TEST METHODS FOR SIGNAL DIODES - SUPERSEDED BY EIA-531, July 1986. See JESD531, April 2002. September 1983; Rescinded September 1986 /JC-22.4 Subcommittee	
JEP 93	MICROELECTRONIC DEVICE TYPE ASSIGNMENTS August 1975; Rescinded June 1992 June 1992 / Committee!33JCJEDC	
JEP 95	JEDEC REGISTERED AND STANDARD OUTLINES FOR SOLID STATE AND RELATED PRODUCTS: This publication is a compilation of some 1800 pages of outline drawings for microelectronic packages including transistors, diodes, DIPS, chip carriers and package interface BGA outlines in both inch and metric versions. January 2000 /JC-11 Committee	$425.00
JEP 95 AUS	ANNUAL UPDATING SERVICE: Subscription to this updating service is available from the JEDEC Office. New outlines are shipped to subscribers for insertion into the appropriate sections of Publication No. 95. JEP95 and Updating Service can be ordered through JEDEC at (703)907-7540 or ptanner@jedec.org. January 2000 /JC-11 Committee	$125.00
JEP 96	GUIDELINES FOR NONDESTRUCTIVE PULL TESTING OF WIRE BONDS ON HYBRID DEVICES March 1977; Rescinded April 2000 /JC-13.5 Subcommittee	
JEP 99	GLOSSARY OF MICROELECTRONIC TERMS, DEFINITIONS, AND SYMBOLS: ELEVATED TO JESD99, June 1985. July 1977; Rescinded June 1985 /JC-10 Committee	
JEP 100	TERMS, DEFINTIONS, AND LETTER SYMBOLS FOR MICROCOMPUTERS AND MEMORY INTEGRATED CIRCUITS: ELEVATED TO JESD100, August 1993. September 1979; Rescinded October 1983 /JC-10 Committee	
JEP 101-C	JEDEC REQUIREMENTS FOR CLASS B MICROCIRCUITS: RESCINDED, May 2006 November 1995; Rescinded May 2006 /JC-13.2 Subcommittee	$38.00
JEP 102	STANDARD FOR 64K x 1 DYNAMIC RAM - SUPERSEDED BY JESD21-C. September 1978; Rescinded April 1985 April 1985 /JC-42 Committee	
JEP 103A	SUGGESTED PRODUCT-DOCUMENTATION, CLASSIFICATIONS, AND DISCLAIMERS In order to improve understanding between manufacturers and users, a consistent set of product-documentation classifications associated with the stages of product development. July 1996; Reaffirmed November 1999, May 2003 /JC-10 Committee	$38.00
JEP 104C.01	REFERENCE GUIDE TO LETTER SYMBOLS FOR SEMICONDUCTOR DEVICES: This publication provides a quick reference to the letter symbols and corresponding terms that are defined in JESD77-B, Terms, Definitions, and Letter Symbols for Discrete Semiconductor and Optoelectronic Devices; JESD99-A, Terms, Definitions, and Letter Symbols for Microelectronic Devices, and JESD100-B, Terms, Definitions, and Letter Symbols for Microcomputers,	

Microprocessors, and Memory Integrated Circuits. It is intended to simplify interpretation of data sheets and specifications and to promote the uniform use of these symbols. The symbols relate to ratings and characteristics found in data sheets and other specifications. Some abbreviations used in lieu of symbols are also included. The newly added Annex B is provided as an aid to determining what symbol should be used and is organized by term, whereas the main body of the publication is organized by symbol or abbreviation as in previous versions. This version contains minor revisions.

May 2003 /JC-10 Committee $91.00

JEP 105

JEDEC GUIDELINE FOR THE CHARACTERIZATION OF HYBRID POLYMERIC MATERIALS - SUPERSEDED BY JESD72, June 2001

April 1983; Rescinded June 2001 /JC-13.5 Subcommittee

JEP 106Z

STANDARD MANUFACTURERS IDENTIFICATION CODE: The manufacturers identification code is defined by one or more 8 bit fields, each consisting of 7 data bits plus 1 odd parity bit. The manufacturers identification code is assigned, maintained and updated by the JEDEC Office. The intent of this identification code is that it may be used whenever a digital field is required, e.g., hardware, software, documentation, etc. To make a request for an ID Code please go to http://www.jedec.org/Home/MIDCODE_request.cfm

January 2009 NOTE: JEP106U was in error starting with bank two an additional continuation code was added. This has been corrected, JEP106U should be discarded. /JC-42.3 Subcommittee $62.00

JEP 107

TEST METHOD FOR QUALIFICATION AND ACCEPTANCE OF PARTICLE GETTERS FOR USE IN HYBRID MICROELECTRONIC APPLICATIONS - SUPERSEDED BY JESD72, June 2001

April 1985; Rescinded June 2001 /JC-13.5 Subcommittee

JEP 108-B

DISTRIBUTOR REQUIREMENTS FOR HANDLING ELECTROSTATIC -DISCHARGE SENSITIVE (ESDS) DEVICES: SUPERSEDED BY JESD42, March 1994.

April 1991; Superseded /JC-14.1 Subcommittee

JEP 109-C

GENERAL REQUIREMENTS FOR DISTRIBUTORS OF MILITARY SEMICONDUCTOR DEVICES: Superseded by JESD31-A, June 2001.

March 1995; Rescinded November 2001 /JC-13 Committee

JEP 110

GUIDELINES FOR THE MEASUREMENT OF THERMAL RESISTANCE OF GaAs FETS: This publication is intended for power GaAs FET applications requiring high reliability. An accurate measurement of thermal resistance is extremely important to provide the user with knowledge of the FETs operating temperature so that more accurate life estimates can be made. FET failure mechanisms and failure rates have, in general, an exponential dependence on temperature (which is why temperature-accelerated testing is successful). Because of the exponential relationship of failure rate with temperature, the thermal resistance should be referenced to the hottest part of the FET.

July 1988 /JC-14.7 Subcommittee $43.00

JEP 111

TEST PROCEDURES FOR CUSTOM MONOLITHIC MICROCIRCUITS - SUPERSEDED BY MIL-PRF-38535C.

July 1986; Rescinded June 1996 June 1996 /JC-13.2 Subcommittee

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JEP 112

TEST METHOD FOR QUALIFICATION AND ACCEPTANCE OF CIRCUIT SUPPORT FILMS FOR USE IN MICROELECTRONIC APPLICATIONS - SUPERSEDED BY JESD72, June 2001

June 1987; Rescinded June 2001 /JC-13 Committee $52.00

JEP 113-B

SYMBOL AND LABELS FOR MOISTURE-SENSITIVE DEVICES: Certain PSMC (Plastic Surface-mount Components) are subject to permanent damage due to moisture-induced failures encountered during high-temperature surface-mount processing unless appropriate precautions are observed. The purpose of this publication is to provide a distinctive symbol and labels to be used to identify those devices that require special packing and handling precautions.

May 1999 /JC-14.1 Subcommittee $45.00

JEP 114.01

GUIDELINES FOR PARTICLE IMPACT NOISE DETECTION (PIND) TESTING, OPERATOR TRAINING, AND CERTIFICATION: This publication was developed to help the user of this test methodology avoid common interference Æs to successful application. The guide contains sections on typical specification requirements, sources of particles, PIND test systems, calibration, maintenance, test interference's, operator training, particle recovery and failure analysis. Application of the information contained in the guide will improve the quality and affectivity for any PIND testing operation.

October 2007 August 2007 /JC-13.5 Subcommittee $72.00

JEP 115

POWER MOSFET ELECTRICAL DOSE RATE TEST METHOD: The purpose of this Test Method is to establish electrical criteria for comparing and specifying power MOSFET performance under high dose rate radiation.

August 1989; Reaffirmed April 1999 /JC-25 Committee $41.00

JEP 116

CMOS SEMICUSTOM DESIGN GUIDELINES: The design of ASIC circuits is becoming a significant part of system or product design, yet many problems continue to exist in current design practice. The guidelines in this document provide an explanation of common ASIC design problems and concerns and where possible offer solutions.

November 1991 / Committee!33JC44 $109.00

JEP 117

GUIDELINES FOR USER NOTIFICATION OF PRODUCT/PROCESS CHANGES BY SEMICONDUCTOR SUPPLIERS - SUPERSEDED BY JESD46, August 1997.

April 1994; Rescinded July 1994 /JC-14.4 Subcommittee

JEP 118

GUIDELINES FOR GaAs MMIC AND FET LIFE TESTING: These guidelines apply to monolithic microwave GaAs integrated circuits (MMICs) and their individual component building blocks, such as GaAs field effect transistors (FETs), resistors, and capacitors. The purpose of this document is to define a standard approach for evaluating the expected live of GaAs MMICs so that results from different life tests can be compared and so that wording of this document that the MMIC contains at least one FET, but the use of this document has no such limitation.

January 1993 /JC-14.7 Subcommittee $48.00

JEP 119A

A PROCEDURE FOR EXECUTING SWEAT: This document describes an algorithm for performing the Standard Wafer Level Electromigration Accelerated Test (SWEAT) method with computer controlled instrumentation. The algorithm requires a separate iterative technique (not provided) to calculate the force current for a given target time to failure. This document does not specify what test structure to use with this procedure. However, users of this algorithm report its effectiveness on both straight-lines and via-terminated test structures. Some test-structures design features are provided in JESD87 and in ASTM 1259M - 96.

August 2003 /JC-14.2 Subcommittee $57.00

JEP 120-A

INDEX OF TERMS DEFINED IN JEDEC PUBLICATIONS: This publication provides an index to terms that are defined in certain JEDEC publications. It is intended to promote the uniform use of these terms and their definitions while reducing the proliferation of new definitions for old terms.

May 2000 /JC-10 Committee $109.00

JEP 121A

REQUIREMENTS FOR MICROELECTRONIC SCREENING AND TEST OPTIMIZATION: The purpose of this document provides the basis for the optimization of 100% screening/stress operations and sample inspection test activities. This document is designed to assist the manufacturer in optimizing the test flow while maintaining and/or improving assurance of providing high quality and reliable product in an efficient manner. This will allow for optimization of testing that is not adding value, hence, reducing cycle time and costs.

October 2006 May 2006 /JC-13.2 Subcommittee $59.00

JEP 122E

FAILURE MECHANISMS AND MODELS FOR SEMICONDUCTOR DEVICES: This publication provides a list of failure mechanisms and their associated activation energies or acceleration factors that may be used in making system failure rate estimations when the only available data is based on tests performed at accelerated stress test conditions. The method to be used is the Sum of the Failure Rates method.

March 2009 January 2009 /JC-14.1 Subcommittee $136.00

JEP 123

GUIDELINE FOR MEASUREMENT OF ELECTRONIC PACKAGE INDUCTANCE AND CAPACITANCE MODEL PARAMETERS: The need for this guideline arose from widespread lack of consistency in characterizing electrical parameters of electronic packages, which existed in the industry until the early 1990s. Then, the JEDEC Committee JC-15 provided the forum where various methods were discussed and commonality in approach emerged. The result is that today we have relatively consistent results in measuring and reporting electrical package parameters, as well as specialized tools (e.g., the IPA-510, the interconnect parameter analyzer) which were developed to support the methodology.

October 1995 /JC-15.2 Subcommittee $49.00

JEP 124

GUIDELINES FOR THE PACKING, HANDLING, AND REPACKING OF MOISTURE-SENSITIVE COMPONENTS - SUPERSEDED BY J-STD-033, May 1999.

December 1995; Rescinded November 1999 November 1999 /JC-14.4 Subcommittee

JEP 126

GUIDELINE FOR DEVELOPING AND DOCUMENTING PACKAGE ELECTRICAL MODELS DERIVED FROM COMPUTATIONAL ANALYSIS: This publication provides a guideline to suppliers of IC components with a template for documenting the numerical simulation assumptions. In addition this guideline also suggests a model environment to reference when comparing various packages or component suppliers. This publication should improve the communication between the package model suppliers. This publication should improve the communication between the package model supplier and the end user.

May 1996 /JC-15.2 Subcommittee $38.00

JEP 128

GUIDE FOR STANDARD PROBE PAD SIZES AND LAYOUTS FOR WAFER LEVEL ELECTRICAL TESTING: This guide was developed to expedite inter-laboratory experiments used to evaluate or develop standard test methods that involve test-structure measurements or tests. It also facilitates, generally, any electrical tests that require wafer-probe card to make electrical contact to test structures. Widespread use of this guide will afford the efficient and cost-effective use of water-probe test stations because of the need for fewer probe cards and probe-card changes to accommodate the various test structures that may need to be tested.

November 1996 /JC-14.2 Subcommittee $40.00

JEP 129

THERMAL TEST CHIP GUIDELINE (WIRE BOND TYPE CHIP)- SUPERSEDED BY JESD51-4, September 1997.

February 1997; Elevated September 1997 /JC-15.1 Subcommittee

JEP 130A

GUIDELINES FOR PACKING AND LABELING OF INTEGRATED CIRCUITS IN UNIT CONTAINER PACKING: This document establishes guidelines for integrated circuit unit container and the next level (intermediate) container packing and labeling. The guidelines include tube/rail standardization, intermediate packing, date codes, tube labeling, intermediate container and shipping labels, and standardize tube quantities. Future revisions of this document will also include tray and reel guidelines. The objective of this publication is to promote the standardization of practices between manufacturers and distributors resulting in improved efficiency, profitability, and product quality.

February 2006 January 2005 /JC-14.4 Subcommittee $43.00

JEP 131A

PROCESS FAILURE MODE AND EFFECTS ANALYSIS (FMEA): This publication was created in response to the need for a straight forward FMEA procedure. The objective is to provide a guideline for the application of FMEA techniques to improve quality, reliability and/or consistency of electronic components and subassemblies by continually evaluating processes/products against potential failure modes.

May 2005 October 2004 /JC-15.1 Subcommittee $55.00

JEP 132

PROCESS CHARACTERIZATION GUIDELINE: This guideline provides a methodology to characterize a new or existing process and is applicable to any manufacturing or service process. It describes when to use specific tools such as failure mode effects analysis (FEMA), design or experiments (DOE), measurement system evaluation (MSE), capability analysis (CpK), statistical process control (SPC), and problem solving tools. It also provides a brief description of each tool. In December 2004 the document was renumbered to conform with JM7, JEDEC Style Manual.

July 1998; Reaffirmed September 2003, January 2007 /JC-13 Committee $59.00

JEP 133B

GUIDE FOR THE PRODUCTION AND ACQUISITION OF RADIATION-HARDNESS ASSURED MULTICHIP MODULES AND HYBRID MICROCIRCUITS: A revised and expanded publication for suppliers and users of radiation hardness assured (RHA) multichip modules (MCMs) and hybrid microcircuits, is now available. Revision A of JEP133 includes modifications to the introduction, clarification of a definition and clarification of several technical issues within the document. In addition, the Bibliography section was updated to include added references. The document provides guidance as to how to achieve, maintain and ensure required levels of radiation-hardness given the fact that the constituent dice can have different levels of hardness assurance. It also describes how to deal with the various radiation hardness situations that an MCM/Hybrid developer, procuring activity or user will encounter. The guide is intended to supplement three relevant performance specifications: MIL-PRF-38534, MIL-PRF-38535 and MIL-PRF-19500.

March 2005 September 2003 /JC-13.5 Subcommittee $59.00

JEP 134

GUIDELINES FOR PREPARING CUSTOMER-SUPPLIED BACKGROUND INFORMATION RELATING TO A SEMICONDUCTOR-DEVICE FAILURE ANALYSIS: The purpose of this Guideline is to provide a vehicle for acquiring and transmitting the necessary information in a concise, organized, and consistent format. Included in the Guideline is a sample form that facilitates transferring the maximum amount of background data to the failure analyst in a readily interpretable format. Immediate availability of this key information assists that analyst in completing a timely and accurate failure analysis.

September 1998 /JC-14.6 Subcommittee $45.00

JEP 136

SIGNATURE ANALYSIS: Signature Analysis is a method to reduce the number of comprehensive physical failure analyses by the application of statistical inference techniques. The purpose of this document is to promote a common definition of Signature Analysis by inference, using the same statistical techniques, and to recognize that it is formal means of doing failure analysis.

July 1999 /JC-14.6 Subcommittee $47.00

JEP 137B

COMMON FLASH INTERFACE (CFI) IDENTIFICATION CODES: This publication is a companion document to the Common Flash Interface (CFI) standard, JESD68, which outlines the device and host system software interrogation handshake. JEP137 documents ID Code assignments for: 1)) the Algorithm-specific Command Set and Control Interfaces and 2) the Device Interfaces. It is published as needed when additions are made to either of these lists of codes. To make a request for an ID Code please contact the JEDEC Office at (703)907-7558.

May 2004 /JC-42.4 Subcommittee $41.00

JEP 138

USER GUIDELINES FOR IR THERMAL IMAGING DETERMINATION OF DIE TEMPERATURE: The purpose of these user guidelines is to provide background and an example for the use of an infrared (IR) microscope to determine die temperature of electronic devices for calculations such as thermal resistance.

September 1999 /JC-25 Committee $41.00

JEP 139

GUIDELINE FOR CONSTANT TEMPERATURE AGING TO CHARACTERIZE ALUMINUM INTERCONNECT METALLIZATIONS FOR STRESS-INDUCED VOIDING: This document describes a constant temperature (isothermal) aging method for testing aluminum (Al) metallization test structures on microelectronics wafers for susceptibility to stress-induced voiding. This method is valid for metallization/dielectric systems in which the dielectric is deposited onto the metallization at a temperature considerably above the intended use temperature, and above or equal to the deposition temperature of the metal. Although this is a wafer test, it is not a fast (less than 5 minutes per probe) test. It is intended to be used for lifetime prediction and failure analysis, not for production Go-NoGo lot checking.

December 2000 /JC-14.2 Subcommittee $47.00

JEP 140

BEADED THERMOCOUPLE TEMPERATURE MEASUREMENT OF SEMICONDUCTOR PACKAGES: The beaded thermocouple temperature measurement guideline provides a procedure to accurately and consistently measure the temperature of semiconductor packages during exposure to thermal excursions. The guideline applications can include, but not limited to, temperature profile measurement in reliability test chambers and solder reflow operations that are associated with component assembly to printed wiring boards.

June 2002; Reaffirmed June 2006 /JC-14.1 Subcommittee $43.00

JEP 142

GUIDELINE FOR OBTAINING AND ACCEPTING MATERIAL FOR USE IN HYBRID / MCM PRODUCTS: This document provides guidance regarding design considerations, material assessment techniques, and recommendations for material acceptance prior to use in Hybrid / MCM Products. As part of the risk assessment process, both technical requirements and cost should be carefully considered with regard to testing / evaluating the elements of a hybrid

requirements and cost should be carefully considered with regard to testing / evaluating the elements of a hybrid microcircuit or Multi-chip Module (MCM) prior to material release for assembly. The intent of this document is to highlight various options that are available to the Hybrid / MCM manufacturer and provide associated guidance, not to impose a specific set of tests.

May 2002 /JC-13.5 Subcommittee $55.00

JEP 143B.01

SOLID STATE RELIABILITY ASSESSMENT QUALIFICATION METHODOLOGIES: The purpose of this publication is to provide an overview of some of the most commonly used systems and test methods historically performed by manufacturers to assess and qualify the reliability of solid state products. The appropriate references to existing and proposed JEDEC (or EIA) standards and publications are cited. This document is also intended to provide an educational background and overview of some of the technical and economic factors associated with assessing and qualifying microcircuit reliability.

June 2008 September 2007 /JC-14.3 Subcommittee $70.00

JEP 144

GUIDELINE FOR RESIDUAL GAS ANALYSIS (RGA) FOR MICROELECTRONIC PACKAGES The intent of this document is to give guidance on the Residual Gas Analysis (RGA) process and surrounding issues. The guideline describes how to select a suitable test lab and includes RGA history, measurement methodology, and issues that arise with the test. Interpreting the lab results along with common failure mechanisms are discussed at length along with process controls and alternative test techniques for measuring the moisture content within packages.

July 2002 /JC-13 Committee $57.00

JEP 145

GUIDELINE FOR ASSESSING THE CURRENT-CARRYING CAPABILITY OF THE LEADS IN A POWER PACKAGE SYSTEM: This publication is intended as a guideline to establish procedures, consideration and common practices that will allow a manufacturer, an application entity, a system designer and other interested parties to define current capability limitations in the leads of components and power systems with semiconductor components. This is a guideline, not a standardized method, it was developed over several years to clarify questions that had been posed to committee members in their respective engineering functions.

February 2003 /JC-25 Committee $41.00

JEP 146A

GUIDELINES FOR SUPPLIER PERFORMANCE RATING: The intent of this document is to establish guidelines and provide examples by which customers can measure their suppliers based on mutually agreed upon objective criteria. These results can then be used to improve communications between customers and suppliers.

January 2009 January 2008 /JC-14.4 Subcommittee $58.00

JEP 147

PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER (VNA): This procedure describes a recommended way to measure pin capacitance of devices with SSTL (Stub Series Terminated Logic) interface pins by use of a Vector Network Analyzer. One purpose of this standard procedure is to reduce the lengthy and often inaccurate footnote - usually found around the specification of pin parasitics - to a simple reference to this document. In special cases modifying statements may adjust this procedure to the special needs of certain component.

October 2003 December 2002 / Committee!33JC162 $41.00

JEP 148A

RELIABILITY QUALIFICATION OF SEMICONDUCTOR DEVICES BASED ON PHYSICS OF FAILURE RISK AND OPPORTUNITY ASSESSMENT A concept is outlined, which proactively integrates qualification into the development process and provides a systematic procedure as support tool to development and gives early focus on required activities. It converts requirements for a product into measures of development and qualification in combination with a risk and opportunity assessment step and accompanies the development process as guiding and recording tool for advanced quality planning and confirmation. The collected data enlarge the knowledge database for DFR / BIR (design for reliability / building-in reliability) to be used for future projects. The procedure challenges and promotes teamwork of all involved disciplines. Based on the Physics-of-Failure (PoF) concept the reliability qualification methodology is re-arranged with regard to the relationships between design, technology, manufacturing and the different product life phases at use conditions. It makes use of the Physics-of-Failure concept by considering the potential individual failure mechanisms and relates most of the reliability aspects to the technology rather than to the individual product design. Evaluation of complex products using common reliability models and definition of sample sizes with respect to systematic inherent product properties and fractions of defects are discussed.

December 2008 January 2008 /JC-14.3 Subcommittee $72.00

JEP 149

APPLICATION THERMAL DERATING METHODOLOGIES: This publication applies to the application of integrated circuits and their associated packages in end use designs. It summarizes the methodology of thermal derating and the suitability of such methodologies.

November 2004 June 2004 /JC-14.3 Subcommittee $47.00

JEP 150

STRESS-TEST-DRIVEN QUALIFICATION OF AND FAILURE MECHANISMS ASSOCIATED WITH ASSEMBLED SOLID STATE SURFACE-MOUNT COMPONENTS This publication contains a set of frequently recommended and accepted JEDEC reliability stress tests. These tests are used for qualifying new and modified technology/ process/ product families, as well as individual solid state surface-mount products, in particular leadless chip carriers, ball grid array (BGA) packages, direct chip attach die and packages with exposed pads that are attached to the PWB for thermal considerations. Assembly level testing may not be a prerequisite for device qualification; however, if the effect of assembly conditions on the component is not known, there could be reliability concerns for that component that are not evident in component level testing. As such, it is recommended that assembly level testing be performed to determine if there are any adverse effects on that component due to its assembly to a PWB.

May 2005 October 2004 /JC-14.3 Subcommittee $48.00

JEP 152

DDR2 DIMM CLOCK SKEW MEASUREMENT PROCEDURE USING A CLOCK REFERENCE BOARD This document is the work

	product of the JC-45.1 □DDR2 DIMM Clock Skew Measurement□ task group.The purpose of this document is to define procedures to measure clock parameters on registered DIMMs using the DDR2 Clock Reference Board. It is NOT the intent of this document to set specification values or validation requirements. May 2007 February 2004 /JC-45.1 Subcommittee	$55.00
JEP 153	CHARACTERIZATION AND MONITORING OF THERMAL STRESS TEST OVEN TEMPURATURES This document provides an industry standard method for characterization and monitoring thermal stress test oven temperatures. The procedures described in this document should be used to insure thermal stress test conditions are being achieved and maintained during various test procedures. January 2008 June 2007 /JC-14.1 Subcommittee	$55.00
JEP 154	GUIDELINE FOR CHARACTERIZING SOLDER BUMP ELECTROMIGRATION UNDER CONSTANT CURRENT AND TEMPERATURE STRESS This document describes a method to test the electromigration (EM) susceptibility of solder bumps, including other types of bumps, such as solder capped copper pillars, used in flip-chip packages. The method is valid for Sn/Pb eutectic, high Pb, and Pb-free solder bumps. The document discusses the advantages and concerns associated with EM testing, as well as options for data analysis. January 2008 September 2007 /JC-14.1 Subcommittee	$70.00
JEP 155	RECOMMENDED ESD TARGET LEVELS FOR HBM/MM QUALIFICATION This document was written with the intent to provide information for quality organizations in both semiconductor companies and their customers to assess and make decisions on safe ESD level requirements. It will be shown through this document why realistic modifying of the ESD target levels for component level ESD is not only essential but is also urgent. The document is organized in different sections to give as many technical details as possible to support the purpose given in the abstract. August 2008 September 2007 /JC-14 Committee	$84.00
JEP 156	CHIP-PACKAGE INTERACTION UNDERSTANDING, IDENTIFICATION AND EVALUATION: This publication references a set of frequently recommended and accepted JEDEC reliability stress tests. These tests are used for qualifying new and modified technology/ process/ product families, as well as individual solid state surface-mount products. March 2009 September 2008 /JC-14.3 Subcommittee	$65.00
JEP 179	DDR2 SPD INTERPRETATION OF TEMPERATURE RANGE AND (SELF-) REFRESH OPERATION The purpose of this document is to explain the meaning of SPD setting (JESD21 SPD section) for DDR2 SDRAM (JESD79-2) in normal and extended temperature operationy67. June 2006 March 2005 /JC-42.3 Subcommittee	$40.00
NUMBER	**EIA Standards (EIA)**	**PRICE**
EIA 236-C	COLOR CODING OF DISCRETE SEMICONDUCTOR DEVICES: This standard details the methods to be followed if color coding is used to identify JEDEC-assigned type numbers or for cathode identification of discrete semiconductor devices. ANSI/EIA-236-C-1986. March 1986; Reaffirmed November 1999 /JC-10 Committee	$38.00
EIA 282-A	STANDARD FOR SILICON RECTIFIER DIODES: SEE JESD282-B ANSI/EIA-282-A-1989 February 1990; Elevated Became JESD282-B after revision April 2000 /JC-22.2 Subcommittee	
EIA 283	TEST METHOD FOR TRANSISTOR NOISE FIGURE MEASUREMENTS AT MEDIUM FREQUENCIES - SUPERSEDED BY EIA-311-A. November 1963; Rescinded November 1981 November 1981 /JC-25 Committee	
EIA 284-A	TEST METHODS FOR THE COLLECTOR-BASE TIME CONSTANT AND FOR THE RESISTIVE PART OF THE COMMON-EMITTER INPUT IMPEDANCE: SEE JESD284A. EIA-284-A became JESD284A after reaffirmation in October 2002. November 1963; Reaffirmed /JC-25 Committee	
EIA 286-A	STANDARD FOR MEASURING FORWARD SWITCHING CHARACTERISTICS OF SEMICONDUCTOR DIODES: SEE JESD286-B. ANSI/EIA-286-A-1991. February 1991; Elevated Became JESD286-B after revision February 2000 /JC-22.4 Subcommittee	
EIA 308-A	PREPARATION OF OUTLINE DRAWINGS OF SOLID-STATE PRODUCTS FOR JEDEC TYPE REGISTRATION: This standard is intended to serve as a guide to manufacturers of solid state products for the preparation of outline drawings of solid state product packages for JEDEC type registration. August 1981 /JC-11 Committee	$38.00
EIA 318-B	MEASUREMENT OF REVERSE RECOVERY TIME FOR SEMICONDUCTOR SIGNAL DIODES: This standard describes the measurement of signal diodes (I_F <=500mA dc) reverse recovery times of less than 300 ns duration. It may, however, also be used for the measurement of longer recovery times. This standard is also intended to establish a method which to characterize the test fixture used for this measurement. July 1996; Reaffirmed April 1999 /JC-22.4 Subcommittee	$47.00
EIA 321-C	NUMBERING OF LIKE-NAMED TERMINAL FUNCTIONS IN SEMICONDUCTOR DEVICES AND DESIGNATION OF UNITS IN MULTIPLE-UNIT SEMICONDUCTOR DEVICES: This standard gives the system for numbering like-named electrodes or terminal functions in semiconductor devices and for assigning numerical designations to units of multiple-unit semiconductor devices. It applies to both integrated circuits and discrete devices. ANSI/EIA-321-C-1987 February 1987; Reaffirmed November 1995 November 1995 /JC-10 Committee	$41.00

February 1987; Reaffirmed November 1995 November 1995 /JC-10 Committee $41.00

EIA 323

AIR-CONVECTION-COOLED, LIFE TEST ENVIRONMENT FOR LEAD-MOUNTED SEMICONDUCTOR DEVICES: This standard is applicable to life testing of lead-mounted semiconductor devices intended for applications in a natural air-cooled environment where most of the power dissipation is obtained by convection and radiation losses from the body to the device.

March 1966; Reaffirmed February 1972, November 2002 November 2002 /JC-22.1 Subcommittee $40.00

EIA 365

PERFORMANCE TEST PROCEDURE FOR SOLAR CELLS AND CALIBRATION PROCEDURE FOR SOLAR CELL STANDARDS FOR SPACE VEHICLE SERVICE: The purpose of this standard is to classify the output of solar cells for space vehicle service in accordance with requirements of EIA Format JS4-RDF4.

November 1969; Reaffirmed February 1984 February 1984 / Committee!33JC231 $47.00

EIA 397

RECOMMENDED STANDARD FOR THYRISTORS: One section of this standard presents a thorough explanation of thyristor principals, defining thedifferent classes of these devices, their Physical structure and detailing the numerous test methods and ratings required in their application to electronic and power circuitry. Another section presents a universally accepted listing of letter symbols. Considerable effort is devoted to the use of JEDEC Type Registration System as related to thyristors. This will permit the device manufacturer to employ a uniform procedure in the development of maximum rating and presentation of performance data.

June 1972 /JC-22.1 Subcommittee $177.00

EIA 397-1

ADDENDUM No. 1 TO EIA-397: A compilation of 12 new or revised thyristor test methods which have been adopted since the original standard was issued in 1972.

July 1980 /JC-22.1 Subcommittee $83.00

EIA 428-A

TYPE DESIGNATION SYSTEM FOR MICROELECTRONIC DEVICES

October 1988; Rescinded September 1993 September 1993 /JC-10 Committee

EIA 471

SYMBOL AND LABEL FOR ELECTROSTATIC SENSITIVE DEVICES: This standard will be useful to anyone engaged in handling semiconductor devices and integrated circuits that are subject to permanent damage due to electrostatic potentials. The standard establishes a symbol and label that will gain the attention of those persons who might inflict electrostatic damage to the device. The label which is placed on the lowest practical level of packaging contains the words 'ATTENTION - OBSERVE PRECAUTIONS FOR HANDLING ELECTROSTATIC SENSITIVE DEVICES'. The symbol contained in this label, which may be used on the device itself, shows a hand in a triangle with a bar through it.

February 1980; Reaffirmed October 1988, September 1996, November 1996 /JC-10 Committee $38.00

EIA 554A

Method Selection for Assessment of Nonconforming Levels in Parts Per Million (PPM) Not all sections of EIA-554 are appropriate for use by device manufacturers therefore JEDEC wishes to continue using JESD16A. To obtain a copy of EIA-554 please contact GEIA at http://www.geia.org/

July 1996; Reaffirmed September 5, 2002. December 2008, removed from JEDEC. January 2006 /JC-13.2 Subcommittee $IHS

EIA 557B

STATISTICAL PROCESS CONTROL SYSTEMS: SPC embraces a management philosophy of continuous process improvement that has a primary focus on prevention of defects. After a process has been characterized using statistical techniques (i.e., design experiments (DOE), capability studies, etc.), SPC is a tool that can be applied to control and optimize the process and reduce variability. An acceptable approach toward an SPC system involves the use of 'end-of-process' data to control the process through the application of SPC techniques. However, the intent of this standard is to emphasize the use of in-process data in order to better control and forecast system quality. This proactive use of SPC in conjunction with other techniques and the appropriate responsiveness to out-of-control situations serves to make SPC techniques critical in continuous process improvement and achieving excellence.

February 2006 /JC-13.5 Subcommittee $IHS

EIA 599-A

NATIONAL ELECTRONIC PROCESS CERTIFICATION STANDARD; GOVERNMENT CONTRACTORS: Due to notification from the JC-14.4 subcommittee that the material contained in EIA599 has been replaced by the ISO 9000 series, the JEDEC Board of Directors, at its August 2003 meeting, approved to remove this standard from the JEDEC Free Download Area.

June 1998; Rescinded August 25, 2003 August 2003 /JC-14.4 Subcommittee

EIA 623

PROCUREMENT QUALITY OF SOLID STATE COMPONENTS BY GOVERNMENT CONTRACTORS: RESCINDED, May 2006

July 1994; Rescinded May 2006 January 2004 /JC-13 Committee $40.00

EIA 625

REQUIREMENTS FOR HANDLING ELECTROSTATIC-DISCHARGE-SENSITIVE (ESDS) DEVICES (SUPERSEDES JEP108-B): SEE JESD625-A.

November 1994; Elevated Became JESD625A after Revision December 1999 /JC-13 Committee

EIA 659

FAILURE-MECHANISM-DRIVEN RELIABILITY MONITORING (SUPERSEDES JESD29-A): SEE JESD659, latest edition.

July 1996; Elevated Became JESD659A after Revision September 1999 /JC-14.3 Subcommittee

EIA 670

QUALITY SYSTEM ASSESSMENT (SUPERSEDES JESD39-A): This standard is used by the electronic industry for preparation of audit checklists for assessing compliance of quality systems to the requirements of ANSI/ASQC Q9001 (ISO9001), ANSI/ASQC Q9002 (ISO9002), ANSI/ASQC Q9003 (ISO9003), and ANSI/EIA599, National

Electronic Process Certification Standard. It also provides a tool for quality system evaluation in accordance with the guidelines of ANSI/ASQC Q9004 (ISO9004) and the Malcolm Baldrige National Quality Award Criteria.

June 1997 /JC-14.4 Subcommittee $63.00

EIA 671

COMPONENT PROBLEM ANALYSIS AND CORRECTIVE ACTION REQUIREMENTS: SEE JESD671-A.

November 1996; Elevated Became JESD671A after revision December 1999 /JC-14.4 Subcommittee

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JESD 302

RANGES AND CONDITIONS FOR SPECIFYING BETA FOR LOW POWER, AUDIO FREQUENCY TRANSISTORS FOR ENTERTAINMENT SERVICE: This standard establishes the preferred rating ranges and conditions for specifying beta for low power, audio frequency transistors intended for entertainment service. Formerly known as RS-302 and EIA-302.

January 1965; Reaffirmed April 1981, April 1999, March 2009 /JC-25 Committee $37.00

JESD 306

MEASUREMENT OF SMALL SIGNAL HF, VHF, AND UHF POWER GAIN OF TRANSISTORS: This standard provides a method of measurement for small-signal HF, VHF, and UHF power gain of low power transistors. Formerly known as RS-306 and/or EIA-306.

May 1965; Reaffirmed April 1981, April 1999, March 2009 /JC-25 Committee $38.00

JESD 311-A

MEASUREMENT OF TRANSISTOR NOISE FIGURE AT MF, HF, AND VHF: This standard describes a test method for measurement of transistor noise figure and effective input noise temperature at MF, HF, and VHF. This standard also adds the necessary information to make 'effective input noise temperature measurements'. This method is a revision of EIA-311 and incorporates material previously found in EIA-283. Formerly known as RS-311A and/or EIA-311-A.

November 1981; Reaffirmed April 1999, March 2009 April 1999 /JC-25 Committee $48.00

JESD 340

STANDARD FOR THE MEASUREMENT OF CRE: This standard offers an easily measured parameter which is one of the significant characteristics in determining the stability of a transistor intended for small-signal operation. The measurement technique allows rapid testing. Its correlation to AC stability will help to establish the interchangeability of a device. Formerly known as RS-340 and/or EIA-340.

November 1967; Reaffirmed April 1981, April 1999, March 2009 /JC-25 Committee $43.00

JESD 353

THE MEASUREMENT OF TRANSISTOR NOISE FIGURE AT FREQUENCIES UP TO 20 kHz BY SINUSOIDAL SIGNAL-GENERATOR METHOD: This noise measurement method applies to transistors whose noise has a Gaussian power distribution, to transistors whose noise has a flat (white) power distribution, and to transistors whose noise has a l/f (power inversely proportional to frequency) power distribution. Formerly known as RS-353 and/or EIA-353

April 1968; Reaffirmed April 1981, April 1999, March 2009 /JC-25 Committee $40.00

JESD 354

THE MEASUREMENT OF TRANSISTOR EQUIVALENT NOISE VOLTAGE AND EQUIVALENT NOISE CURRENT AT FREQUENCIES OF UP TO 20 kHz: This standard provides a method for determining values, for device registration purposes, for transistor equivalent noise voltage and equivalent noise current at frequencies up to 20 kHz. This method is applicable to transistors whose noise has a Gaussian, flat (white) or I/f power distribution. Formerly known as RS-354 and/or EIA-354

April 1968; Reaffirmed April 1981, April 1999, March 2009 /JC-25 Committee $40.00

JESD 370B

DESIGNATION SYSTEM FOR SEMICONDUCTOR DEVICES: This standard includes several new items and has been completely rewritten from the original EIA-370. The first is a new letter symbol C so that a JEDEC type designation may now be 2C1234, to indicate that a chip is being designated that if it were properly mounted on the package registered for the 2N1234, it would display characteristics similar to those of the 2N1234. The second major addition is the method for assigning the first numeric symbol for type designations of optoelectronic devices. ANSI/EIA-370-B-1992.

February 1982; Reaffirmed November 1995, November 1999, May 2003 /JC-10 Committee $43.00

JESD 371

THE MEASUREMENT OF SMALL-SIGNAL VHF-UHF TRANSISTOR SHORT-CIRCUIT FORWARD CURRENT TRANSFER RATIO: This standard describes the method to be used for the measurement of small-signal VHF-UHF transistor short-circuit forward current transfer ratio, in preparing data sheets for JEDEC registration of low power transistors. Formerly known as RS-371 and/or EIA-371.

February 1970; Reaffirmed April 1981, April 1999, March 2009 /JC-25 Committee $41.00

JESD 372

THE MEASUREMENT OF SMALL-SIGNAL VHF-UHF TRANSISTOR ADMITTANCE PARAMETERS: This standard describes the method to be used for the measurement of small-signal VHF-UHF transistor admittance parameters, in preparing data sheets for JEDEC registration of low power transistors. Formerly known as RS-372 and/or EIA-372

May 1970; Reaffirmed April 1981, April 1999, March 2009 /JC-25 Committee $43.00

JESD 390-A

STANDARD TEST PROCEDURE FOR NOISE MARGIN MEASUREMENTS FOR SEMICONDUCTOR LOGIC GATING MICROCIRCUITS, Reaffirmed September 2003. RESCINDED October 2008

February 1981; Rescinded October 2008 May 2008 /JC-13 Committee

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JESD 398

MEASUREMENT OF SMALL VALUES OF TRANSISTOR CAPACITANCE: This standard contains a three-terminal procedure for capacitance measurement with due precautions for shielding of extraneous effects due to terminal leads and metal enclosures. Formerly known as RS-398 and/or EIA-398

July 1972; Reaffirmed April 1981, April 1999, March 2009 /JC-25 Committee $43.00

JESD 435 **STANDARD FOR THE MEASUREMENT OF SMALL-SIGNAL TRANSISTOR SCATTERING PARAMETERS:** This standard

	STANDARD FOR THE MEASUREMENT OF SMALL-SIGNAL TRANSISTOR SCATTERING PARAMETERS: This standard specifies the standard for the measurement of small-signal transistor scattering parameters. Formerly known as RS-435 and/or EIA-435 April 1976; Reaffirmed April 1999, March 2009 /JC-25 Committee	$49.00

NUMBER	Joint Industry Guide (JIG)	PRICE
JIG -101-A	Material Composition Declaration for Electronic Products This document has been worked on for more than three years by member companies of EICTA (Europe), JGPSSI (Japan), EIA (USA) and JEDEC (USA). The purpose of this guide establishes the materials and substances to be disclosed by suppliers when those materials and substances are present in products and subparts that are incorporated into EEE. It benefits suppliers and their commercial customers by providing consistency and efficiency to the material declaration process. It promotes the development of consistent data exchange formats and tools that will facilitate and improve data transfer along the entire global supply chain. September 2007 January 2002 /JC-14 Committee	

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Committees

JC-10 Terms/Defin/Symbols

EIA 236-C	COLOR CODING OF DISCRETE SEMICONDUCTOR DEVICES:
EIA 321-C	NUMBERING OF LIKE-NAMED TERMINAL FUNCTIONS IN SEMICONDUCTOR DEVICES AND DESIGNATION OF UNITS IN MULTIPLE-UNIT SEMICONDUCTOR DEVICES:
JESD 370B	DESIGNATION SYSTEM FOR SEMICONDUCTOR DEVICES:
EIA 428-A	TYPE DESIGNATION SYSTEM FOR MICROELECTRONIC DEVICES
EIA 471	SYMBOL AND LABEL FOR ELECTROSTATIC SENSITIVE DEVICES:
JEP 100	TERMS, DEFINTIONS, AND LETTER SYMBOLS FOR MICROCOMPUTERS AND MEMORY INTEGRATED CIRCUITS: ELEVATED TO JESD100, August 1993.
JEP 103A	SUGGESTED PRODUCT-DOCUMENTATION, CLASSIFICATIONS, AND DISCLAIMERS
JEP 120-A	INDEX OF TERMS DEFINED IN JEDEC PUBLICATIONS:
JEP 75	LETTER SYMBOLS USED WITH INFRARED DEVICES - INCORPORATED INTO JESD77-A.
JEP 99	GLOSSARY OF MICROELECTRONIC TERMS, DEFINITIONS, AND SYMBOLS: ELEVATED TO JESD99, June 1985.
JESD 100B.01	TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR MICROCOMPUTERS, MICROPROCESSORS, AND MEMORY INTEGRATED CIRCUITS:
JESD 99B	TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR MICROELECTRONIC DEVICES:
JESD 99-1	ADDENDUM No. 1 to JESD99 - TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR ANALOG-TO-DIGITAL AND DIGITAL-TO-ANALOG CONVERTERS:
JEP 104C.01	REFERENCE GUIDE TO LETTER SYMBOLS FOR SEMICONDUCTOR DEVICES:
JESD 77B.01	TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR DISCRETE SEMICONDUCTOR AND OPTOELECTRONIC DEVICES:
JESD 88C	DICTIONARY OF TERMS FOR SOLID STATE TECHNOLOGY, Fourth Edition:

JC-11 Mechanical Pkg Outlines

JESD 95-1	DESIGN REQUIRMENTS FOR OUTLINES OF SOLID STATE AND RELATED PRODUCTS: DISCONTINUED AS A SEPARATE ITEM CONTAINED IN JEP95, BOOK 1, SECTION 4.
JESD 30E	DESCRIPTIVE DESIGNATION SYSTEM FOR SEMICONDUCTOR-DEVICE PACKAGES:
JEP 95 AUS	ANNUAL UPDATING SERVICE:
JEP 95	JEDEC REGISTERED AND STANDARD OUTLINES FOR SOLID STATE AND RELATED PRODUCTS:
JEP 86-A	RECOMMENDED PRACTICE FOR DUAL DIMENSIONING
JEB 20	ACCEPTED PRACTICES FOR MAKING MICROELECTRONIC DEVICE THERMAL CHARACTERISTICS TESTS
EIA 308-A	PREPARATION OF OUTLINE DRAWINGS OF SOLID-STATE PRODUCTS FOR JEDEC TYPE REGISTRATION:

JC-13 Government Liaison

EIA 623	PROCUREMENT QUALITY OF SOLID STATE COMPONENTS BY GOVERNMENT CONTRACTORS: RESCINDED, May 2006

EIA 625	REQUIREMENTS FOR HANDLING ELECTROSTATIC-DISCHARGE-SENSITIVE (ESDS) DEVICES (SUPERSEDES JEP108-B): SEE JESD625-A.
JESD 390-A	STANDARD TEST PROCEDURE FOR NOISE MARGIN MEASUREMENTS FOR SEMICONDUCTOR LOGIC GATING MICROCIRCUITS, Reaffirmed September 2003. RESCINDED October 2008
JEP 132	PROCESS CHARACTERIZATION GUIDELINE:
JEP 109-C	GENERAL REQUIREMENTS FOR DISTRIBUTORS OF MILITARY SEMICONDUCTOR DEVICES:
JEP 112	TEST METHOD FOR QUALIFICATION AND ACCEPTANCE OF CIRCUIT SUPPORT FILMS FOR USE IN MICROELECTRONIC APPLICATIONS - SUPERSEDED BY JESD72, June 2001
JESD 40	PROCUREMENT QUALITY OF SOLID STATE COMPONENTS BY GOVERNMENT CONTRACTORS - SUPERSEDED BY EIA-623, July 1994
JESD 42	REQUIREMENTS FOR HANDLING ELECTROSTATIC-DISCHARGE-SENSITIVE (ESDS) DEVICES - SUPERSEDED BY EIA-625, November 1994.
JESD 16-A	ASSESSMENT OF AVERAGE OUTGOING QUALITY LEVELS IN PARTS PER MILLION (PPM):
JESD 19	GENERAL STANDARD FOR STATISTICAL PROCESS CONTROL (SPC) - SUPERSEDED by EIA-557-A
JESD 49A	PROCUREMENT STANDARD FOR KNOWN GOOD DIE (KGD):
JEP 144	GUIDELINE FOR RESIDUAL GAS ANALYSIS (RGA) FOR MICROELECTRONIC PACKAGES

JC-13.2 Microelec. Devices

JESD 53	MANAGEMENT OF COMPONENT OBSOLESCENCE BY GOVERNMENT CONTRACTORS: RESCINDED, October 2002
JESD 26-A	GENERAL SPECIFICATION FOR PLASTIC ENCAPSULATED MICROCIRCUITS FOR USE IN RUGGED APPLICATIONS - RESCINDED, July 2001
JEP 121A	REQUIREMENTS FOR MICROELECTRONIC SCREENING AND TEST OPTIMIZATION:
JEP 111	TEST PROCEDURES FOR CUSTOM MONOLITHIC MICROCIRCUITS - SUPERSEDED BY MIL-PRF-38535C.
JEP 101-C	JEDEC REQUIREMENTS FOR CLASS B MICROCIRCUITS: RESCINDED, May 2006
EIA 554A	Method Selection for Assessment of Nonconforming Levels in Parts Per Million (PPM)

JC-13.4 Radiation Hardness

JESD 57	TEST PROCEDURE FOR THE MANAGEMENT OF SINGLE-EVENT EFFECTS IN SEMICONDUCTOR DEVICES FROM HEAVY ION IRRADIATION:
JESD 89A	MEASUREMENT AND REPORTING OF ALPHA PARTICLE AND TERRESTRIAL COSMIC RAY INDUCED SOFT ERRORS IN SEMICONDUCTOR DEVICES:

JC-13.5 Committee on Hybrid

JEP 142	GUIDELINE FOR OBTAINING AND ACCEPTING MATERIAL FOR USE IN HYBRID / MCM PRODUCTS:
JESD 72	TEST METHODS AND ACCEPTANCE PROCEDURES FOR THE EVALUATION OF POLYMERIC MATERIALS:
JESD 9-A	METAL PACKAGE SPECIFICATION FOR MICROELECTRONIC PACKAGES AND COVERS:
JESD 27	CERAMIC PACKAGE SPECIFICATION FOR MICROELECTRONIC PACKAGES:
JEP 105	JEDEC GUIDELINE FOR THE CHARACTERIZATION OF HYBRID POLYMERIC MATERIALS - SUPERSEDED BY JESD72, June 2001
JEP 107	TEST METHOD FOR QUALIFICATION AND ACCEPTANCE OF PARTICLE GETTERS FOR USE IN HYBRID MICROELECTRONIC APPLICATIONS - SUPERSEDED BY JESD72, June 2001
EIA 557B	STATISTICAL PROCESS CONTROL SYSTEMS:
JEP 114.01	GUIDELINES FOR PARTICLE IMPACT NOISE DETECTION (PIND) TESTING, OPERATOR TRAINING, AND CERTIFICATION:
JEP 133B	GUIDE FOR THE PRODUCTION AND ACQUISITION OF RADIATION-HARDNESS ASSURED MULTICHIP MODULES AND HYBRID MICROCIRCUITS:
JEP 96	GUIDELINES FOR NONDESTRUCTIVE PULL TESTING OF WIRE BONDS ON HYBRID DEVICES
JESD 93	HYBRIDS/MCM

JC-14 Quality/Reliability

JC-14 Quality/Reliability

JEP 155	RECOMMENDED ESD TARGET LEVELS FOR HBM/MM QUALIFICATION
JIG -101-A	Material Composition Declaration for Electronic Products
JESD JIG-101	Material Composition Declaration Guide for Electronic Products
JEB 16	USER GUIDE FOR MICROCIRCUIT FAILURE ANALYSIS:

JC-14.1 Rel.Test Meth.Pkg.Dev.

J-STD-020D.01	JOINT IPC/JEDEC STANDARD FOR MOISTURE/REFLOW SENSITIVITY CLASSIFICATION FOR NONHERMETIC SOLID STATE SURFACE-MOUNT DEVICES:
J-STD- 033B.1	JOINT IPC/JEDEC STANDARD FOR HANDLING, PACKING, SHIPPING AND USE OF MOISTURE/REFLOW SENSITIVE SURFACE-MOUNT DEVICES:
JEP 108-B	DISTRIBUTOR REQUIREMENTS FOR HANDLING ELECTROSTATIC -DISCHARGE SENSITIVE (ESDS) DEVICES: SUPERSEDED BY JESD42, March 1994.
JP 002	CURRENT TIN WHISKERS THEORY AND MITIGATION PRACTICES GUIDELINE
JEP 154	GUIDELINE FOR CHARACTERIZING SOLDER BUMP ELECTROMIGRATION UNDER CONSTANT CURRENT AND TEMPERATURE STRESS
JEP 153	CHARACTERIZATION AND MONITORING OF THERMAL STRESS TEST OVEN TEMPURATURES
JESD 22-B115	SOLDER BALL PULL
JESD 22-A122	POWER CYCLING
JESD 22-A100C	CYCLED TEMPERATURE HUMIDITY BIAS LIFE TEST:
JESD 22-A101C	STEADY-STATE TEMPERATURE HUMIDITY BIAS LIFE TEST:
JESD 22-A102-C	ACCELERATED MOISTURE RESISTANCE - UNBIASED AUTOCLAVE:
JESD 22-A103C	HIGH TEMPERATURE STORAGE LIFE:
JESD 22-A104D	TEMPERATURE CYCLING:
JESD 22-A106B	THERMAL SHOCK:
JESD 22-A107B	SALT ATMOSPHERE:
JESD 22-A109-A	HERMETICITY:
JESD 22-A110C	HIGHLY ACCELERATED TEMPERATURE AND HUMIDITY STRESS TEST (HAST)
JESD 22-A112-A	MOISTURE-INDUCED STRESS SENSITIVITY FOR PLASTIC SURFACE MOUNT DEVICES - SUPERSEDED BY J-STD-020A, April 1999.
JESD 22-A113F	PRECONDITIONING OF PLASTIC SURFACE MOUNT DEVICES PRIOR TO RELIABILITY TESTING:
JESD 22-A114F	ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY TESTING HUMAN BODY MODEL (HBM):
JESD 22-A115-A	ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY TESTING MACHINE MODEL (MM):
JESD 22-B100B	PHYSICAL DIMENSION:
JESD 22-B101A	EXTERNAL VISUAL:
JESD 22-B102E	SOLDERABILITY:
JESD 22-B103B	VIBRATION, VARIABLE FREQUENCY:
JESD 22-B104C	MECHANICAL SHOCK:
JESD 22-B105C	LEAD INTEGRITY:
JESD 22-B106D	RESISTANCE TO SOLDER SHOCK FOR THROUGH-HOLE MOUNTED DEVICES:

JESD 22-B107C MARKING PERMANENCY:

JESD 22-B108A COPLANARITY TEST FOR SURFACE-MOUNT SEMICONDUCTOR DEVICES:

JESD 22-B116 WIRE BOND SHEAR TEST:

JESD 22-C100-A HIGH TEMPERATURE CONTINUITY - RESCINDED, November 1999

JESD 22-C101D FIELD-INDUCED CHARGED-DEVICE MODEL TEST METHOD FOR ELECTROSTATIC DISCHARGE WITHSTAND THRESHOLDS OF MICROELECTRONIC COMPONENTS:

JEP 113-B SYMBOL AND LABELS FOR MOISTURE-SENSITIVE DEVICES:

JEP 122E FAILURE MECHANISMS AND MODELS FOR SEMICONDUCTOR DEVICES:

JESD 22-A118 ACCELERATED MOISTURE RESISTANCE - UNBIASED HAST:

JESD 22-B110A SUBASSEMBLY MECHANICAL SHOCK:

JESD 22-A120A TEST METHOD FOR THE MEASUREMENT OF MOISTURE DIFFUSIVITY AND WATER SOLUBILITY IN ORGANIC MATERIALS USED IN INTEGRATED CIRCUITS:

JESD 78B IC LATCH-UP TEST:

JESD 625-A REQUIREMENTS FOR HANDLING ELECTROSTATIC-DISCHARGE-SENSITIVE (ESDS) DEVICES:

JESD 22-A108C TEMPERATURE, BIAS, AND OPERATING LIFE:

JESD 22-B117A SOLDER BALL SHEAR:

JESD 22-B109A FLIP CHIP TENSILE PULL:

JEP 140 BEADED THERMOCOUPLE TEMPERATURE MEASUREMENT OF SEMICONDUCTOR PACKAGES:

J-STD- 002B SOLDERABILITY TESTS FOR COMPONENT LEADS, TERMINATIONS, LUGS, TERMINALS AND WIRES:

JESD 22-B113 BOARD LEVEL CYCLIC BEND TEST METHOD FOR INTERCONNECT RELIABILITY CHARACTERIZATION OF COMPONENTS FOR HANDHELD ELECTRONIC PRODUCTS

JESD 22-B111 BOARD LEVEL DROP TEST METHOD OF COMPONENTS FOR HANDHELD ELECTRONIC PRODUCTS:

JESD 22-B112 HIGH TEMPERATURE PACKAGE WARPAGE MEASUREMENT METHODOLOGY

JESD 22-A121A MEASURING WHISKER GROWTH ON TIN AND TIN ALLOY SURFACE FINISHES

JESD 89-2A TEST METHOD FOR ALPHA SOURCE ACCELERATED SOFT ERROR RATE:

JESD 22-A119 LOW TEMPERATURE STORAGE LIFE

JS 9702 IPC/JEDEC-9702: MONOTONIC BEND CHARACTERIZATION OF BOARD-LEVEL INTERCONNECTS (IPC/JEDEC-9702)

JESD 22-A105C POWER AND TEMPERATURE CYCLING:

JESD 97 MARKING, SYMBOLS, AND LABELS FOR IDENTIFICATION OF LEAD (Pb) FREE ASSEMBLIES, COMPONENTS, AND DEVICES - SUPERSEDED BY J-STD-609, August 2007

JESD 22-A111 EVALUATION PROCEDURE FOR DETERMINING CAPABILITY TO BOTTOM SIDE BOARD ATTACH BY FULL BODY SOLDER IMMERSION OF SMALL SURFACE MOUNT SOLID STATE DEVICES:

JESD 89-1A TEST METHOD FOR REAL-TIME SOFT ERROR RATE:

JS 9704 IPC/JEDEC-9704: Printed Wiring Board (PWB) Strain Gage Test Guideline

JESD 89-3A TEST METHOD FOR BEAM ACCELERATED SOFT ERROR RATE

JC-14.1B JEDEC/IPC Joint Task

J-STD- 035 JOINT IPC/JEDEC STANDARD FOR ACOUSTIC MICROSCOPY FOR NONHERMETRIC ENCAPSULATED ELECTRONIC COMPONENTS:

JC-14.2 Wafer Level Reliab

JEP 119A A PROCEDURE FOR EXECUTING SWEAT:

JEP 128 GUIDE FOR STANDARD PROBE PAD SIZES AND LAYOUTS FOR WAFER LEVEL ELECTRICAL TESTING:

JP 001.01	FOUNDRY PROCESS QUALIFICATION GUIDELINES (Wafer Fabrication Manufacturing Sites)
JESD 28-1	N-CHANNEL MOSFET HOT CARRIER DATA ANALYSIS:
JESD 87	STANDARD TEST STRUCTURE FOR RELIABILITY ASSESSMENT OF AlCu METALLIZATIONS WITH BARRIER MATERIALS
JEP 139	GUIDELINE FOR CONSTANT TEMPERATURE AGING TO CHARACTERIZE ALUMINUM INTERCONNECT METALLIZATIONS FOR STRESS-INDUCED VOIDING:
JESD 28-A	A PROCEDURE FOR MEASURING N-CHANNEL MOSFET HOT-CARRIER-INDUCED DEGRADATION UNDER DC STRESS:
JESD 37	STANDARD LOGNORMAL ANALYSIS OF UNCENSORED DATA, AND OF SINGLY RIGHT -CENSORED DATA UTILIZING THE PERSSON AND ROOTZEN METHOD:
JESD 33-B	STANDARD METHOD FOR MEASURING AND USING THE TEMPERATURE COEFFICIENT OF RESISTANCE TO DETERMINE THE TEMPERATURE OF A METALLIZATION LINE:
JESD 34	FAILURE-MECHANISM-DRIVEN RELIABILITY QUALIFICATION OF SILICON DEVICES:
JESD 35-A	PROCEDURE FOR WAFER-LEVEL-TESTING OF THIN DIELECTRICS:
JESD 35-1	ADDENDUM No. 1 to JESD35 - GENERAL GUIDELINES FOR DESIGNING TEST STRUCTURES FOR THE WAFER-LEVEL TESTING OF THIN DIELECTRICS:
JESD 35-2	ADDENDUM No. 2 to JESD35 - TEST CRITERIA FOR THE WAFER-LEVEL TESTING OF THIN DIELECTRICS:
JESD 60A	A PROCEDURE FOR MEASURING P-CHANNEL MOSFET HOT-CARRIER-INDUCED DEGRADATION AT MAXIMUM GATE CURRENT UNDER DC STRESS:
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JESD 92	PROCEDURE FOR CHARACTERIZING TIME-DEPENDENT DIELECTRIC BREAKDOWN OF ULTRA-THIN GATE DIELECTRICS:
JESD 202	METHOD FOR CHARACTERIZING THE ELECTROMIGRATION FAILURE TIME DISTRIBUTION OF INTERCONNECTS UNDER CONSTANT-CURRENT AND TEMPERATURE STRESS:
JESD 90	A PROCEDURE FOR MEASURING P-CHANNEL MOSFET NEGATIVE BIAS TEMPERATURE INSTABILITIES

JC-14.3 Silicon Devices RQM

JEP 150	STRESS-TEST-DRIVEN QUALIFICATION OF AND FAILURE MECHANISMS ASSOCIATED WITH ASSEMBLED SOLID STATE SURFACE-MOUNT COMPONENTS
JEP 149	APPLICATION THERMAL DERATING METHODOLOGIES:
JESD 94A	APPLICATION SPECIFIC QUALIFICATION USING KNOWLEDGE BASED TEST METHODOLOGY:
JESD 201A	ENVIRONMENTAL ACCEPTANCE REQUIREMENTS FOR TIN WHISKER SUSCEPTIBILITY OF TIN AND TIN ALLOY SURFACE FINISHED:
JESD 22B114	MARK LEGIBILITY
JEP 148A	RELIABILITY QUALIFICATION OF SEMICONDUCTOR DEVICES BASED ON PHYSICS OF FAILURE RISK AND OPPORTUNITY ASSESSMENT
JESD 62-A	OUTLIER IDENTIFICATION AND MANAGEMENT SYSTEM FOR ELECTRONIC COMPONENTS, RESCINDED January 2009. Replaced by JESD50.
JESD 659B	FAILURE-MECHANISM-DRIVEN RELIABILITY MONITORING:
JESD 47G	STRESS-TEST-DRIVEN QUALIFICATION OF INTEGRATED CIRCUITS:
JESD 50B.01	SPECIAL REQUIREMENTS FOR MAVERICK PRODUCT ELIMINATION AND OUTLIER MANAGEMENT
JESD 29-A	FAILURE-MECHANISM-DRIVEN RELIABILITY MONITORING - SUPERSEDED BY EIA/ANSI-659, July 1996.
JESD 69B	INFORMATION REQUIREMENTS FOR THE QUALIFICATION OF SILICON DEVICES:
JESD 74A	EARLY LIFE FAILURE RATE CALCULATION PROCEDURE FOR SEMICONDUCTOR COMPONENTS:
JESD 85	METHODS FOR CALCULATING FAILURE RATES IN UNITS OF FITS:
JESD 86	ELECTRICAL PARAMETERS ASSESSMENT:
JEP 143B.01	SOLID STATE RELIABILITY ASSESSMENT QUALIFICATION METHODOLOGIES:

JESD 91-A METHOD FOR DEVELOPING ACCELERATION MODELS FOR ELECTRONIC COMPONENT FAILURE MECHANISMS:

JESD 22-A117B ELECTRICALLY ERASABLE PROGRAMMABLE ROM (EEPROM) PROGRAM/ERASE ENDURANCE AND DATA RETENTION TEST:

JEP 156 CHIP-PACKAGE INTERACTION UNDERSTANDING, IDENTIFICATION AND EVALUATION:

EIA 659 FAILURE-MECHANISM-DRIVEN RELIABILITY MONITORING (SUPERSEDES JESD29-A): SEE JESD659, latest edition.

JC-14.4 Quality System Stand

EIA 670 QUALITY SYSTEM ASSESSMENT (SUPERSEDES JESD39-A):

EIA 671 COMPONENT PROBLEM ANALYSIS AND CORRECTIVE ACTION REQUIREMENTS: SEE JESD671-A.

EIA 599-A NATIONAL ELECTRONIC PROCESS CERTIFICATION STANDARD; GOVERNMENT CONTRACTORS:

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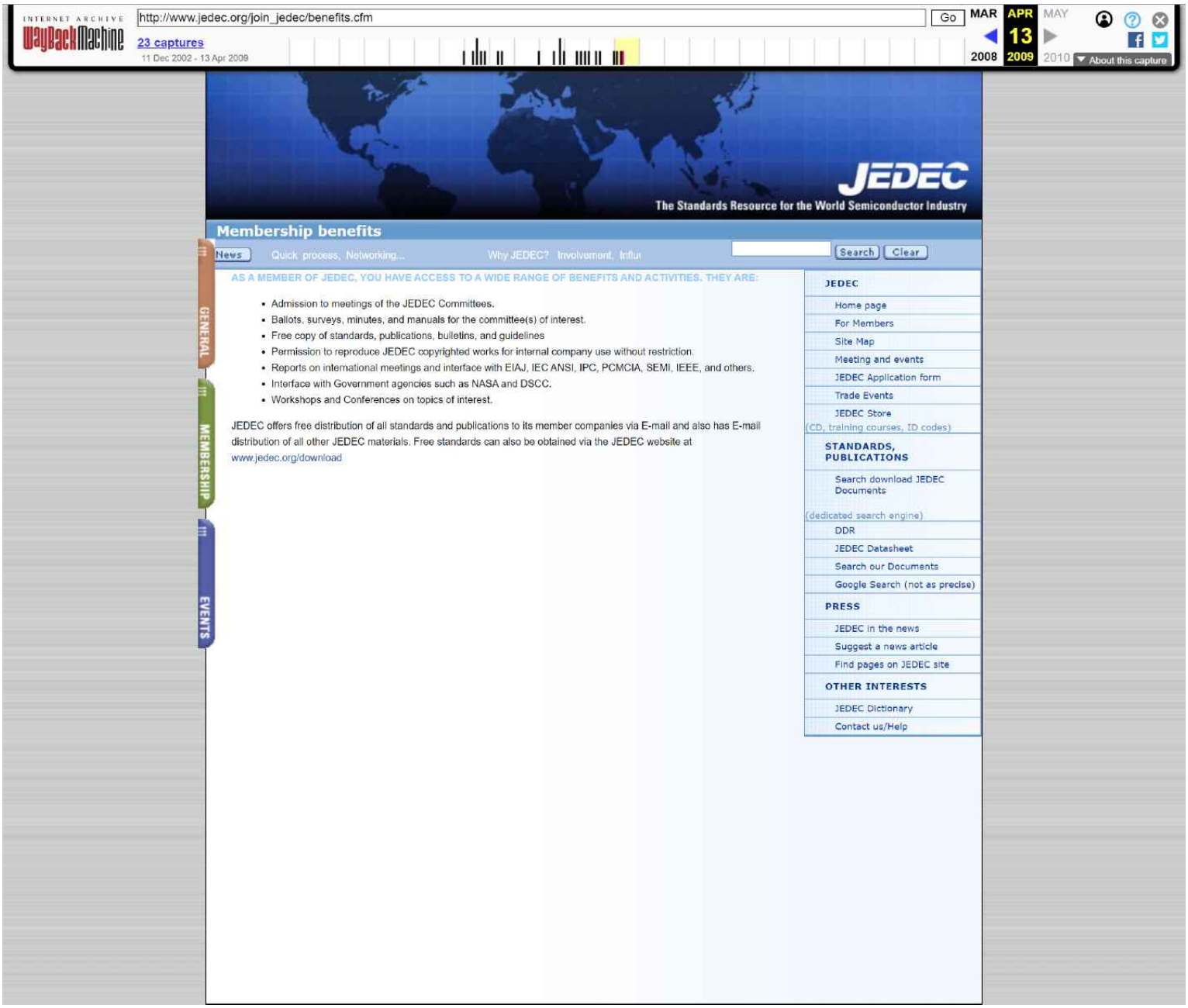
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