

IPR~~2022-00062~~2022-00064

4 U.S. Patent No.

~~9,858,218~~10,474,595

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner, v.

NETLIST, INC.,

Patent Owner.

Case No. IPR~~2022-00062~~2022-00064

U.S. Patent No. ~~9,858,218~~10,474,595

DECLARATION OF ROBERT J. MURPHY

Netlist, Inc. Ex. 2027
Samsung Electronics Co., Ltd. v. Netlist, Inc.

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n. Cover

Samsung Electronics Co., Ltd.

Ex. 1078, p. 1

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Appendix	Description
A	Curriculum Vitae of Robert J. Murphy

I, Robert J. Murphy, make this declaration in connection with the U.S. Patent No. ~~9,858,218~~10,474,595

identified above.

I. INTRODUCTION

1. I have been retained by counsel for Netlist, Inc. (“the Patent Owner”) as a technical expert in connection with the proceeding identified above. I submit this declaration in support of Patent Owner’s Response to the Petition for Inter Partes Review of United States Patent No. ~~9,858,218~~10,474,595 (“the ‘~~218~~595 Patent”) (IPR~~2022-00062~~2022-00064) (“Petition” or “Pet.”). I previously submitted a declaration in support of Patent Owner’s Preliminary Response to the same Petition for Inter Partes Review. ~~Exhibit~~(Ex. 2001). I have been retained to provide a technical opinion concerning the ‘~~218~~595 Patent, the IPR~~2022-00062~~2022-00064 Petition, and certain exhibits and references cited in that Petition, which are discussed in further detail below.

II. EXPERT QUALIFICATIONS

2. I have over forty-five years of experience in the semiconductor industry, and have experience in the design of high speed, high complexity semiconductor products, including Full Custom Microprocessors, E2CMOS and BiCMOS PALs, CMOS and NMOS SRAMs (Static Random Access Memory), CCDs, DRAMs (Conventional and Pseudo-Static), and RAD Hard SOS CMOS.

3. I earned a Bachelor of Science Degree in Electrical Engineering in 1974 from Drexel University, in Philadelphia, Pennsylvania. I earned a Master of

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Science Degree in Electrical Engineering in 1976 from the University of California, Los Angeles.

4. Since January, 2021 I have been employed as the VP of Engineering for IC Manage, a company that makes software tools to assist in the design of Integrated Circuits.

5. Before that, since 1998, I was self-employed in my own consulting business known as Firenza, LLC, which is an outsource engineering design company that assists in the design and implementation of semiconductor devices. I currently continue my consulting activities at Firenza, LLC. Additionally, I perform expert witness work as available. For example, I was an expert witness or consultant for Netlist in the related matters of *In the Matter of Certain Memory Modules and Components Thereof and Products Containing Same*, Inv. No. 337- TA-1023 (USITC filed September 1, 2016), *In the Matter of Certain Memory Modules and Components Thereof and Products Containing Same*, Inv. No. 337- TA-1089 (USITC filed October 31, 2017) and *Inter Partes* Reviews of related U.S. Patent No. 8,489,837, Case No. IPR2017-00548, and U.S. Patent No. 9,535,623, Case No. IPR2017-00303. In addition, I was an expert witness or consultant for Netlist in the prior Inter Partes Review proceedings concerning the ‘~~218~~595 Patent, Case No. IPR~~2020-01044~~2020-01042, as well as U.S. Patent No. ~~10,474,595~~9,858,218, Case No. IPR ~~2020-01042~~2020-01044.

6. Before founding Firenza, LLC, I was Director of Engineering at

Silicon Graphics, Inc. ("SGI") in Mountain View, California. I was employed by SGI from June 1992 through April 1998. I was involved in the hiring, management and direction of circuit engineers in processor and floating point chip designs. I also assisted in the design of phase locked loops ("PLL").

7. Prior to SGI, I worked with Weitek Corporation in Sunnyvale, California, from February 1989 to June 1992, achieving the position of Director of Engineering in 1990. While at Weitek, I was charged with, among other things, the responsibility for designing circuitry to implement high performance memory, output drivers, and electrostatic discharge (ESD) devices. Examples include a 40 MHz SPARC combined IU/FPU product and a floating point coprocessor compatible with the Intel i486.

8. Before Weitek, I was employed by National Semiconductor Corporation in Santa Clara, California from October 1985 through February 1989. I achieved the position of design manager and chief technical contributor for their E2CMOS PAL group. Significant design projects included the world's first BiCMOS PAL, and improved Ti-W fuse blowing circuitry. Prior to my employment with National Semiconductor, I worked with RCA in Sommerville, New Jersey from April 1982 to October 1983. There, I led an inter-divisional program to develop 2 micron CMOS technology, and also helped design a 64K SRAM (Static Random Access Memory).

9. Prior to RCA, I was an SRAM design manager with National

Semiconductor in Santa Clara, California and West Jordan, Utah from February No. 9,858,218 10,474,595 1978 to April 1982. I directed the design of a 4T cell 4K SRAM product, and was promoted to Section Head when my first design went into production on the first mask set. I was later promoted to Design Manager. My first design at National Semiconductor was a Pseudo-Static DRAM. Before National Semiconductor I worked for Hughes Aircraft in El Segundo, California from June 1974 to February 1978. This began as a part-time position, wherein I worked as a Test Engineer testing space flight sub-assemblies, and later became an integrated circuit designer, all while obtaining my Master's Degree.

10. My professional background and technical qualifications are stated above and are reflected in my Curriculum Vitae, attached as Appendix A to this Declaration.

11. I have no personal or financial stake or interest in the outcome of the present Petition for *inter partes* review.

12. This declaration is based on information known to me as of the date of this declaration, and I reserve the right to modify or expand upon my opinions based on new information and in response to additional discovery, rulings, declarations and testimony. I further reserve the right to provide additional opinions, if requested of me. I have not previously testified as an expert witness at trial, hearing, or by deposition during the last four years, other than what is disclosed on my Curriculum Vitae and in this declaration.

III. MATERIALS CONSIDERED

13. In forming the opinions set forth in this declaration, I have considered and relied upon my education, knowledge of the relevant field, and my experience. I have also reviewed and considered the specification of the ‘~~218~~595 Patent and the prosecution history of the ‘~~218~~595 Patent. I understand that Samsung Electronics Co., Ltd. (“Samsung” or “Petitioner”) has requested *inter partes* review of the ‘~~218~~595 Patent in a Petition dated October 15, 2021 (IPR~~2022-00062~~2022-00064), and that the United States Patent Trial and Appeal Board granted institution of that Petition on May 16, 2020 (Paper 14). I understand that the October 15, 2021 Petition was accompanied by an expert declaration by Dr. Donald Alpert (Ex. 1003, “Alpert Declaration” or “Alpert Decl.”) dated September 15, 2021. I further understand that Dr. Alpert was deposed on July 26 and 27, 2022, in connection with this matter (Ex. 2023, “Alpert Transcript” or “Alpert Tr.”). I have reviewed the Petition, the Alpert Declaration, the Alpert Transcript, as well as the additional exhibits cited or referenced in each.

14. I understand that in the Petition, Samsung requested the Patent Trial and Appeal Board (“the Board”) to institute an *inter partes* review of claims ~~1-22~~1-24 of the ‘~~218~~595 Patent based on references cited in the Petition. I have reviewed and am familiar with those references, which include:

- U.S. Patent Application Publication No. 2008/0098277 to Hazelzet

(“Hazelzet”);

U.S. Patent No.

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- JEDEC Committee Letter Ballot, Committee: JC-40.4, Committee Item

Number: 142.35 (“JEDEC”);

- U.S. Patent No. 8,139,430 to Buchmann et al. (“Buchmann”); and
- U.S. Patent No. 8,359,521 to Kim et al. (“Kim”).

I have also reviewed and considered the other exhibits attached to the Petition (Exhibits 1001 through 1067), as well as those cited in the Alpert Declaration, the exhibits referenced in the Alpert Transcript, and the additional references as cited herein, each of which also form the basis of my opinions. I have reviewed the Institution Decision dated May 16, 2022. I have also reviewed the deposition transcripts of John Halbert (Ex. 2022), Julie Carlson (Ex. 2024), and Sung Joo Park (Ex. 2025). I have reviewed all exhibits submitted by Patent Owner in this matter.

IV. DEFINITIONS AND STANDARDS

15. I have been informed and understand that claims are construed from the perspective of a hypothetical person of ordinary skill in the art (“POSITA”) at the time of the claimed invention. I understand that, in this proceeding, the claims should be given their ordinary and accustomed meaning as understood by one of ordinary skill in the art in view of the patent and its file history.

16. With respect to anticipation under 35 U.S.C. § 102, I have been informed that a single reference must describe the claimed invention with sufficient precision and detail to establish that the subject matter existed in the

prior art. I understand that a vague or ambiguous teaching that neither discloses nor enables the claimed invention cannot anticipate the invention. I understand that a limitation may be deemed inherently disclosed in a prior-art reference, but only if it is necessarily present in the prior-art reference, as opposed to being merely probable or possible.

17. I have also been informed and understand that the subject matter of a patent claim is obvious under 35 U.S.C. § 103 if the differences between the subject matter of the claim and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a POSITA. I have also been informed that the framework for determining obviousness involves considering the following factors: (i) the scope and content of the prior art; (ii) the differences between the prior art and the claimed subject matter; (iii) the level of ordinary skill in the art; and (iv) any objective evidence of non-obviousness. I understand that the claimed subject matter would have been obvious to a POSITA if, for example, it results from the combination of known elements according to known methods to yield predictable results, the simple substitution of one known element for another to obtain predictable results, use of a known technique to improve similar devices in the same way or applying a known technique to a known device ready for improvement to yield predictable results. I have also been informed that the

analysis of obviousness may include recourse to logic, judgment, and common sense available to a POSITA that does not necessarily require explanation in any reference.

18. I understand that 35 U.S.C. § 112 imposes a “written description” requirement on patentees. I understand the “written description” requirement is met if a person of ordinary skill in the art would have understood the inventor to have been in possession of the claimed invention at the time of filing, even if every nuance of the claims is not explicitly described in the specification.

V. LEVEL OF ORDINARY SKILL IN THE ART

19. I understand that U.S. patent law interprets patents and prior art from the point of view of a hypothetical person of ordinary skill in the art (“POSITA”).

20. The field of the ‘~~218~~595 Patent includes memory module initialization and training sequencing. Professionals in these fields will generally be electrical engineers, computer engineers, or computer scientists.

21. I understand that Petitioner proposed that a person of ordinary skill in the art would have “a bachelor’s degree in computer engineering, or a related field, and several years of additional experience working with computer memory systems. [POSITA] would have been familiar with computer memory systems and basic CPU architecture documented in the literature, including standards, and generally available in commercial systems, including how computer components access a

computer's memory, the role of a memory controller, the basic operation of memory modules and devices, and the techniques used to couple memory devices to the other components of the computer system.” (Pet. at 10).

22. I also understand that Patent Owner has previously proposed that a person of ordinary skill in the art for a related proceeding would have a Bachelor's degree in electrical engineering, computer engineering, or in a related field and at least one year of work experience relating to memory systems, and would be familiar with the design of memory devices and modules. *See Netlist, Inc. v. SK Hynix, Inc.*, 8:16-CV-1605 (C.D. Cal.), Dkt. 124 at 6.

23. In my review of the ‘~~218~~595 Patent, from my education, from my knowledge of the relevant field, and my experience, and for the same reasons stated above, I agree with the Patent Owner's proposal for the level ordinary skill in the art. I meet these criteria under either Petitioner's proposed level of skill and Patent Owner's proposed level of skill, at least because electrical engineering is a “related field” to computer engineering. I consider myself to be a person with at least ordinary skill in the art pertaining to the ‘~~218~~595 Patent and knew what others of ordinary skill in the art at the relevant time would have known. In addition, I was a person of ordinary skill in the art at the time of invention of the ‘~~218~~595 Patent and knew what others of ordinary skill in the art at the relevant time would have known.

24. The ‘~~218~~595 Patent is a continuation of a series of continuations of a

utility application filed June 14, 2010, and also claims priority to U.S. Provisional Application No. ~~9,858,218~~10,474,595 Application No. 61/186,799 (Ex. 1008) (the “Provisional”), filed June 12, 2009. (Ex. 1001). I see that the Petition and Dr. Alpert dispute the priority date of the ‘~~218~~595 Patent. (Pet. at 5-10; Ex. 1003, Alpert Decl., Section III.A). The Petition contends that the priority date is June 14, 2010. (Pet. at 10). As discussed below, it is my opinion that the priority date of the ‘~~218~~595 Patent is June 12,

2009, and I will support that conclusion in a later section of this declaration. My opinion of a person of ordinary skill in the art does not change whether the priority date is June 12, 2009 or June 14, 2010.

VI. CLAIM CONSTRUCTION

25. I understand that Samsung has provided some proposed constructions of three claim phrases in the ‘~~218~~595 Patent claims. (Pet. at ~~20-24~~18-24). I have also read the Board’s Decision Granting Institution of Inter Partes Review in IPR2020- ~~01044~~01042 that addressed claim construction of the ‘~~218~~595 Patent. (IPR~~2020-01044~~2020-01042 Paper ~~13~~14). I disagree with Petitioner that its proposed constructions are accurately represent how a POSITA would understand the ‘~~218~~595 Patent claims.

26. I understand that Petitioner contends that “*memory read or write operations*” in the ‘~~218~~595 Patent claims means “operations used to communicate data between the memory module and the memory controller in response to commands from the memory controller.” (Pet. at ~~20-21~~18-19). This is not how a

POSITA would understand this claim phrase. In particular, “memory read or write operations” are well-known functions of memory devices and have a plain, ordinary, and understood meaning in the art. By contrast, “operations used to communicate data ... in response to commands from the memory controller” refers potentially to a significantly more expansive list of operations that extend beyond what a POSITA would understand to be a “memory read” or a “memory write” operation. For instance, essentially *any* signal sent between the memory module and the memory controller—including commands that are not themselves “read operations” or “write operations,” or indeed the “notification signal” described in the ‘~~218~~595 Patent—could potentially qualify as communication of “data ... in response to commands from the memory controller.” I understand that the Board previously declined to construe this phrase in a related IPR

(IPR~~2020-01044~~2020-01042). In my opinion, therefore, the plain and ordinary meaning of this claim phrase accurately reflects a POSITA’s understanding of the ‘595 Patent.

27. I understand that Petitioner further contends that “*normal* memory read or write operations” should have an identical meaning to “memory read or write operations.” (Pet. at 19-21). I disagree. The phrases “memory read or write operations” and “*normal* memory read or write operations” are separately discussed in the specification and recited in different claims of the ‘595 Patent.

28. The specification of the ‘595 patent explains that memory read and/or

write operations are conducted “according to an industry standard.” (Ex. 1001 at 21). ~~9,858,218~~ 10,474,595

1:54-57; 2:7-11, 15-19; 8:4-12). These explanations are *without* reference to “normal” memory read and/or write operations, meaning that the ‘595 Patent explicitly (and correctly) recognizes that a POSITA would understand the meaning of “memory read or write operations,” and that this understanding would be informed by “industry standard[s].” (Ex. 1001 at 1:54-57; 2:7-11, 15-19; 8:4-12). The ‘595 Patent then *separately* explains that “normal” read and write operations are specifically those that occur during the “operational mode,” which is the “normal mode” “during standard computer operation *not associated with initialization*”:

The operational mode is the normal mode of the memory module 10. For example, during the operational mode, the memory module 10 is generally accessed by the system memory controller 14 of the host computer 16 *during standard computer operation not associated with initialization.*

(Ex. 1001 at 6:45-50). The ‘595 Patent also describes using an error-out pin that “generates an interrupt communicated to the system during the initialization period and indicative of completion of the required or requested task,” and that “[a]ssertion of the same pin during normal (*non-initialization*) operation upon an error occurring ... generates an interrupt communicated to the system during the *normal operation* indicative of the occurrence of the error condition.” Ex. 1001 at 8:49-67. A POSITA would thus have understood that the ‘595 Patent draws an intentional distinction between *any* “memory read or write operations” on one hand, and the

“*normal* memory read or write operations” on the other. A POSITA would have understood the plain and ordinary meaning of “*normal* memory read or write operations” to refer to operations that only occur during the “normal mode” and *not* during “initialization,” and would further have understood that this refers to a sub-set of the operations otherwise comprising “memory read or write operations.”

29. In my opinion, this is confirmed by the differing references in the claims to either “memory read or write operations” and “*normal* memory read or write operations.” (Ex. 1001 at claim 17 (“memory read or write operations”), claim 1 (“*normal* memory read or write operations”). If these terms were equated, as Petitioner incorrectly suggests, it would render the term “normal” meaningless in those claims that refer to “*normal* memory read or write operations.” However, as discussed above, “normal operation” is a term of art in field, consistent with the patent’s description of a normal operational mode, and thus, a POSITA would have understood “*normal* memory read or write operations” to refer to read and write operations that specifically occur during the “operational mode,” which is the “normal mode.” In my opinion, therefore, the plain and ordinary meaning of this claim phrase accurately reflects a POSITA’s understanding of the ‘~~218~~595 Patent.

30. ~~27~~I understand that Petitioner contends that “*training sequence*” means “a set of operations occurring in a particular order and used for training.” (Pet. at 22-23). This proposal is unhelpful as a POSITA would understand the plain

and ordinary meaning of “training sequences” in the context of the ‘~~218,595~~Patent No. 9,858,21810,474,595’ and memory device technology generally. In particular, the proposal is circular with respect to the term “training.” Furthermore, a POSITA would understand that “training sequences,” in the context of memory devices, do not necessarily need to be performed in a certain “particular order.” In my opinion, therefore, the plain and ordinary meaning of this claim phrase accurately reflects a POSITA’s understanding of the ‘~~218,595~~Patent’.

31. ~~28.~~ I understand that Petitioner also proposes that several longer claim phrases which include “training sequences” mean “unscheduled signal/information/open-drain signals provided without polling that indicate the status of the one or more training sequences.” (Pet. at 23-24). I understand that a prior district court ruling determined that these terms should have their “plain and ordinary meaning, which does not encompass polling.” (Ex. 1061 at 2-3). I agree with the district court’s prior construction. Therefore, all Petitioner’s proposal appears to add is that the various signals referenced are “unscheduled,” which only adds ambiguity (as to what “unscheduled” means or how Petitioner interprets that word) into otherwise well-understood terms. A POSITA would further not understand this additional limitation to be part of these claim phrases because “unscheduled” signals are never mentioned in the ‘~~218,595~~Patent’. In my opinion, therefore, the plain and ordinary meaning of these claim phrases (which does not encompass polling) accurately reflect a POSITA’s understanding of the ‘~~218,595~~Patent’.

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32. ~~29.~~ Notwithstanding the above, my ensuing analysis is the same regardless of whether Petitioner's proposed constructions are accepted or whether their plain and ordinary meaning controls. I also reserve the right to offer claim constructions and address Samsung's claim constructions in this proceeding if requested to do so.

VII. RELEVANT INFORMATION CONCERNING THE '~~218~~595 PATENT

A. The Correct Priority Date of the '~~218~~595 Patent is June 12, 2009

33. ~~30.~~ I have been asked to opine on the priority date of the '~~218~~595 Patent. I understand that Petitioner and its expert argue that the '~~218~~595 Patent is not entitled to its priority date of June 12, 2009 because they claim certain claim elements are not disclosed in the Provisional. (Pet. at 5-10; Ex. 1003 at Section III.A). I disagree. A review of the Provisional shows that there is written description support for all of the disputed claim elements.

B. ~~1.~~ The Provisional Supports ~~the '218 Patent Claims Reciting That "the First Edge Connections Are not Active"~~ The Element of Claim 1 Involving "Normal Read and Write Operations" And Other Independent Claims Petitioner Identifies

34. ~~31.~~ In my opinion, the Petition incorrectly asserts that the ~~claim-~~
~~elements requiring "train[ing] with~~ Provisional does not provide written
description support for the '595 patent claims which varyingly reciting a "second

mode” during which the memory module “is not accessed by the memory controller for normal memory read or write operations,” *or* “one or more training sequences ~~while~~” during which the ~~first edge connections are not active,~~ are not sufficiently disclosed in the Provisional. (Pet. at 5-10). memory module “is not accessed by the memory controller for memory read or write operations.” (Pet. at 5-8; Ex. 1001 at claims 1, 10, 17, 21).

35. I first note that Petitioner does not address the material differences between the language of these four claims, and only refers to the element of claim 1, which recites that the memory module is “not accessed” for “normal memory read or write operations” during the “second mode.” (Ex. 1001 at claim 1). As I explained above in Section [Claim Construction], a POSITA would understand the plain and ordinary meaning of “normal memory read or write operations” to *exclude* “memory read or write operations” conducted during “initialization.”

36. In my opinion, the Provisional discloses an “initialization” mode (what the ‘595 Patent refers to as the “second mode”) during which there are no “normal memory read or write operations” as a POSITA would understand that term. The Provisional discloses two modes of operation: “normal operation” and “initialization.” (Ex. 1008 at 22-23, Figure 3.) In my opinion, these align, respectively, with the “first mode” (also called the “normal mode”) and the “second mode” (also called the “initialization sequences”) recited in the ‘595 Patent claims.

37. The Provisional further discloses that “normal operation” U.S. Patent No.

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coincide with “initialization.” Specifically, a POSITA would have understood that “normal operation” refers to standard computer operations, such as the use of the memory system for running user applications on a computer system, and that by contrast, “initialization” refers to the steps required to enable the memory system to function in normal operation.

38. The disclosures in the Provisional reinforce this understanding. For instance, the Provisional discloses using a single physical pin for two different purposes (a “notifying signal” or an “error-out” signal). (Ex. 1008 at 22). During “initialization” (the “second mode”), the shared pin is acting as a “notifying signal,” and “[t]he output of the notifying signal is low impedance while the memory subsystem controller [is] executing each section of the initialization step.” (Ex. 1008 at 23). Then, as each step is completed, the “notifying signal” is driven high, “indicat[ing] that training is done” and the system is ready for “normal operation.” (Ex. 1008 at 23, Figure 3). Once in “normal operation,” the signal on the shared pin has a different function (providing an “error-out” signal) and remains “high during normal operation unless a parity error occurs.” (Ex. 1008 at Figure 3). Thus, a POSITA would have understood that “normal memory read or write operations” only occur during normal operation and cannot occur during initialization, and would further understand that those two modes cannot coincide. In my opinion, therefore, the Provisional provides written description for this element of claim 1.

39. I note that the remaining claims challenged by Petitioner U.S. Patent No.

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“normal memory read or write operations”—claim 17, for instance, instead recites

“one or more training sequences while the memory module is not accessed by the
memory controller for memory read or write operations.” (Ex. 1001 at claim 17).

Petitioner does not offer any explanation as to why its argument with respect to
claim 1 would also apply to these materially different claims. In my opinion, these

other claim elements of the other claims have different requirements. The

Provisional also supports these elements as actually recited in independent claims

10, 17, and 21.

40. ~~32.~~ The Provisional refers to “MB Training” in Figure 3, and all of the

figures in the Provisional depict an element titled “MB.” (Ex. 1008 at Figures 1- 3).

“MB” is a well-known acronym for a “memory buffer,” which a POSITA,

particularly in view of the Provisional’s description and the location of the “MB”

on the DIMMs in each figure, would have readily understood refers to a “memory

buffer.” A POSITA would have understood that the “MB Training” disclosed in the

Provisional refers to the “MB-DRAM Training” step (sometimes referred to as the

“MB-DRAM Interface Training” step) of LR-DIMM initialization known at the

time of the Provisional, during which the edge connections between the Host and

the DIMMs (the “first edge connections”) are not active.

41. ~~33.~~ MB-DRAM Training would have been well-known to a POSITA at

the time of the Provisional as a necessary step of LR-DIMM initialization. To start,

I understand that Petitioner's expert, Dr. Alpert, also understands that LR-DIMMs were known to a POSITA at the time of the Provisional, including the initialization sequences for LR-DIMMs. (Ex. 2023 at 307:18-20; 309:19-22). I agree that a POSITA would have understood certain steps and requirements of LR- DIMM initialization, as they existed at the time of the Provisional.

42. ~~34.~~ Based on this knowledge, a POSITA would have understood that MB-DRAM Training is a known step of LR-DIMM initialization, in particular one that is necessary to achieve the optimal performance of LR-DIMM systems. In particular, a POSITA would have known that, at the time of the Provisional, in an LR-DIMM system, the Host communicates with the DRAMs via a "memory buffer" (or "MB") that is interposed between the Host and the DRAMs, and which buffers read and write commands and returns between the Host and the DIMMs. A POSITA would have understood that part of the LR-DIMM initialization sequence involves determining the amount of time associated with delays for a read operation from the Host to each of the DRAMs. These delays occur at various points within the Host-MB-DRAM chain, and include: (1) the delay for a command from the Host to the MB, (2) the delay for a command through the MB, (3) the delay for a command from the MB to the DRAM, (4) the latency within the DRAM itself, (5) the return time for a data strobe from the DRAM to the MB, (6) the delay for the data strobe through the MB, and (7) the delay for the data strobe from the MB back to the Host.).

43. ~~35.~~ A POSITA would have understood that Host-MB Training Patent No. ~~9,858,218~~10,474,595

(sometimes referred to as “Host-MB Interface Training”) includes determining the correct total round-trip delay for a read command from the Host to the MB through to the DRAM, and back through the MB to the Host. However, a POSITA would have understood that each individual delay must first be ascertained prior to Host-MB training so that the total round-trip delay may be determined. In an LR-DIMM system, where the MB buffers data signals sent between the Host and the DRAMs, this includes delays from communication between the MB and the DRAMs as well as within the MB itself.

44. ~~36.~~ The MB-DRAM Training performed during LR-DIMM

initialization determines these delays associated with the memory buffer through sequences of training including “Write Leveling” and “Read Enable Training.”

45. ~~37.~~ Memory systems that employed a memory buffer to buffer the data

lines between a Host and memory module components (such as DRAMs) were well-known in the art at the time of the Provisional. For example, Fully Buffered DIMM systems (“FB-DIMMs”) predate the Provisional by many years and employ a “buffer” interposed between a memory controller and the DRAMs which buffers the data lines between the Host and the DIMMs. (~~Exhibit~~Ex. 2016 (Fully Buffered DIMM (FB-DIMM) Design Considerations, dated February 18, 2004) at 4) (“DRAM interface is entirely behind the buffer.”). It was therefore known to a POSITA that memory systems which employed a memory buffer would hand off

training conducted between the memory buffer and the DRAMs to the memory buffer, giving the Host a reduced workload and allowing it to perform other operations with other memory system components. (Ex. 1008 at 22) (“This method allows the MCH to execute independent command while it is waiting for a notification signaling from the memory subsystem controller.”).

46. ~~38.~~A POSITA would also have understood that, during the training sequences which were handed off from the Host to the memory buffer (such as “MB-DRAM Training”), the Host would not be issuing memory read or write operations during training (because the MB to DRAM signal lines were being used instead to conduct training) and would consequently be waiting for the memory buffer to complete that training sequence.

47. ~~39.~~A POSITA would therefore have understood that MB-DRAM Training is critical to implement during LR-DIMM initialization so that the Host can be optimally configured to issue read and write commands to the DIMMs via the MB. I understand that Dr. Alpert agrees with this notion. (Ex. 2023 at 216:16-21) (Write Leveling and Read Enable Training are “critical to implement” for LR-DIMMs). I further note that both the Petitioner and Dr. Alpert have a consistent understanding. The Petition and Dr. Alpert both cite a JEDEC proposal for LR-DIMM initialization titled “MB Initialization Sequence Item 142.35,” dated June 4, 2009 (Ex. 1039) (the “pre-Provisional JEDEC Proposal”), that they contend would be known by a POSITA at the time of the Provisional. (Pet., ~~6-77-8~~6-77-8; Ex. 1003 ¶¶~~46-~~46-

~~47~~48).

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The pre-Provisional JEDEC Proposal (Ex. 1039) bears a publication date of June 4, 2009, and the disclosures in this document are consistent with both the Provisional's description of the "recent JEDEC proposal for L[R]-DIMM" and initialization and training sequences (Ex. 1008 at ~~22-24~~, ~~Figure 3~~22), and my description immediately above of a POSITA's knowledge at the time of the Provisional.

48. ~~40~~ Both the Petitioner and Dr. Alpert also appear to contend that the JEDEC Proposal (Ex. 1015) was "known" to a POSITA. (Pet., ~~6-77-8~~; Ex. 1003 ¶¶ ~~46-47~~48). Although I note that the JEDEC Proposal (Ex. 1015) indicates a date several months (November 2009) after the Provisional, its disclosures are nonetheless generally consistent with my description immediately above of the knowledge of a POSITA at the time of the Provisional, for example, and particularly, that certain training sequences during initialization would be handed off from the Host to the memory buffer during training (i.e. "MB-DRAM Training"). I do note, however, that signal notification relating to training and initialization from the MB to the host that is described in the JEDEC Proposal (Ex. 1015) is *not* described in the pre-Provisional JEDEC Proposal (Ex. 1039), and such signaling appears to have been first described in the Provisional. (Ex. 1008 at 23) ("Certain embodiments described herein provide a method of establishing a handshake mechanism based on the notification signaling. This mechanism can be implemented by adding a

new interface (notifying) signal between the MCH and the memory subsystem controller or by adding an additional functionality to an existing, non-timing critical, signal without altering the memory subsystem hardware.”).

49. ~~41.~~A POSITA would have understood that the Provisional’s reference to “MB Training” referred to MB-DRAM Training known to a POSITA at the time (as described above). The Provisional describes methods of “handshaking” between the MCH [the “Host”] and a memory subsystem [i.e. the “DIMM”], particularly in an LR-DIMM system, which is advantageous because the Host “hand[s] over one or more parts of the initialization operation sequences to the memory subsystem controller [the “memory buffer” or “MB”],” rather performing them directly. (Ex. 1008 at 22). The Provisional proposes the use of a “notification signal” from the memory subsystem controller back to the Host when the memory subsystem controller completes that training in order to allow the Host to execute independent commands instead of idling for some period of time while the MB performs training. (Ex. 1008 at 22) (“In the notifying method, the memory subsystem controller sends a signal to the MCH when it completes the required or requested operation. This method allows the MCH to execute independent command while it is waiting for a notification signaling for the memory subsystem controller.”). Indeed, idling, or “waiting” is what is described in the pre-Provisional JEDEC Proposal (Ex. 1039 at 7-10), which, as described above, a POSITA would have understood as the then-known implementation in

LR-DIMMs at the time of the Provisional.

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50. ~~42.~~ The Provisional explains that the disclosed “MB Training” occurs during “initialization.” The Provisional discloses “[s]haring a pin between the Error-out and Notifying signal.” (Ex. 1008 at Figure 3). During “initialization,” the shared pin functions as a notifying signal, and “is low impedance while the memory subsystem controller [is] executing each section of the initialization step.” (Ex. 1008 at 23). As each step is completed, the notifying signal pin is driven to the high impedance state and this causes the signal to be pulled high by the MCH [Host], thus resulting in the “notifying signal” that the initialization sequence is complete. (Ex. 1008 at 23). Conversely, the pin is “[h]igh during normal operation unless a parity error occurs,” resulting in an “error-out” signal. (Ex. 1008 at Figure 3). This is depicted and summarized in Figure 3 of the Provisional:

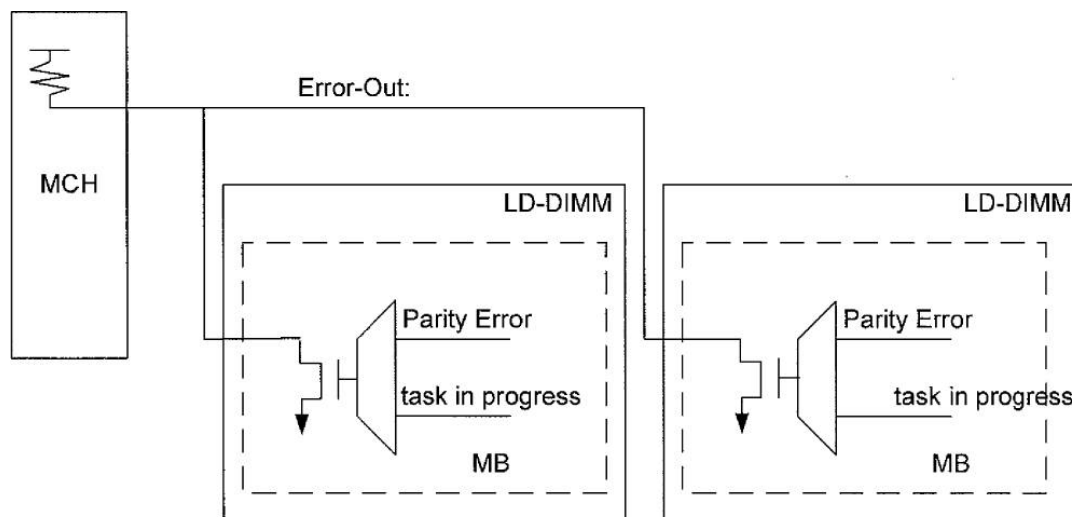


Figure 3: Sharing a pin between the Error-out and Notifying signal

Error-Out pin: Low during MB training (high signal indicates that training is done)
High during normal operation unless a parity error occurs

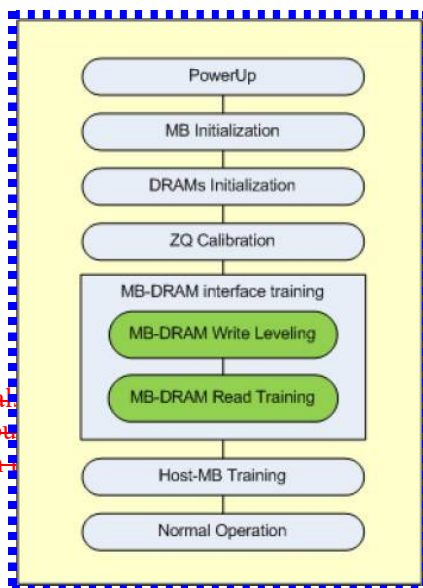
51. ~~43.~~A POSITA would therefore have understood the Provisional Patent No. ~~9,858,218~~10,474,595 teach that “MB training,” which is performed during the initialization discussed immediately above, is not performed at the same time as “normal operation” (which occurs after “MB training” is “done”). A POSITA would thus have also understood that, during “MB training,” the data lines between the MCH and DIMM are not available for normal read and write operations, because the data lines between the MB and the DRAMs are being used to conduct the MB-DRAM ~~training~~Training. Additionally, the logic on the shared pin (the “high” or “low” signal) conveys different information depending on whether it is providing a “notifying signal” (during “MB training”) or an “error-out” signal (during “normal operation”). (Ex. 1008 at 23, Figure 3). Instead, a POSITA would have understood that “MB training” must occur during the “initialization operation sequences” because the shared pin is only providing the “notifying signal” during “MB training” and is otherwise providing the error-out signal in “normal operation.” (Ex. 1008 at 23, Figure 3). This makes perfect sense—MB-DRAM Training is performed during LR-DIMM initialization to ensure the optimization of signal capture prior to any normal memory read or write operations that occur in “normal operation.” A POSITA would have understood that the LR-DIMMs would not run at full speed during normal operations without having previously completed MB-DRAM Training.

52. ~~44.~~Because the Provisional addresses “MB training” that occurs during

“initialization operation sequences” that the Host hands off to the MB, a POSITA No. 9,858,218 10,474,595 would have understood that the Provisional’s reference to “MB training” referred to the MB-DRAM Training of LR-DIMMs known at that time. As I explained above, a POSITA would have understood that LR-DIMM initialization involved handing off certain training sequences to the MB, including “MB-DRAM Training.” This is confirmed by Exhibit 1039 (the JEDEC document dated before the Provisional), which explains that MB-DRAM Training is the *only* portion of the LR-DIMM initialization sequences that is handed-off to the MB and not conducted directly by the Host. (Ex. 1039 at 7 (“Host issues [a] CWord write to start MB-DRAM interface training and wait[s]. MB does write leveling training to DRAM. MB does RxEn [i.e. read] training to DRAM. MB return[s] to idle state and ready to start normal operation.”); Ex. 1039 at 10 (“After enabling the IMB-DRAM training by setting F0RC12 to 010b, the Host must wait a predetermined number of cycles before moving to next step.”)). My opinion of POSITA’s understanding at the time of the Provisional is further supported by Exhibit 1015, which, although dated after the Provisional, also confirms that MB-DRAM training is handed off to the MB (as described above, a POSITA would have understood this at the time of the Provisional). (Ex. 1015 at 8 (“After all the DRAMs are fully operational, the host triggers the DRAM interface training by setting the control bit DA4 in F0RC12. Once enabled, the MB assumes autonomous control of the Command/Address, Control and Data/Strobe signals to the DRAMs, without any

further assistance from the host.”), Ex. 1015 at 8 (“The MB performs ‘Write Leveling’ to the DRAMs to ensure successful writes, and ‘Read Enable Training’ to ensure it can capture read data from the DRAMs correctly.”)).

53. ~~45.~~ Finally, a POSITA would have understood that no reads or writes are performed over the Host edge connections during the “MB training” (e.g., MB-DRAM Training) disclosed in the Provisional. As I explained above, POSITA would have understood that memory read and write operations are not issued by the Host during “MB-DRAM Training” because the Host is waiting for the MB to complete that training.¹ This understanding is supported by Exhibit 1039 (the JEDEC document dated before the Provisional), which explains that, during MB-DRAM Training, the Host is in idle or standby mode, not in “normal operation,” until the MB has completed the MB-DRAM training. (Ex. 1039 at 7) (“Host writes CWord, F0RC12, to start the IMB-DRAM training and wait. MB does write leveling to DRAM. MB does RxEn training to DRAM. MB return to idle state and ready to start normal operation.”)).



¹ ~~A POSITA would not be handing off control to the memory because the Host would know when~~

~~training (such as Host-MB Training) did not require the Host, and thus the Host would not have to wait until completed.~~

(Ex. 1039 at 2). My understanding of a POSITA's knowledge ~~at the time of the~~9:858, 31810474.595

Provisional is further supported by Exhibit 1015, which, again, although dated

¹ A POSITA would also understand that other types of training (such as Host-MB Training) did not require handing off control to the memory buffer and were instead controlled by the Host, and thus the Host would not have to wait because the Host would know when the training it was controlling was completed.

after the Provisional, is consistent in some aspects with what a POSITA would have understood at the time of the Provisional. In particular, Exhibit 1015 describes that no DRAM commands or control word writes can be issued to the MB until the MB-DRAM Interface training is complete, which, as described above, a POSITA would have understood at the time of the Provisional. (Ex. 1015 at 8) (“No DRAM commands or control word writes ... can be issued to the MB until the MB-DRAM Interface training is complete.”). Because the Host cannot issue reads or writes during MB-DRAM training, a POSITA would have understood that the Host edge connections are not active during “MB training.”

54. ~~46.~~ Thus, in my opinion, the Provisional reasonably conveys to a POSITA “train[ing] with one or more training sequences while the first edge connections are not active.”

C. ~~2.~~ The ~~Provisional~~Priority Application Supports ~~the~~
~~‘218~~The ‘595 Patent Claims Reciting ~~Performance of that~~
 “One or More ~~Memory Read or Write Operations Not~~
~~Associated With the One or More Training Sequences~~Pins

are Not Active”

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55. ~~47.~~In my opinion, the Petition incorrectly asserts that ~~“configured to perform the claim elements requiring “pins not active,” such as “the second edge connections include one or more pins that are not active while the memory read or write operations not associated with the one or more training sequences,” as recited in claim 1 of the ‘218 Patent, is not sufficiently disclosed in the Provisional. (Pet. at 8-9). module is in the second mode,” are not supported by the Priority Application. (Pet. at 9-10). The Provisional does describe these claim elements.~~

56. ~~48.~~~~Contrary to~~In my opinion, Petitioner’s ~~contention,~~suggestion that a POSITA would not understand an “edge,” “edge connection[s],” a “mode” and “active” to not be supported by the Provisional is entirely untenable and gives no consideration to disclose the concepts fundamental understandings of what a “read operation,” a “write operation” (or

just “write”), “data signals” (or just “data”), “first edge connections” (or just “edge”), “address signals” (or just “address”), “command signals,” and “second edge connections.”POSITA would have known at the time of the Provisional. (Pet. at 810).~~A POSITA would understand that each~~ Each of these ~~concepts/functions~~terms is a fundamental component or function of memory devices ~~generally (including but not limited to LR-DIMMs), and POSITA would thus understand the Provisional to include these concepts~~have understood them to be disclosed at least ~~because by virtue~~ of the Provisional’s ~~disclosure of a memory~~

system including an MCH [Host] and DIMMs comprising a MB [memory controller] and DRAMs, as well as its reference to “the “recent JEDEC proposal in JEDEC for L[R]-DIMM.” (Ex. 1008 at 22-24, Figure 3). A POSITA would also have understood that and the purpose components of LR-DIMMs is to perform a “memory read controller hub” and write operations” that are not associated with “training sequences.” This is typically referred to as “normal operation.” By contrast, a POSITA would also have “DRAM[s],” which were also present in many other well-understood that LR-DIMM memory systems perform “initialization” during which the system undergoes “training” to prepare it for the normal memory reads and writes conducted during “normal operation.” (Ex. 1039 at 1-9; Ex. 1015 at 1-9). A POSITA would have understood that “memory read or write operations” are conducted, at a minimum, during “normal operation” of LR-DIMMs.

49. A POSITA would have understood that the Provisional plainly discloses “normal operation.” The Provisional discloses “[s]haring a pin between the Error-out and Notifying signal,” because the “error-out” pin is not monitored during initialization. (Ex. 1008 at 22-23, Figure 3). Specifically, the pin is “[l]ow during MB training” and “a “high signal indicates that training is done.” (Ex. 1008 at Figure 3). Conversely, the pin is “[h]igh during normal operation unless a parity error occurs.” (Ex. 1008 at Figure 3). The Provisional discloses both an “initialization” sequence that includes “MB training,” and also discloses “normal operation.” (Ex. 1008 at 24 (“Since the notification of completion of the required or

~~requested task from the memory subsystem controller would generate an error out signal to the system during the initialization period as an error occurrence generates an interrupt to the system during the normal operation, the error out signal in the current memory subsystem can be used to support the notifying function.”); Ex. 1008 at Figure 3 (output of the shared pin is “high during normal operation unless a parity error occurs”)).~~

~~50. A POSITA would therefore have understood that “MB training” the only training disclosed in the Provisional would not occur during “normal operation,” because the data lines otherwise used for memory read or write operations are occupied by the MB training. Additionally, the logic on the shared pin conveys different information depending on whether training or normal operation is occurring. A POSITA would thus have recognized that when the memory subsystem is being initialized, it is *not* ready for normal memory operation (normal read and write operations), and thus is *not* accessed by the MCH for read or write operations as it is during “normal operation.”~~

~~51. In view of these disclosures, a~~ 1008 at 22, 24). Memory devices long-predating the Provisional communicated over “edge connections” and operated in “modes,” and the edge connections on those memory devices would be “active” or “not active” depending, among other things, on the “mode” in which the memory device was operation. As discussed above, the Provisional describes these different “modes.”

57. I also disagree with the Petition's assertion that "the collection of pins

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[for address and command] on an edge connection are not active during certain

modes" is not supported by the Provisional. (Pet. at 10). As I explained above in

Section VII.B., a POSITA would understand that "memory read or write

operations" (or "normal memory read or write operations") occur only at certain

times during the "normal mode" (or, alternatively, *do not* occur during the

"initialization" mode). A POSITA would have understood known that, when a

memory module is performing training, it is *not* accessed by the MCH for normal the

pins associated with a particular DRAM would only be "active" when performing

these "memory read or write operations. Thus" Therefore, in my opinion, a POSITA

would have understood understand that the Provisional discloses the performance of

normal read or write operations that are not associated with any training—indeed,

this is the purpose of a memory system in its normal operation.

52. Petitioner and Dr. Alpert corroborate that all the parts of this claim

element would have been known to a POSITA when reading the Provisional.

Petitioner's only argument is that training "could" occur during normal operation.

(Pet. at 9) ("In fact, as Dr. Alpert explains, a Skilled Artisan would understand

training *could* occur during normal operation."). Dr. Alpert testified similarly. (Ex.

2002 at 31:10-32:4) (arguing that it is not the case that training can never be done in

normal operation). But the Provisional does not describe any training occurring

during normal operation, and, as discussed above, the training described in the

~~Provisional does not occur during “normal operation.” Petitioner and Dr. Alpert, U.S. Patent No. 9,858,218 10,474,595 seem to tacitly concede that a POSITA would *expect* that training *does not* occur during normal operation. (Pet. at 9; Ex. 2002 at 31:10-32:4). And, as I both explained above in Section VII.1 and as Dr. Alpert agrees, the Provisional *only* discloses training that occurs during initialization (i.e. MB-DRAM Training). (Ex. 2023 at 124:11-13).~~

~~53. This serves as an explicit message to a POSITA that the Provisional discloses normal read or write operations that are not associated with training that “one or more pins” would *not* be “active” when the memory module is in the “second mode”—i.e. when in the “initialization” mode.~~

**D. ~~3.~~ The ~~Provisional~~Priority Application Supports the
~~‘218’~~595 Patent Claims Reciting “One or More” Training
“Sequences”**

58. ~~54.~~ In my opinion, the Petition incorrectly asserts that “one or more” training “sequences,” as recited in each independent claim of the ~~‘218’~~595 Patent, is not sufficiently disclosed in the Provisional. (Pet. at ~~9-10~~8-9). Petitioner’s and Dr. Alpert’s argument as to why “one or more training sequences” is not disclosed is that the Provisional “only discloses ‘MB Training.’” (Pet. at ~~9-10~~8-9). In my opinion, Petitioner’s and Dr. Alpert’s arguments are inconsistent with and do not give credit to what a POSITA would have known, and thus, would have understood the Provisional to describe.

59. In my opinion, the Petition incorrectly asserts that “one or more training sequences,” as recited in each independent claim of the ‘595 Patent, is not sufficiently disclosed in the Provisional. (Pet. at 8-9). Petitioner’s and Dr. Alpert’s argument as to why “one or more training sequences” is not disclosed is that the Provisional “only discloses ‘MB Training.’” (Pet. at 8-9). In my opinion, Petitioner’s and Dr. Alpert’s arguments are inconsistent with and do not give credit to what a POSITA would have known, and thus, would have understood the Provisional to describe.

60. ~~55.~~ As I explained above in Section VII.~~4B.~~, a POSITA would have understood that the “MB training” disclosed in the Provisional is “MB-DRAM Training,” a process well-known to a POSITA in the LR-DIMM initialization sequences. And as I further explained above, in LR-DIMMs, MB-DRAM Training includes two distinct training steps, (1) Write Leveling and (2) Read Enable Training, which are performed one after the other. Therefore, a POSITA would have understood that the “MB training” disclosed in the Provisional referred to at least two “training sequences” performed one after the other. (Ex. 1039 at 7) (“MB-DRAM Interface Training: MB does write leveling to DRAM. MB does RxEn [read enable] training to DRAM”).

61. ~~56.~~ Dr. Alpert appears to agree. I understand he testified that “[d]uring MB-DRAM training, the memory buffer is doing a certain set of training sequences with the DRAMs,” which includes “Write Leveling and Read

Enable Training that are done in sequence.” (Ex. 2023 at 56:17-23; ~~U.S. Patent No. 10,236,111~~
~~9,858,218~~10,474,595
61:22- 62:1; 67:7-10; 70:15-22). Dr. Alpert also previously testified that a

POSITA would have understood that the Provisional discloses “multiple different types of training.” (Ex. 2002 at 33:17-20). And I agree that this confirms that a POSITA

would have understood that the Provisional discloses “one or more” training “sequences” in the context of “MB training.”

62. ~~57.~~ Additionally and separately, Dr. Alpert explains that the Provisional discloses “MB training” in the context of existing proposals relating to ~~the “training of registers/buffers~~the interfaces of a Memory Buffer used in the then[-]current DDR3 LRDIMMs under development/standardization.” (Ex. 1003 at ¶ ~~46~~47). In that same context, the Provisional also discloses initialization sequences when describing that newly developed LR-DIMM memory modules require “the MCH to hand over *one or more parts of the initialization operation sequences* to the memory subsystem controller” as an issue to be addressed by the invention. (Ex. 1008 at 22).

63. ~~58.~~ Furthermore, as I explain above, the training disclosed in the Provisional does not occur during “normal operation” because the “High” or “Low” logic of the shared pin conveys different information during “MB training” than it does during “normal operation.” (Ex. 1008 at Figure 3) (“Error-Out pin: Low during MB training (high signal indicates that training is done). High during normal

operation unless a parity error occurs.”). The Provisional specifically states that No. 9,858,218 10,474,595 “[t]he output of the notifying signal is low impedance while the memory subsystem controller execut[es] *each section* of the initialization step.” (Ex. 1008 at 23). As described above, a POSITA would understand that “MB training” occurs during initialization. This conforms with a POSITA’s understanding that, during MB training, the data lines used for memory read and write operations are in use performing the training functions, and are therefore not available for performing any memory read and write operations ~~sent~~send from the Host/MCH to the MB. A POSITA would therefore have understood that the disclosed MB training occurs during the “initialization operation sequences” while the “notifying signal is low impedance.”

64. ~~59.~~ The Provisional explicitly states that the low impedance state can be asserted for different sections of the overall initialization step. (Ex. 1008 at 23) (“Figure 3 shows the operation of the notifying signal in accordance with an example embodiment. The output of the notifying signal is *low impedance* while the memory subsystem controller is executing *each section of the initialization step*, thus the notifying signal is pulled low by the memory subsystem controller.”). Collectively, multiple training operations may be performed, thereby disclosing to a POSITA that “one or more” training “sequences” may occur.

65. ~~60.~~ Thus, in my opinion, the Provisional reasonably conveys operation sequences (e.g., sequences of operations) that would occur during the initialization

of a memory subsystem (e.g., “initialization operation sequences”). ~~U.S. Patent No. 9,858,218~~U.S. Patent No. 10,474,595 would have understood that the Provisional’s reference to MB training referred to MB-DRAM Training, which includes sequences of Write Leveling and Read Enable Training, each of which occurs during initialization and is necessary for the performance-optimized functioning of LR-DIMMs. (Ex. 1039 at 2, 7-10). Therefore, in my opinion, the Provisional discloses one or more training sequences.

E. The Provisional Supports ’595 Patent Claims Reciting “One or More N-Bit-Wide Data Signals”

66. The Petition incorrectly asserts that the Provisional does not disclose “dynamic random access memory elements” (“DRAMs”) which “communicate one or more N-bit-wide data signals...where N is at least 32,” as recited in claim 21 of the ’595 Patent. (Pet. at 9).

67. DRAMs that communicated via data signals of bit-width 32 or more were exceedingly well-known at the time of the Provisional. For instance, DDR2 SDRAMs that communicated 32-bit signals were known to a POSITA at the time of the Provisional. (See Ex. 2021 (“8Mx32 DDR2 SDRAMs feature a 32 bit bus”), Ex. 2029 at 1 (“Configuration: 4 Meg x 32 (1 Meg x 32 x 4 banks), Marking: 4M32”)). The Petition further refers to LR-DIMM configurations comprising different “DRAM density,” “speed,” and “configuration” (Ex. 1008 at 23), confirming to POSITA the Provisional was referring generally to the DRAM designs known at the

time, and not a particular design.

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68. Dr. Alpert also agreed that the Provisional discloses “MB training” in the context of existing proposals relating to the “training of registers/buffers used in the then[-]current DDR3 LRDIMMs under development/standardization,” which Dr. Alpert explained included “a type of register/buffer” that “buffered both address and data signals.” (Ex. 1003 at ¶ 47). The then-current DDR3 LRDIMMs, at least, supported 64-bit I/O configurations for the communication of data signals, and a POSITA would have known this. (Ex. 2021 & Ex. 2029).

69. Thus, in my opinion, a POSITA would have understood the Provisional to disclose DRAMs which “communicate one or more N-bit-wide data signals ... where N is at least 32.”

F. ~~B.~~ General Overview of the ‘~~218~~595’ Patent

70. ~~61.~~ The ‘~~218~~595’ Patent has a priority date of June 12, 2009, and relates generally to the operation of memory modules. (Ex. 1001). Specifically, the ‘~~218~~595’ Patent discloses a memory module that can function in two different modes communicating with a host system. (Ex. 1001 at Abstract).

71. ~~62.~~ As described in the ‘~~218~~595’ Patent, memory modules operate in two distinct modes of operation: “a “first mode” and a “second mode.” (Ex. 1001 at

~~1:42-52, 1:63-2:8, 2:9-14, 4:24-28, 5:61-64, 7:58-65, 9:20-24, 11:47-51, 12:13-17, 12:44-48). The first mode of operation is a mode in which the memory module~~

~~executes training sequences during initialization, during which the memory module~~

~~may transmit to the memory controller a notification signal associated with the~~ U.S. Patent No.

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~~training sequence, but during which the memory module is not accessed by the host~~

~~for normal memory read or write operations. (Ex. 1001 at 1:45-49, 2:17-24, 4:24-31,~~

~~5:61-6:10, 6:15-30, 7:3-18, 9:20-27, 11:46-54, 11:55-63). The second~~ 1:47-57,

2:2-12, 2:14-19, 4:29-33, 5:66-6:2, 7:63-8:3, 9:24-28, 11:50-54, 12:16-20,

12:47-51). The first mode of operation is a normal operational mode, in which the

memory module performs normal read and write operations as well as pre-charge,

refresh, and similar other standard operations receiving/sending system data to be

retrieved/stored by the host system, during which the memory devices are generally

~~accessible by the host system. (Ex. 1001 at 1:49-58, 2:2-6, 6:41-48,~~

~~12:4-8).~~

generally accessible by the host system. (Ex. 1001 at 1:54-61, 2:7-11, 6:45-53,

12:7-11). The second mode of operation is a mode in which the memory module

executes training sequences during initialization, during which the memory module

may transmit to the memory controller a notification signal associated with the

training sequence, but during which the memory module is not accessed by the host

for normal memory read or write operations. (Ex. 1001 at 1:50-54, 2:22-29, 4:34-42,

5:66-6:14, 6:19-34, 7:7-23, 9:24-31, 11:50-57, 11:58-66).

72. ~~63.~~ The memory module includes a notification circuit which outputs a notification signal associated with the training sequences to the host system. (Ex.

1001 at ~~1:45-49, 1:66-2:2, 2:20-24, 4:31-37, 7:2-14~~1:50-54, 2:5-7, 2:25-29,

4:36-42, 7:7-19).

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VIII. OVERVIEW OF THE REFERENCES

A. Hazelzet

73. ~~64.~~ U.S. Patent App. Pub. No. 2008/0098277 to Hazelzet (“Hazelzet”) is a U.S. Patent Publication that was filed on October 23, 2006. Hazelzet discloses a memory module including error correction code (ECC) logic “to identify and correct single bit errors on the command or address bus” (Ex. 1014 at [0008]) and a system incorporating many such memory modules. (Ex. 1014 at [0036]). The invention disclosed in Hazelzet further includes an error reporting mode during which the system can interrogate the module regarding its error status. (Ex. 1014 at [0009]). The invention implements these features in a register “having error correction code (ECC), parity checking, a multi-byte fault reporting register, read via an independent bus, and real time error lines for both correctable errors and uncorrectable error conditions.” (Ex. 1014 at [0016]). Thus, Hazelzet's invention discloses a hybrid device utilizing error detection, error correction, and parity.

74. ~~65.~~ Hazelzet does not include memory buffers that buffer the data lines. (Ex. 1014 at [0038], [0042]–[0044]). This is a modification that Petitioner concedes would be required to combine Hazelzet with any teachings from JEDEC and Buchmann. (Pet. at ~~39~~35). Hazelzet also does not disclose training or any motivation to add training, let alone the specific training disclosed in JEDEC and Buchmann. Although Hazelzet discloses “initialization of the memory subsystem”

(Ex. 1014 at [0123]–[0125]), it does not discuss or mention training (U.S. Patent No. 9,858,218/10,474,595 initialization mode or a normal mode of operation). Hazelzet presents a solution to a problem not addressed by JEDEC or Buchman, through a memory system architecture that is incompatible with JEDEC and Buchmann.

B. JEDEC

75. ~~66.~~ I understand that the JEDEC reference which Petitioner relies on (Ex. 1015) is not prior art to the ‘218595’ Patent because it bears a date (November 2009) after the priority date of the ‘218595’ Patent. The ‘218595’ Patent claims priority to the Provisional which has a priority date of June 12, 2009. (Ex. 1001-~~at~~₂ Cover).

Nonetheless, JEDEC discloses Write Leveling and Read Enable Training. (Ex. 1015 at 8). JEDEC states that the MB performs “Write Leveling” to the DRAMs to ensure successful writes, and “Read Enable Training” to ensure it can capture read data from the DRAMs correctly, as part of the DRAM interface training. (Ex. 1015 at 8). Both Write Leveling and Read Enable Training are training operations performed between the memory buffer (MB) and the DRAMs. (Ex. 1015 at 8).

76. ~~67.~~ JEDEC discloses initialization procedures for a system that already includes memory buffers that buffer data lines. (Ex. 1015 at 3). JEDEC does not describe the implementation of such a memory buffer or that including such a memory buffer that buffers data lines would offer any benefits over memory buffers that do not buffer data lines.

C. Buchmann

U.S. Patent No.

~~9,858,218~~10,474,595

77. ~~68.~~ U.S. Patent No. 8,139,430 to Buchmann (“Buchmann”) discloses a power-on initialization test for a cascade interconnect system. Buchmann discloses a memory buffer that includes a bus interface to links in a high-speed channel for communicating with a memory controller via a direct connection or via a cascade interconnection and another memory buffer. (Ex. 1016 at 1:39-43). The interface is operable in a static bit communication (SBC) mode and a high-speed mode. (Ex. 1016 at 1:43-44). The memory buffer includes logic for executing a power-on and initialization training sequence initiated by the memory controller. (Ex. 1016 at 1:44-48). The sequence includes initializing the links to the high-speed channel. (Ex. 1016 at 1:48-50). Buchmann teaches that its training commands are 6-bit SBC commands that are sent via a bus. (Ex. 1016 at 5:66-11:32, 15:46-58, 16:16- 26, Figure 11 (line with /6 between elements 1142 and 1144). Buchmann’s 6-bit SBC commands cannot be sent over an open drain because an open drain (like a UE line in Buchman and Hazelzet) is only a one bit signal. Thus, Buchmann does not disclose sending a notification regarding training via an open drain.

IX. ANALYSIS OF THE CITED REFERENCES

78. ~~69.~~ I understand the Petition presents two combinations to challenge all independent claims of the ‘~~218~~595 Patent: (1) Hazelzet with JEDEC (“Ground 1”), and

(2) Hazelzet with Buchmann (“Ground 2”).² Ground 3, Hazelzet, JEDEC Patent No. ~~9,858,218~~10,474,595 Buchmann, and Kim (“Ground 3”) only challenges dependent claims.³

Ground	References	Basis	Challenged Claims
1	Hazelzet and JEDEC	35 U.S.C. § 103	~~1-22~~ <u>1-24</u>
2	Hazelzet and Buchmann	35 U.S.C. § 103	~~1-22~~ <u>1-24</u>
3	Hazelzet, JEDEC <i>or</i> Buchmann, and Kim	35 U.S.C. § 103	~~3-6, 10-12, 17-20~~ <u>3-7, 12-14, 20, 22 and 23</u>

At this time, I respond to the Petition’s challenges to the independent claims of the ‘~~218~~595 Patent (Grounds 1 and 2) which also applies to all dependent claims. Also, because I do not believe the combination in Grounds 1 and 2 is proper, the Ground 3 is also improper because it relies on the faulty rationale in Grounds 1 and 2.

79. ~~70.~~In ~~Both~~both Ground 1 and Ground 2, the Petition first asserts that in each alleged combination, “*Hazelzet’s memory modules would be modified to add the functionality of buffering the data signals similar to that in the DDR3 LRDIMM of the time and an initialization mode* (‘first mode/operation’) into which each module could be switched and which includes training sequences whose completion is reported by the memory buffer using a status signal output over an open drain output (i.e., UE 121) of Hazelzet.” (Pet. at ~~32~~30). Thus, Petitioner’s Grounds require—*before* training could even be implemented in Hazelzet—that a POSITA

² The independent claims of the ‘~~218~~595 Patent are: claims 1, 91017, and ~~15~~21.

³ I understand that if Grounds 1 and 2 fail, because the Petition does not demonstrate a likelihood of success

would have first changed Hazelzet’s memory modules and architecture to add a new memory buffer that buffers the data signals (because Hazelzet’s memory modules only buffer the address and control signals), *and* then also add a new initialization mode “into which each [new] module could be switched.” As discussed below, Petitioner’s Grounds require this modification to Hazelzet’s memory module architecture because Hazelzet’s memory modules—as actually described in Hazelzet—are incompatible with JEDEC’s and Buchmann’s alleged training in an initialization mode. Petitioner’s expert, Dr. Alpert, also admitted this during deposition. (Ex. 2002 at 68:19-79:24, 81:18-83:5; Ex. 2023, 201:22- 203:19).

80. ~~71.~~ Then, after already first changing Hazelzet’s system architecture, in Ground 1 the Petition alleges that Hazelzet could be further modified, combined with JEDEC, to add JEDEC’s specific training in that new initialization mode and to also send signals associated with that new training in the new initialization mode implemented in the new memory modules, *but* using via Hazelzet’s *premodified* open drain. (Pet. at ~~32-42~~30-40). More specifically, the Petition alleges that the combination of Hazelzet and JEDEC “include a ‘*first mode*’ in which training is carried out.” (Pet. at ~~48-49~~46-47). The Petition relies on JEDEC’s Write Leveling and Read Enable Training function to satisfy the “training sequences” limitation of Claim 1. (Pet. at ~~49~~50-51). The Petition alleges that JEDEC’s ERROUT# signal is “*associated with the one or more training sequences*” and could be transmitted via

as to the independent claims, then the Petition’s Ground 3 would also fail for the same reasons.

an open drain output. (Pet. at ~~54-55~~52-53).

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81. ~~72.~~Alternatively, again after already first changing Hazelzet’s system architecture, in Ground 2 the Petition asserts that Hazelzet could be further modified, combined with Buchmann, to add Buchmann’s specific training in that new initialization mode and to also send signals associated with that new training in the new initialization mode implemented in the new memory modules, *but* again also using via Hazelzet’s *premodified* open drain. (Pet. at ~~32-42~~30-40). Specifically, the Petition alleges that the combination of Hazelzet and Buchman “include a ‘*first mode*’ in which training is carried out.” (Pet. at ~~48-49~~46-47). The Petition relies on Buchmann’s TS0 and TS3 function to satisfy the “training sequences” limitation of Claim 1. (Pet. at 49). The Petition alleges that Buchmann’s TS0 done, TS3 ack, or TS3 done signals are “*associated with the one or more training sequences*” and could be transmitted via an open drain output. (Pet. at ~~54-55~~52-53).

82. ~~73.~~Accordingly, Petitioner’s Grounds need to demonstrate, at a minimum, that a POSITA would have found it obvious to (1) redesign Hazelzet’s memory module to add a new memory buffer that buffers data signals in addition to address and control signals, (2) then add the kind of alleged training in JEDEC or Buchmann to Hazelzet in an entirely new mode during initialization that is separate from Hazelzet’s normal mode of operation, and (3) then utilize a single open drain output—specifically Hazelzet’s UE line—to communicate parity errors and information associated with the new training. As discussed below, the Petition

follows an illogical sequence of the steps above, each building upon the last, not turning Hazelzet's actual memory architecture into a completely different system from what Hazelzet actually discloses and teaches a POSITA.

83. ~~74.~~ Petitioner relies on each modification to Hazelzet above to build upon the previous modification to transform Hazelzet into something new. As explained below, in my opinion Petitioner's Grounds fail because there is (1) no motivation to redesign Hazelzet's memory module to add a memory buffer that buffers data signals in addition to address and control signals, (2) no motivation to add the kind of alleged training in JEDEC or Buchmann to Hazelzet in an entirely new mode during initialization that is separate from Hazelzet's normal mode of operation, and (3) no motivation to combine Hazelzet with JEDEC or Buchmann such that Hazelzet is reconstructed to output signals related to training sequences over its UE line while in a training mode during initialization.

84. ~~75.~~ Moreover, POSITA could have added training to Hazelzet without adding a memory buffer that buffered the data lines. Specifically, even if POSITA would have added training to Hazelzet, Hazelzet's Memory Controller (reference number 19) could already perform and control that training, which Dr. Alpert appears to agree. (Ex. 2023 at 291:12–292:12) (Q. So, if a person of ordinary skill in the art in 2009 were to implement write level training and 'Read Enable Training' to the architecture in Figure 2, the memory control or processor would implement that

training; is that correct? A. Yes.)

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85. ~~76.~~ Hazelzet's ECC/Parity Register would not need to be modified to

buffer data signals in addition to address and control signals, and thus, no

notification signal from a memory buffer or memory controller or ECC/Parity

Register to the MCH or Memory Controller (on an open drain line or otherwise)

would be required to implement that training, another point in which Dr. Alpert

appears to agree:

12 Q So just kind of wrapping up what we were just
13 talking about in terms of the MB-DRAM training and
14 Host-MB training, if the memory system does not have a
15 memory buffer that buffers the data signals, then there 16
17 doesn't need to be a signal from the memory buffer to
18 the host to tell the host that the memory buffer has
19 done its training, correct?
20 THE WITNESS: I can't think of a reason why
21 you'd need a -- a signal from the memory buffer back to
22 the host to indicate that training is complete if the
23 data were not buffered.

(Ex. 2023, ~~82:12-23~~82:12-23). Hazelzet's Memory Controller, because it would
control that training, would know when that training was complete.

86. ~~77.~~ In my opinion, Petitioner's combinations are predicated on

adding training, but adding training does not require the additional modifications

to Hazelzet that Petitioner contends would then satisfy the claim limitations.

Thus, there is no motivation to make Petitioner's modifications to Hazelzet.

**A. Hazelzet, JEDEC, and Buchmann Provide No Motivation to
POSITA to Redesign Hazelzet's Memory Module to Buffer
the Data Signals**

87. ~~78.~~ Each Ground requires redesigning Hazelzet's memory. In Patent No.

~~9,858,218~~ 10,474,595

add the functionality of buffering data signals. (Pet. at ~~3230~~3230). However, in my

opinion, neither Hazelzet, JEDEC, nor Buchmann provide any motivation for

POSITA to make that modification.

1. Petitioner Concedes that POSITA Would Have Had to First Redesign Hazelzet’s Memory Buffer to Buffer Data Signals

88. ~~79.~~ The Petition's Grounds require—*before* JEDEC's or Buchmann's

training could even be implemented in Hazelzet—that a POSITA would have first redesigned Hazelzet’s memory modules and system architecture to add a new memory buffer that buffers the data signals. The Petition contends at the very outset that, with respect to “each” combination, “Hazelzet’s memory modules *would be modified to add the functionality of buffering the data signals* similar to that in the DDR3 LRDIMM of the time.” (Pet. at [3230](#), [3936](#); Ex. 2019 at 49). Hazelzet’s memory modules—as actually disclosed in Hazelzet—are incompatible with JEDEC’s and Buchmann’s alleged training in an initialization mode because in Hazelzet there is not a buffer or ECC/Parity register on the data lines between the memory controller and the memory devices (SDRAMs). Dr. Alpert appears to agree with me that Hazelzet does not have a memory buffer that buffers data lines. (Ex. 2023 at 210:15-18).

89. ~~80.~~In both JEDEC and Buchmann, the alleged training is implemented

in, and carried out by, the memory module over data signal lines between the module

controller (e.g., a buffer on the memory module) and the memory device Patent No. ~~9,858,218~~10,474,595 DRAMs). For example, as argued in the Petition, “JEDEC disclosed an initialization

mode including MB-DRAM Training that entailed at least two training sequences:

Write Leveling Training and Read Enable Training, both *between the Memory*

Buffer and the DRAMs of the module.” (Pet. at ~~29~~27) (citing

Ex. 1015 at 8 (§6.7)). In JEDEC, “during training of the LR-DIMM, ‘[t]he MB

performs ‘Write Leveling’ to the DRAMs to ensure successful *writes*, and ‘Read

Enable Training’ to ensure it can capture *read data* from the DRAMs correctly, as

part of the DRAM interface training,’ and discloses that ‘MB DRAM interface

training must be completed before any MB host interface read or write training to

ensure that the MB DRAM interface is configured optimally for *DRAM reads and*

writes.’” (Pet. at ~~36~~34) (citing Ex. 1015 at 3, 8-9). “[T]he training *is carried out by*

memory buffer (module controller) itself.’” (Pet. at ~~32~~30). Thus, in JEDEC, a

memory buffer on the memory module performs training on the data signal lines.

(See Ex. 1015).

90. ~~81.~~ The Petition also contends that in Buchmann, “training sequence TS3 involves ‘upstream lane training’ and is ‘used to perform *upstream data lane*

training.’” (Pet. at ~~31~~29) (citing Ex. 1016 at 8:24-47). According to the Petition,

Buchmann “discloses a ‘training phase that allows more flexibility and improved

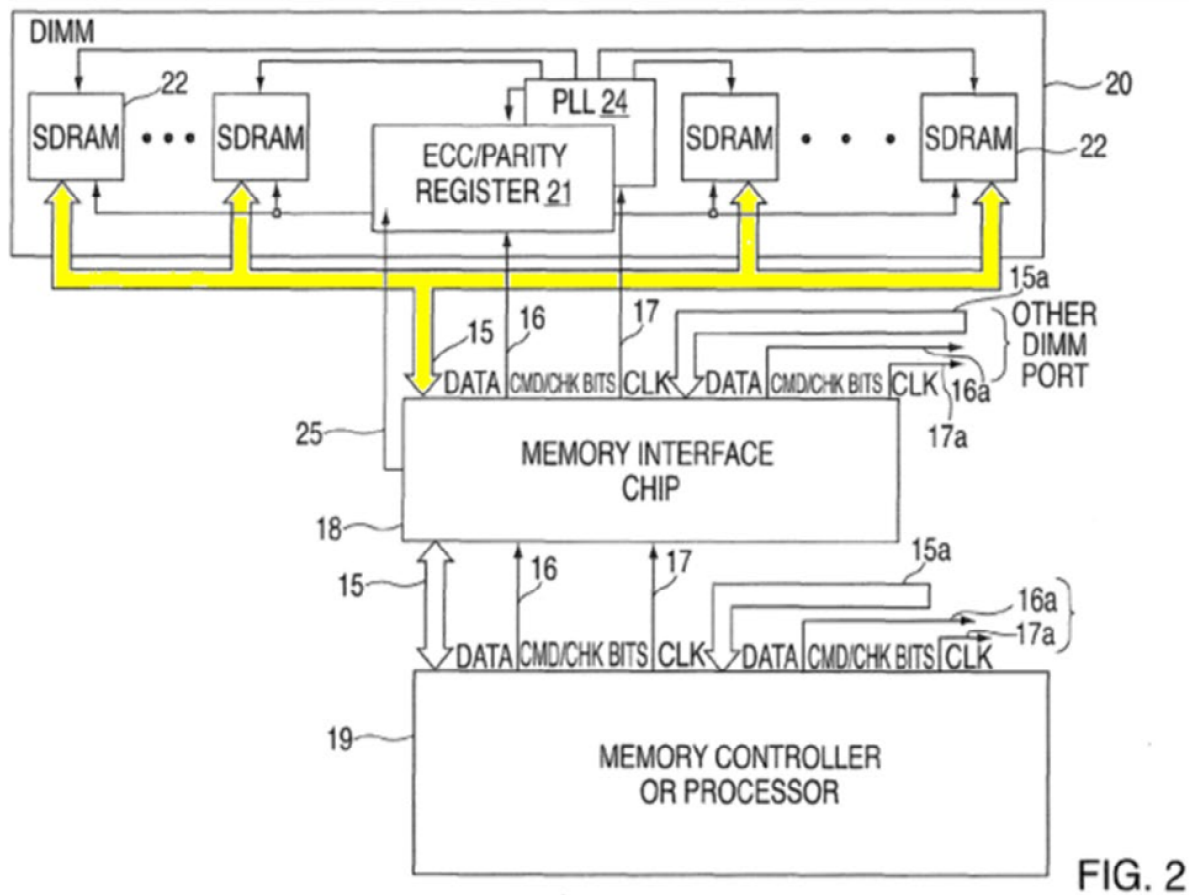
control *data exchange* during start-up.” (Pet. at ~~38~~36) (citing Ex. 2016 at 3:64-67).

Although I do not agree that the Petition’s citations teach training between the

memory buffers (106) and the DRAM memory devices (108), Buchholz does not disclose training the data signals between the memory buffer and the memory devices. (See Ex. 1016 at 11:48-12:59, ~~Figure~~, Figures 13 & 16, claim 10).

91. ~~82.~~ Hazelzet does not have memory modules that buffer data signals.

The Petition acknowledges this fact. (Pet. at ~~37~~35) (“~~Like~~[L]ike Hazelzet’s module, which buffers only address and command signals”). As shown in Figure 2 of Hazelzet, there is no memory module component that sits between the memory controller (19) or memory interface chip (25) and the memory devices (SDRAMs 22). The data lines of Hazelzet are annotated yellow below:



Thus, the memory modules of Hazelzet are incompatible with JEDEC's and Buchmann's alleged training in an initialization mode. The Petition acknowledges that Hazelzet's memory modules cannot perform the JEDEC or Buchmann alleged training, instead arguing that "[i]n either combination, the circuitry of Hazelzet's module, *in particular the ECC/Parity register*, would be modified to implement the training as part of an additional mode to run, for example, at initialization." (Pet. at [3331](#)).

[92.](#) ~~83.~~ As discussed in more detail below (Section IX.B.), "modifying" Hazelzet's ECC/Parity register just to implement training like JEDEC or Buchmann

would include fundamental and complex redesigns to the entire system. IPR~~2022-00062~~2022-0006 No. ~~9,858,218~~10,474,595
 IPR concerning the ‘~~218~~595 Patent (IPR~~2020-01044~~2020-01042), which both myself and Petitioner’s expert Dr. Alpert were involved with, when addressing these same combinations of Hazelzet/JEDEC and Hazelzet/Buchmann, Dr. Alpert acknowledged that Hazelzet does not have the memory buffer or the interfaces that would be needed to add the particular training sequences of JEDEC or Buchmann to Hazelzet, and that modification of the Hazelzet system to implement such training would require “extensive” testing. (Ex. 2002 at 68:19-79:24, 81:18-83:5).

93. ~~84.~~ Unlike in the prior IPR (IPR~~2020-01044~~2020-01042), where neither the Petitioner in that IPR nor Dr. Albert acknowledged (or understood) that a foundational predicate to adding JEDEC’s or Buchmann’s specific training in Hazelzet required fundamentally changing Hazelzet’s memory modules, the present Petition now contends that a POSITA would have been motivated to “modify” or “update Hazelzet’s RDIMM to a LR-DIMM of JEDEC” before implementing the JEDEC or Buchmann alleged training. (Pet. at ~~3230~~3634).

2. POSITA Would Not Have Been Motivated by Hazelzet, JEDEC, and/or Buchmann To Redesign Hazelzet’s Memory Modules to Buffer Data Signals

94. ~~85.~~ Each of Petitioner’s Grounds requires that POSITA would have redesigned Hazelzet’s memory modules to add JEDEC’s or Buchmann’s memory buffers to buffer data signals in addition to the address and control signals. (Pet.

at~~32~~30). Each combination is predicated on Petitioner's contention that Patent No. ~~9,858,218~~10,474,595 "[a]lthough Hazelzet discloses a Registered DIMM (RDIMM), it would have been obvious to update Hazelzet's RDIMM to a LR-DIMM of JEDEC." (Pet. at ~~36~~34, ~~39~~37). In my opinion, all Grounds require this modification to Hazelzet to succeed because Hazelzet's disclosed memory modules are incompatible with JEDEC's and Buchmann's alleged training in an initialization mode (Petitioner's second modification to Hazelzet). (Ex. 2002 at 68:19-79:24, 81:18-83:5). However, it is also my opinion that all Grounds should be rejected because neither Hazelzet, JEDEC, nor Buchman provide any teaching that would have motivated POSITA to change Hazelzet's memory modules to buffer data signals.

95. ~~86~~. The Petition contends that a POSITA would have been motivated to make this complex redesign of Hazelzet's memory modules in order to "increase performance and capacity":

The LRDIMM Design Specification explained in detail the advantages, including *increased performance and capacity*, of adding the LRDIMM's data buffering functionality to an RDIMM, like Hazelzet's module, which buffers only address and command signals. EX1036, 5. Thus, a Skilled Artisan would have understood and been motivated at the time to upgrade Hazelzet's RDIMM with an LRDIMM functionality to buffer the data lines as well.

(Pet. at ~~37~~35). The Petition provided the same conclusory opinion in view of Buchmann. (Pet. at ~~38~~36). Petitioner offers no other reason to change the memory module of Hazelzet, and simply states that "[s]uch an upgraded LRDIMM would

have worked even in Hazelzet's RDIMM platforms (with appropriate BIOS changes)." (Pet. at ~~37~~35). In my opinion, just because one could increase performance and capacity, it does not necessarily follow that one would have been motivated to do so. Neither Hazelzet, JEDEC, nor Buchman provide that motivation.

96. ~~87.~~ Even years after LR-DIMMs were commonly and commercially available, the industry still debated the trade-offs between LR-DIMMs and RDIMMs, recognizing, like Hazelzet does, that different overall system configurations and requirements motivate a POSITA to use one or the other. (*See* Ex. 2006 at 1 ("We have encountered many clients that assume since the LRDIMM is the newest memory on the block, it must be the best memory to use in their newest server. However, this is often not the case!")); Ex. 2017 at 1 ("Recently, while carrying out memory testing in our integration lab, Lead Systems Integrator, Rick Warner, was able to clearly identify when it is appropriate to choose load-reduced DIMMs (LRDIMM) and when it is appropriate to choose registered DIMMs (RDIMM) for servers running large amounts of DDR4 RAM (i.e., 256 Gigabytes and greater). The critical factors to consider are latency, speed, and capacity, along with what your computing objectives are with respect to them.")).

97. ~~88.~~ The industry recommended that in certain use cases, "you should be using RDIMMs (which are less expensive than LRDIMMs)." (Ex 2006 at 5). The

industry also advised that “[m]any of our [] customers are looking for ~~high speed~~ high speed ~~9,858,218~~ 10,474,595 *and low latency*. In that realm, *RDIMMs are the hands down winner*.” (Ex. 2017 at

3). And balancing *cost and performance*, *RDIMMs were endorsed as the “right choice”* for memory performance. (Ex. 2017 at 3) (“At slightly cheaper cost and with the ability to ramp up memory frequency on certain motherboards, they [RDIMMs] are the right choice for fast memory performance.”) Thus, “increased performance” (Pet. at 37) would not have motivated POSITA to redesign Hazelzet’s RDIMM to LR-DIMMS because RDIMMs are “the right choice for fast memory performance.” (Ex. 2017 at 3).

98. ~~89.~~ The Petition does not address *why* a POSITA would modify Hazelzet to add LR-DIMM functionality other than a generic statement about increasing performance and capacity. As discussed in more detail below, a POSITA would not be motivated to redesign Hazelzet’s RDIMMs with LR-DIMM functionality because this would be contrary to Hazelzet’s stated design for “low or midrange server markets” that used “simple, relatively inexpensive” “*reduced-function memory assemblies*” having an “adequate level of asset-protection” at “low cost,” which also had the benefit of “*eliminating the need to produce or procure two*

types of buffer devices or to *re-design existing memory modules*.” (Ex. 1014 at

US Patent No. ~~9,858,218~~10,474,595

[0005]-[0007], [0014]).

99. ~~90.~~ Although the Petition suggests that a “LRDIMM Design Specification explained in detail the advantages, including *increased performance and capacity*, of adding the LRDIMM’s data buffering functionality to an RDIMM,” that document states only that:

The Memory Buffer (MB) buffers both address and data. Increased performance is achieved based on the LRDIMM presenting only one load to the system. Increased capacity is achieved since the MB drives only the SDRAMs on the module and therefore a well defined topology and load.

(Ex. 1036 at 5). This is not a “detailed explanation” and that design specification does not describe any additional advantage to using LR-DIMMs over RDIMMs other than generically stating that increased performance and capacity are achieved. This would not have motivated a POSITA to change Hazelzet’s memory modules, particularly, as discussed below, in view of Hazelzet’s teaching away from using such modified memory modules in that system. Moreover, that LR-DIMM Design Specification (Ex. 1036) is not even included among the art Petitioner relies on in any Ground challenging the claims.

100. ~~91.~~ The LR-DIMM Design Specification (Ex. 1036) also does not describe *how* one would change RDIMMs to LR-DIMMs within an existing memory architecture designed to use RDIMMs (like Hazelzet). (See Ex. 1036). JEDEC has, for many years, concerned itself with providing manufacturers with the

means to create compatible/interchangeable parts to supply the computer/electronics industries. However, JEDEC's standards are limited to the general functionality and interoperability aspects of chip design—that is: the border specifications and general internal workings. JEDEC rarely, if ever, teaches the manufacturers how to design any detailed aspects of the circuitry needed to comply with the standards that JEDEC sets by the manufacturers. The same is true here. Neither the LRDIMM Design Specification (Ex. 1036), nor JEDEC (Ex. 1015), inform a POSITA *how* to make a memory module such as a LR-DIMM, and does not inform a POSITA *how* to change RDIMMs to LR-DIMMs within an existing memory architecture designed to use RDIMMs.

101. ~~92.~~ Although the present Petition now asserts that “[s]uch an upgraded LRDIMM would have worked even in Hazelzet’s RDIMM platforms (with appropriate BIOS changes)” (Pet. at ~~37~~35), neither the Petition nor Dr. Alpert actually explain how that could be done and thus why a POSITA would have been motivated to do so—particularly in view of Dr. Alpert’s prior testimony that making such a modification would require several changes and extensive testing. (Ex. 2002 at 68:19-79:24, 81:18-83:5).

a) Hazelzet Provides No Motivation to POSITA to Redesign Hazelzet’s Memory Modules to Buffer Data Signals

102. ~~93.~~ In my opinion, Hazelzet provides no motivation to add a memory

buffer that buffers the data signals. Instead, Hazelzet teaches away from adding more complex data line buffers to its memory architecture.

(1) Memory Modules that Buffered Data Signals Existed At the Time of Hazelzet

103. ~~94.~~ As discussed above, all Grounds require, and the Petition contends, that a POSITA would have been motivated to replace “Hazelzet’s RDIMM with an LRDIMM functionality to buffer the data lines” in order to “increase performance and capacity.” (Pet. at ~~37~~35). There are a number of different ways known to a POSITA at the time of Hazelzet to increase memory performance and capacity. For example, Dr. Alpert explained that *Hazelzet’s use of parity* increased the system’s performance. (See Ex. 2003 (Alpert Deposition) at 65:13-66:3) (“A. ... ECC mode would give a better coverage for errors and the parity could give better performance. Q. And how would the parity give better performance? A. The parity mode does not provide the capability of correcting errors, and so the memory accesses proceed, and if there is an error that’s found, it’s reported later, after the error might have had an effect on the system, but there was basically no delays associated with the error detection for parity.”). As another example, U.S. Patent Publication No. 2009/0103373 (Ex. 2018) describes a number of then-prior art systems that were developed to *increase capacity* of memory systems, as compared to the system architecture of Hazelzet. (Ex. 2018 at [0011]-[0016]; Figures 1(c), 2(a), 2(b) & 2(c)). However, the Petition and Dr. Alpert only blindly

consider redesigning the memory modules to include the added functionality of No. ~~9,858,218~~10,474,595 buffering the data lines as the **only** choice to increase memory performance and capacity. Yet, as discussed throughout this declaration, reading Hazelzet as a whole, a POSITA would not be motivated to change Hazelzet's RDIMMs to LRDIMMS (or other similar memory module that buffered the data lines) to increase performance and capacity in Hazelzet's "low cost," "reduced function memory assembly" for "low or midrange server markets." (Ex. 1014 at [0005]-[0014]); [0014] ("***eliminating*** the need to produce or procure ***two types of buffer devices or to re-design existing memory modules***").

104. ~~95.~~ Indeed, at the time of Hazelzet, memory modules were known that buffered data signals *and* performed training sequences. For example, U.S. Patent Publication No. 2005/0138267 to Bains *et al.* (Ex. 2004, "Bains") describes "fully-buffered memory modules" that buffer data, address and control signals, and implement "built-in self test (BIST)" function that "can initiate test sequences to test the device's memory channels and/or test the DRAM devices." (Ex. 2004 at [0023]-[0034], Figures 4-6). Bains describes "fully-buffered memory modules," which differ from standard DIMMs in several respects. "Primary among these differences is the presence on the memory module of *a memory module buffer that isolates the memory devices on the module from the memory channel that connects the module to an MCH (or processor).*" (Ex. 2004 at [0023]). This is analogous to an LR-DIMM buffer as discussed in the Petition, which hides the memory devices

behind the memory buffer from the memory controller. Bains further describes that “southbound data path comprises a host-side memory channel SB data input and a downstream memory channel SB data output that normally redrives the differential signals received at the SB data input. A SB data interface 330 passes buffer commands and data received at the SB data input to a DRAM interface 340, and potentially to BIST 350. In test modes, BIST 350 can also provide signals to SB data interface 330 to be driven on the southbound data output.” (Ex. 2004 at [0031]). Bains further describes that “BIST [built-in self test] function 350 can initiate test sequences to test the device’s memory channels and/or test the DRAM devices.” (Ex. 2004 at [0034]). Similar to Buchmann (discussed below, Section IX.C.2-), Bains also teaches that “a SMBus controller 360 connects to BIST function 350.” (Ex. 2004 at [0034]).

105. ~~96.~~ Additional examples of memory modules that buffered data signals *and/or* performed training sequences before the time of Hazelzet include: U.S. Patent Publication 2005/0138302 (Ex. 2015) at [0014]-[0016], [0023] [0039] & [0048]-[0052], and Intel, *Fully Buffered DIMM (FB-DIMM) Design Considerations* (Ex. 2016) at 4, 5, 24 & 30.

106. ~~97.~~ Buffering data lines was a well-known option at the time of Hazelzet. However, as demonstrated by Hazelzet’s decision *not* to use an additional buffer to, or include additional functionality in the ECC/Parity register to, buffer the data lines, just because a POSITA *could* buffer the data lines, does not mean that a

POSITA *would* buffer the data lines. As discussed immediately below, Sw. Petition No. ~~9,858,218~~10,474,595 not to use an RDIMM or a memory module that also buffers the data lines (like an LR-DIMM) is driven by the overall system design considerations beyond merely “increased performance and capacity.”

(2) There Was—And Still Are—Significant Design Problems To Overcome If Implementing Memory Modules that Buffer Data Lines

107. ~~98.~~ In my opinion, POSITA would have understood that implementing a memory buffer that buffers the data signals would not necessarily have been desired or the right choice in designing a memory system.

108. ~~99.~~ Although, as discussed immediately above, memory modules that buffered data signals *and* performed training sequences were known before Hazelzet—contrary to the Petition’s position—Hazelzet does not teach to use them. This is because, which would also have been known to POSITA, memory modules that buffered data signals had several disadvantages, such as increased complexity, power consumption, and perhaps most significantly, costs. (Ex. 1027 at ~~2:12–19~~2:12–19 (“[T]raining sequence[s] may require bi-directional data exchange, certain components or registers are not available for such training methods, since the provision of bi-directionality may require a disadvantageous addition of circuitry. Additional circuitry may not only increase device complexity and cost, but may also worsen signal transmission characteristics, and, therefore,

the reliability.”)); *see also* Section IX.A.2. above, including Ex. 2006 and Ex. 2010 No. 9,858,218 10,474,595 (describing known trade-offs between LR-DIMMs and RDIMMs). As discussed above, increased cost and complexity is something Hazelzet teaches away from.

109. ~~100.~~ A POSITA could not simply swap out RDIMMs for LR-DIMMs (or similar type memory modules as the Petition contends). The Petition failed to demonstrate how the proposed combinations of Hazelzet/JEDEC or Hazelzet/Buchmann could have been done (or that there would have been any reasonable expectation of success in doing so). Petitioner merely makes the conclusory contention that “[s]uch an upgraded LRDIMM would have worked even in Hazelzet’s RDIMM platforms (with appropriate BIOS changes)” (Pet. at 3735 (citing ~~Exhibit~~ Ex. 1036, which is not a reference combined in any Ground)). The

Petition does not provide any other support for this conclusory position, and Dr. Alpert provides the similar conclusory opinion that it “was possible to achieve these advantages in existing, RDIMM based systems, like in Hazelzet.” (Ex. 1003 at ¶ ~~155~~ 176). These unsupported contentions are contrary to the contemporaneous references at the time of the ‘~~218~~ 595 Patent.

110. ~~101.~~ As an initial matter, that same document that the Petition and Dr. Alpert cite for their conclusory positions (Ex. 1036, LRDIMM Design Specification) contradicts them, describing that “[a]s defined the controller must have the capability to do address mirroring.” (Ex. 1036 at 5). Hazelzet does *not* teach

a controller with the capability to do address mirroring, and neither the ~~US Patent No. 9,858,218~~ US Patent No. 10,474,595 Dr. Alpert contends that it does. Thus, even the document the Petition and Dr. Alpert cite for their generic assertions contradicts their positions.

111. ~~102.~~ In addition, it was well known at the time of the ~~‘218~~ 595 Patent that there were significant design problems to overcome if one were to attempt replacing RDIMMs with LR-DIMMs (or similar type memory modules as the Petition contends) in an existing memory system. The Petition does not address the contemporaneous art detailing the problems associated with LR-DIMMs, or address how POSITA would implement LR-DIMMs in Hazelzet:

- LR-DIMMs complicate memory configuration. (Ex. 2007 (US 8,402,208) at 1:37-61) (“However, different types of DIMMs consume varying numbers of clock signals (CLK), clock enable signals (CKE), on- die termination signals (ODT), and rank chip select signals (CS). Some of these signals are configurable via LR-DIMM control and status registers (CSRs). Complicating memory configuration matters for IHS designers, the number of physical ranks per DIMM varies from 1 to 8, the number of different operating voltages is 2 and will soon be 3, and the number of possible operating frequencies is now 3 but will soon be 5-6. An operating frequency of a DIMM is a function of DIMM type, number of data and address/control loads per DIMM, IO drivers, and physical channel characteristics.”)
- LR-DIMMs introduce delays that result in mismatched signals between the host and memory interface. (Ex. 2008 (US 8,452,917) at 2:12-30) (“Buffering in LRDIMMs results in the addition of at least one clock cycle delay in the control path (the same as in an RDIMM), but there is also delay added in the data path, which will cause a mismatch between the Data Queue Strobe (DQS) on the external memory bus, i.e. the memory bus 104, that carries the DQS signal between the host and the RDIMMs, and the strobe signal at the interface of the DRAM memory device within the LRDIMM.”)
- LR-DIMMs reduce timing margins. (Ex. 2009 (US Pub. 2011/0007585) at

[0003]) (“To address the issues mentioned above, the industry proposed fully buffered memory architectures such as FB-DIMM (Fully Buffered Dual In Line Memory Module) and LR-DIMM (Load-Reducing Dual In Line Memory Module). Each of such DIMMs has one or more buffers thereon to buffer data exchange between DRAMs (Dynamic Random Access Memory) on the DIMMs and a memory controller or a host. Each buffer provides a clock signal for read/write operations to the corresponding DRAMs using a multi-drop (fly-by) topology, so there will be phase difference between the clock signals received by different DRAMs due to different trace lengths. To ensure proper data transmission, each DRAM aligns its data signal (DQ) and a pair of data strobe signals (DQS/DQS#) with the received clock signal when sending the signals to the buffer, wherein DQS signal and DQS# signal are a pair of differential signals. But the phase relationship between the DQ/DQS/DQS# signals and the received clock signal may change with process, voltage, and temperature variations over time, leading to reduced timing margin for the buffer”)

- LR-DIMMs create long wiring paths for outputting signals. (Ex. 2010 (US 8,054,664) at 4:8-15) (“The LR buffer requires long wiring paths for outputting CA signals. It is known that when the output of the LR buffer is followed by long aggregate wiring paths, a large ring-back generally occurs in a DRAM at a distal end, and this can be said to constitute a factor for degrading the reliability of transmission quality.”)
- LR-DIMMs create non-uniform distribution of allocated loads. (Ex. 2010 (US 8,054,664) at ~~4:16-25~~4:16-25) (“Allocated loads (DRAMs) are not uniformly distributed to CA signal outputs of the LR buffer. Discontinuity of loads causes discontinuity of execution characteristic impedance (which includes taking into consideration on the influence of a capacitive load placed on a wire added to characteristic impedance Z_0 originally exhibited by the wire. It is generally known that the capacitive load causes an impedance exhibited by a wire itself to be lower than its original value), which can constitute a factor for degrading the reliability of transmission quality.”)
- LR-DIMMs create limited wire routing options. (Ex. 2010 (US 8,054,664) at ~~4:26-38~~4:26-38) (“The routing of wires is penalized by the termination resistors positioned in a central region of the board. Generally, this region is densely populated with wires such as CA wires coming back from connectors, wires for CA output signals and DQ output signals of the LR buffers, and the like. There is no wiring space

available on a surface layer because pads for mounting DRAMs, passive parts and the like are mounted on the surface layer, and the foregoing signals, generally in a bus form, cannot pass through the surface layer, and therefore pass through an inner layer. Also, since CA signals traveling through the inner layer eventually reach a termination resistor, they once appear on the surface layer through TVH (Thru Via Hole) or BVH (Blind Via Hole).”)

- LR-DIMMs limit routing output options. (Ex. 2010 (US 8,054,664) at ~~4:48-53~~4:48-53) (“Limitations exist in methods for routing outputs from the LR buffers (topology). Due to the positional relationship between LR buffers in LR-DIMM, even if one attempts to modify the wiring structure in order to improve the transmission quality, the only option is a wiring structure which involves discontinuous loads as shown in FIG. 5.”)
- LR-DIMMs create crowded wiring around outputs. (Ex. 2010 (US 8,054,664) at ~~4:54-51~~4:54-51) (“Wires are crowded around outputs of the LR buffers because a mixture of input and output CA signals and DQ signals go back and forth there. As is apparent from FIGS. 5 and 6, wires are densely crowded in the LR-DIMM due to a bus which accommodates input/output CA signals that go back and forth around the outputs of the LR buffer, and input/output DQ signals which extend radially. For the reason set forth above, such crowded wires should be avoided.”)

112. ~~103.~~ In addition, other references discussed significant design problems to overcome when buffering both data signals and address and control signals. For example, U.S. Patent Publication 2005/0138302 (Ex. 2015) describes that fully buffered memory devices (that buffer data lines and control and signal lines) create challenges associated with validation and debugging because, referring to Figure 2, “[t]he memory device bus (not shown) between the MMB 146 and the DRAMs 144 on each memory module 120, 130, 140, 150 operates at significantly slower speeds than the memory channels 112, 122, 132, 142. For example, typical speeds for the memory channels 112, 122, 132, and 142 are on the order of 3 to 5 giga-

transfers/second, while between the MMB 146 and the DRAMs it is ~~US Multiplied.~~
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to approximately 6 times slower for data and approximately 12 times slower for
address and control signals. Conventional logic analyzers do not have the ability to
directly probe signals at the same speeds as the memory channels 112, 122, 132, and
142. And even though the MMB to DRAM buses typically operate at much lower
frequencies they are inaccessible to the logic analyzer since they are buried internal
to the memory module board.” (Ex. 2015 at [0024]-[0025]).

113. ~~104.~~ Each of these above problems is directly associated with
implementing LR-DIMMs in a system like Hazelzet and the resulting performance
and reliability of an LR-DIMM and its associated read and write functionality in
normal operation. The claimed invention requires the memory module to operate
in a mode in which it performs read and write operations. Modifying the memory
module in Hazelzet to an LR-DIMM (or adding a buffer that buffered the data
signals) would introduce at least each of these problems when redesigning
Hazelzet and during normal operation in Hazelzet’s redesigned memory system.

114. ~~105.~~ The Petition and Dr. Alpert do not address these issues, instead
suggesting only, in conclusory fashion, that “LRDIMM would have worked even in
Hazelzet’s RDIMM platforms.” (Pet. at ~~37~~35). The conclusory statements in the
Petition and in Dr. Alpert’s declaration do not change my opinion that Hazelzet
(alone or when read in view of the other art presented in the Petition, including the
LRDIMM Design Specification (Ex. 1036), JEDEC, and Buchmann), and in view

of the knowledge at the time demonstrated through contemporaneous use. ~~US Patent No.~~
~~9,858,218~~10,474,595
above, would not have provided POSITA any motivation to replace Hazelzet's

RDIMMs with LR-DIMMs (or similar type memory modules as the Petition contends). For instance, despite Dr. Alpert opining that the "combination would have been well within the level of skill at the time" (Pet. at ~~373~~35; Ex. 1003 at ¶ ~~156~~177), when making the same combination, Dr. Alpert previously testified that his analysis was "not concerned with the physical embodiments and how... those structures might be physically modified. ... I haven't considered what—you know, exactly how those changes would be made." (Ex. 2002-~~at~~2, 68:19-69:20).

115. ~~106.~~ In my opinion, Dr. Alpert's conclusory testimony would not have motivated POSITA to implement JEDEC's or Buchmann's memory buffers into Hazelzet's system, nor would it demonstrate that such a combination could even be accomplished.

**(3) Hazelzet Already Solves the Problems
that Hazelzet Identifies—the Petition**

**Seeks to Solve Problems *Not* Identified by
Hazelzet and In a Different Way from
Hazelzet's Solutions**

116. ~~107.~~ As discussed above, the Petition repeatedly contends that POSITA would have been motivated to replace “Hazelzet’s RDIMM with an LRDIMM functionality to buffer the data lines” in order to “*increase performance and capacity.*” (See Pet. at ~~37~~35). But Hazelzet does not identify either increased performance or increased capacity as a problem to be solved by Hazelzet. Instead, as the Petition contends, Hazelzet addresses a need for “improved overall system *reliability.*” (Pet. at ~~35~~33 (citing Ex. 1014 at ¶¶ [0001]-[0004], [0007], [0042], [0044])).⁴ Neither the Petition, nor Dr. Alpert, identify anything specific in

Hazelzet identifying a problem to be solved regarding “increase performance and capacity.” Thus, the Petition’s focus on applying a generic motivation to “increase performance and capacity”—based on a reference that *post-dates* the ‘~~218~~595 Patent Provisional—appears to be backwards looking and not tied in any meaningful way to Hazelzet; Hazelzet does not even identify these alleged problems that Petitioner contends POSITA would be motivated to solve through (and starting with) Hazelzet. Since Hazelzet does not identify or address problems with “increased performance and capacity,” the Petition does not identify why

⁴ This alleged “problem” of “overall system reliability” is addressed by the Petition (and Dr. Alpert) in connection with an alleged motivation to add *training*, which I address below in connection with my opinions regarding a lack of motivation in the art to add any training to

POSITA would have been motivated to attempt to solve these general problems. ~~U.S. Patent No. 9,858,218~~10,474,595 in the context of Hazelzet. POSITA would not have been motivated to “increase performance and capacity” of Hazelzet through the disparate teachings of JEDEC and Buchmann.

117. ~~+08.~~ Instead, as described in the Petition, Hazelzet focusses on “improved overall system reliability” (Pet. at ~~35~~34) and discloses a solution that strikes a balance between performance, capacity, reliability, and cost for low or midrange systems, which POSITA would have understood to teach away from memory modules that buffered data signals. (Ex. 1014 at [0001]-[0006]). See Section IX.A.2. above, including Ex. 2006 and Ex. 2017 (describing known trade-offs between LR- DIMMs and RDIMMs in terms of performance, capacity, reliability, and cost). Petitioner contends that “Hazelzet emphasizes the need for ‘improved overall system reliability’” (Pet. at ~~35~~34), but Hazelzet’s disclosures are silent as to how other memory systems, let alone the memory systems disclosed in JEDEC or Buchmann, would satisfy this alleged need. Instead, Hazelzet expressly discloses that “[t]he present invention accomplishes all these ends, resulting in a high density and enhanced reliability memory solution at low cost.” (Ex. 1014 at ¶ [0007]). Thus, in my opinion, POSITA reading Hazelzet’s disclosure regarding improved system reliability would have understood that Hazelzet’s memory systems and

solutions, and *not* other memory systems, accomplished those alleged. See Patent No.

~~9,858,218~~10,474,595

118. ~~109.~~ Hazelzet does not focus myopically on the system's reliability to the detriment of its performance, capacity or cost. Instead, Hazelzet considered all of these factors and disclosed a system that balanced all those needs. Rather than replacing its memory modules with increased performance and capacity memory modules, which it could have done, Hazelzet focuses instead on improving the system reliability in memory modules for "low or midrange server markets" that used "simple, relatively inexpensive" "*reduced-function memory assemblies*" having an "adequate level of asset-protection" at "low cost." (Ex. 1014 at [0005]-[0007]). Hazelzet teaches away from the then-known, more complex memory modules that buffered data signals by "*eliminating the need to produce or procure two types of buffer devices* or to *re-design existing memory modules.*" (Ex. 1014 at [0014]).

119. ~~110.~~ Thus, it is my opinion that POSITA would have been led away from adding more complex memory components that buffer data signals in addition to buffering the address and control signals. Adding more complex and more costly components to buffer the data signals would be the opposite of Hazelzet's stated purpose to use "reduced-function memory assemblies" for the "low or midrange server markets." (Ex. 1014 at [0005]-[0007]). Petitioner's conclusory motivation of increased performance and capacity does not consider Hazelzet's disclosure as a whole, which considered a balance of trade-offs between reliability, performance,

capacity and cost to arrive at Hazelzet's particular memory system and Solution No.

~~9,858,218~~10,474,595

b) JEDEC Provides No Motivation to POSITA to Redesign Hazelzet's Memory Modules to Buffer Data Signals

120. ~~111.~~ Petitioner further alleges that JEDEC would have motivated POSITA to redesign Hazelzet's memory modules to buffer data signals, but fails to point to a single teaching or disclosure in JEDEC that suggests why POSITA would, on balance, use memory modules that buffer data signals in Hazelzet.

121. ~~112.~~ There is no teaching in JEDEC that would have suggested to POSITA that JEDEC's memory subsystems are particularly advantageous over other systems. It is also my opinion that JEDEC would not have taught or motivated POSITA to use the memory subsystem (LR-DIMM) referred to in JEDEC in a system like Hazelzet. Rather, JEDEC is merely a "ballot proposal" that was approved to "specify LRDIMM DDR3 Memory Initialization." (Ex. 1015 at 1). POSITA reading JEDEC would have understood that JEDEC was simply proposing certain *training* specifications for memory systems that *already used* LRDIMM DD3. JEDEC would not have taught, suggested or motivated POSITA to actually use JEDEC's particular memory modules over other memory modules, such as the RDIMM memory modules disclosed in Hazelzet. It does not logically follow (particularly in view of the known trade-offs between LR-DIMMs and RDIMMs, discussed above) that just because JEDEC describes certain *training features* of LR-DIMMs that POSITA would have been motivated to implement

JEDEC's underlying *memory subsystem architecture* (LR-DIMMs) in ~~the~~ Patent No.

~~9,858,218~~10,474,595

The memory subsystem architecture, on the one hand, and training of that particular architecture, on the other, are two completely different, unrelated things.

122. ~~113.~~ For example, a particular memory subsystem arrangement, like those that use LR-DIMMs, will create different problems that can be specifically addressed by different training features as compared to other memory subsystem arrangements, like those that use RDIMMs. JEDEC specifically addresses training of LR-DIMMs. Memory systems that use LR-DIMMs hand over certain training sequences to the memory buffer of the LR-DIMM because the LR-DIMM memory buffer controls buffering of data signals between the host and the DRAMs. Thus, systems like JEDEC can employ training that is specific for read and write operations between the LR-DIMM memory buffer and the DRAMs. And because the JEDEC memory system hands over training to the LR-DIMM memory buffer for those read and writes between the LR-DIMM memory buffer and DRAM, the training described in JEDEC is specific to that particular memory subsystem arrangement. That JEDEC training, however, is irrelevant to the teachings of memory systems that use RDIMMs, like Hazelzet, because RDIMMs do not buffer data reads and writes to the DRAMs, and thus, no training of the memory subsystem is needed for those nonexistent system operations. Instead, in systems like Hazelzet, the memory controller, which sends the reads and writes directly to the DRAMs, is the memory system component that would control training associated with those

reads and writes *if* POSITA were motivated to perform training on reads and writes between the memory controller and DRAMs.

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123. ~~114.~~ Accordingly, JEDEC would not have motivated POSITA to change Hazelzet's memory subsystem to be an LR-DIMM architecture, especially in view of the lack of any disclosure in JEDEC that the use of LR-DIMMs was particularly advantageous or preferred.

c) Buchmann Provides No Motivation to POSITA to Redesign Hazelzet's Memory Modules to Buffer Data Signals

124. ~~115.~~ Petitioner asserts that "Buchmann discloses a buffer/register that buffers data signals in addition to address and command signals," but fails to identify anything specifically in Buchman that would have motivated POSITA to modify Hazelzet's memory buffers that are used on the address and control lines to also buffer the data signals. (Pet. at ~~38~~36). In my opinion, Buchmann would not have taught or motivated POSITA to modify Hazelzet's memory buffer to also buffer the data signals. There is no teaching in Buchmann that would have suggested to POSITA that Buchmann's memory subsystems are particularly advantageous over other systems. It is also my opinion that Buchmann would not have taught or motivated POSITA to use the memory subsystem described in Buchmann in a system like Hazelzet.

125. ~~116.~~ Buchmann, like Hazelzet, recognizes that in designing a memory

system, various constraints, including power, performance, and costs, ~~U.S. Patent No.~~ ~~9,858,218~~ 10,474,595 considered. (Ex. 1016~~-at,~~₂ 28:32-35, 29:15-19). Buchmann explains that module support devices, including buffers, may be combined or integrated “based on technology, power, space, cost and other tradeoffs.” (Ex. 1016 at 31:10-14). In my opinion, Buchmann focused on performance at the expense of cost and power in designing its memory systems that includes more chips and components, driving up the cost. This directly contrasts with Hazelzet’s systems.

126. ~~117.~~ Hazelzet balanced various needs, such as performance, capacity and cost, in designing a memory system, and taught that its lower end system would meet all those needs. Rather than replacing its memory modules with more costly components, which it could have done, Hazelzet focuses instead on improving the system reliability in memory modules for “low or midrange server markets” that used “simple, relatively inexpensive” “*reduced-function memory assemblies*” having an “adequate level of asset-protection” at “low cost.” (Ex. 1014~~-at,~~₂ [0005]-[0007]. Moreover, Hazelzet teaches “*eliminating the need to produce or procure two types of buffer devices* or to *re-design existing memory modules.*” (Ex. 1014~~-at,~~₂ [0014]).

127. ~~118.~~ Thus, in my opinion, POSITA reading Buchmann would have recognized that adding the functionality of buffering data signals would require considering various factors, such as performance and cost. POSITA would have

further understood Hazelzet explicitly already made that determination. ~~US Patent No. 9,858,218~~US Patent No. 10,474,595 to use the invention Hazelzet disclosed. Thus, POSITA would not have been motivated by Buchmann based on generic “increase performance and capacity” to modify Hazelzet’s ECC/Parity Register to buffer data signals.

3. Hazelzet Teaches Away from Using Memory Modules that Buffer the Data Signals

128. ~~119.~~ The Petition contends that “Hazelzet emphasizes the need for ‘improved overall system reliability’” and that “[g]iven that emphasis, a Skilled Artisan would have been motivated to add training to Hazelzet because it was known that training improved memory module reliability.” (Pet. at ~~35-36~~34). The petition, as discussed above, also contends that a POSITA would have been motivated to “modify” or “update Hazelzet’s RDIMM to a LR-DIMM of JEDEC” before implementing the JEDEC or Buchmann alleged training in order to “increase performance and capacity.” (Pet. at ~~36~~34).

129. ~~120.~~ But in considering system reliability, Hazelzet considered various factors, including performance, capacity and cost. Hazelzet’s solution balanced performance, reliability, capacity (i.e., density) and cost, for low-end and midrange systems (“reduced function” systems having an “adequate level of asset-protection”). (See Ex. 1014 at [0001]-[0014]). Hazelzet identified, and a POSITA would have understood, this being as being a problem overlooked by the industry. (See Ex. 1014 at [0001]-[0014]). Specifically, Hazelzet teaches “a simple, relatively

inexpensive and reliable solution that provides high memory density and differentiated product quality, that provides an adequate level of asset- protection that does not endanger the reliability of the system through the use of reduced-function memory assemblies and yet is cost competitive.” (Ex. 1014 at [0006]).

130. ~~121.~~ Hazelzet considered numerous, different solutions when balancing these competing issues for a “*low or midrange server*,” including: “memory mirroring, symbol slicing and extensive forms of fault rejection and redundancy” as well as “error detection and/or correction methods such as CRC (Cyclic Redundancy Code), EDC (Error Detection and Correction), parity or other encoding/decoding methods suited for this purpose” and “further reliability enhancements [that] may include operation re-try (to overcome intermittent faults such as those associated with the transfer of information), the use of one or more alternate or replacement communication paths to replace failing paths and/or lines, complement-re- complement techniques” and “the use of bus termination, on busses as simple as point-to-point links or as complex as multi-drop structures” (e.g., a system like Buchmann’s), which “is becoming more common consistent with increased performance demands.” (Ex. 1014 at [0005], [0127], [0128]). Ultimately, based on performance, capacity (i.e., density), cost, and reliability considerations, Hazelzet chose to implement a hybrid solution focused on error code

correction (“ECC”) functionality that, as discussed below, allows a netlist to perform normal operations in conjunction with parity. (Ex. 1014 at [0016]). Hazelzet relied on parity to enhance its system’s performance and ECC to enhance its reliability in a system designed for “low or midrange server markets.” Petitioner’s expert, Dr. Alpert, agrees. (Ex. 2003 at 65:13-19).

131. ~~122.~~ With these considerations in mind, Hazelzet presents a solution that teaches away from replacing its memory modules with more complex, increased performance and capacity memory modules. Hazelzet presents solutions to improve system reliability in memory modules for “low or midrange server markets” that used “simple, relatively inexpensive” “*reduced-function memory assemblies*” having an “adequate level of asset-protection” at “low cost.” (Ex. 1014 at [0005]-[0007]). Even more contrary to the notion that a POSITA would have been motivated to replace Hazelzet’s memory modules with LR-DIMMS, is that a “further object of the present invention” in Hazelzet was to “*eliminat[e] the need to produce or procure two types of buffer devices or to re-design existing memory modules.*” (Ex. 1014 at [0014]). The Petition’s contention that a POSITA would have been motivated to redesign Hazelzet’s existing RDIMMs with LR-DIMMs that have an *additional* buffer to buffer the data fails to consider the purpose and teachings of Hazelzet as a whole, and directly contradicts Hazelzet’s teachings for a “low cost,” “reduced function memory assembly” for “low or

midrange server markets.” (Ex. 1014 at [0005]-[0014]).

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132. ~~123.~~ Additionally, Hazelzet teaches away from the type of system that

Buchmann teaches. First, Hazelzet teaches that the DRAMs (22) of the Memory DIMM (10) should be in direct connection with the edge pins on the DIMM which then is in communication with the Memory Interface Chip on the motherboard (18)

(Ex. 1014 at Figures 2, 3A & 3B). Buchmann teaches that the DRAMs on the

DIMM (110) should be directly connected to the HUB (106) which then is in

communication via the edge pins to the Host Memory Controller (104) on the

motherboard. (Ex. 1016 at 1:63-2:4, Figures 1, 2, 13 & 16). Second, Hazelzet

teaches that multiple parallel data connections should be made via the edge pins,

with no buffering, to the Memory Interface Chip on the motherboard providing

direct low latency data operations. (Ex. 1014 at Figure 2). Buchmann however

teaches that the data should be serialized before it travels back to the HMC (104),

requiring the data to make an intermediate stop in the HUB (106), which increases

the latency and increases the power consumed by the addition of an additional chip.

(Ex. 1016 at Figure 16). Further a POSITA would have understood that for each

additional DIMM placed in Buchmann’s system, the latency would increase yet

again as another HUB crossing is encountered. (Ex. 1016 at Figure 13).

Hazelzet (one of at least ordinary skill in the art) had ample opportunity to use

these types of improvements—the application uses both buffered solutions (the

additional ECC/Parity Register for registered buffering of the address and control

lines), and the serial data solution (as shown by the use of the IIC bus, ~~S. Patent No. 9,858,218~~10,474,595 known serial bus configuration, *see* Figure 4B (ERROR BUS (IIC) (122)).

However, Hazelzet chose differently, and taught away from the use of those techniques in the proposed solution based on the design goals for *that* memory system. Thus it would not have been obvious to a POSITA to incorporate those specific features from Buchmann either.

B. There Is No Motivation to Add a Separate Training Mode in Hazelzet, Let Alone the Specific Training of JEDEC/Buchmann

133. ~~124.~~ Both of Petitioners' Grounds further require—after first redesigning Hazelzet's memory modules to add JEDEC's or Buchmann's memory buffers—adding the alleged training of JEDEC or Buchman during Hazelzet's initialization. (Pet. at 4, ~~32-33, 35-40~~30-31, 34-39). In my opinion, Hazelzet, JEDEC, and Buchmann, do not provide any teaching or suggestion that would have motivated POSITA to do so.

This is an independent reason why Grounds ~~1-3~~1-3 fail to demonstrate the challenged claims of the '~~218 Patent~~595 patent are unpatentable.

1. POSITA Would Not Have Been Motivated to Create *Any* Separate Training Mode in Hazelzet

134. ~~125.~~ Petitioner's Grounds further require, after first modifying Hazelzet's RDIMMs to include LR-DIMM functionality (or similar type memory module functionality), that a POSITA would have been motivated to also add

Buchmann's or JEDEC's alleged training to Hazelzet as a new mode of operation that is distinct from Hazelzet's normal mode of operation. (Pet. at 4, ~~32-33, 35-40~~30-31, 34-39).

Specifically, Petitioner argues, in a section titled "Motivation to Add Training in an Initialization Mode Separate from Normal Operations," that a POSITA "would have been motivated to combine the[] references by adding training in an initialization mode separate from normal operation" in Hazelzet. (Pet. at ~~39~~37). As discussed above, this alleged motivation assumes that a POSITA first would have been motivated to "modify" the "circuitry of Hazelzet's module, in particular the ECC/Parity register, . . . to implement the training as part of an additional mode to run." (Pet. at ~~33~~31).

135. ~~126.~~ The Petition, however, glosses over the discordant reconstruction of Hazelzet that would be required to add an entirely new mode of operation to that system. Indeed, Petitioner provides no evidence or explanation as to why the addition of an entirely new mode of operation would be obvious and straightforward. (Pet. at ~~35-40~~34-39). The opposite is true. Adding an entirely new mode of operation would require substantial reconstruction and redesign of Hazelzet, and doing so is not obvious, nor would there be a reasonable likelihood of success in doing so.

136. ~~127.~~ For example, below is a list of all the things a POSITA would need to contemplate when adding a new mode of operation to a memory module:

- How the "new" mode would interact with all the other existing

modes so that there would be no unwanted interactions. U.S. Patent No.

~~9,858,218~~10,474,595

- How commands to enter this “new” mode would be received and decoded and what they would control.
- What exact state the memory module would be in after the command to enter was decoded.
- What state each of the memory devices would be in while in the “new” mode, including the control of all input/output pins such that no signal contentions would occur.
- All actions that the memory module would be permitted to perform while in the “new” mode, ensuring that those actions would be permissible to the components on the module (e.g., DRAMs, Memory Buffer, Serial Detect, etc.)
- All interactions with the Host Controller while in the “new” mode, including preventing unwanted interactions with the other Memory Modules in the system.
- How to achieve proper signaling (Timing and Signal Levels) between the Memory Module and the Host Controller.
- How to know when to exit from the “new” mode, including how to exit such that the Memory Module and Host Controller are appropriately set up for any of their next potential operations.
- What power might be consumed during the “new” mode and implementation of potential power mitigation strategies.

137. ~~128.~~ The Petition and Dr. Alpert fail to address any of these issues that

any POSITA would have understood would be necessary to consider when adding a new mode of operation to a memory module. And these are just considerations one would need to contemplate when adding a new mode to a memory module. For Hazelzet, which discloses a memory device, a similar list of considerations would need to be considered:

- How the “new” mode would interact with all the other existing

modes so that there would be no unwanted interactions. U.S. Patent No.

~~9,858,218~~10,474,595

- How commands to enter this “new” mode would be received and decoded and what they would control.
- What exact state the memory device would be in after the command to enter was decoded.
- What state each of the memory devices would be in while in the “new” mode, including the control of all input/output pins such that no signal contentions would occur.
- All actions that the memory device would be permitted to perform while in the “new” mode, ensuring that those actions would be permissible to the components on the module (e.g., DRAMs, Memory Buffer, Serial Detect, etc.)
- What signal actions are permissible between the Memory Device and the Memory Buffer while in the “new” mode.
- All interactions with the Memory Buffer while in the “new” mode, including preventing unwanted interactions with the other Memory Devices on the Memory Module.
- How to achieve proper signaling (Timing and Signal Levels) between the Memory Device and the Memory Buffer.
- How to know when to exit from the “new” mode, including how to exit such that the Memory Device and the Memory Buffer are appropriately set up for any of their next potential operations.
- What power might be consumed during the “new” mode and implementation of potential power mitigation strategies.

138. ~~129.~~ Dr. Alpert appears to have conceded this point during the prior

IPR (IPR~~2020-01044~~2020-01042), noting that adding a new mode of operation to a memory module like Hazelzet would include fundamental and complex redesigns to the entire system, which would have to be tested “extensively.” (Ex. 2002 (Alpert Deposition) at 68:19-79:24, 81:18-83:5). Despite acknowledging these

issues, the Petition and Dr. Alpert fail to address any of them when discussing Patent No. ~~9,858,218~~10,474,595 they would add training to Hazelzet, and instead suggest the combinations would be “exceedingly straightforward.” (Pet. at ~~32~~30). I disagree. For at least the reasons above and below, a POSITA would have recognized that the Petition’s proposed combinations would not have had a reasonable likelihood of success.

a) Adding Training To Hazelzet Would Have Added Unnecessary Complexity and Cost

139. ~~130.~~ Before demonstrating that it would have been obvious to add JEDEC/Buchmann’s specific training to Hazelzet, it must first be demonstrated that it would have been obvious to add *any* training at all. Petitioner contends that POSITA would have been motivated to add training because it was allegedly known that “training improved memory module reliability.” (Pet. at ~~35-36~~34). Even assuming training would improve memory module reliability in *some* systems, in my opinion, POSITA would have understood that training is not necessary, or even desired, in other systems, particularly in systems like those described in Hazelzet, which specifically did not include training in favor of more cost-effective solutions, such as parity bit error checking.

140. ~~131.~~ Indeed, Dr. Albert admitted that adding training from JEDEC into Hazelzet would require implementing bi-directional data exchange, a feature not present in the ECC/Parity register in Hazelzet. (Ex. 2023 at ~~244:17-245:16~~244:17-245:16). As one of Petitioner’s references explains, implementing bi-directional data exchange requires additional components and

circuitry that may “not only increase device complexity and cost, but may also worsen signal transmission characteristics, and, therefore, the reliability.” (Ex. 1027 at ~~2:12-19~~2:12-19) (“Since this training sequence may require bi-directional data exchange, certain components or registers are not available for such training methods, since the provision of bi-directionality may require a disadvantageous addition of circuitry. Additional circuitry may not only increase device complexity and cost, but may also worsen signal transmission characteristics, and, therefore, the reliability.”). Thus, in my opinion, POSITA would have understood—including from Petitioner’s own references—that *adding* JEDEC/Buchman training to Hazelzet would require additional circuitry, which can actually *worsen* reliability in some systems.

141. ~~132.~~ It is my opinion that POSITA would have further understood that any improved module reliability would come at the cost of decreased efficiency, or other trade-offs. For instance, in describing the implementation of training, Buchmann describes that “[e]ntering TS0 using SBC during run-time will result in a downstream CRC error. This will cause the MB chip to enter the error recovery state (ERS).” (Ex. 1016 at ~~5:61-63~~5:61-63). Buchmann thus teaches that the system cannot enter training during run-time; otherwise, the training would result in an error. As such, Buchmann teaches that the memory module must hold for the training sequence to return a “handshake” to resume status. (Ex. 1016 at 6:59-62) (“[w]hen MB0 has completed the TS0 a state processing it returns a handshake

(e.g., via SBC) to the HMC to let it know that TS0 a has been completed. Let's Patent No. ~~9,858,218~~10,474,595 status (e.g., successful).”). Therefore, POSITA would understand that there is an inherent inefficiency when using the training described in the prior art in that the system must wait for a signal from the training module that training is complete. Indeed, as another of Petitioner’s references explains, entering training mode inhibits the operational mode of the memory system. (Ex. 1057 at 2:28-34) (“The memory controller uses one or more interface parameters in the operational mode. The method include inhibiting the operational mode to enter a training mode.”).

142. ~~133.~~ It is for these reasons that some memory systems do not implement training at all, especially when balancing various factors like cost and efficiency. (Ex. 2028 at 7) (“*The LX processor/DDR2 solution does not do DQS training.* The LX processor’s memory controller does not have the adjustability to make this worthwhile, and the speeds are slow enough that this is not a problem.”)). Thus, in my opinion, when reading Hazelzet (alone or when read in view of the other art presented in the Petition, including JEDEC, and Buchmann), POSITA would not have been motivated to add training to a memory system like Hazelzet’s, especially when balancing all of the factors.

2. Hazelzet, JEDEC, and Buchmann Would Not Have Motivated POSITA To Add Training To Hazelzet

a) Hazelzet Provides No Motivation To Add Training Because It Doesn’t Mention Training

143. ~~134.~~ As an initial matter, Hazelzet does not disclose training, which Dr.

Alpert appears to concede. (Ex. 2023, 210:19-23) (“I don't recall any ~~US Patent No.~~ 9,858,218 10,474,595 Hazelzet.”). It would also not have been obvious to POSITA to implement

JEDEC's or Buchmann's training in Hazelzet because such a combination would be inoperable by Hazelzet's memory module. Dr. Alpert appears to agree with me in view of his deposition admissions. (Ex. 2002 at 68:19-79:24, 81:18-83:5).

Also, during his deposition in this IPR, Dr. Alpert admitted that in the context of DDR generation of DRAMs (like Hazelzet), he was “*not aware of any reason why one of ordinary skill in the art, reading Hazelzet, would be motivated to add training to Hazelzet.*” (Ex. 2023 at 288:10-17).

144. ~~135.~~ In my opinion, adding an entirely new training mode of operation to Hazelzet would require substantial reconstruction and redesign. It appears that Dr. Alpert also conceded this point during his deposition in a prior IPR, admitting that adding a new mode of operation to a memory module like Hazelzet would include fundamental and complex redesigns to the entire system (Ex. 2002 at 70:3-76:10), which would then have to be tested “extensively:”

14 Q Other than changes to the
15 interfaces, are there any other changes that
16 you would need to make to the high-level
17 model of Hazelzet?
18 A Yeah. After you did that, I think
19 you would want to identify how the state of
20 the training mode would be represented.
21 Generally, one or two or a certain
22 number of bits. The combination that's
23 inscribed here only uses the parity mode of
24 Hazelzet.

25 But you would want either the
1 parity mode or a training mode, and that
2 would be represented as a particular bit in a
3 control register, or multiple bits.
4 And then you would go ahead and
5 design, again, the high -- at an HDL level,
6 the logic that would sequence through

7 these -- for these training sequences, such
8 as the right leveling and the read enable
9 training.

10 *And then you would test that*
11 *extensively versus a -- some type of model or*
12 *test suites that were available.* And 13
eventually, after you're convinced that the 14
logic level was appropriately accurate in 15
terms of the functions that were being 16
performed, you would develop the circuit 17
level, circuit -- physical design level, 18 circuit
and layout of the logic elements and 19 of the
interfaces, you know, simulate that as 20 well, in
particular for the performance 21 requirements
and the voltage ranges, voltage 22 and
temperature ranges.

(Ex. 2002 at 70:14-71:22). Despite previously acknowledging these very issues,
Petitioner and Dr. Alpert still failed to address any of them when discussing how
POSITA would allegedly add a new training mode to Hazelzet. (Pet. at
~~32-40~~[30-40](#)).

[145.](#) ~~136.~~ Petitioner argues that Hazelzet would have motivated POSITA to
add training because it emphasized the need for “improved overall system
reliability.” (Pet. at 36; Ex. 1014, ¶ [0003]). But Hazelzet’s disclosures do not say
anything about how adding *training* would satisfy this alleged need. Rather,
Hazelzet identifies that “the emphasis and need for improved overall system
reliability is increasing dramatically and *requires a comprehensive system*
solution that includes both a high degree of fault tolerance and overall
reliability.” (Ex. 1014 at [~~0003~~[0004](#)]). Contrary to Petitioner’s assertions, Hazelzet

does not provide any disclosure that would have motivated POSITA to add any other features or components outside of Hazelzet’s disclosures and recited solutions, such as training, would meet this alleged need. Indeed, Hazelzet expressly teaches that “[t]he present invention *accomplishes all these ends*, resulting in a high density and enhanced reliability memory solution at low cost.” (Ex. 1014 at ¶ [0007]). As such, in my opinion, POSITA would have understood that the invention disclosed in Hazelzet would have accomplished “all [the] ends” of any alleged need for “improved overall system reliability,” and would not have motivated POSITA to look to other, more costly and more complex features like training.

[146.](#) ~~137.~~ Also, memory modules that performed/controlled training sequences existed at the time of Hazelzet. (See Ex. 2001 at ¶¶ 74-75; Ex. 2004 at [0023]- [0034], Figures 4-6 (describing memory modules with “built-in self test (BIST)” that “can initiate test sequences.”)). Yet Hazelzet does not include such memory buffers with training sequences in its invention. Rather, Hazelzet teaches that its invention meets *all* the alleged needs it identifies (*without* data buffers or training), and provides no motivation at all to POSITA to implement features that would only add complexity and costs to its memory system. Indeed, Dr. Alpert seems to agree. When Dr. Alpert was asked whether Hazelzet needs training between the memory interface and the memory modules, without any modification, Dr. Alpert testified that he was “not aware of any training that would be required.”

(Ex. 2023 at ~~285:20-286:1~~[285:20-286:1](#)).

[147.](#) ~~138.~~ Thus, in my opinion, the Petition failed to demonstrate that redesigning Hazelzet’s ECC/Parity register to accommodate *any* training in a new initialization mode would have been obvious, which must be first shown to even consider whether it would have been obvious to implement *the specific training* of JEDEC/Buchmann (as opposed to any other known training).

[148.](#) ~~139.~~ The Petition also failed to demonstrate that POSITA would have understood that there would have been a reasonable likelihood of success in modifying Hazelzet as the Petition contends in Grounds 1-3. The Petition makes unsubstantiated assertion that it “would have been well within the level of skill at the time” for POSITA to simply *further modify* Hazelzet’s ECC/Parity register to implement the alleged training in combination (Pet. at ~~37-38~~[35-36](#)) . These contentions do not alter my opinion that the Petition fails to demonstrate POSITA would have been motivated, or even understood how, to add the JEDEC or Buchmann training in Hazelzet as a new initialization mode.

b) JEDEC and Buchmann Provide No Motivation To Add Training to a System Like Hazelzet’s

[149.](#) ~~140.~~ In my opinion, there is no teaching in JEDEC that would have suggested or motivated POSITA to add the training described in JEDEC to other memory systems like Hazelzet. Rather, JEDEC describes a training sequence to be used in LR-DIMM DD3 memory systems. (Ex. 1015 at 1). POSITA reading JEDEC

would understand it is proposing certain specifications for memory

systems that *already use* LR-DIMM DD3. This would not itself provide motivation to add training to other systems, like Hazelzet, which increases costs and reduces efficiency. Particularly when the training disclosed in JEDEC is specific to the memory system architecture described in JEDEC (LR-DIMMs), and not necessarily applicable to other memory system architectures, like Hazelzet that uses RDIMMs in the memory subsystem.

[150.](#) ~~141.~~ Buchmann also would not have provided any motivation to POSITA to add Buchmann's training sequences to Hazelzet memory system. POSITA would have understood that Buchmann's memory system architecture requires the use of a "handshake" between the memory controller and the memory subsystem during training, which is not required in an RDIMM system like Hazelzet. POSITA would have understood that this training, specific to Buchmann, would have introduced an inefficient use of time and resources, particular if attempting to use Buchmann's training in a memory system that does not require training specific for a memory subsystem (like Hazelzet). (Ex. 1016 at 6:59-62). Further, Buchmann teaches that the system cannot enter training during run-time; otherwise, the training would result in any error. (Ex. 1016 at 5:61-63) ("Entering TS0 using SBC during run-time will result in a downstream CRC error. This will cause the MB chip to enter the error recovery state (ERS).").

[151.](#) ~~142.~~ Therefore, in my opinion, POSITA would have understood that

Buchmann discloses an inherent inefficiency in Buchmann's training, which is addressed for Buchmann's memory architecture, but is not related to Hazelzet's memory system, in that the system must wait for a signal from the training module to confirm that training is complete.

3. POSITA Would Not Have Been Motivated to Add *the Specific Training of JEDEC/Buchmann*

a) Problem and Solution Taught in Hazelzet

[152.](#) ~~143.~~ The Petition appears to identify an alleged problem with Hazelzet related to errors in data between a host system and a memory module. (Pet. at 24-25). This is not an accurate characterization of Hazelzet after reading its entire disclosure. In reality, a POSITA would have understood that Hazelzet focused on providing a cost-sensitive solution for optimizing performance and reliability. (Ex. 1014 at [0001]-[0014]). Unlike the Petition's and Dr. Alpert's characterization, Hazelzet did not focus myopically on a system's reliability to the detriment of its performance, capacity or cost considerations. Instead, as discussed above, Hazelzet sought a solution that would strike a balance, for low-end and midrange systems ("reduced function" systems having an "adequate level of asset- protection"), between performance, reliability, capacity (i.e., density) and cost. (Ex. 1014 at [0001]-[0014]). Hazelzet identified this, and a POSITA would understand, as being a problem overlooked by the industry. (Ex. 1014 at [0001]-[0014]).

[153.](#) ~~144.~~ The Hazelzet reference contemplated numerous, different solutions

to this problem including: “memory mirroring, symbol slicing and extensive forms of fault rejection and redundancy” as well as “error detection and/or correction methods such as CRC (Cyclic Redundancy Code), EDC (Error Detection and Correction), parity or other encoding/decoding methods suited for this purpose” and “further reliability enhancements [that] may include operation re-try (to overcome intermittent faults such as those associated with the transfer of information), the use of one or more alternate or replacement communication paths to replace failing paths and/or lines, complement-re- complement techniques” and “the use of bus termination, on busses as simple as point-to-point links or as complex as multi-drop structures” (e.g., a system like Buchmann’s), which “is becoming more common consistent with increased performance demands.” (Ex. 1014 at [0005], [0127], [0128]). Ultimately, based on performance, capacity, cost, and reliability considerations, Hazelzet chose to implement a hybrid solution focused on error code correction (“ECC”) functionality that allows a memory module system to perform normal operations in conjunction with parity. (Ex. 1014 at [0016]). Hazelzet used parity to enhance a system’s performance and ECC to enhance its reliability, both of which applied to data transmissions that already occurred. Petitioner’s expert, Dr. Alpert, appears to agree. (Ex. 2003 (Alpert Deposition), 65:13-19). According to Hazelzet’s “present invention,” these features “eliminat[ed] the need [for] two types of buffer devices or to re-design existing memory modules.” (Ex. 1014 at [0014]).

154. ~~145.~~ Hazelzet makes no mention of training—even in its contemplated alternative solutions to the problem it identified (i.e., the appropriate balance of performance and reliability for low end memory systems). (Ex. 1014 at [0005], [0127], [0128]). Notwithstanding, Petitioner and Dr. Alpert allege that a POSITA would be motivated to add training—specifically, the alleged training disclosed in Buchmann and JEDEC—to Hazelzet. (Pet. at ~~32-40~~30-40), but as a POSITA I disagree.

155. ~~146.~~ A POSITA would not have been motivated to add Buchmann's or JEDEC's alleged training to Hazelzet. As a POSITA would have understood, Buchmann's and JEDEC's alleged training, in contrast to Hazelzet's chosen solution of ECC, are fundamentally different solutions to distinct problems in memory modules. As I explain in further detail below, ECC uses an algorithm to correct errors in received data packets after the data has been transmitted. Buchmann's alleged training seeks to synchronize the timing of memory module communication to ensure error-free transmission of data packets via a high-speed link before the data is sent, while JEDEC's alleged training is meant to solve the timing issues related to the memory buffers in LR-DIMM, which are not present in Hazelzet. Put simply, ECC corrects data errors once they have occurred, and, in contrast, Buchmann's or JEDEC's alleged training is used to prevent timing errors from occurring before they do.

b) General Overview of ECC

[156.](#) ~~147.~~ A system implementing ECC leverages redundancies encoded in data packets to detect errors in transmitted data, and to apply a correcting algorithm to the corrupted data. Redundancy is used primarily for correcting “hard” errors in memory circuits to improve production yield. (Ex. 1014 at [0008], [0016]-[0022], [0035], [0038], [0041], [0042], [0044], [0059], [0063-64], [0069] & Figures 3A, 3B, 3C, 3D, 4A, 4B, 6; Ex. 2012 at 764). With error correction it is possible to detect and correct errors occurring either in manufacturing or in the field to “improve the reliability of the memory device in the system” as well as the yield. (Ex. 1014 at [0017], [0041], [0042]; Ex. 2012 at 765). Detecting and correcting errors can be used to give improvement in long term in-system yield. (Ex. 1014 at [0009], [0041], [0042]; Ex. 2012 at 765).

[157.](#) ~~148.~~ Generally, error correction involves two simple steps: first, an error must be detected, and, second, the error must be corrected. (Ex. 1014 at [0008]; Ex. 2012 at 765). The simplest method of error correction is a simple duplication of every bit in the array. (Ex. 1014 at [0005]; Ex. 2012 at 765). The drawback to this is that the chip size is increased. Different techniques can be deployed which take less area on the chip, though. (Ex. 2012 at 765). Hamming codes are frequently used for this purpose. (Ex. 2012 at 765). With Hamming codes, error correction can be performed on many different bit field sizes with the assistance of additional parity bits in the array. (Ex. 2012 at 765). There is a trade-off in that small bit fields

allow fast error detection but require a large number of extra parity bits in the memory matrix. (Ex. 2012 at 766). Large bit fields permit use of a smaller amount of extra matrix for the parity cells but error detection is slower. (Ex. 2012 at 766).

[158.](#) ~~149.~~ With single error correction, a memory word with one bad bit can be corrected to recover the original information, whereas two bad bits can be detected, but not corrected. (Ex. 1014 at [0016], [0028], [0035]; Ex. 2012 at 766). Error correction is useful in system not only to correct soft errors due to noise or alpha particle hits, but also for hard error correction. (Ex. 1014 at [0042]; Ex. 2012 at 766). A soft error can be corrected by reprogramming the bit. (Ex. 1014 at [0016]; Ex. 2012 at 766). A hard error is a “stuck at” failure. Since only one error in a word can be corrected, a system failure with error correction present occurs only if two errors occur in the same word. (Ex. 1014 at [0035], [0063]; Ex. 2012 at 766). This occurrence can be lessened by clearing the soft errors more frequently and by regularly replacing parts with hard errors. (Ex. 2012 at 766). For these reasons, ECC is an effective way to reduce and eliminate soft and hard errors in memory systems in order to improve the reliability of data being communicated. (Ex. 1014 at [0004], [0008], [0009]).

c) General Overview of Training

[159.](#) ~~150.~~ Timing uncertainty is a challenge—separate from the existence of soft and hard errors in memory systems that can be resolved via ECC—related to data capture and processing in memory systems. (Ex. 1016 at 1:46-48; Ex. 2011 at

195). POSITA would understand that this would exist in Buchmann's high speed link or JEDEC's memory buffers [because in those systems—unlike Hazelzet—the memory devices are hidden from the memory bus behind a buffer](#). (Ex. 1015 at 8-9; Ex. 1016 at 5:40-50).⁵ It is related to data capture and processing, which is a different problem than Hazelzet attempted to resolve. In operation, a clock path that runs between the clock pads and capture latches may include a clock receiver, timing adjust circuits, and a clock distribution network (or clock tree). (Ex. 1015 at 8-9; Ex. 1016 at 7:15-24; Ex. 2011 at 195). Data, command, and address paths, on the other hand, may be much shorter and only include input buffers. (Ex. 2011 at 195). With different electrical lengths, the input paths are no longer source synchronous internally. (Ex. 2011 at 195).

~~151.~~ Furthermore, process, voltage and temperature (PVT) variations introduce excessive jitter, and even post-production trimming may not be sufficient as the timing margin shrinks. (Ex. 2011 at 195). Aligning the clock with data, command and address helps to ensure synchronous communication. One way to retain the clock and data relationship is by matching the routing all the way from the pads to the capture points. (Ex. 2011 at 195). On-chip, closed-loop synchronization or input path “de-skewing” is another approach. (Ex. 2011 at 195). For instance,

⁵ Hazelzet, which does not buffer the data lines, has less complicated timing issues compared to the JEDEC and Buchmann memory systems. Therefore, a POSITA would not have been motivated to implement the data line training that JEDEC and Buchmann implement to address the timing of those memory systems.

data training, either in relation to a host memory controller or conducted inside the DRAM itself, can improve the capture timing or ensure reliable data capture over PVT variations. (Ex. 2011 at 195).

d) General Differences Between ECC and Training

[160.](#) ~~152.~~ Training is a solution to a different problem than that addressed by ECC. Training seeks to pre-emptively ensure reliable performance of a memory module. From the perspective of the memory controller, each component on a memory module is a slightly different distance away, and each component takes a slightly different amount of time to perform an operation. Conventional memory modules include predetermined constants for timing that balance these concerns by erring on the side of allowing more time, and thus result in inefficiency. Training reduces the amount of time by synchronizing the data transfer to a clock signal. Thus, while training can improve a memory system's timing efficiency, training also increases the system costs and complexity to implement training.

[161.](#) ~~153.~~ ECC cannot, and does not, seek to optimize the timing of signals between memory controller and components on the memory module. ECC is used to correct errors in data packets by including redundant information in each data packet. Upon receipt of the data packets, an algorithm compares all the data to determine whether there are any errors, and if so, to use the redundant information to correct the errors.

[162.](#) ~~154.~~ At a high level, the shipment of a package from a shipping

company to a recipient is a useful analogy to highlight the differences between ECC and training. Training is used to determine when a package should be sent and received to ensure that the intended recipient is available to receive it. If it is sent too early or late, the intended recipient will not be home to receive it. Training makes sure that the shipping company sends the package at a time when the recipient is home. ECC, on the other hand, seeks to ensure that the right content is sent in the package, and, if not, resending the correct content. This is done without regard for when the package is sent. ECC ensures that, if a basketball is intended to be shipped, a basketball is ultimately shipped. If, instead, a football is shipped, ECC will correct the mistake and resend a package that includes a basketball.

4. There is No Motivation to Add Buchmann’s or JEDEC’s Alleged Training to Hazelzet for Multiple Reasons

[163.](#) ~~155.~~ All of Petitioner’s Grounds require Buchmann’s or JEDEC’s alleged training to be added to Hazelzet. (Pet. at ~~32-33~~[30-31](#)). Petitioner alleges that a POSITA “would have been motivated to add training to Hazelzet because it was known that training improved memory module reliability.” (Pet. at ~~35-36~~[34](#)). That is the only motivation Petitioner gives for why a POSITA would specifically—and to the exclusion of other choices—add Buchmann’s or JEDEC’s alleged training to Hazelzet. This single, conclusory statement fails to establish, with any particularity, why a POSITA would have specifically chosen Buchmann’s or JEDEC’s alleged training—as opposed to any other technique to improve memory module reliability,

including other training not specific to JEDEC or Buchmann—to add to Hazelzet, without hindsight teachings from the ‘~~218~~[595](#) Patent.

[164.](#) ~~156.~~ Petitioner and Dr. Alpert do not explain why a POSITA would have been motivated to add JEDEC’s or Buchmann’s training to Hazelzet beyond the generic, conclusory statement that all the references relate to “reliability.” (Pet. at 34-35). I understand this fails to satisfy a motivation to combine the references. Petitioner does not even attempt to analyze why a POSITA would be motivated to add training—to the exclusion of any other technique—to Hazelzet in order to “improve overall system reliability.”

[165.](#) ~~157.~~ A POSITA would understand that Hazelzet, itself, presents a different memory module from that of Buchmann or JEDEC, and aims to solve a different problem. Specifically, as discussed above, Hazelzet uses ECC to improve system reliability. In my opinion, this demonstrates that a POSITA would *not* be motivated to add training, because there is no teaching or suggestion of any other problems to be solved using training besides the alleged problem of “system reliability” which has already been resolved by ECC. In fact, different solutions to the same problem, like Hazelzet’s choice to use ECC instead of training, is further evidence of non-obviousness. This does not demonstrate obviousness or a motivation to add training to Hazelzet, let alone the specific type of training alleged to be disclosed in Buchmann or JEDEC. In fact, Hazelzet’s choice to use ECC to solve the only problem it presents, is further indicia of non-obviousness.

[166.](#) ~~158.~~ Discussed above, there are numerous options available to improve the “reliability” of a memory system—many of which are identified in Hazelzet (Ex. 1014 at [0005], [0127] and [0128]) and do not include training—but Petitioner states that training, alone, would be the obvious choice. As a POSITA I disagree and such a conclusory, unsupported statement does not demonstrate why a POSITA would have combined the elements from specific references in the way that the claimed invention does.

[167.](#) ~~159.~~ Here, Petitioners offer a cure (training) to an alleged problem (increased reliability) that has already been resolved (Hazelzet’s ECC). But even more egregious, Petitioner offers a cure (training) to a specific reliability problem (timing) that doesn’t even exist in Hazelzet—at least not until Petitioner itself modified Hazelzet to include buffering of the data lines that thereby introduces the problem JEDEC’s and Buchmann’s training are intended to solve. In my opinion, Petitioner’s motivation is backwards—Petitioner offers a cure to a problem that Petitioner introduces (by adding JEDEC or Buchmann memory buffers), not one that existed in Hazelzet to start. This does not demonstrate obviousness or a motivation to add training to Hazelzet, let alone the specific type of training alleged to be disclosed in Buchmann or JEDEC.

[168.](#) ~~160.~~ In my opinion, the conclusory testimony of Petitioner’s expert does not provide an articulated motivation to add Buchmann’s or JEDEC’s alleged training to Hazelzet either. (Ex. 1003 at Section IV.D).

5. Hazelzet, Buchmann and JEDEC Diverge from One Another—Petitioner’s Motivation to Combine Appears Based on What a POSITA *Could* Have Done, Not what a POSITA *Would* Have Done

[169.](#) ~~161.~~ As previously stated, Petitioner alleges that “a Skilled Artisan would have been motivated to add training to Hazelzet because it was known that training improved memory module reliability.” (Pet. at ~~35-36~~[34](#)). In my opinion this statement provides no reason for why a POSITA would be motivated to add Buchmann’s or JEDEC’s alleged training to Hazelzet, specifically. It simply states that training can improve memory module reliability. This is tantamount to saying that a POSITA would add Buchmann’s or JEDEC’s alleged training to Hazelzet because they *could* add training to Hazelzet. However, a POSITA would understand that Hazelzet identifies numerous, different improvements that a POSITA *could* implement to improve the “reliability” of its specific memory module including: “memory mirroring, symbol slicing and extensive forms of fault rejection and redundancy” as well as “error detection and/or correction methods such as CRC (Cyclic Redundancy Code), EDC (Error Detection and Correction), parity or other encoding/decoding methods suited for this purpose” and “further reliability enhancements [that] may include operation re-try (to overcome intermittent faults such as those associated with the transfer of information), the use of one or more alternate or replacement communication paths to replace failing paths and/or lines,

complement-re- complement techniques” and “the use of bus termination, on busses as simple as point-to-point links or as complex as multi- drop structures” (e.g., a system like Buchmann’s), which “is becoming more common consistent with increased performance demands.” (Ex. 1014 at [0005], [0127], [0128]). But, what a POSITA theoretically *could have* done does not demonstrate, particularly without any other evidence, what a POSITA *would have* been motivated to do.

[170.](#) ~~162.~~ Petitioner ignores the fact that the teachings of Hazelzet diverge from Buchmann’s and JEDEC’s alleged training. As explained earlier, ECC and training are different solutions to different problems. *See* Section IX.B.3. Moreover, Hazelzet identifies numerous, different improvements that a POSITA could implement to improve “reliability” of its system—none of which include training. (Ex. 1014 at [0005], [0127], [0128]). Unlike the ‘~~218~~[595](#) Patent, which chose training as a method to improve system reliability, Hazelzet chose ECC after contemplating numerous other techniques—none of which involved training. Accordingly, Hazelzet’s teaching would lead a POSITA on a path that diverges from the one taken by the ‘~~218~~[595](#) Patent.

C. There is No Motivation to Use Hazelzet's UE Line (Open Drain) to Communicate Training Signals During Initialization

[171.](#) ~~163.~~ Petitioner’s Grounds require that a POSITA would have found it obvious to (1) redesign Hazelzet’s memory module to add a new memory buffer that buffers data signals in addition to address and control signals, then (2) add the kind

of alleged training in JEDEC or Buchmann to Hazelzet in an entirely new mode during initialization that is separate from Hazelzet's normal mode of operation, *and then* (3) utilize Hazelzet's premodified UE line. (Pet. at ~~32-42~~[30-40](#)). The Petition alleges "[i]t would have been further obvious to communicate training status in an initialization mode using the same open drain output already used in other modes/operations." (Pet. at ~~40~~[38](#)). However, Petitioner provides no articulated reason why a POSITA would have been motivated to use Hazelzet's open drain UE line, specifically, as opposed to any other communication line of Hazelzet "used in other modes/operations." (Pet. at ~~40-42~~[38-40](#)). Instead, Petitioner makes a number of generic statements related to a POSITA's ability to utilize an open drain output for multiple purposes. (Pet. at ~~40-42~~[38-40](#)). This amounts to a contention that a POSITA *could* have, not *would* have, used an open drain for multiple purposes. As explained further below, Hazelzet teaches away from using its UE to output during initialization, which is when Petitioner argues the new training would occur, but instead Hazelzet expressly teaches to use a bus (not an open drain).

[172.](#) ~~164.~~ Further, none of the references that the Petition or Dr. Alpert cite describe *why* a POSITA should use an open drain, specifically, as opposed to any other line of communication, to communicate training status during an initialization mode (or any other mode of operation). The Petition and Dr. Alpert cite Hazelzet

(Ex. 1014), Kim (Ex. 1017) and James (Ex. 1043)⁶ as alleged support for the contentions that “a Skilled Artisan would have been motivated to arrange the modified Hazelzet to communicate signals indicating training completion only when all memory modules have completed that training, in order to ensure that the entire memory system had been trained before proceeding to normal operation,” and that a “Skilled Artisan would have been further motivated to modify Hazelzet as described above because Hazelzet’s memory system includes multiple memory modules in need of training,” and the “combinations analyzed here would therefore allow any module in the system to pull the open drain pin to ‘low’ (i.e. to ground) while still executing its training sequence, regardless of whether other modules in the system have completed training and were no longer pulling that pin low, thereby delaying normal operations until the system is completely ready.” (Pet. at 42) (citing Ex. 1043 at 7:30-51 (not a reference in any of the Grounds); Ex. 1017 at Figure 4, 5:65-6:12 (cited in only Ground 3); Ex. 1014 at [0018], [0109]). But none of these references actually disclose or suggest to a POSITA to use an open drain, specifically, to communicate training status during an initialization mode, and do not disclose the novel arrangement claimed in the ‘~~218~~[595](#)’ patent. For example, James (Ex. 1043; not a reference in any of the Grounds) states that normal operation cannot start until all the receivers are synchronized; but, James does not describe

⁶ Neither Kim (Ex. 1017), nor James (Ex. 1043), are references cited in Grounds 1 or 2;

anything about open drain communication. (Ex. 1043 at 7:30- 51). Kim (Ex. 1017; cited in only in Ground 3) teaches an open drain configuration for sending signals from multiple DIMMs on a single open drain line (errorout); but, the error out signal may go direct to the memory controller or be sent through a hub or some other buffer (at which point it would no longer be an open drain signal). (Ex. 1017 at Figure 4; 5:65-6:12). Hazelzet teaches that the UE error line can be an open drain and shared by multiple modules (Ex. 1014 at [0018],[0109]); but, as discussed below, Hazelzet does not teach training and, importantly, Hazelzet uses a bus—not the UE line—during initialization. None of the references relied upon by the Petition and Dr. Alpert disclose or teach using an open drain signal as a training signal of any kind.

[173.](#) ~~165.~~ Instead, the only reference cited by Petitioner or Dr. Alpert that actually teaches and would have motivated a POSITA to use an open drain to provide a signal associated with training sequences is the '~~218~~[595](#) Patent, which the Petition and Dr. Alpert repeat. (Pet. at ~~42~~[40](#); see Ex. 1001 at 2:49-62; 3:59-4:12; 7:66-8:29; 8:30-39; 8:45-61; 9:55-67; 10:11-20; 33-46; 11:26-31).

1. Hazelzet Teaches Away from Using Its UE Line During Initialization

[174.](#) ~~166.~~ According to the Petitioner, because “Hazelzet uses the same open drain output, UE 121, to indicate an ‘uncorrectable error’ in ECC mode and parity error in parity mode,” it would have been obvious “to use that same output in the

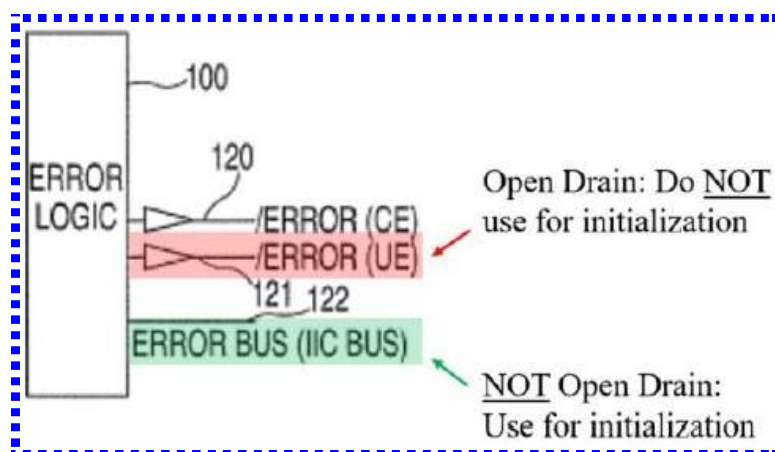
James (Ex. 1043) is not a reference cited [in](#) any of the Grounds.

added training mode/operation” since “those modes would not be using the open drain outputs while the training operation was running during initialization.” (Pet. at ~~40-41~~[38-39](#)). In my opinion, Petitioner’s argument is deficient for several reasons.

[175.](#) ~~167.~~ First, training status is not an “error” and thus not an analogous signal to Hazelzet’s UE line signals. Second, Petitioner ignores, and does not consider, that there would be a number of other unused pins available while Petitioner’s theoretical Hazelzet/JEDEC or Hazelzet/Buchmann training operation would be running during initialization. Hazelzet has a total of 276 pins “for electrically connecting the external circuitry to the SDRAMs in a direct or indirect manner.” (Ex. 1014~~-at~~[. 1](#), [0015], Figures 7A-7C). That Hazelzet’s UE line is used in both ECC and parity is not itself a motivation, teaching or suggestion to use that specific output in a new “added training mode/operation.” Just because POSITA could use the UE line, does not mean POSITA would have been motivated to use it. In my opinion, POSITA would not have been motivated to use Hazelzet’s UE line for any training signals during initialization because Hazelzet used a bus for those initialization signals.

[176.](#) ~~168.~~ Hazelzet discourages use of its UE (open drain) pin during initialization. Instead, Hazelzet discloses initialization that utilizes a bus that is distinct from the UE during initialization. (Ex. 1014, [0123]-[0125]). Specifically,

Hazelzet teaches that “[i]n one embodiment, the high speed bus may be used to complete the initialization of the memory subsystem(s),” e.g., the Error Bus 122. (Ex. 1014 at [0123]). Hazelzet further teaches a POSITA to use “a distinct bus, such as a *presence detect bus* (such as the one defined in U.S. Pat. No. 5,513,135 to Dell et al., of common assignment herewith), an *IIC bus* (such as defined in published JEDEC standards such as the 168 Pin DIMM family in publication 21-C revision 7R8) and/or the *SMBUS*, which has been widely utilized and documented in computer systems using such memory modules.” (Ex. 1014 at [0124]). Both examples, which are the only examples of initialization that Hazelzet provides, Hazelzet teaches the use of a bus—not the UE line—for initialization. Accordingly, Hazelzet teaches the use of bus (such as an IIC bus) for initialization and not use of its UE pin. Such a bus is depicted in Figure 4B of Hazelzet (annotated green), which is separate and distinct from the UE line (annotated red):



(Ex. 1014 at Figure 4B) (annotated).

[177.](#) ~~169.~~ With respect to the Petition’s (and Dr. Alpert’s) contention that a POSITA would have been motivated to use Hazelzet’s UE line in order to utilize the same pin for multiple uses (Pet. at ~~41~~[38-39](#)), Hazelzet expressly teaches the benefits of using a bus instead:

The use of a separate bus... also offers the advantage of providing an independent means ***for both initialization and uses other than initialization***, such as described in U.S. Pat. No. 6,381,685 to Dell et al., of common assignment herewith, including changes to the subsystem operational characteristics on-the-fly and for the reporting of and response to operational subsystem information such as utilization, temperature data, failure information or other purposes.

(Ex. 1014 at [0125]). In other words, Hazelzet expressly teaches to reuse its IIC bus (or another bus)—not its UE—for different functions while in either its normal mode of operation (ECC and parity) *and/or* during initialization; Petitioner argues that the alleged training that would be added to Hazelzet would be added to Hazelzet’s initialization.

[178.](#) ~~170.~~ Thus, *even if* a POSITA would have been motivated to add training during initialization in Hazelzet (whether JEDEC’s, Buchmann’s or any other training)—which as discussed above a POSITA would not—Hazelzet teaches away from using the UE line and to instead use a bus for initialization in order to “connect[] to one or more modules within a memory system” thereby “providing an independent means of interrogating memory subsystems, programming each of the one or more memory subsystems to operate within the overall system environment,

and adjusting the operational characteristics at other times during the normal system operation based on performance, thermal, configuration or other changes desired or detected in the system environment.” (Ex. 1014 at [0124]). Hazelzet not only teaches use of a bus during initialization, but it also describes the advantages of doing so, thereby expressly teaching away from using its UE line for training during initialization.

[179.](#) ~~171.~~ Not only does Petitioner fail to muster an argument as to why POSITA would be motivated to use Hazelzet’s UE line for training outputs during initialization, such an argument is contrary to the teachings of Hazelzet because Hazelzet expressly teaches utilizing the IIC bus (or another bus) during initialization for numerous perceived benefits and advantages. (Ex. 1014 at [0124]-[0125]). Accordingly, a POSITA would not be motivated to use Hazelzet’s UE to communicate training status as Petitioner suggests in conclusory fashion. A POSITA would have been motivated to reuse Hazelzet’s IIC bus (or another bus) if adding training to an initialization mode.

2. Buchmann Also Teaches Away from Using Hazelzet’s UE Line for Training During Initialization

[180.](#) ~~172.~~ Buchmann also expressly discloses communicating training signals over a bus—not its UE line or an open drain output.

[181.](#) ~~173.~~ The Petition (and Dr. Alpert) contend that Buchmann “discloses executing training sequences in SBC mode.” (Pet. at ~~30~~[28](#); Ex. 1003 at ¶ ~~130~~[151](#))

(“Buchmann discloses executing training and/or initialization sequences in its ‘SBC mode’”). Dr. Alpert provides examples of Buchmann’s training and/or initialization sequences in SBC mode as including TS0 and TS3 training sequences. (Ex. 1003 at ¶ ~~130~~[151](#)). The Petition and Dr. Alpert then contend it would

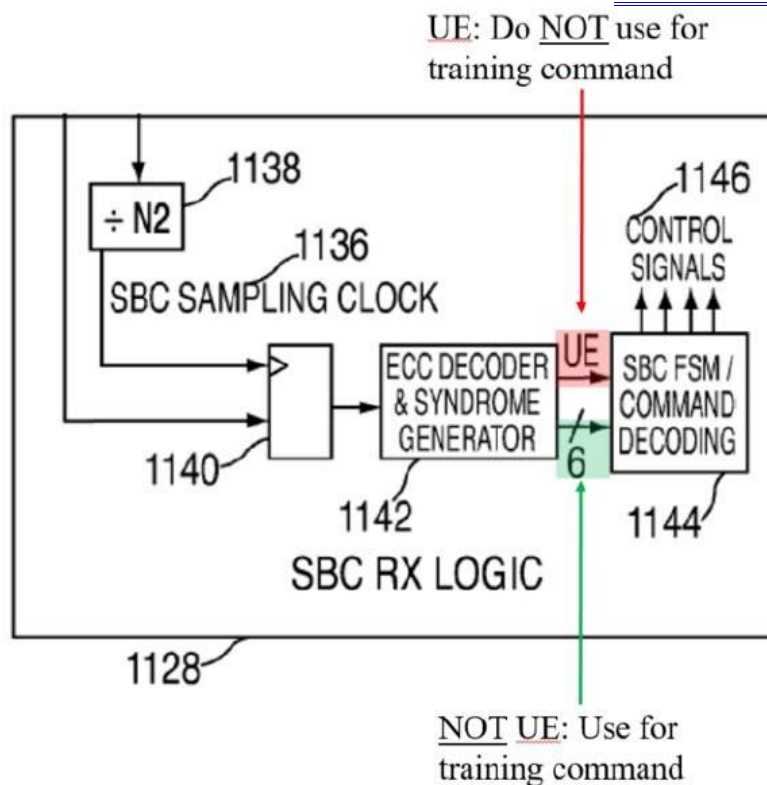
have been obvious to a POSITA to output Buchmann's TS commands (specifically, TS0_done, TS3_ack, and TS3_done) via Hazelzet's UE line in order to satisfy the claimed "associated with the one or more training sequences" and "wherein the module controller is further configured to drive a notification signal associated with the one or more training sequences." (Pet. at ~~32-33, 40-42, 54-55~~[30-32, 38-40, 52-53](#)).

[182.](#) ~~+74.~~ Buchmann does have a UE line; however, Buchmann does *not* send its TS/SBC commands over it, which Dr. Alpert appears to have admitted during depositions in this and a prior IPR. (Ex. 2003-~~at~~[, 106:20-107:11; 108:6-14; 124:17- 19; Ex. 2023-~~at~~\[, 269:6–270:22\]\(#\)](#)). Moreover, unlike Hazelzet, Buchmann's UE line is *not* even an open drain output. (Ex. 1016 at Figure 11). Even further, Buchmann's UE line is not even an *output* as any commands on the UE line are sent to the "SBC FSM/command decoding logic 1144" within the same "SBC receiver logic 1128" component. (Ex. 1016 at Figure 11; 16:3-29).

[183.](#) ~~+75.~~ Instead, Buchmann sends its TS/SBC commands via separate bus. (Ex. 1016 at Figure 11). Indeed, Petitioner's expert Dr. Alpert testified that Buchmann's UE line does not communicate Buchmann's training commands (TS/SBC commands). (Ex. 2003 at 106:20-107:11; 108:6-14; 124:17-19; Ex. 2023 at 269:70–270:22). Dr. Alpert confirmed (in a prior related IPR (IPR2018-00303)) that Buchman sends its training commands (TS/SBC commands) via a bus. (Ex. 2003, 108:6-14 ("that bus with six lines would carry the SBC command")). Dr.

Alpert confirmed his same understanding during deposition in this IPR (Ex. 2023 at 269:6–16) (“Q. And TS_done and TS3_ack are in Table 5? A. They are, yes. Q. And those signals are communicated by the SBC commands of Buchmann, correct? A. That's correct, yes.”)

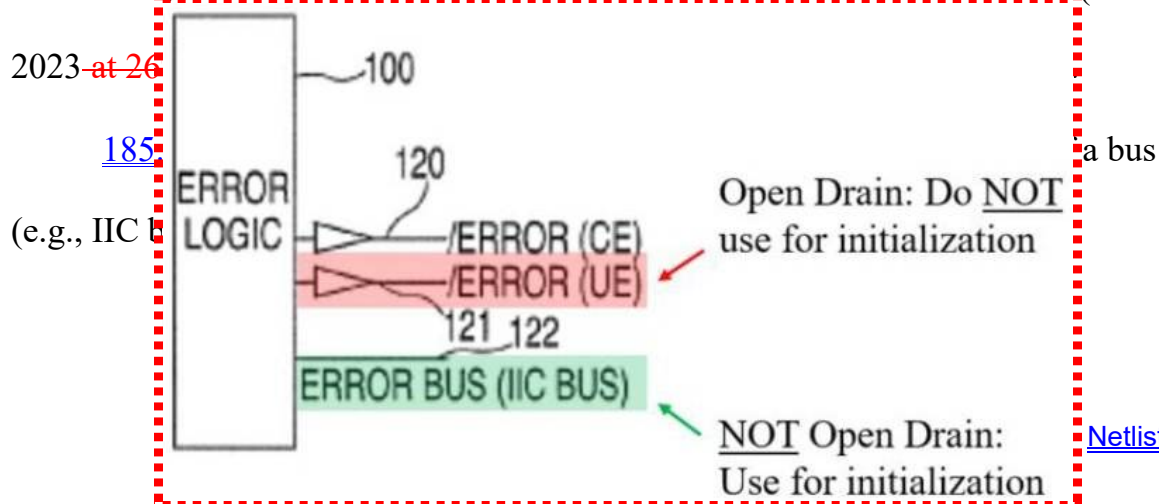
[184.](#) ~~176.~~ Dr. Alpert also explained why Buchmann sends its training signals via a bus—and not over the UE line. Specifically, Buchmann’s SBC training commands are 6-bits (Ex. 1016 at 18:66-19:14, Table 11), and thus, the “bus with six lines would carry the SBC command.” (Ex. 2003 at 102:2-4; 108:6-14). In contrast, the UE line is only a one bit signal. (Ex. 2003 at 108:15-109:2). Therefore, as confirmed by Petitioner’s expert Dr. Alpert, Buchmann’s UE line does not output Buchmann’s training commands. (Ex. 2023 at 270:4-22) (“Q. And, in Figure 11, there's also a line above the line with the / 6 that has a UE over it. · You see that? A. Yes, I do. Q. The SBC commands in Buchmann are not sent on that line, correct? A. Yes, I believe that's correct.”) As such, Figure 11 of Buchmann depicts its UE line (annotated red), which does not send training commands, and the separate bus (annotated green), which does communicate training commands:

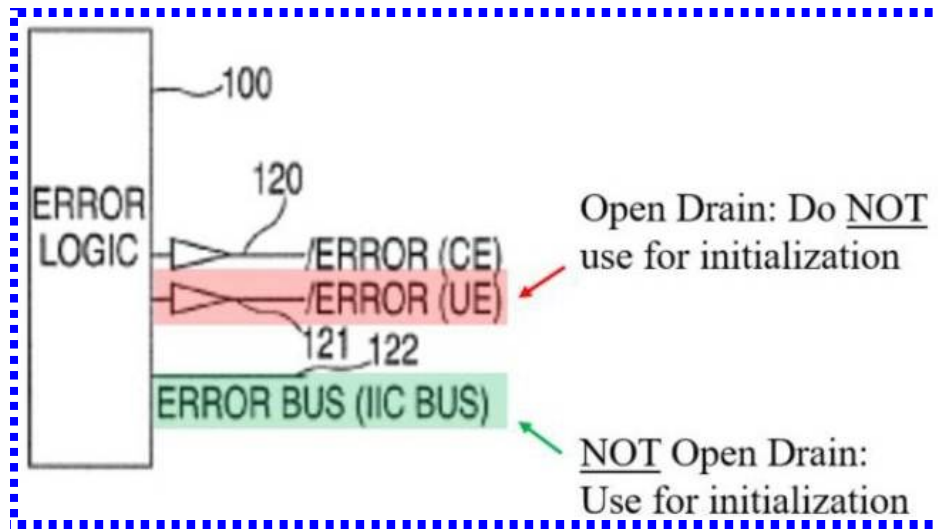


(Ex. 1016 at Figure 11) (annotated). As Dr. Alpert explains, Buchmann’s training signals are output via a bus—and not over the UE line—for good reason.

Buchmann’s SBC training commands are six-bits, and thus, the “bus with six lines would carry the SBC command.” (Ex. 2003-at, 102:2-4; 108:6-14; *see also* Ex. 1016 at, 18:66-19:14, Table 11). On the other hand, the UE line is only a one-bit signal.

(Ex. 2003-at, 108:15-109:2). Thus, as Dr. Alpert confirmed, Buchmann’s training commands, which are sent as SBC commands, are not sent on the UE line. (Ex.





(Ex. 1014 at Figure 4B). Accordingly, both Buchmann and Hazelzet disclose teachings that diverge from the ‘[218595 Patent](#)’ claims. Both Buchmann and Hazelzet teach sending signals during initialization using a bus—not their UE—and Hazelzet *explains why* to use the bus. The modification and combination proposed by the Petition do not make the ‘[218595](#)’ claims obvious; they actually teach away from the ‘[218595](#)’ claims.

[186.](#) ~~478.~~ It is also worth noting that Petitioner’s expert, Dr. Alpert, previously stated that Buchmann’s TS3 commands “wouldn’t necessarily be a very appropriate command” for Hazelzet. (Ex. 2003 at 121:6-15). I agree. Not only does Hazelzet not have the same “cascaded connection that is shown in Buchmann’s embodiments” (as Dr. Alpert explained, Ex. 2003 at 121:6-15), but as discussed above, Buchmann’s TS/SBC commands are 6-bits sent in parallel, and therefore cannot be sent over a 1-bit UE line (both Hazelzet’s and Buchmann’s UE

line is a 1-bit signal). The Petitioner and Dr. Alpert make no attempt in the Petition to explain why Buchmann's TS3 commands would be a good fit now, and make no attempt to explain why Buchmann's TS0 commands—or any other TS command for that matter—are actually appropriate for inclusion in Hazelzet. Dr. Alpert did not know the significance of Buchmann's particular TS3 commands when previously making the same combination of Hazelzet and Buchmann. (Ex. 2003-at, 103:3-11) (Q Okay. Let me come back to that passage that you just read, but for now focusing on table 11, is there a reason that Buchmann utilizes 6 bits for the training commands that are shown in table 11? A I don't recall a particular significance to the 6 bits for this embodiment.). Dr. Alpert also previously testified

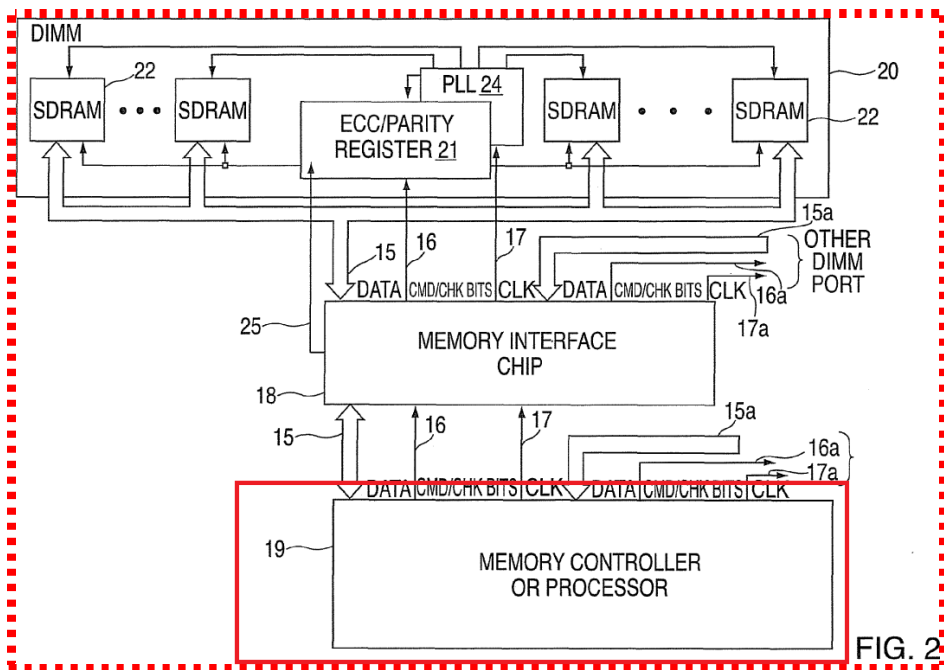
that there are many ways Buchmann’s six-bit message could be implemented in Hazelzet, and his only rationale for adding it to Hazelzet’s UE line was that he “d[id]n’t see a reason why the UE line couldn’t be used for that purpose.” (Ex. 2003 at 126:15-24). And even then, Dr. Alpert admitted that to do so, one would also have to further change Buchmann to communicate the six-bit training signals serially, as opposed to in parallel as actually described in Buchmann. (Ex. 2003 at 104:5-11) (“I don’t believe this would be showing a serial path for transmitting the 6 bits of commands.”). This is also contrary to the patent’s description of the notification signal being either high or low to notify training completion—not a serial transmission. These ~~contentions~~contention are conclusory, contradicted by Dr. Alpert’s repeated testimony.

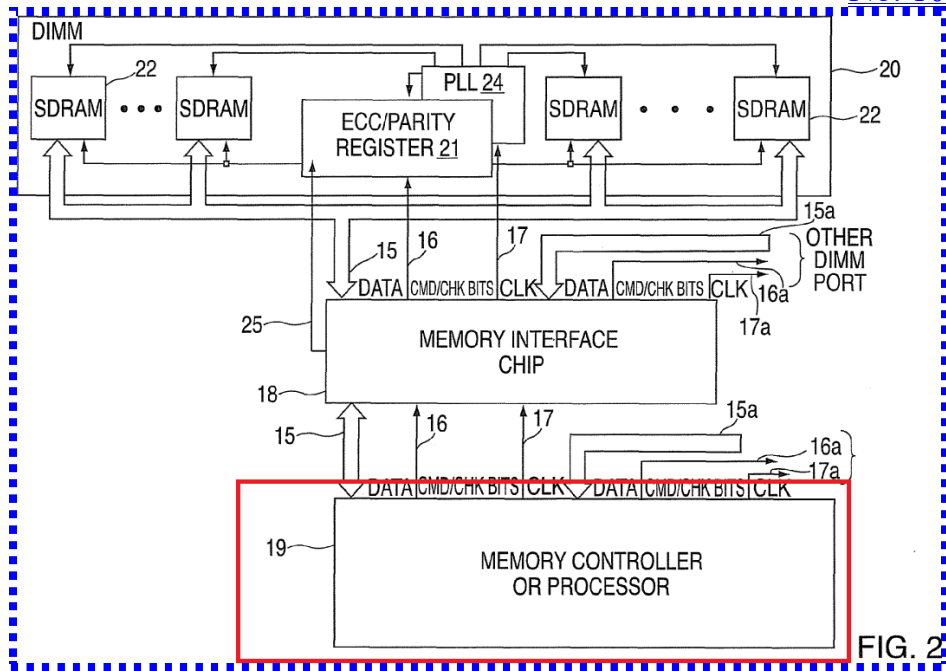
3. JEDEC is Consistent with Hazelzet’s Teachings to Use the Bus, and Provides No Motivation to Use Hazelzet’s UE Line for Training

187. ~~179.~~ Separately, even if combining Hazelzet with JEDEC, a POSITA would not have implemented a notification signal associated with a training sequence via an open drain from a memory module controller (allegedly the ECC/Parity register of Hazelzet). This feature is required by all independent claims of the ~~218~~595 Patent (claim elements 1.i, 9.h, and 15.i, as identified in the Petition). Hazelzet and JEDEC would have taught POSITA at least ways to

implement training in Hazelzet, neither of which are the feature claimed in the ‘~~218~~595 Patent.

188. ~~180.~~ First, even *if* JEDEC would have motivated POSITA to add training to Hazelzet, then POSITA would have known to use the existing components of Hazelzet’s memory system to implement that training (instead of changing Hazelzet’s architecture to include memory buffers that buffered data lines in order to conform to JEDEC’s particular training for LR-DIMMs). Dr. Alpert confirmed, of which I agree, that if POSITA would have implemented training in Hazelzet, POSITA would have used the memory controller (reference number 19) to do that training. (Ex. 2023 at 292:5-12).





(Ex. 1014 at Figure 2). Consequently, no notification signal from the DIMM (including from the ECC/Parity register) to the Memory Controller would be necessary because the Memory Controller itself would perform that training and know when training was completed, which Dr. Alpert appears to agree. (Ex. 2023 at 82:12-23, 292:5-12). Without modifying Hazelzet's ECC/Parity register to also buffer data signals, adding training would not require the novel notification from the memory buffer described in the '248,595 Patent claims, and Petitioner's combination of just adding training would not meet all the claims' limitations.

189. ~~181.~~ Second, even if JEDEC would have further motivated POSITA to add JEDEC's specific training to Hazelzet, then POSITA would **not** have used Hazelzet's UE line in the ECC/Parity register to output JEDEC's training notifications. Hazelzet expressly teaches away from doing this. Instead, Hazelzet

teaches initialization using a separate, distinct bus, like “an IIC bus (such as defined in published JEDEC standards...)” (Ex. 1014 at [0124]-[0125]) (describing the benefits of doing so, discussed above in Section ~~IV~~IX.C.1). Thus, because Hazelzet and JEDEC both include an IIC bus, and *Hazelzet* specifically teaches that JEDEC’s IIC bus should be used in *Hazelzet* initialization, POSITA would not have been motivated to implement JEDEC’s training notification signals during initialization via Hazelzet’s UE line. JEDEC does not describe any benefit or reason to communicate training status using an open drain output, and therefore, JEDEC would not have taught, suggested, or motivated POSITA to further modify Hazelzet to use Hazelzet’s UE output for training during initialization when Hazelzet already discloses, and teaches the benefits of, using a bus during initialization. (*See* Ex. 1015 at 1-9).

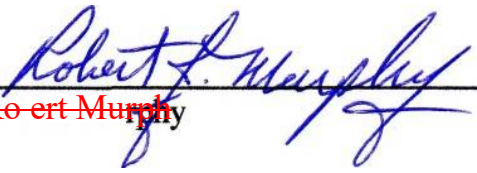
190. ~~182.~~ In addition, as discussed above (Section IX.A.1), Hazelzet’s memory module does not have memory buffers on the data lines—which would cause data timing issues and which would hide the memory devices, behind the memory buffer, from the memory bus—a problem JEDEC’s alleged training aims to address. Thus, a POSITA would not have been motivated to add JEDEC’s training to Hazelzet in the first place, let alone trying to perform JEDEC’s training in Hazelzet’s ECC/Parity register, which is where Hazelzet’s UE line resides. (Ex. 1014 at ~~Figures~~Figure 4A and 4B).

191. ~~183.~~ For at least these additional reasons, it is my opinion that a
POSITA would not have been motivated to implement JEDEC's training on
Hazelzet's UE line.

* * * * *

I, Robert J. Murphy, declare under penalty of ~~perjury~~[perjury](#) under the laws of the United States of America that the foregoing is true and correct. I hereby also declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that willful false statements and the like so made could jeopardize the validity of the patent at issue in this proceeding.

Executed on August [1](#), 2022


~~Robert Murphy~~
[Robert Mu](#)

~~114~~

[118](#)

ATTACHMENT A

Robert J. Murphy
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Los Gatos, California 95030
(408) 396-6098
murf@firenza-llc.com

Abstract: More than 47 Years of experience in management, design, hands-on development & debug of: High speed, high complexity, high density and high volume commercial semiconductor products including Full Custom Microprocessors, E²CMOS and BiCMOS PALs, CMOS and NMOS SRAMs, CCDs and RAD Hard SOS CMOS.

Vice President of Engineering **IC Manage, INC.**
1/21 - PRESENT **Campbell, CA.**

Responsible for all software engineering including development, applications engineering, testing and documentation for Integrated Circuit Revision Control & Cloud Computing Software.

Founder & Owner **Firenza, LLC**
4/98 - PRESENT **Los Gatos, CA.**

Founded company to respond to the growing needs of the semiconductor industry to license quality high performance building blocks for Semi-Custom and ASIC designs. Developed business plan, cultivated customers and managed the efforts of Design Professionals to deliver world class building blocks in 0.25u 0.18u, 0.13u, 65nM & 14nM processes. Provided circuit design reviews on 65 nM Major Microprocessor. Designed EFUSE circuit for another 65 nM Microprocessor. Debugged and provided layout based solutions for 65 nM process latch-up issue. Designed 28nM & 14nM SRAM circuits. Developed custom 10Ghz SRAMs IP Blocks for custom processor in 14nM process.

Performed Expert Witness work on the following cases:

NeoMagic Corporation v. Trident Microsystems, Inc.
D. Del., C.A. No. 98-699-RRM, Client: Trident, Year: 1999

Rambus, Inc. v. Infineon Technologies AG,
Infineon Technologies North America Corp.,
And Infineon Technologies Holding North
America, Inc.
Eastern D. Virginia, C.A. No. 3:00cv524, Client: Rambus, Year: 2001

Micron v, Rambus, Inc.
D. Del., C.A. No. 00-792-(RRM), Client: Rambus Year: 2001

Hynix Semiconductor Inc. et al. v. Rambus, Inc.
Northern D. Calif., Case No. CV 00-20905 RMW
Client: Rambus, Year: 2005

Career History for Robert J. Murphy (Cont'd)

Rambus, Inc. v. Hynix Semiconductor Inc. et al. Northern
D. Calif., Case Nos. C-05-00334, C-05-02298, C-06-00244,
C-00-20905 RMW, Client: Rambus Year: 2007

Toshiba v. Hynix International Trade Commission, Investigation No.
337-TA-592 Client: Toshiba Year: 2007

UniRAM Technology, Inc. v. MONOLITHIC SYSTEM TECHNOLOGY, TAIWAN
SEMICONDUCTOR MANUFACTURING COMPANY, LTD, & TSMC NORTH AMERICA Northern
D. Calif., Case No. CV-04-01268-VRW Client: UniRAM Year: 2008

Perego, et al. v. Drehmel, et al.
U.S.P.T.O., Patent Interference No. 105,467 (Bd. Pat, App.& Int.) Client:
Rambus Year: 2007

Reexamination proceedings involving various U.S. Patents in the Farmwald
/ Horowitz Family derived from Application No. 07/510,898 Client: Rambus
Year: 2011

Reexamination proceedings involving U.S. Patents #'s 7,210,016;
7,177,998, Client: Rambus, Year: 2009

Reexamination proceedings involving U.S. Patents #'s 7,287,119;
7,330,952; 7,330,953; 7,360,050; Client: Rambus, Year: 2010

Reexamination proceedings involving U.S. Patents #'s 7,287,109;
6,591,353; 6,470,405; Client: Rambus, Year: 2009

*In The Matter Of: CERTAIN MLC FLASH MEMORY DEVICES AND PRODUCTS CONTAINING
SAME*, International Trade Commission, Investigation No. 337-TA-683,
Client: BTG, Year: 2009

e.Digital Corporation v. Toshiba America Information Systems Inc.
Southern D. California, Case No, '13CV2909 BEN BGS, Client: Toshiba,
Year: 2013, Matter: Flash Memory File System in a Handheld Record and
Playback Device

*In The Matter Of: CERTAIN STATIC RANDOM ACCESS MEMORIES AND PRODUCTS
CONTAINING SAME*, International Trade Commission, Investigation No.
337-TA-792, Client: GSI Year: 2013

*In The Matter Of: CERTAIN WIRELESS COMMUNICATIONS EQUIPMENT AND ARTICLES
THEREIN*, International Trade Commission, Investigation No. 337-TA-866,
Client: Ericsson Year: 2013, Matter: Wireless Communication Equipment &
Power Supplies

Solid State Storage Solutions, Inc. v. STEC, INC., OCZ TECHNOLOGY, INC.,
CORSAIR MEMORY, TEXAS MEMORY SYSTEMS, INC., PNY TECHNOLOGIES, INC.,
PATRIOT MEMORY LLC, FUSION-IO, INC., OTHER WORLD COMPUTING, INC., and
MUSKIN, INC. Eastern D. Texas, Case No. 2:11-cv-00391- JRG-RSP,
Client: Solid State Year: 2012

GSI Technology, Inc. v. UNITED MEMORIES INC. and INTEGRATED SILICON
SOLUTION, INC., Northern D. Calif., Case No. 13-cv-1081-PSG Client: GSI
Year: 2015, Matter: Static RAM Memory Devices & Features

Career History for Robert J. Murphy (Cont'd)

GSI Technology, Inc. v. CYPRESS SEMICONDUCTOR CORP.
Northern D. Calif., Case No. 5:11-cv-03613-EJD Client: GSI, Year: 2015,
Matter: Static RAM Memory Devices & Features

CYPRESS SEMICONDUCTOR CORP. v. GSI Technology, Inc.
Northern D. Calif., Case Nos. 3:13-cv-02013-JST (JCS), 4:13-cv-03757-JST
(JCS), Client: GSI, Year: 2015, Matter: Static RAM Memory Devices &
Features

Petition for *Inter Partes* Review involving U.S. Patents nos. 6,292,403
(Case IPR2014-00121) and 6,069,839 (Case IPR2014-00202),
Client: GSI, Year: 2015, Matter: Static RAM Memory Devices &
Features

Petition for *Inter Partes* Review involving U.S. Patent no. 6,058,045
(Case IPR2014-00113), Client: Toshiba, Year: 2015, Matter: DRAM
Memory & Features for Display Operations

Petition for *Inter Partes* Review involving U.S. Patent no. 5,687,132
(Case IPR2014-00317), Client: Toshiba, Year: 2015, Matter: DRAM
Memory & Features for Display Operations

*In The Matter Of: CERTAIN INTEGRATED CIRCUITS AND PRODUCTS
CONTAINING THE SAME, U.S. ITC Inv. No. 337-TA-920,*
Client: Freescale, Year: 2014, Matter: Circuitry for timing operations
within memory circuits and to bond pad structures and layouts used on
integrated circuits.

Freescale Semiconductor, Inc. v. MediaTek Inc., et al., Northern D.
of California, Case No. 5:14cv02185BLF, Client: Freescale, Year: 2014,
Matter: Circuitry for timing operations within memory circuits and to
bond pad structures and layouts used on integrated circuits.

Petition for *Inter Partes* Review involving U.S. Patent no. 5,500,819
(Case IPR2014-00418), Client: Toshiba, Year: 2015, Matter: DRAM
Memory & Features for Display Operations

Intellectual Ventures I LCC et al. v. Toshiba Corporation et al. D,
Del., C.A. No. 13-453-SLR-SRF, Client: Toshiba, Year: 2017, Matter:
DRAM Memory & Features for Display Operations

*In The Matter Of: CERTAIN MEMORY MODULES AND COMPONENTS THEREOF, AND
PRODUCTS CONTAINING SAME, U.S. ITC Inv. No. 337-TA-1023,*
Client: Netlist, Year: 2017, Matter: Features of DRAM Memory Modules

Petition for *Inter Partes* Review involving U.S. Patent no. 8,489,837
(Case IPR2017-00548), Client: Netlist, Year: 2017, Matter: Features of
DRAM Memory Modules

*In The Matter Of: CERTAIN MEMORY MODULES AND COMPONENTS THEREOF, U.S.
ITC Inv. No. 337-TA-1089,* Client: Netlist, Year: 2018, Matter: Features
of DRAM Memory Modules

Petition for *Inter Partes* Review involving U.S. Patent no. 9,535,623
(Case IPR2018-00303), Client: Netlist, Year: 2018, Matter: Features of
DRAM Memory Modules

Career History for Robert J. Murphy (Cont'd)

PHENIX LONGHORN, LLC v. WISTRON CORP. et al.
Eastern D. Texas, Case No. 2:17-cv-000711-RWS, Client: Phenix, Year:
2018, Matter: Gamma Reference Generator for Monitors & Televisions

Petition for *Inter Partes* Review involving U.S. Patent no. 7,233,305
(Case IPR2018-01255), Client: Phenix, Year: 2018, Matter: Gamma
Reference Generator for Monitors & Televisions

PHENIX LONGHORN, LLC v. TEXAS INSTRUMENTS INC.
Eastern D. Texas, Case No. 2:18-cv-00020-RWS, Client: Phenix, Year:
2018, Matter: Gamma Reference Generator for Monitors & Televisions

Petition for *Inter Partes* Review involving U.S. Patent no. 6,651,134
(Case IPR2020-01492), Client: Qualcomm, Year: 2020, Matter: DRAM
Memory Device with Fixed Burst Length

Director of Engineering
6/92 - 4/98

Silicon Graphics Inc.
Mountain View, CA.

Beast Program: Hired, managed and directed circuit designers on this 500 MHz design. Responsible for the scheduling and design reviews for all custom circuit design on the chip. Supported CAD tool development with test structures, test cases and debug.

T5 (R10000) Program: Assisted in the final completion of this processor. Took my team of people down to the project in it's late stages and managed 10% of the Units (3) on the chip. Was a key member of the schedule review team.

TFP (R8000) Program: Managed the design and implementation of the Floating Point Chip for SGI's POWER CHALLENGE systems. Directed the re-design of a large Tag Ram done for SGI by Toshiba. Managed a group of Toshiba's engineers in the US and interacted with their counterparts in Japan to debug and repair the design. The repaired design was fully functional with speeds of 110 MHz.

The redesign was accomplished while holding 16 lots of silicon in the fab. All of the lots were saved and parts delivered to SGI on time.

Major accomplishments included:

- * Hired over 20 people.
- * Managed a total team of 30 people.
- * Developed extensive relationships with our Japanese Partners.
- * Hired contractors as needed for specific expertise

- * Directed the development and implementation of world class PLL designs onto the whole SGI campus.
- * Developed internal circuit design resources via training and assignment selection.

Director of Engineering
2/89 - 6/92

Weitek Corp.
Sunnyvale, CA

Career History for Robert J. Murphy (Cont'd)

Initially hired as a Design Manager with responsibility for putting a single chip into production. One year later, was managing the company's most important product along with others. Developed circuitry which gave the company world-class performance in memory, output drivers, and Electro-Static Discharge (ESD). Promoted to Director (1990). Managed the circuit design, architecture and layout groups. This included budgeting, staffing, and resource allocation for multiple programs, the largest of which was over 400K transistors. Responsible for the technical and administrative management of a staff that included 20 engineers and 5 layout people.

Major accomplishments included:

- * Managed the product design and release to production of a 40 MHz SPARC combined IU/FPU product
- * Managed the development and release to production of a Floating Point Coprocessor that works with the Intel i486.
- * Directed the redesign and release to production of two products, completed by other managers, which were not production worthy.
- * Aided Manufacturing in the pre- and post-production release management of our silicon foundries. This included modeling, process issues and production/testing problems.
- * Increased the staff by more than 50% in a one year period.
- * Delivered multiple projects on time.

Senior Engineering Manager
10/83 - 2/89

National Semiconductor Corp.
Santa Clara, CA

As the design manager and chief technical contributor for the E2CMOS PAL group, was a member of a team of three responsible for the introduction of three second-sourced products. Enlarged the design staff, established methodology and set circuit design criteria for new products under development.

The group's actions enabled the product line to go from zero revenue to greater than \$1 million/month in just 12 months. Prior to the start up of the E2CMOS PAL group, designed a Bi-CMOS PAL using lateral Ti-W fuses.

Major accomplishments included:

- * Doubled the reliability of the second-sourced devices.
- * Participated fully in all aspects of the second-sourcing licensing agreement.
- * Designed the world's first BiCMOS PAL, which was given as a paper at the ISSCC conference in 1986.
- * Developed the methodology and theory to improve lateral Ti-W fuse blowing circuitry.

Program Manager
4/82 - 10/83

RCA
Sommerville, NJ

Lead an inter-divisional program to develop 2 micron CMOS technology and a 64K SRAM for the commodity market. Responsible for a team of 15 people who: developed

Career History for Robert J. Murphy (Cont'd)

the process, did the modeling, designed the circuits, created the layout, and performed the testing.

Major accomplishments included:

- * Created a test chip (4K SRAM) shown to be fully functional, at speed, less than half way thru the program. This test chip was used to flush out the final bugs in the processing.
- * Managed the development of three new process features (Poly fuses, Poly Resistors and a 1 mask twin-tub process) that previously did not exist at RCA. Was technically responsible for Poly Resistors and Poly fuses.
- * Produced fully functional units at speed on first silicon.(64K SRAM)
- * Completed the program within two weeks of an 18 month schedule and under our \$1.2 million budget.

SRAM Design Manager
2/78 - 4/82

National Semiconductor
West Jordan, Utah

Hired as a circuit designer into the Santa Clara, Ca memory group to design a Pseudo-Static DRAM memory. Then designed a 4T cell 4K SRAM product. Promoted to Section Head when my first SRAM design went into production on the first mask set, not at the original design size, but on a 10% shrink die which was placed on the wafer across one of the rows.

Later, promoted to SRAM Design Manager and transferred to National's production facility in West Jordan. Supervised a team of six design engineers developing new products and providing production support for SRAM material in the fab.

Major accomplishments included:

- * Designed National's first SRAM with a 4T cell using poly resistors.
- * Developed a power-on standby circuit for the 2147 (4Kx1 SRAM 55nS) that was eventually copied by Intel.
- * Technical Management of the development of the world's first output short circuit control put into an SRAM.
- * Responsible for SRAM products which had a peak production rate of 30 K 4 inch (100 mm) wafers per month
- * Lead the team that brought the 2114 (4K SRAM) wafer yield from 50 die/wafer to over 280 die/wafer in 62 days.
- * Re-designed the 2114 to get the yield to 375 die / wafer and increased the production run rate to 4 million units per month.

Circuit Designer
6/74 - 2/78

Hughes Aircraft Co.
El Segundo, CA

Won a Hughes Masters Fellowship and worked part-time at Hughes while getting my Masters degree at UCLA. Initially, a Test Engineer testing space flight sub-assemblies, then my first design work was in power supplies. After receiving my MSEE, moved into IC design. Designed custom LSI's using SOS CMOS and a standard cell approach. Team Member designing Hughes 64K CCD Memories and Career History for Robert J. Murphy (Cont'd)

Career History for Robert J. Murphy (Cont'd)

also solely designed the Analog Buried Channel CCD used for the Liquid Crystal Light Valve.

Major accomplishments included:

- * Helped develop the first Liquid Crystal Light Valve at Hughes.
- * Designed or tested circuits that are still performing somewhere in space.

EDUCATION: BSEE Drexel University, Philadelphia, PA June 1974
 MSEE UCLA, Los Angeles, CA June 1976

SIGNIFICANT PUBLICATIONS: European Patent Application EP 1 580 762 A2
 "MEMMORY CELL HAVING AN ELECTRIC FIELD PROGRAMMABLE
 STORAGE ELEMENT, AND METHOD OF OPERATING SAME"
 Greer, Murphy, Szmanda; Appl. No. 05251696.0
 Filed 19.03.2005

 US Patent Application US 20055/0212022 "MEMMORY CELL
 HAVING AN ELECTRIC FIELD PROGRAMMABLE STORAGE ELEMENT,
 AND METHOD OF OPERATING SAME" Greer et al., Appl. No.
 10/964,382 Filed Oct. 13, 2004

 "A Bipolar-CMOS Field Programmable Array" ISSCC Feb 1986;
 "Liquid-Crystal Electro-Optical Modulators for Optical
 Processing of Two-Dimensional Data" SPIE Sept. 1977

SKILL SET: C, Verilog, Hspice, Dracula, Cadence/Mentor Design Tools

Document comparison by Workshare Compare on Wednesday, October 26, 2022
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Legend:	
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Padding cell	

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