

Petitioner Samsung Electronics Co., Ltd.'s Oral Argument for PTAB Hearing

***Samsung Electronics Co., Ltd. v. Netlist, Inc.*, Case Nos. IPR2022-00062 and IPR2022-00064
February 15, 2023**

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OVERVIEW OF 218 AND 595 PATENTS,
AND INSTITUTED GROUNDS

218 AND 595 PATENTS

'218 Patent

(12) **United States Patent**
Lee

(10) **Patent No.:** US 9,858,218 B1
(45) **Date of Patent:** *Jan. 2, 2018

(54) **MEMORY MODULE AND METHODS FOR HANDSHAKING WITH A MEMORY CONTROLLER**

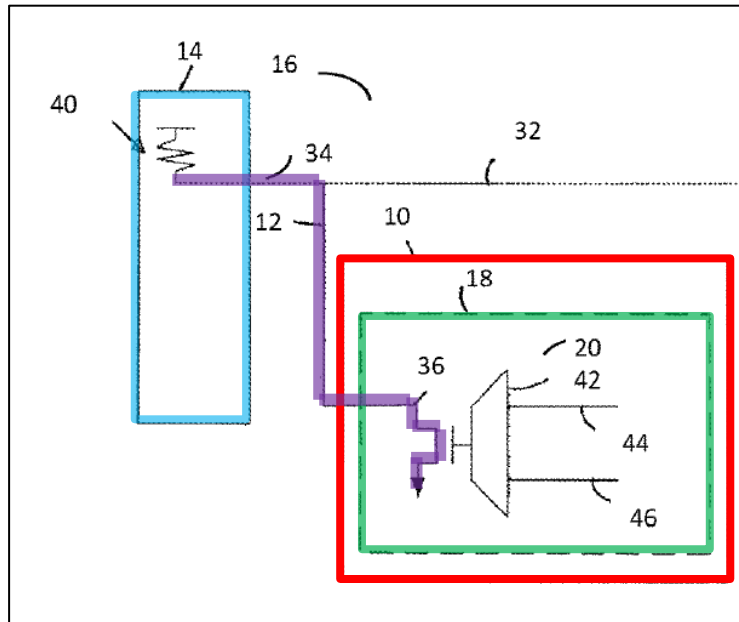
(71) Applicant: **Netlist, Inc.**, Irvine, CA (US)

(72) Inventor: **Hyun Lee**, Ladera Ranch, CA (US)

(73) Assignee: **Netlist, Inc.**, Irvine, CA (US)

(56)

1. A memory module operable with **a memory controller** of a host system, comprising:
a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;
dynamic random access memory elements on the printed circuit board;
a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller **having an open drain output** coupled to the error edge connection; and
wherein the memory module is operable in at least a first mode and a second mode, wherein **the memory module in the first mode is configured to be trained with one or more training sequences**; wherein **the memory module in the second mode is configured to perform one or more memory read or write operations not associated with the one or more training sequences** by communicating data signals via the first edge connections in response to address and command signals received via the second edge connections;
wherein the module controller is configured to receive via the second edge connections the address and command signals associated with the one or more memory read or write operations and to control the dynamic random access memory elements in accordance with the address and command signals, and wherein **the module controller is further configured to output via the open drain output** and the error edge connection a signal indicating a **parity error** having occurred while the memory module is **in the second mode**;
wherein **the module controller is further configured to drive a notification signal associated with the one or more training sequences** to the error edge connection **via the open drain output** while the memory module is **in the first mode**.



EX1001 ('218 Patent) (Cover, Fig. 3, in part)

EX1001 ('218 Patent) at Claim 1

'595 Patent

(12) **United States Patent**
Lee

(10) **Patent No.:** **US 10,474,595 B2**

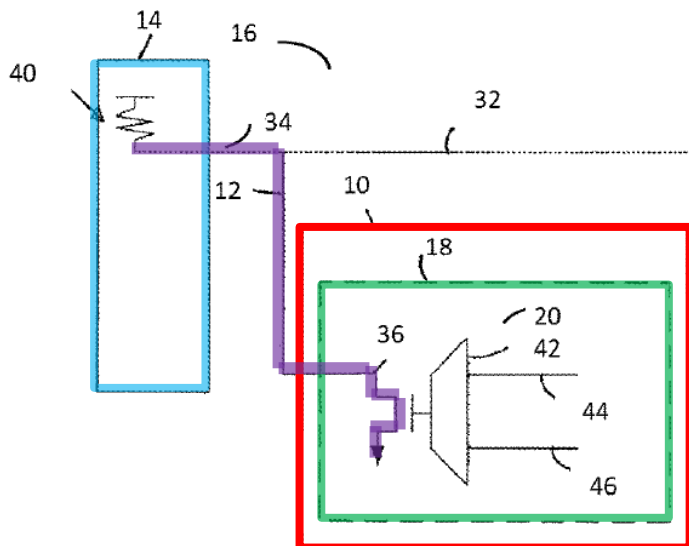
(45) **Date of Patent:** ***Nov. 12, 2019**

(54) **MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT PIN FOR PARITY ERROR IN A FIRST MODE AND FOR TRAINING SEQUENCES IN A SECOND MODE**

(71) Applicant: **Netlist, Inc.**, Irvine, CA (US)

(72) Inventor: **Hyun Lee**, Ladera Ranch, CA (US)

(73) Assignee: **NETLIST, INC.**, Irvine, CA (US)



EX1001 ('595 Patent) (Cover, Fig. 3, in part)

1. A memory module operable with a memory controller of a host system, comprising:

a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;

dynamic random access memory elements on the printed circuit board;

a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller **having an open drain output** coupled to the error edge connection; and

wherein the memory module is configurable to operate in any of at least a first mode and a second mode;

wherein **the memory module in the first mode** is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, wherein **the memory module in the second mode** is not accessed by the memory controller for normal memory read or write operations, and wherein **the memory module in the second mode** is configurable to perform operations related to one or more training sequences;

wherein the module controller is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein **the module controller** is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the first mode;

wherein **the module controller in the second mode** is further configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection to a first state or to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.

EX1001 ('595 Patent) at Claim 1

EX1001 ('595 Patent)

'218 and '595 Patent - Overview

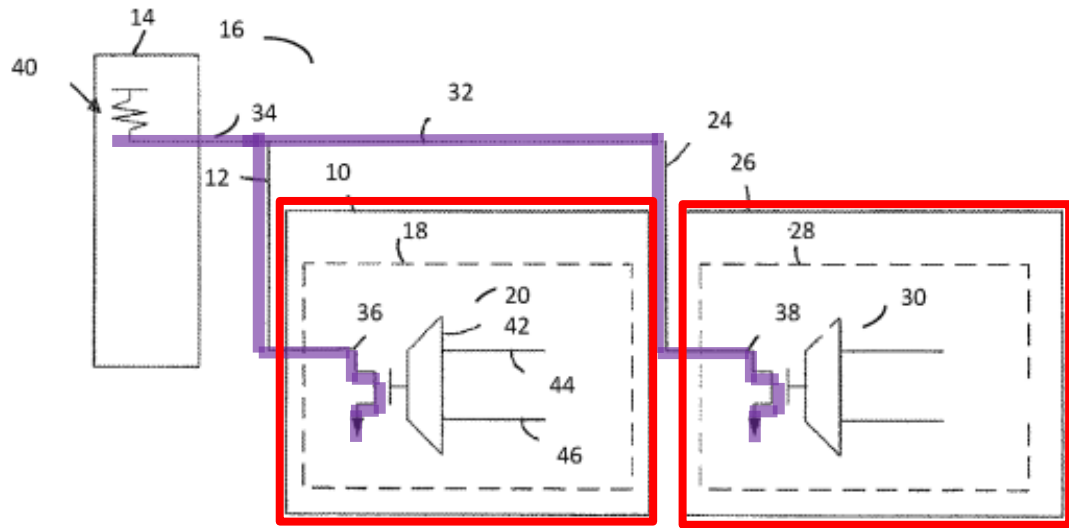


Figure 3

EX1001 ('595 Patent) at Fig. 3; EX1001 ('218 Patent) at Fig. 3

Certain embodiments described herein provide a method of establishing a handshake mechanism based on notification signaling. In certain embodiments, this mechanism can be implemented by adding a new interface (notifying) signal between the MCH and the memory subsystem controller, or by adding an additional functionality to an existing, non-timing critical signal without altering the memory subsystem hardware. In either case, the interface between the MCH and the memory subsystem controller of certain embodiments can be an open drain signaling from the memory subsystem controller to the MCH, although a variety of other configurations are possible. As will be appreciated by persons

EX1001 ('218 Patent) at 4:1-12

21 Q. In your opinion would a person of ordinary
22 skill in the art have known that an open drain output
23 in combination with a pull-up or pull-down resistor
24 would result in a wired-or function?

2 THE WITNESS: Yes. One of ordinary skill in
3 the art would have known this. It's probably 40
4 years old.

EX1077 (Murphy Dep. Tr.) at 178:21-179:4

218: Paper 1 (Pet.) at 10-13; Paper 35 (Repl.) at 27
595: Paper 1 (Pet.) at 10-13; Paper 35 (Repl.) at 27

INSTITUTED GROUNDS

Instituted Grounds

'218 Patent:

Grounds	Claims	Prior art
1	Claims 1-22	<u>Hazelzet</u> (EX1014) and <u>JEDEC</u> (EX1015)
2	Claims 1-22	<u>Hazelzet</u> and <u>Buchmann</u> (EX1016)
3	Claims 3-6, 10-12, 17-20	<u>Hazelzet</u> and (<u>JEDEC</u> or <u>Buchmann</u>), and <u>Kim</u> (EX1017)

'595 Patent:

Grounds	Claims	Prior art
1	Claims 1-24	<u>Hazelzet</u> (EX1014) and <u>JEDEC</u> (EX1015)
2	Claims 1-24	<u>Hazelzet</u> and <u>Buchmann</u> (EX1016)
3	Claims 3-7, 12-14, 20, 22, 23	<u>Hazelzet</u> and (<u>JEDEC</u> or <u>Buchmann</u>), and <u>Kim</u> (EX1017)

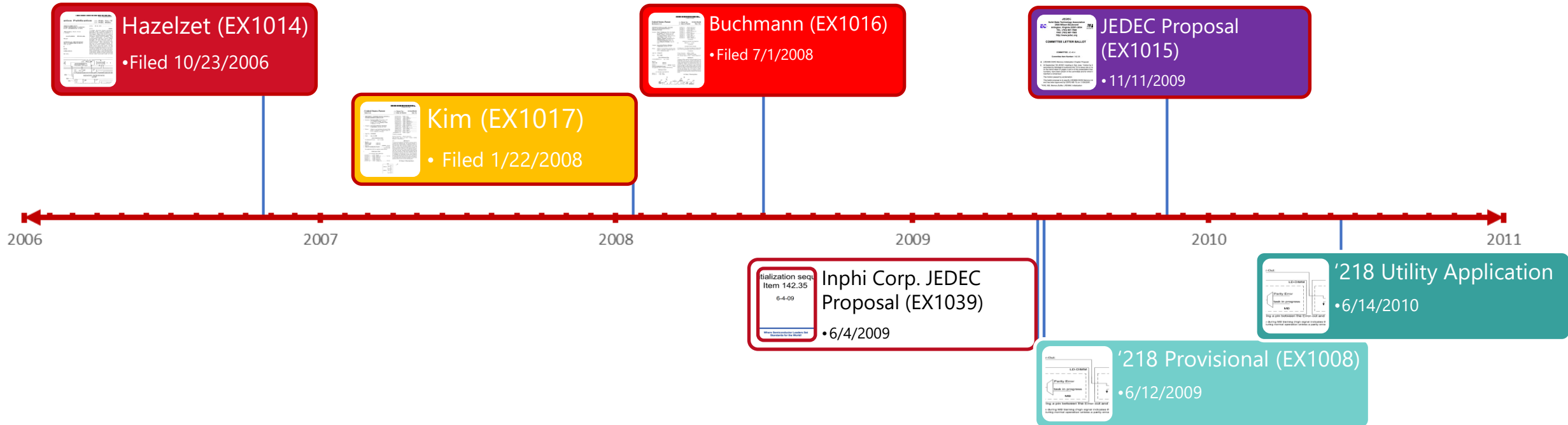
Same grounds in Final Written Decision in IPR2018-00303, invalidating related '623 Patent

EX1034 (IPR2018-00303 FWD)

'218: Paper 1 (Pet.) at 4, 15-16; Paper 14 (ID) at 57

'595: Paper 1 (Pet.) at 4, 13; Paper 14 (ID) at 55

Timeline of References



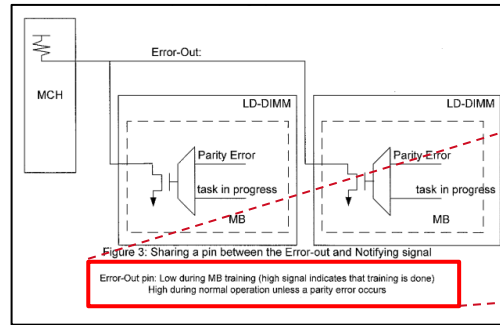
Grounds	'218 Claims	'595 Claims	Prior art
1	Claims 1-22	Claims 1-24	Hazelzet and JEDEC (EX1015)
2	Claims 1-22	Claims 1-24	Hazelzet and Buchmann
3	Claims 3-6, 10-12, 17-20	Claims 3-7, 12-14, 20, 22, 23	Hazelzet and (JEDEC or Buchmann), and Kim

'218: Paper 1 (Pet.) at 4, 24-30

'595: Paper 1 (Pet.) at 4, 24-30

THE PROVISIONAL FILED JUNE 12, 2009 02

Provisional Application (EX1008) Does Not Provide §112 Support



Error-Out pin: Low during MB training (high signal indicates that training is done)
High during normal operation unless a parity error occurs

	'218 Patent claims	'595 Patent claims
#1	"first edge connections are not active" during training (Claims 7, 9, 15)	"second edge connections include ... pins that are not active" in training related mode (Claims 8, 15-16, 18-19)
#2	"memory read or write operations not associated with ... training sequences" (Claim 1)	"memory module [...] is not accessed ... for [...] memory read or write operations" in training related mode (Claims 1, 10, 17, 21)
#3	"one or more" training "sequences" (Claims 1, 9, 15)	"one or more" training "sequences" (Claims 1, 10, 17, 21)
#4	—	"one or more N-bit-wide data signals" (Claim 21)

'218: Paper 1 (Pet.) at 5-10; Paper 35 (Repl.) at 8-14

'595: Paper 1 (Pet.) at 5-10; Paper 35 (Repl.) at 9-15

Provisional Application Does Not Provide §112 Support

#1: “first edge connections are not active” during training (‘218 claims 7, 9, 15) and
“second edge connections include ... pins that are not active” in training related mode (‘595 claims 8, 15-16, 18-19)

Institution Decision

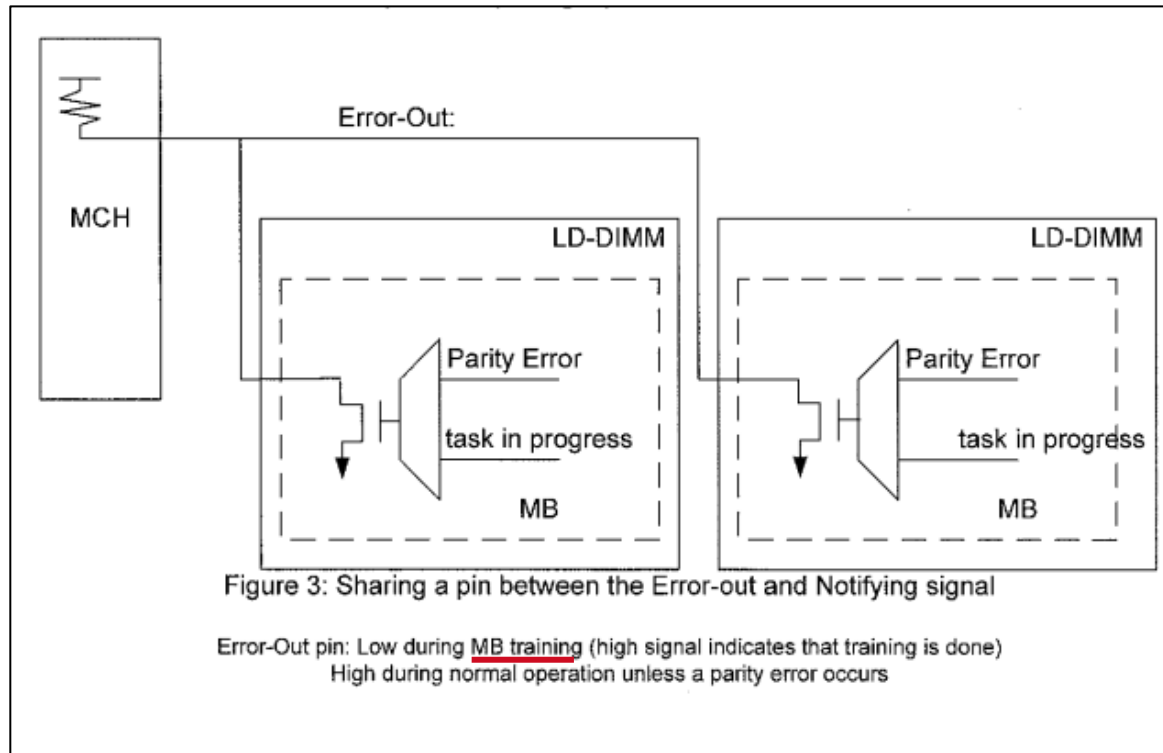
On the record before us, we are not persuaded that the portion of the Provisional that Patent Owner relies upon sufficiently discloses [“first edge connections are *not active*” during training (‘218 claims 7, 9, 15)]. Rather, we agree with Petitioner that the **portion of the Provisional cited by Patent Owner discusses the shortcomings in the prior art, rather than the claimed invention**. See Ex. 1008, 22–23 (“The shortcoming of the current the [sic] LR-DIMM proposal is that, instead of adopting the notification, the proposal requires the MCH to be in standby (idle, or wait) while the memory subsystem controller completes its task.”). **This portion of the Provisional does not refer to training or edge connections, or provide any indication that the inventor was in possession of the foregoing limitations**. See *Lockwood v. American Airlines, Inc.*, 107 F.3d 1565, 1572 (Fed. Cir. 1997) (“It is not sufficient for purposes of the written description requirement of § 112 that the disclosure, when combined with the knowledge in the art, would lead one to speculate as to modifications that the inventor might have envisioned, but failed to disclose.”). Therefore, on this record and at this stage of the proceeding, **we do not find that the evidence demonstrates sufficient written description support as to each of these limitations**.

218: Paper 14 (ID) at 21-22;
see also 595: Paper 14 (ID) at 23-24

‘218: Paper 1 (Pet.) at 5-8; Paper 14 (ID) at 21-22; Paper 35 (Repl.) at 9-12
‘595: Paper 1 (Pet.) at 9-10; Paper 14 (ID) at 23-24; Paper 35 (Repl.) at 12-13

Provisional Application Does Not Provide §112 Support

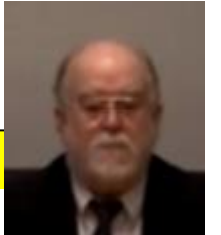
#1: “first edge connections are not active” during training (‘218 claims 7, 9, 15) and
“second edge connections include ... pins that are not active” in training related mode (‘595 claims 8, 15-16, 18-19)



EX1008 (Provisional) at p.25

13	Q. Let's start there. Is literally the only
14	time that the word "training" is used in the
15	provisional application marked as Exhibit 1008,
16	quote, MB training, end quote?
17	A. Yes. From my scan right now, the only
18	literal use of that term I can find is in a note
19	below Figure 3 on page 25.

EX1077 (Murphy Dep. Tr.) at 177:13-19



Provisional Application Does Not Provide §112 Support

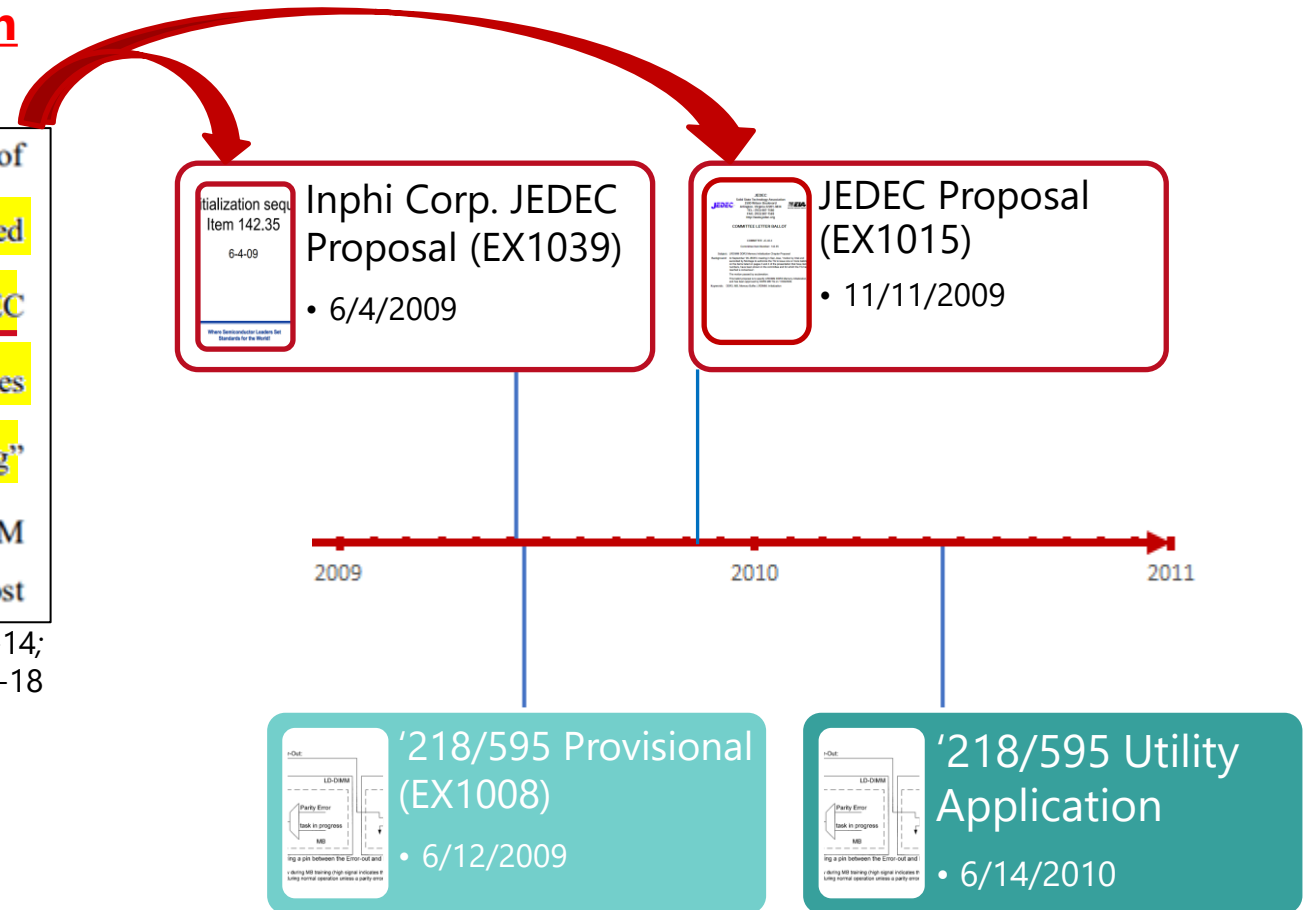
#1: “first edge connections are **not** active” during training (‘218 claims 7, 9, 15) and

“second edge connections include ... pins that are **not** active” in training related mode (‘595 claims 8, 15-16, 18-19)

Netlist points to the prior art rather than its own provisional to show support

Petitioner concedes that POSITA would have understood the functions of LR-DIMMs and would have “known” a pre-Provisional JEDEC document titled “MB Initialization Sequence” (EX1039). Pet., 6-7. The pre-Provisional JEDEC document defines the “initialization sequence” for LR-DIMMs, which includes “MB-DRAM Interface Training” comprising both “MB-DRAM Write Leveling” and “MB-DRAM Read Training” training sequences. EX1039.2. MB-DRAM Interface Training is performed by the memory buffer (“MB”), **not** the Host: “Host

‘218: Paper 31 (POR) at 13-14;
see also ‘595: Paper 31 (POR) at 16-18



‘218: Paper 35 (Repl.) at 10-12

‘595: Paper 35 (Repl.) at 11-12

Provisional Application Does Not Provide §112 Support

#1: “first edge connections are **not** active” during training (‘218 claims 7, 9, 15) and

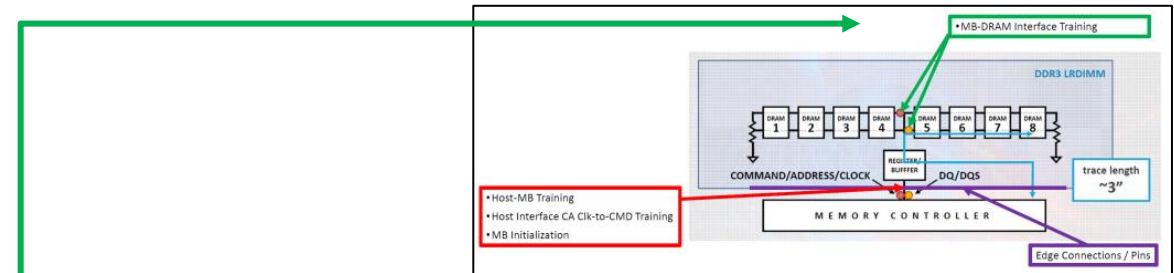
“second edge connections include ... pins that are **not** active” in training related mode (‘595 claims 8, 15-16, 18-19)

EX1081, p.1

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Petitioner concedes that POSITA would have understood the functions of LR-DIMMs and would have “known” a pre-Provisional JEDEC document titled “MB Initialization Sequence” (EX1039). Pet., 6-7. The pre-Provisional JEDEC document defines the “initialization sequence” for LR-DIMMs, which includes “MB-DRAM Interface Training” comprising both “MB-DRAM Write Leveling” and “MB-DRAM Read Training” training sequences. EX1039, 2. MB-DRAM Interface Training is performed by the memory buffer (“MB”), **not** the Host: “Host

‘218: Paper 31 (POR) at 13-14;
see also ‘595: Paper 31 (POR) at 16-18



[T]he written description inquiry looks to the ‘four corners of the specification’....The knowledge of ordinary artisans may be used to inform what is actually in the specification, **but not to teach limitations that are not in the specification, even if those limitations would be rendered obvious by the disclosure in the specification.**

Rivera v. ITC, 857 F.3d 1315, 1322 (Fed. Cir. 2017) (citations omitted).

While a **negative limitation** need not be recited in the specification *in haec verba*, there generally must be something in the specification that conveys to a skilled artisan that the inventor **intended the exclusion** ... [T]he written description requirement cannot be met through simple disregard of the presence or absence of a limitation.

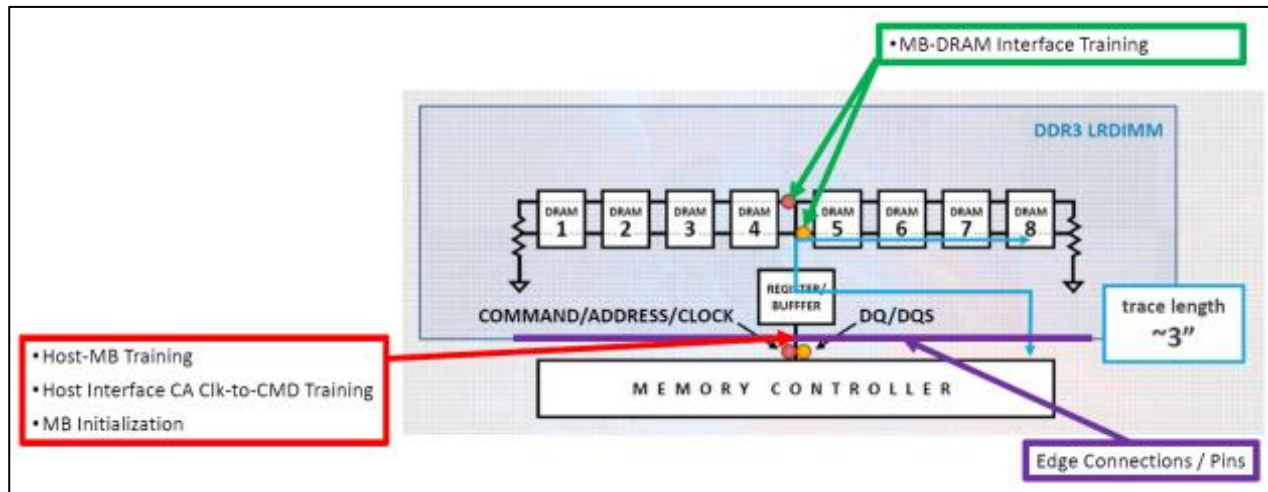
Novartis Pharms. Corp. v. Accord Healthcare, Inc., 38 F.4th 1013, 1017 (Fed. Cir. 2022)



Provisional Application Does Not Provide §112 Support

#1: “first edge connections are **not active**” during training (‘218 claims 7, 9, 15) and

“second edge connections include ... pins that are **not active**” in training related mode (‘595 claims 8, 15-16, 18-19)



EX1081, p.1

19 Q. And in your opinion would a person of
20 ordinary skill in the art have known that, on a DDR3
21 LR-DIMM memory module, that Host-MB Training, Host
22 Interface CA Clk-to-CMD Training and MB
23 Initialization each require the edge connections and
24 pins to be **active**?

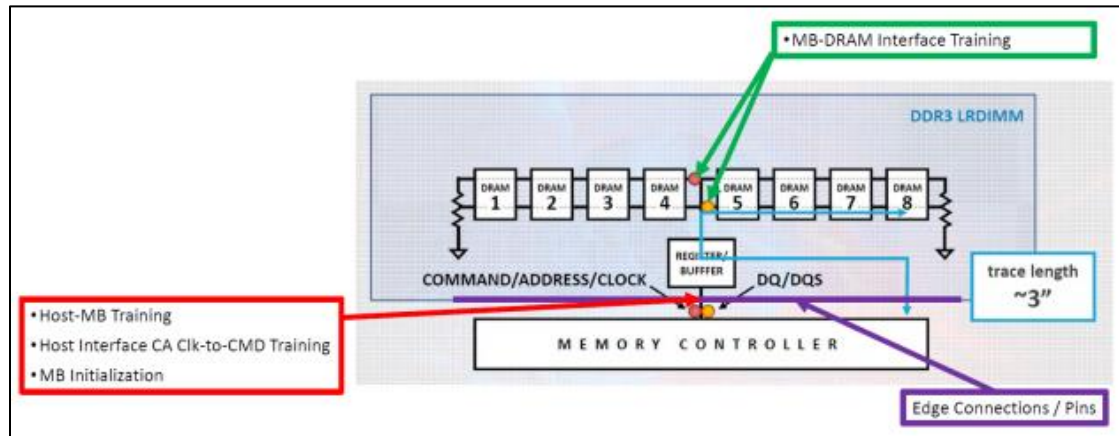
2 THE WITNESS: **Yes**, I believe that's the
3 case.

EX1077 (Murphy Dep. Tr.) at 132:19-133:3;
see also *id.* at 118:10-19

Provisional Application Does Not Provide §112 Support

#1: “first edge connections are **not active**” during training (‘218 claims 7, 9, 15) and

“second edge connections include ... pins that are **not active**” in training related mode (‘595 claims 8, 15-16, 18-19)



EX1081, p.1

Moreover, it is not the case that use of the edge connections would “*always*” be understood...as being *necessarily* excluded” by the Provisional, *Novartis*, 38 F.4th at 1017-18, even if “MB Training” were understood to encompass “MB-DRAM Interface Training” (green above). The Provisional application set out to solve the problem of the host computer (MCH) being “in standby (idle, or wait) while the memory subsystem controller completes its task” and expressly states that the “[notifying] method allows the MCH to execute *independent command* while it is waiting for a notification signaling for the memory subsystem controller.” EX1008, 22-23. A POSITA would have understood that such an independent command may include data communication, in which case the edge connections *would* be active. EX1003, ¶¶45, 50. That understanding is consistent with the proposed solution to the problem identified by the Provisional.

Provisional Application Does Not Provide §112 Support

#2: “one or more memory read or write operations **not** associated with the one or more training sequences” (‘218 Patent Claim 1) and “memory module [...] is **not** accessed ... for [...] memory read or write operations” in training related mode (‘595 Patent Claims 1, 10, 17, 21)

Institution Decision

On the record before us, we are not persuaded that the portion of the Provisional that Patent Owner relies upon (Ex. 1008, 22–23) sufficiently discloses [“one or more memory read or write operations **not** associated with the one or more training sequences” (‘218 Patent Claim 1)]. We agree with Petitioner that this portion of the Provisional does not contain any discussion of training sequences or the various operations, data signals, or edge connections. Moreover, we are not persuaded at this stage that mere reference to an “initialization period” and “normal operation,” without any discussion of training or training sequences, conveys to one of ordinary skill in the art that training sequences occur during the initialization period and not during normal operation. ...

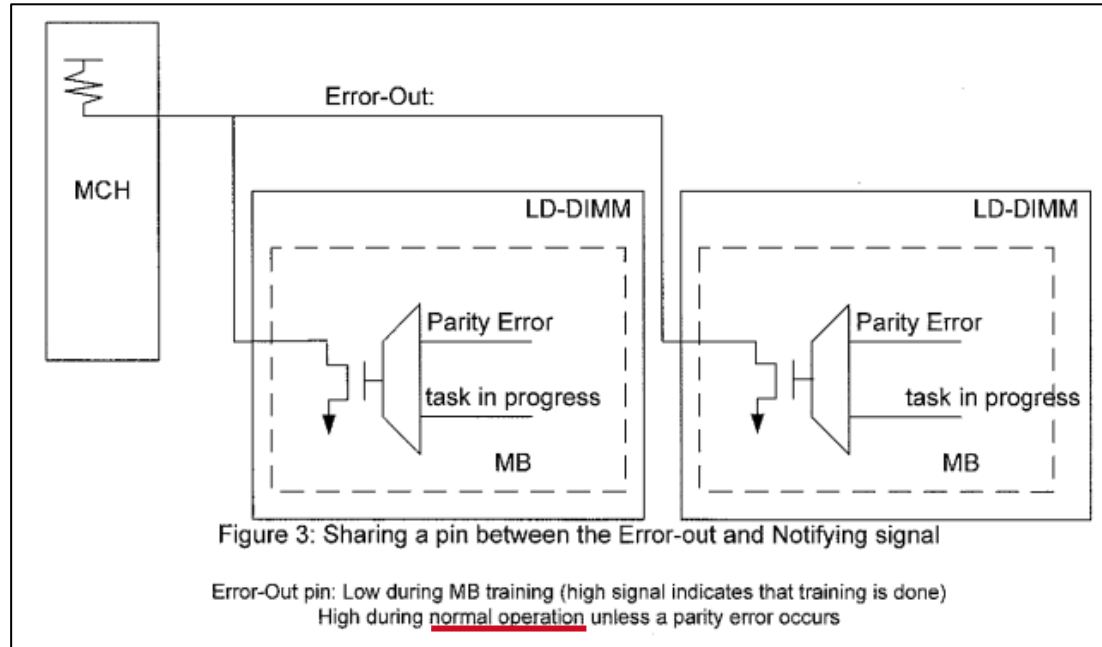
Additionally, silence in a Specification does not meet the written description requirement for a negative limitation. The Court of Appeals for the Federal Circuit has determined that an express intent to confer on the claim language the novel meaning imparted by the negative limitation is required, such as an express disclaimer or independent lexicography in the written description that provides support for the negative limitation. *Omega Engineering, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1323 (Fed. Cir. 2003). Therefore, on this record and at this stage of the proceeding, we do not find that the evidence demonstrates sufficient written description support as to this limitation.

218: Paper 14 (ID) at 23-24;
see also 595: Paper 14 (ID) at 20-21

218: Paper 1 (Pet.) at 8-9; Paper 14 (ID) at 22-24; Paper 35 (Repl.) at 12-13
595: Paper 1 (Pet.) at 5-8; Paper 14 (ID) at 20-21; Paper 35 (Repl.) at 9-12

Provisional Application Does Not Provide §112 Support

#2: “one or more memory read or write operations **not** associated with the one or more training sequences” (‘218 Patent Claim 1) and “memory module [...] is **not** accessed ... for [...] memory read or write operations” in training related mode (‘595 Patent Claims 1, 10, 17, 21)



EX1008 (Provisional) at 25

While a **negative limitation** need not be recited in the specification *in haec verba*, there generally must be something in the specification that conveys to a skilled artisan that the inventor **intended the exclusion** ... [T]he written description requirement cannot be met through simple disregard of the presence or absence of a limitation.



Novartis Pharms. Corp. v. Accord Healthcare, Inc., 38 F.4th 1013, 1017 (Fed. Cir. 2022)

52. There are two passing references to “normal operation” of the error-out pin in the provisional, and perhaps Patent Owner will argue that necessarily provides support for all the aforementioned terms and their interrelations during “normal operation.” But nothing in the provisional says that its “training” used during initialization does not perform “normal” read or write operations or such a training is necessarily excluded from its “normal operation.” In fact, it is my opinion that a Skilled Artisan would understand training could occur during normal operation. For



218: EX1003 (Alpert) at 152

See also 595: EX1003 (Alpert) at 44-48

218: Paper 1 (Pet.) at 8-9; Paper 14 (ID) at 22-24; Paper 35 (Repl.) at 12-13

595: Paper 1 (Pet.) at 5-8; Paper 14 (ID) at 20-21; Paper 35 (Repl.) at 9-12

Samsung Electronics Co., Ltd., Ex. 1082, p. 20

Provisional Application Does Not Provide §112 Support

#2: “one or more memory **read or write operations** **not** associated with the one or more **training** sequences” (‘218 Patent Claim 1) and “memory module [...] is **not accessed** ... for [...] memory **read or write operations**” in **training** related mode (‘595 Patent Claims 1, 10, 17, 21)



Q. Yes. So let me ask it again. Would a
22 person of ordinary skill in the art know about
23 **read-and-write operations** on a memory module that **are**
24 **associated with training**?

3 THE WITNESS: **Yes**, I believe one of ordinary
4 skill in the art would have known about memory
5 operations, memory read-and-write operations that
6 would have been part of training.

EX1077 (Murphy Dep. Tr.) at 191:21-192:6

The operational mode is the normal mode of the memory module 10. For example, during the operational mode, the memory module 10 is generally accessed by the system memory controller 14 of the host computer 16 during
45 standard computer operation not associated with initialization. For example, the system memory controller 14 may cause the memory module 10 to perform standard operations such as memory **read/write**, pre-charge, refresh, etc., while in operational mode, although it will be appreciated that one
50 or more of these operations can also be performed by the memory module 10 while in initialization mode in certain embodiments.

EX1001 (‘218 Patent) at 6:41-52

Provisional Application Does Not Provide §112 Support

#3: “one or more” training “sequences” (‘218 claims 1, 9, 15) (‘595 claims 1, 10, 17, 21)

Institution Decision

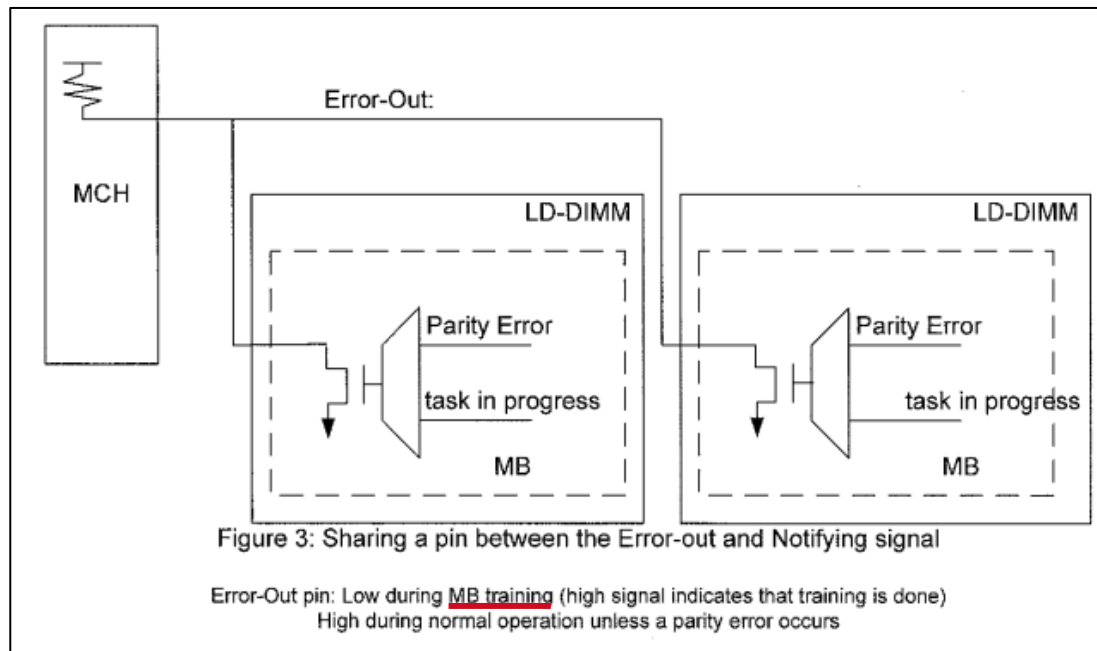
On the record before us, we are not persuaded that the portion of the Provisional that Patent Owner relies upon sufficiently discloses “configured to be trained with one or more training sequences” or “training with one or more training sequences.” We agree with Petitioner that the Provisional does not explicitly discuss training sequences and, at this stage of the proceeding, are not persuaded that the mere reference to “MB Training” in connection with Figure 3 sufficiently discloses these limitations. Accordingly, on this record and at this stage of the proceeding, we do not find that the evidence demonstrates sufficient written description support as to this limitation.

218: Paper 14 (ID) at 25;
see also 595: Paper 14 (ID) at 22

Provisional Application Does Not Provide §112 Support

#3: “one or more” training “sequences” (‘218 claims 1, 9, 15) (‘595 claims 1, 10, 17, 21)

Provisional discloses “MB training” only in general, without any details about “one or more training sequences”



EX1008 (Provisional) at 25

55. The provisional, however, only discloses a single “MB training”, that a Skilled Artisan would understand as a generic disclosure of “training” a memory buffer in some way. It does not disclose any training “sequences,” and particularly not “one or more” training sequences, much less that such specific “training sequences” are associated with “a notification signal.” Indeed, the phrases “train sequence” and “training sequences” are completely absent from the provisional.

218: EX1003 (Alpert) at ¶55
See also 595: EX1003 (Alpert) at 44-48

Provisional Application Does Not Provide §112 Support

#4: “one or more N-bit-wide data signals” (‘595 Claim 21)

Institution Decision

Patent Owner contends that Petitioner concedes that a person of ordinary skill in the art “would have been aware of the then-current DDR3 LRDIMMs, which supported 64-bit I/O configurations for the communication of data signals. Prelim. Resp. 15 (citing Ex. 2001 ¶ 40). Even assuming one would have known of 64-bit I/O configurations for data signals, that does not provide support for the recited “N-bit-wide data signals” over the entire range of “N” being “at least 32.” See, e.g., *In re Lukach*, 442 F.2d 967 (CCPA 1971) (range not supported by written description of specific example within the range). Consequently, Patent Owner has not shown that the Provisional provides sufficient written description support for this limitation.

595: Paper 14 (ID) at 23

Provisional Application Does Not Provide §112 Support

#4: “one or more N-bit-wide data signals” (‘595 Claim 21)



address and control signals, where N is at least 32.” EX1001, 18:31-35. However, dynamic random access memory or DRAM is mentioned just once in the provisional, in the following sentence: “This method allows the MCH to work with a non-homogenous memory subsystem, such as mixing of DIMMs with different DIMM density, ranks, DRAM density, speed, DRAM configuration, etc.” EX1008, 23. And the terms “data signal,” “bit,” “width,” and “32” are found nowhere in the provisional, much less the concept of data signals of a certain width, particularly “at least 32.” There is no support for this limitation of this claim in the provisional.

595: EX1003 (Alpert) at ¶53

Netlist failed to satisfy its burden of production for §112

Institution Decision

Because the Provisional does not have the same disclosure as the '218 patent, we do not presume the '218 patent is entitled to the benefit of the Provisional's filing date. But because Petitioner has the burden to show a reasonable likelihood of prevailing on a ground of patentability to institute trial, we require Petitioner to show that the art existed as of the date of invention, presumed to be the filing date of an application until an earlier date is proved. *Bausch & Lomb, Inc. v. Barnes-Hind/Hydrocurve, Inc.*, 796 F.2d 443, 449 (Fed. Cir. 1986); *In re Fong*, 378 F.2d 977, 980 (CCPA 1967) ("Appellants' filing date, no earlier date having been proved, is their date of invention."). The burden of production then shifts to Patent Owner to respond to Petitioner's specific arguments to show sufficiently that the '218 patent claims are entitled to the earlier filing date of the Provisional.

218: Paper 14 (ID) at 19; *see also* 595: Paper 14 (ID) at 18

218: Paper 14 (ID) at 19; Paper 35 (Reply) at 14
595: Paper 14 (ID) at 18; Paper 35 (Reply) at 14-15

Netlist failed to satisfy its burden of production for §112

§112 requires “a written description of the invention...to make and use the same”

Q. And Mr. Murphy, you understand that this -- this is my time to ask you questions, so I'm not going to get another opportunity in the future to ask you your opinions. Now is the designated time for us to conduct this deposition. So I just want to be sure, give you the opportunity to express any opinion you have now with respect to whether or not a person of ordinary skill in the art reading the provisional application marked as Exhibit 1008 would be able to **make and use** a memory module as claimed in the '218 patent or the '595 patent.

THE WITNESS: Counselor, can you point me to a particular paragraph in my declaration that talks about either making or using an LR-DIMM with respect to the '595 patent in my declaration?

EX1077 at 167:6-:22

Q. No. Again, that's the question we're trying to get clarity on is I don't see that you've offered any opinion that a person of ordinary skill in the art reading the provisional application marked as Exhibit 1008 would be able to **make and use** a memory module that practices the claims of either the '218 patent or the '595 patent. But if I've overlooked something, please let me know.

THE WITNESS: As of this point in time today, Counselor, my opinions, all of my opinions on this matter, are included in my declaration. They are the opinions that I have been asked to offer.

EX1077 at 167:24-168:12

Q. And in preparation for the deposition today, you reviewed your declarations marked as Exhibit 2027; is that correct?

A. I did.

Q. Carefully?

A. Yes.

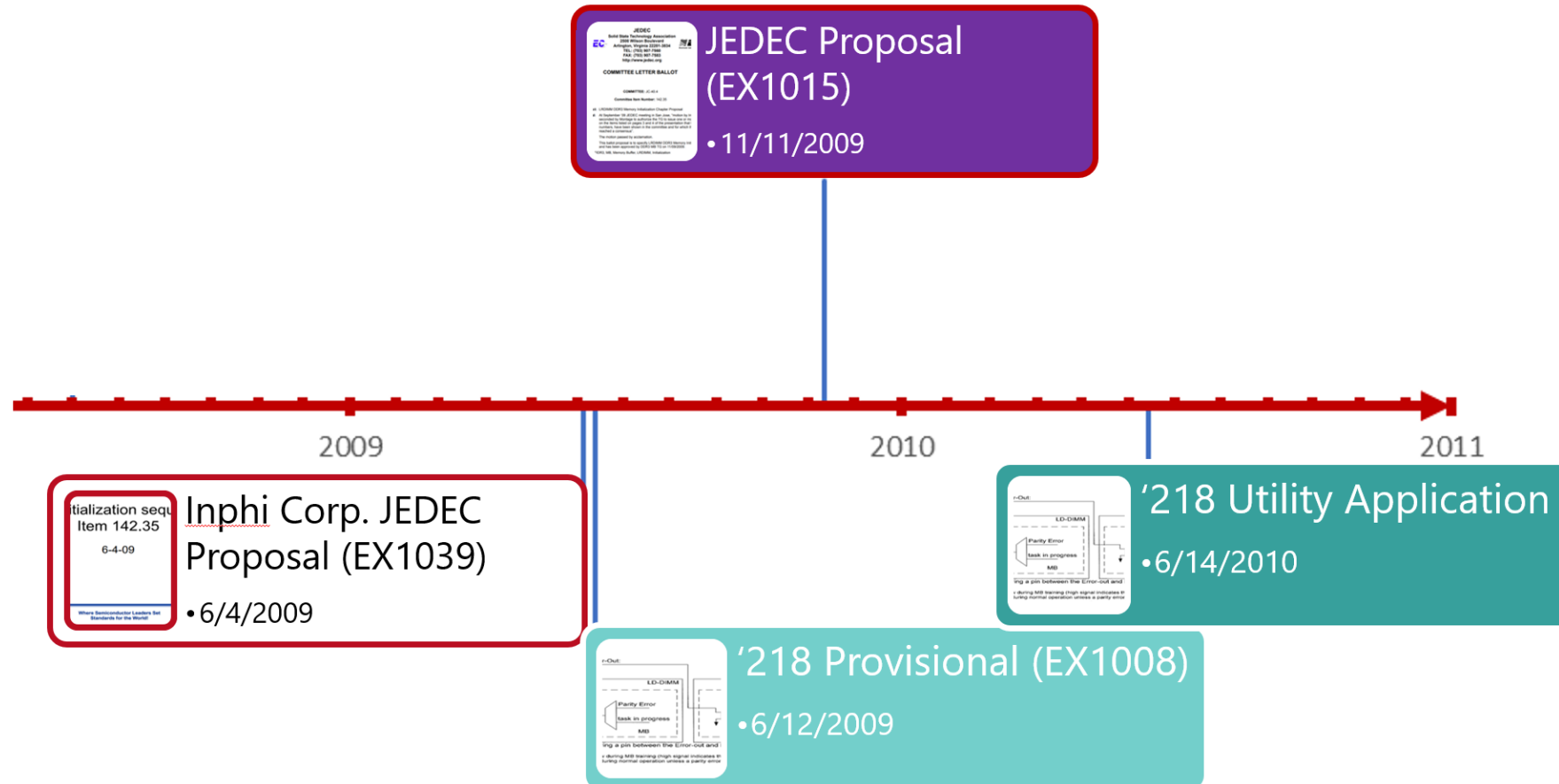
EX1077 at 168:21-169:1

218: Paper 35 (Reply) at 14
595: Paper 35 (Reply) at 14-15

JEDEC (EX1015) IS A PRIOR-ART
“PRINTED PUBLICATION”

03

JEDEC (EX1015) is a prior-art “printed publication”



'218: Paper 1 (Pet.) at 4, 24-30

'595: Paper 1 (Pet.) at 4, 24-30

What is JEDEC?



For over 50 years, JEDEC has been the global leader in developing and publishing open standards for the microelectronics industry. JEDEC's membership consists of more than 3,000 volunteers representing nearly 300 member companies, and includes key technical individuals from most device, assembly, system and testing companies. JEDEC publications and standards are adopted worldwide. JEDEC is accredited by ANSI and maintains liaisons with numerous standards bodies throughout the world.



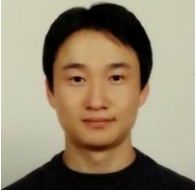
JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

1050 (Carlson Decl.) ¶¶4, 15 & p.146

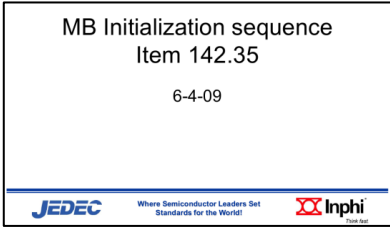
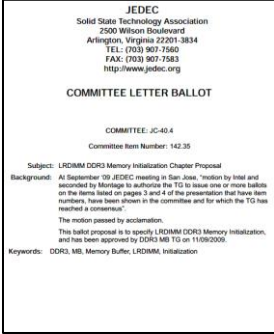
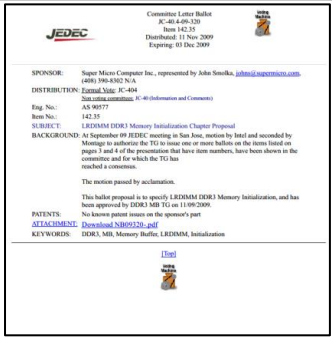
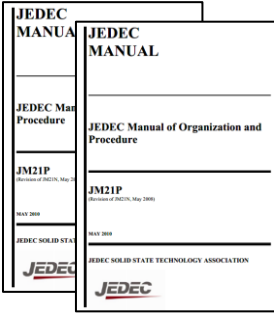
'218: Paper 1 (Pet.) at 25-27, n.5; Paper 35 (Repl.) at 2-8

'595: Paper 1 (Pet.) at 25-26, n.7; Paper 35 (Repl.) at 2-9

JEDEC witnesses

Witness	Exhibits
 Julie Carlson Custodian of JEDEC Documents	EX1050 (declaration, attaching copies of EX1015 (Ex.A), EX1051 (Ex.B), EX1037 (Ex.C), EX1036 (Ex.D), EX1052 (Ex.E), EX1053 (Ex.F), EX1039 (Ex.G), EX1046 (Ex.H), EX1049 (Ex.I), EX1048 (Ex.J)); EX2024 (deposition)
 John Halbert Intel engineer who participated in relevant JEDEC committees and task groups from 2001-2017	EX1054 (declaration); EX2022 (deposition)
 SJ Park Samsung engineer who participated in the creation and approval of the JEDEC Proposal (EX1015)	EX1055 (declaration, attaching copies of EX1051 (Ex.A), EX1015 (Ex.B), EX1037 (Ex.C), EX1052 (Ex.D), EX1036 (Ex.E), EX1053 (Ex.F)); EX2025 (deposition)
 Internet Archive Maintained archived copies of public JEDEC webpages from 2009	EX1076 (declaration, attaching copies of EX1071-EX1075)
 Robert Murphy Patent Owner's Technical Expert	EX2027 (declaration); EX1077 (deposition)

Exhibits relevant to the JEDEC proposal #142.35 (EX1015)

Exhibit	Description	Exhibit	Description
EX1039 	Inphi presentation #142.35 to JEDEC on June 4, 2009 (with no confidentiality markings)	EX1015 	JEDEC proposal #142.35 (with no confidentiality markings) approved December 2009 Part of Grounds 1 & 3
EX1046 	JEDEC minutes for June 2009 meeting showing EX1039 was presented to dozens of people, including to Netlist's sole named inventor, Hyun Lee, and Samsung's engineer, SJ Park (at 1-2, 21-22)	EX1037 	Tally of votes for JEDEC proposal #142.35 as of December 4, 2009
EX1051 	JEDEC ballot for #142.35 distributed November 11, 2009 (with no confidentiality markings)	EX1048-49 	JEDEC manuals of procedures (2008 to 2010) showing no confidentiality requirements

'218: Paper 1 (Pet.) at 25-30, n.5; Paper 35 (Repl.) at 2-8

'595: Paper 1 (Pet.) at 25-28, n.7; Paper 35 (Repl.) at 2-9

JEDEC's public webpages in 2009

Exhibit	Description	Exhibit	Description
EX1071	JEDEC webpage listing committee meeting dates and locations in 2009 (as of April 6, 2009)	EX1074	JEDEC membership list (as of May 5, 2009)
EX1072	JEDEC webpage with catalog of committee numbers and publications (as of April 21, 2009)	EX1075	JEDEC webpage with benefits of membership (as of April 13, 2009)
EX1073	JEDEC webpage about membership (as of April 10, 2009)		

'218: Paper 1 (Pet.) at 25-30, n.5; Paper 35 (Repl.) at 2-8

'595: Paper 1 (Pet.) at 25-28, n.7; Paper 35 (Repl.) at 2-9

Who can join JEDEC?

Membership in JEDEC is open to independent entities that manufacture semiconductor products, or provide related services or equipment. Membership is company based, not by individual.

Membership in JEDEC entitles the company to appoint one principal member and alternate members to the committee or committee(s) of choice. The range of activities covered by each JEDEC committee chosen is published in [JM18](#). A company representative may attend a committee meeting on a one-time guest basis to determine whether the committee activities are beneficial to the company.

Annual Dues are calculated on a calendar year basis (January-December).*

- One committee and subcommittees \$4,000
- Two committees and subcommittees \$6,500
- Three committees and subcommittees \$9,000
- Four or more committees and subcommittees \$12,000

*As of January 1, 2007 new members pay only \$2,000 for the first year's dues when joining one committee and its subcommittees.



Public accessibility is **not limited** to circumstances of **free** or academic distributions.

Centripetal Networks, Inc. v. Cisco Sys., Inc., 847 Fed. Appx. 869, 878 (Fed. Cir. Mar. 10, 2021) (emphasis added)

A reference will be considered publicly accessible if it was disseminated or otherwise made available to the extent that persons interested and ordinarily skilled in the subject matter or art ***exercising reasonable diligence, can locate it***

M & K Holdings, Inc. v. Samsung Elec. Co., 985 F.3d 1376, 1379 (Fed. Cir. 2021) (quotations omitted)

[W]e explained that '[a]ccessibility goes to the issue of whether interested members of the relevant public could obtain the information ***if they wanted to***' and '[i]f accessibility is proved, there is ***no requirement to*** show that particular members of the public ***actually received*** the information.'

GoPro, Inc. v. Contour IP Holding LLC., 908 F.3d 690, 693 (Fed. Cir. 2018) (emphasis added)

'218: Paper 1 (Pet.) at 25-27, n.5; Paper 35 (Repl.) at 2-8

'595: Paper 1 (Pet.) at 25-26, n.7; Paper 35 (Repl.) at 2-9

Samsung Electronics Co., Ltd., Ex. 1082, p. 34

34

Who can join JEDEC?

JEDEC membership is open to any company or organization, or one of its related entities, that manufactures electronic equipment or electronic-related products or related services. Anyone interested can join JEDEC online, at JEDEC.org. When joining, any interested person can join any committee, including JC-40: Digital Logic (which includes its subcommittees, such as JC-40.4: Registered & Fully Buffered Memory Support Logic) and JC-45: DRAM Modules (which includes its subcommittee, such as JC-45.4: Fully Buffered DRAM Modules). The joining members would have access to documents available to the committees and subcommittees the members join, such as

1050 (Carlson Decl.) at ¶15

25 Q. And going back to Paragraph 5 of your
2 declaration, I just want to understand part of -- of
3 this. It says, "JEDEC membership is open to any
4 company, organization, or one of its related entities,
5 that manufacturers electronic equipment or
6 electronic-related products or related services."
7 Do you see that?
8 A. Yes.
9 Q. Was that true in 2009/2010 as well?
10 A. Yes, I believe it was.

EX2024 (Carlson Dep. Tr.) at 26:25-27:10



9 Q If an interested member of the public wanted
10 to join JEDEC, how easy was it to become a member of
11 JEDEC?

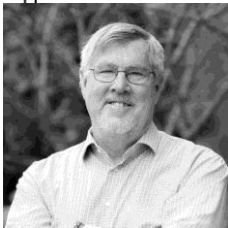
14 THE WITNESS: Just bring your checkbook.

15 BY MR. CHANDLER:

16 Q Are you aware of any examples where JEDEC
17 refused to allow someone from joining JEDEC?

20 THE WITNESS: No.

EX2022 (Halbert Dep. Tr.) at 43:9-20



'218: Paper 1 (Pet.) at 25-27, n.5; Paper 35 (Repl.) at 2-8

'595: Paper 1 (Pet.) at 25-26, n.7; Paper 35 (Repl.) at 2-9

[illegible]

Samsung Semiconductor

Hypertek GmbH	Texas Instruments
I/O Data Device Inc.	Tezzaron Semiconductor Corporation
IBM Corporation	Thermo Fisher Scientific
ITE Tech. Inc.	Tokyo Electron Device Ltd.
ITW/ECPS	Toshiba America
IXYS Corporation	Transcend
Ibiden USA Corporation	TriQuint Semiconductor
INCOMM Technologies Co. Ltd.	Tyco Electronics
Infilink Co. Ltd.	U.S. Army
Industrial Tech Research Institute	ULink Technology Inc.
Infineon Technologies	Ultra Communications Inc.
Inphi Corporation	Unifoa Corporation
Integrated Device Technology	Unigen Corporation
Integrated Silicon Solution Inc.	Unisem
Intel Corporation	Unisys Corporation
International Rectifier Company	UniTest
IAE Electronics Inc.	Unity Semiconductor
King Tiger Technology Inc.	VIA Technologies Inc.
Kingmax Semiconductor Inc.	VPT Inc.
Kingston Technology Company Inc.	Ventura Technology Group Inc.
Kostal Incorporated	Verigy US Inc.

'218: Paper 1 (Pet.) at 25-27, n.5;
Paper 35 (Repl.) at 2-8
'595: Paper 1 (Pet.) at 25-26, n.7;

Paper 35 (Repl.) at 2-8

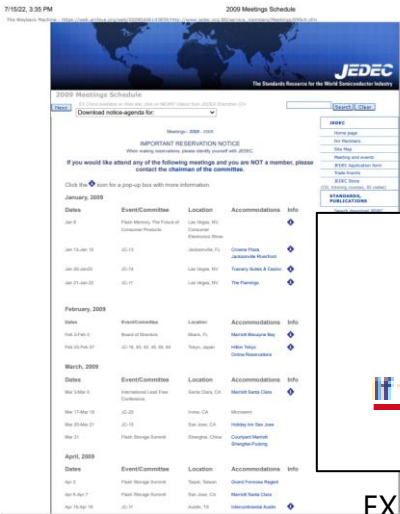
Paper 35 (Repl.) at 2-9

Benefits of JEDEC membership

AS A MEMBER OF JEDEC, YOU HAVE ACCESS TO A WIDE RANGE OF BENEFITS AND ACTIVITIES. THEY ARE:

- Admission to meetings of the JEDEC Committees.
- Ballots, surveys, minutes, and manuals for the committee(s) of interest.
- Free copy of standards, publications, bulletins, and guidelines
- Permission to reproduce JEDEC copyrighted works for internal company use without restriction.
- Reports on international meetings and interface with EIAJ, IEC ANSI, IPC, PCMCIA, SEMI, IEEE, and others.
- Interface with Government agencies such as NASA and DSCC.
- Workshops and Conferences on topics of interest.

JEDEC offers free distribution of all standards and publications to its member companies via E-mail and also has E-mail distribution of all other JEDEC materials. Free standards can also be obtained via the JEDEC website at www.jedec.org/download



Meetings:- 2008 - 2009

IMPORTANT RESERVATION NOTICE

When making reservations, please identify yourself with JEDEC.

If you would like attend any of the following meetings and you are NOT a member, please contact the chairman of the committee.

EX1071 at 1

EX1075 at 1
See also EX1076 (Internet Archive Declaration);
EX1054 (Halbert), ¶¶6, 11
EX2022 (Halbert Dep. Tr.) at 13:4-14:11, 15:14-:22, 32:7-56:20, 59:10-60:15

JEDEC membership gives access to past documents

Ms. Carlson also testifies that JEDEC membership is open to any company or organization ... and that once a party joins it is given access JEDEC documents such as [EX1015] and the other documents cited above. EX1050, ¶15.

218: Paper 1 (Pet.) at 29 n.5; see also 595: Paper 1 (Pet.) at 26 n.7



5. JEDEC membership is open to any company or organization, or one of its related entities, that manufactures electronic equipment or electronic-related products or related services. Anyone interested can join JEDEC online, at JEDEC.org. When joining, any interested person can join any committee, including JC-40: Digital Logic (which includes its subcommittees, such as JC-40.4: Registered & Fully Buffered Memory Support Logic) and JC-45: DRAM Modules (which includes its subcommittee, such as JC-45.4: Fully Buffered DRAM Modules). The joining members would have access to documents available to the committees and subcommittees the members join, such as Exhibits A-J attached hereto, available to any such members who joined JC-40.4 and JC-45.4.

1050 (Carlson Decl.) at ¶15

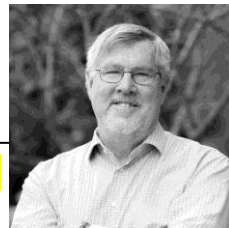
JEDEC's catalog of committees and publications

JEDEC CATALOGUE	
Document Type	
NUMBER JEDEC Engineering Bulletin (EB) JED-3-6 METHOD OF MEASUREMENT FOR SEMICONDUCTOR LOSS: GATE MICROSCOPICALLY PURPOSE OF THIS PUBLICATION IS TO RECOMMEND FOR USE IN THE TESTING OF SEMICONDUCTOR DEVICES WHICH USE THE GATE SOURCE TO MEASURE AND PROVIDE LOG INFORMATION. Static and dynamic measurements are covered. January 1975; Resubmitted February 1986 / JEDEC Committee JED-6 STANDARD MEASUREMENTS OF THE ELECTRICAL CHARACTERISTICS OF SEMICONDUCTOR OPERATING CHARACTERISTICS December 1966; Resubmitted October 1984 / Committee 33/JEDEC JED-15 THERMAL AND MECHANICAL MEASUREMENTS FOR SEMICONDUCTOR DEVICES: This bulletin explains the technology and methods of measuring semiconductor parameters. It is also intended to be used with the EIA Registration Data format for semiconductor integrated circuit logic chips. November 1969 / JC-40 Committee JED-14 DATA GUIDE FOR MICROELECTRONIC ASSEMBLIES: This guide defines general procedures for the failure analysis of monolithic integrated microelectronic chips. Although the generalized procedural steps may apply to all microelectronic circuit additional analysis steps unique to the chip are included. July 1976; Resubmitted November 2006 / September 2003 / JC-14 Committee JED-17 OVER-TEMPERATURE FOR QUALITY AND RELIABILITY ASSURANCE OF LOG CIRCUITS November 1970; Resubmitted April 1987 April 1987 JED-18 RECOMMENDED CHARACTERIZATION OF MOS DEPT RESISTORS: This recommended applies to MOS DEPT Resistors. Definitions are given for 7 digital registers but applicable to all CMOS and 8 channel with changes in power supply notation. November 1972 / JC-40 Committee JED-30 ACCEPTED PRACTICES FOR MEASUREMENTS OF DEVICE THERMAL CHARACTERISTICS January 1975; Resubmitted November 1988 / JC-11 Committee	
NUMBER Tentative Standards (TENTSTD) TENTSTD-11 HANDLING AND INSTALLATION OF POWER SEMICONDUCTORS IN STATIC TEST RACKS INCLUDING IN-PROCESS AND WIP July 1973; Resubmitted June 1992 June 1992 / JC-22.2 Subcommittee TENTSTD-12 STANDARD FOR RELIABLE JUNCTION RESISTORS: The supplier furnished under standard shall be a product that has been tested and meets the definitions and requirements specified herein. November 1973 / JC-22.1 Subcommittee	
NUMBER JEDEC Specifications (ES) JED-2 TRANSDUCER, GALLIUM ARSENIDE POWER PNP, SEMICONDUCTOR: Equal performance requirements and quality assurance requirements for gallium arsenide power PNP effect transistors (FETs), also known as MESFETs designed for use in high-reliability space applications. September 1970 / JC-40 Committee	

EX1072 (JEDEC Catalogue) at 1, 59

Q. Did JEDEC publicize that JC-40 was the committee working on digital logic -- for memory modules?

THE WITNESS: Yes.



EX2022 (Halbert Dep. Tr.) at 40:9-16

JC-40 CMOS Digital Logic

Q. Does JEDEC organize its documents and presentations by committee member?

THE WITNESS: Yes.

Q. If you are interested in JEDEC documents and presentations related to a particular technical area such as memory modules, can you use the committee number to easily find relevant documents?

THE WITNESS: Yes.

Q. Could you briefly explain how?

A. So you can go to the JEDEC website, click on the committee, and then there's a -- a search box. You can search for particular words, by date, by item number, however you want to search for the document you're interested in.



EX2022 (Halbert Dep. Tr.) at 52:22-53:16

Q. Is it possible to use the minutes of the JEDEC meetings to find relevant documents that were presented at prior JEDEC meetings in a given technical area?

THE WITNESS: Yes. Because you can search by item number.

Q. If you ever needed help trying to find a JEDEC document, was there a person at JEDEC you could call who could help you find what you were looking for?

THE WITNESS: Yes.

Q. Can you tell us little bit about that?

THE WITNESS: Yeah. So Donna McEntire was one person you could call. There was another person you could call who was in charge of the item numbers or assigning item numbers to documents. You could also call her for help to find documents.



EX2022 (Halbert Dep. Tr.) at 54:12-55:8

Exhibits 1071-76 and argument regarding “indexing/cataloging” were timely

Petitioner’s Authorized Reply to POPR	Institution Decision
“Patent Owner cites <i>Jazz</i> (POPR at 6, 9–10), but that case supports Petitioner because, like here, the reference was ‘disseminated’ in connection with a meeting, and thus ‘neither indexing nor searchability was required.’” 895 F.3d at 1356–57, 1359.” 218: Paper 11 at 3; see also 595: Paper 11 at 3	“Patent Owner further argues that Petitioner did not show that persons of ordinary skill in the art could have reasonably found the JEDEC proposal. Prelim. Resp. 8–10. Petitioner counters that the JEDEC proposal was disseminated in connection with a JEDEC meeting, and thus neither indexing nor searchability was required. Prelim. Reply 3.... We agree that Petitioner relies on dissemination of the JEDEC proposal, as opposed to indexing or cataloging, to establish public accessibility of the JEDEC proposal.... To the extent Patent Owner continues to challenge the printed publication status of this reference, the parties are requested to further develop the record on this issue.” 218: Paper 14 (ID) at 31-32; see also 595: Paper 14 at 29-30

Exhibits 1071-76 and argument regarding “indexing/cataloging” were timely

I. Reply to Patent Owner Response and Reply to Petitioner Opposition to a Motion to

Amend; Sur-Replies

A petitioner may file a reply to a patent owner response, and a patent owner may file a reply to an opposition to a motion to amend. 37 C.F.R. § 42.23. Additionally, in response to issues arising from the Supreme Court’s decision in *SAS* (138 S. Ct. at 1358), the Board will permit the petitioner, in its reply brief, to address issues discussed in the institution decision.

The patent owner will similarly be allowed to address the institution decision in its sur-reply, if necessary to respond to petitioner’s reply. Petitioner may not submit new evidence or argument in reply that it could have presented earlier, e.g. to make out a prima facie case of unpatentability. A party also may submit rebuttal evidence in support of its reply. See *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1077–78 (Fed. Cir. 2015). If a party submits a new expert declaration with its reply, the opposing party may cross-examine the expert, move to exclude the declaration, and comment on the declaration and cross-examination in any sur-reply. *Id.* at 1081–82.

Consolidated Trial Practice Guide at 73 (Nov. 2019)



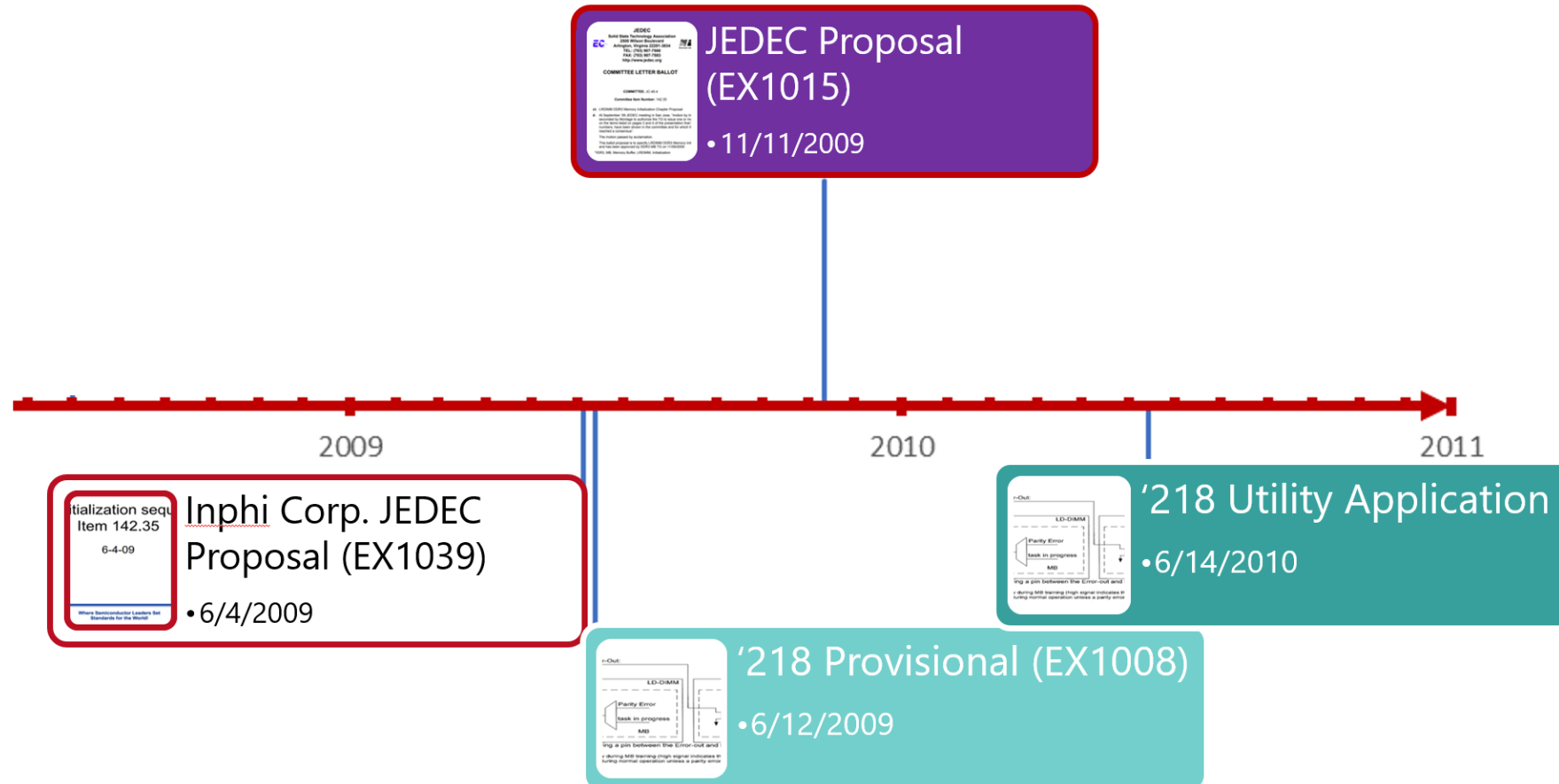
[I]f the patent owner challenges a reference’s status as a printed publication, a petitioner may submit a ***supporting declaration with its reply*** to further support its argument that a reference qualifies as a printed publication.

Hulu, LLC v. Sound View Innovations, LLC, IPR2018-01039, Paper 29, at 15 (PTAB Dec. 20, 2019) (precedential)

²¹⁸: Paper 1 (Pet.) at 25-27, n.5; Paper 35 (Repl.) at 2-8; Paper 48 (Opp. to PO Mot. to Exclude) at 1-3

⁵⁹⁵: Paper 1 (Pet.) at 25-26, n.7; Paper 35 (Repl.) at 2-9; Paper 48 (Opp. to PO Mot. to Exclude) at 1-3

JEDEC (EX1015) is a prior-art “printed publication”



'218: Paper 1 (Pet.) at 4, 24-30

'595: Paper 1 (Pet.) at 4, 24-30

EX1071: JEDEC meeting in June 2009

The Wayback Machine - https://web.archive.org/web/20090406143859/http://www.jedec.org:80/service_members/Meetings/09Sch.cfm



EX1071 at 1



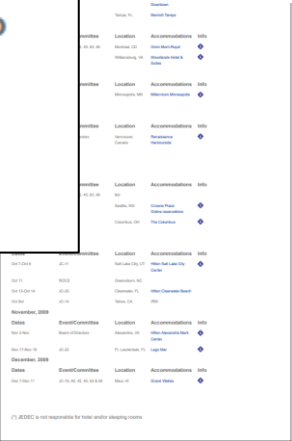
The Standards Resource for the World Semiconductor Industry

2009 Meetings Schedule

News EX China available on Web site, click on NEWS! Videos from JEDEX Shenzhen (Ch

Download notice-agenda for:

June, 2009				
Dates	Event/Committee	Location	Accommodations	Info
Jun1-Jun 5	JC-16, 40, 42, 45, 63, 64	Montreal, CD	Omni Mont-Royal	
Jun 23-Jun 25	JC-14	Williamsburg, VA	Woodlands Hotel & Suites	



EX1071 at 2

'218: Paper 1 (Pet.) at 25-27, n.5; Paper 35 (Repl.) at 2-8
'595: Paper 1 (Pet.) at 25-26, n.7; Paper 35 (Repl.) at 2-9

EX1039: JEDEC presentation #142.35 on June 4, 2009

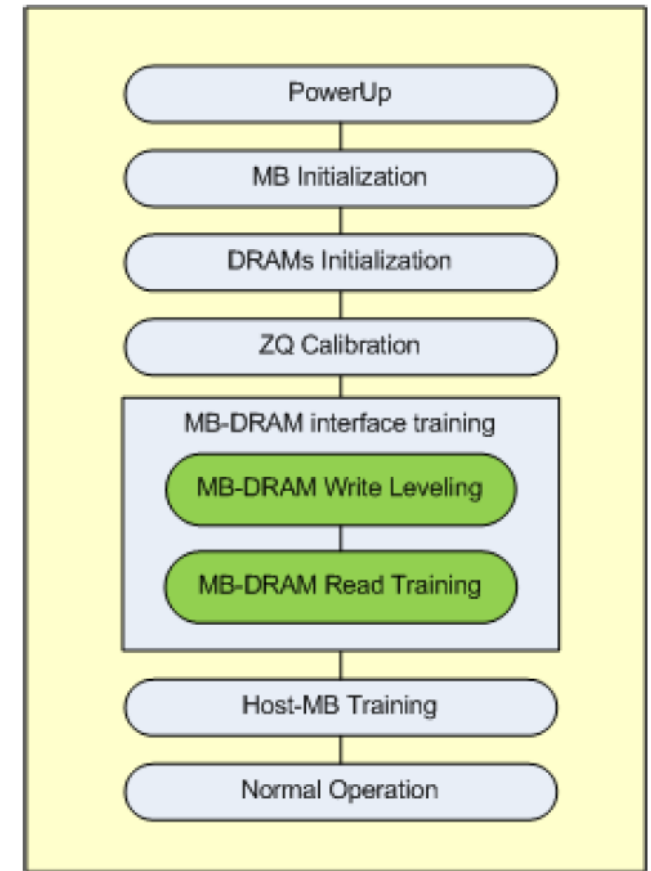
MB Initialization sequence

Item 142.35

6-4-09



Where Semiconductor Leaders Set
Standards for the World!



EX1039 at 2

EX1039 at 1

EX1046: JEDEC meeting minutes for June 4, 2009

Minutes of Meeting No. 158 JC-40 Digital Logic Committee

June 4, 2009 Montreal, Canada

Members Present	Company	Telephone	E-mail
John Smolka, Chairman	Silego Technology	408-466-0412	jsmolka@silego.com
Mark Kellogg, Secretary	JEDEC Consultant	(c) 585-455-3545	mkellogg@kcdservices.com
Sam Patel	Advanced Micro Devices Inc.	408-774-7161	sam.patel@amd.com
Perry Keller	Agilent Technologies	719-590-5651	perry_keller@agilent.com
Paul Goodwin	Avant Technology L.P.	512-719-6303	paul_goodwin@avanttechnology.com
Alan Grossmeier	Cray Inc.	715-726-4815	agross@cray.com
Cecil Ho	CST Inc	972-241-2662	cecil@simmtester.com
Maheer Amer	Diablo Technologies Inc.	819-776-9393	mamer@diablo-technologies.com
Ilan Krashinsky	Diablo Technologies Inc.	408-378-7938	ikrashinsky@diablo-technologies.com
Takao Ono	Elpida Memory Incorporated	81-42-775-7355	t.ono.gz@elpida.com
Toshio Sugano	Elpida Memory Incorporated	81-42-775-7225	tsugano.wq@elpida.com
Bill Gervasi	FormFactor Inc.	408-621-4157	bilge@discobolusdesigns.com
Mark Farley	Freescale Semiconductor	512-895-2318	mark.farley@freescale.com
Robert Sprinkle	Google Inc.	650-253-0631	rsprinkle@google.com
Belal Gharaibeh	Hewlett Packard Company	812-418-5263	belal.gharaibeh@hp.com
Michael Oh	Hynix Semiconductor	82-10-8729-3685	taehyun.oh@hynix.com
Art Kilmer	IBM Corporation	802-769-7378	ckilmer@us.ibm.com
Kyu-hyun Kim	IBM Corporation	914-945-2216	kimk@us.ibm.com
Oliver Kiehl	Infineon	802-659-4596	jedec.kiehl@gmail.com
Chet Jewan	Inphi Corporation	805-446-4152	cjewan@inphi-corp.com
Sameer Kuppahalli	Inphi Corporation	805-418-3306	skuppahalli@inphi-corp.com
Paul Washkewicz	Inphi Corporation	805-446-5119	pwashkewicz@inphi-corp.com
Roland Knaack	Integrated Device Technology Inc.	678-775-2932	rtk@adc.idt.com
Kuljit Bains	Intel Corporation	253-371-7178	kuljit.bains@intel.com
Joseph Tsang	Intel Corporation	916-356-4194	joseph.tsang@intel.com
Janis Kellogg	JEDEC Consultant	(c) 585-455-3545	mkellogg@kcdservices.com
Charles Fumweger	JEDEC SSTA Inc.	510-440-1084	charles@caf.org
Ivan Chiang	Kingston Technology Company Inc.	714-427-3856	ivan_chiang@kingston.com
William Shen	LSI Corporation	408-433-4072	william.shen@lsi.com
Scott Graham	Micron Technology Inc.	208-368-3960	sgraham@micron.com
George Pax	Micron Technology Inc.	208-368-2809	gpax@micron.com
Joe Quddus	Montage Technology Group Ltd.	408-982-2785	joe.quddus@montage-tech.com
Desi Rhoden	Montage Technology Group Ltd.	512-402-1011	desi@brite-sun.com
Mario Martinez	Netlist Inc.	949-679-0159	mmartinez@netlist.com
Roelof Salters	NXP Semiconductors	31-40-272-9806	roelof.salters@nxp.com
Jang Seok Choi	Samsung Semiconductor	82-31-208-6376	jschoi@sec.samsung.com
Sung Joo Park	Samsung Semiconductor	82-31-208-6674	sjoo@sec.samsung.com
Mia Quddus	Samsung Semiconductor	408-544-4354	mquddus@ssi.samsung.com
Jonathan Hinkle	Sanmina-SCI Corporation	949-643-7255	jonathan.hinkle@vikingmodular.com
Howard Sussman	Sanyo Semiconductor Corporation	978-562-9660	sanyo.hs@ix.netcom.com

090278:mwk:07/01/09

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Sung Joo Park Samsung Semiconductor 82-31-208-6674 sjoo@sec.samsung.com

EX1046 at 1

Hyun Lee Netlist 949-232-8396 hlee@netlist.com

EX1046 at 2

Minutes of Meeting No. 158 JC-40 Digital Logic Committee

June 4, 2009 Montreal, Canada

Jeffrey Chung	Silego Technology	408-327-8807	jchung@silego.com
Kelvin Marino	Smart Modular Technologies, Inc.	949-788-3833	kelvin.marino@smartm.com
Clement Fang	Sun Microsystems Inc.	650-786-6595	clement.fang@sun.com
Ricki Williams	Sun Microsystems Inc.	858-876-3042	ricki.williams@sun.com
Ingolf Frank	Texas Instruments Inc.	49-81-61-80-48-65	ingolf.frank@ti.com
Christian Harrieder	Texas Instruments Inc.	49-8161-80-3374	christian.harrieder@ti.com
Edmundo de la Puente	Verigy US Inc.	408-553-6805	edmundo.delapuate@verigy.com
David Chan	Wintec Industries Inc.	408-856-0830	davidc@wintecind.com
Others Present			
Michael Litt	Advanced Micro Devices Inc.	905-882-8142	michael.litt@amd.com
Joseph Macri	Advanced Micro Devices Inc.	408-572-6032	joe.macri@amd.com
Kazuyoshi Tsukada	Buffalo Inc.	81-52-619-1895	tsukada@melcoinc.co.jp
Wendy Elsassser	Denali Software Inc.	512-345-6064	wbshop@denali.com
Michael Takefman	Diablo Technologies	613-220-6991	tak@diablo-technologies.com
Franco Forlini	Diablo Technologies Inc	514-941-2331	fiorlini@diablo-technologies.com
Hong-bae Kim	Hynix Semiconductor	82-31-630-5086	hongbae.kim@hynix.com
Rami Sethi	IDT	408-373-3145	rami.sethi@idt.com
Hyun Mun (Sean) In	Indilinx Co Ltd	82-31-709-6321	sean@indilinx.com
Victor Cai	Inphi	(805) 446-5175	vcai@inphi-corp.com
Jim Chapman	Maxim Integrated Products	503-547-2270	jim.chapman@maxim-ic.com
Todd Farrell	Micron Technology Inc.	208-363-5545	tfarrell@micron.com
Kevin Ryan	Micron Technology Inc.	208-368-3954	kryan@micron.com
Frank Shu	Microsoft Corporation	425-707-1779	frankshu@microsoft.com
Chia Jen Chang	Nanya	713-774-4113	jrchang@tx.nanya.com
Peter Linder	Nanya Technology Corporation	713-774-4113	jedec@tx.nanya.com
Steve Wang	Nanya Technology Corporation	408-961-4010	swang@us.nanya.com
Hyun Lee	Netlist	949-232-8396	hlee@netlist.com
James Malatesta	Numonyx B.V.	916-356-4348	james.malatesta@numonyx.com
Brett Clark	PMC-Sierra Ltd.	610-289-5213	brett_clark@pmc-sierra.com
Christopher Socci	PNY Technologies Inc.	973-560-5366	csocci@pny.com
Hung Vuong	Qualcomm Inc.	858-658-2871	hvuong@qualcomm.com
Masashi Umino	Renesas Technology Corporation	81-3-5201-5083	umino.masashi@renesas.com
Keun Soo Jo	Samsung Semiconductor	82-31-208-4961	ksjo@sec.samsung.com
Ramzi Ammar	Silego	408-327-8800	rammar@silego.com
Alan Ruberg	Silicon Image Inc.	408-616-4027	atr@siliconimage.com
Wladyslaw Bolanowski	Sony Ericsson Mobile Communications	46-1080-14188	wladyslaw.bolanowski@sonyericsson.com
Bin Chi Chiou	Winbond Electronics Corporation	886-3-5678168	bcchiu@winbond.com
Bo Zhang	Wintec	4088560815	jiauz@wintecind.com

Page 2 of 33

4.3.4.0 #142.35 Inphi

MB Initialization Sequence

A high-level overview of the initialization sequence was shown, covering host operations prior to normal operation. The MB power-up timing was then shown and was described as being fundamentally the same as the SSTE32882 device.

The MB power-up table was reviewed, followed by the host configuration of the MB control words, the host MRS to configure the DRAM (the buffer simply forwards these commands), the MB-DRAM interface training (MB write-leveling to DRAM, read training, etc), after which normal operation can begin. The MB-DRAM write leveling steps and read training were then shown in greater detail – the TG will work the details.

Page 21 of 33

Samsung Electronics Co., L
Ex. 1046, p. 1

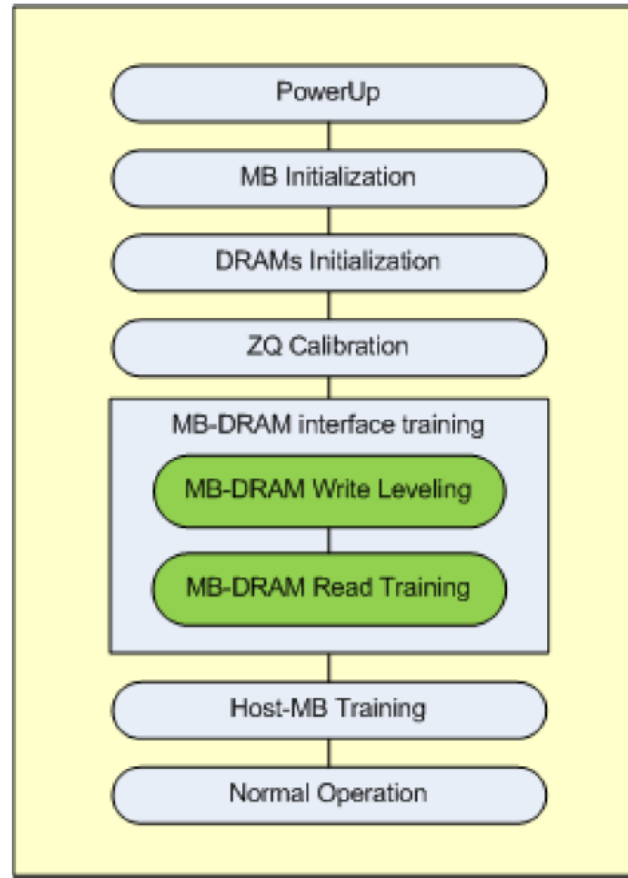
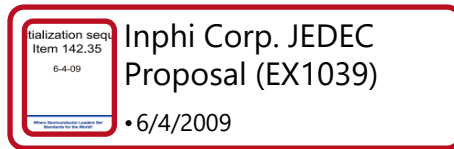
Minutes of Meeting No. 158 JC-40 Digital Logic Committee

June 4, 2009 Montreal, Canada

Discussion:
- A request was made to change the text from "iMB" to "MB" where this shows up in the presentation.

EX1046 at 21-22

JEDEC's "task group" worked on the proposal from June (EX1039) to November (EX1015)



EX1039 at 2

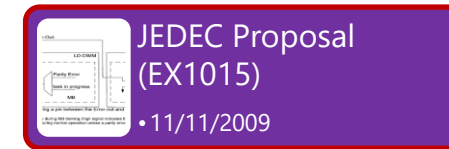
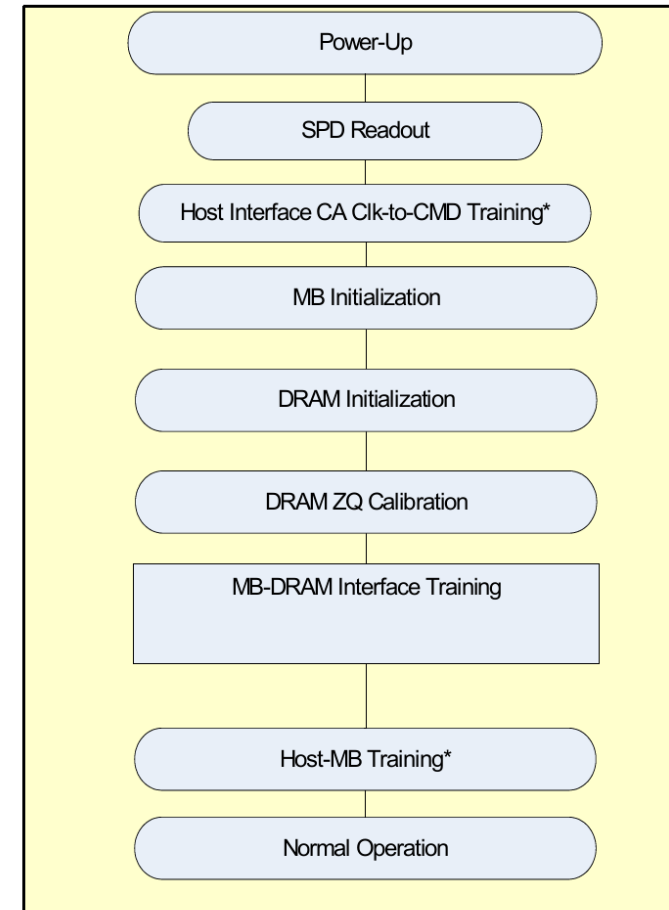


Figure 1 — Initialization Overview



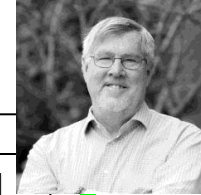
EX1015 at 4

* This step is optional for the MB but may be done by some platforms

JEDEC's "task group" worked on EX1015 between June and November 2009

So a task group is where the work actually gets done, technical work, and then the task group will approve a ballot to send to the committee, and then the committee will then vote to -- there'll be votes, and the -- the ballot will then pass and then move into the -- eventually the spec. So, the JEDEC committees meet once a quarter to do voting and JEDEC business, and the task groups will meet what -- at least once a week.

EX2022 (Halbert Dep. Tr.)
at 13:25-14:11



Q. What is the mechanism for a JEDEC member to bring new subject matter to -- to a JEDEC task group and begin the standardization process?

A. You post a presentation, and then it's discussed in the task group prior to the meeting beginning. Usually, there's a rule that it has to be posted, oh, maybe six to twelve hours before the meeting, give people a chance to read it.

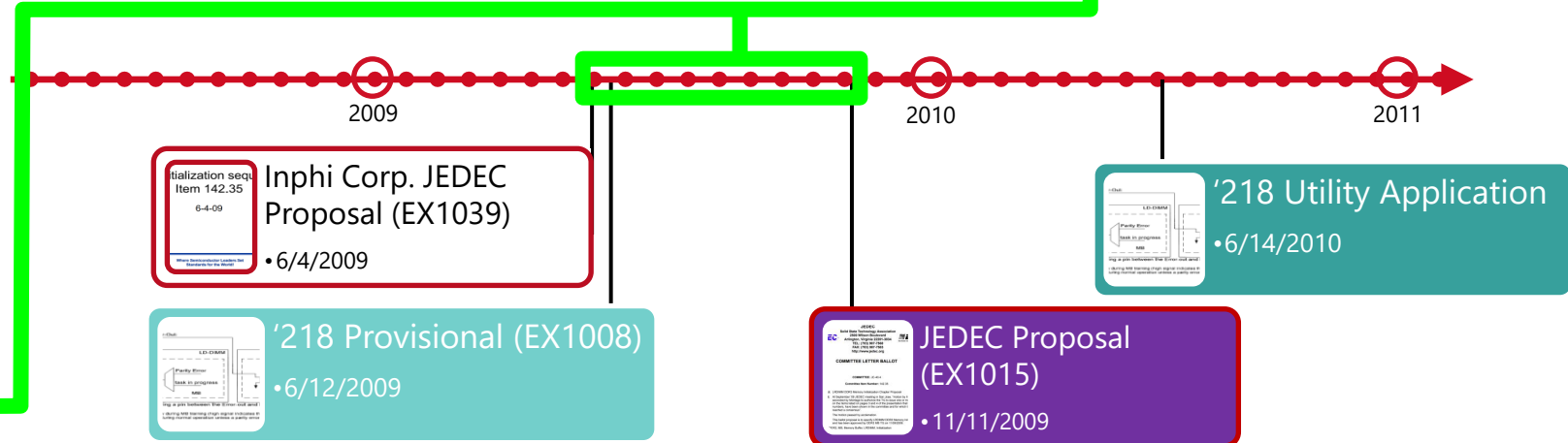
EX2022 (Halbert Dep. Tr.)
at 26:4-27:13

Q. And then, in a task group meeting, that presentation is discussed among the JEDEC members that are part of that task group; is that correct?

A. Yes.

[B]efore the voting process takes place, so there is a long discussion in the task groups, and only when there is consensus, then the consensus would be uploaded in the voting machine. And these task groups would be weekly -- these task groups would be held on a weekly basis, and it would go through a five-day review process as well.

EX2025 (Park Dep. Tr.) at 32:23-33:10



'218: Paper 1 (Pet.) at 4, 24-30

'595: Paper 1 (Pet.) at 4, 24-30

EX1015 was distributed for formal vote on November 11, 2009



Committee Item Number 142.35 (hereinafter “Item Number 142.35”), attached as Exhibit A, with the Subject “LRDIMM DDR3 Memory Initialization Chapter Proposal” is a proposal to the JC-40.4 committee for ballot approval. Ex. A. On November 9, 2009, Item Number 142.35 was approved by DDR3 MB TG (“Task Group”) and referred to JC-40.4 to vote for ballot approval. See Ex. A at 1; see also Ex. B at 1. After approval, Committee Letter Ballot JC-40.4-09-320 (hereinafter “Letter Ballot for Item Number 142.35”), attached as Exhibit B, was distributed to the members of JEDEC JC-40.4 on November 11, 2009. Ex. B. Letter Ballot for Item Number 142.35 itself distributes Item Number 142.35 to JC-40.4, in the link labeled “Download NB09320-.pdf.” Ex. B. A true and

JEDEC
(EX1015)

1050 (Carlson Decl.) at ¶7

EX1015: JEDEC proposal #142.35 is NOT marked confidential



JEDEC
Solid State Technology Association
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TEL: (703) 907-7560
FAX: (703) 907-7583
<http://www.jedec.org>



COMMITTEE LETTER BALLOT

COMMITTEE: JC-40.4

Committee Item Number: 142.35

Subject: LRDIMM DDR3 Memory Initialization Chapter Proposal

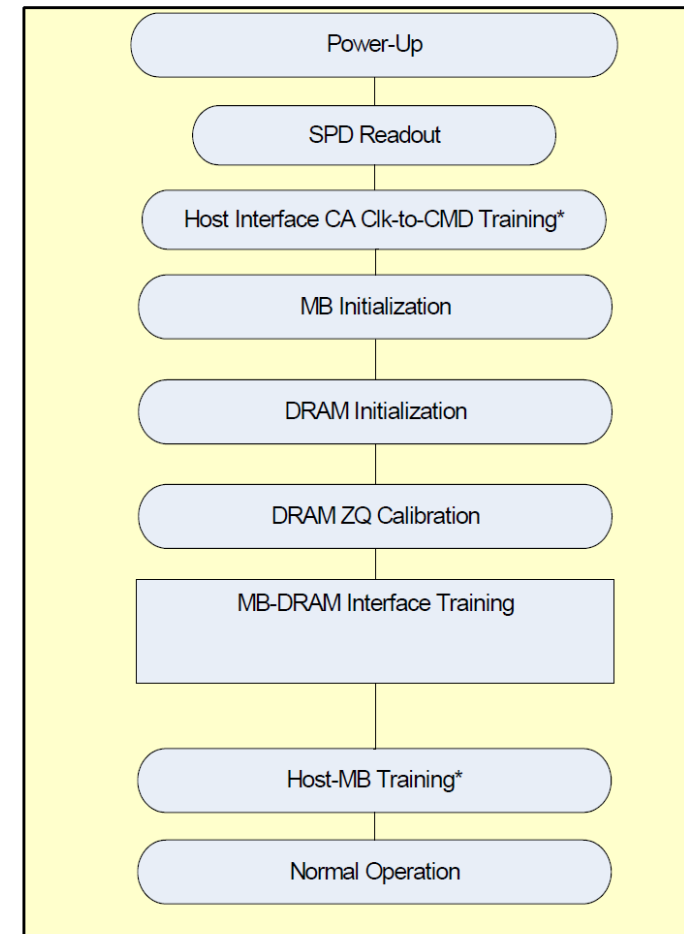
Background: At September '09 JEDEC meeting in San Jose, "motion by Intel and seconded by Montage to authorize the TG to issue one or more ballots on the items listed on pages 3 and 4 of the presentation that have item numbers, have been shown in the committee and for which the TG has reached a consensus".

The motion passed by acclamation.

This ballot proposal is to specify LRDIMM DDR3 Memory Initialization, and has been approved by DDR3 MB TG on 11/09/2009.

Keywords: DDR3, MB, Memory Buffer, LRDIMM, Initialization

Figure 1 — Initialization Overview



* This step is optional for the MB but may be done by some platforms

EX1015 (JEDEC) at 4

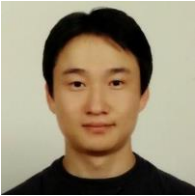
EX1037: Tally of votes in December 2009 for EX1015

Committee Letter Ballot JC-40.4-09-320 Item 142.35								
<u>Subject:</u> LRDIMM DDR3 Memory Initialization Chapter Proposal								
PATENTS: No known patent issues on the sponsor's part								
Click here for NB09320-.pdf								
Ballot distributed: 11 Nov 2009, Expired: 03 Dec 2009								
Sponsor: Mr. John Smolka Silego Technology e-mail (jsmolka@silego.com)								
NON FINAL REPORT/ Attend meeting or read minutes for final results.								
Company / voter	Y*	N*	A*	P*	C*	PC*	DoV*	DoR*
20 companies voted	15	0	5	1	1_Y			
Advanced Micro Devices Inc. Patel	Y						12/03/09	
Cray Inc. Grossmeier	Y						11/16/09	
Dell Inc. Berke	Y						12/01/09	
Elpida Memory Incorporated Ono	Y						11/26/09	
Hynix Semiconductor Kim	Y						12/02/09	
IBM Corporation Stout			A				11/20/09	
Inphi Corporation Washkewicz	Y						12/02/09	
Integrated Device Technology Inc. Franklin	Y						12/02/09	
Intel Corporation Tsang	Y				X	N/A	12/03/09	
Kingston Technology Company Inc. Cheng	Y						11/23/09	
Legacy Electronics Inc. Mecker			A				12/01/09	
Micron Technology Inc. Graham	Y						11/30/09	
Netlist Inc. Martinez			A	P			12/01/09	
Nvidia Corporation Wagner			A				12/01/09	
NXP Semiconductors Roozeboom	Y						12/01/09	
Samsung Semiconductor Park	Y						12/02/09	
Silego Technology Chung	Y						12/03/09	
Smart Modular Technologies, Inc. Marino			A				12/02/09	
Sun Microsystems Inc. Lee	Y						11/13/09	
Texas Instruments Inc. Harrieder	Y						11/30/09	
* Y = Yes, N = No, A = Abstain, P = Patent(s), C = Comments PC: Postcard, Y = approved response, N = did not approve response, N/A: not available, sponsor and / or voter did not respond, DoV: Date of Vote								

EX1037 at 21

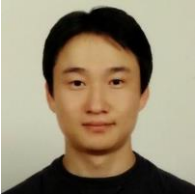
'218: Paper 1 (Pet.) at 25-27, n.5; Paper 35 (Repl.) at 2-8
 '595: Paper 1 (Pet.) at 25-26, n.7; Paper 35 (Repl.) at 2-9

Testimony of SJ Park about EX1015



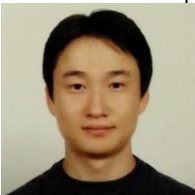
As a member of the JC-40.4 committee, Samsung and I received [EX1015] on or about November 11, 2009

EX1055 (Park), ¶7



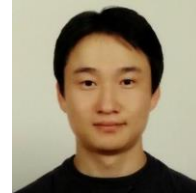
Q. And for this subcommittee in 2009, you were designated by Samsung as the representative to cast Samsung's vote; is that correct?
A. That's right.

EX2025 (Park Dep. Tr.) at 24:24-25:3



Q. In 2009, Dr. Park, did you personally go to JEDEC meetings and look at committee letter ballots and vote on committee item numbers on a regular basis as part of your work for Samsung?
THE WITNESS: Yes. That was my responsibilities.

EX2025 (Park Dep. Tr.) at 28:17-:24



Q. Dr. Park, during the 21-day review period for the committee letter ballot attached as Exhibits A and B to your declaration marked as Exhibit 1055, do you believe that you and your colleagues at Samsung actually had a copy of the document marked as Exhibit B that you and your colleagues reviewed before you personally voted in December of 2009 to approve the ballot marked as Exhibit B to your declaration?
THE WITNESS: Yes.

EX2025 (Park Dep. Tr.) at 35:18-36:4

EX1071: JEDEC meeting in December 2009

The Wayback Machine - https://web.archive.org/web/20090406143859/http://www.jedec.org:80/service_members/Meetings/09Sch.cfm



EX1071 at 1



The Standards Resource for the World Semiconductor Industry

2009 Meetings Schedule

News EX China available on Web site, click on NEWS! Videos from JEDEX Shenzhen (Ch

Download notice-agenda for:

December, 2009				
Dates	Event/ <u>Committee</u>	Location	Accommodations	Info
Dec 7-Dec 11	<u>JC-16</u> , <u>40</u> , 42, 45, 63 & 64	Maui, HI	Grand Wailea	

September, 2009				
Dates	Event/Committee	Location	Accommodations	Info
Sept 14-15	JEDEC	San Jose, CA	San Jose Marriott	
Sept 16-17	JEDEC	San Jose, CA	San Jose Marriott	
Sept 18-19	JEDEC	San Jose, CA	San Jose Marriott	
October, 2009				
Dates	Event/Committee	Location	Accommodations	Info
Oct 1-2	JEDEC	San Jose, CA	San Jose Marriott	
Oct 3-4	JEDEC	San Jose, CA	San Jose Marriott	
Oct 5-6	JEDEC	San Jose, CA	San Jose Marriott	
November, 2009				
Dates	Event/Committee	Location	Accommodations	Info
Nov 1-2	JEDEC	San Jose, CA	San Jose Marriott	
Nov 3-4	JEDEC	San Jose, CA	San Jose Marriott	
Nov 5-6	JEDEC	San Jose, CA	San Jose Marriott	

EX1071 at 2

'218: Paper 1 (Pet.) at 25-27, n.5; Paper 35 (Repl.) at 2-8
'595: Paper 1 (Pet.) at 25-26, n.7; Paper 35 (Repl.) at 2-9

JEDEC proposals like EX1015 were not confidential

11. While I participated in JEDEC on Intel's behalf, there was no rule or other requirement that members treat ballots, technology presentations, or meeting minutes as confidential. Rather, these documents were freely disclosed and distributed within JEDEC's committees and subcommittees between JEDEC members manufacturing memory related products. JEDEC members are expected to discuss proposed technology — such as in ballots, technology presentations or meeting minutes — within their company and among all third-parties interested in interoperability of memory related products. These disclosures are required to determine the feasibility of implementing the proposed standard and also for determining whether other technology might be preferred for standardization. Were confidentiality restrictions in place, JEDEC members would be unable to carry out the purpose of JEDEC, which is to design products that can interoperate with each other.

EX1054 (Halbert) at ¶11

Q Are you aware of any nondisclosure agreements that JEDEC had with anyone?

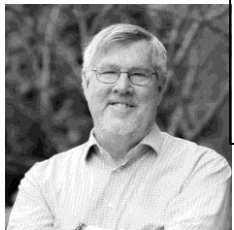
THE WITNESS: No.

EX2022 (Halbert Dep. Tr.) at 56:1-:5 (objections omitted)

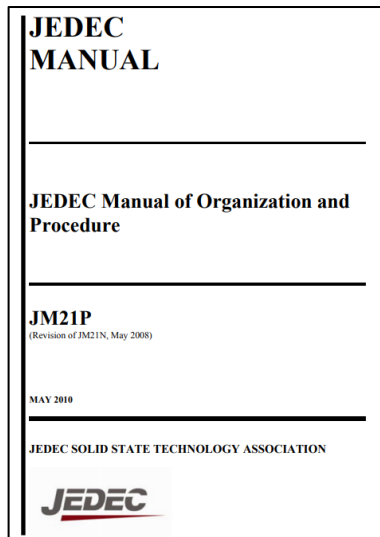
Q At any of the JEDEC meetings that you attended, between 2001 and 2017, do you ever recall being instructed by anyone that you had to keep the information learned at that meeting a secret?

THE WITNESS: No.

EX2022 (Halbert Dep. Tr.) at 56:14-:20 (objections omitted)



JEDEC proposals are Copyrighted, but not confidential (only surveys are confidential)



EX1048 (JM21P) at 15, 19-20

7 JEDEC documents

JEDEC documents are available from the JEDEC website: www.jedec.org. JEDEC documents may not be sold without written authorization from JEDEC.

6.7 Survey ballots

Surveys may be issued to determine whether a proposal warrants further action. A survey may ask for information or for a support/nonsupport position. No committee vote is required for the distribution of a survey ballot; however, every survey must be approved by the committee chairperson and issued by the JEDEC Office following legal approval. The JEDEC Office shall monitor every survey to ensure adherence to JEDEC legal guidelines. Surveys that contain company-sensitive material that must remain confidential shall be stripped of any reference to a company by the JEDEC Office prior to use of the material. In all cases, survey results shall be presented to the full committee at the first meeting following the voting period expiration date.

4.1 Copyrights

JEDEC owns the copyright to all documents created through JEDEC, and use of that copyrighted material is at the sole discretion of the JEDEC Board.

JEDEC member companies may reproduce any JEDEC document for internal use, without restriction. Use of JEDEC material outside of member companies is at the discretion of the Board. Generally, all JEDEC documents are available on the JEDEC website: www.jedec.org.

Copyright ≠ Confidential



\$1.50

Public accessibility is **not limited** to circumstances of **free** or academic distributions.

Centripetal Networks, Inc. v. Cisco Sys., Inc., 847 Fed. Appx. 869, 878 (Fed. Cir. Mar. 10, 2021) (emphasis added)



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Netlist's expert agrees JEDEC proposals were disseminated to POSITAs (even if not members of JEDEC)



Q. In forming your opinions in this matter, did you believe a person of ordinary skill in the art would have known about JEDEC, the organization?

A. In forming my opinion in this matter, I used the opinion that JEDEC would have been known to one of ordinary skill in the art, yes.

Q. And you believe that's the correct opinion?

A. I think for this matter it is, yes.

EX1077 (Murphy Dep. Tr.) at 49:12-:19



Q. In your opinion would a person of ordinary skill in the art have known about the contents of presentations and proposals to JEDEC relevant to memory modules and memory devices, for example, by a word-of-mouth in the industry even if they did not have copies of those presentations and proposals to JEDEC?

THE WITNESS: Yes, I believe that that would have been the case, and that is so reflected in my declaration.

EX1077 (Murphy Dep. Tr.) at 55:8-:20



Q. And specifically with respect to the JEDEC proposals and presentations for LR-DIMM, you believe that a person of ordinary skill in the art would have been familiar with the contents of the proposals and presentation to JEDEC about LR-DIMM regardless of whether they actually had a copy of those proposals and presentations?

THE WITNESS: I believe I just answered that, and it is stated in my declaration as effectively a basis for my opinion that one of ordinary skill in the art would understand about the content that was available in the JEDEC proposals independent of how they got that information.

EX1077 (Murphy Dep. Tr.) at 55:22-56:11

Netlist's expert agrees JEDEC proposals were disseminated to POSITAs (even if not members of JEDEC)



18 Q. In your opinion would a person of ordinary
19 skill in the art know that the MB on a DDR3 LR-DIMM
20 refers to a Memory Buffer that buffers data, address
21 and command signals?
22 A. Yes. Based on the information, they would
23 have known via the word of mouth, et cetera, from the
24 JEDEC proposal, Exhibit 1015.

EX1077 (Murphy Dep. Tr.) at 133:18-24



18 Q. In your opinion would a person of ordinary
19 skill in the art have known about the JEDEC standards
20 relevant to memory modules and memory devices?
21 A. Yes. With respect to my opinion in this
22 matter that is -- that is what I believe we're
23 discussing in this matter.
24 Q. In your opinion would a person of ordinary
25 skill in the art have known about the presentations
1 and proposals to JEDEC relevant to memory modules and
2 memory devices?

5 THE WITNESS: Yes. In this matter I believe
6 a person of ordinary skill in the art would know
7 those things.

EX1077 (Murphy Dep. Tr.) at 51:18-52:7



1 Q. In your opinion would a person of ordinary
2 skill in the art have known about the proposed JEDEC
3 standards for DDR3 LR-DIMM memory modules?

4 A. As I have stated in my report -- in my
5 declaration, sorry -- it is -- it is something that I
6 agree to that one of ordinary skill in the art would
7 have known about a DDR3 LR-DIMM module.

8 Q. And would they have known about the
9 proposals within JEDEC concerning standards for the
0 DDR3 LR-DIMM memory module?

3 THE WITNESS: With respect to the JEDEC
4 standards, It's my belief that the -- that one of
5 ordinary skill in the art, as I've stated in my
6 declaration, would have understand [sic] the content
7 of those proposals, even though they may not have
8 been specifically in JEDEC or on the committee.

EX1077 (Murphy Dep. Tr.) at 62:1-18

218: Paper 35 (Repl.) at 5

595: Paper 35 (Repl.) at 5

Dr. Yang's hearsay about "confidentiality" should be excluded

Paragraphs 20-21 of EX2026 (Declaration of Dr. Yang) should be excluded under FRE 602 and FRE 801-802



20. Both in the 2009-2010 timeframe and throughout my time at JEDEC, it was understood and the practice of JEDEC members that committee ballots were treated as confidential within the committee.¹ Of course, I and other JEDEC member representatives would discuss technology proposals or ballots internally and among committee members as necessary to determine how to vote or comment on proposals.² But it was understood that pending committee ballots could not be distributed *outside* of the relevant group of JEDEC members to other, non-JEDEC entities. This is further reflected by the fact that, as noted above, access to ballots

EX2026 (Yang) at ¶20

- **Hearsay**
- **Not personal knowledge**
(he was not a member of JC-40)



21. In my entire experience, including my many years at Intel where I worked with Mr. Halbert, I have never heard of any JEDEC committee ballot being distributed or sent to a non-JEDEC member (that is, to a third party) prior to any standard being formally adopted. This would have been improper, and I see in Mr. Halpert's deposition that he agrees with me on this point. 7/22/22 Halbert Depo. Tr. [Exhibit 2022] at 23:14–17. When Mr. Halbert states in his declaration (paragraph 11) that ballots were discussed "among all third-parties," I do not understand him to be saying that the ballots themselves were circulated to third-parties (versus technical issues related to such being discussed). And Mr. Halbert clarified in his deposition that his understanding matches mine that ballots were *not* distributed to third parties. Exhibit 2022 at 23:14–17. Regardless, as I note above, I am not aware of any instance when the content of JEDEC ballots were ever shared with third parties, much less the ballots themselves being distributed to third parties.

EX2026 (Yang) at ¶21

218: Paper 46 (Pet. MTE) at 6-15; Paper 50 (Repl. ISO MTE) at 3-5

595: Paper 46 (Pet. MTE) at 6-15; Paper 50 (Repl. ISO MTE) at 3-5

Samsung Electronics Co., Ltd., Ex. 1082, p. 58

58

Dr. Yang's declaration about "confidentiality," if not excluded, should be given no weight

- Dr. Yang does not disclose any support for his statements about "confidentiality":

"Opinions expressed without disclosing the underlying facts or data may be given **little or no weight**"

Consolidated Trial Practice Guide (Nov. 2019) at 35, 40-41; see also 37 C.F.R. § 42.65(a)



- Dr. Yang's declaration is inconsistent with JEDEC's manuals of procedure (EX1048-49), which do not require proposals to be "confidential"
- Dr. Yang's declaration is inconsistent with EX1015, which is not marked "confidential"
- Dr. Yang's declaration is inconsistent with the testimony of John Halbert (EX2022 at 56:1:20) and Netlist's own technical expert, Mr. Murphy (EX1077 at 49:12-62:18)
- Dr. Yang's declaration is irrelevant, because the legal standard under *GoPro* is "accessibility," not actually received, and Dr. Yang does not dispute that a POSITA easily could have joined JEDEC to get access to EX1015:

[W]e explained that '[a]ccessibility goes to the issue of whether interested members of the relevant public could obtain the information **if they wanted to**' and '[i]f accessibility is proved, there is **no requirement to** show that particular members of the public **actually received** the information.'

GoPro, Inc. v. Contour IP Holding LLC., 908 F.3d 690, 693 (Fed. Cir. 2018) (emphasis added)

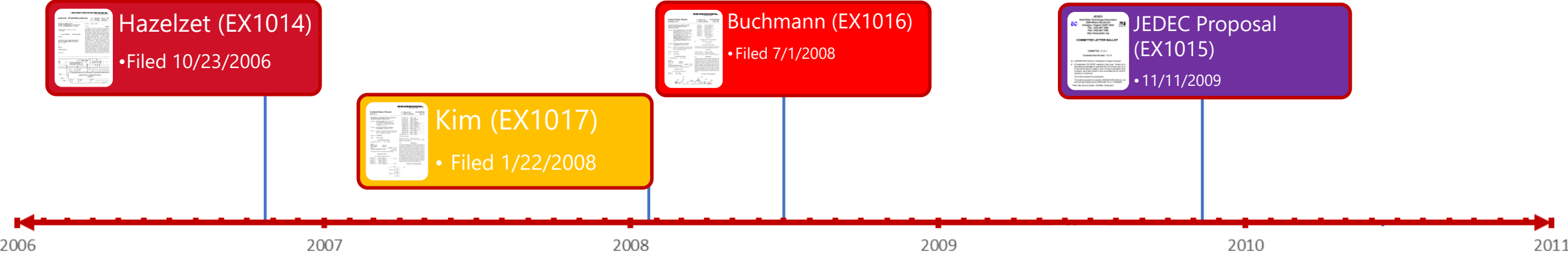


OBVIOUSNESS OF THE 218 AND 595 PATENTS

04

OVERVIEW OF THE PRIOR ART

Prior Art for Grounds 1-3



Grounds	'218 Claims	'595 Claims	Prior art
1	Claims 1-22	Claims 1-24	Hazelzet and JEDEC (EX1015)
2	Claims 1-22	Claims 1-24	Hazelzet and Buchmann
3	Claims 3-6, 10-12, 17-20	Claims 3-7, 12-14, 20, 22, 23	Hazelzet and (JEDEC or Buchmann), and Kim

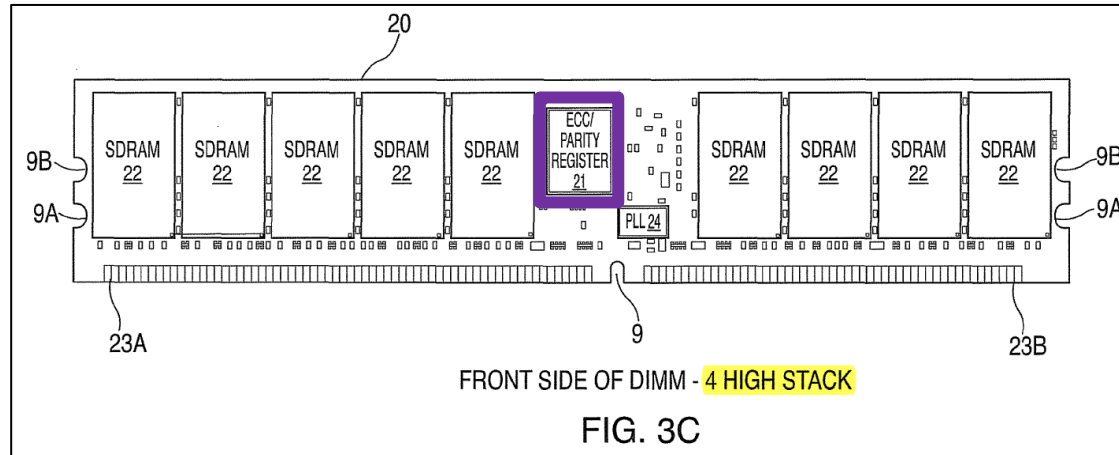
'218: Paper 1 (Pet.) at 4, 24-30

'595: Paper 1 (Pet.) at 4, 24-30

Hazelzet (U.S. Patent Pub. No. 2008/0098277) [EX1014]

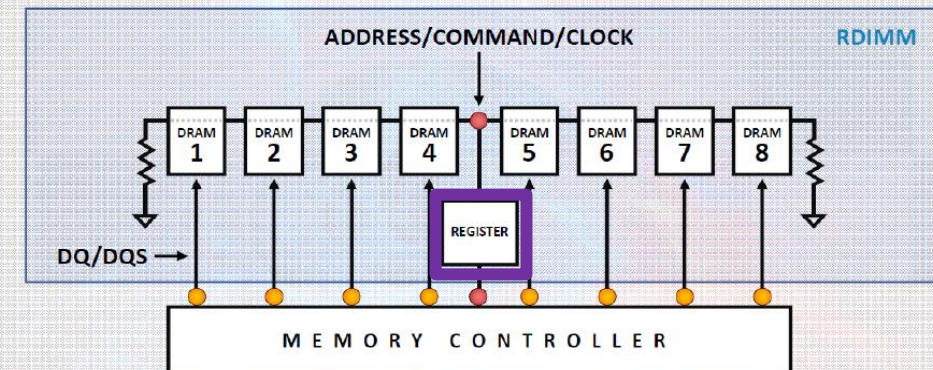
Hazelzet discloses a memory module including **four ranks** of memory in **RDIMM** format, where a **register** buffers address/command/clock signals, but not data signals (DQ/DQS)

Hazelzet [EX1014] Figure 3C



RDIMM from Netlist's Technology Tutorial

Evolution of DIMMs: JEDEC Registered DIMM (RDIMM)

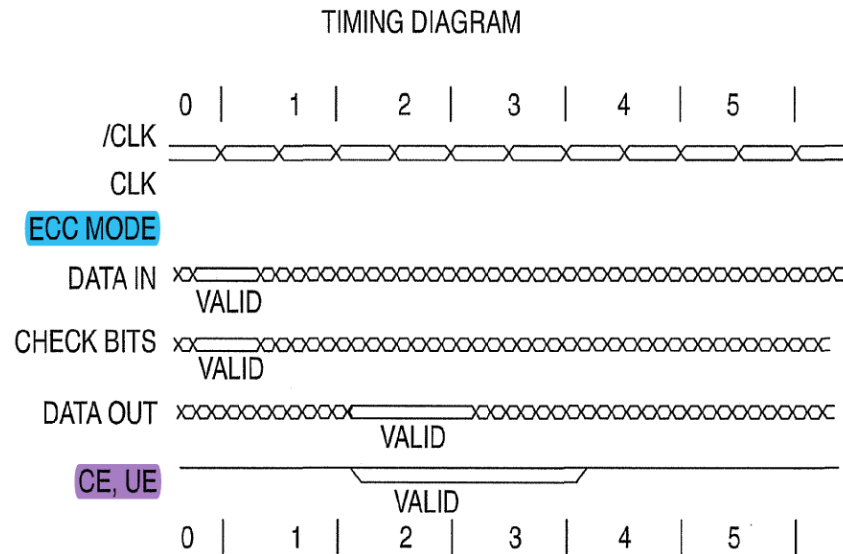


EX1079, 8; EX1077, 61:19-:25, 77:11-:20, 81:16-83:20, 84:14-86:21.

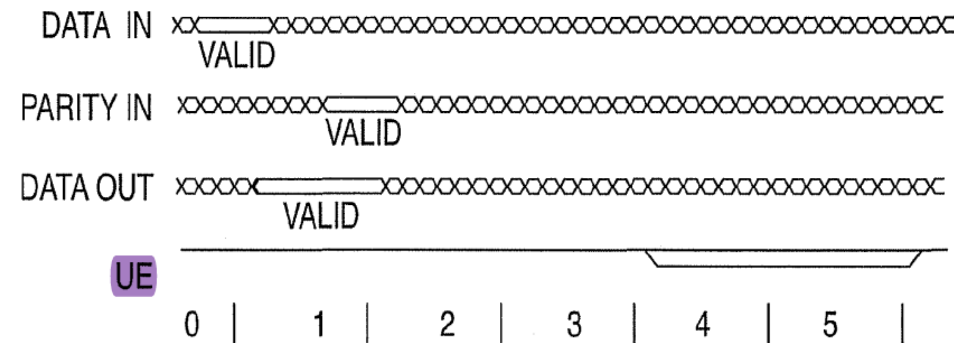
218: Paper 1 (Pet.) at 24-25, 37; EX1003 (Alpert Decl.) at ¶¶ 118-123
595: Paper 1 (Pet.) at 24-25, 35; EX1003 (Alpert Decl.) at ¶¶ 139-144

Hazelzet (U.S. Patent Pub. No. 2008/0098277) [EX1014]

Hazelzet's memory module can operate in **multiple modes**, and uses **open-drain outputs CE** (correctable error) and **UE** (uncorrectable error) to report errors to the host



PARITY MODE



NOTES: CS GATING DISABLED

PARITY IN AND CHECK BIT 0 SHARE A COMMON PIN (CHK0/ PARITY_IN)

IF AN ERROR OCCURS, CE OR UE ARE DRIVEN LOW

FIG. 8

EX1014 (Hazelzet) at Fig. 8, [0072]

[0072] Error reporting circuitry is included to permit external monitoring of DIMM operation. Two open-drain outputs are available to permit multiple modules to share a common signal line for reporting an error that occurred during a valid command (/CS=low) cycle (consistent with the re-driven signals). These two outputs are driven low for

218: Paper 1 (Pet.) at 24-25; EX1003 (Alpert Decl.) at ¶¶ 118-123

595: Paper 1 (Pet.) at 24-25; EX1003 (Alpert Decl.) at ¶¶ 139-144

JEDEC proposal [EX1015]

JEDEC
Solid State Technology Association
2500 Wilson Boulevard
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TEL: (703) 907-7560
FAX: (703) 907-7583
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EIA
Electronic Industries Alliance

COMMITTEE LETTER BALLOT

COMMITTEE: JC-40.4
Committee Item Number: 142.35

Subject: LRDIMM DDR3 Memory Initialization Chapter Proposal

Background: At September '09 JEDEC meeting in San Jose, "motion by Intel and seconded by Montage to authorize the TG to issue one or more ballots on the items listed on pages 3 and 4 of the presentation that have item numbers, have been shown in the committee and for which the TG has reached a consensus".

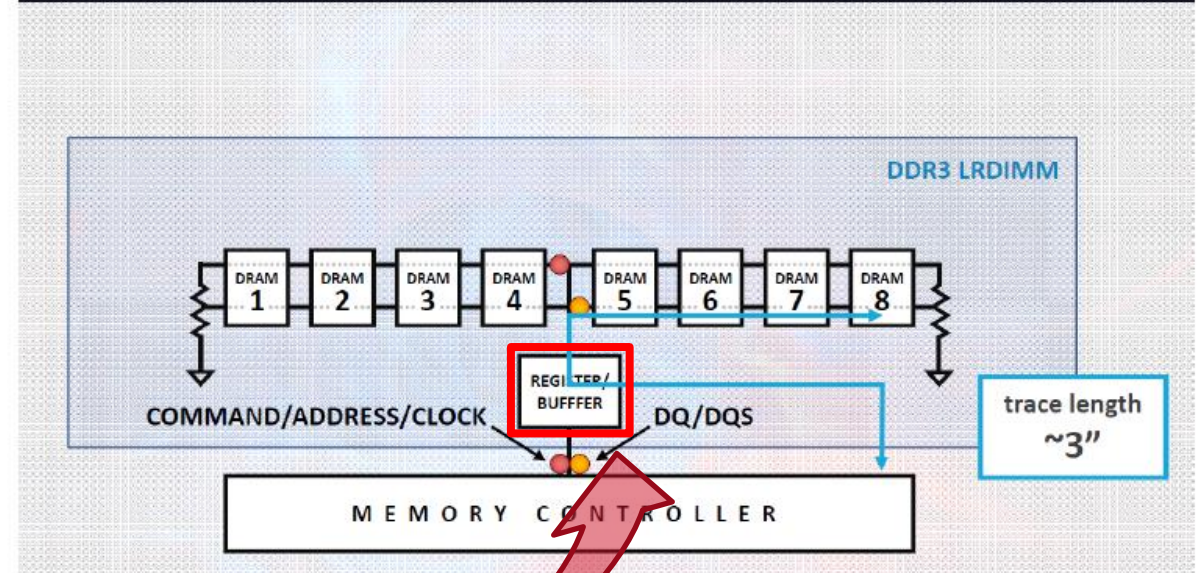
The motion passed by acclamation.

This ballot proposal is to specify LRDIMM DDR3 Memory Initialization, and has been approved by DDR3 MB TG on 11/09/2009.

Keywords: DDR3, MB, Memory Buffer, LRDIMM, Initialization

EX1015 at 1

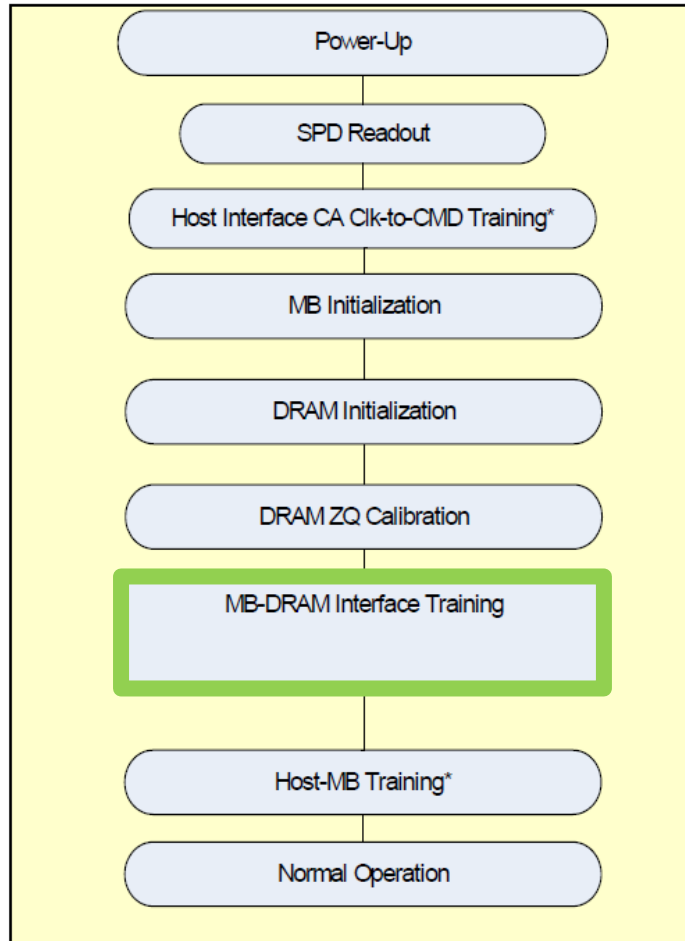
Evolution of DIMMs: JEDEC DDR3 LRDIMM (Gen1)



EX1079, 10; EX1077, 61:5-:10, 62:1-:18, 90:9-93:4.

JEDEC proposal [EX1015]

Figure 1 — Initialization Overview



* This step is optional for the MB but may be done by some platforms

EX1015 at 4

6.7 MB-DRAM Training

After all the DRAMs are fully operational, the host triggers the DRAM interface training by setting the control bit DA4 in F0RC12. Once enabled, the MB assumes autonomous control of the Command/Address, Control and Data/Strobe signals to the DRAMs, without any further assistance from the host.

The MB performs ‘Write Leveling’ to the DRAMs to ensure successful writes, and ‘Read Enable Training’ to ensure it can capture read data from the DRAMs correctly, as part of the DRAM interface training.

No DRAM commands or control word writes (either over the Command/Address and Control buses or via SMBus) can be issued to the MB until the MB-DRAM Interface training is complete and the DODTn inputs must be kept low. The MB responds to SMBus CSR read accesses whether or not DRAM interface training is active. To determine DRAM interface training completion the host may either wait for a time ‘tCAL * number of physical ranks’ (which is the maximum amount of time that the MB-DRAM Interface training is allowed to take) or it may periodically poll the content of the MB CSR ‘Training Completion’ (see ‘Configuration Registers’ chapter) over the SMBus.

In addition, training completion can be signaled by the assertion of ERROUT#. This is not the power-up default but can be enabled by setting the DBA1 bit in the F3RC14 Training Completion Control Word.

EX1015 at 8

DDR3 SDRAM LRDIMM Design Specification Pinout and Description

Load Reduced DIMM Input/Output Functional Description

ErrOut_n	OUT (open drain)	Parity error detected on the Address and Command bus. A resistor may be connected from ErrOut_n bus line to V _{DD} on the system planar to act as a pull up.
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EX1036 at 9

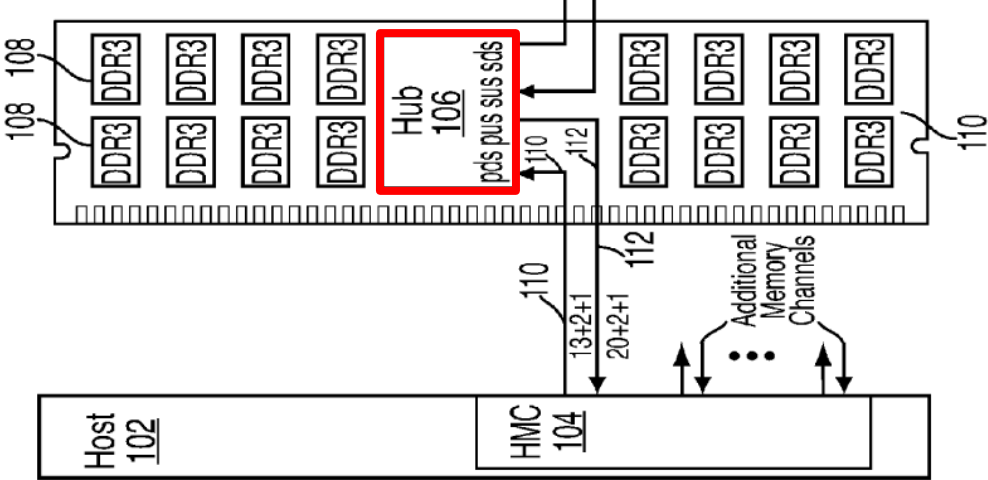
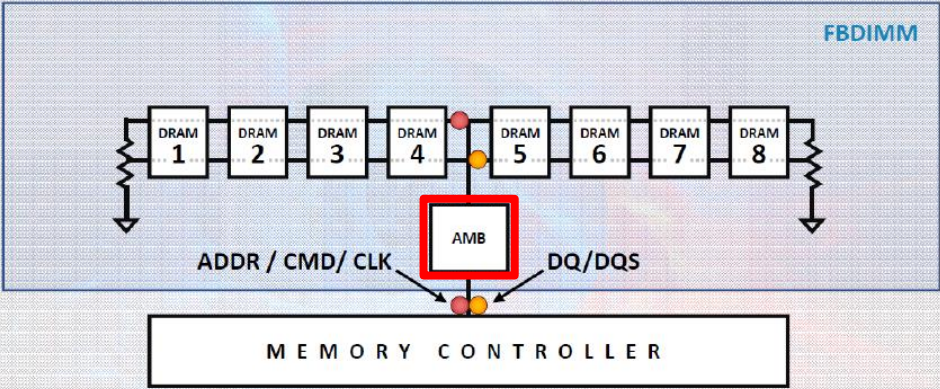
‘218: Paper 1 (Pet.) at 25-32; Paper 35 (Reply) at 27

‘595: Paper 1 (Pet.) at 25-30; Paper 35 (Reply) at 27

Samsung Electronics Co., Ltd., Ex. 1082, p. 66

Buchmann (U.S. Patent No. 8,139,430) [EX1016]

Buchmann discloses a memory module (110) with **DDR3 memories** in **FBDIMM** format including a **memory buffer** (106) that buffers **data**/address/command/clock signals.

Buchmann [EX1016] Figure 1	FBDIMM from Netlist's Technology Tutorial
 The diagram illustrates a memory module 110. It features a central Hub 106, highlighted with a red box, which is connected to multiple DDR3 memory modules 108. The Hub 106 is also connected to a Host 102 and an HMC 104. The Host 102 and HMC 104 are connected to the module via a bus 110. The bus 110 is divided into two sections: a top section 112 and a bottom section 114. The top section 112 is connected to the Host 102, and the bottom section 114 is connected to the HMC 104. The Hub 106 is connected to the bus 110 via a connection 111. The Hub 106 is also connected to the DDR3 memories 108 via a connection 113. The Hub 106 is labeled 'Hub 106' and 'pds plus sus sds'. The Host 102 is labeled 'Host 102' and the HMC 104 is labeled 'HMC 104'. The DDR3 memories 108 are labeled 'DDR3'. The bus 110 is labeled '110' and the sections 112 and 114 are labeled '112' and '114' respectively. The connection 111 is labeled '111' and the connection 113 is labeled '113'. The diagram also shows 'Additional Memory Channels' and a 'Host 102'.	 The diagram illustrates the evolution of DIMMs: Fully-Buffered DIMM (FBDIMM). It shows a sequence of DRAM modules (1-8) connected to a Memory Controller via an AMB (Address Memory Buffer). The AMB is highlighted with a red box. The Memory Controller is connected to the AMB via a bus. The bus is labeled 'ADDR / CMD / CLK' and 'DQ/DQS'. The DRAM modules are labeled 'DRAM 1' through 'DRAM 8'. The AMB is labeled 'AMB'. The Memory Controller is labeled 'MEMORY CONTROLLER'. The diagram is titled 'FBDIMM' and 'Evolution of DIMMs: Fully-Buffered DIMM (FBDIMM)'. Below the diagram, the text 'EX1079, 9; EX1077, 61:11-:18, 87:1-90:5' is displayed.

218: Paper 1 (Pet.) at 30-31; EX1003 (Alpert Decl.) at ¶¶ 127-134
595: Paper 1 (Pet.) at 28-30; EX1003 (Alpert Decl.) at ¶¶ 148-155

Buchmann (U.S. Patent No. 8,139,430) [EX1016]

Buchmann discloses a **power-on initialization mode** of its module that includes training sequences, such as **TS0** for clock detection and repair and **TS3** for upstream lane training, performed by the memory buffer, which notifies the Host that the training is done (**TS_done**).

TABLE 1

Static Bit Communication commands used during TS0	
Name	Description
TS0_pdsck	This command causes the downstream receiver logic to enter the TS0 state, reset its memory channel PLLs and select the PDSCK clock as the MB reference clock. This SBC is not forwarded.
TS0_pdss0	This command signals the downstream receiver to reset its memory channel PLLs and select the spare clock, PDSS0 as the MB reference clock. This SBC is not forwarded.
TS0_pusck	This command signals the MB PUS Tx logic to select the PUSCK as the returned bus clock and to deactivate the PUSS0 spare clock.
TS0_puss0	This command signals the MB PUS Tx logic to select the PUSS0 as the returned bus clock and to deactivate the PUSCK clock.
TS_done	This response indicates the local and all cascaded MBs are done with TS0.

TABLE 5

Static Bit Communication commands used during TS3	
Name	Description
TS3_annc	This command announces the beginning of TS3a. This SBC is corrected and forwarded by MBs in the memory channel.
TS3_ack	This response indicates that all downstream MBs have returned the TS3a_ack SBC, The last MB issues this response upon detecting the TS3a_annc.
TS_[clk,data]	Clock and data SBC is used to send the 32 bit lane repair vector to the MB/host immediately downstream in the memory channel.
TS_done	This response indicates the local and all cascaded MBs are done with TS2.

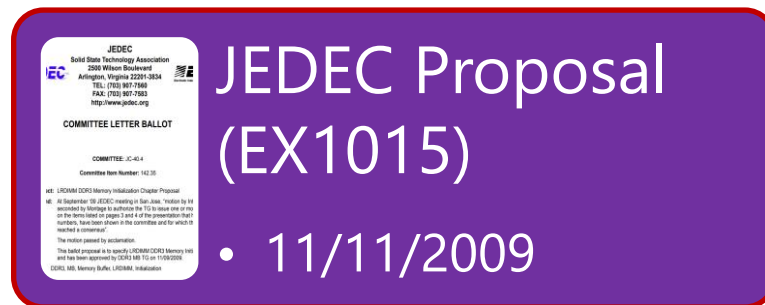
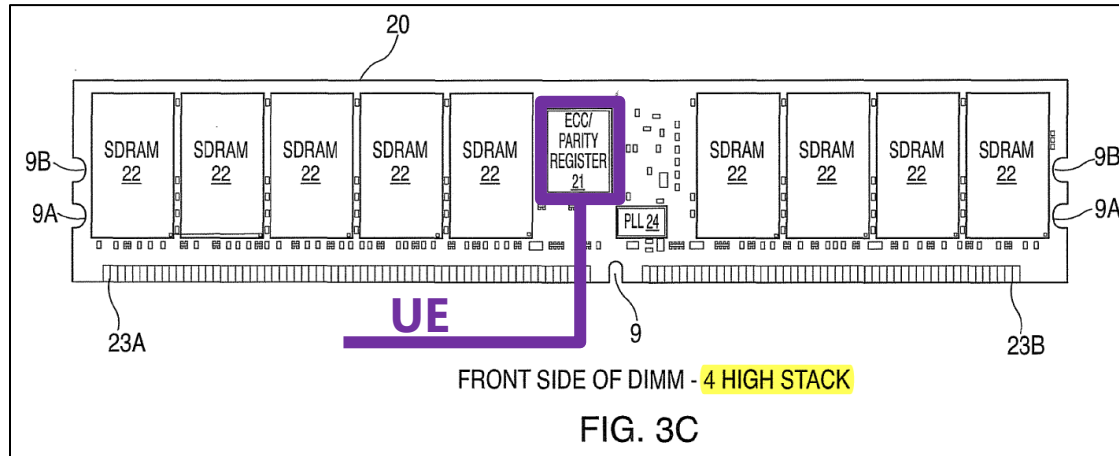
EX1016, 8:30-45

EX1016, 6:1-22

218: Paper 1 (Pet.) at 30-31; EX1003 (Alpert Decl.) at ¶¶ 127-134
595: Paper 1 (Pet.) at 28-30; EX1003 (Alpert Decl.) at ¶¶ 148-155

COMBINATIONS FOR GROUNDS

Ground 1: Hazelzet + JEDEC



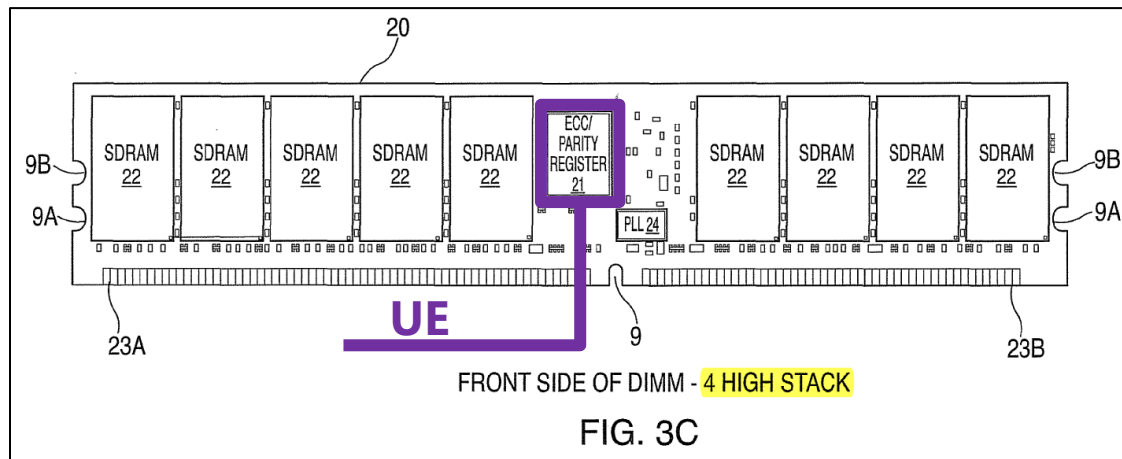
Hazelzet

- DIMM module with 4 ranks of memory
- Error reporting on open-drain outputs like UE
- Operating in different modes
 - Each mode using the same open-drain outputs for reporting

JEDEC

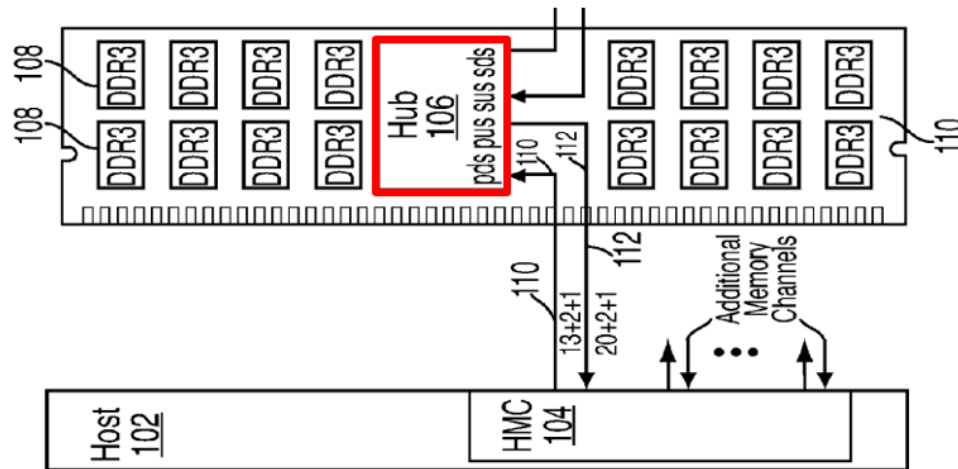
- Data buffering to lower load on DIMM module
- Operating in initialization and normal modes
- Uses same open-drain output (ERROUT) to report error in normal mode, and training completion in initialization mode

Ground 2: Hazelzet + Buchmann



Hazelzet

- DIMM module with 4 ranks of memory
- Error reporting on **open-drain outputs** like **UE**
- Operating in different modes
 - Each mode using the same **open-drain outputs** for reporting



Buchmann

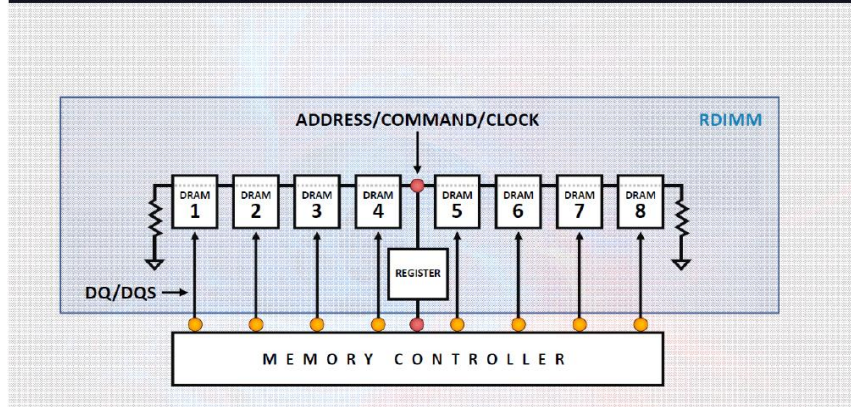
- **Data buffering** to lower load on DIMM module
- Operating in initialization and normal modes
- Reports training completion in initialization mode

#1: Adding data buffering to Hazelzet was obvious

Adding data buffering (e.g., from Buchmann or JEDEC's DDR3 LRDIMM) to Hazelzet would:

- lower the load of Hazelzet's RDIMM with four ranks of memory
- thereby increasing performance and capacity

Evolution of DIMMs: JEDEC Registered DIMM (RDIMM)

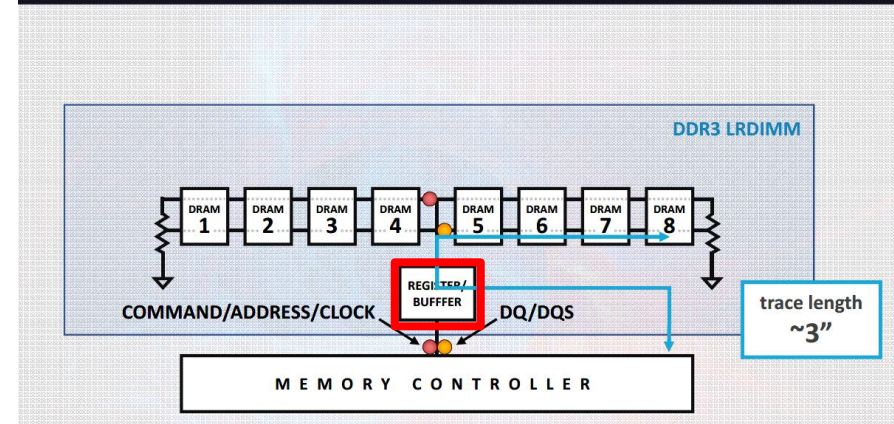


EX1079, 8; EX1077, 61:19-:25, 77:11-:20, 81:16-83:20, 84:14-86:21.

The LRDIMM differs from RDIMMs in that the SDRAMs do not connect directly to the edge connector with the exception of VDD and VSS (ground). The Memory Buffer (MB) buffers both address and data. Increased performance is achieved based on the LRDIMM presenting only one load to the system. Increased capacity is achieved since the MB drives only the SDRAMs on the module and therefore a well defined topology and load. The maximum number of SDRAM die is 144. The LRDIMM is intended to function in all RDIMM platforms with appropriate BIOS changes. Systems designed to function with LRDIMMs will be better able to take advantage of LRDIMM features.

EX1036, 5

Evolution of DIMMs: JEDEC DDR3 LRDIMM (Gen1)



EX1079, 10; EX1077, 90:9-25

'218: Paper 1 (Pet.) at 35-42; Paper 35 (Repl.) at 15-30

'595: Paper 1 (Pet.) at 33-40; Paper 35 (Repl.) at 15-30

#2: Adding training to initialization mode was obvious

Adding data training (e.g., from JEDEC or Buchmann) to Hazelzet's initialization would:

- ensure proper operation and communication for memory operations
- optimize read and write operations, thereby providing reliable performance during subsequent normal operation

The MB performs 'Write Leveling' to the DRAMs to ensure successful writes, and 'Read Enable Training' to ensure it can capture read data from the DRAMs correctly, as part of the DRAM interface training.

EX1015, 8

MB DRAM interface training must be completed before any MB host interface read or write training to ensure that the MB DRAM interface is configured optimally for DRAM reads and writes. The host

EX1015, 9

3 Channel Initialization

This chapter defines the process of initializing the FBD channel. The FBD initialization process generally follows the top to bottom sequence of state transitions shown in the high level AMB Initialization Flow diagram in Figure 3-4. The host must sequence the AMB devices through the Disable, Calibrate, (back to Disable), Training, Testing, and Polling states in order to transition the AMBs into the active channel L0 state. The value in parenthesis in each state bubble indicates the condition/activity of the links during these states.

EX1025, 15

'218: Paper 1 (Pet.) at 35-42; Paper 35 (Repl.) at 15-30

'595: Paper 1 (Pet.) at 33-40; Paper 35 (Repl.) at 15-30

#3: Using open drain for training notifications was obvious

- Open-drain output shared by multiple modules obvious choice to provide “wired-or” function
- Pre-existing open-drain outputs, not being used during training, obvious choice to use for training notifications
- JEDEC teaches using open-drain error reporting pin for training notification during initialization

In addition, training completion can be signaled by the assertion of ERROUT#.

present invention. In alternate exemplary embodiments, other functions also share the error feedback pin (e.g., parity or CRC error(s) on command and address information).

EX1015 (JEDEC) at 8

EX1017 (Kim) at 6:16-18

[0123] Initialization of the memory subsystem may be completed via one or more methods, based on the available interface busses, the desired initialization speed, available space, cost/complexity objectives, subsystem interconnect structures, the use of alternate processors (such as a service processor) which may be used for this and other purposes, etc. In one embodiment, the high speed bus may be used to complete the initialization of the memory subsystem(s).

EX1014 (Hazelzet), [0123]

[0072] Error reporting circuitry is included to permit external monitoring of DIMM operation. Two open-drain outputs are available to permit multiple modules to share a common signal line for reporting an error that occurred during a valid command (/CS=low) cycle (consistent with the re-driven signals). These two outputs are driven low for

EX1014 (Hazelzet), [0072]

'218: Paper 1 (Pet.) at 35-42; Paper 35 (Repl.) at 15-30

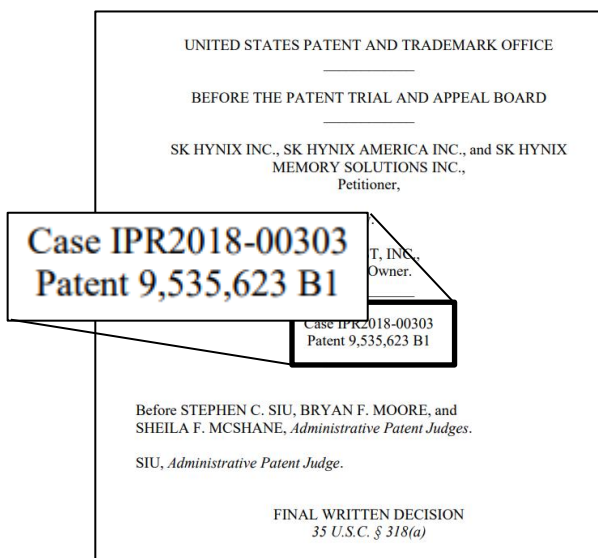
'595: Paper 1 (Pet.) at 33-40; Paper 35 (Repl.) at 15-30

NETLIST IS PRECLUDED FROM CHALLENGING GROUND 2

HAZELZET + BUCHMANN

Collateral estoppel precludes Netlist on Ground 2

Netlist is precluded by the Final Written Decision in IPR2018-00303 (623 patent) from challenging the combination of Hazelzet + Buchmann



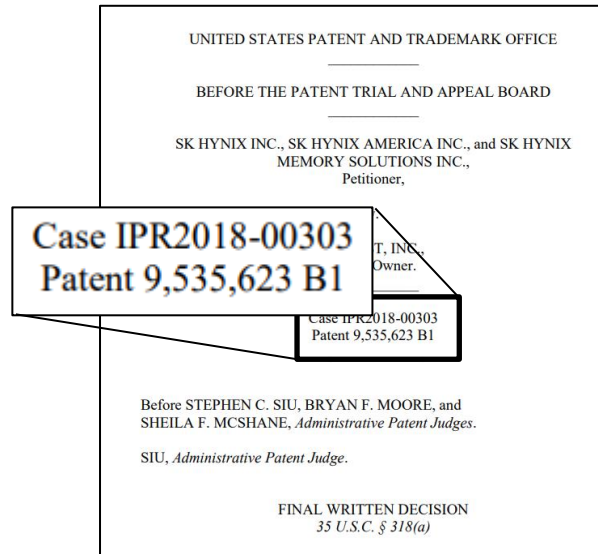
EX1034 (IPR2018-00303 FWD)
at 12-13 (Mar. 21, 2019)

We agree with Petitioner that **Buchmann** and Talbot are **analogous art** to **Hazelzet** and the '623 patent because they are all directed to the field of error detection and correction in memory modules. Pet. 59, 63. We also agree with Petitioner that it would have been obvious to one of ordinary skill in the art to have **combined** the known memory system containing a memory controller connected to a memory module that may operate in more than one mode (e.g., **Hazelzet, Buchmann,** or Talbot), including a known mode in which the memory module performs a training sequence, to notify (send a **notification signal** to) the memory controller of the **status of the training** sequence (e.g., **Buchmann** or Talbot) in order to improve overall reliability. *Id.* at 59–61, 63–64. Dr. Alpert's testimony supports that the combination of **Hazelzet** with **Buchmann** or Talbot would achieve the **predictable and expected result** of a known (multi-mode) memory system containing known components of a memory controller connected to a memory module performing a known function of executing a training sequence and notifying the memory controller of the status of the training sequence (e.g., **Buchmann** or Talbot). Ex. 1003 ¶¶ 159, 175. "The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *KSR*, 550 U.S. at 416.

Notwithstanding Patent Owner's contrary arguments, which we discuss below, we agree with Petitioner's showing that the combination of **Hazelzet** and any one of **Buchmann** or Talbot teaches every limitation of claims 1, 12, and 21 of the '623 patent and that a person of ordinary skill in the art would have had reason, with rational underpinning, to combine the references. Further, we credit Dr. Alpert's supporting testimony (Ex. 1003 ¶¶ 121–150, 158–186), as it is consistent with the prior art disclosures.

Collateral estoppel precludes Netlist on Ground 2

Netlist is precluded by the Final Written Decision in IPR2018-00303 (623 patent) from challenging the combination of Hazelzet + Buchmann



EX1034 (IPR2018-00303 FWD)
at 12-13 (Mar. 21, 2019)

A patent applicant or owner is precluded from ***taking action inconsistent with the adverse judgment, including*** obtaining in any patent:

(i) A claim that is ***not patentably distinct*** from a finally refused or canceled claim; or

37 C.F.R. § 42.73(d)(3) (emphasis added); see also *Arthrex, Inc. v. Smith & Nephew, Inc.*, 880 F.3d 1345, 1350 (Fed. Cir. 2018)

It is well established that ***patent claims need not be identical*** for collateral estoppel to apply....[C]ollateral estoppel may apply even if the patent claims “use slightly different language to describe substantially the same invention,” ***so long as “the differences between the unadjudicated patent claims and adjudicated patent claims do not materially alter the question of invalidity.”*** Whether the differences between the patent claims materially alter the question of patentability is a ***legal conclusion*** based on underlying facts.

Google LLC v. Hammond Dev. Int'l, Inc., 54 F.4th 1377, 1381 (Fed. Cir. 2022)
(citations omitted)



Collateral estoppel precludes Netlist on Ground 2

Netlist is precluded by the Final Written Decision in IPR2018-00303 (623 patent) from challenging the combination of Hazelzet + Buchmann

'623 patent (Jan. 3, 2017) [EX1031]	'218 patent (Jan. 2, 2018) [EX1001]	'595 patent (Nov. 12, 2019) [EX1001]
(21) Appl. No.: 15/169,745 (22) Filed: Jun. 1, 2016 Related U.S. Application Data (63) Continuation of application No. 15/088,115, filed on Apr. 1, 2016, which is a continuation of application No. 13/942,721, filed on Jul. 16, 2013, now Pat. No. 9,311,116, which is a continuation of application No. 12/815,339, filed on Jun. 14, 2010, now Pat. No. 8,489,837. (60) Provisional application No. 61/186,799, filed on Jun. 12, 2009.	(21) Appl. No.: 15/088,115 (22) Filed: Apr. 1, 2016 Related U.S. Application Data (63) Continuation of application No. 13/942,721, filed on Jul. 16, 2013, now Pat. No. 9,311,116, which is a continuation of application No. 12/815,339, filed on Jun. 14, 2010, now Pat. No. 8,489,837. (60) Provisional application No. 61/186,799, filed on Jun. 12, 2009.	(21) Appl. No.: 15/857,553 (22) Filed: Dec. 28, 2017 Related U.S. Application Data (63) Continuation of application No. 15/088,115, filed on Apr. 1, 2016, now Pat. No. 9,858,218, which is a continuation of application No. 13/942,721, filed on Jul. 16, 2013, now Pat. No. 9,311,116, which is a continuation of application No. 12/815,339, filed on Jun. 14, 2010, now Pat. No. 8,489,837. (60) Provisional application No. 61/186,799, filed on Jun. 12, 2009.

218: Paper 1 (Pet.) at 43; Paper 35 (Repl.) at 14-15

595: Paper 1 (Pet.) at 13-14

Collateral estoppel precludes Netlist on Ground 2

Netlist is precluded by the Final Written Decision in IPR2018-00303 (623 patent) from challenging the combination of Hazelzet + Buchmann

'623 patent (Jan. 3, 2017) [EX1031]	'218 patent (Jan. 2, 2018) [EX1001]	'595 patent (Nov. 12, 2019) [EX1001]
1. A memory module configured to fit into a corresponding slot of a host system to operate with a memory controller of the host system, the memory module comprising: a module controller having an open drain output, the module controller generating a parity error signal and driving the parity error signal to the memory controller of the host system via the open drain output while the memory module operates in a first mode, ..., the module controller generating a notification signal indicating at least one status of one or more training sequences while the memory module is in the second mode and outputting the notification signal to the memory controller of the host system via the open drain output while the memory module is in the second mode; and a printed circuit board having a first set of edge connections for communicating address and control signals from the memory controller of the host system, a second set of edge connections for communicating data signals between the memory module and the memory controller of the host system while the memory module operates in the first mode, and an error edge connection coupled to the open drain output of the module controller, the memory module communicating to the memory controller of the host system via the error edge connection the parity error signal while the memory module operates in the first mode and the notification signal while the memory module is in the second mode.	1. A memory module operable with a memory controller of a host system, comprising: ... a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection; and wherein the memory module is operable in at least a first mode and a second mode, wherein the memory module in the first mode is configured to be trained with one or more training sequences; wherein the memory module in the second mode is configured to perform one or more memory read or write operations not associated with the one or more training sequences ...; ..., and wherein the module controller is further configured to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the second mode; wherein the module controller is further configured to drive a notification signal associated with the one or more training sequences to the error edge connection via the open drain output while the memory module is in the first mode.	1. A memory module operable with a memory controller of a host system, comprising: ... a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection; and ... wherein the memory module in the first mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences; ... wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the first mode; wherein the module controller in the second mode is further configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection to a first state or to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.

Collateral estoppel precludes Netlist on Ground 2

Netlist is precluded by the Final Written Decision in IPR2018-00303 (623 patent) from challenging the combination of Hazelzet + Buchmann

595 claims not patentably distinct from 218 claims

3. Claims 1-7 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-18 of U.S. Patent No. 8489837; claims 1-20 of U.S. Patent No. 9311116; and **claims 1-22 of U.S. Patent No. 9858218**. Although the claims at issue are not identical, they are **not patentably distinct** from each other because the pending claims make obvious the claims of the issued patents and vice versa.

EX1002 ('595 file history) at 83

TERMINAL DISCLAIMER

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Sir:

Applicant, **Netlist, Inc.**, is the assignee of the entire **100%** right, title and interest in and to the above identified application by virtue of assignments recorded on November 15, 2017 at reel/frame 044140 / 0019.

Applicant hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the above identified application which would extend beyond the expiration date of the full statutory term of U.S. Patent No. 8,489,837, (the "prior patent"), which issued on July 16, 2013, U.S. Patent No. 9,311,116, (the "prior patent"), which issued on April 12, 2016, and, **U.S. Patent No. 9,858,218**, (the "prior patent"), which issued on January 2, 2018 as the term of said prior patents are presently shortened by any terminal disclaimer. Applicant hereby agrees that any patent so granted on the above identified application shall be enforceable only for and during such period that it and the prior patent are commonly owned.

EX1002 ('595 file history) at 106

218: Paper 1 (Pet.) at 43; Paper 35 (Repl.) at 14-15

595: Paper 1 (Pet.) at 13-14

HAZELZET, BUCHMANN, AND JEDEC ARE ANALOGOUS ART

Hazelzet, Buchmann, and JEDEC are all analogous art

Netlist Mischaracterizes the Petition

Petition	Netlist’s belated argument in its Sur-Reply
“The prior art relied on here is analogous to the 218 Patent because all are in the same field of invention – memory module design, including error detection and correction, initialization, training and the use of pins/paths for multiple purposes during different operations/modes, ... ” 218: Paper 1 (Pet.) at 34 (citations omitted); see also 595: Paper 1 (Pet.) at 32-33.	“Petitioner overstates the field of endeavor as memory module design, generically. Petition, 34.” 218: Paper 37 (Sur-Reply) at 15; See also ‘595: Paper 37 (Sur-Reply) at 15.

Hazelzet, Buchmann, and JEDEC are all analogous art

Netlist's belated argument in its Sur-Reply...

The Hazelzet/JEDEC and Hazelzet/Buchmann combinations are **not analogous** art to the *claimed invention*—combinations that are directed to completely incompatible architectures that present different solutions to different problems. POR, 5-7, 26-30, 48-53. Fatal to the Petition, Hazelzet is **not analogous** art—it is neither “from the same field of endeavor as the *claimed invention*,” nor “reasonably pertinent to the problem faced by the inventor.” MPEP §2141.01(a) (9th ed. Rev. 10, June 2020); *In re Bigio*, 381 F. 3d 1320, 1325 (Fed. Cir. 2004).

218: Paper 37 (Sur-Reply) at 14; *see also* 595: Paper 35 (Sur-Reply) at 15

...is precluded by the 623 Final Written Decision

We agree with Petitioner that Buchmann and Talbot **are analogous** art to Hazelzet and the '623 patent because they are all directed to the field of error detection and correction in memory modules. Pet. 59, 63. We also agree with Petitioner that it would have been obvious to one of ordinary skill in the art to have combined the known memory system containing a memory controller connected to a memory module that may operate in more than one mode (e.g., Hazelzet, Buchmann, or Talbot), including a known mode in which the memory module performs a training sequence, to notify (send a notification signal to) the memory controller of the status of the training sequence (e.g., Buchmann or Talbot) in order to improve overall reliability.

EX1034 (IPR2018-00303 FWD) at p. 12

Hazelzet, Buchmann, and JEDEC are all analogous art

Netlist misrepresents Dr. Alpert's testimony

Netlist's Sur-Reply	Dr. Alpert's actual testimony
"Indeed, Petitioner's expert conceded that he was "not aware of any reason why one of ordinary skill in the art, reading Hazelzet, would be motivated to add training to Hazelzet." EX2023(Alpert), 288:10-17." 218: Paper 37 (Sur-Reply) at 15; See also '595: Paper 37 (Sur-Reply) at 16.	15THE WITNESS: That's correct. And, again, in 16the context of an embodiment with <u>DDR</u> generation of 17<u>DRAMs</u>. EX2023 (Alpert Dep. Tr.) at 288:10-17 14Q Okay. And, in that modified version of 15Hazelzet that you combine with JEDEC or that you combine 16with Buchmann, what <u>DDR generation</u> are you implementing 17into Hazelzet to do that combination? 18A That would be the <u>DDR3 generation</u> for which 19the write -- for which the training that we've seen in 20the JEDEC proposal is defined, and particularly the 21'Write Leveling' and the 'Read Enable Training.' EX2023 (Alpert Dep. Tr.) at 289:14-21; see also EX2023 (Alpert Dep. Tr.) at 329, errata to 288:19-22 ("I later clarified this testimony at 305:8-306:5, 311:7-312:4") "[A POSITA] would have been motivated to add training to <u>Hazelzet</u> because it was known that training improved the reliability of a memory module's operations ... This is particularly true given the emerging <u>DDR3 applications</u> in the 2009-10 time-frame and their increased speeds. 218: EX1003 (Alpert) at ¶151; 595: EX1003 (Alpert) at ¶172

Hazelzet, Buchmann, and JEDEC are all analogous art

Netlist argues Hazelzet is not related to training...

Hazelzet is outside that field of endeavor—Hazelzet does not relate to training.

218: Paper 37 (Sur-Reply) at 15;
see also 595: Paper 35 (Sur-Reply) at 15-16

...but Hazelzet discloses initialization of DDR3 memory...

[0123] Initialization of the memory subsystem may be completed via one or more methods, based on the available interface busses, the desired initialization speed, available space, cost/complexity objectives, subsystem interconnect structures, the processor) wh etc. In one em complete the SDR (Single Data Rate) Synchronous DRAMs, DDR (Double Data Rate) Synchronous DRAMs or any of the expected follow-on devices such as DDR2, **DDR3**, DDR4 and related technologies such as Graphics RAMs, Video RAMs, LP RAM (Low Power DRAMs) which are often based on the fundamental functions, features and/or interfaces found on related DRAMs.

EX1014 (Hazelzet) [0113], [0123]

...and Netlist admits initialization of DDR3 memory (used in Hazelzet) includes training

Petitioner concedes that **POSITA would have understood** the functions of LR-DIMMs and would have “known” a pre-Provisional JEDEC document titled “MB Initialization Sequence” (EX1039). Pet., 6-7. The pre-Provisional JEDEC document defines the “initialization sequence” for LR-DIMMs, which includes “**MB-DRAM Interface Training**” comprising both “MB-DRAM Write Leveling” and “MB-DRAM Read Training” training sequences. EX1039, 2. MB-DRAM

218: Paper 31 (POR) at 13;
see also 595: Paper 31 (POR) at 16

NETLIST APPLIES THE WRONG LEGAL STANDARD

Netlist applies the wrong legal standard for motivation to combine

Netlist’s argument about motivation...	...is contrary to Federal Circuit precedent
Grounds, and is not prior art (EX1036 post-dates the Provisional). Petitioner is reaching <u>outside of the Grounds for motivation</u>, and asking the Board to reconstitute its grounds to add the LRDIMM Design Specification, which <u>is improper</u>. 218: Paper 31 (POR) at 33; see also 595: Paper 31 (POR) at 34	The motivation need not be found in the references sought to be combined, but may be found in any number of sources, including common knowledge, the prior art as a whole, or the nature of the problem itself. <i>DyStar Textilfarben GmbH v. C.H. Patrick Co.</i>, 464 F.3d 1356, 1361 (Fed. Cir. 2006) 

Netlist applies the wrong legal standard for motivation to combine

Netlist's Sur-Reply cites *Koninklijke* extensively to argue that the motivation to combine cannot come from outside the grounds...

obvious. Petitioner's attempts to go outside those express Grounds for alleged motivation—relying on Kim (to support Grounds 1/2), EX1036, EX1079, and others—has been expressly rejected. *Koninklijke Philips N.V. v. Google LLC*, 948 F.3d 1330, 1335-37 (Fed. Cir. 2020).

218: Paper 37 (Sur-Reply) at 17-18, 24, 26-27;
see also 595: Paper 37 (Sur-Reply) at 17-19, 25, 27-28

...but the cited portion of *Koninklijke* deals with the Board's reliance on a ground not advanced in the petition (not motivation to combine)...

[T]he Board stated, 'we **exercise our discretion** and institute an inter partes review on the **additional ground** that claims 1-11 would have been obvious over SMIL 1.0 and Hua based on the arguments and evidence presented in the Petition.'

Koninklijke Philips N.V. v. Google LLC, 948 F.3d 1330, 1336 (Fed. Cir. 2020)

...and in any event *Koninklijke* expressly permits the Board to rely on corroborated evidence of the knowledge of a POSITA based on a reference not included in the grounds:

Philips argues that ... § 311(b) **prohibits use of general knowledge to supply a missing claim limitation** in an inter partes review. **We disagree.** ... The Board relied on expert evidence, which **was corroborated by Hua**, in concluding that pipelining was not only in the prior art, but also within the general knowledge of a skilled artisan.

Id. at 1337-38.

218: Paper 37 (Sur-Reply) at 17-18, 24, 26-27

595: Paper 37 (Sur-Reply) at 17-19, 25, 27-28

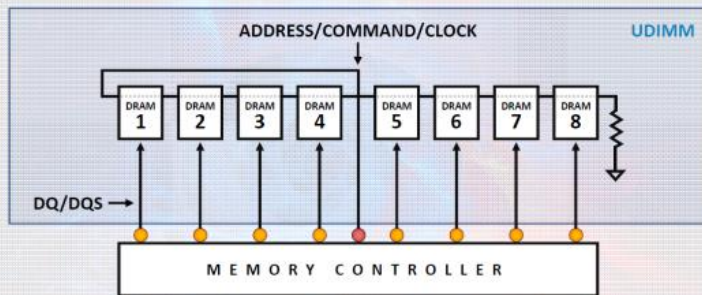


#1: MOTIVATION TO ADD DATA BUFFERS TO HAZELZET

Data buffers were a well-known option for memory modules

DIMMs without data buffers (like Hazelzet/RDIMM)

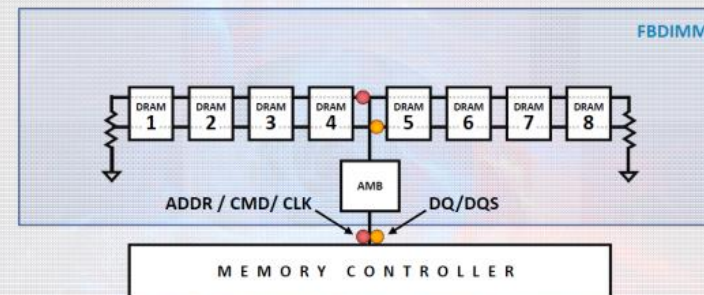
Evolution of DIMMs: JEDEC Un-Buffered DIMM (UDIMM)



EX1079, at 7;
EX1077, at
73:6-74:11

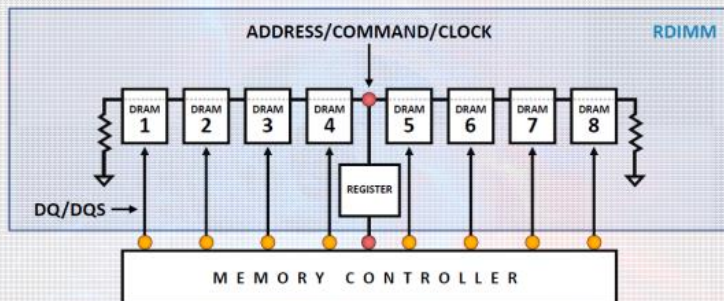
DIMMs with data buffers (like Buchmann/FBDIMM & LRDIMM)

Evolution of DIMMs: Fully-Buffered DIMM (FBDIMM)



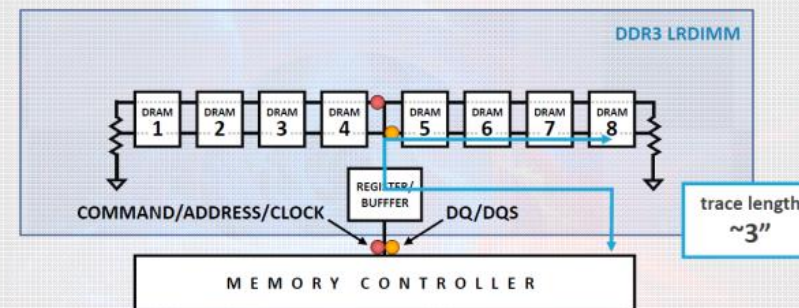
EX1079, at 9;
EX1077, at
61:11-:18, 87:1-
90:5

Evolution of DIMMs: JEDEC Registered DIMM (RDIMM)



EX1079, at 8;
EX1077, at
61:19-:25,
77:11-:20,
81:16-83:20,
84:14-86:21

Evolution of DIMMs: JEDEC DDR3 LRDIMM (Gen1)



EX1079, at 10;
EX1077, at
61:5-:10, 62:1-
:18, 90:9-93:4

'218: Paper 35 (Repl.) at 16-19

'595: Paper 35 (Repl.) at 16-19

LRDIMM (with data buffers) was a known alternative to RDIMM

LRDIMMs Provide Better Capacity

LRDIMMs use memory buffers to consolidate the electrical loads of the ranks on the LRDIMM to a single electrical load, allowing them to have up to eight ranks on a single DIMM module. Using LRDIMMs you can configure systems with the largest possible memory footprints. However, LRDIMMs also use more power and have higher latencies compared to the lower capacity RDIMMs.

Below is a table showing the greater capacity that can be obtained using LRDIMM vs RDIMM.

Number of DIMM Slots	DIMM Type	Maximum Capacity	Configuration
24	RDIMM	768 GB	24 x 32 GB 2R
	LRDIMM	3072 GB	24 x 128 GB 8R
16	RDIMM	512 GB	16 x 32 GB 2R
	LRDIMM	2048 GB	16 x 128 GB 8R

EX2006, p. 4
218: Paper 35 (Repl.) at 21-22
595: Paper 35 (Repl.) at 21-22

LRDIMM and FBDIMM (with data buffers) were known alternatives to RDIMM

MAINSTREAM 2 SOCKET SERVER								
	2006	2007	2009	2010	2011	2012	2013	2014
DRAM	DDR2	DDR2	DDR3	DDR3	DDR3	DDR3	DDR4	DDR4
DRAM VOLTAGE SUPPORTED	1.8v	1.8v, 1.5v	1.5v	1.5v, 1.35v	1.5v, 1.35v	1.5v, 1.35v, 1.25v	1.20v	1.20v, 1.10v
RANKS PER DIMM SUPPORTED	1, 2	1, 2, 4	1, 2, 4	1, 2, 4	1, 2, 4, 8	1, 2, 4, 8	1, 2, 4, 8	1, 2, 4, 8
DIMM TYPES SUPPORTED IN STANDARD DIMM CONNECTOR	FBDIMM	FBDIMM	RDIMM, UDIMM, LR-DIMM	RDIMM, UDIMM, LR-DIMM	RDIMM, UDIMM, LR-DIMM	RDIMM, UDIMM, LR-DIMM	RDIMM, UDIMM, LR-DIMM	RDIMM, UDIMM, LR-DIMM
FREQUENCY SUPPORTED	533, 667	533, 667, 800	800, 1066, 1333	800, 1066, 1333, 1600	800, 1066, 1333, 1600, 1866	800, 1066, 1333, 1600, 1866, 2133	1600, 1866, 2133, 2400	1600, 1866, 2133, 2400, 2667

Fig. 2

EX2007, Fig. 2; EX1077, 95:9-96:25; EX2023, 294:5-296:4



11 Q. In your opinion would a person of ordinary
12 skill in the art have known about the tradeoffs
13 between UDIMM, RDIMM, FBDIMM and LR-DIMM?
14 MR. ROE: Objection. Vague.
15 THE WITNESS: Generally speaking I believe
16 they would. They -- they each have a different
17 architecture, and those architectures lend themselves
18 to certain performance metrics, and they definitely
19 would -- one of ordinary skill in the art would have
20 been at least aware of those differences, yes.

EX1077 (Murphy Dep. Tr.) at 98:11-16

12 Q. What were the known benefits at the time of
13 having a Memory Buffer on an FBDIMM or an LR-DIMM for
14 buffering the data lines?
18 THE WITNESS: Well, I think the -- in the --
19 in the general sense, the known -- the known benefits
20 would have been the reduction of load to the data
21 lines themselves. That's what buffers generally
22 provide.



EX1077 (Murphy Dep. Tr.)
at 102:12-22

6 Q. In what situations would an LR-DIMM memory
7 module be more advantageous than a memory module
8 without a data buffer?

12 THE WITNESS: So I believe that the -- the
13 biggest -- the biggest difference here would be that
14 people understood that RDIMMs had shorter latencies.
15 At the -- at the time of comparison they were -- you
16 were able to run them at higher speeds, but that also
17 comes about at a design choice of not having as much
18 capacity as the LR-DIMMs. So I would say generally,
19 if you needed something high speed, you would -- and
20 somewhat lower cost, you would be interested more in
21 RDIMMs than you would in LR-DIMMs. And if you need
22 something that needed large capacity, you would pick
23 the LR-DIMMs or anything that had a data buffer on
24 it.



EX1077 (Murphy Dep. Tr.)
at 104:6-24

The Petition and Reply explained the motivation for data buffers

Netlist's Sur-Reply ignores...	... the Petition ...
"Petitioner did not even attempt to rebut that neither JEDEC, nor Buchmann, provides a motivation to add data buffers to Hazelzet. POR 39-41. Instead, Petitioner doubled down on alleged motivation from EX1036. Reply, 20." 218: Paper 37 (Sur-Reply) at 18-19	"Buchmann also discloses a 'training phase that allows more flexibility and improved control data exchange during start-up,' id., 3:64-67, to establish 'reliable communication' on the bus, id. at 14:28-35, 14:5-8. A Skilled Artisan would have been motivated by these disclosures to look to systems such as JEDEC's and Buchman's to improve reliability. EX1003, ¶154. ... As discussed above with reference to JEDEC, a Skilled Artisan would have been motivated to add the functionality of buffering the data signals and corresponding training to Hazelzet's Registered DIMM, because it was a known, reliable technique which improved performance and higher capacity, as discussed above. EX1003, ¶¶154-156, 158." 218: Paper 1 (Pet.) at 38 "The LRDIMM Design Specification explained in detail the advantages, including increased performance and capacity, of adding the LRDIMM's data buffering functionality to an RDIMM, like Hazelzet's module, which buffers only address and command signals. EX1036, 5. Thus, Skilled Artisan would have understood and been motivated at the time to upgrade Hazelzet's RDIMM with an LRDIMM functionality to buffer the data lines as well. EX1003, ¶¶155-156... These advantages of buffering the data lines were well known to a Skilled Artisan at the time. See, e.g., EX1003, ¶¶155-156; EX1028, [0031]." 218: Paper 1 (Pet.) at 37
... and the Reply	
"Indeed, Netlist's expert has admitted that these advantages of reducing the load by buffering the data signals (as in LR-DIMM) were well known to a POSITA. EX1077, 86:18-:21 ("Q. So if I understand correctly, as a benefit of reducing electrical load, that it can permit the signaling on the memory module to be faster? ... THE WITNESS: Yes."), 104:6-24 ("Q. In what situations would an LR-DIMM memory module be more advantageous than a memory module without a data buffer? ... THE WITNESS:[I]f you need something that needed large capacity, you would pick the LR-DIMMs or anything that had a data buffer on it."). 218: Paper 35 (Repl.) at 21	

218: Paper 1 (Pet.) at 37-38; Paper 35 (Repl.) at 21-22

595: Paper 1 (Pet.) at 35-36; Paper 35 (Repl.) at 21-22

Hazelzet discloses 4 ranks of memory, providing a need for data buffers

Netlist argues Hazelzet's disclosure of "buffer" refers to address and control signals only...

"Petitioner's citation is consistent with Hazelzet's ubiquitous reference to its ECC/Parity Register 21 as a memory buffer; but Hazelzet's memory buffer only buffers address and control signals—not data signals."

218: Paper 37 (Sur-Reply) at 19-20

595: Paper 37 (Sur-Reply) at 19-20

...but Netlist ignores Hazelzet's disclosure of a "buffer" for a four-rank module, whose load is a motivation to add data buffering...

Netlist argues that Hazelzet eliminates the need for two types of buffer devices, POR 35, 36-37, but Hazelzet solves that problem with a single "buffer which is operable with up to 4 ranks of memory devices." EX1014, [0014]. Instead of teaching away, such a four-rank module would have motivated a POSITA to add data buffering to lower the load. Pet. 36-37; EX1003, ¶¶154-56, 158; EX1077, 84:14- 86:21 ("Generally, when the load is lower, ... the signal is able to get to the load in a quicker amount of time.").

218: Paper 35 (Repl.) at 22
595: Paper 35 (Repl.) at 22

...and Hazelzet discloses a "memory buffer," which at the time included data buffering:

[0118] As used herein, the term memory subsystem refers to, but is not limited to: one or more memory devices; one or more memory devices and associated interface and/or timing/control circuitry; and/or one or more memory devices in conjunction with a memory buffer, and/or switch. The term memory subsystem may also refer to one or more memory devices, in addition to any associated interface and/or timing/control circuitry and/or a memory buffer assembled into a substrate, a card, a module or related

EX1014, [0118]

218: Paper 1 (Pet.) at 36-37; Paper 35 (Repl.) at 22

595: Paper 1 (Pet.) at 34-35; Paper 35 (Repl.) at 22

Netlist's "teaching away" argument was correctly rejected

Netlist's "teaching away" argument...	...was already rejected by the Institution Decision:
Thus, POSITA "would be led in a direction divergent from" adding more costly and complex memory components that buffer data signals, which itself would be opposite of Hazelzet's intended purpose to use "reduced-function memory assemblies" for the "low or midrange server markets." <i>In re Gurley</i>, 27 F.2d 551, 218: Paper 31 (POR) at 37 See also 595: Paper 31 (POR) at 37	Patent Owner's "teaching away" argument is unpersuasive. Patent Owner has not shown that Hazelzet "criticize[s], discredit[s], or otherwise discourage[s]" memory modules with increased performance and capacity. <i>See Galderma Laboratories, L.P. v. Tolmar, Inc.</i>, 737 F.3d 731, 738 (Fed. Cir. 2013) (a prior art reference does not teach away if it does not criticize, discredit, or otherwise discourage investigation into the invention claimed). 218: Paper 14 (ID) at 46 See also 595: Paper 14 (ID) at 43

#2: MOTIVATION TO ADD TRAINING TO HAZELZET

Both experts agreed that DDR3 created a need for training at initialization

Given Hazelzet's emphasis on the need for "improved overall system reliability," one skilled in the art would have been motivated to add training to Hazelzet because it was known that training improved the reliability of a memory module's operations. ... This is particularly true given the emerging DDR3 applications in the 2009-10 time-frame and their increased speeds.



218: EX1003 (Alpert Dec.) at ¶151
595: EX1003 (Alpert Dec.) at ¶172

Q. As the speed of the DRAM memory increases, for example, from the DDR2 memory devices to the DDR3 memory devices, would initialization become more important?
THE WITNESS: ... So from SDRAM to DDR to DDR2 to DDR3, the features and functions inside those devices generally changed from generation to generation. And on the basis of just the fact that there were more features; therefore, more things that potentially had to be initialized, I would say in general the answer to your question is yes because, now instead of potentially having five things to set up to get the part to work, maybe I had eight things to set up. And so the initialization sequences became more important at least in that fashion.



EX1077 (Murphy Dep. Tr.) at 109:12-110:7.

I think in general one of ordinary skill in the art would understand that training can be done during the initialization. It can be one of the initialization sequences that can happen inside of the memory module.



EX1077 (Murphy Dep. Tr.) at 146:4-14.

218: Paper 1 (Pet.) at 35-40; Paper 35 (Repl.) at 23-26
595: Paper 1 (Pet.) at 34-37; Paper 35 (Repl.) at 23-25

Netlist's expert agreed that LRDIMM created a need for training at initialization

Q. In your opinion would a person of ordinary skill in the art know that training the Memory Buffer on an LR-DIMM would be needed to achieve optimal performance?

THE WITNESS: Well, as I've already answered if the -- if one of ordinary skill in the art knew that on an LR-DIMM data buffering was going to be part of the solution, then from other information that was available before the LR-DIMM, they would know that that training would need to be performed to make -- to make that data buffering be viable and be optimal, yes.



EX1077 (Murphy Dep. Tr.) at 146:16-147:3

Q. And to be clear, I mean, an LR-DIMM has data buffering Memory Buffer; correct?

A. That's basically identified in the provisional, yes.

Q. And would that have been known before the provisional?

THE WITNESS: Yes. Before the provisional, data buffering was known in, for example, FBDIMMs in 2004.



EX1077 (Murphy Dep. Tr.) at 147:5-14

I think one of ordinary skill in the art at the time of the provisional would have known that any memory subsystem that uses training is required to have that training set the timing optimally so that the part can achieve its highest performance and have its best reliability. And I don't think it matters whether it was LR-DIMMs or a different -- a different type of memory architecture.



EX1077 (Murphy Dep. Tr.) at 155:7-22

218: Paper 1 (Pet.) at 35-40; Paper 35 (Repl.) at 23-26

595: Paper 1 (Pet.) at 34-37; Paper 35 (Repl.) at 23-25

Netlist incorrectly assumes the motivation must come from Hazelzet itself

Netlist incorrectly argues the motivation for training must be found within <u>Hazelzet</u> itself...	
And Petitioner does not rebut <i>both parties'</i> expert opinions that there is <i>no</i> “reason why one of ordinary skill in the art, <u>reading Hazelzet</u>, would be motivated to add training to <u>Hazelzet</u>.” EX2023(Alpert), 288:10-17; POR, 44; EX2027(Murphy), 218: Paper 37 (Sur-Reply) at 20; 595: Paper 37 (Sur-Reply) at 21	
...contrary to Federal Circuit precedent...	...and based on a misrepresentation of Dr. Alpert’s testimony...
The motivation need not be found in the references sought to be combined, but may be found in any number of sources, including common knowledge, the prior art as a whole, or the nature of the problem itself. <i>DyStar Textilfarben GmbH v. C.H. Patrick Co.</i>, 464 F.3d 1356, 1361 (Fed. Cir. 2006) 	10Q But sitting here today, you're not aware of 11any reason why one of ordinary skill in the art, <u>reading</u> 12<u>Hazelzet</u>, would be motivated to add training to 13Hazelzet, correct? 14MR. CHANDLER: Objection. Form. 15THE WITNESS: That's correct. <u>And, again, in</u> 16<u>the context of an embodiment with <u>DDR</u> generation of</u> 17<u>DRAMs .</u> EX2023 (Alpert Dep. Tr.) at 288:10-17

Dr. Alpert explained Hazelzet's disclosure of DDR3 provided a motivation to add training to Hazelzet

Dr. Alpert's actual testimony

"[A POSITA] would have been motivated to add training to Hazelzet because it was known that training improved the reliability of a memory module's operations ... This is particularly true given the emerging DDR3 applications in the 2009-10 time-frame and their increased speeds.

218: EX1003 (Alpert) at ¶151;
595: EX1003 (Alpert) at ¶172

14 Q Okay. And, in that modified version of
15 Hazelzet that you combine with JEDEC or that you combine
16 with Buchmann, what DDR generation are you implementing
17 into Hazelzet to do that combination?
18 A That would be the DDR3 generation for which
19 the write -- for which the training that we've seen in
20 the JEDEC proposal is defined, and particularly the
21 'Write Leveling' and the 'Read Enable Training.'

EX2023 (Alpert Dep. Tr.) at 289:14-21;
see also EX2023 (Alpert Dep. Tr.) at 329, errata to 288:19-22
("I later clarified this testimony at 305:8-306:5, 311:7-312:4")

Netlist's "bodily incorporation" argument is legally wrong

Netlist's "bodily incorporation" argument...	...was rejected by the prior Final Written Decision
Importantly, Petitioner did not rebut Netlist's evidence that adding <u>JEDEC</u> or <u>Buchmann</u> training to <u>Hazelzet</u> would require bi-directional data exchange, a feature <u>Hazelzet</u> lacks. POR, 42; EX2023(Alpert), 244:17-245:16. Or rebut Netlist's evidence that adding training would be complex and costly. POR, 42-43. 218: Paper 37 (Sur-Reply) at 21; 595: Paper 37 (Sur-Reply) at 22	To the extent that Patent Owner argues that it would not have been obvious to one of ordinary skill in the art to have bodily incorporated the teachings of either of Buchmann or Talbot (i.e., training mode) into those of Hazelzet (i.e., a mode during which training is not performed), we note that "[t]he test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference. . . . Rather, the test is what the combined teachings of those references would have suggested to those of ordinary skill in the art." <i>In re Keller</i>, 642 F.2d 413, 425 (CCPA 1981); <i>see also In re Sneed</i>, 710 F.2d 1544, 1550 (Fed. Cir. 1983) ("[I]t is not necessary that the inventions of the references be physically combinable to render obvious the invention under review."); <i>In re Nievelt</i>, 482 F.2d 965, 968 (CCPA 1973) ("Combining the teachings of references does not involve an ability to combine their specific structures."). EX1034 (IPR2018-00303 FWD) at 15

#3: MOTIVATION TO USE HAZELZET'S OPEN-DRAIN UE LINE AS NOTIFICATION SIGNAL

Open-drain was a well-known technique to provide a “wired OR”

21 Q. In your opinion would a person of ordinary
22 skill in the art have known that an open drain output
23 in combination with a pull-up or pull-down resistor
24 would result in a wired-or function?

2 THE WITNESS: Yes. One of ordinary skill in
3 the art would have known this. It's probably 40
4 years old.

EX1077 (Murphy Dep. Tr.) at 178:21-179:4



Hazelzet 's open-drain UE line was obvious choice for notification signal indicating status of training on modules

a Skilled Artisan would have been motivated to arrange the modified Hazelzet to communicate a signal indicating completion of training only when all memory modules have completed that training, in order to ensure that the entire memory system had been trained before proceeding to normal operation. This would permit training to be completed in an orderly and systematic manner, thereby limiting the complexity of the control circuitry needed to implement the training. EX1043, 7:30-51. Use of an open drain signal in this manner was a known, efficient way to communicate information about multiple circuits because it effectively OR'd the inputs into a single output. EX1017 (Kim) at FIG. 4; 5:656:12



218: EX1003 (Alpert Dec.) at ¶168

595: EX1003 (Alpert Dec.) at ¶189

[A] person of ordinary skill in the art would have been motivated to use the same output to notify error signals and training status because such multiple use of a pin was known, and would have been considered an efficient use of the limited number of output pins on integrated circuits. For instance, Kim, EX1017, ... would have motivated a Skilled Artisan to use Hazelzet's "/Error (UE)" 121 open-drain output (corresponding to Kim's "error feedback pin") to notify the memory controller that the training was in progress or done.



218: EX1003 (Alpert Dec.) at ¶166

595: EX1003 (Alpert Dec.) at ¶187

As another example, Talbot [EX1022] ... discloses using a CRC (i.e. ECC) signal path to return signals relating to training during the training mode when the CRC functionality is off. ... Such disclosures would have motivated a Skilled Artisan to use Hazelzet's "/Error (UE)" 121 open-drain output (corresponding to Talbot's "CRC 93 signal path") to notify the memory controller that the training was in progress or done.



218: EX1003 (Alpert Dec.) at ¶167

595: EX1003 (Alpert Dec.) at ¶188

218: Paper 1 (Pet.) at 32-34, 40-42; Paper 35 (Repl.) at 26-30

595: Paper 1 (Pet.) at 30-32, 38-40; Paper 35 (Repl.) at 26-30

JEDEC (EX1015) discloses using the same error-out line to signal training completion as the 218 and 595 Patents

6.7 MB-DRAM Training

After all the DRAMs are fully operational, the host triggers the DRAM interface training by setting the control bit DA4 in F0RC12. Once enabled, the MB assumes autonomous control of the Command/Address, Control and Data/Strobe signals to the DRAMs, without any further assistance from the host.

The MB performs 'Write Leveling' to the DRAMs to ensure successful writes, and 'Read Enable Training' to ensure it can capture read data from the DRAMs correctly, as part of the DRAM interface training.

No DRAM commands or control word writes (either over the Command/Address and Control buses or via SMBus) can be issued to the MB until the MB-DRAM Interface training is complete and the DODTn inputs must be kept low. The MB responds to SMBus CSR read accesses whether or not DRAM interface training is active. To determine DRAM interface training completion the host may either wait for a time 'tCAL * number of physical ranks' (which is the maximum amount of time that the MB-DRAM Interface training is allowed to take) or it may periodically poll the content of the MB CSR 'Training Completion' (see 'Configuration Registers' chapter) over the SMBus.

In addition, training completion can be signaled by the assertion of ERROUT#. This is not the power-up default but can be enabled by setting the DBA1 bit in the F3RC14 Training Completion Control Word.

EX1015 at 8

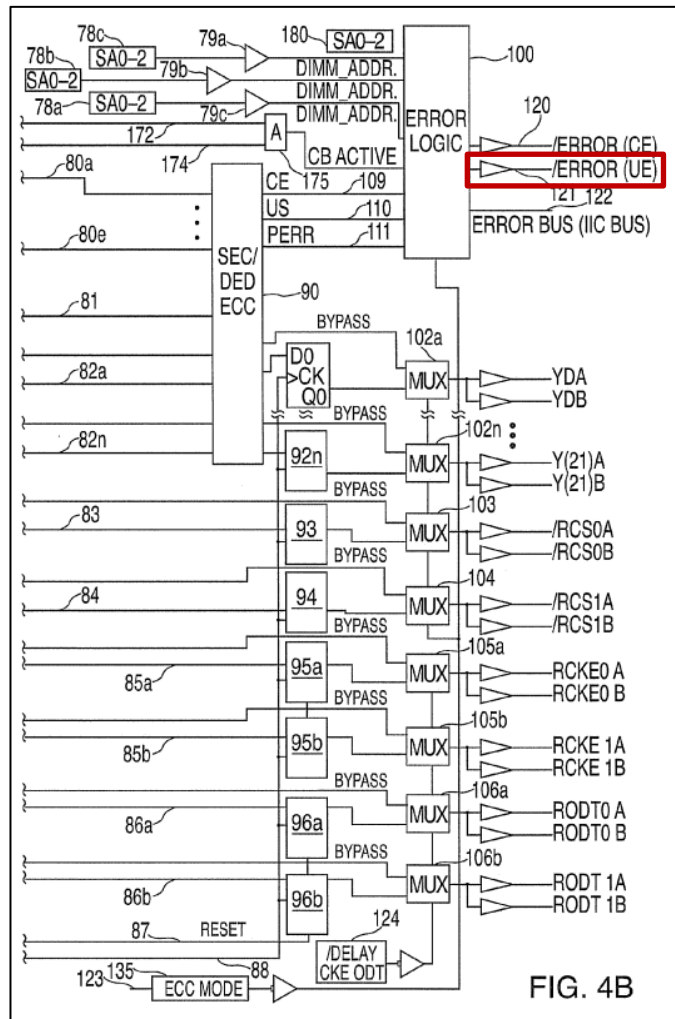
DDR3 SDRAM LRDIMM Design Specification Pinout and Description

Load Reduced DIMM Input/Output Functional Description

ErrOut_n	OUT (open drain)	Parity error detected on the Address and Command bus. A resistor may be connected from ErrOut_n bus line to V _{DD} on the system planar to act as a pull up.
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EX1036 at 9

Hazelzet does not teach away from using its open-drain UE line during initialization



EX1014 (Hazelzet) at Fig. 4B

[0123] Initialization of the memory subsystem may be completed via one or more methods, based on the available interface busses, the desired initialization speed, available space, cost/complexity objectives, subsystem interconnect structures, the use of alternate processors (such as a service processor) which may be used for this and other purposes, etc. In one embodiment, the high speed bus may be used to complete the initialization of the memory subsystem(s).

EX1014 (Hazelzet) at [0123]



Hazelzet's use of the same output in two different modes would have suggested to, and motivated a person of ordinary skill in the art to use that same output in the added training mode, particularly when the training mode was implemented separate from, and before, the parity and ECC modes of Hazelzet, as 91 here. In such a system, those modes, which include normal memory operations, would therefore not be using the open drain outputs while the training mode was running during initialization.

218: EX1003 (Alpert Dec.) at ¶164
595: EX1003 (Alpert Dec.) at ¶185

Netlist applies the wrong legal standard for motivation to combine

Netlist's arguments about motivation to combine...

Netlist does not ignore that “the Petition relies on Hazelzet in combination with JEDEC or Buchmann.” (Reply, 27). Those are the *only* Grounds, *Koninklijke Philips*, 948 F.3d at 1335-37, and none of Hazelzet/JEDEC/Buchmann—individually or in combination—teach, suggest or motivate POSITA to use Hazelzet’s open-drain to communicate training signals as required by all claims (elements 1.i, 9.h, and 15.i). POR, 59-70.

218: Paper 37 (Sur-Reply) at 24; 595: Paper 37 (Sur-Reply) at 25

As for Ground 3 (Hazelzet/JEDEC), Petitioner asserts baldly that “POSITA would have known the benefits” to use Hazelzet’s open-drain (Reply 30), but JEDEC describes no benefit. POR, 70. Indeed, Petitioner appears to concede that its “motivation” comes from outside the express Grounds. Reply, 30 (arguing that “the motivation” can come from outside the Ground). Petitioner is limited to the express Grounds in the Petition. *Koninklijke Philips*, 948 F.3d at 1335-37.

218: Paper 37 (Sur-Reply) at 27; 595: Paper 37 (Sur-Reply) at 28

... are contrary to Federal Circuit precedent

The motivation need **not** be found in the references sought to be combined, but may be found in any number of sources, including common knowledge, the prior art as a whole, or the nature of the problem itself.

DyStar Textilfarben GmbH v. C.H. Patrick Co.,
464 F.3d 1356, 1361 (Fed. Cir. 2006)



In sum, we conclude that the Board did not violate § 311(b) or the inter partes review statute in determining that the claims would have been obvious over SMIL 1.0 **in light of the general knowledge of a skilled artisan**.

Koninklijke Philips N.V. v. Google LLC,
948 F.3d 1330, 1338 (Fed. Cir. 2020)



218: Paper 1 (Pet.) at 32-34, 40-42; Paper 35 (Repl.) at 26-30

595: Paper 1 (Pet.) at 30-32, 38-40; Paper 35 (Repl.) at 26-30

MOTIONS TO EXCLUDE 05

PETITIONER'S MOTION TO EXCLUDE

EX2017 (WEBSITE PRINTOUT) AND
¶¶20-21 OF EXHIBIT 2026 (DR. YANG)

Petitioner's Motion to Exclude

EX2017 (a website printout) is inadmissible hearsay

Netlist relies on EX2017 for the truth of the matter asserted

And with respect to Petitioner's alleged "increased performance" motivation, RDIMMs (like Hazelzet)—not LRDIMMs—are "the hands down winner." EX2017, 3 ("[m]any of our [] customers are looking for *high speed and low latency*. In that realm, *RDIMMs are the hands down winner*"). Balancing cost and *increased performance*, RDIMMs were endorsed as the "*right choice for fast memory performance*." *Id.* Thus, "increased performance" (Pet., 37) would not have motivated POSITA to redesign Hazelzet's RDIMM to LR-DIMMS because RDIMMs are "the right choice for fast memory performance." *Id.*

Paper 31 (POR) at 34

218: Paper 46 (Pet. MTE) at 1-3

595: Paper 46 (Pet. MTE) at 1-3

111

Petitioner's Motion to Exclude

EX2017 (a website printout allegedly dated **2015**) is irrelevant, particularly if Patent Owner's argument is credited

Patent Owner Response

And with respect to Petitioner's alleged "increased performance" motivation, RDIMMs (like Hazelzet)—not LRDIMMs—are **"the hands down winner."**

218: Paper 31 (POR) at 34

See also 595: Paper 31 (POR) at 35

vs.

Patent Owner Opposition to Motion to Exclude

[I]t is **irrelevant** whether RDIMMs are actually **"the hands down winner"** as compared to LRDIMMs.

218: Paper 47 (PO Opp.) at 1-2

See also 595: Paper 47 (PO Opp.) at 1-2



Petitioner
Agrees!

Petitioner's Motion to Exclude

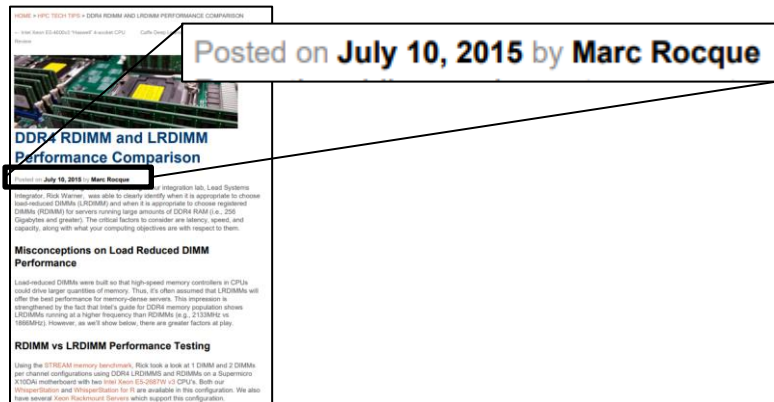
EX2017 (a website printout allegedly dated **2015**) is irrelevant and constitutes inadmissible hearsay

Netlist's opposition to Petitioner's motion to exclude:

Exhibit 2017 reflects **what a POSITA would have known *in 2015***, years after the instruction of LRDIMMs

Paper 47 (PO Opp. to Pet. MTE) at 2 (emphasis added)

EX2017 bears a date of **2015**:



EX1017 at 1

“In assessing obviousness, the knowledge [of] one skilled in the art must be evaluated ***at the time of the invention ...***”

Comcast Cable Commc'ns Corp. v. Finisar Corp., 571 F. Supp. 2d 1137, 1145 (N.D. Cal. 2008), *aff'd*, 319 F.App'x 916 (Fed. Cir. Apr. 10, 2009)



Petitioner's Motion to Exclude

EX2017 (a website printout allegedly dated 2015) is irrelevant

Where is the
citation to
evidence?

Netlist's opposition, *cont'd*:

If the question of whether LRDIMMs were preferred over RDIMMs in all use cases was not a settled consensus and was still being debated in 2015, **it certainly also would not have been a settled consensus and would still have been debated years earlier in June 2009.**

Paper 47 (PO Opp. to Pet. MTE) at 2-3



“Attorney argument is not evidence and cannot rebut other admitted evidence”

Elbit Sys. of Am., LLC v. Thales Visionix, 881 F. 3d 1354, 1359 (Fed. Cir. 2018) (emphasis added)

Petitioner's Motion to Exclude

Paragraphs 20-21 of EX2026 (Declaration of Dr. Yang) should be excluded under FRE 602 and FRE 801-802



20. Both in the 2009-2010 timeframe and throughout my time at JEDEC, it was understood and the practice of JEDEC members that committee ballots were treated as confidential within the committee.¹ Of course, I and other JEDEC member representatives would discuss technology proposals or ballots internally and among committee members as necessary to determine how to vote or comment on proposals.² But it was understood that pending committee ballots could not be distributed *outside* of the relevant group of JEDEC members to other, non-JEDEC entities. This is further reflected by the fact that, as noted above, access to ballots

EX2026 (Yang) at ¶20

- **Hearsay**
- **Not personal knowledge**
(he was not a member of JC-40)



21. In my entire experience, including my many years at Intel where I worked with Mr. Halbert, I have never heard of any JEDEC committee ballot being distributed or sent to a non-JEDEC member (that is, to a third party) prior to any standard being formally adopted. This would have been improper, and I see in Mr. Halpert's deposition that he agrees with me on this point. 7/22/22 Halbert Depo. Tr. [Exhibit 2022] at 23:14–17. When Mr. Halbert states in his declaration (paragraph 11) that ballots were discussed “among all third-parties,” I do not understand him to be saying that the ballots themselves were circulated to third-parties (versus technical issues related to such being discussed). And Mr. Halbert clarified in his deposition that his understanding matches mine that ballots were *not* distributed to third parties. Exhibit 2022 at 23:14–17. Regardless, as I note above, I am not aware of any instance when the content of JEDEC ballots were ever shared with third parties, much less the ballots themselves being distributed to third parties.

EX2026 (Yang) at ¶21

218: Paper 46 (Pet. MTE) at 6-15; Paper 50 (Repl. ISO MTE) at 3-5

595: Paper 46 (Pet. MTE) at 6-15; Paper 50 (Repl. ISO MTE) at 3-5

Samsung Electronics Co., Ltd., Ex. 1082, p. 115

115

PATENT OWNER'S MOTION TO EXCLUDE

EXHIBITS 1015, 1024-25, 1036-37, 1039,
1048-49, 1051, 1056, 1071-76, AND 1080-81

Netlist's Motion to Exclude

Authentication is a “low bar,” and Netlist Has Failed to Establish that Any Exhibit Is Inadmissible

“We agree with Patent Owner that Petitioner bears the burden to authenticate Exhibit 1005. ... But, **authentication is a low bar**, requiring only a rational basis that Exhibit 1005 is what it is asserted to be. ... Moreover, **Patent Owner bears the burden of establishing that Exhibit 1005 is not admissible**. See 37 C.F.R. § 42.20(c) (indicating the moving party has the burden of proof to establish that it is entitled to the requested relief.).

... Petitioner has provided a rational basis that Exhibit 1005 is what Petitioner purports it to be... On the other hand, **Patent Owner has not carried its burden of establishing Exhibit 1005 is inadmissible. Notably, Patent Owner never challenged that Exhibit 1005 is what it purports to be or that the exhibit was somehow altered.**”

Advanced Micro Devices, Inc. v. Aquila Innovations, Inc., IPR2019-01526, Paper 37, at 97-101 (PTAB Mar. 10, 2021) (citations omitted), *aff'd*, 2022 WL 1089229 (Fed. Cir. 12, 2022).



As Petitioner has failed to authenticate Exhibits 1015, 1024-25, 1036-37, 1039, 1048-49, 1051, 1056, and 1080-81, the Board should exclude each of these exhibits in their entirety under Federal Rule of Evidence 901. *See, e.g., TRW Automotive U.S. LLC v. Magna Elecs. Inc.*, IPR2014-01347, Paper 25 at 12 (P.T.A.B. Jan. 6, 2016) (excluding asserted prior art for lack of authentication).

Paper 45 (PO Mtn. to Exclude Evidence) at 12

218: Paper 48 (Pet. Opp. to PO Mtn. to Exclude) at 3-13

595: Paper 48 (Pet. Opp. to PO Mtn. to Exclude) at 3-13

Netlist's Motion to Exclude

Samsung Has Established the Authenticity of the Challenged Exhibits in Multiple, Exemplary Ways

1. "Testimony that an item is what it is claimed to be" (FRE 901(b)(1))



- *Liquidia Techs., Inc. v. United Therapeutics Corp.*, IPR2021-00406, Paper 78, at 43–45 (PTAB July 19, 2022) (finding authenticity given (1) declarants' description of an exhibit and (2) various exhibit sections consistent with that description)
- *Advanced Micro Devices*, IPR2019-01526, Paper 37, at 99–100 (finding authenticity based on expert testimony relying on challenged exhibit)
- *eBay Inc. v. Global Equity Mgmt. (SA) Pty. Ltd.*, IPR2016-01829, Paper 60, at 8 (PTAB Apr. 18, 2018) ("Petitioner has satisfied the requirement of authenticating the APM Specification through expert testimony identifying and relying on it.").

2. "The appearance, contents, substance, internal patterns, or other distinctive characteristics of the item, taken together with all the circumstances" (FRE 901(b)(4)); *see also* FRE 902(7)



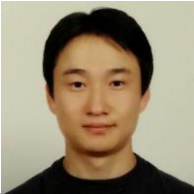
- *New World Med., Inc. v. Microsurgical Tech., Inc.*, IPR2020-01573, Paper 63, at 8–9 (PTAB Feb. 16, 2022) (finding authenticity because "Exhibit 1020 bears indicia that it is such a publication [by the American Glaucoma Society] in the form of a header indicating the society's name and annual meeting number" and "the indicia of authenticity on the face of Exhibit 1020 can be substantially confirmed by the most basic [online] investigation");
- *Advanced Micro Devices*, IPR2019-01526, Paper 37, at 100 ("Exhibit 1005 has multiple references to Microsoft Corporation and a copyright date on its cover page, which are tags or labels affixed in the course of business indicating origin and ownership. . . . Exhibit 1005 additionally has the appearance and distinctive characteristics of Microsoft's Hardware White Paper, Draft ACPI Driver Interface Design Notes and Reference, given the title on its cover page.");
- *Arris Grp., Inc. v. C-Cation Techs., LLC*, IPR2015-00635, Paper 55, at 36–37 (PTAB July 28, 2016) (finding authenticity based on "logo...on their covers" and "distinctive characteristics such as library catalog numbers, copyright pages, and ISBNs").

218: Paper 48 (Pet. Opp. to PO Mtn. to Exclude) at 3-13

595: Paper 48 (Pet. Opp. to PO Mtn. to Exclude) at 3-13

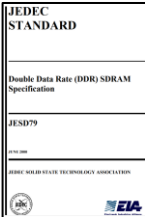
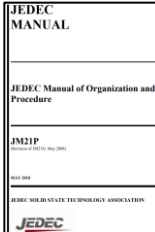
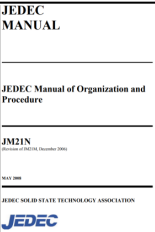
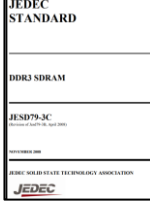
Netlist's Motion to Exclude

The Challenged JEDEC Materials (EX1015, 1024-25, 1036-37, 1048-40, 1051, 1056) are Authenticated by Julie Carlson, SJ Park, and Comparison to Other Uncontested JEDEC documents

Witness		Exhibits
	Julie Carlson Custodian of JEDEC Documents	EX1050 (declaration, attaching copies of EX1015 (Ex.A), EX1051 (Ex.B), EX1037 (Ex.C), EX1036 (Ex.D), EX1039 (Ex.G), EX1049 (Ex.I), EX1048 (Ex.J)); EX2024 (deposition)
	SJ Park Samsung engineer who participated in the creation and approval of the JEDEC Proposal (EX1015)	EX1055 (declaration, attaching copies of EX1051 (Ex.A), EX1015 (Ex.B), EX1037 (Ex.C), EX1036 (Ex.E); EX2025 (deposition)

Netlist's Motion to Exclude

The JEDEC materials (EX1015, 1024-25, 1036-37, 1048-49, 1051, and 1056) each bear distinctive characteristics indicating their authenticity

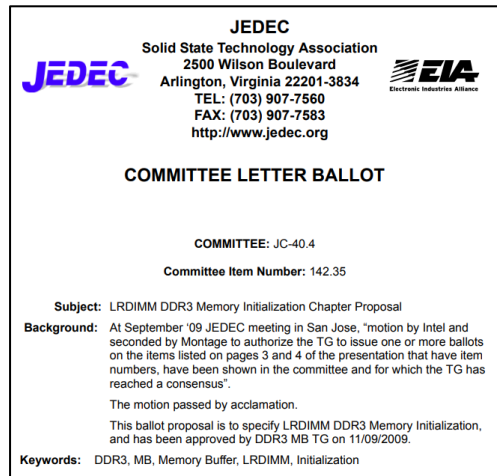
Exhibit		Description	Exhibit		Description
EX1015	 JEDEC Solid State Technology Association 2500 Wilson Boulevard Arlington, Virginia 22201-3834 TEL: (703) 907-7560 FAX: (703) 907-7583 http://www.jedec.org 	JEDEC proposal #142.35 approved December 2009	EX1039	 Where Semiconductor Leaders Set Standards for the World! 	Inphi presentation #142.35 to JEDEC on June 4, 2009
EX1024-25	 	JEDEC Standards JESD79 (June 2000) and JESD206 (Jan. 2007)	EX1048-49	 	JEDEC manuals of procedures (2008 to 2010)
EX1036	 JEDEC Solid State Technology Association 2500 Wilson Boulevard Arlington, Virginia 22201-3834 TEL: (703) 907-7560 FAX: (703) 907-7583 http://www.jedec.org 	JEDEC Proposal #2192.44 (Dec. 2009)	EX1051	 Committee Letter Ballot JC-40.4-09-320 Item 142.35 Distributed: 11 Nov 2009 Expiring: 03 Dec 2009 	JEDEC ballot for #142.35 distributed November 11, 2009
EX1037	 JEDEC Compilation of Tallies for JC-40 CMOS Digital Logic and point committees 	Tally of votes for JEDEC proposal #142.35 as of December 4, 2009	EX1056		JEDEC standard JESD79-3C (April 2008)

218: Paper 48 (Pet. Opp. to PO Mtn. to Exclude) at 3-13

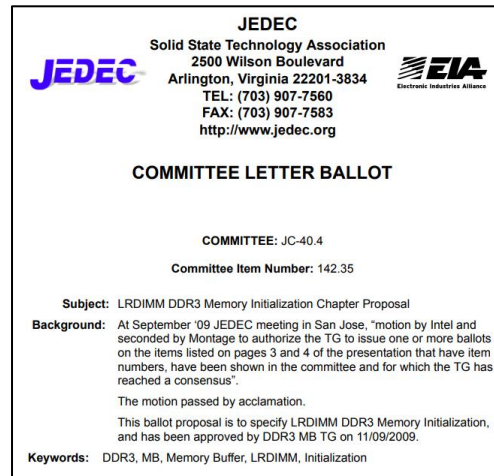
595: Paper 48 (Pet. Opp. to PO Mtn. to Exclude) at 3-13

Netlist's Motion to Exclude

EX1015 (JEDEC) is authenticated by Julie Carlson and SJ Park



EX1015

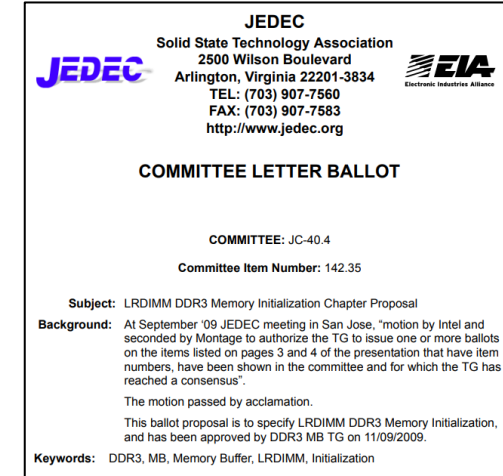


EX1050 (Carlson), Ex. A



Committee Item Number 142.35 (hereinafter "Item Number 142.35"), attached as Exhibit A, with the Subject "LRDIMM DDR3 Memory Initialization Chapter Proposal" is a proposal to the JC-40.4 committee for ballot approval. Ex. A. ... A true and correct copy of Item Number 142.35 is attached as Exhibit A JEDEC maintains all item numbers and letter ballots, such as Exhibits A and B, as business records, and it is the general practice of JEDEC employees and members to generate them at or around the time of the event they describe, and to keep them.

EX1050 (Carlson), ¶17

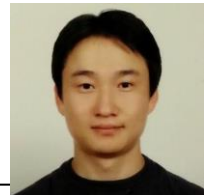


EX1055 (Park), Ex. B



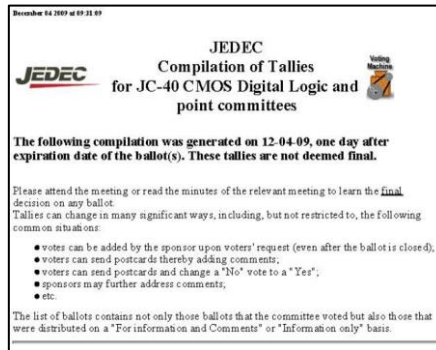
This file, "NB09320-.pdf" contains a technology proposal , Committee Item Number 142.35, which is attached as Exhibit B. As a member of the JC-40.4 committee, Samsung and I received both Exhibits A and B on or about November 11 , 2009, as indicated by the "Distributed" date on the Letter Ballot JC-40.4-09-320 and because, under JEDEC procedures, letter ballots were distributed to all committee members.

EX1055 (Park), ¶17

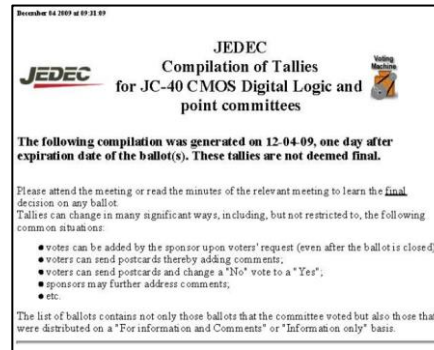


Netlist's Motion to Exclude

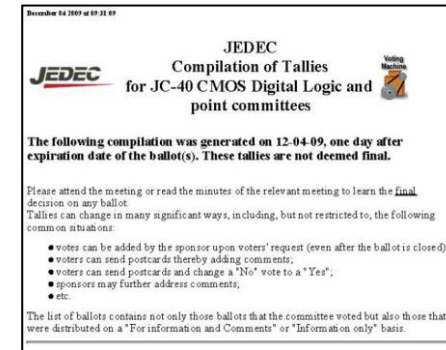
EX1037 (JEDEC, Compilation of Tallies for JC-40 CMOS Digital Logic and point committees (Dec. 4, 2009)) is authenticated by Julie Carlson and SJ Park



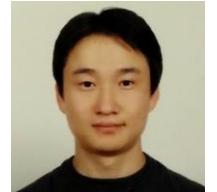
EX1037



EX1050 (Carlson), Ex. C



EX1055 (Park), Ex. C



“JEDEC Compilation of Tallies for JC-40 CMOS Digital Logic and point committees” (hereinafter, “JEDEC Tally for Item Number 142.35”), attached as Exhibit C, records JEDEC member votes for, among others, Letter Ballot for Item Number 142.35 on page 21. See Ex. C at 1, 21 (identifying “Committee Letter Ballot, JC-40.4-09-320, 142.35”). JEDEC Tally for Item Number 142.35 also confirms that Letter Ballot for Item Number 142.35 was distributed on November 11, 2009 to JC-40.4. Ex. C at 21.

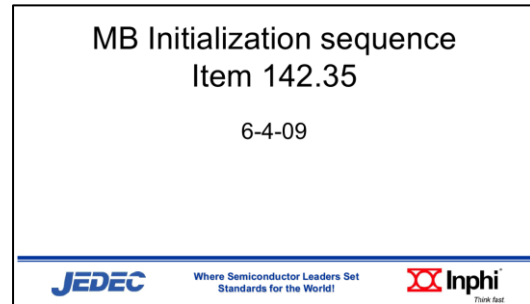
EX1050 (Carlson), ¶18

JEDEC Compilation of Tallies for JC-40 CMOS Digital Logic and point committees (hereinafter “Tally JC-40.4-09-320”) Shows that I (on behalf of Samsung) voted in favor of the technology proposed by Letter Ballot JC-40.4-09-320 on December 2, 2009. Ex. C at 40 (indicating “Letter Ballot JC-40.4-09-320 Item 142.35”).

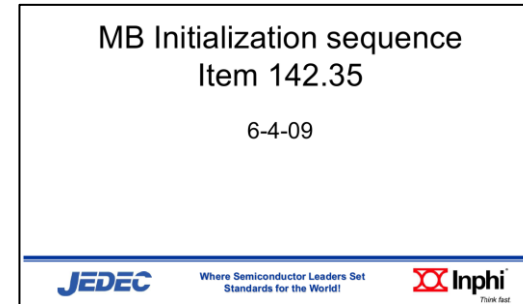
EX1055 (Park), ¶18

Netlist's Motion to Exclude

EX1039 (Inphi Corporation, "MB Initialization sequence Item 142.35," June 4, 2009) is authenticated by Julie Carlson



EX1039



EX1050 (Carlson), Ex. G



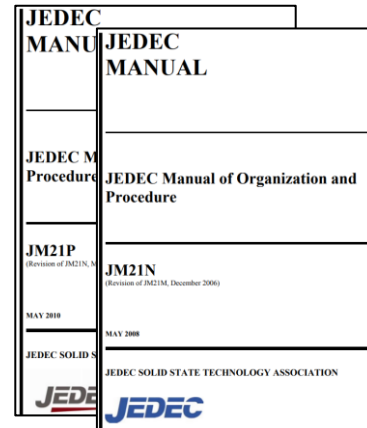
Exhibit G identifies Inphi Corp. as making the presentation “MB Initialization sequence Item 142.35,” (hereinafter, “142.35 Presentation”). Ex. G at 1. The 142.35 Presentation is dated June 4, 2009, and was presented to JC-40, as discussed as noted hereafter. Ex. G at 1. A true and correct copy of the 142.35 Presentation is attached as Exhibit G. As I noted above, JEDEC maintains specification proposals, such as Exhibit G, as business records, and it is the general practice of JEDEC employees and members to generate them at or around the time of the event they describe, and to keep them.

EX1050 (Carlson), ¶13

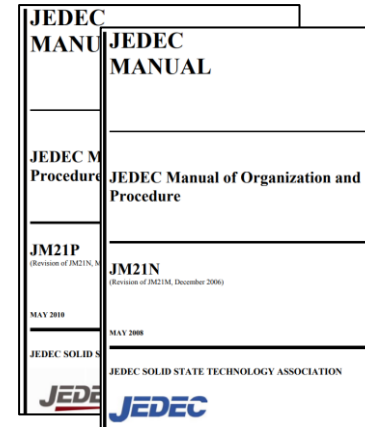
Netlist's Motion to Exclude

EX1048-49 (JEDEC Manuals of Organization and Procedure (2008-10)) are authenticated by Julie

Carlson



EX1048, EX1049



EX1050 (Carlson), Ex. I, J

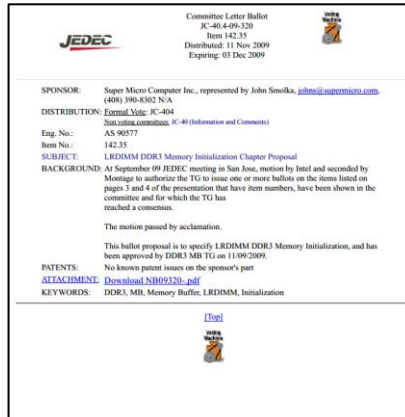


Attached as Exhibit I is a true and correct copy of the JEDEC Manual of Organization and Procedure JM21N (hereinafter "JM21N") in effect commencing May 2008. Attached as Exhibit J is a true and correct copy JEDEC Manual of Organization and Procedure JM21P, which revises JM21N, that went into effect commencing May 2010.

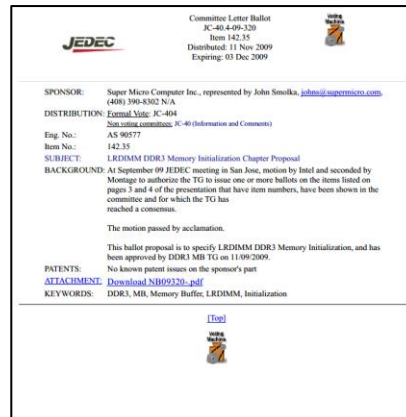
EX1050 (Carlson), ¶15

Netlist's Motion to Exclude

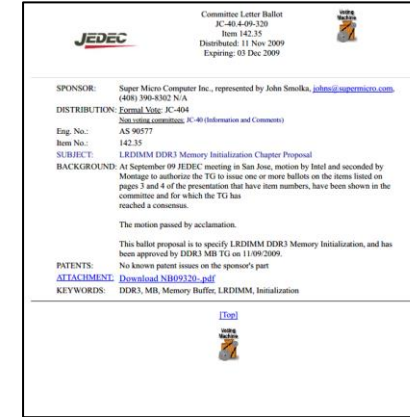
EX1051 ("Committee Letter Ballot, JC-40.4-09-320, Item 142.35," (Dec. 2009)) is authenticated by Julie Carlson and SJ Park



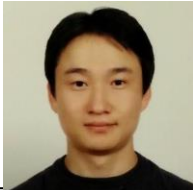
EX1051



EX1050 (Carlson), Ex. B



EX1055 (Park), Ex. A



After approval, **Committee Letter Ballot JC-40.4-09-320** (hereinafter "Letter Ballot for Item Number 142.35"), attached as **Exhibit B**, was distributed to the members of JEDEC JC-40.4 on November 11, 2009. Ex. B. ... A ... **true and correct copy of Letter Ballot for Item Number 142.35 is attached as Exhibit B**. As I noted above, JEDEC maintains all item numbers and letter ballots, such as Exhibits A and B, **as business records**, and it is the general practice of JEDEC employees and members to generate them at or around the time of the event they describe, and to keep them.

EX1050 (Carlson), ¶7

... Samsung received **Committee Letter Ballot JC-40.4-09-320** (hereinafter, "Letter Ballot JC-40.4-09-320") on or about November 11, 2009, as indicated by the "Distributed" date on this document and because, under JEDEC procedures, letter ballots were distributed to all committee members. **Ex. A. Letter Ballot JC-40.4-09-320 is attached as Exhibit A**. ... As a member of the JC-40.4 committee, Samsung and I **received both Exhibits A and B on or about November 11, 2009**, as indicated by the "Distributed" date on the Letter Ballot JC-40.4-09-320 and because, under JEDEC procedures, letter ballots were distributed to all committee members. Ex. A.

EX1055 (Park), ¶6-7

Netlist's Motion to Exclude

EX1024-25 and EX1056 (JEDEC Documents) are Authenticated by Comparison to Other Uncontested JEDEC documents

15. Attached as Exhibit I is a true and correct copy of the JEDEC Manual of Organization and Procedure JM21N (hereinafter "JM21N") in effect commencing May 2008. Attached as Exhibit J is a true and correct copy JEDEC Manual of Organization and Procedure JM21P, which revises JM21N, that went into effect commencing May 2010.

EX1050 (Declaration of Julie Carlson) at ¶ 15

Executed on June 3, 2020.



(signature)

Julie D. Carlson

(name printed)

EX1050 (Declaration of Julie Carlson) at p. 9

JEDEC MANUAL

JEDEC Manual of Organization and Procedure

JM21N

(Revision of JM21M, December 2006)

MAY 2008

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

JEDEC

EX1050 (Declaration of Julie Carlson),
Attachment I, Cover

JEDEC MANUAL

JEDEC Manual of Organization and Procedure

JM21P

(Revision of JM21N, May 2008)

MAY 2010

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

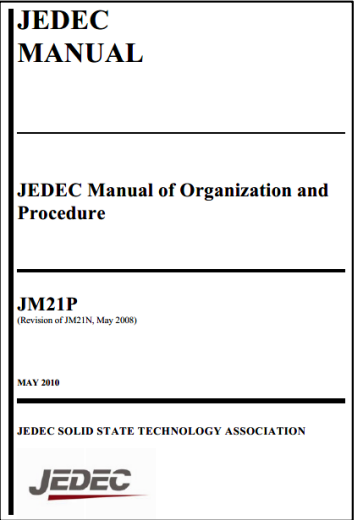
JEDEC

EX1050 (Declaration of Julie Carlson),
Attachment J, Cover



Netlist's Motion to Exclude

EX1024-25 and EX1056 (JEDEC Documents) are Authenticated by Comparison to Other Uncontested JEDEC documents

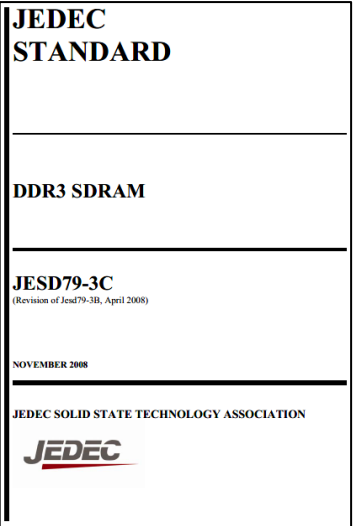


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Authenticity can be established by "[a] comparison with an authenticated specimen by ... the trier of fact." Fed. R. Evid. 901(b)(3).

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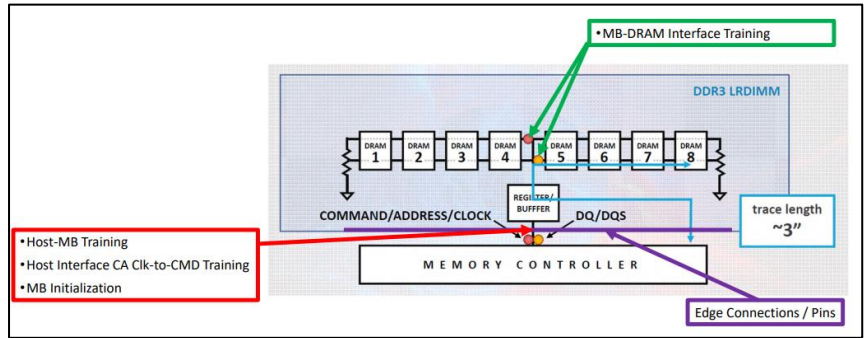


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Netlist's Motion to Exclude

EX1080 and EX1081 are figures annotated for Netlist's expert and discussed during his deposition



EX1081

Q. Do you see on the bottom right of Exhibit 1081 there's a label in **purple** that says "Edge Connection/Pins"?

A. Yes.

Q. Does the horizontal purple line on Exhibit 1081 provide a reasonable approximation of where the edge connections and pins would be located on a DDR3 LR-DIMM memory module?

THE WITNESS: Yes, it does.

EX1077 (Murphy Dep. Tr.) at 132:4-14

Q. And do you see on the upper right of Exhibit 1081 there's a label in **green**?

A. I do.

Q. Would it be fair to say that, on a DDR3 LR-DIMM, that MB-DRAM Interface Training does not require the edge connections and pins to be active?

A. Yes. Based on the JEDEC proposal, Exhibit 1015, that would be the case.

EX1077 (Murphy Dep. Tr.) at 131:14-21

Q. Do you see on the bottom left of Exhibit 1081 there's a label in **red**?

A. I do.

Q. And in your opinion would a person of ordinary skill in the art have known that, on a DDR3 LR-DIMM memory module, that Host-MB Training, Host Interface CA Clk-to-CMD Training and MB Initialization each require the edge connections and pins to be active?

THE WITNESS: Yes, I believe that's the case.

EX1077 (Murphy Dep. Tr.) at 132:16-133:3

Netlist's Motion to Exclude

The Challenged Exhibits Are Not Hearsay

Petitioner is not relying solely on the copyright date (or other printed date) to establish the date of each document

Exhibits 1015, 1036–37, 1039, 1048–49, and 1051 are business records of JEDEC under FRE 803(6):



JEDEC maintains **business records** to document when standards are modified, balloted, and approved, and when its standards are published. Through my work at JEDEC, **I am familiar with these business records** and standardization practices

EX1005 (Carlson) at ¶16



As I noted above, JEDEC maintains **all item numbers and letter ballots**, such as **Exhibits A and B**, as **business records**

EX1005 (Carlson) at ¶17



As I noted above, JEDEC maintains **all vote tallies**, such as those contained in **Exhibit C**, as **business records**

EX1005 (Carlson) at ¶9

As I noted above, JEDEC maintains **all item numbers and letter ballots**, such as **Exhibits D and E**, as **business records**

EX1005 (Carlson) at ¶10



As I noted above, JEDEC maintains **all vote tallies**, such as **Exhibit F**, as **business records**

EX1005 (Carlson) at ¶12



As I noted above, JEDEC maintains **specification proposals**, such as **Exhibit G**, as **business records**

EX1005 (Carlson) at ¶13



As I noted above, JEDEC maintains **meeting minutes**, such as **Exhibit H**, as **business records**

EX1005 (Carlson) at ¶14



Netlist's Motion to Exclude

Exhibit 1076 (declaration from Internet Archive) establishes Exhibits 1071-75 as business records as of the dates shown on those documents



7. Attached hereto as Exhibit A are true and accurate copies of screenshots of the Internet Archive's records of the archived files for the URLs and the dates specified in the attached coversheet of each printout.

DECLARATION OF NATHANIEL E FRANK-WHITE

I, NATHANIEL E FRANK-WHITE, declare as follows:

EX1076



District courts have taken judicial notice of the contents of webpages available through the Wayback Machine 'as facts that can be accurately and readily determined from sources whose accuracy **cannot reasonably be questioned**.'

Valve Corp. v. Ironburg Inventions Ltd., 8 F.4th 1364, 1374–75 (Fed. Cir. 2021)

John Halbert corroborates the dates of Exhibits 1071-75 based on his personal knowledge.

Q. Do you recognize Exhibit 1071 as a printout from the JEDEC website available to the public, listing out all of the JEDEC meetings in 2009?
THE WITNESS: Yes.



EX2022 (Halbert Dep. Tr.) at 34:11-16; *see also id* at 39:10-16 (regarding EX1072), 44:6-13 (regarding EX1073), 46:16-24 (regarding EX1074), 48:9-16 (regarding EX1075)

Netlist's Motion to Exclude

Exhibits 1024-25 and 1056 Are Not Hearsay Because They Are Merely Used to Show What a POSITA Would Have Known

Moreover, even assuming Patent Owner's Motion were the proper mechanism to address this issue, as argued by Petitioner, **the Federal Circuit has held that non-prior art evidence may be used**—as Exhibits 1017 and 1022 are used here—**to show the state of the art and the knowledge of one of ordinary skill in the art.** *See Yeda Research v. Mylan Pharm. Inc.*, 906 F.3d 1031, 1041 (Fed. Cir. 2018) (“[N]on-prior art evidence of what was known cannot be applied, independently, as teachings separately combinable with other prior art, but can be relied on for their proper supporting roles, e.g., indicating the level of ordinary skill in the art, what certain terms would mean to one with ordinary skill in the art, and how one with ordinary skill in the art would have understood a prior art disclosure.” (quotation and citation omitted)), *cited at* MTE Opp. 4–5; *see also* MTE 2 (admitting that Exhibits



We turn now to Patent Owner's third argument, that Exhibits 1017 and 1022 are inadmissible in that any copyright dates on these exhibits are hearsay not falling into any exception. MTE 3–4. We are not persuaded by this argument. As an initial matter, for the same reasons discussed as to the first argument, **the copyright date goes to public availability, which, under *Yeda Research*, is not a basis to exclude these two exhibits.** *See* MTE Opp. 7 (relying on the prior discussion as to this argument). **Thus, Petitioner need not rely on the date in the copyright marks for the truth of the matter asserted—i.e., the years.**¹⁷ *See id.* (arguing that “the dates listed on the disputed evidence are not hearsay because Petitioner is not relying on them ‘to prove the truth of the matter asserted’” (quoting Fed. R. Evid. 801(c)(2))). Accordingly, the copyright marks in Exhibits 1017 and 1022 are not hearsay in the context of how they are relied on by Petitioner in this proceeding.

Beable Education, Inc v. Achieve3000, Inc., IPR2021-01169, Paper 34, at 89–91 (PTAB Jan. 3, 2023) (citing *Yeda Research v. Mylan Pharm. Inc.*, 906 F.3d 1031, 1041 (Fed. Cir. 2018))

CLAIM CONSTRUCTION 06

'218 Patent - Claim Construction

Claim Term	Samsung's Proposed Construction	Board's Institution Decision
"memory read and write operations"	operations used to communicate data between the memory module and the memory controller in response to commands from the memory controller	"We determine that, at this stage of this proceeding, there is no need to expressly construe these claim terms in order to determine whether or not to institute review because the parties do not dispute the claimed terms' meanings, and their ordinary and customary meanings suffice for our analysis." '218 Paper 14 (ID) at 17
"mode"	No construction needed	
"training sequence"	a set of operations occurring in a particular order and used for training	
notification signal associated with the [one or more training sequences] / "information related to the [one or more training sequences]" / "open-drain signals related to the [one or more training sequences]"	unscheduled signal / information / open-drain signals provided without polling that indicate the status of the one or more training sequences	

'595 Patent - Claim Construction

Claim Term	Samsung's Proposed Construction	Board's Institution Decision
"memory read and write operations"	operations used to communicate data between the memory module and the memory controller in response to commands from the memory controller	"We determine that, at this stage of this proceeding, there is no need to expressly construe these claim terms in order to determine whether or not to institute review because the parties do not dispute the claimed terms' meanings, and their ordinary and customary meanings suffice for our analysis." '595 Paper 14 (ID) at 16
"normal memory read or write operations "	operations used to communicate data between the memory module and the memory controller in response to commands from the memory controller	
"mode"	No construction needed	
"training sequence"	a set of operations occurring in a particular order and used for training	
notification signal associated with the [one or more training sequences] / "information related to the [one or more training sequences]" / "open-drain signals related to the [one or more training sequences]"	unscheduled signal / information / open-drain signals provided without polling that indicate the status of the one or more training sequences	

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