

Displayed by Document Type

NUMBER	JEDEC Engineering Bulletins (JEB)	PRICE
JEB 5-A	METHODS OF MEASUREMENT FOR SEMICONDUCTOR LOGIC GATING MICROCIRCUITS: The purpose of this bulletin is to recommend for use in the rating of semiconductor logic gating microcircuits which use the binary states to represent and process logic information. Both static and dynamic measurements are covered. January 1970; Reaffirmed February 1984 /JEDEC Committee	\$63.00
JEB 6	STANDARD MEASUREMENTS OF THE ELECTRICAL CHARACTERISTICS OF SEMICONDUCTOR INTEGRATED CIRCUITS December 1966; Rescinded October 1984 /JEDEC	
JEB 15	TERMINOLOGY AND METHODS OF MEASUREMENT FOR BISTABLE SEMICONDUCTOR MICROCIRCUITS: This bulletin explains the terminology and methods of measurement for bistable semiconductor microcircuits. It is also intended to be used with the EIA Registration Data Format for semiconductor integrated bistable logic circuits. November 1969 /JC-40 Committee	\$109.00
JEB 16	USER GUIDE FOR MICROCIRCUIT FAILURE ANALYSIS: This guide defines generalized procedures for the failure analysis of monolithic integrated microelectronic circuits. Although the generalized procedural steps may apply to all microelectronic circuits, additional analysis steps unique to thin/thick film hybrid devices are not covered. July 1970 /JC-14 Committee	\$41.00
JEB 17	USER GUIDELINES FOR QUALITY AND RELIABILITY ASSURANCE OF LSI COMPONENTS November 1970; Rescinded April 1987 April 1987	
JEB 19	RECOMMENDED CHARACTERIZATION OF MOS SHIFT REGISTERS: This recommendation applies to MOS Shift Registers. Definitions are given for P-channel registers but are applicable to all CMOS and N-channel with changes in power supply notation. November 1972 /JC-40 Committee	\$40.00
JEB 20	ACCEPTED PRACTICES FOR MAKING MICROELECTRONIC DEVICE THERMAL CHARACTERISTICS TESTS January 1975; Rescinded November 1988 /JC-11 Committee	

NUMBER	Tentative Standards (TENTSTD)	PRICE
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TENTSTD 11 HANDLING AND INSTALLATION OF POWER SEMICONDUCTORS IN DISC TYPE PACKAGES: Included in JESD282 and EIA397.

July 1973; Rescinded June 1992 June 1992 /JC-22.2 Subcommittee

TENTSTD 12 STANDARD FOR SELENIUM SURGE SUPPRESSORS: The suppresser furnished under this standard shall be a product that has been tested and meets the definitions and minimum requirements specified herein.

November 1973 /JC-22.5 Subcommittee

\$49.00

NUMBER	JEDEC Specifications (JES)	PRICE
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JES 2 TRANSISTOR, GALLIUM ARSENIDE POWER FET, GENERIC SPECIFICATION: Establishes guideline requirements and quality assurance provisions for gallium arsenide power field-effect transistors (FETs, also know as MESFETs) designed for use in high-reliability space application such as spacecraft communications transmitters. Identifies the electrical parameters, wafer acceptance tests, screening tests, qualification tests, and lot acceptance tests pertinent to power GaAs FETs. Applicable to packaged and chip-carrier parts; portions may not be applicable to unpackaged and unmounted chips.

July 1992 /JC-14.7 Subcommittee

\$71.00

NUMBER	JEDEC Standards (JESD)	PRICE
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JESD 1 LEADLESS CHIP CARRIER PINOUTS STANDARDIZED FOR LINEARS: This standard shows how to convert existing DIP pinouts for op-amps, comparators, and D/A converters, to chip carrier packages.

April 1982 / Committee!33JC41

\$41.00

JESD 2 DIGITAL BIPOLAR LOGIC PINOUTS FOR CHIP CARRIERS: This standard provides a chip carrier format for digital devices by defining pin functions and locations for 20, 38, 44, 52, and 68-terminal devices.

December 1982 /JC-40.1 Subcommittee

\$41.00

JESD 22-A111 EVALUATION PROCEDURE FOR DETERMINING CAPABILITY TO BOTTOM SIDE BOARD ATTACH BY FULL BODY SOLDER IMMERSION OF SMALL SURFACE MOUNT SOLID STATE DEVICES: The purpose of this test method is to identify the potential wave solder classification level of small plastic Surface Mount Devices (SMDs) that are sensitive to moisture-induced stress so that they can be properly packaged, stored, and handled to avoid subsequent mechanical damage during the assembly wave solder attachment and/or repair operations. This test method also provides a reliability preconditioning sequence for small SMDs that are wave soldered

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using full body immersion. This test method, may be used by users to determine what classification level should be used for initial board level reliability qualification.

May 2004 June 2000 /JC-14.1 Subcommittee

\$47.00

JESD 3-C STANDARD DATA TRANSFER FORMAT BETWEEN DATA PREPARATION SYSTEM AND PROGRAMMABLE LOGIC DEVICE PROGRAMMER: This standard was developed to prevent the proliferation of data transfer formats that occurred with microprocessor development systems. The focus of the standard is on field programmable devices and their support tools. It is not intended for other types of semicustom logic devices or other types of fabrication or testing equipment.

June 1994 / Committee!33JC421

\$61.00

JESD 4 DEFINITION OF EXTERNAL CLEARANCE AND CREEPAGE DISTANCES OF DISCRETE SEMICONDUCTOR PACKAGES FOR THYRISTORS AND RECTIFIER DIODES: This standard defines reference distances between terminals of the device and the external package at specific voltages.

November 1983; Reaffirmed January 1991, April 1999, April 2002 April 2002 /JC-22.2 Subcommittee

\$38.00

JESD 5 MEASUREMENT OF TEMPERATURE COEFFICIENT OF VOLTAGE REGULATOR DIODES: This standard is designed to define voltage-temperature characteristic measurement techniques and a method of calculation. Although many methods could be defined, this method provides a desired uniformity and lends itself to production testing. Formerly JEDEC Suggested Standard No. 5A

February 1982; Reaffirmed April 1999, April 2002 April 2002 /JC-22.4 Subcommittee

\$38.00

JESD 6 MEASUREMENT OF SMALL VALUES OF TRANSISTOR CAPACITANCE: This standard gives a test method for measuring transistor capacitance using a three-terminal bridge which employs a guard-circuit that eliminates the effect of extraneous capacitance.

February 1967; Reaffirmed September 1981, April 1999, October 2002 /JC-25 Committee

\$47.00

JESD 7-A STANDARD FOR DESCRIPTION OF 54/74HCXXXX AND 54/74HCTXXXX HIGH SPEED CMOS DEVICES: This standard provides uniformity, multiplicity of sources, eliminate confusion, and ease of device specification and design by users for HC, and HCT CMOS devices. This standard specifies electrical parameters. It also includes appendices listing part numbers.

August 1986 / Committee!33JC402

\$109.00

JESD 8- 1 ADDENDUM No. 1 to JESD8: INTERFACE STANDARD FOR LOW VOLTAGE TTL-COMPATIBLE (LVTTTL) VLSI DIGITAL CIRCUITS

June 1994; Incorporated into JESD8-A, June 1994 /JC-16 Committee

JESD 8- 1- A INTERFACE STANDARD FOR NOMINAL 0.3 V/3.3 V SUPPLY DIGITAL INTEGRATED CIRCUITS

June 1994; Incorporated into JESD8-A, June 1994 /JC-16 Committee

JESD 8- 2 ADDENDUM No. 2 to JESD8 - STANDARD FOR OPERATING VOLTAGES AND INTERFACE LEVELS FOR LOW VOLTAGE EMITTER-COUPLED LOGIC (ECL) INTEGRATED CIRCUITS:

This Addendum No. 2 to JEDEC Standard No. 8 provides standard operating voltage and interface levels that can be used by designers and application engineers as they develop and introduce new products. Covers the ECL logic family designated 300K ECL. The 300K ECL family is Voltage and Temperature Compensated, with I/O interface levels compatible with the existing 100K ECL and 101K ECL families.

March 1993 /JC-16 Committee

\$40.00

JESD 8- 3 ADDENDUM No. 3 to JESD8 - GUNNING TRANSCEIVER LOGIC (GTL) LOW-LEVEL, HIGH-SPEED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS:

This Addendum No. 3 to JEDEC Standard No. 8 defines the dc input and output specifications for a low-level, high-speed interface for integrated devices.

November 1993 /JC-16 Committee

\$38.00

JESD 8- 4 ADDENDUM No. 4 to JESD8 - CENTER-TAP-TERMINATED (CTT) INTERFACE LOW-LEVEL, HIGH-SPEED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS:

This Addendum No. 4 to JEDEC Standard No. 8 defines the dc input and output specifications for a low-level, high-speed interface for integrated devices that can be a super-set of LVCMOS and LVTTTL.

November 1993 /JC-16 Committee

\$38.00

JESD 8- 5 ADDENDUM No. 5 to JESD8 - 2.5 V 0.2 V (NORMAL RANGE), AND 1.8 V TO 2.7 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUIT:

This standard defines power supply voltage ranges, dc interface parameters for a high speed, low voltage family of non-terminated digital circuits driving/driven by parts of the same family. The specifications in this standard represent a minimum set of 'base line' set of interface specifications for CMOS-compatible circuits.

October 1995 /JC-16 Committee

\$40.00

JESD 8- 6 ADDENDUM No. 6 to JESD8 - HIGH SPEED TRANSCEIVER LOGIC (HSTL) - A 1.5 V OUTPUT BUFFER SUPPLY VOLTAGE BASED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS:

This

standard is a 1.5 volt high performance CMOS-based interface document suitable for high I/O count CMOS and BiCMOS devices operating at frequencies in excess of 200 Mhz.

August 1995 /JC-16 Committee

\$48.00

JESD 8- 7 ADDENDUM No. 7 to JESD8 - 1.8 V + -0.15 V (NORMAL RANGE) , AND 1.2 V - 1.95 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUIT:

This standard continues the voltage specification migration to the next level beyond the 2.5 V specification already established. Since this migration is driven by both process changes and performance/power, more entries can be expected in supporting required voltage levels. The rapidity of this evolution is expecting to increase because of the same feature sizes expected.

February 1997 /JC-16 Committee

\$40.00

JESD 8- 8 ADDENDUM No. 8 to JESD8 - STUB SERIES TERMINATED LOGIC FOR 3.3 VOLTS (SSTL_3) A 3.3 V VOLTAGE BASED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS: This standard is a result of a major effort by the JC-16 Committee to develop a high performance CMOS-based interface suitable for high speed main memory applications in excess of 125 MHz.

August 1996 /JC-16 Committee

\$47.00

JESD 8- 9B ADDENDUM No. 9B to JESD8 - STUB SERIES TERMINATED LOGIC FOR 2.5 VOLTS (SSTL_2): Includes Errata and Corrected Page 7 as of October 18, 2002. This standard defines the input, output specifications and ac test conditions for devices that are designed to operate in the SSTL_2 logic switching range, nominally 0 V to 2.5 V. The standard may be applied to ICs operating with separate VDD and VDDQ supply voltages. This standard has been developed particularly with the objective of providing a relatively simple upgrade path from MOS push-pull interface designs. The standard is particularly intended to improve operation in situations where busses must be isolated from relatively large stubs.

May 2002 /JC-16 Committee

\$55.00

JESD 8-11 ADDENDUM No. 11 to JESD8 - 1.5 V +/- 0.1 V (NORMAL RANGE) AND 0.9 - 1.6 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUITS: This new standard provides specifications that will be used by several companies in new 1.5 V products designed in 0.12-0.15 um CMOS technologies, and in components that interface with them. The specifications allow limited interoperability with products using the existing JEDEC HSTL specification (JESD8-6).

October 2000 /JC-16 Committee

\$38.00

JESD 8-12	1.2 V +/- 0.1 V (NORMAL RANGE) AND 0.8 - 1.3 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUITS: This standard defines power supply voltage ranges, dc interface and switching parameters for a high speed, low voltage family of nonterminated digital circuits driving/driven by parts of the same family, or mixed families which comply with the input receiver specifications. The specifications in this standard represent a minimum set of interface specifications for CMOS compatible circuits. May 2001 /JC-16 Committee	\$37.00
JESD 8-13	SCALABLE LOW-VOLTAGE SIGNALING FOR 400 mV (SLVS-400): This standard defines the input, output, and termination specifications for differential signaling in the SLVS-400 environment, nominally between 0 and 400 mV. Power supplies other than the nominal 800 mV power for the SLVS interface are not specified. October 2001 /JC-16 Committee	\$41.00
JESD 8-14	1.0 V +/- 0.1 V (NORMAL RANGE) AND 0.7 V - 1.1 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUITS: This new standard provides specifications that will be used by several companies in new 1.0 V products designed in 0.10-0.12 μ m CMOS technologies, and in components that interface with them. This standard defines power supply voltage ranges, dc interface and switching parameters for a high speed, low voltage family of nonterminated digital circuits driving/driven by parts of the same family, or mixed families which comply with the input receiver specifications. The specifications in this standard represent a minimum set of interface specifications for CMOS compatible circuits. December 2001 /JC-16 Committee	\$38.00
JESD 8-15A	STUB SERIES TERMINATED LOGIC FOR 1.8 V (SSTL₁₈): This standard defines the input, output specifications and ac test conditions for devices that are designed to operate in the SSTL ₁₈ logic switching range, nominally 0 V to 1.8 V. The standard may be applied to ICs operating with separate VDD and VDDQ supply voltages. The VDD value is not specified in this standard; however VDD and VDDQ will have the same voltage level in many cases. September 2003 /JC-16 Committee	\$49.00
JESD 8-B	INTERFACE STANDARD FOR NOMINAL 0.3 V/3.3 V SUPPLY DIGITAL INTEGRATED CIRCUITS: This standard (a replacement of JEDEC Standards No. 8, 8-1, 8-1-A, and 8-A) defines dc interface parameters for a family of digital circuits operating from a power supply of nominal 3.0 V/3.3. V and driving/driven by parts of the same family. The specifications in this standard represent a	

minimum set of 'base line' set of interface specifications for LVTTL-compatible and LVCMOS-compatible circuits.

September 1999 /JC-16 Committee

\$40.00

JESD 9-A METAL PACKAGE SPECIFICATION FOR MICROELECTRONIC PACKAGES AND COVERS: This standard establishes the general requirements and quality assurance provisions that can be specified and met in procuring microelectronics packages and covers, manufactured from matched seal with and without high thermal conductivity base materials, intended for use in fabricating hybrid microelectronics circuits. This document details those minimum requirements necessary for metal packages' use exclusively.

April 1987; Under Revision /JC-13.5 Subcommittee

\$71.00

JESD 10 LOW FREQUENCY POWER TRANSISTORS: This standard consists of a listing of letter symbols, terms, and definitions that are used in power transistors. It also includes information on JEDEC registration procedures, verification tests, and thermal characteristics.

January 1976; Reaffirmed September 1981, October 2002 April 1999 /JC-25 Committee

\$147.00

JESD 11 CHIP CARRIER PINOUTS STANDARDIZED FOR CMOS 4000, HC AND HCT SERIES OF LOGIC CIRCUITS: This standard indicates the procedures used to convert existing DIP and flat packages for digital parts (SSI & MSI) to chip carrier packages.

December 1984 / Committee!33JC402

\$41.00

JESD 12 SEMICUSTOM INTEGRATED CIRCUITS (FORMERLY PUBLISHED AS STANDARD FOR GATE ARRAY BENCHMARK SET): The purpose of these benchmarks is to provide a common set of high level functions which serve as vehicles for comparing the performance of gate arrays implemented in any technology using any internal structure. These benchmarks effectively provide an unbiased measure of gate array vendors' ability to implement a desired complex function on a particular gate array at a known level of performance.

June 1985 / Committee!33JC44

\$43.00

JESD 12-1B ADDENDUM No. 1 to JESD12 - TERMS AND DEFINITIONS FOR GATE ARRAYS AND CELL-BASED INTEGRATED CIRCUITS: The purpose of this standard is to promote the uniform use of abbreviations, terms, and definitions throughout the semiconductor industry. It is a useful guide for users, manufactures, educators, technical writers, and others interested in the characterization, nomenclature, and classification of semicustom integrated circuits.

August 1993 / Committee!33JC44

\$48.00

JESD 12-2	ADDENDUM No. 2 to JESD12 - STANDARD FOR CELL-BASED INTEGRATED CIRCUIT BENCHMARK SET: The purpose of these benchmarks is to provide a common set of high level functions that serve as vehicles for comparing the performance of cell-based ICs implemented in any technology using any internal structure. JESD12-2 extends the gate array benchmark set (JESD12) to cell-based ICs. February 1986 / Committee!33JC44	\$61.00
JESD 12-3	ADDENDUM No. 3 to JESD12 - CMOS GATE ARRAY MACROCELL STANDARD: This standard defines a minimum set of macro cell standards for CMOS gate arrays. A total of 41 macro cell types are addressed, all of which are commonly used by gate array designers to implement Application Specific Integrated Circuits. June 1986 / Committee!33JC44	\$47.00
JESD 12-4	ADDENDUM No. 4 to JESD12 - METHOD OF SPECIFICATION OF PERFORMANCE PARAMETERS FOR CMOS SEMICUSTOM INTEGRATED CIRCUITS: This standard defines how to specify various performance parameters of semicustom ICs, including cell and interconnect propagation delays, input/output levels and capacitance, and power dissipation. April 1987 / Committee!33JC44	\$48.00
JESD 12-5	ADDENDUM No. 5 to JESD12 - DESIGN FOR TESTABILITY GUIDELINES: This standard is intended to provide circuit designers with the information needed to develop complex integrated circuits that can be reliably and economically tested without compromising flexibility. August 1988 / Committee!33JC44	\$109.00
JESD 12-6	ADDENDUM No. 6 to JESD12 - INTERFACE STANDARD FOR SEMICUSTOM INTEGRATED CIRCUITS: This standard defines logic interface levels for CMOS, TTL, ECL, and BiCC inputs and outputs. This standard is intended to provide an industry-wide set of specifications, for Application Specific Integrated Circuit (ASIC) signal inputs and outputs, both necessary and sufficient to define a circuits electrical interfacing with the external environment. JESD12-6 is intended to provide the ASIC manufacturer and user with a common set of signal interface levels. The standard defines interface levels for 5 volt operation. March 1991 / Committee!33JC44	\$43.00
JESD 13-B	STANDARD SPECIFICATION FOR DESCRIPTION OF B SERIES CMOS DEVICES: This standard provides for uniformity, multiplicity of sources, elimination of confusion, and ease of device specifications and system design by users. It gives electrical levels and timing diagrams for B Series CMOS devices.	

May 1980 / Committee!33JC402

\$63.00

JESD 14	SEMICONDUCTOR POWER CONTROL MODULES: Semiconductor Power Control Modules (SPCM) are modules consisting of thyristors or transistors, or both, as the primary controlling elements. Methods of manufacture of semiconductor power control modules include the assembling of individual components and the use of semiconductor hybrids or monolithic processing technologies, or both. November 1986; Reaffirmed June 1992, April 1999, April 2002 April 2002 /JC-22.2 Subcommittee	\$47.00
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JESD 16-A	ASSESSMENT OF AVERAGE OUTGOING QUALITY LEVELS IN PARTS PER MILLION (PPM): This standard was revised to clarify assumptions necessary to estimate AOQ, revise the minimum sample size algorithm, address small sample size concerns, and provide methods for combining groups for AOQ estimation. Derivation of any new methods for combining groups for AOQ estimation. Derivation of any new methods introduced into this document have been provided in annexes. A statistical method is based on confidence interval statistics. A procedure was established for reporting AOQ when the minimum sample size criterion is not met. April 1995 /JC-13 Committee	\$61.00
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JESD 17	LATCH-UP IN CMOS INTEGRATED CIRCUITS - SUPERSEDED BY JESD78, February 1999 August 1988; Rescinded February 1999 February 1999 / Committee!33JC402	
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JESD 18-A	STANDARD FOR DESCRIPTION OF FAST CMOS TTL COMPATIBLE LOGIC: The purpose of this standard is to provide for uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users. The standard covers specifications for description of '54/74FCTXXXX' series fast CMOS TTL compatible devices. January 1993 / Committee!33JC402	\$63.00
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JESD 19	GENERAL STANDARD FOR STATISTICAL PROCESS CONTROL (SPC) - SUPERSEDED by EIA-557-A July 1988; Rescinded July 1995 /JC-13 Committee	
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JESD 20	STANDARD FOR DESCRIPTION OF 54/74ACXXXXX AND 54/74ACTXXXXX ADVANCED HIGH-SPEED CMOS DEVICES: This standard describes electrical parameters for this class of CMOS devices. September 1990 / Committee!33JC402	\$147.00
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JESD 21-C CONFIGURATIONS FOR SOLID STATE MEMORIES: This revision of JESD21 is substantially different from previous issues because it reflects advancement in semiconductor technology and computer design needs. A new class of memory devices, the multiport DRAM (MPDRAM) C also know as 'Video Ram' because of the most common application for the devices C is represented. A new family of SRAMs which addresses the increasing need for high speed is introduced. Additional families of devices in the SOJ and Zip packages are included. The material in this revision is organized primarily by function (ROM, EPROM, SRAM, DRAM, etc.) rather than by technology and word length. Pinouts for SIMM and DIMM are included along with presence detect schemes. A current set of terms has also been included. JESD21-C is a compilation of all memory device standards that have been developed by the JC-42 Committee and approved by the JEDEC BoD from September 1989 to present. This latest issue has changed to a loose-leaf format and comes in a three-ring binder so that new drawings can be added without requiring a new publication. Time of publication of the material is identified by release number, i.e., if marked Release 8, this item was approved and released in 1998, if marked Release 13, this item was approved and released in 2003. May 2003; Under Revision Sections in this document may be under revision at any time. /JC-42 Committee \$150.00

JESD 21-C ANNUAL UPDATING SERVICE: The JEDEC Office has generated a mailing list for those who wish to subscribe to updates of this publication. A payment is required for subscription to this updating service. January 2004 /JC-42 Committee \$50.00

JESD 22-A100-B CYCLED TEMPERATURE HUMIDITY BIAS LIFE TEST: The Cycled Temperature-humidity-bias Life Test is performed for the purpose of evaluating the reliability of nonhermetic packaged solid state devices in humid environments. It employs conditions of temperature cycling, humidity, and bias that accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors that pass through it. The Cycled Temperature-Humidity-Bias Life Test is typically performed on cavity packages (e.g. MQUADs, lidded ceramic pin grid arrays, etc.) as an alternative to JESD22-A101 or JESD22-A110. April 2000 /JC-14.1 Subcommittee \$40.00

JESD 22-A101-B STEADY-STATE TEMPERATURE HUMIDITY BIAS LIFE TEST: This standard establishes a defined method and conditions for performing a temperature humidity life test with bias applied. The test is used to evaluate the reliability of non-hermetic packaged solid state devices in humid environments. It employs high

temperature and humidity conditions to accelerate the penetration of moisture through external protective material or along interfaces between the external protective coating and conductors or other features which pass through it. This revision enhances the ability to perform this test on a device which cannot be biased to achieve very low power dissipation.

April 1997 /JC-14.1 Subcommittee

\$40.00

**JESD 22-
A102-C**

ACCELERATED MOISTURE RESISTANCE - UNBIASED AUTOCLAVE:

This test allows the user to evaluate the moisture resistance of nonhermetic packaged solid state devices. The Unbiased Autoclave Test is performed to evaluate the moisture resistance integrity of non-hermetic packaged solid state devices using moisture condensing or moisture saturated steam environments. It is a highly accelerated test which employs conditions of pressure, humidity and temperature under condensing conditions to accelerate moisture penetration through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors passing through it. This test is used to identify failure mechanisms internal to the package and is destructive.

December 2000 /JC-14.1 Subcommittee

\$38.00

**JESD 22-
A103-B**

HIGH TEMPERATURE STORAGE LIFE: The test is applicable for evaluation, screening, monitoring, and/or qualification of all solid state devices. High Temperature storage test is typically used to determine the effect of time and temperature, understorage conditions, for thermally activated failure mechanisms of solid state electronic devices, including nonvolatile memory devices (data retention failure mechanisms). During the test elevated temperatures (accelerated test conditions) are used without electrical stress applied. This test may be destructive, depending on Time, Temperature and Packaging (if any).

August 2001 /JC-14.1 Subcommittee

\$38.00

**JESD 22-
A104-B**

TEMPERATURE CYCLING: This standard provides a method for determining solid state devices capability to withstand extreme temperature cycling. Changes in this revision include requirements that the worst-case load temperature must reach the specific extremes rather than just requiring that the chamber ambient temperature reach the extremes. This ensures that the test specimens will reach the specified temperature extremes regardless of chamber loading. Definitions are provided for Load, Monitoring Sensor, Worst-Case Load Temperature, and Working Zone. The transfer time has been tightened from 5 minutes to 1 minute. Five new test conditions have been added as well as a caution on test conditions which exceed the glass transition temperature of plastic package solid devices.

July 2000 /JC-14.1 Subcommittee

\$43.00

JESD 22-A106B	THERMAL SHOCK: This test is conducted to determine the resistance of a part to sudden exposure to extreme changes in temperature and to the effect of alternate exposures to these extremes. June 2004 January 2003 /JC-14.1 Subcommittee	\$40.00
JESD 22-A107B	SALT ATMOSPHERE: This salt Atmosphere test is conducted to determine the resistance of solid state devices to corrosion. It is an accelerated test that simulates the effects of severe seacoast atmosphere on all exposed surfaces. The salt atmosphere test is considered destructive. It is intended for lot acceptance, process monitor, and qualification testing. January 2004 January 2003 /JC-14.1 Subcommittee	\$38.00
JESD 22-A108-B	TEMPERATURE, BIAS, AND OPERATING LIFE: A revised method for determining the effects of bias conditions and temperature, over time, on solid state devices is now available. Revision B of A108 includes low temperature operating life (LTOL) and high temperature gate bias (HTGB) stress conditions, revised cool down requirements for high temperature stress, and a procedure to follow if parts are not tested within the allowed time window. December 2000 /JC-14.1 Subcommittee	\$40.00
JESD 22-A109-A	HERMETICITY: This revised test method establishes a standard procedure for determining the effectiveness of the seal of hermetically sealed solid state devices. The objective of this revision was to modify the test parameters to reflect current practice and to eliminate the specification of fluorocarbons, banned from use due to environmental concerns. July 2001 /JC-14.1 Subcommittee	\$43.00
JESD 22-A110-B	HIGHLY ACCELERATED TEMPERATURE AND HUMIDITY STRESS TEST (HAST) The purpose of this new test method is to evaluate the reliability of nonhermetic packaged solid state devices in humid environments. It employs severe conditions of temperature, humidity, and bias that accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it. February 1999; Under Revision /JC-14.1 Subcommittee	\$40.00
JESD 22-A112-A	MOISTURE-INDUCED STRESS SENSITIVITY FOR PLASTIC SURFACE MOUNT DEVICES - SUPERSEDED BY J-STD-020A, April 1999. See J-STD-020B, published July 2002. November 1995; Rescinded May 2000 May 2000 /JC-14.1 Subcommittee	
JESD 22-A113D	PRECONDITIONING OF PLASTIC SURFACE MOUNT DEVICES PRIOR TO RELIABILITY TESTING: This Test Method establishes an industry	

standard preconditioning flow for nonhermetic solid state SMDs (surface mount devices) that is representative of a typical industry multiple solder reflow operation. These SMDs should be subjected to the appropriate preconditioning sequence of this document by the semiconductor manufacturer prior to being submitted to specific in-house reliability testing (qualification and reliability monitoring) to evaluate long term reliability (which might be impacted by solder reflow).

August 2003 /JC-14.1 Subcommittee

\$45.00

**JESD 22-
A114-B**

ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY TESTING HUMAN BODY MODEL (HBM) : This test method establishes a standard procedure for testing and classifying microcircuits according to their susceptibility to damage or degradation by exposure to a defined electrostatic Human Body Model (HBM) discharge (ESD). The objective is to provide reliable, repeatable HBM ESD test results so that accurate classifications can be performed.

June 2000 /JC-14.1 Subcommittee

\$45.00

**JESD 22-
A115-A**

ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY TESTING MACHINE MODEL (MM) : This method establishes a standard procedure for testing and classifying microcircuits according to their susceptibility to damage or degradation by exposure to a defined Machine Model (MM) electrostatic discharge (ESD). The objective is to provide reliable, repeatable MM ESD test results so that accurate classifications can be performed.

October 1997; Under Revision /JC-14.1 Subcommittee

\$45.00

**JESD 22-
A117**

ELECTRICALLY ERASABLE PROGRAMMABLE ROM (EEPROM) PROGRAM/ERASE ENDURANCE AND DATA RETENTION TEST: This method establishes a standard procedure for determining the data cycling endurance and data retention capability of non-volatile memory cells. It is intended as a qualification and monitor test procedure. This test is also applicable to FLASH EEPROM integrated circuits and Erasable Programmable Logic Devices (EPLD) with embedded EEPROM or FLASH memory.

January 2000 /JC-14.1 Subcommittee

\$40.00

**JESD 22-
A118**

ACCELERATED MOISTURE RESISTANCE - UNBIASED HAST: The Unbiased HAST is performed for the purpose of evaluating the reliability of non-hermetic packaged solid-state devices in humid environments. It is a highly accelerated test which employs temperature and humidity under non-condensing conditions to accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it. Bias is not applied in this test to ensure the failure mechanisms potentially overshadowed by bias can be uncovered (e.g. galvanic corrosion). This test is used to

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identify failure mechanisms internal to the package and is destructive.

December 2000 /JC-14.1 Subcommittee

\$41.00

JESD 22-A120

TEST METHOD FOR THE MEASUREMENT OF MOISTURE DIFFUSIVITY AND WATER SOLUBILITY IN ORGANIC MATERIALS USED IN

INTEGRATED CIRCUITS: This specification details the procedures for the measurement of characteristic bulk material properties of moisture diffusivity and water solubility in organic materials used in the packaging of IC components. These two material properties are important parameters for the effective reliability performance of plastic packaged ICs after exposure to moisture and subjected to high temperature solder reflow.

June 2001 /JC-14.1 Subcommittee

\$41.00

JESD 22-B100B

PHYSICAL DIMENSION: The standard provides a method for determining whether the external physical dimensions of the device are in accordance with the applicable procurement document. This revision includes a change in details to be specified by the procurement document.

June 2003 September 2002 /JC-14.1 Subcommittee

\$38.00

JESD 22-B101

EXTERNAL VISUAL: The purpose of this inspection is to verify that the materials, design, construction, markings, and workmanship of the device are in accordance with the applicable procurement document. External visual is a nondestructive test and applicable for all package types. The test is useful for qualification, process monitor, or lot acceptance.

September 1987; Under Revision /JC-14.1 Subcommittee

\$37.00

JESD 22-B102-C

SOLDERABILITY: The purpose of this test method is to provide a means of determining the solderability of device package terminations that are intended to be joined to another surface using solder for the attachment. It also provides optional conditions for aging and soldering for the purpose of allowing simulation of the soldering process to be used in the device applications. It provides procedures for dip and look solderability testing of through hole, axial and surface mount devices and reflow simulated use testing for surface mount packages.

September 1998; Under Revision /JC-14.1 Subcommittee

\$49.00

JESD 22-B103-B

VIBRATION, VARIABLE FREQUENCY: The Vibration, Variable Frequency Test Method is intended to determine the ability of component(s) to withstand moderate to severe vibration as a result of motion produced by transportation or field operation of electrical equipment. This is a destructive test that is intended for component qualification.

June 2002; Under Revision /JC-14.1 Subcommittee

\$43.00

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**JESD 22-
B104-B**

MECHANICAL SHOCK: This test is intended to determine the suitability of component parts for use in electronic equipment that may be subjected to moderately severe shocks as a result of suddenly applied forces or abrupt changes in motion produced by rough handling, transportation, or field operation. Shock of this type may disturb operating characteristics, particularly if the shock pulses are repetitive. This is a destructive test intended for device qualification. It is normally applicable to cavity-type packages.

May 2001 /JC-14.1 Subcommittee

\$38.00

**JESD 22-
B105C**

LEAD INTEGRITY: This test method provides various tests for determining the integrity lead/package interface and the lead itself when the lead(s) are bent due to faulty board assembly followed by rework of the part for reassembly. For hermetic packages it is recommended that this test be followed by hermeticity tests in accordance with Test Method A109 to determine if there are any adverse effects from the stresses applied to the seals as well as to the leads. These tests, including each of its test conditions, is considered destructive and is only recommended for qualification testing. This test is applicable to all through-hole devices and surface-mount devices requiring lead forming by the user.

May 2003 /JC-14.1 Subcommittee

\$48.00

**JESD 22-
B106-B**

RESISTANCE TO SOLDERING TEMPERATURE FOR THROUGH-HOLE MOUNTED DEVICES: This method established a standard procedure for determining whether through-hole solid state devices can withstand the effects of the temperature to which they will be subject during soldering of their leads. This revision updates the references to currently military standards.

February 1999 /JC-14.1 Subcommittee

\$38.00

**JESD 22-
B107B**

MARKING PERMANENCY: This test method provides two tests for determining the marking permanency of ink marked integrated circuits. A new non-destructive tape test method is introduced to quickly determine marking integrity. The test method also specifies a resistance to solvents method based upon MIL Std 883 Method 2015.

January 2004 June 2002 /JC-14.1 Subcommittee

\$49.00

**JESD 22-
B108A**

COPLANARITY TEST FOR SURFACE-MOUNT SEMICONDUCTOR DEVICES: The purpose of this test is to measure the deviation of the terminals (leads or solder balls) from coplanarity for surface-mount semiconductor devices.

January 2003 /JC-14.1 Subcommittee

\$41.00

**JESD 22-
B109**

FLIP CHIP TENSILE PULL: The Flip Chip Tensile Pull Test Method is performed to determine the fracture mode and strength of the solder bump interconnection between the flip chip die and the

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substrate. It should be used to assess the consistency of the chip join process. This test method is a destructive test.

June 2002 /JC-14.1 Subcommittee

\$41.00

JESD 22-B110

SUBASSEMBLY MECHANICAL SHOCK: The new test method JESD22-B110 provides guidance for in-situ testing of mechanical shock resistance of components as mounted in a subassembly. Using terms, procedures, and test levels in common with JESD22-B104B, this test method provides a range of test level options to improve test applicability and compatibility with fragility test procedures. Test procedures are detailed, including test card and fixture needs, test tolerances, test documentation, component preparation, and definition of terms.

May 2001 /JC-14.1 Subcommittee

\$41.00

JESD 22-B116

WIRE BOND SHEAR TEST: This test method establishes a standard procedure for determining the strength of an integrated circuit wire bond by shearing the wire from the surface it is bonded to and measuring the force required. This method serves as an alternative to pulling the wire vertically until the wire separates from one of its two bonded surfaces. It also provides guidelines for determining an appropriate minimum shear force for gold balls on aluminum alloy bonding surfaces.

July 1998 /JC-14.1 Subcommittee

\$45.00

JESD 22-B117

BALL GRID ARRAY (BGA) BALL SHEAR: Test method for BGA Ball Shear. This test method has ball shear terms and definitions; apparatus description; the BGA ball shear procedure; and BGA ball shear failure modes and their criteria. Where applicable, figures are included to show the apparatus and six typical failure modes.

July 2000 /JC-14.1 Subcommittee

\$41.00

JESD 22-C100-A

HIGH TEMPERATURE CONTINUITY - RESCINDED, November 1999

April 1990; Rescinded November 1999 /JC-14.1 Subcommittee

JESD 22-C101B.01

FIELD-INDUCED CHARGED-DEVICE MODEL TEST METHOD FOR ELECTROSTATIC DISCHARGE WITHSTAND THRESHOLDS OF MICROELECTRONIC COMPONENTS: This new test method describes a uniform method for establishing charged-device model electrostatic discharge withstand thresholds. The charged-device-model simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing. One of many examples is a device sliding down a shipping tube hitting a metal surface. Discharges to devices on unterminated circuit assemblies are also well-modeled by the CDM test. DM ESD events not only reduce assembly yields but can also produce device

damage that goes undetected by factory test and later is the cause of a latent failure.

June 2004 An error was found in the document published 5/2004. \$47.00
See annex A for details June 2003 /JC-14.1 Subcommittee

JESD 23 TEST METHODS AND CHARACTER DESIGNATION FOR LIQUID CRYSTAL DEVICES: This standard specifies a collection of procedures for testing and character designation of liquid crystal devices.
May 1982 \$57.00

JESD 24 POWER MOSFETS: This standard contains a listing of terms and definitions and letter symbols; a description of established procedures that are followed in the assignment of semiconductor-industry-type designations to power transistors; electrical verification test; thermal characteristics; and a user's guide.
July 1985 /JC-25 Committee \$71.00

JESD 24- 1 ADDENDUM No. 1 to JESD24 - METHOD FOR MEASUREMENT OF POWER DEVICE TURN-OFF SWITCHING LOSS: Describes the method of a typical oscilloscope waveform and the basic test circuit employed in the measurement of turn off loss for bipolar, IGBT and MOSFET power semiconductors. This method can be used as a standard for evaluating power semiconductor turn-off switching loss capability and defines standard terminology that should be referenced within the electronic industry.
October 1989; Reaffirmed April 1999, October 2002 /JC-25 Committee \$41.00

JESD 24- 2 ADDENDUM No. 2 to JESD24 - GATE CHARGE TEST METHOD: This addendum establishes a method for measuring power device gate charge. A gate charge test is performed by driving the device gate with a constant current and measuring the resulting gate voltage response. Constant gate current scales the gate voltage, a function of time, to a function of coulombs. The slope of the generated response reflects the active device capacitance as it varies during the switching transition . Gate charge measurements are useful for characterizing the large signal switching performance of power MOS and IGBT devices. Developed over a four year span by the JEDEC JC-25 Committee, the method defines a repeatable means of measuring the widely published Qgd charge values.
January 1991; Reaffirmed October 2002 April 1999 /JC-25 Committee \$41.00

JESD 24- 3 ADDENDUM No. 3 to JESD24 - THERMAL IMPEDANCE MEASUREMENTS FOR VERTICAL POWER MOSFETS (DELTA SOURCE-DRAIN VOLTAGE METHOD) : The purpose of this test method is to measure the thermal impedance of the MOSFET under the specified conditions of applied voltage, current and pulse duration. The temperature

sensitivity if the forward voltage drop of the source-drain is used as the junction temperature indicator. This method is particularly suitable to enhancement mode, power MOSFETs having relatively long thermal response times. This test method may be used to measure the thermal response of junction to a heating pulse, to ensure proper die mountdown to its case, or the dc thermal resistance, by the proper choice of the pulse duration and magnitude if the heating pulse.

November 1990; Reaffirmed April 1999 /JC-25 Committee

\$47.00

JESD 24- 4 ADDENDUM No. 4 to JESD24 - THERMAL IMPEDANCE MEASUREMENTS FOR BIPOLAR TRANSISTORS (DELTA BASE-EMITTER VOLTAGE METHOD) :

The purpose of this test method is to measure the thermal impedance of the Bipolar Transistor under the specified conditions of applied voltage, current and pulse duration. The temperature sensitivity of the base-emitter voltage is used as the junction temperature indicator. This test method is used to measure the thermal response of the junction to a heating pulse. Specifically, the test may be used to measure dc thermal resistance, and to ensure proper die mountdown to its case. This is accomplished through the appropriate choice of pulse duration and heating power magnitude.

November 1990; Reaffirmed October 2002 April 1999 /JC-25 Committee

\$47.00

JESD 24- 5 ADDENDUM No. 5 to JESD24 - SINGLE PULSE UNCLAMPED INDUCTIVE SWITCHING (UIS) AVALANCHE TEST METHOD: This method describes a means for testing the ability of a power switching device to withstand avalanche breakdown.

August 1990; Reaffirmed october 2002 April 1999 /JC-25 Committee

\$38.00

JESD 24- 6 ADDENDUM No. 6 to JESD24 - THERMAL IMPEDANCE MEASUREMENTS FOR INSULATED GATE BIPOLAR TRANSISTORS:

This standard describes in detail the method for thermal measurements of Insulated Gate Bipolar Transistors (IGBTs) and is suitable for use both in manufacturing and application of the devices. The method covers both thermal transient and thermal equilibrium measurements for manufacturing process control and device characterization purposes. Properly implemented, JESD24-6 provides a basis for obtaining realistic thermal parametric values that will benefit supplier's internal effectiveness and will be useful to the design and manufacturer of reliable IGBT circuits.

October 1991; Reaffirmed October 2002 April 1999 /JC-25 Committee

\$47.00

JESD 24- 7 ADDENDUM No. 7 to JESD24 - COMMUTATING DIODE SAFE OPERATING AREA TEST PROCEDURE FOR MEASURING dv/dt DURING

REVERSE RECOVERY OF POWER TRANSISTORS: Defines methods for verifying the diode recovery stress capability of power transistors.

August 1982; Reaffirmed October 2002 April 1999 /JC-25 Committee

\$40.00

JESD 24- 8 ADDENDUM No. 8 to JESD24 - METHOD FOR REPETITIVE INDUCTIVE LOAD AVALANCHE SWITCHING: Determines the repetitive inductive avalanche switching capability of power switching transistors.

August 1992; Reaffirmed October 2002 April 1999 /JC-25 Committee

\$40.00

JESD 24- 9 ADDENDUM No. 9 to JESD24 - SHORT CIRCUIT WITHSTAND TIME TEST METHOD: Test method to determine how long a device can survive a short circuit condition with a given drive level.

August 1992; Reaffirmed October 2002 April 1999 /JC-25 Committee

\$40.00

JESD 24-10 ADDENDUM No. 10 to JESD24 - TEST METHOD FOR MEASUREMENT OF REVERSE RECOVERY TIME t_{rr} FOR POWER MOSFET DRAIN-SOURCE DIODES: Test method to measure the reverse recovery characteristics of the drain source diode of a power MOSFET.

August 1994; Reaffirmed October 2002 April 1999 /JC-25 Committee

\$41.00

JESD 24-11 ADDENDUM No. 11 to JESD24 - POWER MOSFET EQUIVALENT SERIES GATE RESISTANCE TEST METHOD: Test method to measure the equivalent resistance of the gate to source of a power MOSFET.

August 1996; Reaffirmed March 2001, October 2002 March 2001 /JC-25 Committee

\$38.00

JESD 24-12 Thermal Impedance Measurement for Insulated Gate Bipolar Transistors - (Delta $V_{CE(on)}$ Method) The purpose of this test method is to measure the thermal impedance of the IGBT (Insulated Gate Bipolar Transistor) under the specified conditions of applied voltage, current and pulse duration. The temperature sensitivity of the collector-emitter on voltage, $V_{CE(on)}$, is used as the junction temperature indicator. This is an alternative method to JEDEC Standard No. 24-6.

June 2004 September 2002 /JC-25 Committee

\$45.00

JESD 25 MEASUREMENT OF SMALL-SIGNAL TRANSISTOR SCATTERING PARAMETERS: This standard provides a test method and definition for small-signal conditions at microwave frequencies.

November 1972; Reaffirmed September 1981, April 2000, October 2002 /JC-25 Committee

\$57.00

JESD 26-A	GENERAL SPECIFICATION FOR PLASTIC ENCAPSULATED MICROCIRCUITS FOR USE IN RUGGED APPLICATIONS - RESCINDED, July 2001 April 1990; Rescinded July 2001 /JC-13.2 Subcommittee	
JESD 27	CERAMIC PACKAGE SPECIFICATION FOR MICROELECTRONIC PACKAGES: The intent of this standard is to be a guide in the manufacture and procurement of ceramic packages, especially for the hybrid industry. Manufacturers or ceramic packages and procuring activities for these packages will now be able to use this document as the means for agreement in the imposition of minimum requirements in qualification, screening, and quality conformance. August 1993; Under Revision , will be merged with JESD9-A /JC-13.5 Subcommittee	\$67.00
JESD 28-1	N-CHANNEL MOSFET HOT CARRIER DATA ANALYSIS: This addendum provides data analysis examples useful in analyzing MOSFET n-channel hot-carrier-induced degradation data. This addendum to JESD28 (Hot carrier n-channel testing standard) suggests hot-carrier data analysis techniques. September 2001 /JC-14.2 Subcommittee	\$43.00
JESD 28-A	A PROCEDURE FOR MEASURING N-CHANNEL MOSFET HOT-CARRIER-INDUCED DEGRADATION UNDER DC STRESS: This document describes an accelerated test for measuring the hot-carrier-induced degradation of a single n-channel MOSFET using dc bias. The purpose of this document is to specify a minimum set of measurements so that valid comparisons can be made between different technologies, IC processes, and process variations in a simple, consistent and controlled way. The measurements specified should be viewed as a starting point in the characterization and benchmarking of the transistor manufacturing process. December 2001 /JC-14.2 Subcommittee	\$47.00
JESD 29-A	FAILURE-MECHANISM-DRIVEN RELIABILITY MONITORING - SUPERSEDED BY EIA/ANSI-659, July 1996. July 1996; Superseded July 1996 /JC-14.3 Subcommittee	
JESD 30C	DESCRIPTIVE DESIGNATION SYSTEM FOR SEMICONDUCTOR-DEVICE PACKAGES: This standard describes a systematic method for generating universal descriptive designators for semiconductor-device packages. The descriptive designator is intended to provide a useful communication tool but has no implied control for assuring package interchangeability. September 2003 January 2001 /JC-11 Committee	\$55.00

JESD 31C	GENERAL REQUIREMENTS FOR DISTRIBUTORS OF COMMERCIAL AND MILITARY SEMICONDUCTOR DEVICES: This publication identifies the general requirements for Distributors that supply Commercial and Military products. This document identifies the general requirements for Distributors that supply Commercial and Military products. Now updated to provide clarification, these requirements apply to all discrete semiconductors, integrated circuits and hybrids, whether packaged or in wafer/die form, manufactured by all component Manufacturers. This revision was incorporated to better define the requirements for the handling of moisture-sensitive devices in distribution. The addition of IPC/JEDEC J-STD-020 and IPC/JEDEC J-STD-033 ensure consistent requirements throughout the distribution channel. September 2003 January 2003 /JC-14.4 Subcommittee	\$52.00
JESD 32	STANDARD FOR CHAIN DESCRIPTION FILE: This document provides a standard for describing an ISP device chain, opening up the possibility for third-party companies to provide value-added ISP software. The purpose of the Chain Description File is to describe the configuration of a programming chain made up of devices that can be connected in some serial fashion. No assumptions are made about how data is used by the device, nor about the nature or configuration of the control signals that affect programming. It will support devices configured using electrically-erasable(EE), Flash, SRAM, or any other reconfigurable cell. For devices programmed via an IEEE programmable devices in the same chain. June 1996 / Committee!33JC421	\$47.00
JESD 33-B	STANDARD METHOD FOR MEASURING AND USING THE TEMPERATURE COEFFICIENT OF RESISTANCE TO DETERMINE THE TEMPERATURE OF A METALLIZATION LINE: This newly revised test method provides a procedure for measuring the temperature coefficient of resistance, TCR(T), of thin-film metallizations used in microelectronic circuits and devices. Procedures are also provided to use the TCR(T) to determine the temperature of a metallization line under Joule-heating conditions and to determine the ambient temperature where the metallization line is used as a temperature sensor. Originally, the method was intended only for aluminum-based metallizations and for other metallizations that satisfy the linear dependence and stability stipulations of the method. The method has been revised to make it explicitly applicable to copper-based metallizations, as well, and at temperatures beyond where the resistivity of copper is no longer linearly dependent on temperature (beyond approximately 200 ½C). Using the TCR(T) measured for copper in the linear-dependent region, a factor is used to correct the calculated temperature at these higher temperatures. February 2004 April 2003 /JC-14.2 Subcommittee	\$61.00

JESD 34	FAILURE-MECHANISM-DRIVEN RELIABILITY QUALIFICATION OF SILICON DEVICES: This document applies to the reliability qualification of new or changed silicon devices, and their materials or manufacturing processes. Does not address qualification of product quality or functionality. Provides an alternative to traditional stress-driven qualification. March 1993 /JC-14.2 Subcommittee	\$43.00
JESD 35-1	ADDENDUM No. 1 to JESD35 - GENERAL GUIDELINES FOR DESIGNING TEST STRUCTURES FOR THE WAFER-LEVEL TESTING OF THIN DIELECTRICS: This addendum expands the usefulness of the Standard 35 (JESD35) by detailing the various sources of measurement error that could effect the test results obtained by the ramped tests described in JESD35. Each source of error is described and its implications on test structure design is noted. This addendum can be used as a guide when designing test structures for the qualification and characterization of thin oxide reliability, specifically, by implementing accelerated voltage or current ramp tests. September 1995 /JC-14.2 Subcommittee	\$52.00
JESD 35-2	ADDENDUM No. 2 to JESD35 - TEST CRITERIA FOR THE WAFER-LEVEL TESTING OF THIN DIELECTRICS: This addendum includes test criteria to supplement JESD35. JESD35 describes procedures developed for estimating the overall integrity of thin oxides in the MOS Integrated Circuit manufacturing industry. Two test procedures are included in JESD35: a Voltage-Ramp (V-Ramp) and a Current-Ramp (J-Ramp). As JESD35 became implemented into production facilities on a variety of test structures and oxide attributes, a need arose to clarify end point determination and point out some of the obstacles that could be overcome by careful characterization of the equipment and test structures. February 1996 /JC-14.2 Subcommittee	\$43.00
JESD 35-A	PROCEDURE FOR WAFER-LEVEL-TESTING OF THIN DIELECTRICS: The revised JESD35 is intended for use in the MOS Integrated Circuit manufacturing industry. It describes procedures developed for estimating the overall integrity and reliability of thin gate oxides. Three basic test procedures are described, the Voltage-Ramp (V-Ramp), the Current-Ramp (J-Ramp) and the new Constant Current (Bounded J-Ramp) test. Each test is designed for simplicity, speed and ease of use. The standard has been updated to include breakdown criteria that are more robust in detecting breakdown in thinner gate oxides that may not experience hard thermal breakdown. April 2001 /JC-14.2 Subcommittee	\$67.00
JESD 36	STANDARD DESCRIPTION OF LOW-VOLTAGE TTL-COMPATIBLE, 5 V TOLERANT CMOS LOGIC DEVICES: This standard outlines the	

standard dc specifications, test conditions, and test loading for logic products that are designed to tolerate input and output voltages which exceed the device's power supply. More specifically this standardizes 5 V - tolerant logic products that run from 'low voltage' (2.7 V to 3.6 V) power supplies. Products that meet this standard can be used to effectively interface between LVCMOS/LVTTL and 5 V TTL buses, bridging the gap between low-voltage and 5 V TTL busses.

June 1996 /JC-40 Committee

\$45.00

JESD 37

STANDARD LOGNORMAL ANALYSIS OF UNCENSORED DATA, AND OF SINGLY RIGHT -CENSORED DATA UTILIZING THE PERSSON AND ROOTZEN METHOD: This standard details techniques for estimating the values of a two parameter lognormal distribution from complete lifetime data (all samples in an experiment have failed) or singly right-censored lifetime data (the experiment have failed) or singly right-censored lifetime data gathered from rapid stress test; however, not all types of failure data can be analyzed with these techniques.

October 1992 /JC-14.2 Subcommittee

\$59.00

JESD 38

STANDARD FOR FAILURE ANALYSIS REPORT FORMAT: This standard is to promote unification of content and format of semiconductor device failure-analysis reports so that reports from diverse laboratories may be easily read, compared, and understood by customers. Additional objectives are to ensure that reports can be easily ready by users, satisfactorily reproduced on copying machines, adequately transmitted by telefax, and conveniently stored in standard filing cabinets.

December 1995 /JC-14.6 Subcommittee

\$43.00

JESD 39-A

QUALITY SYSTEM ASSESSMENT - SUPERSEDED BY ANSI/EIA-670, June 1997.

June 1997; Superseded /JC-14.4 Subcommittee

JESD 40

PROCUREMENT QUALITY OF SOLID STATE COMPONENTS BY GOVERNMENT CONTRACTORS - SUPERSEDED BY EIA-623, July 1994

July 1994 /JC-13 Committee

JESD 41

REVERSE RECOVERY CHARACTERISTICS OF SILICON DIODES: Rescinded June 2002.

May 1995; Rescinded June 2002 /JC-22.1 Subcommittee

JESD 42

REQUIREMENTS FOR HANDLING ELECTROSTATIC-DISCHARGE-SENSITIVE (ESDS) DEVICES - SUPERSEDED BY EIA-625, November 1994.

March 1994; Superseded /JC-13 Committee

JESD 43	COMPONENT PROBLEM ANALYSIS AND CORRECTIVE ACTION REQUIREMENTS - SUPERSEDED BY EIA-671, November 1996. November 1996; Superseded /JC-14.4 Subcommittee	
JESD 45	MEASUREMENT METHOD FOR THERMAL RESISTANCE OF BRIDGE RECTIFIER ASSEMBLIES: Rescinded June 2002. Replaced by JESD282-B. December 1994; Rescinded June 2002 /JC-22.2 Subcommittee	
JESD 46-B	CUSTOMER NOTIFICATION OF PRODUCT/PROCESS CHANGES BY SEMICONDUCTOR SUPPLIERS: This standard establishes procedures to notify customers of semiconductor product and process changes. Requirements include: documentation; procedures for classification, notification and customer response; content; and records. Documentation of a suppliers change notification system should set clear and understandable expectations for both the originators of the change and their end customers. August 2001 /JC-14.4 Subcommittee	\$38.00
JESD 47B	STRESS-TEST-DRIVEN QUALIFICATION OF INTEGRATED CIRCUITS: This standard contains a set of most frequently encountered and accepted reliability stress tests. These tests are used for qualifying new and changed technology/process/ product families as well as individual products. These reliability stress tests have been found capable of stimulating and precipitating semiconductor device failures, in an accelerated manner. This document does not relieve the supplier of the responsibility to meet internal qualification programs. NOTE The headers in this document wer corrected on 9/23/03, if you printed the document prior to this date please discard. August 2003 January 2003 /JC-14.3 Subcommittee	\$55.00
JESD 48-A	PRODUCT DISCONTINUANCE: This standard establishes the requirements for timely customer notification of planned productdiscontinuance, which will assist customers in managing end-of-life supply, or to transition on-goingrequirements to alternate products. August 2001 /JC-14.4 Subcommittee	\$37.00
JESD 49	PROCUREMENT STANDARD FOR KNOWN GOOD DIE (KGD): This standard was created to facilitate the procurement and use of high reliability semiconductor microcircuits or discrete devices provided in bare die form, commonly known as Known Good Die (KGD). February 1996 /JC-13 Committee	\$45.00
JESD 50	SPECIAL REQUIREMENTS FOR MAVERICK PRODUCT ELIMINATION: This standard applies to the identification and control of Maverick Product that can occur during fabrication, assembly, packaging, or	

test of any electronic component. It can be implemented for an entire product line or to segregate product that has a higher probability of adversely impacting quality or reliability.

December 1995 /JC-14.3 Subcommittee

\$40.00

JESD 51 METHODOLOGY FOR THE THERMAL MEASUREMENT OF COMPONENT PACKAGES (SINGLE SEMICONDUCTOR DEVICE) This standard and its subsequent addendum's, provides a standard for thermal measurement that, if followed fully, will provide correct and meaningful data that will allow for determination of junction temperature for specific conditions. The data can be used for package design evaluation, device characterization and reliability predictions.

December 1995 /JC-15.1 Subcommittee

\$40.00

JESD 51- 1 INTEGRATED CIRCUIT THERMAL MEASUREMENT METHOD - ELECTRICAL TEST METHOD (SINGLE SEMICONDUCTOR DEVICE) : The purpose of this test method is to define a standard Electrical Test Method (ETM) that can be used to determine the thermal characteristics of single integrated circuit devices housed in some form of electrical package. This method will provide a basis for comparison of different devices housed in the same electronic package or similar devices housed in different electronic packages.

December 1995 /JC-15 Committee

\$61.00

JESD 51- 2 INTEGRATED CIRCUITS THERMAL TEST METHOD ENVIRONMENTAL CONDITIONS - NATURAL CONVECTION (STILL AIR) : This document outlines the environmental conditions necessary to ensure accuracy and repeatability for a standard junction-to-ambient thermal resistance measurement in natural convection.

December 1995 /JC-15 Committee

\$47.00

JESD 51- 3 LOW EFFECTIVE THERMAL CONDUCTIVITY TEST BOARD FOR LEADED SURFACE MOUNT PACKAGES: This standard describes design requirements for a single layer, leaded surface mount integrated circuit package thermal test board. The standard describes board material and geometry requirements, minimum trace lengths, trace thickness, and routing considerations. Application includes still air and moving air thermal tests.

August 1996 /JC-15.1 Subcommittee

\$41.00

JESD 51- 4 THERMAL TEST CHIP GUIDELINE (WIRE BOND TYPE CHIP) : This guideline describes design requirements for wire bond type semiconductor chips to be used for thermal resistance listing of IC packages. This document provides specific guidelines for chip design but allows flexibility in the materials and layout requirements.

February 1997 /JC-15.1 Subcommittee

\$45.00

JESD 51- 5 EXTENSION OF THERMAL TEST BOARD STANDARDS FOR PACKAGES

WITH DIRECT THERMAL ATTACHMENT MECHANISMS: This extension of the thermal standards provides a standard fixture for direct attach type packages such as deep-downset of thermally tabbed packages. This specification provides additional design detail for use in developing thermal test boards with application to these package types. This document is in addition to and not replacement for the design specifications in other standards.

February 1999 /JC-15.1 Subcommittee

\$38.00

JESD 51- 6 INTEGRATED CIRCUIT THERMAL TEST METHOD ENVIRONMENTAL

CONDITIONS - FORCED CONVECTION (MOVING AIR): This standard specifies the environmental conditions for determining thermal performance of an integrated circuit device in a forced convection environment when mounted on a standard thermal test board.

March 1999 /JC-15.1 Subcommittee

\$38.00

JESD 51- 7 HIGH EFFECTIVE THERMAL CONDUCTIVITY TEST BOARD FOR LEADED

SURFACE MOUNT PACKAGES: This fixturing further defines the environment for thermal test of packaged microelectronic devices. Its function is to provide an alternate mounting surface for the analysis of heat flow in electronic components. The objective of the standard is to provide a high effective thermal conductivity mounting surface that can be compared equally against standard tests done in different laboratories with typical variations of less than or equal to 10%.

February 1999 /JC-15.1 Subcommittee

\$41.00

JESD 51- 8 INTEGRATED CIRCUIT THERMAL TEST METHOD ENVIRONMENTAL

CONDITIONS - JUNCTION-TO-BOARD: This specification should be used in conjunction with the overview document JESD51, Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device) [1] and the electrical test procedures described in JESD51-1, 'Integrated Circuit Thermal Measurement Method (Single Semiconductor Device)' [2]. The environmental conditions described in this document are specifically designed for testing of integrated circuit devices that are mounted on standard test boards with two internal copper planes [3]. This standard is not applicable to packages that have asymmetric heat flow paths to the printed board caused by such thermal enhancements as fused leads (leads connected to the die pad) or power style packages with the exposed heat slug on one side of the package.

October 1999 /JC-15.1 Subcommittee

\$45.00

JESD 51- 9 TEST BOARDS FOR AREA ARRAY SURFACE MOUNT PACKAGE THERMAL

MEASUREMENTS: This standard covers the design of printed circuit boards (PCBs) used in the thermal characterization of ball grid array (BGA) and land grid array (LGA) packages. It is intended to

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be used in conjunction with the JESD51 series of standards that cover the test methods and test environments. JESD51-9 was developed to give a figure-of-merit of thermal performance that allows for accurate comparisons of packages from different suppliers. It can be used to give a first order approximation of system performance and, in conjunction with the other JESD51 PCB standards, allows for comparisons of the various package families.

July 2000 /JC-15.1 Subcommittee

\$48.00

JESD 51-10 TEST BOARDS FOR THROUGH-HOLE PERIMETER LEADED PACKAGE

THERMAL MEASUREMENTS: This standard covers the design of printed circuit boards (PCBs) used in the thermal characterization of Dual-Inline Packages (DIP) and Single-Inline Packages (SIP). It is intended to be used in conjunction with the JESD51 series of standards that cover the test methods and test environments. JESD51-10 was developed to give a figure-of-merit of thermal performance that allows for accurate comparisons of packages from different suppliers. It can be used to give a first order approximation of system performance and, in conjunction with the other JESD51 PCB standards, allows for comparisons of the various package families.

July 2000 /JC-15.1 Subcommittee

\$45.00

JESD 51-11 TEST BOARDS FOR THROUGH-HOLE AREA ARRAY LEADED PACKAGE

THERMAL MEASUREMENT: This standard covers the design of printed circuit boards (PCBs) used in the thermal characterization of Pin Grid Array (PGA) packages. It is intended to be used in conjunction with the JESD51 series of standards that cover the test methods and test environments. JESD51-11 was developed to give a figure-of-merit of thermal performance that allows for accurate comparisons of packages from different suppliers. It can be used to give a first order approximation of system performance and, in conjunction with the other JESD51 PCB standards, allows for comparisons of the various package families.

June 2001 /JC-15.1 Subcommittee

\$47.00

JESD 52 STANDARD FOR DESCRIPTION OF LOW VOLTAGE TTL-COMPATIBLE

CMOS LOGIC DEVICES: This standard describes dc interface specifications and test environment for these devices that operate with 2.7 V to 3.6 V power supplies. The goal is to provide a consistent set of dc specifications for reference by logic suppliers and users alike.

November 1995 /JC-40 Committee

\$45.00

JESD 53 MANAGEMENT OF COMPONENT OBSOLESCENCE BY GOVERNMENT CONTRACTORS: Rescinded, October 2002

January 1996; Rescinded October 2002 /JC-13.2 Subcommittee

JESD 54	STANDARD FOR DESCRIPTION OF 54/74ABTXXX AND 74BCXXX TTL-COMPATIBLE BiCMOS LOGIC DEVICES: The purpose is to provide a standard of BiCMOS Logic series specifications to provide for uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users. February 1996 /JC-40 Committee	\$61.00
JESD 55	STANDARD FOR DESCRIPTION OF LOW-VOLTAGE TTL-COMPATIBLE BiCMOS LOGIC DEVICES: The purpose is to provide a standard of BiCMOS Logic series specifications for uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users. May 1996 /JC-40 Committee	\$49.00
JESD 57	TEST PROCEDURE FOR THE MANAGEMENT OF SINGLE-EVENT EFFECTS IN SEMICONDUCTOR DEVICES FROM HEAVY ION IRRADIATION: This test method defines requirements and procedures for ground simulation and single event effects (SEE) and implementation of the method in testing integrated circuits. This standard is valid when using a cyclotron or Van de Graaff accelerator. Microcircuits under test must be delidded. The ions used at the facilities have an atomic number $Z > 2$. It does not apply to SEE testing that uses protons, neutrons, or other lighter particles. This standard is designed to eliminate any misunderstanding between users of the method and test facilities, to minimize delays, and to promote standardization of testing and test data. December 1996; Under Revision September 2003 /JC-13.4 Subcommittee	\$67.00
JESD 59	BOND WIRE MODELING STANDARD: This standard describes the modeling of a bond wire from an integrated circuit (IC) die to a package lead in a ball or wedge type wire bond configuration. June 1997 /JC-15 Committee	\$45.00
JESD 60	A PROCEDURE FOR MEASURING P-CHANNEL MOSFET HOT-CARRIER-INDUCED DEGRADATION AT MAXIMUM GATE CURRENT UNDER DC STRESS: This method establishes a standard procedure for accelerated testing of the hot-carrier-induced change of a p-channel MOSFET. The objective is to provide a minimum set of measurements so that accurate comparisons can be made. April 1997 /JC-14.2 Subcommittee	\$45.00
JESD 61	ISOTHERMAL ELECTROMIGRATION TEST PROCEDURE: This standard describes an algorithm for the execution of the isothermal test, using computer-controlled instrumentation. The primary use of this test is for the monitoring of microelectronic metallization lines at water level (1) in process development, to evaluate process options, (2) in manufacturing, to monitor metallization reliability	

and (3) to monitor/evaluate process equipment. While it is developed as a fast WLR test, it can also be an effective tool for controlling the uniformity of stress applied during the standard package level electromigration test.

April 1997 /JC-14.2 Subcommittee

\$49.00

JESD 62-A OUTLIER IDENTIFICATION AND MANAGEMENT SYSTEM FOR ELECTRONIC COMPONENTS: This revision incorporates recommended tests and an example of a statistics-based method for identifying and removing outliers, i.e., parts that meet supplier specifications and end-user requirements but lie outside typical distribution limits. Outlier product can occur during fabrication, assembly, packaging, or test of any electronic components.

May 2002 /JC-14.3 Subcommittee

\$45.00

JESD 63 STANDARD METHOD FOR CALCULATING THE ELECTROMIGRATION MODEL PARAMETERS FOR CURRENT DENSITY AND TEMPERATURE: This method provides procedures to calculate sample estimates and their confidence intervals for the electromigration model parameters of current density and temperature. The model parameter for current density is the exponent (n) to which the current density is raised in Black's equation. The parameter for temperature is the activation energy for the electromigration failure process.

February 1998 /JC-14.2 Subcommittee

\$61.00

JESD 64-A STANDARD FOR DESCRIPTION OF 2.5 V CMOS LOGIC DEVICES WITH 3.6 V CMOS TOLERANT INPUTS AND OUTPUTS: The purpose is to provide a standard for 2.5 V nominal supply voltage logic devices for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. This specification provides for compatibility between devices operating between either the Standard Range of 1.8 V to 2.7 V or the optional Extended Range of 1.65 V to 2.7 V supply voltages, as well as over-voltage tolerance with devices operating at 3.6 V.

October 2000 /JC-40 Committee

\$40.00

JESD 65B DEFINITION OF SKEW SPECIFICATIONS FOR STANDARD LOGIC DEVICES: This standard defines skew specifications and skew testing for standard logic devices. The purpose is to provide a standard for specifications to achieve uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users.

September 2003 /JC-40 Committee

\$48.00

JESD 66 TRANSIENT VOLTAGE SUPPRESSOR STANDARD FOR THYRISTOR SURGE PROTECTIVE DEVICE: This standard is applicable to Thyristor Surge Protective Devices. It describes terms and definitions and explains methods for verifying device ratings and measuring device

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characteristics. The intended users of this standard are those interested in Thyristor Surge Protective Device characterization and rating verification. These devices are used primarily by the telecommunications industry to protect circuits from harmful overvoltages. The Thyristor Surge Protective Device (TSPD) is a semiconductor device that is finding widespread application in the telecommunication industry. The intent of this stand is to provide information on test methods that will reduce the possibility of disagreement and misunderstanding between TSPD vendors and users, and facilitate the determination of device interchangeability.

November 1999 /JC-22.5 Subcommittee

\$91.00

JESD 67 I/O DRIVERS AND RECEIVERS WITH CONFIGURABLE COMMUNICATION VOLTAGE, IMPEDANCE, AND RECEIVER THRESHOLD: This standard attempts to aid in the design of electronic systems comprised of components that operate at several different supply voltages. This document covers respectively configurable I/O voltage, receiver type and switchpoint, and driver impedance.

February 1999 /JC-16 Committee

\$45.00

JESD 68.01 COMMON FLASH INTERFACE (CFI): The Common Flash Interface (CFI) specification outlines a device and host system software interrogation handshake that allows specific software algorithms to be used for entire families of devices. This allows device-independent, JEDEC ID-independent, and forward- and backward-compatible software support for the specific flash families. It allows flash vendors to standardize their existing interfaces for long-term compatibility. The changes for this minor revision are indicated in Annex A on page 11.

September 2003 December 2002 /JC-42.4 Subcommittee

\$48.00

JESD 69 INFORMATION REQUIREMENTS FOR THE QUALIFICATION OF SILICON DEVICES: This standard establishes the information required by semiconductor users from IC manufacturers and distributors in order to judge whether a semiconductor component is fit for use in their particular application. It establishes a set of data elements that describes the component and defines what each element means. It does not define the quality and reliability requirements that the component must satisfy. This standard can be used in conjunction with other reliability qualification standards, such as JESD34 'Failure Mechanism-Driven Reliability Qualification of Silicon Devices' and JESD47 'Stress Test Driven Qualification of Integrated Circuits'.

April 2000 /JC-14.3 Subcommittee

\$40.00

JESD 70 2.5 V BiCMOS LOGIC DEVICE FAMILY SPECIFICATION WITH 5 V TOLERANT INPUTS AND OUTPUTS: The purpose is to provide a standard for 2.5 V nominal supply voltage logic devices, for uniformity, multiplicity of sources, elimination of confusion, ease of

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device specification, and ease of use, thus providing compatibility between devices operating between 2.3 V and 2.7 V supply voltages, as well as overvoltage tolerance with devices operating at 3.3 V, or 5 V.

June 1999 /JC-40 Committee

\$41.00

JESD 71

STANDARD TEST AND PROGRAMMING LANGUAGE (STAPL): STAPL is a vendor- and platform-independent language for programming and testing devices via the IEEE standard 1149.1 interface, commonly known as JTAG. STAPL enables programming of designs into programmable logic devices (PLDs) offered by a variety of PLD vendors. STAPL is also suitable for testing 1149.1-compliant devices.

August 1999 / Committee!33JC421

\$67.00

JESD 72

TEST METHODS AND ACCEPTANCE PROCEDURES FOR THE EVALUATION OF POLYMERIC MATERIALS: This Test Method covers the minimum requirements that should be in effect for the evaluation and acceptance of polymeric materials for use in industrial, military, space, and other special-condition products which may require capabilities beyond standard commercial microelectronics applications. It is not the intent of this Publication to specify a material, but to evaluate the material to assure that the quality and reliability of the microelectronic devices are not compromised. This document replaces JEP105, JEP107 and JEP112.

June 2001 January 2001 /JC-13.5 Subcommittee

\$52.00

JESD 73

DESCRIPTION OF 5 V BUS SWITCH WITH TTL-COMPATIBLE CONTROL INPUTS: This standard covers specifications for a family of 5 V NMOS FET bus switch devices with 5 V TTL compatible control inputs. Not included in this document are device-specific parameters and performance levels that the vendor must also apply for full device description.

June 1999 /JC-40 Committee

\$40.00

JESD 73-1

STANDARD FOR DESCRIPTION OF 3.3 V NFET BUS SWITCH DEVICES: This standard covers specifications for a family of 3.3 V NMOS FET bus switch devices. Not included in this document are device specific parameters and performance levels that the vendor must also supply for full device description. The purpose of this document is to provide a set of uniform data sheet parameters for the description of bus switch devices. This standard includes required parameters, test conditions, test levels, and measurement methods for data sheet descriptions of bus switch devices.

August 2001 /JC-40 Committee

\$40.00

JESD 73-2

STANDARD FOR DESCRIPTION OF 3.3 V NFET BUS SWITCH DEVICES WITH INTEGRATED CHARGE PUMPS: This standard covers

specifications for a family of 3.3 V NMOS FET bus switch devices with integrated charge pumps. Not included in this document are device specific parameters and performance levels that the vendor must also supply for full device description. The purpose of this standard is to provide a set of uniform data sheet parameters for the description of bus switch devices. This standard includes required parameters, test conditions, test levels, and measurement methods for data sheet descriptions of bus switch devices.

August 2001 /JC-40 Committee

\$40.00

JESD 73-3 STANDARD FOR DESCRIPTION OF 3867 - 2.5 V, SINGLE 10-BIT, 2-PORT, DDR FET SWITCH: This standard provides a set of uniform data sheet parameters for the description of a single 10-bit, 2.5 V FET transmission-gate bus switch device for DDR memory module and motherboard applications. This bus switch device has a low ON resistance allowing inputs to be connected directly to outputs, with near zero propagation delay.

November 2001 / Committee!33JC402

\$40.00

JESD 73-4 STANDARD FOR DESCRIPTION OF 3877 - 2.5 V, DUAL 5-BIT, 2-PORT, DDR FET SWITCH: This standard provides a set of uniform data sheet parameters for the description of a dual 5-bit, 2.5 V FET transmission-gate bus switch device for DDR memory module and motherboard applications. This bus switch device has a low ON resistance allowing inputs to be connected directly to outputs, with near zero propagation delay.

November 2001 / Committee!33JC402

\$40.00

JESD 74 EARLY LIFE FAILURE RATE CALCULATION PROCEDURE FOR ELECTRONIC COMPONENTS: This new standard defines a procedure for calculating the point estimate of the time-dependent failure rate of electronic components from early life failure rate (ELFR) reliability test data. Calculation techniques are developed for constant failure rate and decreasing failure rate distributions. Projections can be used to compare reliability performance with objectives, provide line feedback, support service cost estimates, and set product test and reliability screen strategies.

April 2000 /JC-14.3 Subcommittee

\$43.00

JESD 75 BALL GRID ARRAY PINOUTS STANDARDIZED FOR 32-BIT LOGIC FUNCTIONS: The purpose of this standard is to provide a pinout standard for dual-die 32-bit logic devices offered in a 96- and 144-ball grid array package for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease use. This standard defines device output for 32-bit wide buffer, driver and transceiver functions. This pinout specifically applies to the conversion of DIP-packaged 16-bit logic devices to LFBGA-packaged dual-die 32-bit logic devices.

November 1999 /JC-40 Committee

\$38.00

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JESD 75-1	BALL GRID ARRAY PINOUTS STANDARDIZED FOR 16, 18, AND 20-BIT LOGIC FUNCTIONS USING A 54 BALL PACKAGE: This standard establishes a 54 Ball Grid Array pinout for 16, 18 and 20-bit standard logic devices that are currently being produced in 48 and 56 Pin SSOP and TSSOP packages. The 54 Ball Grid Array Package is organized as a 6 x 9 array with balls on a .8mm x .8mm grid pitch. October 2001 /JC-40 Committee	\$38.00
JESD 75-2	BALL GRID ARRAY PINOUTS STANDARDIZED FOR 16-BIT LOGIC FUNCTIONS: This standard provides a pinout standard for 16-bit wide logic devices offered in a 56-ball areagrid array package to provide for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. July 2001 /JC-40 Committee	\$38.00
JESD 75-3	BALL GRID ARRAY PINOUTS STANDARDIZED FOR 8-BIT LOGIC FUNCTIONS: This standard provides a pinout standard for 8-bit logic devices offered in a 20-ball area gridarray package to provide for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. July 2001 /JC-40 Committee	\$37.00
JESD 75-4	Ball Grid Array Pinout for 1-, 2-, and 3-Bit Logic Functions This standard defines device pinout for 1-, 2- and 3-bit wide logic functions. This pinout specifically applies to the conversion of Dual-Inline-Packaged (DIP) 1-, 2- and 3-bit logic devices to DSBGA-packaged 1-, 2- and 3-bit logic devices. March 2004 June 2003 /JC-40 Committee	\$41.00
JESD 75-5	SON/QFN PACKAGE PINOUTS STANDARDIZED FOR 1-, 2-, AND 3-BIT LOGIC FUNCTIONS This standard defines device pinout for 1-, 2- and 3-bit wide logic functions. This pinout specifically applies to the conversion of Dual-Inline-Packaged (DIP) 1-, 2- and 3-bit logic devices to SON/QFN packaged 1-, 2- and 3-bit logic devices. The purpose of this document is to provide a pinout standard for 1-, 2- and 3-bit logic devices offered in 5-, 6- or 8-land SON/QFN packages for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. July 2004 December 2003 /JC-40.1 Subcommittee	\$41.00
JESD 76	DESCRIPTION OF 1.8 V CMOS LOGIC DEVICES: This standard continues the voltage specification migration to the next level beyond the 2.5 V specification already established in JESD80. In this standard, the input and output conditions are described for CMOS Logic products in a 1.8 V (Normal Range) application. April 2000 /JC-40.1 Subcommittee	\$38.00

JESD 76-1	STANDARD DESCRIPTION OF 1.2 V CMOS LOGIC DEVICES (WIDE RANGE OPERATION): This standard defines dc interface, switching parameters and test loading for digital logic devices based on 1.2 V (nominal) power supply levels. The purpose is to provide a standard specification for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. June 2001 /JC-40 Committee	\$38.00
JESD 76-2	STANDARD DESCRIPTION OF 1.2 V CMOS LOGIC DEVICES (NORMAL RANGE OPERATION): This standard defines dc interface, switching parameters and test loading for digital logic devices based on 1.2 V (normal range) power supply levels. The purpose is to provide a standard specification for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. June 2001 /JC-40 Committee	\$38.00
JESD 76-3	STANDARD DESCRIPTION OF 1.5 V CMOS LOGIC DEVICES: This standard continues the voltage specification migration to the next level beyond the 1.8 V specification already established. The purpose is to provide a standard for 1.5 V nominal supply voltage CMOS logic devices, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. August 2001 /JC-40.1 Subcommittee	\$38.00
JESD 77B	TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR DISCRETE SEMICONDUCTOR AND OPTOELECTRONIC DEVICES: A revised and significantly expanded reference for technical writers and educators, manufacturers, buyers and users of discrete semiconductor and optoelectronic devices, is now available. Revision B of JEDEC Standard No. 77 includes extensive information on: letter symbol conventions; diodes and rectifiers (including signal, rectifier, microwave, tunnel and backward, voltage-regulator, voltage-reference, current regulator, and varactor diodes); transistors (including FETs, JFETs, and IGBTs); photosensitive devices, photoemitters, and optocouplers; thyristors and PUTs; and transient voltage suppressors. Terms and symbols, with their definitions, are arranged alphabetically by product type. Where applicable, graphical symbols are also included. February 2000 /JC-10 Committee	\$162.00
JESD 78	IC LATCH-UP TEST: This standard has been adopted by the Defense Logistics Agency (DLA) as project 5962-1880. This standard establishes a defined method for latch-up testing of ICs. It defines Classes and Levels for a device's latch-up capability so that both the user and supplier understand a device's latch-up	Samsung Electronics Co., Ltd. Ex. 1086, p. 34

capabilities. It is applicable to NMOS, CMOS, Bipolar, and all variations and combinations of these technologies. Latch-up is an extremely important factor in determining product reliability. This document contains the corrected figure 4 to include T6 on page 12, this change was made in January 1998.

March 1997 /JC-14.1 Subcommittee

\$48.00

JESD 79-2A DDR2 SDRAM SPECIFICATION This comprehensive standard defines all required aspects of 256Mb through 4Gb DDR2 SDRAMs with x4/x8/x16 data interfaces, including pinout, addressing, functional description, features, ac and dc parametrics, truth tables, and packages. Standard JESD79-2 uses a SSTL_18 interface, which is described in another JEDEC standard called JESD8-15. The purpose of this Standard is to define the minimum set of requirements for compliant devices 256Mb through 4Gb, x4/x8/x16 DDR2 SDRAMs. System designs based on the required aspects of this specification will be supported by all DDR2 SDRAM vendors providing compliant devices. Changes between versions is indicated in Annex A.

January 2004 /JC-42.3 Subcommittee

\$109.00

JESD 79D DOUBLE DATA RATE (DDR) SDRAM SPECIFICATION: This comprehensive standard defines all required aspects of 64Mb through 1Gb DDR SDRAMs with X4/X8/X16 data interfaces, including features, functionality, ac and dc parametrics, packages and pin assignments. This scope will subsequently be expanded to formally apply to x32 devices, and higher density devices as well. The purpose of this Standard is to define the minimum set of requirements for JEDEC compliant 64Mb through 1Gb, X4/X8/X16 DDR SDRAMs. System designs based on the required aspects of this specification will be supported by all DDR SDRAM vendors providing JEDEC compliant devices.

February 2004 / Committee!33JC423C

\$109.00

JESD 8-16 Bus Interconnect Logic (BIC) for 1.2 Volts This standard defines the electrical parameters for high-speed interfaces for use in the 1.2V electrical environment. Included in the standard are a single ended signaling interface suitable for parallel busses, and a differential signaling interface suitable for clock applications or parallel differential buses. JEDEC $\frac{1}{2}$ BIC $\frac{1}{2}$ Standard JESD8-16 continues the tradition of the JESD8-xx standards, defining electrical interfaces for the industry as new technologies and bus requirements develop. Previously, JEDEC defined standard JESD8-6, the $\frac{1}{2}$ HSTL $\frac{1}{2}$ standard, for use in 1.5V electrical environments. BIC is similar to HSTL, except the power supply voltage has dropped from 1.5V to 1.2V, and interface requirements are tightened to allow much higher speeds.

April 2004 December 2003 / Committee!33JC161

\$45.00

JESD 80	STANDARD FOR DESCRIPTION OF 2.5 V CMOS LOGIC DEVICES: The purpose of this standard is to provide a standard for 2.5 V nominal supply-voltage CMOS logic devices, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. This standard defines dc interface parameters and test loading for CMOS digital logic family based on 2.5 V (nominal) power supply levels at 2.5 V input tolerance. November 1999 /JC-40 Committee	\$38.00
JESD 82	DEFINITION OF CDCV857 PLL CLOCK DRIVER FOR REGISTERED DDR DIMM APPLICATIONS: This specification is a reference for Registered DDR DIMM designers. JESD82 defines the physical, electrical, interface and timing requirements of a 1:10 PLL clock driver for DDR Registered DIMMs from DDR200 to DDR266 as refined in revision C of JEDEC Standard 21-C (JESD21-C). JESD82 was also written to meet the future performance requirements of Registered DIMMs for DDR300 and DDR333. July 2000 /JC-40 Committee	\$47.00
JESD 82-1A	DEFINITION OF CVF857 PLL CLOCK DRIVER FOR REGISTERED PC1600, PC2100, AND PC2700 DIMM APPLICATIONS: This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of a CV857 PLL clock device for registered PC1600, PC2100 and PC2700 DIMM applications. The purpose is to provide a standard for a CV857 PLL clock device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. May 2004 /JC-40 Committee	\$52.00
JESD 82-2	STANDARD FOR DESCRIPTION OF A 3.3 V, 18-BIT, LVTTTL I/O REGISTER FOR PC133 REGISTERED DIMM APPLICATIONS: This standard defines the register support devices needed for standard height and low profile registered PC133 SDRAM DIMM modules. The objective of the standard is to clearly define the functionality, pinout and electrical characteristics required for this type of SDRAM module. July 2001 /JC-40 Committee	\$45.00
JESD 82-3A	DEFINITION OF THE SSTV16857 2.5 V, 14-BIT SSTL_2 REGISTERED BUFFER FOR DDR DIMM APPLICATIONS: This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTV16857 14-bit SSTL_2 registered buffer for DDR DIMM applications. The purpose is to provide a standard for the SSTV16857 logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. October 2002 /JC-40 Committee	\$43.00

JESD 82-4B STANDARD FOR DEFINITION OF THE SSTV16859 2.5 V, 13-BIT TO 26-BIT SSTL_2 REGISTERED BUFFER FOR STACKED DDR DIMM

APPLICATIONS: This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTV16859 13-bit to 26-bit SSTL_2 registered buffer for stacked DDR DIMM applications. The purpose is to provide a standard for the SSTV16859 logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

May 2003 /JC-40 Committee

\$47.00

JESD 82-5 STANDARD FOR DESCRIPTION OF A 3.3 V, ZERO DELAY CLOCK DISTRIBUTION DEVICE COMPLIANT WITH THE JESD21-C PC133 REGISTERED DIMM SPECIFICATION

This standard defines the PLL support devices required for standard height and low profile registered PC133 SDRAM DIMM modules. The objective of the standard is to clearly define the functionality, pinout and electrical characteristics of the PLL used on JEDEC standard modules. JESD82-5 is the latest specification to be added to the JESD82 family of specifications for memory module support devices. Additional specifications are currently under development for DDRII support devices.

July 2002 /JC-40 Committee

\$43.00

JESD 82-6 DEFINITION OF THE SSTV32852 2.5-V 24-BIT TO 48-BIT SSTL_2 REGISTERED BUFFER FOR 1U STACKED DDR DIMM APPLICATIONS:

This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTV32852 24-bit to 48-bit SSTL_2 registered buffer for stacked DDR DIMM applications. The purpose is to provide a standard for the SSTV32852 logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

November 2002 / Committee!33JC404

\$43.00

JESD 82-7 DEFINITION OF THE SSTU32864 1.8-V CONFIGURABLE REGISTERED BUFFER FOR DDR2 RDIMM APPLICATIONS:

This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTU32864 configurable registered buffer for DDR-II RDIMM applications. The purpose is to provide a standard for the SSTU32864 logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

November 2002 / Committee!33JC404

\$47.00

JESD 82-9 DEFINITION OF SSTU32865 REGISTERED BUFFER WITH PARITY FOR 2R x 4 DDR2 RDIMM APPLICATIONS

This standard provides the functional definition, ball-out configuration and package outline, signal definitions and input/output characteristics for a 28-bit 1:2

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registered driver with parity suitable for use on DDR2 RDIMMs. The SSTU32865 integrates the functional equivalent of two SSTU32864 devices (as defined in JESD82-7) into a single device, thereby easing layout and board design constraints especially on high density RDIMMs such as dual rank, by four configurations. Moreover, the optional use of a parity function is provided for, permitting detection and reporting of parity errors across its 22 data inputs. JESD82-9 specifies a 160-pin Thin-profile, fine-pitch ball-grid array (TFBGA) package.

September 2003 March 2003 / Committee!33JC404

\$49.00

JESD 85

METHODS FOR CALCULATING FAILURE RATES IN UNITS OF FITS:

This standard establishes methods for calculating failure rates in units of FITs by using data in varying degrees of detail such that results can be obtained from almost any data set. The objective is to provide a reference to the way failure rates are calculated.

July 2001 /JC-14.3 Subcommittee

\$55.00

JESD 86

ELECTRICAL PARAMETERS ASSESSMENT: This standard is intended to describe various methods for obtaining electrical variate data on devices currently produced on the manufacturing and testing process to be qualified. The intent is to assess the device's capability to function within the specification parameters over time and the application environment (operating range of temperature, voltage, humidity, input/output levels, noise, power supply stability etc.).

August 2001 /JC-14.3 Subcommittee

\$38.00

JESD 87

STANDARD TEST STRUCTURE FOR RELIABILITY ASSESSMENT OF AlCu METALLIZATIONS WITH BARRIER MATERIALS

This document describes design of test structures needed to assess the reliability of aluminum-copper, refractory metal barrier interconnect systems. This includes any metal interconnect system where a refractory metal barrier or other barrier material prevents the flow of aluminum and/or copper metal ions from moving between interconnect layers. This document is not intended to show design of test structures to assess aluminum or aluminum-copper alloy systems, without barriers to Al and Cu ion movement, nor for Cu only metal systems. Some total interconnect systems might not include barrier materials on all metal layers. The structures in this standard are designed for cases where a barrier material separates two Al or Al alloy metal layers. The purpose of this document is to describe the design of test structures needed to assess electromigration (EM) and stress-induced-void (SIV) reliability of AlCu barrier metal systems.

July 2001 /JC-14.2 Subcommittee

\$43.00

JESD 88

DICTIONARY OF TERMS FOR SOLID STATE TECHNOLOGY, First Edition:

This reference for technical writers and educators,

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manufacturers, and buyers and users of discrete solid state devices is now available. It should aid the technical committees of JEDEC in the avoidance of multiple definitions and reduce the proliferation of redundant definitions. The long-term goal is to include definitions from all JEDEC publications and standards. Even in this first edition, that goal has been largely met. Each of the approximately two thousand entries is referenced to its source publication, and an annex listing the names of the source publications and their releases dates is included. All entries were reviewed for punctuation, grammar, and clarity, as well as accuracy, and reworded if such was considered warranted. The purpose of this dictionary is to promote the uniform use of terms, definitions, abbreviations, and symbols throughout the solid state industry.

September 2001 /JC-10 Committee

\$50.00

JESD 89

MEASUREMENT AND REPORTING OF ALPHA PARTICLE AND TERRESTRIAL COSMIC RAY INDUCED SOFT ERRORS IN SEMICONDUCTOR DEVICES:

This specification defines the standard requirements and procedures for terrestrial soft-error-rate (SER) testing of integrated circuits and reporting of results. Both real-time (unaccelerated) and accelerated testing procedures are described. At terrestrial, Earth-based altitudes, the predominant sources of radiation include both cosmic-ray radiation and alpha-particle radiation from radioisotopic impurities in the package and chip materials. An overall assessment of a device's SER is complete, only when an unaccelerated test is done, or accelerated SER data for the alpha-particle component and the cosmic-radiation component has been obtained.

August 2001 /JC-13.4 Subcommittee

\$83.00

JESD 89-1

System Soft Error Rate (SSER) Test Method This method describes a standard procedure for collecting life test data with respect to soft errors. JESD89-1 is published as an addendum to the existing overall technical content of JESD89. JESD89-1 provides a concise procedure for those in need of collecting system soft error test data for comparative purposes.

June 2004 September 2003 /JC-14.1 Subcommittee

\$41.00

JESD 91-A

METHOD FOR DEVELOPING ACCELERATION MODELS FOR ELECTRONIC COMPONENT FAILURE MECHANISMS:

The method described in this document applies to all reliability mechanisms associated with electronic components. The purpose of this standard is to provide a reference for developing acceleration models for defect-related and wear-out mechanisms in electronic components.

August 2003 /JC-14.3 Subcommittee

\$49.00

JESD 92

PROCEDURE FOR CHARACTERIZING TIME-DEPENDENT DIELECTRIC BREAKDOWN OF ULTRA-THIN GATE DIELECTRICS: This document defines a constant voltage stress test procedure for characterizing

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time-dependent dielectric breakdown or $\frac{1}{2}$ wear-out $\frac{1}{2}$ of thin gate dielectrics used in integrated circuit technologies. The test is designed to obtain voltage and temperature acceleration parameters required to estimate oxide life at use conditions. The test procedure includes sophisticated techniques to detect breakdown in ultra-thin films that typically exhibit large tunneling currents and soft or noisy breakdown characteristics. This document includes an annex that discusses test structure design, methods to determine the oxide electric field in ultra-thin films, statistical models, extrapolation models, and example failure-rate calculations.

August 2003 July 2002 /JC-14.2 Subcommittee

\$57.00

JESD 94

APPLICATION SPECIFIC QUALIFICATION USING KNOWLEDGE BASED

TEST METHODOLOGY: The method described in this document applies to all application specific reliability testing for solid state components with known failure mechanisms where the test duration and conditions vary based on application variables. This document does not cover reliability tests that are characterization based or essentially go / no-go type tests, for example, ESD, latch-up, or electrical over stress. Also, it does not attempt to cover every failure mechanism or test environment, but does provide a methodology that can be extended to other failure mechanisms and test environments.

January 2004 June 2003 /JC-14.3 Subcommittee

\$49.00

JESD 96

Radio Front End - Baseband (RF-BB) Interface

The normative information in this standard is intended to provide a technical design team to construct the interface on a FED and a BED such that they will operate correctly with each other (at the interface level), when designed to this specification. Additional informative information is provided in the appendices to help illustrate the normative material. This document addresses the following interface topics: 1) RF-BB Electrical layer: time and amplitude specifications for lines, drivers, receivers, clocks; 2) RF-BB Link layer: bits, clock-data synchronization, power modes; 3) RF-BB Transport layer: data types, data framing, data bandwidth, connection to core IC; 4) RF-BB Interface Registers. This document defines a high-speed serial link that enables the bi-directional transfer of data and control information between the FED and BED. The document does not mandate the use of specific signaling, standard framing or standard messaging needed to make this an interoperable interface standard for RF devices or BB devices.

April 2004 November 2003 /JC-61 Committee

\$71.00

JESD 97

Marking, Symbols, and Labels for Identification of Lead (Pb) Free Assemblies, Components, and Devices

The Semiconductor Industry has been working toward providing Lead (Pb)-Free assemblies, components and devices for the past few years in low volume to meet specific market applications. The

Samsung Electronics Co., Ltd.

acceleration of the global transition to Pb-free electronics is driven by European Union's Restriction of Hazardous Substances (RoHS) legislation. Most electronic components and systems are required to be Pb-free by July 2006. The transition is occurring rapidly and numerous Pb-free solutions are in use at this time. Identification of the Pb-free materials used is critical for those performing assembly, rework, repair and recycling operations. The release of JESD97 makes available a standard method for marking and labeling of Pb-free components and assemblies that provides the critical information.

May 2004 June 2003 /JC-14.1 Subcommittee

\$45.00

JESD 99-1 ADDENDUM No. 1 to JESD99 - TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR ANALOG-TO-DIGITAL AND DIGITAL-TO-ANALOG CONVERTERS:

This addendum has now been incorporated into JESD99-A.

July 1989; Incorporated into JESD99-A, May 2000 /JC-10 Committee

JESD TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR

99A.01 MICROELECTRONIC DEVICES: This standard will be useful to users, manufacturers, educators, technical writers, and others interested in the characterization, nomenclature, and classification of microelectronics devices. There are general guidelines for both letter symbols and abbreviations applicable to all integrated circuits, and detailed sections for digital ICs, linear (analog) ICs, interface ICs (including D/A and A/D converters), voltage regulators, charge-transfer devices. The standard lists and defines more than 400 of the most common physical and electrical terms applicable to these devices and shows the industry-standard symbol and abbreviations that have been established for such terms. JESD99A.01 is the first minor revision of JESD99A, May 2000. Annex A briefly shows entries that have changed.

May 2003 /JC-10 Committee

\$127.00

JESD TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR

100B.01 MICROCOMPUTERS, MICROPROCESSORS, AND MEMORY INTEGRATED CIRCUITS: A revised reference for technical writers and educators, manufacturers, buyers and users of microprocessors, microcomputers, microcontrollers, memory ICs, and other complex devices. The terms and their definitions in this standard have been updated and are in general agreement with the latest publications of the IEEE and the IEC. The companion standard for other integrated circuits is JESD99A. Also included is a system for generating symbols for time intervals found in complex sequential circuits, including memories. JESD100B.01 is the first minor revision of JESD100-B, December 1999. Annex A briefly shows entries that have changed.

December 2002 /JC-10 Committee

\$71.00

JESD 22-A105C

POWER AND TEMPERATURE CYCLING: The power and temperature cycling test is performed to determine the ability of a device to withstand alternate exposures at high and low temperature extremes and simultaneously the operating biases are periodically applied and removed. It is intended to simulate worst case conditions encountered in application environments. The power and temperature cycling test is considered destructive and is only intended for device qualification. This test method applies to semiconductor devices that are subjected to temperature excursions and required to power on and off during all temperatures.

January 2004 June 2003 /JC-14.1 Subcommittee

\$40.00

JESD 22-B111

BOARD LEVEL DROP TEST METHOD OF COMPONENTS FOR HANDHELD ELECTRONIC PRODUCTS: This Board Level Drop Test Method is intended to evaluate and compare drop performance of surface mount electronic components for handheld electronic product applications in an accelerated test environment, where excessive flexure of a circuit board causes product failure. The purpose is to standardize the test board and test methodology to provide a reproducible assessment of the drop test performance of surface mounted components while duplicating the failure modes normally observed during product level test.

July 2003 /JC-14.1 Subcommittee

\$48.00

JESD 282B.01

SILICON RECTIFIER DIODES: This standard provided definitions, electrical characteristics circuit technology, letter symbols and registration format for diodes and stacks. It also covers rating and characteristics, manufacturing and performance as well as test practices to demonstrate the performance of semiconductor rectifier diodes and rectifier stacks used for the conversion and/or control of electric power. This version contains minor revisions to JESD282-B, April 2000.

November 2002 /JC-22.2 Subcommittee

\$177.00

JESD 284-A TEST METHODS FOR THE COLLECTOR-BASE TIME CONSTANT AND FOR THE RESISTIVE PART OF THE COMMON-EMITTER INPUT IMPEDANCE: The test methods described in this Standard are generally applicable to alloy-like devices for which the usual simplified equivalent circuits can be employed.

November 1963; Reaffirmed November 1963, June 1972, April 1981, April 1999, October 2002 /JC-25 Committee

\$38.00

JESD 286-B STANDARD FOR MEASURING FORWARD SWITCHING CHARACTERISTICS OF SEMICONDUCTOR DIODES: This method updates the standard procedure for characterizing the switching of signal or switching diodes when a step function of forward current is applied. The objective is to provide a standard so that accurate comparisons can be made.

JESD 307	VOLTAGE REGULATOR DIODE NOISE VOLTAGE MEASUREMENT: This standard is intended to cover the measurement of noise voltage in voltage regulator diodes in the reverse breakdown region. It describes noise voltage measurements at specified conditions, but may be used as a guide for making such measurements at other than specified conditions.(Formerly EIA-307) May 1965; Reaffirmed January 1992, April 1999, April 2002 April 2002 /JC-22.4 Subcommittee	\$38.00
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JESD 313-B	THERMAL RESISTANCE MEASUREMENTS OF CONDUCTION COOLED POWER TRANSISTORS: This standard provides a test method for measuring thermal resistance for conduction cooled power transistors. October 1975; Reaffirmed April 1981, March 2001 /JC-25 Committee	\$45.00
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JESD 320-A	CONDITIONS FOR MEASUREMENT OF DIODE STATIC PARAMETERS: This standard provides guidance for achieving equilibrium when measuring temperature sensitive static parameters of signal diodes. (Formerly EIA-302-A) December 1992; Reaffirmed April 1999, April 2002 (Original publication July 1965) /JC-22.4 Subcommittee	\$37.00
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JESD 381-A	METHOD OF DIODE Q MEASUREMENT: This standard was updated and revised for the purpose of clarifying the method used to measure Q of a Voltage-Variable-Capacitance Diode in the low VHF range using an RF admittance bridge. Originally published November 1981. Approved as ANSI/EIA-381-A-1992, July 1992. Became JESD381-A after ANSI expiration July 2002. November 1981; Reaffirmed April 1999, April 2002 April 1999 /JC-22.4 Subcommittee	\$48.00
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JESD 419-A	STANDARD LIST OF VALUES TO BE USED IN SEMICONDUCTOR DEVICE SPECIFICATIONS AND REGISTRATION FORMAT: This document contains standard lists of values which are recommended for use in semiconductor device specification and JEDEC Registration Formats. Good reasons should exist in those cases where values are used that are not included in these lists. October 1980; Reaffirmed March 2001 /JC-25 Committee	\$37.00
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JESD 482-A	LIST OF PREFERRED VALUES FOR USE ON VARIOUS TYPES OF SMALL SIGNAL AND REGULATOR DIODES: This standard specifies preferred values to be used on signal and regulator diodes. It will facilitate the standardization for nominal values used on small signal regulator diodes previously established in JEDEC Suggested Standard No. 2. (Formerly EIA-482-A)	
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August 1984; Reaffirmed April 1999, April 2002 April 2002 /JC-22.4 Subcommittee \$38.00

JESD 531 THERMAL RESISTANCE TEST METHOD FOR SIGNAL AND REGULATOR DIODES (FORWARD VOLTAGE, SWITCHING METHOD): This standard describes a test method for measuring the thermal resistance of signal and regulator diodes. The need for modification of this test method arose out of the limited description that existed earlier for both signal and regulator diode applications in testing for thermal resistance. Previously published as ID-13. ANSI/EIA-531-1986 (July) expired June 1996. Became JESD531 after reaffirmation April 2002.

July 1986; Reaffirmed April 1999, April 2002 April 1999 /JC-22.4 Subcommittee \$47.00

JESD 625-A REQUIREMENTS FOR HANDLING ELECTROSTATIC-DISCHARGE-SENSITIVE (ESDS) DEVICES: This standard establishes the minimum requirements for Electrostatic Discharge (ESD) control methods and materials used to protect electronic devices that are susceptible to damage or degradation from electrostatic discharge (ESD). The passage of a static charge through an electrostatic-discharge-sensitive (ESDS) device can result in catastrophic failure or performance degradation of the part. Device sensitivity to ESD is determined by test methods such as EIA/JESD22-A114. ESDS devices with human body model sensitivities of less than +200 volts may need additional protective measures beyond those specified in this standard.

December 1999 /JC-14.1 Subcommittee \$55.00

JESD 659-A FAILURE-MECHANISM-DRIVEN RELIABILITY MONITORING: This method establishes requirements for application of Statistical Reliability Monitoring 'SRM' technology to monitor and improve the reliability of electronic components and subassemblies. The standard also describes the condition under which a monitor may be replaced or eliminated.

September 1999 /JC-14.3 Subcommittee \$48.00

JESD 671-A COMPONENT QUALITY PROBLEM ANALYSIS AND CORRECTIVE ACTION REQUIREMENTS (INCLUDING ADMINISTRATIVE QUALITY PROBLEMS): This revision now encompasses administrative quality problems, in addition to the electrical and visual/mechanical quality problems that were addressed in the original release. A standard set of problem categories for each of these three types of component problems is presented for tracking and reporting purposes. A common set of customer and supplier expectations and requirements are set forth to help facilitate the successful problem analysis and corrective action of any type of component quality problem.

December 1999 /JC-14.4 Subcommittee \$43.00

JESD 82-8.01	STANDARD FOR DEFINITION OF $\pm 1/2$CU877 PLL CLOCK DRIVER FOR REGISTERED DDR2 DIMM APPLICATIONS This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of a $\pm 1/2$ CU877 PLL clock device for registered DDR2 DIMM applications. The purpose is to provide a standard for a $\pm 1/2$ CU877 PLL clock device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. This document includes minor editorial changes as noted in Annex A, page 16. February 2004 /JC-40 Committee	\$49.00
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NUMBER	Joint IPC/JEDEC Standards (J-STD-)	PRICE
J-STD-002B	SOLDERABILITY TESTS FOR COMPONENT LEADS, TERMINATIONS, LUGS, TERMINALS AND WIRES: At the request of IPC, J-STD-002B has been temporarily removed from the free download area until such time when it is revised to include lead-free. In its place, JEDEC's Test Method B102-D, Solderability, which includes lead-free, will be made available soon for free downloading. February 2003 Removed 01/21/04 /JC-14.1 Subcommittee	
J-STD-020C	JOINT IPC/JEDEC STANDARD FOR MOISTURE/REFLOW SENSITIVITY CLASSIFICATION FOR NONHERMETIC SOLID STATE SURFACE-MOUNT DEVICES: This document identifies the classification level of nonhermetic solid-state surface mount devices (SMDs) that are sensitive to moisture-induced stress. It is used to determine what classification level should be used for initial reliability qualification. Once identified, the SMDs can be properly packaged, stored and handled to avoid subsequent thermal and mechanical damage during the assembly solder reflow attachment and/or repair operation. This revision now covers components to be processed at higher temperatures for lead-free assembly. A hard cop version is available for \$20 each for IPC/JEDEC members and \$40 for nonmembers. July 2004 January 2004 /JC-14.1 Subcommittee	
J-STD-033A	JOINT IPC/JEDEC STANDARD FOR HANDLING, PACKING, SHIPPING AND USE OF MOISTURE/REFLOW SENSITIVE SURFACE-MOUNT DEVICES: This document provides SMD manufacturers and users with standardized methods for handling, packing, shipping and use of moisture/reflow sensitive SMDs. Now updated to support components that may need to be processed at higher temperatures, such as lead-free processes, these methods help avoid damage from moisture absorption and exposure to solder reflow temperatures that can result in yield and reliability degradation. IPC/JEDEC J-STD-033A helps achieve safe and damage-free reflow with the dry packing process and provides a minimum shelf life of 12 months from the seal date when using sealed dry bags. Hard copies of this document are available for \$20 each for IPC/JEDEC members and \$40 for nonmembers.	

July 2002 /JC-14.1 Subcommittee

J-STD- 035	JOINT IPC/JEDEC STANDARD FOR ACOUSTIC MICROSCOPY FOR NONHERMETRIC ENCAPSULATED ELECTRONIC COMPONENTS: This test method defines the procedures for performing acoustic microscopy on non-hermetic encapsulated electronic components. This method provides users with an acoustic microscopy process reflow for detecting defects non-destructively in plastic packages while achieving reproducibility. May 1999; Under Revision /JC-14.1 Subcommittee	\$35.00
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NUMBER	Joint Publication (JP)	PRICE
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JP 001.01	FOUNDRI PROCESS QUALIFICATION GUIDELINES (Wafer Fabrication Manufacturing Sites) This document provides a guideline for the minimum set of measurements to qualify a new semiconductor wafer process. It is written with particular reference to a generic silicon based CMOS logic technology. While it may be applicable to other technologies (e.g. analog CMOS, bipolar, BICMOS, GaAs, etc.), some sections apply specifically to CMOS. No effort was made in the present document to cover all the qualification requirements for specific other technologies, e.g. Cu/Low K interconnects or ultra thin gate oxide. This publication, is co-sponsored by JEDEC JC-14.2 and the FSA (Fabless Semiconductor Association). It originated at the FSA as a technology specific document, and has evolved into a generic set of qualification requirements. May 2004 /JC-14.2 Subcommittee	\$67.00
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NUMBER	JEDEC Publications (JEP)	PRICE
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JEP 64	SOLID STATE PRODUCTS REGISTRATION LIST (ORDER FROM TYPE ADMINISTRATION OFFICE): This publication includes addenda from 1976 to August 1986. The purpose of this list is to determine release numbers (file numbers) for JEDEC Type Designations. (See page 6 for more information.) September 1986; Reaffirmed November 2002 / Committee!33JCJEDC	\$162.00
JEP 65	TEST PROCEDURES FOR VERIFICATION OF MAXIMUM RATINGS OF POWER TRANSISTORS: This publication describes tests which are intended to represent the verification of maximum ratings for data sheets; they are not tests for performance or quality level. This material is to be used in conjunction with formats developed for device registration and defining data. December 1967; Reaffirmed September 1981, April 1999 /JC-25 Committee	\$52.00

JEP 69-B	PREFERRED LEAD CONFIGURATION FOR FIELD-EFFECT TRANSISTORS: This publication indicates preferred pinouts for FETs in various package designs. November 1973; Reaffirmed September 1981, April 1999 /JC-25 Committee	\$38.00
JEP 70-B	QUALITY AND RELIABILITY STANDARDS AND PUBLICATIONS: Contains a listing and description of commonly used quality and reliability related standards and publications that are applicable to the semiconductor industry. It is intended to be a reference aid in finding available standards and obtaining a copy from the source of the standard. It is not intended to recommend or imply the applicability of any standard for a specific purpose. This revision has been updated to include recent releases as well as revisions, in addition, URLs have been added to the October 1999 /JC-14.4 Subcommittee	\$57.00
JEP 74	STANDARD LIST OF VALUES TO BE USED IN POWER TRANSISTOR DEVICE REGISTRATION AND MINIMUM DIFFERENCES FOR DISCRETENESS OF REGISTRATIONS - SUPERSEDED BY EIA-419-A, February 1996. July 1969; Rescinded February 1996 /JC-25 Committee	\$38.00
JEP 75	LETTER SYMBOLS USED WITH INFRARED DEVICES - INCORPORATED INTO JESD77-A. August 1984; Rescinded August 1984 /JC-10 Committee	
JEP 78	RELATIVE SPECTRAL RESPONSE CURVES FOR SEMICONDUCTOR INFRARED DETECTORS: The intent of this publication is to facilitate the specification of infrared detector diodes, particularly in conjunction with the preparation of data for JEDEC type registration. October 1969 /JEDEC Committee	\$52.00
JEP 79	LIFE TEST METHODS FOR PHOTOCONDUCTIVE CELLS: This publication is for photoconductive cells sensitive primarily in the visible and near infrared region. September 1969	\$52.00
JEP 84A	RECOMMENDED PRACTICE FOR MEASUREMENT OF TRANSISTOR LEAD TEMPERATURE: This publication covers recommended methods for measurement of transistor lead temperatures under various load conditions. The techniques described are sufficiently accurate for most applications. June 2004 September 2002 /JC-25 Committee	\$41.00
JEP 86-A	RECOMMENDED PRACTICE FOR DUAL DIMENSIONING	

May 1976; Rescinded November 1999 /JC-11 Committee

JEP 87 FORWARD TURN-ON TIME MEASUREMENT ON SEMI-DIODES - INCORPORATED INTO EIA-282-A.

June 1992; Rescinded June 1985 /JC-22.2 Subcommittee

JEP 88 THERMAL RESISTANCE AND THERMAL IMPEDANCE TEST METHODS FOR STUD AND BASE-MOUNTED RECTIFIER DIODES AND THYRISTORS

January 1974; Rescinded June 1992 /JC-22.1 Subcommittee

JEP 90 THERMAL RESISTANCE FOR TEST METHODS FOR SIGNAL DIODES - SUPERSEDED BY EIA-531, July 1986. See JESD531, April 2002.

September 1983; Rescinded September 1986 /JC-22.4 Subcommittee

JEP 93 MICROELECTRONIC DEVICE TYPE ASSIGNMENTS

August 1975; Rescinded June 1992 June 1992 / Committee!33JCJEDC

JEP 95 JEDEC REGISTERED AND STANDARD OUTLINES FOR SOLID STATE AND RELATED PRODUCTS: This publication is a compilation of some 1800 pages of outline drawings for microelectronic packages including transistors, diodes, DIPs, chip carriers and package interface BGA outlines in both inch and metric versions.

January 2000 /JC-11 Committee

\$350.00

JEP 95 AUS ANNUAL UPDATING SERVICE: Subscription to this updating service is available from the JEDEC Office. New outlines are shipped to subscribers for insertion into the appropriate sections of Publication No. 95. JEP95 and Updating Service can be ordered through JEDEC at (703)907-7540 or ptanner@jedec.org.

January 2000 /JC-11 Committee

\$110.00

JEP 95-1 DESIGN REQUIREMENTS (Book 1, Section 4) Type 'section' in the 'by document number' to see the contents of this document. This is currently under construction. Once it has been completed you will be able to click on the 'entire document' icon below and see all the sections contained in this document.

January 2000 /JC-11 Committee

JEP 96 GUIDELINES FOR NONDESTRUCTIVE PULL TESTING OF WIRE BONDS ON HYBRID DEVICES

March 1977; Rescinded April 2000 /JC-13.5 Subcommittee

JEP 99 GLOSSARY OF MICROELECTRONIC TERMS, DEFINITIONS, AND SYMBOLS: ELEVATED TO JESD99, June 1985.

July 1977; Rescinded June 1985 /JC-10 Committee

JEP 100	TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR MICROCOMPUTERS AND MEMORY INTEGRATED CIRCUITS: ELEVATED TO JESD100, August 1993. September 1979; Rescinded October 1983 /JC-10 Committee	
JEP 101-C	JEDEC REQUIREMENTS FOR CLASS B MICROCIRCUITS: This revision reflects the following changes in MIL-Specs: 1) The conversion from MIL-M-38510 to MIL-I-38535 (renamed MIL-PRF-38535) as the General Specification for Microelectronics Devices. 2) The transfer of "Compliance Requirements" from General Provisions paragraph 1.2.1 of MIL-STD-883 to Appendix A of MIL-PRF-38535. November 1995 /JC-13.2 Subcommittee	\$38.00
JEP 102	STANDARD FOR 64K x 1 DYNAMIC RAM - SUPERSEDED BY JESD21-C. September 1978; Rescinded April 1985 April 1985 /JC-42 Committee	
JEP 103A	SUGGESTED PRODUCT-DOCUMENTATION, CLASSIFICATIONS, AND DISCLAIMERS In order to improve understanding between manufacturers and users, a consistent set of product-documentation classifications associated with the stages of product development. July 1996; Reaffirmed November 1999, May 2003 /JC-10 Committee	\$38.00
JEP 104C.01	REFERENCE GUIDE TO LETTER SYMBOLS FOR SEMICONDUCTOR DEVICES: This publication provides a quick reference to the letter symbols and corresponding terms that are defined in JESD77-B, Terms, Definitions, and Letter Symbols for Discrete Semiconductor and Optoelectronic Devices; JESD99-A, Terms, Definitions, and Letter Symbols for Microelectronic Devices, and JESD100-B, Terms, Definitions, and Letter Symbols for Microcomputers, Microprocessors, and Memory Integrated Circuits. It is intended to simplify interpretation of data sheets and specifications and to promote the uniform use of these symbols. The symbols relate to ratings and characteristics found in data sheets and other specifications. Some abbreviations used in lieu of symbols are also included. The newly added Annex B is provided as an aid to determining what symbol should be used and is organized by term, whereas the main body of the publication is organized by symbol or abbreviation as in previous versions. This version contains minor revisions. May 2003 /JC-10 Committee	\$91.00
JEP 105	JEDEC GUIDELINE FOR THE CHARACTERIZATION OF HYBRID POLYMERIC MATERIALS - SUPERSEDED BY JESD72, June 2001 April 1983; Rescinded June 2001 /JC-13.5 Subcommittee	

JEP 106P	STANDARD MANUFACTURERS IDENTIFICATION CODE: The manufacturers identification code is defined by one or more 8 bit fields, each consisting of 7 data bits plus 1 odd parity bit. The manufacturers identification code is assigned, maintained and updated by the JEDEC Office. The intent of this identification code is that it may be used whenever a digital field is required, e.g., hardware, software, documentation, etc. To make a request for an ID Code please go to http://www.jedec.org/Home/MIDCODE_request.cfm May 2004 /JC-42.3 Subcommittee	\$48.00
JEP 107	TEST METHOD FOR QUALIFICATION AND ACCEPTANCE OF PARTICLE GETTERS FOR USE IN HYBRID MICROELECTRONIC APPLICATIONS - SUPERSEDED BY JESD72, June 2001 April 1985; Rescinded June 2001 /JC-13.5 Subcommittee	
JEP 108-B	DISTRIBUTOR REQUIREMENTS FOR HANDLING ELECTROSTATIC - DISCHARGE SENSITIVE (ESDS) DEVICES: SUPERSEDED BY JESD42, March 1994. April 1991; Superseded /JC-14.1 Subcommittee	
JEP 109-C	GENERAL REQUIREMENTS FOR DISTRIBUTORS OF MILITARY SEMICONDUCTOR DEVICES: Superseded by JESD31-A, June 2001. March 1995; Rescinded November 2001 /JC-13 Committee	
JEP 110	GUIDELINES FOR THE MEASUREMENT OF THERMAL RESISTANCE OF GaAs FETS: This publication is intended for power GaAs FET applications requiring high reliability. An accurate measurement of thermal resistance is extremely important to provide the user with knowledge of the FETs operating temperature so that more accurate life estimates can be made. FET failure mechanisms and failure rates have, in general, an exponential dependence on temperature (which is why temperature-accelerated testing is successful). Because of the exponential relationship of failure rate with temperature, the thermal resistance should be referenced to the hottest part of the FET. July 1988 /JC-14.7 Subcommittee	\$43.00
JEP 111	TEST PROCEDURES FOR CUSTOM MONOLITHIC MICROCIRCUITS - SUPERSEDED BY MIL-PRF-38535C. July 1986; Rescinded June 1996 June 1996 /JC-13.2 Subcommittee	
JEP 112	TEST METHOD FOR QUALIFICATION AND ACCEPTANCE OF CIRCUIT SUPPORT FILMS FOR USE IN MICROELECTRONIC APPLICATIONS - SUPERSEDED BY JESD72, June 2001 June 1987; Rescinded June 2001 /JC-13 Committee	\$52.00

JEP 113-B	SYMBOL AND LABELS FOR MOISTURE-SENSITIVE DEVICES: Certain PSMC (Plastic Surface-mount Components) are subject to permanent damage due to moisture-induced failures encountered during high-temperature surface-mount processing unless appropriate precautions are observed. The purpose of this publication is to provide a distinctive symbol and labels to be used to identify those devices that require special packing and handling precautions. May 1999 /JC-14.1 Subcommittee	\$45.00
JEP 114	GUIDELINES FOR PARTICLE IMPACT NOISE DETECTION (PIND) TESTING, OPERATOR TRAINING, AND CERTIFICATION: This publication was developed to help the user of this test methodology avoid common interference's to successful application. The guide contains sections on typical specification requirements, sources of particles, PIND test systems, calibration, maintenance, test interference's, operator training, particle recovery and failure analysis. Application of the information contained in the guide will improve the quality and affectivity for any PIND testing operation. December 1989; Under Revision /JC-13 Committee	\$61.00
JEP 115	POWER MOSFET ELECTRICAL DOSE RATE TEST METHOD: The purpose of this Test Method is to establish electrical criteria for comparing and specifying power MOSFET performance under high dose rate radiation. August 1989; Reaffirmed April 1999 /JC-25 Committee	\$41.00
JEP 116	CMOS SEMICUSTOM DESIGN GUIDELINES: The design of ASIC circuits is becoming a significant part of system or product design, yet many problems continue to exist in current design practice. The guidelines in this document provide an explanation of common ASIC design problems and concerns and where possible offer solutions. November 1991 / Committee!33JC44	\$109.00
JEP 117	GUIDELINES FOR USER NOTIFICATION OF PRODUCT/PROCESS CHANGES BY SEMICONDUCTOR SUPPLIERS - SUPERSEDED BY JESD46, August 1997. April 1994; Rescinded July 1994 /JC-14.4 Subcommittee	
JEP 118	GUIDELINES FOR GaAs MMIC AND FET LIFE TESTING: These guidelines apply to monolithic microwave GaAs integrated circuits (MMICs) and their individual component building blocks, such as GaAs field effect transistors (FETs), resistors, and capacitors. The purpose of this document is to define a standard approach for evaluating the expected live of GaAs MMICs so that results from different life tests can be compared and so that wording of this	

document that the MMIC contains at least one FET, but the use of this document has no such limitation.

January 1993 /JC-14.7 Subcommittee

\$48.00

JEP 119A **A PROCEDURE FOR EXECUTING SWEAT:** This document describes an algorithm for performing the Standard Wafer Level Electromigration Accelerated Test (SWEAT) method with computer controlled instrumentation. The algorithm requires a separate iterative technique (not provided) to calculate the force current for a given target time to failure. This document does not specify what test structure to use with this procedure. However, users of this algorithm report its effectiveness on both straight-lines and via-terminated test structures. Some test-structures design features are provided in JESD87 and in ASTM 1259M - 96.

August 2003 /JC-14.2 Subcommittee

\$57.00

JEP 120-A **INDEX OF TERMS DEFINED IN JEDEC PUBLICATIONS:** This publication provides an index to terms that are defined in certain JEDEC publications. It is intended to promote the uniform use of these terms and their definitions while reducing the proliferation of new definitions for old terms.

May 2000 /JC-10 Committee

\$109.00

JEP 121 **GUIDELINES FOR MIL-STD-883 SCREENING AND QCI OPTIMIZATION:** The intent of this publication was developed to establish uniform guidelines, which would allow the use of In-Line Process Controls and Statistical Process Control as viable alternatives to the 100% screens and

April 1995 /JC-13 Committee

\$109.00

JEP 122-B **FAILURE MECHANISMS AND MODELS FOR SILICON SEMICONDUCTOR DEVICES:** This publication provides a list of failure mechanisms and their associated activation energies or acceleration factors that may be used in making system failure rate estimations when the only available data is based on tests performed at accelerated stress test conditions. The method to be used is the Sum of the Failure Rates method.

August 2003 /JC-14.1 Subcommittee

\$63.00

JEP 123 **GUIDELINE FOR MEASUREMENT OF ELECTRONIC PACKAGE INDUCTANCE AND CAPACITANCE MODEL PARAMETERS:** The need for this guideline arose from widespread lack of consistency in characterizing electrical parameters of electronic packages, which existed in the industry until the early 1990s. Then, the JEDEC Committee JC-15 provided the forum where various methods were discussed and commonality in approach emerged. The result is that today we have relatively consistent results in measuring and reporting electrical package parameters, as well as specialized tools

(e.g., the IPA-510, the interconnect parameter analyzer) which were developed to support the methodology.

October 1995 /JC-15.2 Subcommittee

\$49.00

JEP 124 **GUIDELINES FOR THE PACKING, HANDLING, AND REPACKING OF MOISTURE-SENSITIVE COMPONENTS - SUPERSEDED BY J-STD-033, May 1999.**

December 1995; Rescinded November 1999 November 1999 /JC-14.4 Subcommittee

JEP 126 **GUIDELINE FOR DEVELOPING AND DOCUMENTING PACKAGE ELECTRICAL MODELS DERIVED FROM COMPUTATIONAL ANALYSIS:**
This publication provides a guideline to suppliers of IC components with a template for documenting the numerical simulation assumptions. In addition this guideline also suggests a model environment to reference when comparing various packages or component suppliers. This publication should improve the communication between the package model suppliers. This publication should improve the communication between the package model supplier and the end user.

May 1996 /JC-15.2 Subcommittee

\$38.00

JEP 128 **GUIDE FOR STANDARD PROBE PAD SIZES AND LAYOUTS FOR WAFER LEVEL ELECTRICAL TESTING:** This guide was developed to expedite inter-laboratory experiments used to evaluate or develop standard test methods that involve test-structure measurements or tests. It also facilitates, generally, any electrical tests that require wafer-probe card to make electrical contact to test structures. Widespread use of this guide will afford the efficient and cost-effective use of wafer-probe test stations because of the need for fewer probe cards and probe-card changes to accommodate the various test structures that may need to be tested.

November 1996 /JC-14.2 Subcommittee

\$40.00

JEP 129 **THERMAL TEST CHIP GUIDELINE (WIRE BOND TYPE CHIP) - SUPERSEDED BY JESD51-4, September 1997.**

February 1997; Elevated September 1997 /JC-15.1 Subcommittee

JEP 130 **GUIDELINES FOR PACKING AND LABELING OF INTEGRATED CIRCUITS IN UNIT CONTAINER PACKING:** This document establishes guidelines for integrated circuit unit container and the next level (intermediate) container packing and labeling. The guidelines include tube/rail standardization, intermediate packing, date codes, tube labeling, intermediate container and shipping labels, and standardize tube quantities. Future revisions of this document will also include tray and reel guidelines. The objective of this publication is to promote the standardization of practices between manufacturers and distributors resulting in improved efficiency, profitability, and product quality.

August 1997 /JC-14.4 Subcommittee

\$40.00

JEP 131 **PROCESS FAILURE MODE AND EFFECTS ANALYSIS (FMEA) :** This publication was created in response to the need for a straight forward FMEA procedure. The objective is to provide a guideline for the application of FMEA techniques to improve quality, reliability and/or consistency of electronic components and subassemblies by continually evaluating processes/products against potential failure modes.

February 1998 /JC-14.3 Subcommittee

\$48.00

JEP 132 **PROCESS CHARACTERIZATION GUIDELINE:** This guideline provides a methodology to characterize a new or existing process and is applicable to any manufacturing or service process. It describes when to use specific tools such as failure mode effects analysis (FEMA), design or experiments (DOE), measurement system evaluation (MSE), capability analysis (CpK), statistical process control (SPC), and problem solving tools. It also provides a brief description of each tool.

July 1998 /JC-13 Committee

\$59.00

JEP 133-A **GUIDE FOR THE PRODUCTION AND ACQUISITION OF RADIATION-HARDNESS ASSURED MULTICHIP MODULES AND HYBRID MICROCIRCUITS:** A revised and expanded publication for suppliers and users of radiation hardness assured (RHA) multichip modules (MCMs) and hybrid microcircuits, is now available. Revision A of JEP133 includes modifications to the introduction, clarification of a definition and clarification of several technical issues within the document. In addition, the Bibliography section was updated to include added references. The document provides guidance as to how to achieve, maintain and ensure required levels of radiation-hardness given the fact that the constituent dice can have different levels of hardness assurance. It also describes how to deal with the various radiation hardness situations that an MCM/Hybrid developer, procuring activity or user will encounter. The guide is intended to supplement three relevant performance specifications: MIL-PRF-38534, MIL-PRF-38535 and MIL-PRF-19500.

July 2001 /JC-13.5 Subcommittee

\$59.00

JEP 134 **GUIDELINES FOR PREPARING CUSTOMER-SUPPLIED BACKGROUND INFORMATION RELATING TO A SEMICONDUCTOR-DEVICE FAILURE ANALYSIS:** The purpose of this Guideline is to provide a vehicle for acquiring and transmitting the necessary information in a concise, organized, and consistent format. Included in the Guideline is a sample form that facilitates transferring the maximum amount of background data to the failure analyst in a readily interpretable format. Immediate availability of this key information assists that analyst in completing a timely and accurate failure analysis.

September 1998 /JC-14.6 Subcommittee

\$45.00

Samsung Electronics Co., Ltd.

JEP 136	SIGNATURE ANALYSIS: Signature Analysis is a method to reduce the number of comprehensive physical failure analyses by the application of statistical inference techniques. The purpose of this document is to promote a common definition of Signature Analysis by inference, using the same statistical techniques, and to recognize that it is formal means of doing failure analysis. July 1999 /JC-14.6 Subcommittee	\$47.00
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JEP 137B	COMMON FLASH INTERFACE (CFI) IDENTIFICATION CODES: This publication is a companion document to the Common Flash Interface (CFI) standard, JESD68, which outlines the device and host system software interrogation handshake. JEP137 documents ID Code assignments for: 1)) the Algorithm-specific Command Set and Control Interfaces and 2) the Device Interfaces. It is published as needed when additions are made to either of these lists of codes. To make a request for an ID Code please contact the JEDEC Office at (703)907-7558. May 2004 /JC-42.4 Subcommittee	\$41.00
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JEP 138	USER GUIDELINES FOR IR THERMAL IMAGING DETERMINATION OF DIE TEMPERATURE: The purpose of these user guidelines is to provide background and an example for the use of an infrared (IR) microscope to determine die temperature of electronic devices for calculations such as thermal resistance. September 1999 /JC-25 Committee	\$41.00
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JEP 139	GUIDELINE FOR CONSTANT TEMPERATURE AGING TO CHARACTERIZE ALUMINUM INTERCONNECT METALLIZATIONS FOR STRESS-INDUCED VOIDING: This document describes a constant temperature (isothermal) aging method for testing aluminum (Al) metallization test structures on microelectronics wafers for susceptibility to stress-induced voiding. This method is valid for metallization/dielectric systems in which the dielectric is deposited onto the metallization at a temperature considerably above the intended use temperature, and above or equal to the deposition temperature of the metal. Although this is a wafer test, it is not a fast (less than 5 minutes per probe) test. It is intended to be used for lifetime prediction and failure analysis, not for production Go-NoGo lot checking. December 2000 /JC-14.2 Subcommittee	\$47.00
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JEP 140	BEADED THERMOCOUPLE TEMPERATURE MEASUREMENT OF SEMICONDUCTOR PACKAGES: The beaded thermocouple temperature measurement guideline provides a procedure to accurately and consistently measure the temperature of semiconductor packages during exposure to thermal excursions. The guideline applications can include, but not limited to, temperature profile measurement in	
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reliability test chambers and solder reflow operations that are associated with component assembly to printed wiring boards.

June 2002 /JC-14.1 Subcommittee

\$43.00

JEP 142 **GUIDELINE FOR OBTAINING AND ACCEPTING MATERIAL FOR USE IN HYBRID / MCM PRODUCTS:** This document provides guidance regarding design considerations, material assessment techniques, and recommendations for material acceptance prior to use in Hybrid / MCM Products. As part of the risk assessment process, both technical requirements and cost should be carefully considered with regard to testing / evaluating the elements of a hybrid microcircuit or Multi-chip Module (MCM) prior to material release for assembly. The intent of this document is to highlight various options that are available to the Hybrid / MCM manufacturer and provide associated guidance, not to impose a specific set of tests.

May 2002 /JC-13.5 Subcommittee

\$55.00

JEP 143A **SOLID STATE RELIABILITY ASSESSMENT QUALIFICATION METHODOLOGIES:** The purpose of this publication is to provide an overview of some of the most commonly used systems and test methods historically performed by manufacturers to assess and qualify the reliability of solid state products. The appropriate references to existing and proposed JEDEC (or EIA) standards and publications are cited. This document is also intended to provide an educational background and overview of some of the technical and economic factors associated with assessing and qualifying microcircuit reliability.

May 2004 /JC-14.3 Subcommittee

\$52.00

JEP 144 **GUIDELINE FOR RESIDUAL GAS ANALYSIS (RGA) FOR MICROELECTRONIC PACKAGES** The intent of this document is to give guidance on the Residual Gas Analysis (RGA) process and surrounding issues. The guideline describes how to select a suitable test lab and includes RGA history, measurement methodology, and issues that arise with the test. Interpreting the lab results along with common failure mechanisms are discussed at length along with process controls and alternative test techniques for measuring the moisture content within packages.

July 2002 /JC-13 Committee

\$57.00

JEP 145 **GUIDELINE FOR ASSESSING THE CURRENT-CARRYING CAPABILITY OF THE LEADS IN A POWER PACKAGE SYSTEM:** This publication is intended as a guideline to establish procedures, consideration and common practices that will allow a manufacturer, an application entity, a system designer and other interested parties to define current capability limitations in the leads of components and power systems with semiconductor components. This is a guideline, not a standardized method, it was developed over several years to clarify

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questions that had been posed to committee members in their respective engineering functions.

February 2003 /JC-25 Committee

\$41.00

JEP 146

GUIDELINES FOR SUPPLIER PERFORMANCE RATING: The intent of this document is to establish guidelines and provide examples by which customers can measure their suppliers based on mutually agreed upon objective criteria. These results can then be used to improve communications between customers and suppliers.

June 2003 September 2002 /JC-14.4 Subcommittee

\$47.00

JEP 147

PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER (VNA): This procedure describes a recommended way to measure pin capacitance of devices with SSTL (Stub Series Terminated Logic) interface pins by use of a Vector Network Analyzer. One purpose of this standard procedure is to reduce the lengthy and often inaccurate footnote - usually found around the specification of pin parasitics - to a simple reference to this document. In special cases modifying statements may adjust this procedure to the special needs of certain component.

October 2003 December 2002 / Committee!33JC162

\$41.00

JEP 148

Reliability Qualification of Semiconductor Devices Based on Physics of Failure Risk and Opportunity Assessment A concept is outlined, which proactively integrates qualification into the development process and provides a systematic procedure as support tool to development and gives early focus on required activities. It converts requirements for a product into measures of development and qualification in combination with a risk and opportunity assessment step and accompanies the development process as guiding and recording tool for advanced quality planning and confirmation. The collected data enlarge the knowledge database for DFR / BIR (design for reliability / building-in reliability) to be used for future projects. The procedure challenges and promotes teamwork of all involved disciplines. Based on the Physics-of-Failure (PoF) concept the reliability qualification methodology is re-arranged with regard to the relationships between design, technology, manufacturing and the different product life phases at use conditions. It makes use of the Physics-of-Failure concept by considering the potential individual failure mechanisms and relates most of the reliability aspects to the technology rather than to the individual product design. Evaluation of complex products using common reliability models and definition of sample sizes with respect to systematic inherent product properties and fractions of defects are discussed.

April 2004 January 2003 /JC-14.3 Subcommittee

\$63.00

NUMBER EIA Standards (EIA)

PRICE

EIA 236-C	COLOR CODING OF DISCRETE SEMICONDUCTOR DEVICES: This standard details the methods to be followed if color coding is used to identify JEDEC-assigned type numbers or for cathode identification of discrete semiconductor devices. ANSI/EIA-236-C-1986. March 1986; Reaffirmed November 1999 /JC-10 Committee	\$38.00
EIA 282-A	STANDARD FOR SILICON RECTIFIER DIODES: SEE JESD282-B ANSI/EIA-282-A-1989 February 1990 Became JESD282-B after revision April 2000 /JC-22.2 Subcommittee	
EIA 283	TEST METHOD FOR TRANSISTOR NOISE FIGURE MEASUREMENTS AT MEDIUM FREQUENCIES - SUPERSEDED BY EIA-311-A. November 1963; Rescinded November 1981 November 1981 /JC-25 Committee	
EIA 284-A	TEST METHODS FOR THE COLLECTOR-BASE TIME CONSTANT AND FOR THE RESISTIVE PART OF THE COMMON-EMITTER INPUT IMPEDANCE: SEE JESD284A. EIA-284-A became JESD284A after reaffirmation in October 2002. November 1963; Reaffirmed /JC-25 Committee	
EIA 286-A	STANDARD FOR MEASURING FORWARD SWITCHING CHARACTERISTICS OF SEMICONDUCTOR DIODES: SEE JESD286-B. ANSI/EIA-286-A-1991. February 1991 Became JESD286-B after revision February 2000 /JC-22.4 Subcommittee	
EIA 302	RANGES AND CONDITIONS FOR SPECIFYING BETA FOR LOW POWER, AUDIO FREQUENCY TRANSISTORS FOR ENTERTAINMENT SERVICE: This standard establishes the preferred rating ranges and conditions for specifying beta for low power, audio frequency transistors intended for entertainment service. January 1965; Reaffirmed April 1981, April 1999 /JC-25 Committee	\$37.00
EIA 306	MEASUREMENT OF SMALL SIGNAL HF, VHF, AND UHF POWER GAIN OF TRANSISTORS: This standard provides a method of measurement for small-signal HF, VHF, and UHF power gain of low power transistors. May 1965; Reaffirmed April 1981, April 1999 /JC-25 Committee	\$38.00
EIA 308-A	PREPARATION OF OUTLINE DRAWINGS OF SOLID-STATE PRODUCTS FOR JEDEC TYPE REGISTRATION: This standard is intended to serve as a guide to manufacturers of solid state products for the preparation of outline drawings of solid state product packages for JEDEC type registration. August 1981 /JC-11 Committee	\$38.00

EIA 311-A	MEASUREMENT OF TRANSISTOR NOISE FIGURE AT MF, HF, AND VHF: This standard describes a test method for measurement of transistor noise figure and effective input noise temperature at MF, HF, and VHF. This standard also adds the necessary information to make 'effective input noise temperature measurements'. This method is a revision of EIA-311 and incorporates material previously found in EIA-283. November 1981; Reaffirmed April 1999 /JC-25 Committee	\$48.00
EIA 318-B	MEASUREMENT OF REVERSE RECOVERY TIME FOR SEMICONDUCTOR SIGNAL DIODES: This standard describes the measurement of signal diodes ($I_F \leq 500\text{mA}$ dc) reverse recovery times of less than 300 ns duration. It may, however, also be used for the measurement of longer recovery times. This standard is also intended to establish a method which to characterize the test fixture used for this measurement. July 1996; Reaffirmed April 1999 /JC-22.4 Subcommittee	\$47.00
EIA 321-C	NUMBERING OF LIKE-NAMED TERMINAL FUNCTIONS IN SEMICONDUCTOR DEVICES AND DESIGNATION OF UNITS IN MULTIPLE-UNIT SEMICONDUCTOR DEVICES: This standard gives the system for numbering like-named electrodes or terminal functions in semiconductor devices and for assigning numerical designations to units of multiple-unit semiconductor devices. It applies to both integrated circuits and discrete devices. ANSI/EIA-321-C-1987 February 1987; Reaffirmed November 1995 November 1995 /JC-10 Committee	\$41.00
EIA 323	AIR-CONVECTION-COOLED, LIFE TEST ENVIRONMENT FOR LEAD-MOUNTED SEMICONDUCTOR DEVICES: This standard is applicable to life testing of lead-mounted semiconductor devices intended for applications in a natural air-cooled environment where most of the power dissipation is obtained by convection and radiation losses from the body to the device. March 1966; Reaffirmed February 1972, November 2002 November 2002 /JC-22.1 Subcommittee	\$40.00
EIA 340	STANDARD FOR THE MEASUREMENT OF CRE: This standard offers an easily measured parameter which is one of the significant characteristics in determining the stability of a transistor intended for small-signal operation. The measurement technique allows rapid testing. Its correlation to AC stability will help to establish the interchangeability of a device. November 1967; Reaffirmed April 1981, April 1999 /JC-25 Committee	\$43.00
EIA 353	THE MEASUREMENT OF TRANSISTOR NOISE FIGURE AT FREQUENCIES UP TO 20 kHz BY SINUSOIDAL SIGNAL-GENERATOR METHOD: This	

noise measurement method applies to transistors whose noise has a Gaussian power distribution, to transistors whose noise has a flat (white) power distribution, and to transistors whose noise has a 1/f (power inversely proportional to frequency) power distribution.

April 1968; Reaffirmed April 1981, April 1999 /JC-25 Committee \$40.00

EIA 354 THE MEASUREMENT OF TRANSISTOR EQUIVALENT NOISE VOLTAGE AND EQUIVALENT NOISE CURRENT AT FREQUENCIES OF UP TO 20 kHz: This standard provides a method for determining values, for device registration purposes, for transistor equivalent noise voltage and equivalent noise current at frequencies up to 20 kHz. This method is applicable to transistors whose noise has a Gaussian, flat (white) or 1/f power distribution.

April 1968; Reaffirmed April 1981, April 1999 /JC-25 Committee \$40.00

EIA 365 PERFORMANCE TEST PROCEDURE FOR SOLAR CELLS AND CALIBRATION PROCEDURE FOR SOLAR CELL STANDARDS FOR SPACE VEHICLE SERVICE: The purpose of this standard is to classify the output of solar cells for space vehicle service in accordance with requirements of EIA Format JS4-RDF4.

November 1969; Reaffirmed February 1984 / Committee!33JC231 \$47.00

EIA 371 THE MEASUREMENT OF SMALL-SIGNAL VHF-UHF TRANSISTOR SHORT-CIRCUIT FORWARD CURRENT TRANSFER RATIO: This standard describes the method to be used for the measurement of small-signal VHF-UHF transistor short-circuit forward current transfer ratio, in preparing data sheets for JEDEC registration of low power transistors.

February 1970; Reaffirmed April 1981, April 1999 /JC-25 Committee \$41.00

EIA 372 THE MEASUREMENT OF SMALL-SIGNAL VHF-UHF TRANSISTOR ADMITTANCE PARAMETERS: This standard describes the method to be used for the measurement of small-signal VHF-UHF transistor admittance parameters, in preparing data sheets for JEDEC registration of low power transistors.

May 1970; Reaffirmed April 1981, April 1999 /JC-25 Committee \$43.00

EIA 390-A STANDARD TEST PROCEDURE FOR NOISE MARGIN MEASUREMENTS FOR SEMICONDUCTOR LOGIC GATING MICROCIRCUITS: The purpose of this standard is to define the dc (Steady-State) noise margin and the ac (Transient) Noise Margin in Semiconductor Logic Gating Microcircuits, and to describe the procedures used to measure these parameters. The standardization of the definitions and test procedures is intended to improve the ability to ensure interchangeability of elements by test specification, and to eliminate misunderstandings between manufacturers and users.

February 1981 /JC-13 Committee \$43.00

EIA 397	RECOMMENDED STANDARD FOR THYRISTORS: One section of this standard presents a thorough explanation of thyristor principals, defining the different classes of these devices, their Physical structure and detailing the numerous test methods and ratings required in their application to electronic and power circuitry. Another section presents a universally accepted listing of letter symbols. Considerable effort is devoted to the use of JEDEC Type Registration System as related to thyristors. This will permit the device manufacturer to employ a uniform procedure in the development of maximum rating and presentation of performance data. June 1972 /JC-22.1 Subcommittee	\$177.00
EIA 397-1	ADDENDUM No. 1 TO EIA-397: A compilation of 12 new or revised thyristor test methods which have been adopted since the original standard was issued in 1972. July 1980 /JC-22.1 Subcommittee	\$83.00
EIA 398	MEASUREMENT OF SMALL VALUES OF TRANSISTOR CAPACITANCE: This standard contains a three-terminal procedure for capacitance measurement with due precautions for shielding of extraneous effects due to terminal leads and metal enclosures. July 1972; Reaffirmed April 1981, April 1999 /JC-25 Committee	\$43.00
EIA 428-A	TYPE DESIGNATION SYSTEM FOR MICROELECTRONIC DEVICES October 1988; Rescinded September 1993 September 1993 /JC-10 Committee	
EIA 435	STANDARD FOR THE MEASUREMENT OF SMALL-SIGNAL TRANSISTOR SCATTERING PARAMETERS: This standard specifies the standard for the measurement of small-signal transistor scattering parameters. June 1976; Reaffirmed April 1999 /JC-25 Committee	\$49.00
EIA 471	SYMBOL AND LABEL FOR ELECTROSTATIC SENSITIVE DEVICES: This standard will be useful to anyone engaged in handling semiconductor devices and integrated circuits that are subject to permanent damage due to electrostatic potentials. The standard establishes a symbol and label that will gain the attention of those persons who might inflict electrostatic damage to the device. The label which is placed on the lowest practical level of packaging contains the words 'ATTENTION - OBSERVE PRECAUTIONS FOR HANDLING ELECTROSTATIC SENSITIVE DEVICES'. The symbol contained in this label, which may be used on the device itself, shows a hand in a triangle with a bar through it. February 1980; Reaffirmed October 1988, September 1996, November 1996 /JC-10 Committee	\$38.00

EIA 557-A	STATISTICAL PROCESS CONTROL SYSTEMS: SPC embraces a management philosophy of continuous process improvement that has a primary focus on prevention of defects. After a process has been characterized using statistical techniques (i.e., design experiments (DOE), capability studies, etc.), SPC is a tool that can be applied to control and optimize the process and reduce variability. An acceptable approach toward an SPC system involves the use of 'end-of-process' data to control the process through the application of SPC techniques. However, the intent of this standard is to emphasize the use of in-process data in order to better control and forecast system quality. This proactive use of SPC in conjunction with other techniques and the appropriate responsiveness to out-of-control situations serves to make SPC techniques critical in continuous process improvement and achieving excellence. July 1995 /JC-13.5 Subcommittee	\$61.00
EIA 599-A	NATIONAL ELECTRONIC PROCESS CERTIFICATION STANDARD; GOVERNMENT CONTRACTORS: Due to notification from the JC-14.4 subcommittee that the material contained in EIA599 has been replaced by the ISO 9000 series, the JEDEC Board of Directors, at its August 2003 meeting, approved to remove this standard from the JEDEC Free Download Area. June 1998 August 2003 /JC-14.4 Subcommittee	
EIA 623	PROCUREMENT QUALITY OF SOLID STATE COMPONENTS BY GOVERNMENT CONTRACTORS: This standard defines the practices to be used by government contractors related to the procurement of solid state components. These practices include parts selection, supplier management, and receiving inspection and test. July 1994 /JC-13 Committee	\$40.00
EIA 625	REQUIREMENTS FOR HANDLING ELECTROSTATIC-DISCHARGE-SENSITIVE (ESDS) DEVICES (SUPERSEDES JEP108-B): SEE JESD625-A. November 1994 Became JESD625A after Revision December 1999 /JC-13 Committee	
EIA 659	FAILURE-MECHANISM-DRIVEN RELIABILITY MONITORING (SUPERSEDES JESD29-A): SEE JESD659-A. July 1996 Became JESD659A after Revision September 1999 /JC-14.3 Subcommittee	
EIA 670	QUALITY SYSTEM ASSESSMENT (SUPERSEDES JESD39-A): This standard is used by the electronic industry for preparation of audit checklists for assessing compliance of quality systems to the requirements of ANSI/ASQC Q9001 (ISO9001), ANSI/ASQC Q9002 (ISO9002), ANSI/ASQC Q9003 (ISO9003), and ANSI/EIA599, National Electronic Process Certification Standard. It also provides	

a tool for quality system evaluation in accordance with the guidelines of ANSI/ASQC Q9004 (ISO9004) and the Malcolm Baldrige National Quality Award Criteria.

June 1997 /JC-14.4 Subcommittee

\$63.00

EIA 671 **COMPONENT PROBLEM ANALYSIS AND CORRECTIVE ACTION REQUIREMENTS: SEE JESD671-A.**

November 1996 Became JESD671A after revision December 1999 /JC-14.4 Subcommittee

JESD 370B **DESIGNATION SYSTEM FOR SEMICONDUCTOR DEVICES:** This standard includes several new items and has been completely rewritten from the original EIA-370. The first is a new letter symbol C so that a JEDEC type designation may now be 2C1234, to indicate that a chip is being designated that if it were properly mounted on the package registered for the 2N1234, it would display characteristics similar to those of the 2N1234. The second major addition is the method for assigning the first numeric symbol for type designations of optoelectronic devices. ANSI/EIA-370-B-1992.

February 1982; Reaffirmed November 1995, November 1999, May 2003 /JC-10 Committee

\$43.00

Displayed by Committee

JC-10 Terms/Defin/Symbols

EIA 236-C COLOR CODING OF DISCRETE SEMICONDUCTOR DEVICES:

EIA 321-C NUMBERING OF LIKE-NAMED TERMINAL FUNCTIONS IN SEMICONDUCTOR DEVICES AND DESIGNATION OF UNITS IN MULTIPLE-UNIT SEMICONDUCTOR DEVICES:

JESD 370B DESIGNATION SYSTEM FOR SEMICONDUCTOR DEVICES:

EIA 428-A TYPE DESIGNATION SYSTEM FOR MICROELECTRONIC DEVICES

EIA 471 SYMBOL AND LABEL FOR ELECTROSTATIC SENSITIVE DEVICES:

JEP 100 TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR MICROCOMPUTERS AND MEMORY INTEGRATED CIRCUITS: ELEVATED TO JESD100, August 1993.

JEP 103A SUGGESTED PRODUCT-DOCUMENTATION, CLASSIFICATIONS, AND DISCLAIMERS

JEP 120-A INDEX OF TERMS DEFINED IN JEDEC PUBLICATIONS:

JEP 75 LETTER SYMBOLS USED WITH INFRARED DEVICES - INCORPORATED INTO JESD77-A.

JEP 99	GLOSSARY OF MICROELECTRONIC TERMS, DEFINITIONS, AND SYMBOLS: ELEVATED TO JESD99, June 1985.
JESD 100B.01	TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR MICROCOMPUTERS, MICROPROCESSORS, AND MEMORY INTEGRATED CIRCUITS:
JESD 99A.01	TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR MICROELECTRONIC DEVICES:
JESD 99-1	ADDENDUM No. 1 to JESD99 - TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR ANALOG-TO-DIGITAL AND DIGITAL-TO-ANALOG CONVERTERS:
JEP 104C.01	REFERENCE GUIDE TO LETTER SYMBOLS FOR SEMICONDUCTOR DEVICES:
JESD 77B	TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR DISCRETE SEMICONDUCTOR AND OPTOELECTRONIC DEVICES:
JESD 88	DICTIONARY OF TERMS FOR SOLID STATE TECHNOLOGY, First Edition:

JC-11 Mechanical Pkg Outlines

EIA 308-A	PREPARATION OF OUTLINE DRAWINGS OF SOLID-STATE PRODUCTS FOR JEDEC TYPE REGISTRATION:
JEB 20	ACCEPTED PRACTICES FOR MAKING MICROELECTRONIC DEVICE THERMAL CHARACTERISTICS TESTS
JEP 86-A	RECOMMENDED PRACTICE FOR DUAL DIMENSIONING
JEP 95 AUS	ANNUAL UPDATING SERVICE:
JEP 95	JEDEC REGISTERED AND STANDARD OUTLINES FOR SOLID STATE AND RELATED PRODUCTS:
JEP 95-1	DESIGN REQUIREMENTS (Book 1, Section 4)
JESD 30C	DESCRIPTIVE DESIGNATION SYSTEM FOR SEMICONDUCTOR-DEVICE PACKAGES:

JC-13 Government Liaison

EIA 390-A	STANDARD TEST PROCEDURE FOR NOISE MARGIN MEASUREMENTS FOR SEMICONDUCTOR LOGIC GATING MICROCIRCUITS:
EIA 623	PROCUREMENT QUALITY OF SOLID STATE COMPONENTS BY GOVERNMENT CONTRACTORS:
EIA 625	REQUIREMENTS FOR HANDLING ELECTROSTATIC-DISCHARGE-SENSITIVE (ESDS) DEVICES (SUPERSEDES JEP108-B): SEE JESD625-A.
JEP 109-C	GENERAL REQUIREMENTS FOR DISTRIBUTORS OF MILITARY SEMICONDUCTOR DEVICES:
JEP 112	TEST METHOD FOR QUALIFICATION AND ACCEPTANCE OF CIRCUIT SUPPORT FILMS FOR USE IN MICROELECTRONIC APPLICATIONS - SUPERSEDED BY JESD72, June 2001

JEP 114	GUIDELINES FOR PARTICLE IMPACT NOISE DETECTION (PIND) TESTING, OPERATOR TRAINING, AND CERTIFICATION:
JEP 121	GUIDELINES FOR MIL-STD-883 SCREENING AND QCI OPTIMIZATION:
JEP 132	PROCESS CHARACTERIZATION GUIDELINE:
JESD 16-A	ASSESSMENT OF AVERAGE OUTGOING QUALITY LEVELS IN PARTS PER MILLION (PPM):
JESD 19	GENERAL STANDARD FOR STATISTICAL PROCESS CONTROL (SPC) - SUPERSEDED by EIA-557-A
JESD 40	PROCUREMENT QUALITY OF SOLID STATE COMPONENTS BY GOVERNMENT CONTRACTORS - SUPERSEDED BY EIA-623, July 1994
JESD 42	REQUIREMENTS FOR HANDLING ELECTROSTATIC-DISCHARGE-SENSITIVE (ESDS) DEVICES - SUPERSEDED BY EIA-625, November 1994.
JESD 49	PROCUREMENT STANDARD FOR KNOWN GOOD DIE (KGD):
JEP 144	GUIDELINE FOR RESIDUAL GAS ANALYSIS (RGA) FOR MICROELECTRONIC PACKAGES

JC-13.2 Microelec. Devices

JEP 101-C	JEDEC REQUIREMENTS FOR CLASS B MICROCIRCUITS:
JEP 111	TEST PROCEDURES FOR CUSTOM MONOLITHIC MICROCIRCUITS - SUPERSEDED BY MIL-PRF-38535C.
JESD 26-A	GENERAL SPECIFICATION FOR PLASTIC ENCAPSULATED MICROCIRCUITS FOR USE IN RUGGED APPLICATIONS - RESCINDED, July 2001
JESD 53	MANAGEMENT OF COMPONENT OBSOLESCENCE BY GOVERNMENT CONTRACTORS: Rescinded, October 2002

JC-13.4 Radiation Hardness

JESD 57	TEST PROCEDURE FOR THE MANAGEMENT OF SINGLE-EVENT EFFECTS IN SEMICONDUCTOR DEVICES FROM HEAVY ION IRRADIATION:
JESD 89	MEASUREMENT AND REPORTING OF ALPHA PARTICLE AND TERRESTRIAL COSMIC RAY INDUCED SOFT ERRORS IN SEMICONDUCTOR DEVICES:

JC-13.5 Committee on Hybrid

EIA 557-A	STATISTICAL PROCESS CONTROL SYSTEMS:
JEP 105	JEDEC GUIDELINE FOR THE CHARACTERIZATION OF HYBRID POLYMERIC MATERIALS - SUPERSEDED BY JESD72, June 2001

JEP 107	TEST METHOD FOR QUALIFICATION AND ACCEPTANCE OF PARTICLE GETTERS FOR USE IN HYBRID MICROELECTRONIC APPLICATIONS - SUPERSEDED BY JESD72, June 2001
JEP 133-A	GUIDE FOR THE PRODUCTION AND ACQUISITION OF RADIATION-HARDNESS ASSURED MULTICHIP MODULES AND HYBRID MICROCIRCUITS:
JEP 96	GUIDELINES FOR NONDESTRUCTIVE PULL TESTING OF WIRE BONDS ON HYBRID DEVICES
JESD 27	CERAMIC PACKAGE SPECIFICATION FOR MICROELECTRONIC PACKAGES:
JESD 9-A	METAL PACKAGE SPECIFICATION FOR MICROELECTRONIC PACKAGES AND COVERS:
JESD 72	TEST METHODS AND ACCEPTANCE PROCEDURES FOR THE EVALUATION OF POLYMERIC MATERIALS:
JEP 142	GUIDELINE FOR OBTAINING AND ACCEPTING MATERIAL FOR USE IN HYBRID / MCM PRODUCTS:

JC-14 Quality/Reliability

JEB 16	USER GUIDE FOR MICROCIRCUIT FAILURE ANALYSIS:
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JC-14.1 Rel.Test Meth.Pkg.Dev.

J-STD- 020C	JOINT IPC/JEDEC STANDARD FOR MOISTURE/REFLOW SENSITIVITY CLASSIFICATION FOR NONHERMETIC SOLID STATE SURFACE-MOUNT DEVICES:
J-STD- 033A	JOINT IPC/JEDEC STANDARD FOR HANDLING, PACKING, SHIPPING AND USE OF MOISTURE/REFLOW SENSITIVE SURFACE-MOUNT DEVICES:
JEP 108-B	DISTRIBUTOR REQUIREMENTS FOR HANDLING ELECTROSTATIC - DISCHARGE SENSITIVE (ESDS) DEVICES: SUPERSEDED BY JESD42, March 1994.
JEP 113-B	SYMBOL AND LABELS FOR MOISTURE-SENSITIVE DEVICES:
JEP 122-B	FAILURE MECHANISMS AND MODELS FOR SILICON SEMICONDUCTOR DEVICES:
JESD 22-A100-B	CYCLED TEMPERATURE HUMIDITY BIAS LIFE TEST:
JESD 22-A101-B	STEADY-STATE TEMPERATURE HUMIDITY BIAS LIFE TEST:
JESD 22-A102-C	ACCELERATED MOISTURE RESISTANCE - UNBIASED AUTOCLAVE:
JESD 22-A103-B	HIGH TEMPERATURE STORAGE LIFE:

JESD 22-A104- TEMPERATURE CYCLING:

B

JESD 22-A106B THERMAL SHOCK:

JESD 22-A107B SALT ATMOSPHERE:

JESD 22-A109- HERMETICITY:

A

JESD 22-A110- HIGHLY ACCELERATED TEMPERATURE AND HUMIDITY STRESS TEST
B (HAST)

JESD 22-A112- MOISTURE-INDUCED STRESS SENSITIVITY FOR PLASTIC SURFACE
A MOUNT DEVICES - SUPERSEDED BY J-STD-020A, April 1999.

JESD 22-A113D PRECONDITIONING OF PLASTIC SURFACE MOUNT DEVICES PRIOR TO
RELIABILITY TESTING:

JESD 22-A114- ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY TESTING HUMAN
B BODY MODEL (HBM):

JESD 22-A115- ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY TESTING MACHINE
A MODEL (MM):

JESD 22-A117 ELECTRICALLY ERASABLE PROGRAMMABLE ROM (EEPROM)
PROGRAM/ERASE ENDURANCE AND DATA RETENTION TEST:

JESD 22-B100B PHYSICAL DIMENSION:

JESD 22-B101 EXTERNAL VISUAL:

JESD 22-B102- SOLDERABILITY:

C

JESD 22-B103- VIBRATION, VARIABLE FREQUENCY:

B

JESD 22-B104- MECHANICAL SHOCK:

B

JESD 22-B105C LEAD INTEGRITY:

JESD 22-B106- RESISTANCE TO SOLDERING TEMPERATURE FOR THROUGH-HOLE
B MOUNTED DEVICES:

JESD 22-B107B MARKING PERMANENCY:

JESD 22-B108A COPLANARITY TEST FOR SURFACE-MOUNT SEMICONDUCTOR DEVICES:

JESD 22-B116 WIRE BOND SHEAR TEST:

JESD 22-C100- HIGH TEMPERATURE CONTINUITY - RESCINDED, November 1999

A

JESD 22- FIELD-INDUCED CHARGED-DEVICE MODEL TEST METHOD FOR
C101B.01 ELECTROSTATIC DISCHARGE WITHSTAND THRESHOLDS OF
MICROELECTRONIC COMPONENTS:

JESD 625-A REQUIREMENTS FOR HANDLING ELECTROSTATIC-DISCHARGE-
SENSITIVE (ESDS) DEVICES:

JESD 22-B117 BALL GRID ARRAY (BGA) BALL SHEAR:

JESD 78 IC LATCH-UP TEST:

- JESD 22-A108-B** TEMPERATURE, BIAS, AND OPERATING LIFE:
- JESD 22-A118** ACCELERATED MOISTURE RESISTANCE - UNBIASED HAST:
- JESD 22-B110** SUBASSEMBLY MECHANICAL SHOCK:
- JESD 22-A120** TEST METHOD FOR THE MEASUREMENT OF MOISTURE DIFFUSIVITY AND WATER SOLUBILITY IN ORGANIC MATERIALS USED IN INTEGRATED CIRCUITS:
- JESD 22-B109** FLIP CHIP TENSILE PULL:
- JEP 140** BEADED THERMOCOUPLE TEMPERATURE MEASUREMENT OF SEMICONDUCTOR PACKAGES:
- J-STD- 002B** SOLDERABILITY TESTS FOR COMPONENT LEADS, TERMINATIONS, LUGS, TERMINALS AND WIRES:
- JESD 22-B111** BOARD LEVEL DROP TEST METHOD OF COMPONENTS FOR HANDHELD ELECTRONIC PRODUCTS:
- JESD 22-A105C** POWER AND TEMPERATURE CYCLING:
- JESD 97** Marking, Symbols, and Labels for Identification of Lead (Pb) Free Assemblies, Components, and Devices
- JESD 22-A111** EVALUATION PROCEDURE FOR DETERMINING CAPABILITY TO BOTTOM SIDE BOARD ATTACH BY FULL BODY SOLDER IMMERSION OF SMALL SURFACE MOUNT SOLID STATE DEVICES:
- JESD 89-1** System Soft Error Rate (SSER) Test Method

JC-14.1B JEDEC/IPC Joint Task

- J-STD- 035** JOINT IPC/JEDEC STANDARD FOR ACOUSTIC MICROSCOPY FOR NONHERMETRIC ENCAPSULATED ELECTRONIC COMPONENTS:

JC-14.2 Wafer Level Reliab

- JEP 119A** A PROCEDURE FOR EXECUTING SWEAT:
- JEP 128** GUIDE FOR STANDARD PROBE PAD SIZES AND LAYOUTS FOR WAFER LEVEL ELECTRICAL TESTING:
- JESD 28-A** A PROCEDURE FOR MEASURING N-CHANNEL MOSFET HOT-CARRIER-INDUCED DEGRADATION UNDER DC STRESS:
- JESD 33-B** STANDARD METHOD FOR MEASURING AND USING THE TEMPERATURE COEFFICIENT OF RESISTANCE TO DETERMINE THE TEMPERATURE OF A METALLIZATION LINE:
- JESD 34** FAILURE-MECHANISM-DRIVEN RELIABILITY QUALIFICATION OF SILICON DEVICES:
- JESD 35-A** PROCEDURE FOR WAFER-LEVEL-TESTING OF THIN DIELECTRICS:
- JESD 35-1** ADDENDUM No. 1 to JESD35 - GENERAL GUIDELINES FOR DESIGNING TEST STRUCTURES FOR THE WAFER-LEVEL TESTING OF THIN

DIELECTRICS:

JESD 35-2	ADDENDUM No. 2 to JESD35 - TEST CRITERIA FOR THE WAFER-LEVEL TESTING OF THIN DIELECTRICS:
JESD 37	STANDARD LOGNORMAL ANALYSIS OF UNCENSORED DATA, AND OF SINGLY RIGHT -CENSORED DATA UTILIZING THE PERSSON AND ROOTZEN METHOD:
JESD 60	A PROCEDURE FOR MEASURING P-CHANNEL MOSFET HOT-CARRIER-INDUCED DEGRADATION AT MAXIMUM GATE CURRENT UNDER DC STRESS:
JESD 61	ISOTHERMAL ELECTROMIGRATION TEST PROCEDURE:
JESD 63	STANDARD METHOD FOR CALCULATING THE ELECTROMIGRATION MODEL PARAMETERS FOR CURRENT DENSITY AND TEMPERATURE:
JEP 139	GUIDELINE FOR CONSTANT TEMPERATURE AGING TO CHARACTERIZE ALUMINUM INTERCONNECT METALLIZATIONS FOR STRESS-INDUCED VOIDING:
JESD 87	STANDARD TEST STRUCTURE FOR RELIABILITY ASSESSMENT OF AlCu METALLIZATIONS WITH BARRIER MATERIALS
JESD 28-1	N-CHANNEL MOSFET HOT CARRIER DATA ANALYSIS:
JP 001.01	FOUNDRIY PROCESS QUALIFICATION GUIDELINES (Wafer Fabrication Manufacturing Sites)
JESD 92	PROCEDURE FOR CHARACTERIZING TIME-DEPENDENT DIELECTRIC BREAKDOWN OF ULTRA-THIN GATE DIELECTRICS:

JC-14.3 Silicon Devices RQM

EIA 659	FAILURE-MECHANISM-DRIVEN RELIABILITY MONITORING (SUPERSEDES JESD29-A): SEE JESD659-A.
JEP 131	PROCESS FAILURE MODE AND EFFECTS ANALYSIS (FMEA):
JESD 29-A	FAILURE-MECHANISM-DRIVEN RELIABILITY MONITORING - SUPERSEDED BY EIA/ANSI-659, July 1996.
JESD 47B	STRESS-TEST-DRIVEN QUALIFICATION OF INTEGRATED CIRCUITS:
JESD 50	SPECIAL REQUIREMENTS FOR MAVERICK PRODUCT ELIMINATION:
JESD 62-A	OUTLIER IDENTIFICATION AND MANAGEMENT SYSTEM FOR ELECTRONIC COMPONENTS:
JESD 659-A	FAILURE-MECHANISM-DRIVEN RELIABILITY MONITORING:
JESD 69	INFORMATION REQUIREMENTS FOR THE QUALIFICATION OF SILICON DEVICES:
JESD 74	EARLY LIFE FAILURE RATE CALCULATION PROCEDURE FOR ELECTRONIC COMPONENTS:
JESD 85	METHODS FOR CALCULATING FAILURE RATES IN UNITS OF FITS:
JESD 86	ELECTRICAL PARAMETERS ASSESSMENT:

- JEP 143A** SOLID STATE RELIABILITY ASSESSMENT QUALIFICATION METHODOLOGIES:
- JESD 91-A** METHOD FOR DEVELOPING ACCELERATION MODELS FOR ELECTRONIC COMPONENT FAILURE MECHANISMS:
- JESD 94** APPLICATION SPECIFIC QUALIFICATION USING KNOWLEDGE BASED TEST METHODOLOGY:
- JEP 148** Reliability Qualification of Semiconductor Devices Based on Physics of Failure Risk and Opportunity Assessment

JC-14.4 Quality System Stand

- EIA 599-A** NATIONAL ELECTRONIC PROCESS CERTIFICATION STANDARD; GOVERNMENT CONTRACTORS:
- EIA 670** QUALITY SYSTEM ASSESSMENT (SUPERSEDES JESD39-A):
- EIA 671** COMPONENT PROBLEM ANALYSIS AND CORRECTIVE ACTION REQUIREMENTS: SEE JESD671-A.
- JEP 117** GUIDELINES FOR USER NOTIFICATION OF PRODUCT/PROCESS CHANGES BY SEMICONDUCTOR SUPPLIERS - SUPERSEDED BY JESD46, August 1997.
- JEP 124** GUIDELINES FOR THE PACKING, HANDLING, AND REPACKING OF MOISTURE-SENSITIVE COMPONENTS - SUPERSEDED BY J-STD-033, May 1999.
- JEP 130** GUIDELINES FOR PACKING AND LABELING OF INTEGRATED CIRCUITS IN UNIT CONTAINER PACKING:
- JEP 70-B** QUALITY AND RELIABILITY STANDARDS AND PUBLICATIONS:
- JESD 31C** GENERAL REQUIREMENTS FOR DISTRIBUTORS OF COMMERCIAL AND MILITARY SEMICONDUCTOR DEVICES:
- JESD 39-A** QUALITY SYSTEM ASSESSMENT - SUPERSEDED BY ANSI/EIA-670, June 1997.
- JESD 43** COMPONENT PROBLEM ANALYSIS AND CORRECTIVE ACTION REQUIREMENTS - SUPERSEDED BY EIA-671, November 1996.
- JESD 46-B** CUSTOMER NOTIFICATION OF PRODUCT/PROCESS CHANGES BY SEMICONDUCTOR SUPPLIERS:
- JESD 48-A** PRODUCT DISCONTINUANCE:
- JESD 671-A** COMPONENT QUALITY PROBLEM ANALYSIS AND CORRECTIVE ACTION REQUIREMENTS (INCLUDING ADMINISTRATIVE QUALITY PROBLEMS):
- JEP 146** GUIDELINES FOR SUPPLIER PERFORMANCE RATING:

JC-14.6 Failure Analysis

- JEP 134** GUIDELINES FOR PREPARING CUSTOMER-SUPPLIED BACKGROUND INFORMATION RELATING TO A SEMICONDUCTOR-DEVICE FAILURE

ANALYSIS:

JEP 136

SIGNATURE ANALYSIS:

JESD 38

STANDARD FOR FAILURE ANALYSIS REPORT FORMAT:

JC-14.7 GaAs Rel. & Quality

JEP 110

GUIDELINES FOR THE MEASUREMENT OF THERMAL RESISTANCE OF GaAs FETS:

JEP 118

GUIDELINES FOR GaAs MMIC AND FET LIFE TESTING:

JES 2

TRANSISTOR, GALLIUM ARSENIDE POWER FET, GENERIC SPECIFICATION:

JC-15 Elect./Thermal

JESD 51- 1

INTEGRATED CIRCUIT THERMAL MEASUREMENT METHOD - ELECTRICAL TEST METHOD (SINGLE SEMICONDUCTOR DEVICE):

JESD 51- 2

INTEGRATED CIRCUITS THERMAL TEST METHOD ENVIRONMENTAL CONDITIONS - NATURAL CONVECTION (STILL AIR):

JESD 59

BOND WIRE MODELING STANDARD:

JC-15.1 Thermal Character.

JEP 129

THERMAL TEST CHIP GUIDELINE (WIRE BOND TYPE CHIP)- SUPERSEDED BY JESD51-4, September 1997.

JESD 51

METHODOLOGY FOR THE THERMAL MEASUREMENT OF COMPONENT PACKAGES (SINGLE SEMICONDUCTOR DEVICE)

JESD 51- 3

LOW EFFECTIVE THERMAL CONDUCTIVITY TEST BOARD FOR LEADED SURFACE MOUNT PACKAGES:

JESD 51- 4

THERMAL TEST CHIP GUIDELINE (WIRE BOND TYPE CHIP):

JESD 51- 5

EXTENSION OF THERMAL TEST BOARD STANDARDS FOR PACKAGES WITH DIRECT THERMAL ATTACHMENT MECHANISMS:

JESD 51- 6

INTEGRATED CIRCUIT THERMAL TEST METHOD ENVIRONMENTAL CONDITIONS - FORCED CONVECTION (MOVING AIR):

JESD 51- 7

HIGH EFFECTIVE THERMAL CONDUCTIVITY TEST BOARD FOR LEADED SURFACE MOUNT PACKAGES:

JESD 51- 8

INTEGRATED CIRCUIT THERMAL TEST METHOD ENVIRONMENTAL CONDITIONS - JUNCTION-TO-BOARD:

JESD 51- 9

TEST BOARDS FOR AREA ARRAY SURFACE MOUNT PACKAGE THERMAL MEASUREMENTS:

JESD 51-10

TEST BOARDS FOR THROUGH-HOLE PERIMETER LEADED PACKAGE THERMAL MEASUREMENTS:

JESD 51-11 TEST BOARDS FOR THROUGH-HOLE AREA ARRAY LEADED PACKAGE THERMAL MEASUREMENT:

JC-15.2 Elec. Char. Tech.

JEP 123 GUIDELINE FOR MEASUREMENT OF ELECTRONIC PACKAGE INDUCTANCE AND CAPACITANCE MODEL PARAMETERS:

JEP 126 GUIDELINE FOR DEVELOPING AND DOCUMENTING PACKAGE ELECTRICAL MODELS DERIVED FROM COMPUTATIONAL ANALYSIS:

JC-16 Elec. Intrfcs/Pwr Supply

JESD 8- 1 ADDENDUM No. 1 to JESD8: INTERFACE STANDARD FOR LOW VOLTAGE TTL-COMPATIBLE (LVTTL) VLSI DIGITAL CIRCUITS

JESD 8- 2 ADDENDUM No. 2 to JESD8 - STANDARD FOR OPERATING VOLTAGES AND INTERFACE LEVELS FOR LOW VOLTAGE EMITTER-COUPLED LOGIC (ECL) INTEGRATED CIRCUITS:

JESD 8- 3 ADDENDUM No. 3 to JESD8 - GUNNING TRANSCEIVER LOGIC (GTL) LOW-LEVEL, HIGH-SPEED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS:

JESD 8- 4 ADDENDUM No. 4 to JESD8 - CENTER-TAP-TERMINATED (CTT) INTERFACE LOW-LEVEL, HIGH-SPEED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS:

JESD 8- 5 ADDENDUM No. 5 to JESD8 - 2.5 V 0.2 V (NORMAL RANGE), AND 1.8 V TO 2.7 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUIT:

JESD 8- 6 ADDENDUM No. 6 to JESD8 - HIGH SPEED TRANSCEIVER LOGIC (HSTL)- A 1.5 V OUTPUT BUFFER SUPPLY VOLTAGE BASED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS:

JESD 8- 7 ADDENDUM No. 7 to JESD8 - 1.8 V + -0.15 V (NORMAL RANGE), AND 1.2 V - 1.95 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUIT:

JESD 8- 8 ADDENDUM No. 8 to JESD8 - STUB SERIES TERMINATED LOGIC FOR 3.3 VOLTS (SSTL_3) A 3.3 V VOLTAGE BASED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS:

JESD 8- 9B ADDENDUM No. 9B to JESD8 - STUB SERIES TERMINATED LOGIC FOR 2.5 VOLTS (SSTL_2): Includes Errata and Corrected Page 7 as of October 18, 2002.

JESD 67 I/O DRIVERS AND RECEIVERS WITH CONFIGURABLE COMMUNICATION VOLTAGE, IMPEDANCE, AND RECEIVER THRESHOLD:

JESD 8- 1-A INTERFACE STANDARD FOR NOMINAL 0.3 V/3.3 V SUPPLY DIGITAL INTEGRATED CIRCUITS

JESD 8-B	INTERFACE STANDARD FOR NOMINAL 0.3 V/3.3 V SUPPLY DIGITAL INTEGRATED CIRCUITS:
JESD 8-11	ADDENDUM No. 11 to JESD8 - 1.5 V +/- 0.1 V (NORMAL RANGE) AND 0.9 - 1.6 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUITS:
JESD 8-12	1.2 V +/- 0.1 V (NORMAL RANGE) AND 0.8 - 1.3 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUITS:
JESD 8-13	SCALABLE LOW-VOLTAGE SIGNALING FOR 400 MV (SLVS-400):
JESD 8-14	1.0 V +/- 0.1 V (NORMAL RANGE) AND 0.7 V - 1.1 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUITS:
JESD 8-15A	STUB SERIES TERMINATED LOGIC FOR 1.8 V (SSTL_18):

JC-22.1 Thyristors

EIA 323	AIR-CONVECTION-COOLED, LIFE TEST ENVIRONMENT FOR LEAD-MOUNTED SEMICONDUCTOR DEVICES:
EIA 397-1	ADDENDUM No. 1 TO EIA-397:
JEP 88	THERMAL RESISTANCE AND THERMAL IMPEDANCE TEST METHODS FOR STUD AND BASE-MOUNTED RECTIFIER DIODES AND THYRISTORS
JESD 41	REVERSE RECOVERY CHARACTERISTICS OF SILICON DIODES: Rescinded June 2002.
EIA 397	RECOMMENDED STANDARD FOR THYRISTORS:

JC-22.2 Rectifier Diodes

EIA 282-A	STANDARD FOR SILICON RECTIFIER DIODES: SEE JESD282-B
JEP 87	FORWARD TURN-ON TIME MEASUREMENT ON SEMI-DIODES - INCORPORATED INTO EIA-282-A.
JESD 14	SEMICONDUCTOR POWER CONTROL MODULES:
JESD 4	DEFINITION OF EXTERNAL CLEARANCE AND CREEPAGE DISTANCES OF DISCRETE SEMICONDUCTOR PACKAGES FOR THYRISTORS AND RECTIFIER DIODES:
JESD 45	MEASUREMENT METHOD FOR THERMAL RESISTANCE OF BRIDGE RECTIFIER ASSEMBLIES: Rescinded June 2002. Replaced by JESD282-B.
TENTSTD 11	HANDLING AND INSTALLATION OF POWER SEMICONDUCTORS IN DISC TYPE PACKAGES: Included in JESD282 and EIA397.
JESD 282B.01	SILICON RECTIFIER DIODES:

JC-22.4 Signal Regltr Diodes

EIA 286-A	STANDARD FOR MEASURING FORWARD SWITCHING CHARACTERISTICS OF SEMICONDUCTOR DIODES: SEE JESD286-B.
JESD 307	VOLTAGE REGULATOR DIODE NOISE VOLTAGE MEASUREMENT:
EIA 318-B	MEASUREMENT OF REVERSE RECOVERY TIME FOR SEMICONDUCTOR SIGNAL DIODES:
JESD 320-A	CONDITIONS FOR MEASUREMENT OF DIODE STATIC PARAMETERS:
JESD 381-A	METHOD OF DIODE Q MEASUREMENT:
JESD 482-A	LIST OF PREFERRED VALUES FOR USE ON VARIOUS TYPES OF SMALL SIGNAL AND REGULATOR DIODES:
JESD 531	THERMAL RESISTANCE TEST METHOD FOR SIGNAL AND REGULATOR DIODES (FORWARD VOLTAGE, SWITCHING METHOD):
JEP 90	THERMAL RESISTANCE FOR TEST METHODS FOR SIGNAL DIODES - SUPERSEDED BY EIA-531, July 1986. See JESD531, April 2002.
JESD 5	MEASUREMENT OF TEMPERATURE COEFFICIENT OF VOLTAGE REGULATOR DIODES:
JESD 286-B	STANDARD FOR MEASURING FORWARD SWITCHING CHARACTERISTICS OF SEMICONDUCTOR DIODES:

JC-22.5 Transient Voltage Supp

JESD 66	TRANSIENT VOLTAGE SUPPRESSOR STANDARD FOR THYRISTOR SURGE PROTECTIVE DEVICE:
TENTSTD 12	STANDARD FOR SELENIUM SURGE SUPPRESSORS:

JC-25 Transistors

EIA 283	TEST METHOD FOR TRANSISTOR NOISE FIGURE MEASUREMENTS AT MEDIUM FREQUENCIES - SUPERSEDED BY EIA-311-A.
JESD 284-A	TEST METHODS FOR THE COLLECTOR-BASE TIME CONSTANT AND FOR THE RESISTIVE PART OF THE COMMON-EMITTER INPUT IMPEDANCE:
EIA 302	RANGES AND CONDITIONS FOR SPECIFYING BETA FOR LOW POWER, AUDIO FREQUENCY TRANSISTORS FOR ENTERTAINMENT SERVICE:
EIA 306	MEASUREMENT OF SMALL SIGNAL HF, VHF, AND UHF POWER GAIN OF TRANSISTORS:
EIA 311-A	MEASUREMENT OF TRANSISTOR NOISE FIGURE AT MF, HF, AND VHF:
JESD 313-B	THERMAL RESISTANCE MEASUREMENTS OF CONDUCTION COOLED POWER TRANSISTORS:
EIA 340	STANDARD FOR THE MEASUREMENT OF CRE:
EIA 353	THE MEASUREMENT OF TRANSISTOR NOISE FIGURE AT FREQUENCIES UP TO 20 kHz BY SINUSOIDAL SIGNAL-GENERATOR METHOD:

EIA 354	THE MEASUREMENT OF TRANSISTOR EQUIVALENT NOISE VOLTAGE AND EQUIVALENT NOISE CURRENT AT FREQUENCIES OF UP TO 20 kHz:
EIA 371	THE MEASUREMENT OF SMALL-SIGNAL VHF-UHF TRANSISTOR SHORT-CIRCUIT FORWARD CURRENT TRANSFER RATIO:
EIA 372	THE MEASUREMENT OF SMALL-SIGNAL VHF-UHF TRANSISTOR ADMITTANCE PARAMETERS:
EIA 398	MEASUREMENT OF SMALL VALUES OF TRANSISTOR CAPACITANCE:
JESD 419-A	STANDARD LIST OF VALUES TO BE USED IN SEMICONDUCTOR DEVICE SPECIFICATIONS AND REGISTRATION FORMAT:
EIA 435	STANDARD FOR THE MEASUREMENT OF SMALL-SIGNAL TRANSISTOR SCATTERING PARAMETERS:
JEP 115	POWER MOSFET ELECTRICAL DOSE RATE TEST METHOD:
JEP 138	USER GUIDELINES FOR IR THERMAL IMAGING DETERMINATION OF DIE TEMPERATURE:
JEP 65	TEST PROCEDURES FOR VERIFICATION OF MAXIMUM RATINGS OF POWER TRANSISTORS:
JEP 69-B	PREFERRED LEAD CONFIGURATION FOR FIELD-EFFECT TRANSISTORS:
JEP 74	STANDARD LIST OF VALUES TO BE USED IN POWER TRANSISTOR DEVICE REGISTRATION AND MINIMUM DIFFERENCES FOR DISCRETENESS OF REGISTRATIONS - SUPERSEDED BY EIA-419-A, February 1996.
JEP 84A	RECOMMENDED PRACTICE FOR MEASUREMENT OF TRANSISTOR LEAD TEMPERATURE:
JESD 24	POWER MOSFETS:
JESD 24- 1	ADDENDUM No. 1 to JESD24 - METHOD FOR MEASUREMENT OF POWER DEVICE TURN-OFF SWITCHING LOSS:
JESD 24-10	ADDENDUM No. 10 to JESD24 - TEST METHOD FOR MEASUREMENT OF REVERSE RECOVERY TIME t_{rr} FOR POWER MOSFET DRAIN-SOURCE DIODES:
JESD 24-11	ADDENDUM No. 11 to JESD24 - POWER MOSFET EQUIVALENT SERIES GATE RESISTANCE TEST METHOD:
JESD 24- 2	ADDENDUM No. 2 to JESD24 - GATE CHARGE TEST METHOD:
JESD 24- 3	ADDENDUM No. 3 to JESD24 - THERMAL IMPEDANCE MEASUREMENTS FOR VERTICAL POWER MOSFETS (DELTA SOURCE-DRAIN VOLTAGE METHOD):
JESD 24- 4	ADDENDUM No. 4 to JESD24 - THERMAL IMPEDANCE MEASUREMENTS FOR BIPOLAR TRANSISTORS (DELTA BASE-EMITTER VOLTAGE METHOD):
JESD 24- 5	ADDENDUM No. 5 to JESD24 - SINGLE PULSE UNCLAMPED INDUCTIVE SWITCHING (UIS) AVALANCHE TEST METHOD:
JESD 24- 6	ADDENDUM No. 6 to JESD24 - THERMAL IMPEDANCE MEASUREMENTS FOR INSULATED GATE BIPOLAR TRANSISTORS:

JESD 24- 7	ADDENDUM No. 7 to JESD24 - COMMUTATING DIODE SAFE OPERATING AREA TEST PROCEDURE FOR MEASURING dv/dt DURING REVERSE RECOVERY OF POWER TRANSISTORS:
JESD 24- 8	ADDENDUM No. 8 to JESD24 - METHOD FOR REPETITIVE INDUCTIVE LOAD AVALANCHE SWITCHING:
JESD 24- 9	ADDENDUM No. 9 to JESD24 - SHORT CIRCUIT WITHSTAND TIME TEST METHOD:
JESD 25	MEASUREMENT OF SMALL-SIGNAL TRANSISTOR SCATTERING PARAMETERS:
JESD 6	MEASUREMENT OF SMALL VALUES OF TRANSISTOR CAPACITANCE:
JESD 10	LOW FREQUENCY POWER TRANSISTORS:
EIA 284-A	TEST METHODS FOR THE COLLECTOR-BASE TIME CONSTANT AND FOR THE RESISTIVE PART OF THE COMMON-EMITTER INPUT IMPEDANCE: SEE JESD284A.
JEP 145	GUIDELINE FOR ASSESSING THE CURRENT-CARRYING CAPABILITY OF THE LEADS IN A POWER PACKAGE SYSTEM:
JESD 24-12	Thermal Impedance Measurement for Insulated Gate Bipolar Transistors - (Delta VCE(on) Method)

JC-40 CMOS Digital Logic

JEB 15	TERMINOLOGY AND METHODS OF MEASUREMENT FOR BISTABLE SEMICONDUCTOR MICROCIRCUITS:
JEB 19	RECOMMENDED CHARACTERIZATION OF MOS SHIFT REGISTERS:
JESD 36	STANDARD DESCRIPTION OF LOW-VOLTAGE TTL-COMPATIBLE, 5 V TOLERANT CMOS LOGIC DEVICES:
JESD 52	STANDARD FOR DESCRIPTION OF LOW VOLTAGE TTL-COMPATIBLE CMOS LOGIC DEVICES:
JESD 54	STANDARD FOR DESCRIPTION OF 54/74ABTXXX AND 74BCXXX TTL-COMPATIBLE BiCMOS LOGIC DEVICES:
JESD 55	STANDARD FOR DESCRIPTION OF LOW-VOLTAGE TTL-COMPATIBLE BiCMOS LOGIC DEVICES:
JESD 65B	DEFINITION OF SKEW SPECIFICATIONS FOR STANDARD LOGIC DEVICES:
JESD 70	2.5 V BiCMOS LOGIC DEVICE FAMILY SPECIFICATION WITH 5 V TOLERANT INPUTS AND OUTPUTS:
JESD 73	DESCRIPTION OF 5 V BUS SWITCH WITH TTL-COMPATIBLE CONTROL INPUTS:
JESD 80	STANDARD FOR DESCRIPTION OF 2.5 V CMOS LOGIC DEVICES:
JESD 64-A	STANDARD FOR DESCRIPTION OF 2.5 V CMOS LOGIC DEVICES WITH 3.6 V CMOS TOLERANT INPUTS AND OUTPUTS:

JESD 75	BALL GRID ARRAY PINOUTS STANDARDIZED FOR 32-BIT LOGIC FUNCTIONS:
JESD 82	DEFINITION OF CDCV857 PLL CLOCK DRIVER FOR REGISTERED DDR DIMM APPLICATIONS:
JESD 76-1	STANDARD DESCRIPTION OF 1.2 V CMOS LOGIC DEVICES (WIDE RANGE OPERATION):
JESD 76-2	STANDARD DESCRIPTION OF 1.2 V CMOS LOGIC DEVICES (NORMAL RANGE OPERATION):
JESD 82-2	STANDARD FOR DESCRIPTION OF A 3.3 V, 18-BIT, LVTTTL I/O REGISTER FOR PC133 REGISTERED DIMM APPLICATIONS:
JESD 75-2	BALL GRID ARRAY PINOUTS STANDARDIZED FOR 16-BIT LOGIC FUNCTIONS:
JESD 75-3	BALL GRID ARRAY PINOUTS STANDARDIZED FOR 8-BIT LOGIC FUNCTIONS:
JESD 82-3A	DEFINITION OF THE SSTV16857 2.5 V, 14-BIT SSTL_2 REGISTERED BUFFER FOR DDR DIMM APPLICATIONS:
JESD 73-1	STANDARD FOR DESCRIPTION OF 3.3 V NFET BUS SWITCH DEVICES:
JESD 73-2	STANDARD FOR DESCRIPTION OF 3.3 V NFET BUS SWITCH DEVICES WITH INTEGRATED CHARGE PUMPS:
JESD 82-4B	STANDARD FOR DEFINITION OF THE SSTV16859 2.5 V, 13-BIT TO 26-BIT SSTL_2 REGISTERED BUFFER FOR STACKED DDR DIMM APPLICATIONS:
JESD 75-1	BALL GRID ARRAY PINOUTS STANDARDIZED FOR 16, 18, AND 20-BIT LOGIC FUNCTIONS USING A 54 BALL PACKAGE:
JESD 82-5	STANDARD FOR DESCRIPTION OF A 3.3 V, ZERO DELAY CLOCK DISTRIBUTION DEVICE COMPLIANT WITH THE JESD21-C PC133 REGISTERED DIMM SPECIFICATION
JESD 82-1A	DEFINITION OF CVF857 PLL CLOCK DRIVER FOR REGISTERED PC1600, PC2100, AND PC2700 DIMM APPLICATIONS:
JESD 82-8.01	STANDARD FOR DEFINITION OF $\frac{1}{2}$ CU877 PLL CLOCK DRIVER FOR REGISTERED DDR2 DIMM APPLICATIONS
JESD 75-4	Ball Grid Array Pinout for 1-, 2-, and 3-Bit Logic Functions

JC-40.1 Digital Logic Families

JESD 2	DIGITAL BIPOLAR LOGIC PINOUTS FOR CHIP CARRIERS:
JESD 76	DESCRIPTION OF 1.8 V CMOS LOGIC DEVICES:
JESD 76-3	STANDARD DESCRIPTION OF 1.5 V CMOS LOGIC DEVICES:
JESD 75-5	SON/QFN PACKAGE PINOUTS STANDARDIZED FOR 1-, 2-, AND 3-BIT LOGIC FUNCTIONS

JC-42 for all 42.xx members

JEP 102 STANDARD FOR 64K x 1 DYNAMIC RAM - SUPERSEDED BY JESD21-C.
JESD 21-C CONFIGURATIONS FOR SOLID STATE MEMORIES:
JESD 21-C AUS ANNUAL UPDATING SERVICE:

JC-42.3 RAM Memories

JEP 106P STANDARD MANUFACTURERS IDENTIFICATION CODE:
JESD 79-2A DDR2 SDRAM SPECIFICATION

JC-42.4 Non-Volatile Memories

JEP 137B COMMON FLASH INTERFACE (CFI) IDENTIFICATION CODES:
JESD 68.01 COMMON FLASH INTERFACE (CFI):

JC-61 Wireless Interface Netwo

JESD 96 Radio Front End - Baseband (RF-BB) Interface

JEDEC BOD

JEB 5-A METHODS OF MEASUREMENT FOR SEMICONDUCTOR LOGIC GATING MICROCIRCUITS:

JEDEC Council

JEP 78 RELATIVE SPECTRAL RESPONSE CURVES FOR SEMICONDUCTOR INFRARED DETECTORS:

Displayed by key words

TEMPORARILY REMOVED

A

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AC

Accelerated Moisture Resistance

Accelerated Test

Acceleration Factor

Acceleration Models

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[JESD 22-A102-C](#)

[JESD 22-A118](#)

[JEP 119A](#)

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[JESD 85](#)

[JESD 91-A](#)

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Beaded

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[MS 034-B](#)

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[JESD 22-A108-B](#)

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Bias

Bias Life

Bias Life State-State Temperature Humidity

BIC

BiCC

BiCMOS

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Self-Refresh

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Ultra Thin

ULTRA-THIN

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[Design 4.15-B](#)[EIA 306](#)[MO 236-A](#)[MO 248-B](#)[MO 252-A](#)[MO 255-A](#)[JESD 92](#)[JESD 22-A118](#)[MODULE 4_5_3](#)[MODULE 4_05_10](#)[MODULE 4_20_03](#)[MODULE 4_5_11](#)[MODULE 4_20_06](#)[PR N04-NM7](#)[MODULE 4_05_14](#)[PR N03-NM9](#)[MODULE 4_20_09](#)[PR N04-NM6](#)[MODULE 4_20_05](#)[MODULE 4_20_08](#)[JESD 37](#)[JESD 24- 5](#)

JEP 95 AUS

JESD 21-C AUS

User Notification

[JESD 46-B](#)

uTSOP

[PR N04-SR1](#)

V

Values - Device Specifications

[JESD 419-A](#)

Values - Small Signal and Regulator Diodes

[JESD 482-A](#)

Vector Network Analyzer

[JEP 147](#)

Vertical Power MOSFETs

[JESD 24- 3](#)

Very Thin

[MO 211-C](#)

[MO 220-D](#)

[MO 187-D](#)

[MO 241-B](#)

[MO 250-A](#)

Very Very Thin

[MO 217-B](#)

[MO 229-C](#)

[MO 220-I](#)

[MO 250-A](#)

[MO 252-A](#)

[MO 255-A](#)

VFBGA

VHF

[EIA 306](#)

Vibration

[JESD 22-B103-B](#)

Voltage

[EIA 435](#)

Voltage Regulator Diodes

[JESD 5](#)

Voltage-Variable-Capacitance

[JESD 381-A](#)

VREF

[PR N04-DR18](#)

[PR N04-DR19](#)

W

Wafer Level

[JEP 119A](#)

Wafer Level Electrical Testing

[JEP 128](#)

Wafer Level Reliability

[JP 001.01](#)

Wafer-Level Testing

[JESD 35-A](#)

[JESD 35-1](#)

[JESD 35-2](#)

Wavesolder

[JESD 22-A111](#)

WCSP Logic

[JESD 75-4](#)

Wearout

[JP 001.01](#)

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[JESD 76-1](#)

Wide Range - Power Supply Voltage

[JESD 8- 5](#)

[JESD 8- 7](#)

Wire Bond Shear

[JESD 22-B116](#)

Wire Bond Type Chip

[JESD 51- 4](#)

Wireless

[JESD 96](#)

Wires

[J-STD- 002B](#)

Withstand Time - Short Circuit

[JESD 24- 9](#)

Word Wide

[EEPROM 3_05_02](#)[SRAM 3_07_07](#)[SRAM 3_07_08](#)[DRAM 3_9_4](#)[SDRAM 3_11_04](#)[MPDRAM 3_10_3](#)[PROM 3_3_3-4](#)[ROM 3_2_2](#)[PR N03-NM12](#)[PR N04-DR22](#)

Word Wide Graphics

Word Wide PROM

Word Wide ROM

Write Protect

Write to Read Timing

X

X-DSBGA

[MO 207-I](#)

x16

XBGA

[MO 149-F](#)[MO 195-C](#)

XFBGA

[MO 221-C](#)**Z**

ZIP

[MODULE 4_4_1](#)**MISCELLANY**

0.3 V

[JESD 8-B](#)

0.80 mm pitch

[MO 219-E](#)

1-Bit

[JESD 75-5](#)

1.2 V

[JESD 76-1](#)[JESD 8-16](#)

1.5 V

[JESD 76-3](#)

1.5 V Interface

[JESD 8-11](#)

100 Pin

[MODULE 4_4_8](#)[MODULE 4_20_09](#)

112 pin

[MODULE 4_4_6](#)

144 Pin

[MODULE 4_5_5](#)[MODULE 4_5_6](#)[MODULE 4_5_09](#)[MODULE 4_20_03](#)[MODULE 4_5_13](#)[MODULE 4_5_8](#)[MO 214-B](#)

16 Lead

[MO 253-A](#)

16-Bit Logic

[JESD 75-2](#)

168 Pin

[MODULE 4_5_1](#)[MODULE 4_5_3](#)

172 pin

184 Pin

184-Pin

2-Bit

2.5 V

200 Pin

21C

240 pin

240-Pin

244 Pin

278 Pin

3 Leads

3-Bit

3.3 V

32-Bit Logic Functions

5 V Tolerant - CMOS Devices

54 Ball Package

64 pin

72 pin

78 Ball

8 lead

8-Bit

8.89 mm Body

80 Pin

[MODULE 4_5_13](#)[MODULE 4_5_07](#)[MODULE 4_20_02](#)[MO 214-B](#)[MODULE 4_05_10](#)[MODULE 4_20_05](#)[MODULE 4_20_04](#)[MODULE 4_5_11](#)[MODULE 4_5_12](#)[MO 206-D](#)[MODULE 4_20_07](#)[MODULE 4_20_08](#)[JESD 75-5](#)[JESD 8- 9B](#)[MODULE 4_5_2](#)[MO 224-B](#)[TOC21C](#)[SO 001-B](#)[MODULE 4_05_14](#)[MO 244-A](#)[SO 002A](#)[MODULE 4_6_1](#)[TO 273-B](#)[JESD 75-5](#)[JESD 8-B](#)[JESD 75](#)[JESD 36](#)[JESD 75-1](#)[MODULE 4_4_1](#)[MODULE 4_4_1](#)[MODULE 4_4_2](#)[MODULE 4_4_4](#)[PR N04-DR12](#)[MO 240-A](#)[JESD 75-3](#)[MODULE 4_4_7](#)

Displayed by revision status

EIA 283	TEST METHOD FOR TRANSISTOR NOISE FIGURE MEASUREMENTS AT MEDIUM FREQUENCIES - SUPERSEDED BY EIA-311-A. November 1963; Rescinded November 1981
EIA 318-1	ADDENDUM No. 1 to EIA-318 - CHARACTERIZATION OF A REVERSE TEST FIXTURE: SUPERSEDED BY EIA-318-B, July 1996. February 1981; Rescinded
EIA 428-A	TYPE DESIGNATION SYSTEM FOR MICROELECTRONIC DEVICES October 1988; Rescinded September 1993
JEB 17	USER GUIDELINES FOR QUALITY AND RELIABILITY ASSURANCE OF LSI COMPONENTS November 1970; Rescinded April 1987
JEB 20	ACCEPTED PRACTICES FOR MAKING MICROELECTRONIC DEVICE THERMAL CHARACTERISTICS TESTS January 1975; Rescinded November 1988
JEB 6	STANDARD MEASUREMENTS OF THE ELECTRICAL CHARACTERISTICS OF SEMICONDUCTOR INTEGRATED CIRCUITS December 1966; Rescinded
JEP 100	TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR MICROCOMPUTERS AND MEMORY INTEGRATED CIRCUITS: ELEVATED TO JESD100, August 1993. September 1979; Rescinded October 1983
JEP 102	STANDARD FOR 64K x 1 DYNAMIC RAM - SUPERSEDED BY JESD21-C. September 1978; Rescinded April 1985
JEP 105	JEDEC GUIDELINE FOR THE CHARACTERIZATION OF HYBRID POLYMERIC MATERIALS - SUPERSEDED BY JESD72, June 2001 April 1983; Rescinded June 2001
JEP 107	TEST METHOD FOR QUALIFICATION AND ACCEPTANCE OF PARTICLE GETTERS FOR USE IN HYBRID MICROELECTRONIC APPLICATIONS - SUPERSEDED BY JESD72, June 2001 April 1985; Rescinded June 2001
JEP 108-B	DISTRIBUTOR REQUIREMENTS FOR HANDLING ELECTROSTATIC - DISCHARGE SENSITIVE (ESDS) DEVICES: SUPERSEDED BY JESD42, March 1994. April 1991; Superseded
JEP 109-C	GENERAL REQUIREMENTS FOR DISTRIBUTORS OF MILITARY SEMICONDUCTOR DEVICES: March 1995; Rescinded November 2001

JEP 111	TEST PROCEDURES FOR CUSTOM MONOLITHIC MICROCIRCUITS - SUPERSEDED BY MIL-PRF-38535C. July 1986; Rescinded June 1996
JEP 112	TEST METHOD FOR QUALIFICATION AND ACCEPTANCE OF CIRCUIT SUPPORT FILMS FOR USE IN MICROELECTRONIC APPLICATIONS - SUPERSEDED BY JESD72, June 2001 June 1987; Rescinded June 2001
JEP 117	GUIDELINES FOR USER NOTIFICATION OF PRODUCT/PROCESS CHANGES BY SEMICONDUCTOR SUPPLIERS - SUPERSEDED BY JESD46, August 1997. April 1994; Rescinded July 1994
JEP 124	GUIDELINES FOR THE PACKING, HANDLING, AND REPACKING OF MOISTURE-SENSITIVE COMPONENTS - SUPERSEDED BY J-STD-033, May 1999. December 1995; Rescinded November 1999
JEP 74	STANDARD LIST OF VALUES TO BE USED IN POWER TRANSISTOR DEVICE REGISTRATION AND MINIMUM DIFFERENCES FOR DISCRETENESS OF REGISTRATIONS - SUPERSEDED BY EIA-419-A, February 1996. July 1969; Rescinded February 1996
JEP 75	LETTER SYMBOLS USED WITH INFRARED DEVICES - INCORPORATED INTO JESD77-A. August 1984; Rescinded August 1984
JEP 86-A	RECOMMENDED PRACTICE FOR DUAL DIMENSIONING May 1976; Rescinded November 1999
JEP 87	FORWARD TURN-ON TIME MEASUREMENT ON SEMI-DIODES - INCORPORATED INTO EIA-282-A. June 1992; Rescinded June 1985
JEP 88	THERMAL RESISTANCE AND THERMAL IMPEDANCE TEST METHODS FOR STUD AND BASE-MOUNTED RECTIFIER DIODES AND THYRISTORS January 1974; Rescinded June 1992
JEP 90	THERMAL RESISTANCE FOR TEST METHODS FOR SIGNAL DIODES - SUPERSEDED BY EIA-531, July 1986. See JESD531, April 2002. September 1983; Rescinded September 1986
JEP 93	MICROELECTRONIC DEVICE TYPE ASSIGNMENTS August 1975; Rescinded June 1992
JEP 96	GUIDELINES FOR NONDESTRUCTIVE PULL TESTING OF WIRE BONDS ON HYBRID DEVICES

March 1977; Rescinded April 2000

JEP 99	GLOSSARY OF MICROELECTRONIC TERMS, DEFINITIONS, AND SYMBOLS: ELEVATED TO JESD99, June 1985. July 1977; Rescinded June 1985
JESD 17	LATCH-UP IN CMOS INTEGRATED CIRCUITS - SUPERSEDED BY JESD78, February 1999 August 1988; Rescinded February 1999
JESD 19	GENERAL STANDARD FOR STATISTICAL PROCESS CONTROL (SPC) - SUPERSEDED by EIA-557-A July 1988; Rescinded July 1995
JESD 22-A112-A	MOISTURE-INDUCED STRESS SENSITIVITY FOR PLASTIC SURFACE MOUNT DEVICES - SUPERSEDED BY J-STD-020A, April 1999. November 1995; Rescinded May 2000
JESD 22-C100-A	HIGH TEMPERATURE CONTINUITY - RESCINDED, November 1999 April 1990; Rescinded November 1999
JESD 26-A	GENERAL SPECIFICATION FOR PLASTIC ENCAPSULATED MICROCIRCUITS FOR USE IN RUGGED APPLICATIONS - RESCINDED, July 2001 April 1990; Rescinded July 2001
JESD 29-A	FAILURE-MECHANISM-DRIVEN RELIABILITY MONITORING - SUPERSEDED BY EIA/ANSI-659, July 1996. July 1996; Superseded July 1996
JESD 39-A	QUALITY SYSTEM ASSESSMENT - SUPERSEDED BY ANSI/EIA-670, June 1997. June 1997; Superseded
JESD 41	REVERSE RECOVERY CHARACTERISTICS OF SILICON DIODES: Rescinded June 2002. May 1995; Rescinded June 2002
JESD 42	REQUIREMENTS FOR HANDLING ELECTROSTATIC-DISCHARGE- SENSITIVE (ESDS) DEVICES - SUPERSEDED BY EIA-625, November 1994. March 1994; Superseded
JESD 43	COMPONENT PROBLEM ANALYSIS AND CORRECTIVE ACTION REQUIREMENTS - SUPERSEDED BY EIA-671, November 1996. November 1996; Superseded
JESD 45	MEASUREMENT METHOD FOR THERMAL RESISTANCE OF BRIDGE RECTIFIER ASSEMBLIES: Rescinded June 2002. Replaced by JESD282-

B.
December 1994; Rescinded June 2002

JESD 53 MANAGEMENT OF COMPONENT OBSOLESCENCE BY GOVERNMENT
CONTRACTORS: Rescinded, October 2002
January 1996; Rescinded October 2002

TENTSTD 11 HANDLING AND INSTALLATION OF POWER SEMICONDUCTORS IN DISC
TYPE PACKAGES: Included in JESD282 and EIA397.
July 1973; Rescinded June 1992

MO 177-A Registration - Rescission of 200 Pin Small Outline Dual-In-Line Memory
Module (DIMM) Family, 0.65 mm Pitch. Item 11.14-044.
June 1999; Rescinded June 2001
