

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner

Patent No. 10,474,595

Issued: November 12, 2019

Filed: December 28, 2017

Inventors: Hyun Lee

Title: Memory Module Having An Open-Drain Output Pin For Parity Error
In a First Mode and For Training Sequences In A Second Mode

Inter Partes Review No. IPR2022-00064

**PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 10,474,595**

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Attachment A. Proof of Service of the Petition

Attachment B. List of Evidence and Exhibits Relied Upon in Petition

Attachment C. Table of Claims and Elements

I. PETITIONER’S MANDATORY NOTICES

A. Real Parties-in-Interest (37 C.F.R § 42.8(b)(1))

The real parties in interest are the Petitioner, Samsung Electronics Co., Ltd.; and Samsung Semiconductor, Inc.

B. Related Matters (37 C.F.R § 42.8(b)(2))

The following judicial or administrative matters would affect, or be affected by, a decision in this proceeding concerning U.S. Patent No. 10,474,595.

The following proceedings are currently pending:

- *Samsung Electronics Co., Ltd. v Netlist, Inc.*, IPR2022-00062
- *Samsung Electronics Co., Ltd. et al. v Netlist, Inc.*, No. 1:21-cv-01453 (D. Del. filed Oct. 15, 2021)

The following proceedings are no longer pending:

- *SK hynix Inc., et al v Netlist, Inc.*, IPR2020-01042
- *Netlist, Inc. v. SK hynix Inc. et al.*, Case No. 6:20-CV-00194 (W.D. Tex.)
- *SK hynix Inc., et al v Netlist, Inc.*, IPR2020-01044
- *Netlist, Inc. v. SK hynix Inc., et al*, Case No. 8:17-cv-01030 (C.D. Cal.)

- *In the Matter of Certain Memory Modules and Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1089 (International Trade Commission)
- *SK hynix Inc., et al v Netlist, Inc.*, IPR2018-00303
- *Netlist, Inc. v. SK hynix Inc., et al*, Case Nos. 8:16-cv-01605 (C.D. Cal.)
- *In the Matter of Certain Memory Modules and Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1023 (International Trade Commission)
- *SK hynix Inc., et al. v Netlist, Inc.*, IPR2017-00548

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D. Service Information (37 C.F.R. § 42.8(b)(4))

Service information is provided in the designation of counsel above.

Petitioner consents to service of all documents via electronic mail to

DLSamsungNetlistIPRs@BakerBotts.com.

II. INTRODUCTION

Petitioner respectfully requests trial on claims 1-24 of U.S. Patent 10,474,595 (“595 Patent”)(EX1001) based on the obvious combination of Hazelzet with either JEDEC or Buchmann, and optionally with Kim. The Board previously instituted trial on the same claims based on the same grounds. EX1059 (IPR2020-01042, Paper 14). That IPR was terminated due to settlement shortly after institution, however. EX1060. Petitioner was not involved in the previous IPR and had no reason to join that IPR. This Petition and the supporting expert declaration by Dr. Alpert are substantially similar to what the Board previously considered when it previously instituted trial, and thus for similar reasons trial should be instituted here. In addition, as the Board has already determined, “the

Board's decision in IPR2018-00303 finding similar claims in [a] related patent unpatentable over the same prior art (Hazelzet and Buchmann) signals that the merits in this proceeding favor Petitioner." EX1059, 17.

III. COMPLIANCE WITH REQUIREMENTS FOR A PETITION FOR INTER PARTES REVIEW

A. Certification The Patent May Be Contested By Petitioner

Petitioner certifies that the 595 Patent is available for IPR and that Petitioner is not barred or estopped from requesting an IPR challenging the 595 Patent claims on the grounds identified below.

B. Fee for Inter Partes Review (§ 42.15(a))

The Director is authorized to charge the fee specified by 37 C.F.R. § 42.15(a) to Deposit Account No. 02-0384.

C. Proof of Service (37 C.F.R. §§ 42.6(e), 42.105(a))

Proof of service of this petition is provided in **Attachment A**.

IV. IDENTIFICATION OF CLAIMS BEING CHALLENGED

Claims 1-24 of the 595 Patent are unpatentable as follows:

- (i) Claims 1-24 are obvious in view of Hazelzet and JEDEC;
- (ii) Claims 1-24 are obvious in view of Hazelzet and Buchmann;
- (iii) Claims 3-7, 12-14, 20, 22, and 23 are obvious in view of Hazelzet, JEDEC or Buchmann, and Kim.

Petitioner's proposed claim constructions, the evidence relied upon, and the precise reasons why the claims are unpatentable are provided below. The evidence relied upon in this petition is listed in **Attachment B**.

V. RELEVANT INFORMATION CONCERNING THE CONTESTED PATENT

A. Effective Filing Date Of The 595 Patent

The 595 Patent is a continuation of, *inter alia*, a utility application filed June 14, 2010, and also claims priority to U.S. Provisional Application No. 61/186,799 (EX1008), filed June 12, 2009. EX1001, Face. The claims of the 595 Patent are **not**, however, entitled to the June 2009 date for multiple reasons, discussed below, which the Board agreed with in IPR2020-01044. EX1059, 27.

1. Unsupported Negative Limitation

Each independent claim of the 595 Patent requires the negative limitation that the memory controller not access the module for memory read and write operations in a training mode, that is, a mode that includes training sequences (in some claims referred to as the "second mode"). *E.g.*, EX1001, 14:63-65 (claim 1: "wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations"), 16:19-22 (claim 10), 17:41-44 (claim 17), 18:42-46 (claim 21); EX1003, ¶44.

For the claims of the 595 Patent to be entitled to the benefit of the provisional's filing date, the provisional must provide written description support

for those claims, including for that negative limitation. 35 U.S.C. §§ 119(e), 112(a). To meet that standard, Patent Owner must show¹ from the disclosure of the provisional that the inventor was in “possession” of the invention, which means that “the written description must include all of the limitations of the [claims], or the applicant must show that any absent text **is necessarily comprehended** in the description provided and would have been so understood at the time the patent application was filed.” *Hyatt v. Boone*, 146 F.3d 1348, 1354-55 (Fed. Cir. 1998).²

Patent Owner cannot make that showing. The provisional says nothing about the memory controller not accessing the module for read and write operations in training mode. Indeed, it mentions the word “training” in only one sentence fragment, never explains that such training may occur in its own mode, never uses the word “mode” at all, and never says anything about what operations may or may not occur in training mode. EX1003, ¶45.

Nor can Patent Owner show that the negative limitation “is necessarily comprehended” in the provisional’s disclosure. The 595 Patent itself states that

¹ *Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378-81 (Fed.Cir. 2015) (Patent Owner bears burden to show entitlement to provisional filing date).

² All emphasis in bold in this document has been added.

both memory controller memory operations and training sequences can occur during an initialization mode, confirming that both can occur during the same mode. EX1001, 6:26-30, 6:45-56; EX1003, ¶46.

As noted, only a sentence fragment of the provisional mentions “training”: “Error-Out pin: Low during MB **training** (high signal indicates that **training** is done).” EX1008, 25. A person of ordinary skill in the art in the field of the 595 Patent in the 2009-10 time frame (“Skilled Artisan”) would understand “MB training” as a generic reference to “training” in the context of memory buffers. To the extent one might argue it refers to something more specific, a Skilled Artisan would, at most, understand the phrase in the context of the provisional’s references to “the recent proposal in JEDEC for L[R]-DIMM (Load Reduced DIMM)” which was under development/standardization at the time. EX1008 at 22. Although the provisional does not identify the specific JEDEC “proposals,” a Skilled Artisan would have understood at the time that JEDEC was evaluating proposals for the training of the interfaces to/from and/or operations of the type of register/buffer used in DDR3 LRDIMMs. EX1036, 4; EX1039, 2; EX1003, ¶47.

It was known, however, that such buffers could employ normal memory read and write operations instituted by the memory controller during training. EX1015, 8-9 (“The host performs normal writes to DRAM for write DQ/DQS margining ...[t]he host performs read DQ/DQS margining by using normal reads from DRAM

...”); EX1039, 10-11 (disclosing “Host-MB Training” before June 12, 2009 provisional filing date); EX1022,¶¶[0039],[0043],[0053] (employing normal read/write operations during training); EX1003,¶48. Thus, Patent Owner cannot show from the provisional’s disclosure that the negative limitation that no normal memory read and write operations occur in the training mode “is necessarily comprehended” in that disclosure because it was known that some types of “MB training” did in fact include normal memory read and write operations.³

2. “One or More” Training “Sequences”

Each independent claim of the 595 Patent also requires the ability to “perform operations related to ***one or more*** training ***sequences***.” EX1001, claim 1, claim 10, claim 17, claim 21. EX1003,¶51. The independent claims also require providing information or signals “related to the one or more training sequences.” *Id.* The provisional, however, only discloses “MB training,” that a Skilled Artisan would understand as a generic disclosure of “training” a memory buffer in some way. EX1003,¶52. The provisional also mentions “initialization operation

³ Only claim 1 includes the qualifier “normal” before “memory read or write operations” in the negative limitation. However, if it was known that “normal memory read or write operations” occur in some training modes, it was necessarily known that memory read and write operations did too.

sequences,” but that is just a generic description of initialization. EX1008, 22. It does not disclose any training “sequences,” and particularly not “one or more” training sequences, much less providing information or signals related to such specific “training sequences.”

3. “one or more N-bit-wide data signals”

Claim 21 requires “wherein the [DRAMs] are configurable to communicate one or more N-bit-wide data signals with the memory controller ..., where N is at least 32.” EX1001, 18:31-35. However, DRAM is mentioned just once in the provisional: “This method allows the MCH to work with a non-homogenous memory subsystem, such as mixing of DIMMs with different DIMM density, ranks, DRAM density, speed, DRAM configuration, etc.” EX1008, 23. The terms “data signal,” “bit,” “width,” and “32” are found nowhere in the provisional, much less the concept of data signals of a certain width, particularly “at least 32.” There is no support for this limitation. Nor is it necessarily the case that a DRAM of a module employ 32-bit wide data signals. EX1003, ¶53.

4. “one or more pins that are not active”

Claims 8, 15, 16, 18, and 19 require that “the second edge connections [for address and command] include one or more pins that are not active while the memory module is in the second mode,” or substantially similar “pins not active” limitations. EX1001, 15:51-53, 17:7-13 (claims 15-16), 17:49-56 (claims 18-19).

However, the terms “edge,” “edge connection[s],” “mode” and “active” appear nowhere in the provisional, much less the concept that pins [for address and command] on an edge connection are not active during certain modes, and those concepts are not necessarily comprehended in that disclosure. EX1003,¶54.

The claims of the 595 Patent are accordingly entitled to a priority date no earlier than **June 14, 2010**, as the Board agreed in IPR2020-01044. EX1059, 27.

B. Person Of Ordinary Skill In The Art

A Skilled Artisan would have had a bachelor’s degree in computer engineering, or a related field, and several years of additional experience working with computer memory systems. She would have been familiar with computer memory systems and basic CPU architecture documented in the literature, including standards, and generally available in commercial systems, including how computer components access a computer’s memory, the role of a memory controller, the basic operation of memory modules and devices, and the techniques used to couple memory devices to the other components of the computer system. EX1003,¶55.

C. The 595 Patent

1. Technical Overview

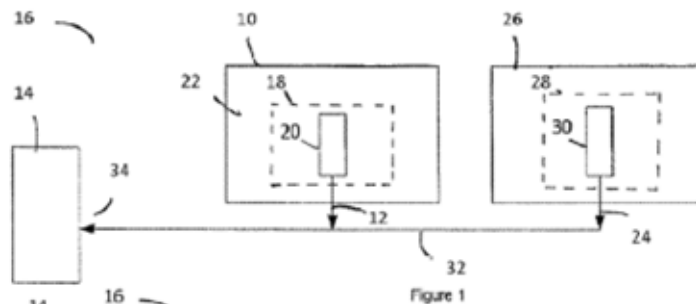
The 595 Patent describes “a method of establishing a handshake mechanism based on notification signaling” that “can be implemented by adding a new interface (notifying) signal between the MCH [*i.e.*, system memory controller] and

the memory subsystem controller,” EX1001, 4:5-12, and that this interface “can be an open drain signaling from the memory subsystem controller to the MCH.”

EX1001, 4:12-16.

The 595 Patent states that “typical” servers of the prior art had “complete control over initialization” and did not need handshaking, or would simply wait a predetermined amount of time and then assume the memory subsystem had completed initialization. EX1001, 2:64-3:22.

Figure 1 shows a computer system including memory module 10 coupled to a memory controller 14 via “output 12” which is driven by notification circuit 20 of controller circuit 18.



EX1001, 4:24-42, FIG. 1. Memory module 26 is also shown, and has essentially the same structure as module 14, having “output 24” driven by notification circuit 30 of controller circuit 28. *Id.*, 6:23-44.

In one specific example of handshaking, the interface between the memory controller (MCH) and memory subsystem controller is implemented using a technique called open drain signaling. EX1001, 4:12-16, 9:47-53, FIGs. 2-3.

Specifically, output 12 of module 10 and output 24 of module 26 are both tied to the same bus 32 using an open drain configured transistor. *Id.*

In that configuration, when starting an initialization procedure, each memory module will drive the gate of the transistor of its open drain output high, placing a logic level low (low impedance) signal on bus 32. When the initialization is complete, the memory module can drive the gate of the transistor, placing a logic level high (high impedance) signal on bus 32. However, because all of the outputs of multiple memory modules are tied to the same bus 32 in an open drain configuration, the state of bus 32 will remain logic level low (low impedance) until each memory module drives the gate of the transistor of its open drain output low, placing a logic level high (high impedance) on its output, which then allows “the bus 32 [to] be pulled high by the internal pull-up configuration 40 of the system memory controller 14.” EX1001, 9:47-10:50. In this manner, the system memory controller may be provided the status of an initialization procedure (*e.g.*, either that it is currently executing or complete) using only a single bus line from multiple memory modules. *Id.*

The 595 Patent further states that bus 32 could be tied to a standard-defined (such as JEDEC) error output pin that is not required by the standard to be used during initialization. EX1001, 8:4-33. EX1003, ¶61. The patent states that output 12 can be operatively coupled to the error-out pin of memory module 10, which is

connected to a multiplexor 42 driving the transistor 36 with either of a task_in_progress signal 44 or an error signal 46 (*e.g.*, parity error signal). EX1001, 11:19-23, FIG. 3. According to the 595 Patent, “the memory module 10 can be advantageously configured to both perform the standard (*e.g.*, JEDEC-specified) error reporting functionality via the error-out pin during the operational mode and provide the status notification functionality during the system initialization mode.” EX1001, 11:29-34.

2. **Prosecution History**

The 595 Patent is a continuation, through two intervening applications, of U.S. Patent 8,489,837 and has the same specification as the 837 Patent. EX1001. The 837 Patent claimed the technique of using a single open drain output to provide parity error information in an operational mode and status information in an initialization mode. *Id.* The Board found the basic claims of the 837 Patent to be unpatentable in IPR2017-00548. EX1035, 16.

U.S. Patent No. 9,535,623 is a continuation, through three intervening applications, of the 837 Patent and has the same specification as the 595 Patent. EX1031. The 623 Patent claimed the technique of using a single open drain output to provide parity error information in an operational mode and status information in a training mode. *Id.* In IPR2018-00303, the Board found all claims of the 623 Patent unpatentable over Hazelzet in view of Buchmann. EX1034, 22.

The 595 Patent issued from U.S. Patent Application 15/857,553. The claims were rejected “on the ground of nonstatutory double patenting as being unpatentable over claims 1-18” of the 837 Patent, EX1002, 83, requiring Patent Owner to file a terminal disclaimer to overcome the rejection, *id.*, 106.

Patent Owner likewise filed a terminal disclaimer over the 837 Patent when prosecuting the application that became the 623 Patent. EX1038, 79(disclaiming over application that issued as ‘218 patent, which disclaims over the ‘837 patent); EX1005, 61.

On March 1, 2019, the applicants filed a RCE and an Amendment amending the claims to remove the term “handshake” from all claims and add other terms. EX1002, 149, 151. After a second notice of allowance, EX1002, 182-183, the applicants filed another RCE, and amended and added claims, including adding for the first time the phrase “**normal** memory read and write operation” to certain claims and to the Abstract. EX1002, 222-233, 240. On August 9, 2019, the examiner issued a third notice of allowance. EX1002, 243-244.

In IPR2020-01042, the Board instituted review of the 595 Patent based on the same references and grounds asserted in this petition, but IPR2020-01042 settled before the Final Written Decision. EX1059, 45; EX1060; EX1003, ¶106.

3. 35 U.S.C. §§ 314(a), 325(d)

Discretionary denial of institution is not warranted for several reasons.

First, the Board should not deny institution under *Advanced Bionics* and §325(d) given that the Board previously instituted trial in IPR2020-01042 on the same grounds asserted in this petition. EX1059. The Board previously considered extensive evidence that the grounds asserted in this petition are not substantially the same as those before the examiner of the 595 Patent, and that the examiner clearly erred in issuing the 595 Patent. EX1058, 16–18. For example, the JEDEC reference used in this petition was not considered during prosecution, and the examiner did not address the Final Written Decision in IPR2018-0303 (EX1034) which found related claims invalid based on the same combination raised here. Given the prior institution in IPR2020-01042 and the similarity between the petitions, there is no basis for a different result here.

Second, Petitioner was not involved in IPR2020-01042 that was instituted on the same grounds, and Petitioner had no reason to join that IPR before it was terminated due to settlement, so discretionary denial under the *General Plastic* factors is not warranted. The petitioner in IPR2020-01042 was SK hynix, which is unrelated to Samsung, the Petitioner here. When SK hynix filed the petition in IPR2020-01042, Samsung had a license to the 595 Patent from Patent Owner, and thus had no reason to join that IPR before it was terminated on May 6, 2021. EX1063, 2 (announcing license in 2015). Patent Owner recently filed a breach of contract action arguing that Samsung’s license has been terminated, but Samsung

moved to dismiss that action in June 2021 and has argued that the license remains in force. EX1064. On August 5, 2021, the judge denied Samsung's motion to dismiss, EX1065, and then Patent Owner moved for summary judgment that Samsung's license has been terminated, EX1066. As a result of this change in circumstances, Samsung now has a reason to raise the same grounds raised in IPR2020-01042, whereas during the pendency of IPR2020-01042 Samsung did not.

In light of the facts above, the fifth *General Plastic* factor weighs against discretionary denial because Petitioner had a legitimate reason for not filing sooner. The timing of this petition is "directly related to Patent Owner's litigation activity" against the prior and present petitioners and "any potential prejudice to Patent Owner in having to respond to multiple petitions is outweighed by actual prejudice to Petitioner if institution is denied based on this Petition" because the proceeding in the previously-instituted IPR has been terminated due to the parties settling. *Google LLC v. Uniloc 2017 LLC*, IPR2020-00396, Paper 11, at 16 (PTAB Aug. 3, 2020). In addition, it is clear that Petitioner here did not "wait[] to file the Petition to gain an unfair advantage." *Unified Patents, LLC v. Oceana Innovations LLC*, IPR2020-01463, Paper 11, at 13 (PTAB Feb. 23, 2021) (granting institution). There was simply no reason for Petitioner to file an IPR against Patent Owner at the time that SK hynix filed its petition in IPR2020-01044.

Furthermore, the first *General Plastic* factor “weigh[s] **overwhelmingly** against a discretionary denial in this proceeding” given that Samsung and SK hynix are competitors and were not co-defendants. *Unified Patents Inc. v. Bradium Technologies LLC*, IPR2018-00952, Paper 31, at 20 (PTAB Dec. 20, 2018). The overlapping nature of the references and arguments between the earlier filed and instant petitions is not enough to create a significant relationship between the prior and present petitioners. *See, e.g., Sony Mobile Communications AB v. Ancora Technologies, Inc.*, IPR2021-00663, Paper 17, at 10 (PTAB June 10, 2021) (finding no “significant relationship” between petitioners because “Patent Owner sued Petitioner . . . separately from its competitors”); *Google LLC*, IPR2020-00396, Paper 11, at 11 (same); *Prollenium US Inc. v. Allergan Industrie, SAS*, IPR2019-01505, Paper 18, at 43–44 (PTAB Mar. 19, 2020) (finding no “significant relationship,” even though petitioner relied on overlapping references with earlier petition, because “this is Prollenium’s first Petition, and Prollenium has no connection to the prior petitioner”). In fact, finding a significant relationship based merely on parallel arguments in petitions would unfairly allow a Patent Owner to inoculate invalid patents from review simply by settling with one petitioner after institution and then seeking discretionary denial if subsequent petitioners seek to rely upon the same successful invalidity arguments. *See Google LLC*, IPR2020-00396, Paper 11, at 16 (considering unfair prejudice to petitioner).

Finally, the sixth and seventh *General Plastic* factors weigh against discretionary denial because there is no longer any IPR pending against the 595 Patent, and the grounds raised here are the same as those in the previous institution so the Board need not expend any additional resources to institute trial here, *see* EX1059.

There is also no basis for a discretionary denial under *Fintiv* and §314(a) because the only parallel, co-pending proceeding between the parties was only recently filed by Petitioner and requests a declaratory judgment of non-infringement, not of invalidity. *See* EX1067.

D. Construction Of Terms Used In The Claims

Claim terms are generally given their ordinary meaning in the context of the patent as understood by a Skilled Artisan. 37 C.F.R. § 42.100(b); *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-13 (Fed.Cir. 2005) (en banc). If Patent Owner contends claim terms should have a special meaning, those contentions should be disregarded unless Patent Owner successfully amends the claims compliant with 35 U.S.C. § 112 to make them expressly correspond to those contentions. 77 Fed. Reg. 48,764 at II.B.6 (August 14, 2012); *cf. In re Youman*, 679 F.3d 1335, 1343 (Fed.Cir. 2012).

1. “memory read or write operations”

In the context of the 595 Patent, a Skilled Artisan would understand the ordinary meaning of “*memory read or write operations*” to be operations used to communicate data between the memory module and the memory controller in response to commands from the memory controller. EX1001, 1:57-61, 5:45-52, 16:26-33; EX1003, ¶¶110-113.

In IPR2020-01042, the Board declined to construe “*memory read or write operations*.” EX1059, 29-30. Regardless, as explained in §VII, the prior art invalidates the 595 Patent. EX1003, ¶114.

2. **“normal memory read or write operations”**

In the context of the 595 Patent, a Skilled Artisan would understand the ordinary meaning of “*normal memory read or write operations*” to be the same as “*memory read or write operations*.” EX1003, ¶115. The phrase “normal memory read or write operations” was added by an amendment, EX1002, 224, 240, in which “[n]o new matter has been added,” *id.*, 233. Thus, any difference in scope between these two terms have been disclaimed. *Kraft Foods, Inc. v. Int’l Trading Co.*, 203 F.3d 1362, 1366-69 (Fed.Cir. 2000); EX1003, ¶¶115,116-117.

In the alternative, the phrase should be construed to mean standard operations used by the memory controller to read from or write to memory devices, whether or not they occur in a normal operating mode of a module, in accordance with the express disclosure of the specification. EX1001, 6:45-56;

EX1003,¶¶118,119,120. This interpretation is also confirmed by the prosecution history, including the parent 837 Patent, which was the subject of IPR2017-00548. *Aylus Networks, Inc. v. Apple Inc.*, 856 F.3d 1353, 1360-61 (Fed.Cir. 2017); *Microsoft Corp. v. Multi-Tech Sys.*, 357 F.3d 1340, 1349-1350 (Fed.Cir. 2004); EX1003,¶122.⁴ During the course of that proceeding, Patent Owner’s expert conceded that memory commands that can be used during initialization would be considered “normal memory commands,” EX1021, 24:24-25:18, and “normal read and writes” can be used in non-normal modes, such as boot-down sequences, *id.*, 17:24-18:11. EX1003,¶123.

In IPR2020-01042, the Board declined to construe “*normal memory read or write operations*.” EX1059, 29-30. Regardless, as explained in §VII, the prior art invalidates the 595 Patent. EX1003,¶124.

Patent Owner may argue that the claimed “*normal memory read or write operations*” should be construed as limited to operations that occur outside of any training, but that would be inconsistent with the intrinsic record that confirms such memory operations can occur in non-normal modes, and it would also read the negative limitation “the memory module in the [training] mode is not accessed by

⁴ The documents from that IPR cited here were also provided to the examiner of the 595 Patent, so are intrinsic evidence for that reason as well.

the memory controller for normal memory read or write operations” out of each independent claim and is thus improper. *Innova/Pure Water v. Safari Water Filtration*, 381 F.3d 1111, 1119 (Fed.Cir. 2004).⁵

3. **“mode”**

During the 837 Patent IPR (and in the District Court case involving the 595 patent), Patent Owner sought to have the term “*mode*” interpreted to mean “a distinct behavioral state that a system may be switched to.” EX1035, 7. Petitioner objected for several reasons, including because it became clear that Patent Owner sought to use the word “distinct” to inject several unwarranted concepts and ambiguities into the claims, such as that different “modes” must necessarily include mutually exclusive operations, EX1041, 6, which was inconsistent with the disclosure of the 837 Patent (and thus of the 595 Patent) that the disclosed memory operations may be used in both an operational mode and an initialization mode. EX1001, 6:50-56. The Board recognized this inconsistency and accordingly declined to construe the word “*mode*.” EX1035, 7. Similarly, in IPR2020-01042, the Board declined to construe “*mode*.” EX1059, 29-30. Indeed, the intrinsic

⁵ For the same reasons, the claimed “*memory read or write operations*” are also not limited to operations actually used during standard computer operation or in any particular mode.

record never defines the term “*mode*” or uses it in any special sense, so the Board should take the same approach here. EX1003,¶¶126-130.

4. “training sequence”

In the context of the 595 Patent, a Skilled Artisan would understand the ordinary meaning of “*training sequence*” to be a set of operations occurring in a particular order and used for training. EX1003,¶131.

Generally, a “sequence” is “a set of related events, movements, or things that follow each other in a particular order.” EX1042, 2; EX1003,¶132.

The 595 Patent provides no details concerning the disclosed “training sequences,” except that they are controlled by the memory module, a module may carry out more than one, and that they may be part of the module’s “initialization sequence.” EX1001, 3:32-35, 6:19-23; EX1003,¶133.

During the 623 Patent IPR, the Board found Buchmann’s TS3 training operations satisfied the “training sequence” claimed in the 623 Patent. EX1034, 11-12. The TS3 operations are a set of operations carried out in a particular order to perform upstream lane training and repair. EX1016, 5:40-44. Indeed, Buchmann explicitly describes his different sets of training operations as “training sequences.” EX1016, 3:49-52, 14:38-41; EX1003,¶134.

In IPR2020-01042, the Board declined to construe “*training sequences*.” EX1059, 29-30. In contrast, the district court in a related case construed “*training*

sequences” to mean “operations in a particular order for preparing a memory system to perform its intended function,” EX1061, 2, which is substantially similar to Petitioner’s proposed construction here. Accordingly, the phrase “*training sequence*” should be construed to mean a set of operations occurring in a particular order and used for training. EX1003, ¶136. Either way, the prior art invalidates the 595 Patent, as explained in §VII. EX1003, ¶135.

5. **“notification signal associated with the [one or more training sequences]” / “information related to the [one of more training sequences]” / “open-drain signals related to the [one or more training sequences]”**

A Skilled Artisan would have understood that, in the context of the 595 patent, these phrases refer to unscheduled signal/information/open-drain signals provided without polling that indicate the status of the one or more training sequences. EX1003, ¶137. This interpretation is supported throughout the specification. EX1001, *e.g.*, Summary at 1:50-54 (“The memory module ... sends a first output signal via the output pin to indicate a status of the at least one initialization sequence to the memory controller.”); 3:42-4:4 (describing advantages of notification over polling); *see also, e.g.*, 4:36-42, 6:57-63, 8:34-38, 11:29-34 (disclosing unscheduled notification signals provided without polling to indicate status of training sequences).

The district court’s construction of these terms referred back to the construction of “*training sequences*,” with the rest of the phrase having its plain

and ordinary meaning, which does not encompass polling. Ex1061, 2-3. To the extent the district court's construction differs from Petitioner's proposed construction, the difference is irrelevant to the present petition because the prior art satisfies both interpretations and invalidates the 595 Patent either way, as explained below in §VII.

VI. OVERVIEW OF THE PRIOR ART

A. Hazelzet (Ex1014)

U.S. Patent Publication No. 2008/0098277 to Hazelzet ("Hazelzet") (EX1014) was filed on October 23, 2006 and published on April 24, 2008. Hazelzet is prior art under 35 U.S.C. §§102(a), (b), and (e).

Hazelzet discloses a system having multiple memory modules that operate in an "ECC mode" or a "parity mode." EX1014, ¶¶[0064],[0069]-[0070]; EX1003, ¶140. Hazelzet explains that the "ECC mode" is a mode that allows the host system to detect and correct "correctable errors" or detect "uncorrectable errors." EX1014, ¶[0069]. In ECC mode, the detected correctable errors are reported through an "/Error (CE)" output pin and uncorrectable errors are reported through an "/Error (UE)" output pin 121 (hereinafter "UE 121"). *Id.* Hazelzet explains that these two outputs are "open-drain outputs." EX1014, ¶¶[0072],[0109]; EX1003, ¶142.

Hazelzet further explains that the “parity operating mode” allows the host system to “interrogate the device to determine the error condition” of the memory module. EX1014, ¶¶[0064],[0070]. In “parity mode” the “error condition” is reported to the host “via the Uncorrectable Error (UE) line” (*i.e.*, UE 121), EX1014, ¶¶[0070],[0072],[0109]; EX1003, ¶143.

B. JEDEC Proposal (EX1015)

EX1015, entitled “LRDIMM DDR3 Memory Initialization Chapter Proposal” hereinafter “JEDEC”), is a proposal to the JEDEC JC-40.4 committee for ballot approval. EX1050, ¶7, Ex.A (also EX1015). As Julie Carlson of JEDEC testifies, JEDEC “maintains business records to document when standards are modified, balloted, and approved, and when its standards are published,” processes with which she is familiar given her twenty-three year association with the organization. EX1050, ¶¶1-3,6.

Per Ms. Carlson, on November 9, 2009, JEDEC “was approved by DDR3 MB TG (‘Task Group’) and referred to JC-40.4 to vote for ballot approval,” and that a letter ballot was distributed to committee members on November 11, 2009, with a link to JEDEC. EX1050, ¶7, Ex. B (also EX1051). A tally of votes shows that twenty-three of the most important companies in the field of computer memories voted on the proposal between November 13, 2009 and December 3, 2009. EX1050, ¶¶8-9, Ex.C, 21-22 (also EX1037) (listing companies/votes, and

explaining that tallies are business records kept in the ordinary course by JEDEC). Thus, numerous interested members of the relevant public were directly provided JEDEC in November 2009.⁶

Further, the committee members to whom JEDEC was distributed were under no obligation to maintain it as confidential. The relevant rules of JEDEC in force at the time include no such obligation, EX1048, 19-20 (chapter on “JEDEC Documents”); EX1049 (same), and Mr. Halbert, who was involved with JEDEC standards processes during that period, confirms the same, and that there was an expectation of distribution to others. EX1054, ¶11. Thus, in November 2009, JEDEC was distributed to twenty-three key members of the interested public, with no obligation of confidentiality, and with the expectation it would be freely discussed with others, including parties who were not members of JEDEC. JEDEC was therefore publically accessible as of November 11, 2009, or at least before June 13, 2010. *GoPro, Inc. v. Contour IP Holding LLC*, 908 F.3d 690, 694 (Fed.Cir. 2018).⁷

⁶ Petitioner’s affiliate was also a member of the relevant committee and received the ballot and proposal on or about November 11, 2009. EX1055, ¶7.

⁷ Ms. Carlson also testifies that “JEDEC membership is open,” and access to documents such as JEDEC provided to those who join. EX1050, ¶5. Thus, JEDEC

JEDEC is therefore prior art to the 595 Patent as a printed publication under 35 U.S.C. §102(a). In IPR2020-01042, the Board agreed. EX1059, 27. In related IPR2020-01044, the Board noted that Patent Owner did not dispute SK hynix’s assertion that JEDEC was publicly accessible by November 11, 2009. EX1062, 34.

JEDEC discloses a proposed modification to the initialization of a Memory Buffer functionality of a DDR3 LRDIMM memory module. EX1015, 1. The DDR3 LRDIMM, which JEDEC standardized at the time, “differs from RDIMMs in that ... [a] Memory Buffer (MB) buffers both address and data.” EX1036, 5. JEDEC disclosed training during an initialization mode including MB-DRAM Training that entailed at least two training sequences, Write Leveling Training and Read Enable Training, both between the Memory Buffer and the DRAMs of the module. EX1015, 8 (§6.7). JEDEC also states that “[n]o DRAM commands or control word writes (either over the Command/Address and Control buses or via SMBus) can be issued to the MB until the MB-DRAM Interface training is complete....” *Id.*; EX1003, ¶145.

In the same description of MB-DRAM Training, JEDEC states that “training

was publicly accessible as of November 11, 2009, or at least before June 13, 2010, in this additional way. *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1560, 1569 (Fed. Cir. 1988).

completion can be signaled by the assertion of ERROUT#.” EX1015, 3, 8. A Skilled Artisan would understand that “ERROUT#” refers to the parity error out pin on a JEDEC standard LRDIMM module of the time, which was used to notify the memory controller of parity errors during normal operation, a pin also referred to as ErrOut_n in other JEDEC documents defining DDR3 LRDIMMs of the time. EX1036, 1, 4 (“Product Description”), 8 (penultimate entry in table re ErrOut_n); EX1003, ¶¶146,147.

C. Buchmann (EX1016)

U.S. Patent No. 8,139,430 to Buchmann (“Buchmann”), the application for which was filed on July 1, 2008, is prior art under 35 U.S.C. §102(e). EX1003, ¶148.

Buchmann is directed to power-on initialization and testing in a memory system, such as a DIMM of DDR3 SDRAMs including a memory buffer (MB) for buffering data, address and command signals. EX1016, 1:7-9, FIGS. 1-2.

Buchmann discloses two modes of operation (*i.e.*, “SBC mode” and “high-speed mode”), EX1016, Abstract, 1:39-44; EX1003, ¶150, and also discloses executing training sequences in SBC mode. EX1016, 4:51-12:59; EX1003, ¶151.

As an example, training sequence TS0 involves “clock detection and repair,” EX1016, 5:51-53, which is training of the clock signal. EX1016, 5:66-6:50. During the TS0 training sequence, Buchmann’s memory module generates and

outputs various notification signals to the memory controller of the host system, including the status of the TS0 training sequence (*e.g.*, “TS_done,” which notifies the host that the TS0 training is “done.”). Ex. 1016, FIG. 4, 5:51-7:2.

EX1003, ¶152.

As another example, training sequence TS3 involves “upstream lane training” and is “used to perform upstream data lane training.” Ex. 1016, 8:24-47; EX1003, ¶153. During this sequence, the memory module generates and outputs notification signals to the system memory controller, including the status of the TS3 training sequence, such as “TS3_ack,” which indicates that all downstream MBs have returned the TS3a_ack SBC, and “TS_done,” which notifies the host that the TS3 training sequence is “done.” EX1016, FIG. 6, 8:24-9:18; EX1003, ¶¶153, 154.

Buchmann discloses a daisy chain arrangement among the various modules of his system, resulting in training sequence-complete signals from the memory module reaching the host only after all modules had completed the sequence. Ex. 1016, 3:49-52, 14:41-43, 16:47-50, 28:23-26. Buchmann also explains that “one or more other bus structure(s) or a combination of bus structures” may be used, including “point-to-point bus(es),” “multi-drop bus(es),” and/or “other shared or parallel bus(es).” *Id.*, 28:26-31; EX1003, ¶155.

D. The Combinations Relied on Here

As Dr. Alpert explains, the combinations analyzed here – Hazelzet/JEDEC and Hazelzet/Buchmann – are exceedingly straightforward. In each, Hazelzet's memory modules would be modified to add the functionality of buffering the data signals similar to that in the DDR3 LRDIMM of the time and an initialization mode (“*second mode*”) into which each module could be switched and which includes training sequences whose completion is reported by the memory buffer using a status signal output over an open drain output (*i.e.*, UE 121) of Hazelzet. EX1003, ¶164.

In the JEDEC combination, the training sequences would be like those described as MB-DRAM Training in JEDEC (*e.g.*, Write Leveling and Read Enable Training), EX1015, 8, and the open drain output signal would be similar to the signal output on the ERROUT# pin as described in JEDEC, *id.*, 8; EX1036, 8 (is open-drain output for parity errors during normal operation). During those training sequences, the system memory controller communicates no data with the module and performs no operations to read or write to the memory devices; the training is carried out by memory buffer (module controller) itself. EX1015, 8; EX1003, ¶165.

In the Buchmann combination, the training sequences would be like those described as TS0, EX1016, FIG. 4, 5:51-7:2, or alternatively, like those described

as TS3, EX1016, FIG. 6, 8:24-9:18. The open drain output signals would be TS0_done, in the former case, EX1016, FIG. 4, 5:51-7:2, and TS3_ack or TS3_done, in the latter case, EX1016, FIG. 6, 8:24-9:18. Buchmann does not disclose the memory controller communicating any data with the module or performing operations to read or write to the memory devices during either TS0 or TS3 sequences during initialization/power-on. EX1003, ¶166.

In either combination, the circuitry of Hazelzet's module, in particular the ECC/Parity register, would be modified to implement the training as part of an additional mode to run, for example, at initialization, to switch among modes when appropriate, and to use the UE 121 open drain output of Hazelzet to communicate the new notification signals. EX1014, ¶[0123] (initialization operations); EX1015, 3 (training occurs during initialization); EX1016, 3:49-60 (same). As explained in more detail below, Hazelzet already uses his UE 121 open drain output for two different signals in two different modes. Thus, this ECC/Parity register necessarily includes circuitry for selecting which signal to drive on the UE 121 output depending on the mode of the module. It was well within the level of ordinary skill to modify such circuitry such that it instead selected among three different signals, depending on mode, and a Skilled Artisan could have made that modification without undue experimentation and with a reasonable expectation of success. EX1003, ¶167.

Finally, these combinations would employ known open drain signaling circuitry, which necessarily included a field effect transistor having its source coupled to ground and its drain as the output. EX1017, FIGs 4&5. A Skilled Artisan would have known that in order to use open drain signaling to indicate training completion among multiple modules, as here, the open drain output would have to be configured such that the transistor output is driven low (ground) while training is still occurring and driven high upon completion. This is because, with an open drain configuration shared by multiple modules, any module can individually drive the output low, but it takes the collective action of all connected modules to drive the output high. Moreover, a Skilled Artisan would also understand that to drive the output low (which would be a low impedance state), the gate of the transistor must be high, causing the transistor to conduct and connect the drain to ground. Conversely, to drive the output high (which would be a high impedance state), the gate of the transistor must be low, turning the transistor off. This is how an open drain output works. EX1014, ¶¶[0099]; EX1017, FIGs. 4-5, 5:65-6:18; EX1003, ¶¶158-163, 168.

E. Reasons to Combine

The prior art relied on here is analogous to the 595 Patent because all are in the same field of invention – memory module design, including error detection and correction, initialization, training and the use of pins/paths for multiple purposes

during different operations/modes, EX1001, Abstract, 5:66-6:14, 8:4-48; EX1014, Abstract, ¶¶[0007],[0069]-[0070],[0123]; EX1015, 1, 3, 8; EX1016, 1:7-9, 3:49-60, 4:51-5:50, 12:60-13:41, 14:1-63, 20:20-21:19, 33:45-67; EX1017, 1:16-22, 5:49-57, 6:8-18, 11:20-34, 12:36-53, and each is reasonably pertinent to the problem addressed by that patent – increasing memory module capacity, performance, and/or reliability by sharing an output pin/path to perform multiple functions during multiple operations/modes, including initialization/training, EX1001(595 Patent) at Abstract, 5:66-6:14, 8:4-48; EX1014, Abstract, ¶¶[0007],[0069]-[0070],[0123]; EX1015, 1, 3, 8; EX1016, 1:7-9, 3:49-60, 4:51-5:50, 12:60-13:41, 14:1-63, 20:20-21:19, 33:45-67; EX1017, 1:16-22, 5:49-57, 6:8-18, 11:20-34, 12:36-53. EX1003,¶169.

Also, a Skilled Artisan would have considered each of the combinations analyzed here to be merely an arrangement of old elements with each performing the same function it had been known to perform and yielding no more than what one would expect from such an arrangement. Combining the Hazelzet, JEDEC, Buchmann and Kim disclosures would have been well within the level of ordinary skill in the art, would not have resulted in any unpredictable results. EX1003,¶170. A Skilled Artisan would have been motivated to make these combinations for at least the following reasons. EX1003,¶171.

1. Motivation to Add Training

Hazelzet emphasizes the need for “improved overall system reliability.” EX1014, ¶¶[0001]-[0004],[0007],[0042],[0044]. Given that emphasis, a Skilled Artisan would have been motivated to add training to Hazelzet because it was known that training improved memory module reliability. EX1027, 1:35-2:12; EX1025, 15-18; EX1014, ¶[0123]; EX1017, 12:36-53; EX1003, ¶172.

Further, the Provisional admits that DDR3 LR-DIMMs and initializing LR-DIMMs were known at the time. EX1008, 22 (describing “recent proposal in JEDEC for L[R]-DIMM (load Reduced DIMM) requires the MCH to hand over one or more parts of the initialization operation sequences to the memory subsystem controller”). Although Hazelzet discloses a Registered DIMM (RDIMM), it would have been obvious to update Hazelzet’s RDIMM to a LR-DIMM of JEDEC for the reasons discussed below. EX1003, ¶173.

JEDEC further explains that, during training of the LR-DIMM, “[t]he MB performs ‘Write Leveling’ to the DRAMs **to ensure successful writes**, and ‘Read Enable Training’ **to ensure it can capture read data from the DRAMs correctly**, as part of the DRAM interface training,” and discloses that “MB DRAM interface training must be completed before any MB host interface read or write training **to ensure that the MB DRAM interface is configured optimally for DRAM reads and writes.**” EX1015, 3, 8-9. These statements would have

motivated a Skilled Artisan to add training to systems such as Hazelzet to ensure optimal and correct operation. EX1003,¶174.

In particular, Hazelzet's memory module can include up to four ranks of memory devices in a Registered DIMM format. EX1014, Abstract, FIG. 1, [0036]. The LRDIMM Design Specification explained in detail the advantages, including increased performance and capacity, of adding the LRDIMM's data buffering functionality to an RDIMM, like Hazelzet's module, which buffers only address and command signals. EX1036, 5. Thus, a Skilled Artisan would have understood and been motivated at the time to upgrade Hazelzet's RDIMM with an LRDIMM functionality to buffer the data lines as well. EX1003,¶¶175-177. Such an upgraded LRDIMM would have worked even in Hazelzet's RDIMM platforms (with appropriate BIOS changes). *Id.*; EX1036, 5. These advantages of buffering the data lines were well known to a Skilled Artisan at the time. *See, e.g.*, EX1003,¶¶175-177; EX1028 (Ellsberry), [0031].

The Skilled Artisan would have been also motivated to use the initialization techniques of JEDEC for the upgraded LRDIMM, including MB-DRAM Training, because it ensured that the different interfaces, including the MB-DRAM interface, are optimally configured for reading and writing the memory devices. EX1003,¶177; EX1015, 8-9. Such a combination would have been well within the level of skill at the time and provided nothing more than what was expected from

the combination: an LRDIMM with a memory buffer (MB) that buffered data, address and command signals and implemented training, including the notification of its completion, to ensure optimal configuration for reading and writing the memory devices. EX1003, ¶177.

Buchmann also discloses a “training phase that allows more flexibility and improved control data exchange during start-up,” *id.*, 3:64-67, to establish “reliable communication” on the bus, *id.*, 14:28-35, 14:5-8. A Skilled Artisan would have been motivated by these disclosures to look to systems such as JEDEC’s and Buchman’s to improve reliability. EX1003, ¶178.

Furthermore, Buchmann discloses a buffer/register that buffers data signals in addition to address and command signals. EX1016, FIG. 1. As discussed above with reference to JEDEC, a Skilled Artisan would have been motivated to add the functionality of buffering the data signals and corresponding training to Hazelzet’s Registered DIMM, because it was a known, reliable technique which improved performance and provided higher capacity. EX1003, ¶¶175-177. Accordingly, making the combination of Hazelzet and Buchmann was well within the level of skill at the time and provided nothing more than expected at the time, a DIMM with a buffer to buffer data, address and command signals, and configured to perform efficient training of that buffer during initialization to ensure optimal read and write performance during normal operation. EX1003, ¶179.

2. **Motivation to Add Training as a Mode Separate from Normal Operations**

As Dr. Alpert explains, a Skilled Artisan would have been motivated to combine these references by adding training in an initialization mode separate from normal operation because it was known that training before normal operation was necessary to minimize errors, by “ensur[ing] successful writes,” and “ensur[ing] [the register on the DIMM] can capture read data from the DRAMs correctly.” EX1015, 3, 8, 9; EX1025, 15-18; EX1022, Fig. 4, ¶¶[0032],[0052],[0088-89]; EX1056, 18, 22, 25-26, 42-44, EX1057, Fig. 5, Abstract, 2:13-34, 2:60-3:3, 9:11-10:44. Likewise, Buchmann’s invention is an “initialization training sequence” completed at “power-on,” EX1016, Abstract, which would suggest to a Skilled Artisan that training before normal operation is important. EX1003,¶180.

Because Hazelzet is initialized upon power-on, EX1014,¶[0123]; EX1025, 15-18; EX1027, 1:61-2:19, 6:24-25, 10:24-45, JEDEC’s and Buchmann’s training that occurs at initialization would have complemented Hazelzet’s initialization after Hazelzet’s DIMM has been updated with a Memory Buffer which buffers both address and data like in JEDEC and Buchmann, and a Skilled Artisan would have accordingly been motivated to combine these references such that the training mode occurred separate from normal operating modes. EX1003,¶181.

To the extent Patent Owner might argue that, in a prior IPR (IPR2018-00303), the Hazelzet and Buchmann references were combined in a different way,

and that somehow is evidence of hindsight, that is incorrect. EX1003,¶182. There is more than one obvious way to combine references: “[A] particular combination need not be the preferred, or the most desirable, combination described in the prior art in order to provide motivation.” *Gen. Elec. Co. v. Raytheon Techs. Corp.*, 983 F.3d 1334, 1351 (Fed. Cir. 2020) (cleaned up). Here, training can be performed both during initialization and during normal operations, as Buchmann itself discloses the option of “re-initialization” during “normal, run-time operation” in addition to initialization. EX1003,¶182; EX1016, 12:60-13:41. Accordingly, it would have been obvious to use Buchmann’s training and notification techniques during either initialization (to correctly set up the system) or normal operation (to repair any errors). EX1003,¶182.

3. Motivation to Use Hazelzet’s Open Drain Signaling for Training Notifications

It would have been further obvious to communicate training status in the new mode using the same open drain output used in other modes. EX1003,¶¶183-185.

Hazelzet uses the same open drain output, UE 121, to indicate an “uncorrectable error” in ECC mode and parity error in parity mode, depending on the mode. EX1014, FIGs. 4B, 7A, ¶¶[0044],[0049],[0059],[0064],[0069],[0072],[0109]. JEDEC also discloses using the same open drain output in two different modes, one for parity error and one for training status. EX1015, 8;

EX1036, 9. These disclosures would have motivated a Skilled Artisan to use that same output in the added training mode, particularly when the training mode was implemented separate from, and before, the parity and ECC modes, as here, because those modes would not be using the open drain outputs while the training mode was running during initialization. EX1003, ¶¶185-186.

A Skilled Artisan would also have been so motivated because such multiple use of a pin was known, and would have been considered an efficient use of the limited number of output pins on integrated circuits. For instance, Kim, EX1017, discloses additional details regarding the use of an open-drain output on a memory module during multiple modes, EX1017, 1:16-22, 5:49-57, 6:8-16, and discloses that, in addition to sharing ECC and parity on the error out pin, “[i]n alternate exemplary embodiments, other functions also share the error feedback pin,” *id.* at 6:16-18. EX1003, ¶187. As another example, Talbot discloses memory modules which use the same output to communicate error information during normal mode and training information during a training mode. EX1022, ¶¶[0004][0005],[0032]-[0033],[0052]. Such disclosures would have motivated a Skilled Artisan to use Hazelzet’s UE 121 open-drain output to notify the memory controller that the training was in progress or done. EX1003, ¶188.

Moreover, as Dr. Alpert explains, a Skilled Artisan would have been motivated to arrange the modified Hazelzet to communicate signals indicating

training completion only when all memory modules have completed that training, in order to ensure that the entire memory system had been trained before proceeding to normal operation. EX1003, ¶189. This would permit training to be completed in an orderly and systematic manner, limiting the complexity of the control circuitry needed to implement the training, while using a known, efficient way to do so. *Id.*; EX1043, 7:30-51; EX1017, FIG. 4, 5:65-6:12; EX1014, ¶¶[0018],[0109].

A Skilled Artisan would have been further motivated to modify Hazelzet as described above because Hazelzet's memory system includes multiple memory modules in need of training. EX1014, ¶¶[0018],[0109]; EX1017, FIG. 4, 5:65-6:12; EX1043, 7:30-51. The combinations analyzed here would therefore allow any module in the system to pull the open drain pin to “low” (*i.e.* to ground) while still executing its training sequence, regardless of whether other modules in the system have completed training and were no longer pulling that pin low, thereby delaying normal operations until the system is completely ready. *Id.*; EX1003, ¶¶158-163,190.

VII. PRECISE REASONS FOR RELIEF REQUESTED

As set forth below, the combinations analyzed here — Hazelzet/JEDEC and Hazelzet/Buchmann — satisfy the claim elements set forth in the attached claim

listing (**Attachment C**).⁸ In IPR2020-01042, the Board agreed. EX1059, 35-

45. Additional grounds, building on and incorporating these basic combinations and addressing arguments Patent Owner may raise, are also included below.

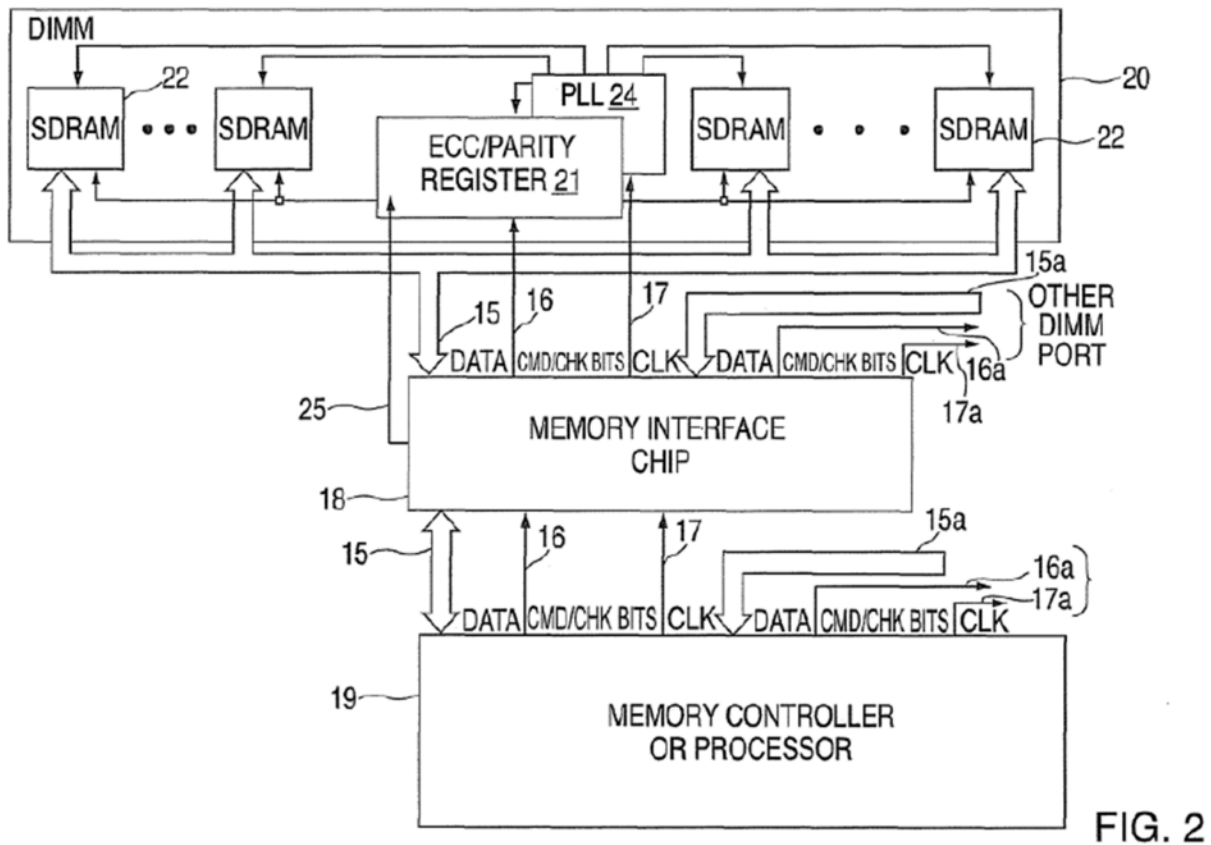
A. Claims 1-24 Are Obvious Over Hazelzet In View Of JEDEC, or Buchmann

1. Claim 1

a) [1.a.] Preamble

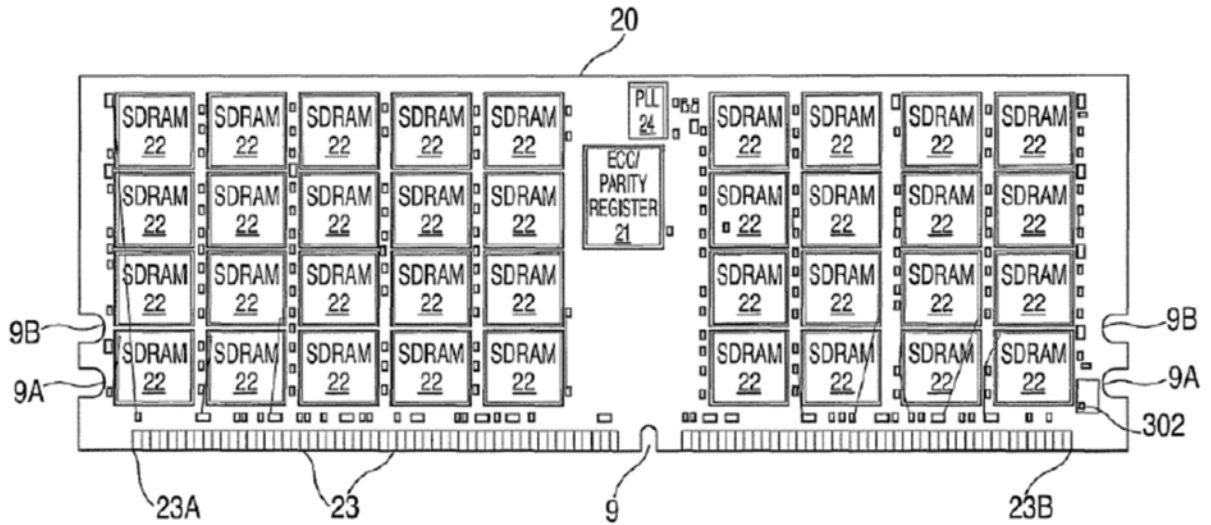
Hazelzet discloses dual inline memory modules (“DIMMs”) configured to operate with the “memory controller” of the host system. EX1014, FIGs. 2, 3A-3D, ¶¶[0036]-[0039]; EX1003, ¶193.

⁸ Specific claim elements are identified in brackets below .



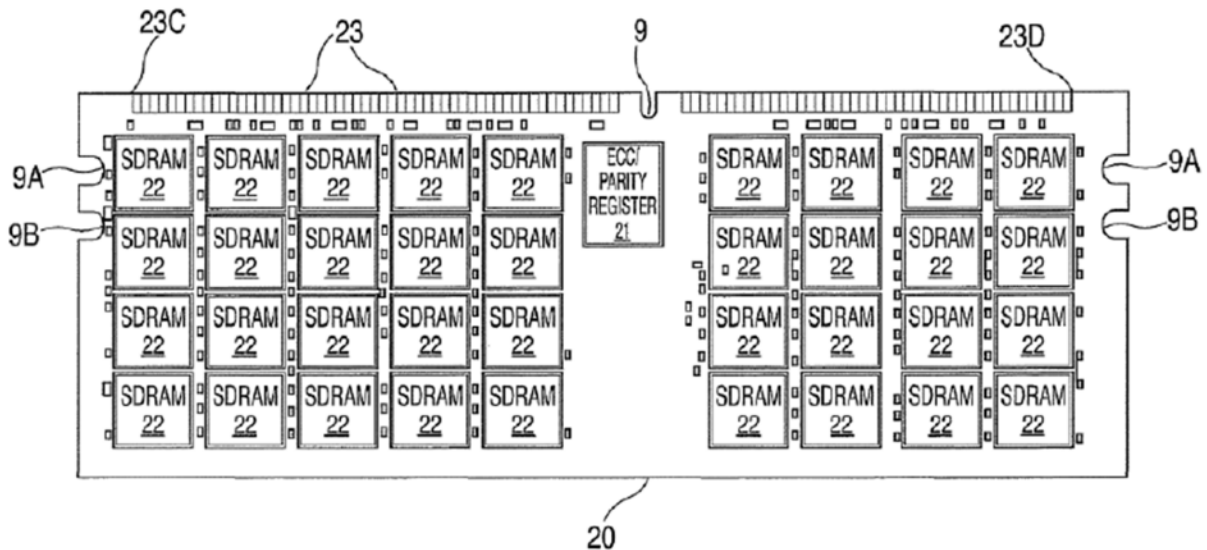
b) [1.b.] Printed Circuit Board

Hazelzet explains the DIMM is “comprised of a printed circuit board having a front side and a back side.” EX1014, ¶[0015], FIGS. 2, 3A-3D, ¶¶[0037],[0039]; EX1003, ¶196.



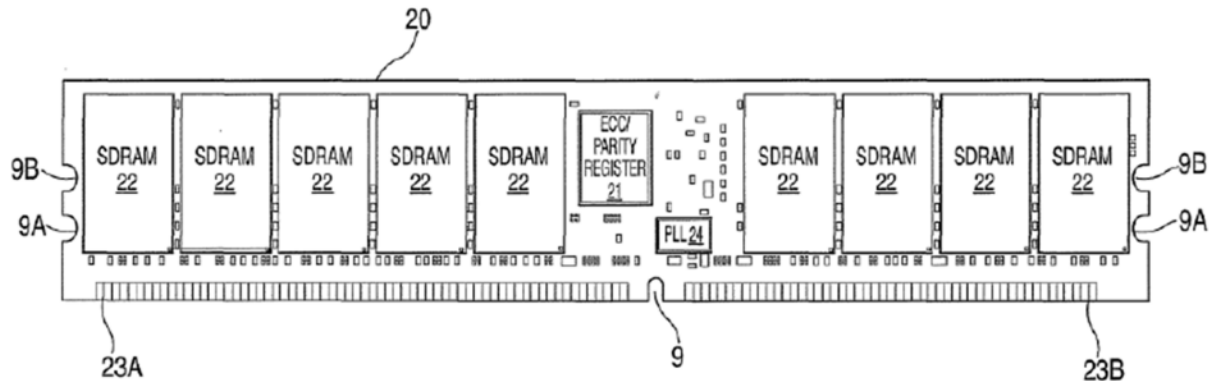
FRONT SIDE OF DIMM - 72 PLANAR

FIG. 3A



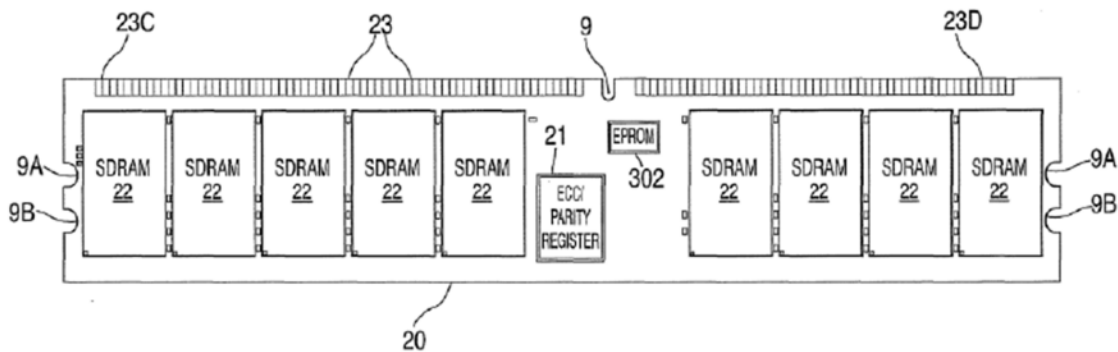
BACK SIDE OF DIMM - 72 PLANAR

FIG. 3B



FRONT SIDE OF DIMM - 4 HIGH STACK

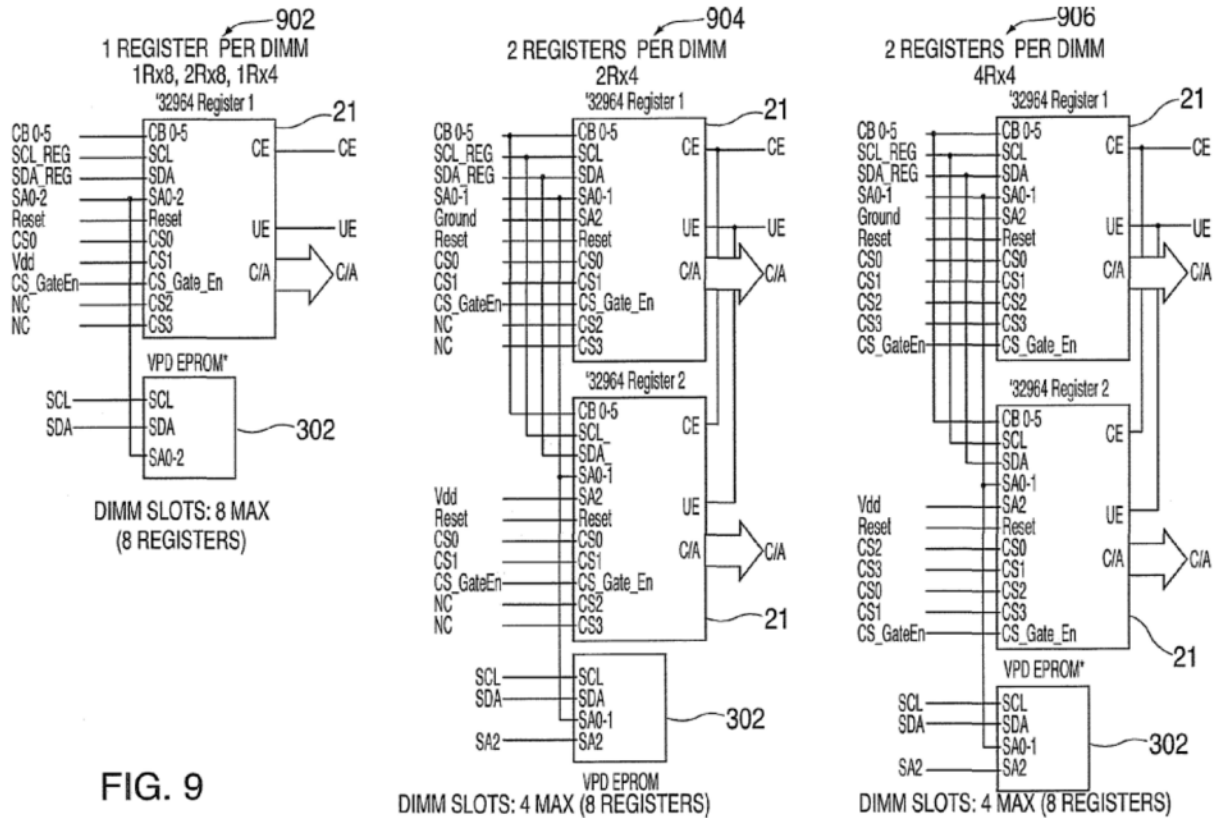
FIG. 3C



BACK SIDE OF DIMM - 4 HIGH STACK

FIG. 3D

Hazelzet explains the memory modules include “connectors 23 along the edge of both the back and front sides,” which are provided to form connections to the memory controller when the module is inserted into a corresponding “slot” of the host system. EX1014, FIGs. 9, 11, ¶¶[0039],[0097]; EX1003,¶197.



Hazelzet therefore discloses “a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller.” EX1003,¶198.

Hazelzet discloses that the printed circuit board has a first set of edge connections for communicating data signals between the module and the memory controller, EX1014, FIGs. 7A-7C, ¶¶[0015],[0035],[0038],[0041]; EX1003,¶199, and a second set of edge connections for communicating address and control signals from the memory controller, EX1014, FIGs 7A-7C, ¶¶[0015],[0035],[0038],[0041]; EX1003,¶200. Hazelzet further discloses that the printed circuit

board has an error edge connection coupled to the open drain output of the module controller. EX1014, FIGs 4B, 7A, ¶¶[0072],[0109]; EX1003,¶201.

c) [1.c.] DRAM

Hazelzet's memory module includes a plurality of "DRAMs" on the "printed circuit board," EX1014, ¶[0015], FIGs. 2, 3A-3D; EX1003,¶204.

d) [1.d.] Module Controller ... Having An Open Drain Output

Hazelzet discloses an ECC/Parity register ("module controller") having an output for uncorrectable errors shown in FIG. 4B as "/ERROR (UE) 121" (i.e., UE 121), which is an "open drain output." EX1014, FIGs. 3A-3D, 4A-4B, ¶¶[0044],[0059],[0072]. The ECC/Parity register is on the "printed circuit board" and coupled to the DRAMs. EX1014, FIGs. 3A-3D, ¶¶[0039],[0042]; EX1003,¶207. The output UE 121 is "coupled to the error edge connection" of the module. Ex. 1014, FIGs. 4B, 7A(pin 142), ¶¶[0059],[0072]; EX1003,¶¶208-211.

e) [1.e.] Wherein Clauses

(1) [1.e.i] Two Modes

Hazelzet discloses the module is configurable to operate in (1) a "parity mode," which is the claimed "*first mode*," and (2) an "ECC mode." EX1014, FIG. 8; ¶¶[0064],[0069]-[0072]; EX1003,¶213. As demonstrated above, §V.D, the combination of Hazelzet and JEDEC or, alternatively, Hazelzet and Buchmann,

include a “*second mode*” in which training is carried out, and the combined module would be configurable to operate in either mode.

(2) [1.e.ii] Normal Read and Write

Hazelzet discloses that “as shown in this FIG. 2, the memory interface chip 18 sends and receives data from the DIMMs via the data line 15 and sends address and commands via line 16.” EX1014, ¶[0038]; FIG. 2. The figure shows line 15 coupling the memory controller and the DRAMs, and line 16 coupling the memory controller and the register 21. *Id.* A Skilled Artisan would understand from Figure 2 that lines 15 and 16 are coupled to edge connectors for data and address/control, respectively, since those lines couple the DIMM to the memory controller.

EX1014, FIGs. 2, 7A-7B, ¶¶[0015],[0035],[0038],[0041]. Hazelzet therefore discloses that the module is configurable to receive address and control signals via the edge connections included on the module for that purpose. EX1003, ¶214.

A Skilled Artisan would also understand that such operations – communicating data with DRAMs while communicating address and command information with the register – to constitute “*normal memory read or write operations*” (and also “*memory read or write operations*”) because they follow the standard configuration for such operations with a JEDEC compliant device, EX1014, ¶[0044], including sending address and control to the register and data to the DRAMs. EX1024, 1, 14, 16; EX1003, ¶215.

Furthermore, as discussed above, it would have been obvious to a Skilled Artisan to add the functionality of buffering the data lines 15 to Hazelzet's module as taught by JEDEC and Buchmann. EX1003, ¶¶175-177. The presence of these data buffers, between the edge connectors and the memory devices on data lines 15, does not change the claimed characteristics of read and write operations during normal operation in response to requests from the system memory controller that would follow the standard JEDEC protocol, as discussed further below. *See also* EX1014, [0044], [0124]; EX1036, 5, Ex. 1024, (JEDEC Standard, Double Data Rate (DDR) SDRAM Specification).

Indeed, Hazelzet explains that its “parity mode” is an “operating mode,” EX1014, ¶¶[0064],[0070]; EX1003, ¶217, in which “the memory interface chip or controller would generate a single parity bit in conjunction with providing **the full address and command field to the module.**” EX1014, ¶[0075]; EX1003, ¶¶217-218. A Skilled Artisan would understand the use of the phrase “operating mode” and the phrase “full address and command field” in this context refers to the signals sent to a memory module during a normal read or write operation. *Id.*; EX1024, 1, 14, 16; EX1014, ¶[0038]. Moreover, Figure 8 of Hazelzet depicts a timing diagram used with his invention and explicitly discloses “Data In” and “Data Out” in parity mode, which movement of data is known to occur in the context of normal read and write operations. Ex. 1014, FIG. 8. Hazelzet therefore

discloses that the address and control signals received by the module over the address/control edge connections are associated with “*normal memory read or write operations*.” EX1003,¶219.

Moreover, Hazelzet relates this configuration to both its ECC and parity mode, EX1014,¶[0038], so a Skilled Artisan would understand these operations occur in parity mode (“*first mode*”). EX1003,¶¶221-223.

To the extent one might argue that Hazelzet does not sufficiently disclose normal memory read and write operations in the parity mode, it would have been obvious to include that in the system of Hazelzet. The use of such operations in an operational mode employing parity checking was known in the prior art. EX1017, 6:19-34. Hazelzet describes how its “parity mode” is an “operating mode,” EX1014,¶¶[0064],[0070], and discloses that in that mode the module is provided “the full address and command field,” EX1014,¶[0075], suggesting the use of normal read and write operations that were known in the prior art, EX1024, 14, 16. A Skilled Artisan would have therefore been motivated to modify Hazelzet’s “parity mode” into the claimed “*first mode*” involving a normal read and write operations over the recited edge connections because to do so would have permitted normal memory operations using existing and convenient connections disclosed in Hazelzet and because it would have been common sense to do so. EX1024, 14, 16. This is confirmed by the passage’s reference to a third mode

without ECC or parity where the register would simply be “operat[ing] the memory” which a Skilled Artisan would also understand to refer to the usual memory operations such as reading and writing. EX1014,¶[0075]; EX1003,¶225.

(3) [1.e.iii] Not Accessed

As demonstrated above, §V.D, the combinations analyzed here include JEDEC or Buchmann training sequences in a training mode (“*second mode*”) during initialization separate from any mode that includes memory read and write operations in response to memory controller commands, thereby satisfying this limitation.

Moreover, none of the portions of Hazelzet, JEDEC, and Buchmann relied upon in the combinations analyzed disclose memory read and write operations in response to memory controller commands occurring during the training operations, EX1003,¶229, so their silence additionally satisfies this limitation. *Süd-Chemie, Inc. v. Multisorb Technologies, Inc.*, 554 F.3d 1001, 1004-05 (Fed. Cir. 2009).

(4) [1.e.iv] Training Sequences

As explained above, §V.D, the combinations analyzed here include a separate training mode (“*second mode*”) into which the module can be placed and in which the module can implement (“*configurable to perform*”) various training sequences (*e.g.*, Write Leveling and Read Enable Training per JEDEC/TS0 and TS3 per Buchmann) (“*operations related to one or more training sequences*”).

Each of those operations includes a set of operations occurring in a particular order, used for training the memory module. EX1015, 8; EX1039, 8-9; EX1016, FIGs. 4, 6, 5:51-7, 8:24-9:18; EX1040, 14:1-15:3; EX1018, Fig. 4; EX1003, ¶230.

f) [1.f.] Operation In the First Mode

(1) [1.f.i] Receive Address and Control Signals

As explained for claim elements [1.b] and [1.e.ii], Hazelzet's module can be placed into a parity mode, which is a normal operating mode in which the module is provided, over the edge connections identified for that purpose, address and control signals for performing “*one or more normal memory read or write operations.*” EX1014, FIGs. 2, 7A-7B, ¶¶[0015],[0035],[0038],[0041],[0064],[0070]; EX1024, 13-14, 16; EX1003, ¶232.

(1) [1.f.ii] Communicate Data

As explained for claim elements [1.b] and [1.e.ii], Hazelzet discloses that the printed circuit board has a first set of edge connections for communicating data signals between the DRAM and the system memory controller, EX1014, FIGs 7A-7C, ¶¶[0015],[0035],[0038],[0041], while the memory module is in the “parity mode” and in accordance with the received address and control signals, *id.* at FIGs. 2, 8, ¶¶[0015],[0035],[0038],[0041],[0064],[0070]. Further, as explained in claim element [1.e.ii], data communication between the memory module and the memory controller is “*in accordance with the address and control signals.*” EX1014, FIGs.

2, 7A-7C, 8, ¶¶[0015],[0035],[0038],[0041],[0064],[0070]; EX1024, 13;
EX1003, ¶¶214-223,233.

(2) [1.f.iii] Output Parity Error

As explained in claim elements [1.b.] and [1.d.], the error edge connection (pin 142) is coupled to the open drain output (UE 121) of the ECC/Parity register (“*module controller*”). EX1014, FIGs. 4B, 7A(pin 142), ¶¶[0059],[0072]; EX1003, ¶234. In particular, Hazelzet’s ECC/Parity register includes an “SEC/DED ECC” 90. EX1014, FIG. 4B. Figure 5 of Hazelzet, which is a block diagram of the “SEC/DED ECC” 90 in Figure 4B, includes a “parity generator/checker circuit 231.” EX1014, ¶¶[0028],[0076]; EX1003, ¶235. When the memory module is in the parity mode (“*first mode*”), the “parity generator/checker circuit 231” generates and sends the “parity error signal (PERR)” to the “error logic circuit” 100, EX1014, FIGs. 4-5, ¶¶[0070],[0076]; EX1003, ¶236, and outputs it to the memory controller through the output line UE 121, EX1014, ¶[0059]; EX1003, ¶237, which is an open-drain output, EX1014, ¶[0072], coupled to the memory controller using pin number 142, EX1014, FIG. 7A(pin 142), ¶¶[0038],[0070],[0072]; EX1003, ¶¶238-240.

g) [1.g.] Operation In The Second Mode

As demonstrated above, §V.D, in the combinations analyzed here, the Hazelzet module would be modified to be configurable to enter a training mode

and output JEDEC or Buchmann training status signals to the system memory controller via open drain output UE 121. *Id.* Each of the status signals analyzed above (ERROUT#, TS0_done, TS3_ack, TS3_done,) represent “*information related to the one or more training sequences*” because each provides status about the related sequences, such as whether it has been completed or whether all memory buffers have returned an acknowledgement. *Id.* Each of these combinations therefore alternatively satisfies “*wherein the module controller in the second mode is further configurable to provide information related to the one or more training sequences.*” EX1003,¶¶243,164-167.

Moreover, Hazelzet’s memory system involves sharing the open drain output so that the memory controller can receive notification signals from multiple modules using the open drain output. EX1014,¶¶[0018],[0072],[0109]; EX1003,¶244. A Skilled Artisan would understand that, in this combination, the added training status signals would be at a low logic level (because the gate signals of the transistors in the open drain circuits in all the modules in which the training is ongoing are high) over a Hazelzet open drain output (UE 121) until the related operations are completed for all modules of the system and the gate signals to the transistors of all the open drain circuits in all the modules are low, at which time the signals would be at a high impedance state, indicating completion. EX1017, FIG. 4, 5:65-6:12 (illustrating and describing how such a system as is in Hazelzet

operates); EX1001, 9:47-10:50 (explaining in same way as Kim functioning of open-drain outputs in memory systems); EX1003, ¶245. The high and low gate signals to the transistors represent “*driving the open drain output and the error edge connection to a first state or to a second state,*” respectively or vice versa. EX1003, ¶245.

Such open drain signals would be changed from a high impedance state to a low state as the gate of the transistor changes from a low to a high to indicate the related training operations were in progress, and changed from a low state to a high impedance state as the gate of the transistor driving the signal changes from a high to a low to indicate when the related operations complete in each memory module. EX1014, FIG. 4B, ¶¶[0059],[0070],[0072]; EX1017, FIG. 4, 5:65-6:12; EX1015, 8; EX1016, FIGs. 4&6, 3:52-54, 5:51-7:2, 8:24-9:18, 26:30-32, 27:18-21; EX1003, ¶246. Each combination therefore satisfies “*one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.*”

2. Claims 2 and 11

Hazelzet’s ECC/Parity register (“*module controller*”) “comprises an integrated circuit.” It is also referred to as a “buffer device” or a “buffer chip.” EX1014, ¶[0038]. Hazelzet explains that the module support devices, including “buffers,” “registers,” and “PLL” may be comprised of “multiple separate chips”

or may be “combined onto a single package or even integrated onto a single device.” EX1014, ¶[0115], FIG. 3A-3D, ¶¶[0039],[0042]; EX1003, ¶¶249-250,329.

3. Claim 3

As explained in claim element [1.d.], Hazelzet discloses that the ECC/Parity register has “*open drain output[s]*.” Hazelzet further explains that the ECC/Parity register has an “error correction code circuit ECC segment 21b,” which is a “*notification circuit*” because it outputs signals notifying the system memory controller of correctable, uncorrectable, and parity errors. EX1014, ¶[0044]. Such “error correction code circuit ECC segment 21b” (within the ECC/Parity register) includes the circuitry for determining whether the errors occurred, SEC/DED ECC circuit 90, and error logic circuit 100 that receives error signals from SEC/DED ECC circuit 90, such as UE 110 and PERR 111, and provides the above-mentioned “open-drain output(s),” such as UE 121. EX1014, FIG 4B, ¶¶[0059],[0072]; EX1003, ¶252.

As noted above, §V.D, the combinations analyzed here include, and a Skilled Artisan would understand an open drain output to necessarily include, a field effect transistor having gate, source, and drain. A Skilled Artisan would have also understood that the disclosed “open drain” output is the output of “*a transistor having an open drain*” while the “*source*” of that transistor is “*coupled to the*

ground.” EX1017, FIGs. 4-5, 5:65-6:18; EX1020, Face, 4:28-37; EX1003, ¶¶158-163,168,253,254.

4. Claim 4

As demonstrated above, §V.D, in the combinations analyzed here the open drain output is configured such that the transistor output is driven low (ground) while training is still occurring and driven high upon completion. Moreover, to drive the output low (i.e., ground), the gate of the transistor must be high, causing the transistor to conduct and connect the drain to ground. On the other hand, to drive the output high (which would be a high impedance state), the gate of the transistor must be low, turning the transistor off. EX1003, ¶¶168,272-275.

Thus, in the combinations analyzed here, the ECC/Parity register is configurable (for example, by placing it in the training mode) “*to drive a gate of the transistor high so as to drive open drain output and the error edge connection to ground, or to drive the gate of the transistor low so as to drive the open drain output and the error edge connection to the high impedance state,*” and thereby output training sequence status signals. EX1003, ¶274.

5. Claim 5

Hazelzet explains that its ECC/Parity register has “open-drain output[s]” capable of utilizing “parity error signals” (PERR) to output signal UE 121 to the host indicating a parity error. EX1014, ¶¶[0059],[0070],[0072],[0076]. Further,

when the memory module is in the parity mode (“*first mode*”), the “parity generator/checker circuit 231” (within SEC/DED ECC circuit 90) generates and sends the “parity error signal (PERR)” to the “error logic circuit” 100. EX1014, FIGs. 4B-5, ¶¶[0059],[0070],[0072],[0076]; EX1003,¶278. Hazelzet explains that in the parity mode the parity error “will be reported two clock pulses later via the Uncorrectable Error (UE) line (driven low for two clock pulses).” EX1014,¶¶[0070];[0018]; EX1003,¶279.

Further, as explained in claim 4, Hazelzet discloses that its open-drain output is driven “low” (i.e., to ground) when the driver is enabled (i.e., gate receives a high voltage), and further explains that the open-drain “output [is] permitted to return to an un-driven state (high impedance)” when the “driver [is] disabled.” EX1014,¶[0099]; EX1003,¶280.

Accordingly, Hazelzet discloses its open-drain output UE 121 is configured to “*output the signal indicating a parity error having occurred by driving the gate of the transistor high to provide a low impedance path between the open drain output and the ground.*” See also analysis in claim 4. EX1017, FIGs. 4-5, 5:65-6:18; EX1003,¶¶158-163,281.

6. Claims 6, 13 and 22

Hazelzet’s “*notification circuit*” includes an “Error Logic 100,” EX1014, FIG. 4B, ¶¶[0044],[0059]; EX1003,¶285; which receives the “US [sic] 110” signal

and the “PERR 111” signal, and outputs one of these signals to the same “/ERROR (UE)” pin depending on which mode the memory module is in. EX1014, FIG. 4B, ¶¶[0044],[0059],[0069-72]. In the combinations analyzed here, that circuitry would be modified to implement the additional training mode, in which the UE 121 open drain output would, when the module is in training mode, be used to send the notification/status signals identified above. EX1003, ¶¶162,167,286,333,372.

As Dr. Alpert explains, a Skilled Artisan would necessarily understand that the UE 121 open drain output is driven by a transistor in an open drain configuration, and that such a transistor necessarily has “*a gate*” that can be driven to assert the open drain output. EX1003, ¶¶158-163,286. Because in the combinations analyzed here Error Logic 100 receives “U[E] 110” signal and the “PERR 111” signal and the training mode notification signals, but uses only one such signal to drive the UE 121 output, depending on mode, a Skilled Artisan would also understand that Error Logic 100 would necessarily include logic circuitry to determine which signal should be used to drive the transistor. EX1017, FIGs. 4-5, 5:65-6:18 (depicting in FIG. 5 OR gate used for such purpose). That additional logic circuitry is a “*logic circuit*,” and necessarily has “*an output coupled to a gate of the transistor*” because that is how a transistor in an open drain configuration is driven. EX1003, ¶¶286-287. Moreover, the signal driving that gate is necessarily related to one of the signals input to Error Logic 100 (*e.g.*,

“PERR 111” (“*first signal*”) or the training notification signals (“*second signal*”), depending on mode, so the additional logic circuitry is “*configurable to drive the gate of the transistor with either a first signal related to the parity error or a second signal related to the one or more training sequences.*”

EX1003, ¶¶288,333,372.

7. Claims 7 and 14

As demonstrated above, §V.D, in the combinations analyzed here the open drain output is configured such that the transistor output is driven low (ground) while training is still occurring and driven high upon completion. Moreover, to drive the output low (i.e., ground), the signal at the gate of the transistor (“*the second signal*” when the system is in training mode) must be high, causing the transistor to conduct and connect the drain to ground. On the other hand, to drive the output high (which would be a high impedance state), the gate of the transistor must be low, turning the transistor off. EX1003, ¶¶168,292-295.

Thus, in the combinations analyzed here, the ECC/Parity register is configurable (for example, by placing it in the training mode) “*to provide the information related to the one or more training sequences by driving a gate of the transistor with the second signal so as to drive the open drain output from the high impedance state to ground or from ground to the high impedance state.*”

8. Claims 8, 9, 15, 16, 18, 19, and 24

As Dr. Alpert explains, JEDEC discloses that during the MB-DRAM training, “[n]o DRAM commands or control word writes (either over the Command/Address and Control buses or via SMBus) can be issued to the MB until the MB-DRAM Interface training is complete and the DODTn inputs must be kept low.” EX1015, 8. Accordingly, during such training the address/control pins (including the high order address/control pins) would remain inactive as those are pins used to provide “DRAM commands or control word writes” and no data signals would be communicated on the data pins. *Id.*; EX1003, ¶¶299,306. That satisfies the limitations of each of these dependent claims.

Additionally, in a Buchmann combination, in which only the TS0 training operations are carried out in the training mode (“*second mode*”), the address/control and data pins (including the high order address/control pins) of the module edge connections would not be active during that training because TS0 training involves training of the “clock” itself, and no address/control or data signals are transmitted between the host and the memory module during such training. EX1016, 5:51-7:2; EX1003, ¶¶300,306,307,349,376. That also satisfies the limitations of each of these dependent claims.

To the extent one might argue otherwise, it would have been obvious not to send any data or address/control signals while the clock is being trained because a

Skilled Artisan would have been motivated to keep the pin(s) for those signals inactive to conserve power and/or avoid unreliable operation during periods that the clock may be unstable. EX1003, ¶¶301,308.

Moreover, neither Hazelzet nor JEDEC or Buchmann disclose address/control or data pins being active while the memory module is in a MB-DRAM Training or TS0 training mode during initialization/power-on. Because these claims each recite a negative limitation, that silence also satisfies these claims. *Süd-Chemie*, 554 F.3d at 1004-05. EX1003, ¶¶302,309.

9. Claim 10

a) [10.a.] Preamble

This language is satisfied for the reasons set forth for claim element [1.a.].

b) [10.b.] Printed Circuit Board

This language is satisfied for the reasons set forth for claim element [1.b.].

c) [10.c.] DRAM

This language is satisfied for the reasons set forth for claim element [1.c.].

d) [10.d.] Module Controller ... Having An Open Drain Output

This language is satisfied for the reasons set forth for claim elements [1.d.] and [1.g.].

While claim element [1.g.] requires the module controller to be “configurable to provide information related to the one or more training sequences

by driving the open drain output and the error edge connection **to a first state or to a second state ...**,” claim element [10.d.] requires the module controller to be “configurable to drive the open drain output **from a first state to a second state and from the second state to the first state, ...**” EX1003, ¶319.

This additional language in claim element [10.d.] is similar to claim 7 and is satisfied by the combinations analyzed here for the same reasons. In particular, as explained in claim element [1.g.] and claim 7, in the combinations analyzed here the open drain signals would be low logic levels to indicate the training sequence (*e.g.*, MB-DRAM/TS0 or TS3) was in progress (*i.e.*, the logic levels of the open drain output changes from a high impedance state to a low state, because the gate of the transistor changes from a low to a high). On the other hand, the open drain signals would be at a high-impedance (*i.e.*, the logic level of the open drain output changes from a low state to a high impedance state, because the gate of the transistor changes from a high to a low) when that sequence completed in all memory modules. EX1014, FIGs. 4B-5, ¶¶[0059],[0070],[0072],[0076]; EX1017, FIGs. 4-5, 5:65-6:18; EX1003, ¶¶320,158-163,168.

e) [10.e.] A First Mode And A Second Mode

This language is satisfied for the reasons set forth for claim element [1.e.] and claim 9.

While claim element [1.e.] recites “***normal*** memory read or write

operations” and this claim element recites “*memory read or write operations*,” as demonstrated above those phrases should be interpreted to mean the same thing and, regardless, in the combinations analyzed, the “memory module is not accessed **by the memory controller** for memory read or write operations” during MB-DRAM Training, TS0 training or TS3 training. The analysis of claim element [1.e.] and claim 9 therefore satisfies this claim element. EX1003,¶323.

f) [10.f.] First Mode Operation

This language is satisfied for the reasons set forth for claim element [1.f.].

g) [10.g.] Second Mode Operation

This language is satisfied for the reasons set forth for claim element [1.g.].

10. Claims 12, 20 and 23

This language is satisfied for the reasons set forth for claims 3, 4 and 5. EX1003,¶¶331,353,374. In particular, the analysis in claim 3 satisfies claim element [12.a.], the analysis in claim 4 satisfies claim element [12.b.], and the analysis in claim 5 satisfies claim element [12.c.].

Similarly, the analysis in claim 3 satisfies claim elements [20.a.] and [23.a.], the analysis in claim 5 satisfies claim elements [20.b.] and [23.b.], and the analysis in claim 4 satisfies claim elements [20.c.] and [23.c.].

Moreover, as demonstrated above, in the combinations analyzed here, the open drain signals relating to the training sequences (*e.g.*, ERROUT#, TS0_done, TS3_ack, TS3_done) are “*unrelated to any memory read or write operation*”

because they are related solely to the JEDEC or Buchmann training sequences, respectively, and not to any memory controller operations that seek to communicate data with the module or seek to read or write to the memory devices, §VI.A.1.g, EX1003, ¶¶164,180,229,347.

11. Claim 17

a) [17.a.] Preamble

This limitation is satisfied by the operation of the combined system analyzed in connection with claim 1. EX1003, ¶341.

b) [17.b.] Printed Circuit Board & DRAMs

This limitation is satisfied for the reasons set forth for claim elements [1.a.], [1.b.] and [1.c.].

c) [17.c.] Memory Read or Write Operations

This limitation is satisfied for the same reasons set for in claim elements [1.e.] and [1.f]. Specifically, Hazelzet discloses normal memory operations that entail the module receiving address and control signals from a system memory controller via the respective address and control edge connections, and in response communicating data between the system memory controller and the module DRAMs via the data edge connections under the control of the module controller. §VI.A.1(2), EX1003, ¶¶214-221,345. Similarly, Hazelzet discloses the module outputting, in the “*first mode*,” a parity error signal via an open drain output (UE

121) in connection with memory read and write operations accessing the module.

See §VI.A.1.f, *above*; EX1003,¶¶231-241,345.

d) [17.d.] Training Sequences

This limitation is satisfied for the same reasons set for in claim elements [1.e.] and [1.g.]. Specifically, as demonstrated above, the combinations analyzed here include a module that performs training sequence operations unrelated to memory read or write operations in response to commands from the memory controller. EX1003,¶¶231-241. Similarly, the module of the combined system outputs to the system memory controller training notification signals (*e.g.*, ERROUT#, TS0_done, TS3_ack, TS3_done, TS3_ack) via an open drain output (UE 121), EX1003,¶¶242-247, which notification signals are related solely to the JEDEC or Buchmann training sequences and not to any memory controller operations that seek to communicate data with the module or seek to read or write to the memory devices during the training mode analyzed here, §VI.A.1.g, EX1003,¶¶164,165,229,180,181,347.

12. Claim 21

a) [21.a.] Preamble

This limitation is satisfied for the reasons set forth for claim element [1.a.].

b) [21.b.] Printed Circuit Board

This limitation is satisfied for the reasons set forth for claim element [1.b.].

c) [21.c.] DRAMs

This limitation is satisfied for the reasons set forth for claim element [1.c.].

d) [21.d.] Module Controller Including ... An Open Drain Output

This limitation is satisfied for the same reasons set forth in claim elements [1.d.], and claims 3 and 4. Specifically, the combinations analyzed here satisfies “*a module controller on the printed circuit board and coupled to the dynamic random access memory elements*” for the reasons set forth for claim element [1.d]. EX1003, ¶¶206-209. It satisfies “*the module controller including a transistor having a gate and an open drain output coupled to the error edge connection*” for the reasons set forth for claim 3. EX1003, ¶¶251-255. And it satisfies “*wherein the module controller is configurable to drive the gate of the transistor so as to drive the open drain output to a first state or a second state, the first state being a low logic level [e.g., ground] and the second state being a high impedance state*” for the reasons set forth for claim 4. See §VI.A.4, above; EX1003, ¶¶271,361.

e) [21.e.] Normal Memory Read or Write Operations

This limitation is satisfied for the same reasons set forth for claim elements [1.f.i-iii], with the following additional explanations.

Hazelzet discloses that the ECC/Parity register is configurable (e.g., when placed in parity mode) to receive address command signals that a Skilled Artisan would understand to be associated with normal memory read and write operations (“*memory commands associated with normal memory read or write operations*”),

EX1003, ¶¶214-221; EX1014, FIGs. 2, 7A-7B, ¶¶[0015],[0035],[0038],[0041],[0064],[0070], and that, in response to such commands, the ECC/Parity register outputs associated address and control signals to the DRAMs of the module, EX1014, [0042],[0075]. Hazelzet therefore discloses claim element [21.e.i]. EX1003, ¶364.

To the extent one might argue that Hazelzet does not sufficiently disclose claim element [21.e.i], it would have been obvious to include it in the combined system. In particular, Hazelzet clearly discloses the ECC/Parity register receiving address and command information associated with memory commands. EX1014, FIGs. 2, 7A-7B, ¶¶[0015],[0038],[0041-42],[0064],[0070],[0075]. A Skilled

Artisan would have been motivated to configure the register to correspondingly output associated address and control signals to the DRAMs, and it would have been common sense to do so, because that would be necessary to carry out the memory operations and access the DRAMs. EX1003, ¶365.

Hazelzet also discloses that the DRAMs are configurable (*i.e.*, when connected to the address, control, data and PLL lines of the module, as described in Hazelzet, EX1014, FIG. 2), to communicate data signals with the system memory controller over the disclosed edge connections in response to address and control signals, EX1003, ¶¶231-241, and discloses pinout information for one embodiment of his module, which includes 64 data lines (DQ0-DQ63), EX1014, FIGs. 7A-7C,

which a Skilled Artisan would understand can communicate a 64-bit wide data signal. Alternatively, Hazelzet discloses a 72 bit wide (*i.e.*, $9 \times 8 = 72$) embodiment. EX1014, ¶[0092]. Hazelzet therefore discloses claim element [21.e.ii]. EX1003, ¶366.

To the extent Patent Owner argues that a single “dynamic random access memory element” must be able to “*communicate one or more N-bit-wide data signals ... where N is at least 32,*” to satisfy the limitation in claim element [21.e.ii], this limitation would nevertheless have been obvious. A Skilled Artisan would have understood that modifying the memory system to use SDRAMs with high bit widths (*e.g.*, 32 bit wide) was not only known (or at least obvious), but also well within the skill of a Skilled Artisan by the effective filing date of the 595 Patent. EX1024, i; EX1029, 1; EX1014, ¶[0113]; EX1003, ¶367.

The combinations analyzed here also discloses claim element [21.e.iii] for the reasons set forth above for [1.f.iii]. EX1003, ¶¶231-241, 368.

f) [21.f.] Operations Related To Training Sequences

This limitation is satisfied for the same reasons set for in claim elements [1.e.], [1.g.] and [10.e]. Like claim element [10.e.], this element recites “*memory read or write operations,*” rather than “***normal*** *memory read or write operations*” like claim element [1.e], and is satisfied for the additional reasons for claim element [10.e.].

B. Claims 3-7, 12-14, 20, 22, And 23 Are Obvious Over the Combinations Analyzed Above, and Kim

To the extent one might argue that the Hazelzet/JEDEC or Hazelzet/Buchmann combinations do not satisfy the limitations in claims 3-7, 12-14, 20, 22, or 23, these claims would have been obvious in view of those combinations further combined with Kim.

Kim discloses an “open drain output” with an output pin coupled to the drain of a transistor, which includes a gate, a source, and a drain. EX1017, FIG. 4. FIG. 4 of Kim shows an open drain output coupled to a pull-up resistor (*i.e.*, connected to a high voltage via a pull-up resistor), the source of the transistor coupled to ground, and the gate coupled to “ERR.” EX1003, ¶256.

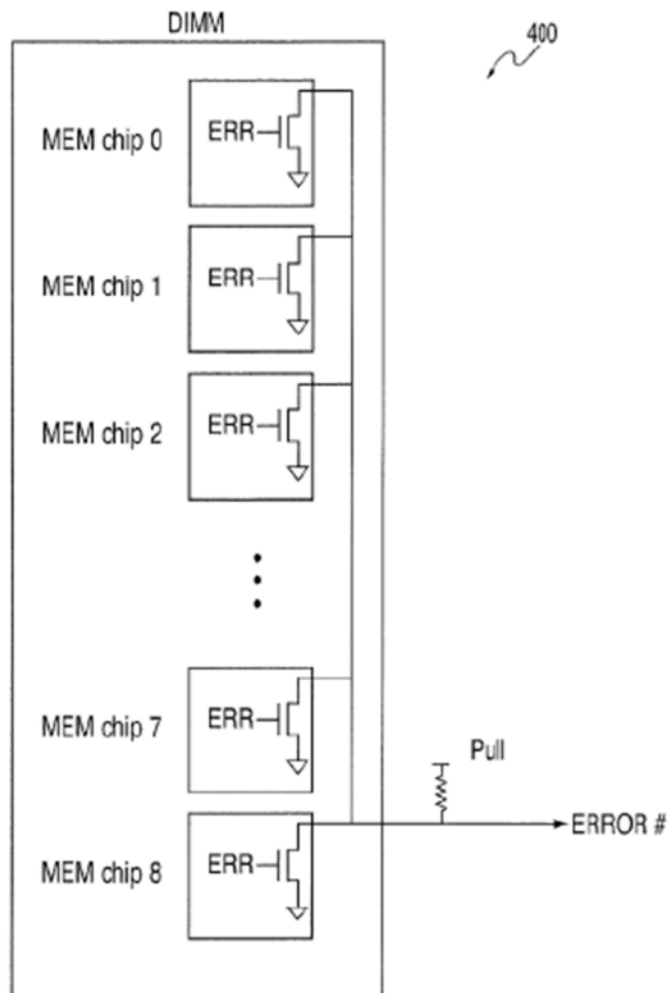


FIG. 4

Kim also discloses in Figure 5 using a logic element (an OR gate) such that multiple error signals could drive the gate of the open-drain transistor. EX1017, FIG. 5, 6:13-6:18.

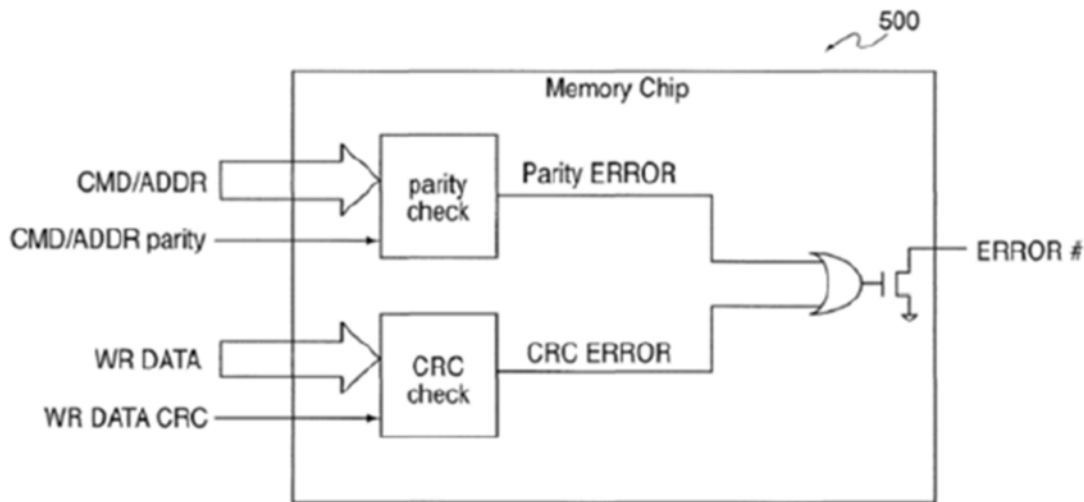
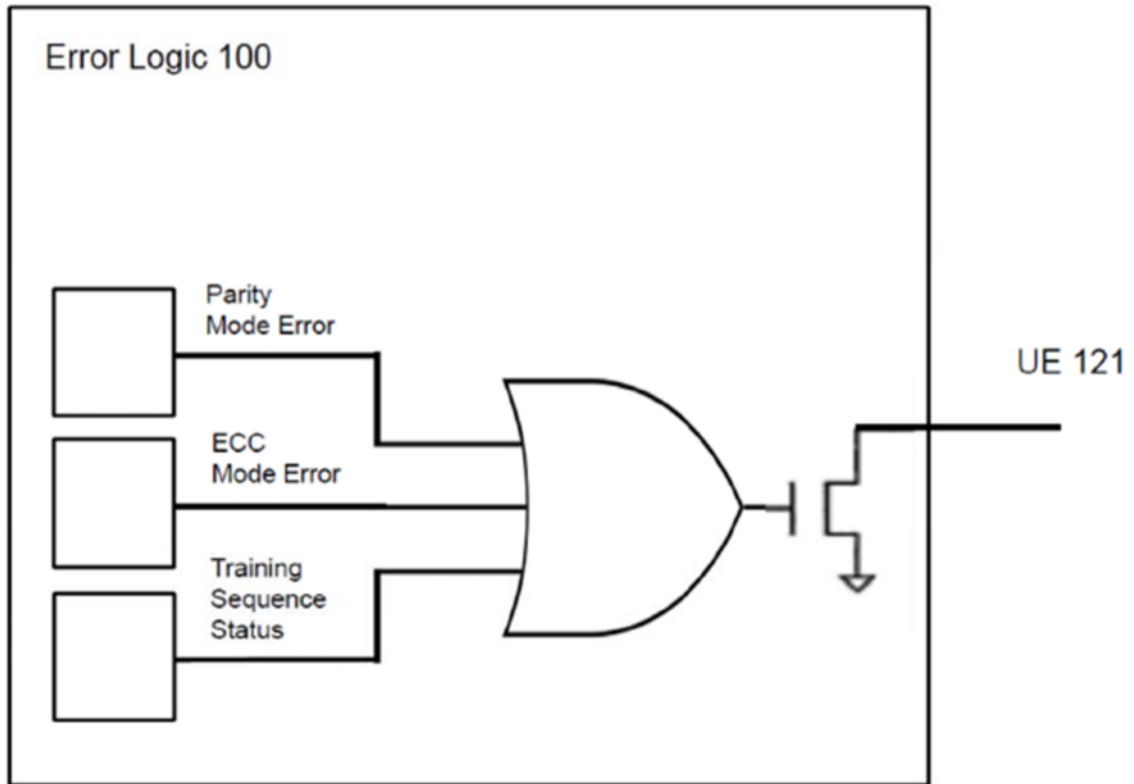


FIG. 5

In the combinations analyzed here, Kim's open drain transistor configuration would be included within Hazelzet's error logic 100 (which is part of the ECC segment 21b – a “*notification circuit*” as claimed) such that signals indicating parity mode error, ECC mode error and training status would be provided to a logic gate, such as an OR gate, as in Kim, which would select among them based on the mode of the module, as in Hazelzet. The output of the OR gate would be coupled to, and would drive, the gate of an open drain transistor, which itself drives UE 121, as shown in the annotation below:



EX1003, ¶258.

In this combination, each signal input to the OR gate would remain low when the module was not in its associated mode, and the signal whose mode was active could be high to indicate the occurrence of the event to be signaled (error in Parity Mode or ECC Mode; ongoing training in Training Mode), or low to indicate that the event is not occurring (Parity/ECC) or acknowledged/completed (training). The signal whose mode was active would then be passed through the OR gate to drive the gate of the transistor. EX1003, ¶¶261,262.

As Dr. Alpert explains, *id.* ¶152, a Skilled Artisan would have understood that an open drain output as set forth in the figure above would be pulled to a high

logic level when the gate of the transistor is low, because the transistor would be off. EX1017 at FIG. 4. The output would then be in an un-driven, high impedance, state. EX1014, ¶[0099]. On the other hand, the open drain output would switch to a low logic level (*e.g.*, ground), and be put in a low impedance state, when the gate of the transistor is high, because the transistor would be on. *Id.* EX1003, ¶¶163,264.

This combined circuit would therefore include the transistor configurations recited in claims 3, 4 and 5, EX1003, ¶¶265,276,283 , the multiplexor configuration as recited in claims 6, 13 and 22, EX1003, ¶¶161,180,196, the open drain training sequence signals of claims 7 and 14, EX1003, ¶¶163,181, and the transistor signaling of claims 12, 20 and 23, EX1003, ¶¶180,187,197.

A Skilled Artisan would have been motivated to combine Kim into the obviousness combinations of Hazelzet and JEDEC or Buchmann. Kim is assigned to the same company as Hazelzet, includes some of the same disclosures, and discloses additional details regarding the use of an open-drain output to notify the memory controller of errors during parity and ECC normal operating modes. EX1017, 1:16-22, 5:49-57, 6:8-16. A Skilled Artisan would therefore have been motivated to consider them together. To use the output-pin scheme of Kim in the system of Hazelzet would also have been only the use of known techniques for their known purposes to achieve predictable results, *i.e.*, using an open-drain

output to provide error or status information from multiple components.

EX1003,¶257.

Kim and Hazelzet/JEDEC/Buchmann are analogous art to the 595 Patent for the reasons stated above. EX1003,¶267; § V.E.

A Skilled Artisan would have been motivated to use the open-drain techniques of Kim in the combinations analyzed here because it represented a well-known (and therefore reliable) and simple technique to provide error and/or status information from a number of components and in different modes.

EX1014,¶¶[0072],[0122]; EX1017, FIGs. 4-5, 5:65-6:18, 12:18-23; EX1003,¶152.

The open-drain technique of Kim permitted a single signal line with an “*OR logic element*” to indicate error or status information, thus simplifying the design of the system and saving pins on the various integrated circuits connected to the bus, which necessarily can have only a finite number of pins. Thus, a person of ordinary skill in the art could readily have modified Hazelzet’s open-drain output with the teachings of Kim and would have been motivated to do so.

EX1003,¶¶251,268-270,330-335,353,372,374.

VIII. CONCLUSION

Petitioner therefore respectfully requests that Trial be instituted and that claims 1-24 be canceled.

Dated: October 15, 2021

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Petition for *Inter Partes* Review of U.S. Patent No. 10,474,595

**PETITION FOR INTER PARTES REVIEW
OF U.S. PATENT NO. 10,474,595**

Attachment A:

Proof of Service of the Petition

CERTIFICATE OF COMPLIANCE

I hereby certify that this brief complies with the type-volume limitations of 37 C.F.R. § 42.24, because it contains 13,986 words (as determined by the Microsoft Word word-processing system used to prepare the brief), excluding the parts of the brief exempted by 37 C.F.R. § 42.24.

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CERTIFICATE OF SERVICE

I hereby certify that on this 15th day of October, 2021, a copy of this Petition, including all attachments, appendices and exhibits, has been served in its entirety by overnight mail on the following counsel of record for patent owner:

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Petition for *Inter Partes* Review of U.S. Patent No. 10,474,595

**PETITION FOR INTER PARTES REVIEW
OF U.S. PATENT NO. 10,474,595**

Attachment B:

List of Evidence and Exhibits Relied Upon in Petition

Petition for *Inter Partes* Review of U.S. Patent No. 10,474,595

Exhibit #	Reference Name
1001	U.S. Patent No. 10,474,595
1002	File History of U.S. Patent No. 10,474,595
1003	Declaration of Donald Alpert
1004	Curriculum Vitae of Donald Alpert
1005	File History of U.S. Patent Application No. 15/088,115 (i.e., U.S. Patent No. 9,858,218)
1006	File History of U.S. Patent Application No. 13/942,721 (i.e., U.S. Patent No. 9,311,116)
1007	File History of U.S. Patent Application No. 12/815,339 (i.e., U.S. Patent No. 8,489,837)
1008	U.S. Provisional App. No. 61/186,799
1009	U.S. Patent Publication No. 2010/0042778 to Tanguay et al.
1010	U.S. Patent Publication No. 2003/0115427 to Roohparvar
1011	U.S. Patent Publication No. 2010/0202240 to Moshayedi et al.
1012	U.S. Patent Publication No. 2008/0256281 to Fahr et al.
1013	U.S. Patent Publication No. 2010/0142383 to Goishi et al.
1014	U.S. Patent Publication No. 2008/0098277 to Hazelzet
1015	JEDEC COMMITTEE LETTER BALLOT, LRDIMM DDR3 Memory Initialization Chapter Proposal (Dec. 2009) (“JEDEC”)
1016	U.S. Patent No. 8,139,430 to Buchmann et al.
1017	U.S. Patent No. 8,359,521 to Kim et al.
1018	U.S. Patent No. 8,407,441 to Giovannini et al.
1019	U.S. Patent No. 8,489,837 to Lee
1020	U.S. Patent No. 3,414,781 to Dill
1021	<i>SK Hynix Inc. et al. v. Netlist, Inc.</i> , IPR2017-00548, Exhibit 1021, (PTAB December 11, 2017) (Deposition of Robert J. Murphy in 837 Patent IPR)
1022	U.S. Patent Application Pub. 2008/0147897 to Talbot
1023	U.S. Patent Application Pub. 2008/0155378 to Amidi

Exhibit #	Reference Name
1024	JEDEC Standard, Double Data Rate (DDR) SDRAM Specification, JESD79 (June 2000) (“JESD79”)
1025	JEDEC Standard, FBDIMM: Architecture and Protocol (January 2007) (“JESD206”)
1026	JEDEC Standard, FBDIMM Advanced Memory Buffer (AMB) (March 2007)(“JESD82-20A”)
1027	U.S. Patent No. 7,411,862 to Hein et al.
1028	US Patent App. Publication No. 2006/0277355 by <u>Ellsberry</u> et al.
1029	JEDEC Standard, Low Power Double Data Rate (LPDDR) SDRAM Specification (August 2007) (“JESD209”)
1030	[Intentionally omitted]
1031	U.S. Patent No. 9,535,623 (623 Patent)
1032	<i>SK hynix, Inc. et al. v. Netlist, Inc.</i> , IPR2018-00303, Paper No. 1 (PTAB December 14, 2017) (623 Patent IPR Petition)
1033	<i>SK hynix, Inc. et al. v. Netlist, Inc.</i> , IPR2018-00303, Exhibit 1003 (PTAB December 14, 2017) (Alpert Declaration in 623 Patent IPR)
1034	<i>SK hynix, Inc. et al. v. Netlist, Inc.</i> , IPR2018-00303, Paper No. 42 (PTAB March 21, 2019) (623 Patent Final Written Decision)
1035	<i>SK hynix Inc. et al. v. Netlist, Inc.</i> , IPR2017-00548, Paper No. 25 (PTAB May 3, 2018) (837 Patent Final Written Decision)
1036	JEDEC COMMITTEE LETTER BALLOT, DDR3 LRDIMM Design Specification Body (Dec. 2009)
1037	JEDEC, Compilation of Tallies for JC-40 CMOS Digital Logic and point committees (Dec. 4, 2009)
1038	File History of U.S. Patent Application No. 15/169,745 (i.e., U.S. Patent No. 9,535,623)
1039	Inphi Corporation, “MB Initialization sequence Item 142.35,” June 4, 2009
1040	U.S. Patent No. 8,386,737 to Jeon et al.

Exhibit #	Reference Name
1041	<i>SK hynix Inc. et al. v. Netlist, Inc.</i> , IPR2017-00548, Paper 14 (PTAB December 11, 2017).
1042	“Sequence,” https://www.lexico.com/en/definition/sequence
1043	U.S. Patent No. 7,222,213 to James
1044	“28-Bit to 56-Bit Registered Buffer with Address Parity Test One Pair to Four Pair Differential Clock PLL Driver” Texas Instruments (October 2008)
1045	“High-Speed DRAM Controller Design” Micron (2008)
1046	“Minutes of Meeting No. 158 JC-40 Digital Logic Committee” JEDEC (June 4, 2009)
1047	<i>SK Hynix Inc. et al. v. Netlist, Inc.</i> , IPR2017-00548, Exhibit 2009, (PTAB September 6, 2017)
1048	JEDEC, JEDEC Manual of Organization and Procedure, JM21P (Rev. of JM21N, May, 2008), (May, 2010)
1049	JEDEC, JEDEC Manual of Organization and Procedure, JM21N (Rev. of JM21M, December, 2006), (May, 2008)
1050	Declaration of Julie Carlson
1051	JEDEC, “Committee Letter Ballot, JC-40.4-09-320, Item 142.35,” (Dec. 2009)
1052	JEDEC, “Committee Letter Ballot, JC-45.4-09-321, Item 2192.44,” (Dec. 2009)
1053	JEDEC, “Tally of Votes, Committee Letter Ballot, JC-45.4-09-321, 2192.44” (Dec. 9, 2009)
1054	Declaration of John Halbert
1055	Declaration of Sung Joo Park
1056	JEDEC Stanard, DDR3 SDRAM, JESD79-3C (November 2008) (“JESD79-3C”)
1057	U.S. Patent No. 7,647,467 to Hutsell et al.
1058	<i>SK Hynix Inc. et al. v. Netlist, Inc.</i> , IPR2020-1042, Paper No. 1 (PTAB June 8, 2020) (595 Patent Petition)

Exhibit #	Reference Name
1059	<i>SK Hynix Inc. et al. v. Netlist, Inc.</i> , IPR2020-1042, Paper No. 14 (PTAB December 17, 2020) (595 Patent Institution Decision)
1060	<i>SK Hynix Inc. et al. v. Netlist, Inc.</i> , IPR2020-1042, Paper No. 25 (PTAB May 6, 2021) (595 Patent Termination Order)
1061	<i>Netlist, Inc. v. SK Hynix Inc. et al.</i> , 6-20-cv-00194-ADA (W.D. Tex. March 12, 2021) (Claim Construction Order)
1062	<i>SK Hynix Inc. et al. v. Netlist, Inc.</i> , IPR2020-1044, Paper No. 1 (PTAB June 8, 2020) (218 Patent Institution Decision)
1063	Netlist's 8-K announcing patent cross license with Samsung on November 12, 2015
1064	Defendant Samsung's Motion for Judgment on the Pleadings in <i>Netlist Inc. v. Samsung Electronics Co., Ltd.</i> , No. 8:20-cv-00993, ECF No. 60 (C.D. Cal. June 22, 2021)
1065	Order denying Samsung's Motion for Judgment on the Pleadings in <i>Netlist Inc. v. Samsung Electronics Co., Ltd.</i> , No. 8:20-cv-00993, ECF No. 120 (C.D. Cal. Aug. 5, 2021)
1066	Plaintiff Netlist's Motion for Partial Summary Judgment in <i>Netlist Inc. v. Samsung Electronics Co., Ltd.</i> , No. 8:20-cv-00993, ECF No. 145 (C.D. Cal. Aug. 16, 2021)
1067	Complaint for Declaratory Judgment of Non-Infringement in <i>Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.</i> , No. 1:21-cv-01453 (D. Del. filed Oct. 15, 2021)

**PETITION FOR INTER PARTES REVIEW
OF U.S. PATENT NO. 10,474,595**

**Attachment C:
Listing of The Claims of 10,474,595**

Claim	Claim Language
1.a	1. A memory module operable with a memory controller of a host system, comprising:
1.b	a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;
1.c	dynamic random access memory elements on the printed circuit board;
1.d	a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection; and

1.e	[i] wherein the memory module is configurable to operate in any of at least a first mode and a second mode; [ii] wherein the memory module in the first mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, [iii] wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations, and
	[iv] wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences;
1.f	[i] wherein the module controller is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations, [ii] wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and

	[iii] wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the first mode;
1.g	wherein the module controller in the second mode is further configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection to a first state or to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.
2	2. The memory module of claim 1, wherein the module controller comprises an integrated circuit.
3	3. The memory module of claim 1, wherein the module controller includes a notification circuit comprising a transistor having an open drain coupled to the open drain output and source coupled to the ground.
4	4. The memory module of claim 3, wherein the module controller is configurable to drive a gate of the transistor high so as to drive open drain output and the error edge connection to ground, or to drive the gate

	of the transistor low so as to drive the open drain output and the error edge connection to the high impedance state.
5	5. The memory module of claim 4, wherein the module controller is configurable to output the signal indicating a parity error having occurred by driving the gate of the transistor high to provide a low impedance path between the open drain output and the ground.
6	6. The memory module of claim 3, wherein the notification circuit further includes a multiplexor or a logic circuit having a output coupled to a gate of the transistor and configurable to drive the gate of the transistor with either a first signal related to the parity error or a second signal related to the one or more training sequences.
7	7. The memory module of claim 3, wherein the module controller is configurable to provide the information related to the one or more training sequences by driving a gate of the transistor with the second signal so as to drive the open drain output from the high impedance state to ground or from ground to the high impedance state.
8	8. The memory module of claim 1, wherein the second edge connections include one or more pins that are not active while the memory module is in the second mode.

9	9. The memory module of claim 1, wherein the memory module in the second mode is configurable to perform the operations related to the one or more training sequences without communicating data signals via the first edge connections while the memory module is in the second mode.
10.a	10. A memory module operable with a memory controller of a host system, comprising:
10.b	a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;
10.c	dynamic random access memory elements on the printed circuit board;
10.d	a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having

	an open drain output coupled to the error edge connection and configurable to drive the open drain output from a first state to a second state and from the second state to the first state, one of the first state and the second state being a low logic level, and the other one of the first state and the second state being a high impedance state; and
10.e	wherein the memory module is operable in at least a first mode in which the memory module is configurable to perform one or more memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, and a second mode in which the memory module is not accessed by the memory controller for memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences without communicating data signals via the first edge connections;
10.f	wherein the module controller in the first mode is configurable to receive via the second edge connections the address and control signals associated with the one or more memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first

	edge connections in accordance with the address and control signals, and wherein the module controller in the first mode is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred in the memory module while the memory module is in the first mode;
10.g	wherein the module controller in the second mode is further configurable to output to the memory controller open-drain signals related to the one or more training sequences via the open drain output and the error edge connection while the memory module is in the second mode.
11	11. The memory module of claim 10, wherein the module controller comprises an integrated circuit.
12.a	12. The memory module of claim 10, wherein the module controller includes a notification circuit having a transistor with an open drain coupled to the open drain output and a source coupled to the ground,
12.b	wherein the module controller is configurable to output to the memory controller the open-drain signals related to the one or more training sequences by driving a gate of the transistor high so as to drive

	the open drain output and the error edge connection to ground, and by driving the gate of the transistor low as to drive the open drain output and the error edge connection to the high impedance state,
12.c	and wherein the notification circuit is configurable to output the signal indicating a parity error having occurred by driving the gate of the transistor high to provide a low impedance path between the open drain output and ground.
13	13. The memory module of claim 12, wherein the notification circuit further includes a multiplexor or a logic circuit having an output coupled to the gate of the transistor and configurable to drive the transistor with either a first signal related to the parity error or a second signal related to the one or more training sequences.
14	14. The memory module of claim 10, wherein the module controller is configurable to output the open-drain signals related to the one or more training sequences by driving the open drain output from the high impedance state to the low logic level or from the low logic level to the high impedance state.

15	15. The memory module of claim 10, wherein the second edge connections include one or more pins that are not active while the memory module is in the second mode.
16	16. The memory module of claim 10, wherein the second edge connections include one or more high-order address pins that are not active while the memory module is in the second mode.
17.a	17. A method, comprising:
17.b	at a memory module coupled with a memory controller of a host system, the memory module including a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections, the memory module further including dynamic random access memory elements on the printed circuit board;
17.c	receiving via the second edge connections address and control signals associated with one or more memory read or write operations;

	controlling the dynamic random access memory elements to communicate data signals corresponding to the one or more memory read or write operations via the first edge connections in response to the address and control signals; outputting via an open drain output coupled to the error edge connection a signal indicating a parity error having occurred in the memory module while the memory module is being accessed by the memory controller for a memory read or write operation;
17.d	performing operations related to one or more training sequences while the memory module is not accessed by the memory controller for memory read or write operations; and outputting to the memory controller via the open drain output and the error edge connection open-drain signals related to the one or more training sequences and unrelated to any memory read or write operation.
18	18. The method of claim 17, wherein the second edge connections include one or more pins that are not active while the memory module is trained with the one or more training sequences.
19	19. The method of claim 18, wherein the second edge connections include one or more high-order address pins that are not

	active while the memory module is trained with the one or more training sequences.
20.a	20. The method of claim 17, wherein the memory module includes a notification circuit having a transistor with an open drain coupled to the open drain output and a source coupled to ground,
20.b	wherein outputting via an open drain output coupled to the error edge connection a signal indicating a parity error having occurred in the memory module comprises driving a gate of the transistor high to provide a low impedance path between the open drain output and ground, and
20.c	wherein outputting the open-drain signals related to the one or more training sequences and unrelated to any memory read or write operation comprises driving the gate of the transistor to drive the open drain output from a high impedance state to ground and from ground to the high impedance state.
21.a	21. A memory module operable with a memory controller of a host system, comprising:
21.b	a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical

	communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;
21.c	dynamic random access memory elements on the printed circuit board; and
21.d	a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller including a transistor having a gate and an open drain output coupled to the error edge connection; wherein the module controller is configurable to drive the gate of the transistor so as to drive the open drain output to a first state or a second state, the first state being a low logic level and the second state being a high impedance state;
21.e	[i] wherein the module controller is configurable to receive via the second edge connections memory commands associated with normal memory read or write operations and to output a set of address and control signals for each of the normal memory read or write operations; [ii] wherein the dynamic random access memory elements are configurable to communicate one or more N-bit-wide data signals with

	the memory controller via the first edge connections in response to the set of address and control signals, where N is at least 32; [iii] wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred during any of the memory read or write operations by driving the open drain output and the error edge connection to the first state;
21.f	wherein the memory module is configurable to perform operations related to one or more training sequences while the memory module is not accessed by the memory controller for memory read or write operations; and wherein the module controller is configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection from one of the first state and the second state to the other one of the first state and the second state.
22	22. The memory module of claim 21, wherein the module controller further includes a multiplexor or a logic circuit having an output coupled to the gate of the transistor, and wherein the module controller is configurable to drive the gate of the transistor with either a

	first signal related to the parity error or a second signal related to the one or more training sequences.
23.a	23. The memory module of claim 22, wherein the transistor has a source coupled to ground,
23.b	wherein the module controller is configurable to output the signal indicating a parity error having occurred by driving the gate of the transistor high to provide a low impedance path between the open drain output and ground, and
23.c	wherein the module controller is configurable to provide the information related to the one or more training sequences by driving the open drain output from a high impedance state to ground or from ground to the high impedance state.
24	24. The memory module of claim 21, wherein the memory module is configurable to perform the operations related to the one or more training sequences while the memory module is not communicating signals via the first edge connections.