

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner

Patent No. 10,474,595

Issued: November 12, 2019

Filed: December 28, 2017

Inventors: Hyun Lee

Title: Memory Module Having An Open-Drain Output Pin For Parity Error In a
First Mode and For Training Sequences In A Second Mode

Inter Partes Review No. IPR2022-00064

**DECLARATION OF DR. DONALD ALPERT REGARDING U.S. PATENT
NO. 10,474,595**

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I. INTRODUCTION

A. Engagement

1. I have been retained by counsel for Samsung Electronics Co., Ltd., Samsung Austin Semiconductor, LLC, and Samsung Semiconductor, Inc. ("Samsung") as an expert witness in the above-captioned proceeding. I have been asked to provide my opinion about the state of the art of the technology described in U.S. Patent No. 10,474,595 ("the 595 Patent") (Ex. 1001) and on the patentability of the claims of this patent. The following is my written declaration on these topics.

B. Background and Qualifications

2. I am an independent consultant with Camelback Computer Architecture, LLC. My residence and place of business is at 2020 21st Street, Sacramento, CA 95818. I am over the age of eighteen, and I am a citizen of the United States.

3. I have 45 years of academic and industrial experience in applying, designing, studying, teaching, and writing about microprocessors and computer systems. I received an Electrical Engineering Ph.D. degree in 1984 from Stanford University. I earlier received an Electrical Engineering B.S. degree from MIT in 1973 and an Electrical Engineering M.S. degree from Stanford University in 1978. I have taught classes in computer architecture at Stanford, Tel Aviv, and Arizona State Universities.

4. From 1976 to 1977, I worked at Burroughs Corporation, where I designed peripheral interface controllers, including those for serial data communications based on Intel 8080 microprocessor components. From 1980 to 1989, I was the lead architect for the design of three high-performance microprocessors at Zilog and National Semiconductor. Later, at Intel, I was the lead architect of the Pentium® Processor from 1989 to 1992 and of the 815 chipset from 1999 to 2000, both of which became the most widely used PC components of their time. The 815 chipset comprised two components: (1) a memory controller hub (MCH) that included a graphics controller and memory controller with interfaces to the CPU, 133 MHz SDRAM system memory modules, an optional, external graphics controller and (2) an I/O controller hub (ICH) that included various I/O controllers (*e.g.*, network, hard drive, USB) for system peripheral devices. Additionally, I served as co-manager for the Itanium processor design from 1993-1997.

5. I am a Senior Member of the Institute of Electrical and Electronics Engineers (IEEE), and served as the chair of the IEEE Technical Committee on Microprocessors and Microcomputers from 1999 to 2000. I was the keynote speaker at the first Cool Chips conference, dedicated to the study of low-power microprocessors and systems. I have given invited lectures at several universities, and published ten papers in various professional journals and conference

proceedings. My paper entitled "Architecture of the Pentium Processor," was selected as best paper in IEEE Micro for 1993. I am a named inventor on over 30 U.S. patents that pertain to microprocessors, computer systems, and related technology.

6. I have reviewed the 595 Patent, and I am familiar with the patent's subject matter, which is within the scope of my education and professional experience. Based at least on my background in academia, industry, and consulting, I am familiar with the issues and technology relating to processors, chipsets, memory, and peripheral devices for computer systems. I have personally analyzed, developed, and tested such computer components and systems. More specifically, the Pentium® Processor and 815 chipset for which I was the lead architect at Intel implemented various features for initializing, calibrating, and testing the memory system, which comprised cache memory, a memory controller, and standard SDRAM modules.

7. My Curriculum Vitae, including my publications and patents, is submitted herewith as Ex. 1004.

C. Compensation and Prior Testimony

8. I am being compensated at a rate of \$600.00 per hour for my study and testimony in this matter. I am also being reimbursed for reasonable and customary expenses associated with my work and testimony in this investigation.

My compensation is not contingent on the outcome of this matter or the specifics of my testimony.

9. I have previously submitted declarations in eight IPR proceedings, namely IPR2014-00970, IPR2014-00971, IPR2015-00148, IPR2015-00191, IPR2017-00548, IPR2018-00303, IPR2020-01042, and IPR2020-01044.

Additionally I have testified as an expert witness in Federal Court and the ITC, as summarized in Exhibit 1004 at 6-7.

D. Information Considered

10. My opinions are based on my years of education, research and experience, as well as my investigation and study of relevant materials. In forming my opinions, I have considered the materials I identify in this report and those listed in the Petition's Attachment B.

11. I may rely upon these materials and/or additional materials to respond to arguments raised by the Patent Owner. I may also consider additional documents and information in forming any necessary opinions — including documents that may not yet have been provided to me.

12. My analysis of the materials produced in this investigation is ongoing and I will continue to review any new material as it is provided. This report represents only those opinions I have formed to date. I reserve the right to revise,

supplement, and/or amend my opinions stated herein based on new information and on my continuing analysis of the materials already provided.

II. LEGAL STANDARDS FOR PATENTABILITY

13. In expressing my opinions and considering the subject matter of the claims of the 595 Patent, I am relying upon certain basic legal principles that have been explained to me.

14. First, I understand that for an invention claimed in a patent to be found patentable, it must be, among other things, new and not obvious from what was known before the invention was made.

15. I understand the information that is used to evaluate whether an invention is new and not obvious is generally referred to as “prior art” and generally includes patents and printed publications (*e.g.*, books, journal publications, articles on websites, product manuals, *etc.*).

16. I understand that in this proceeding the Petitioner has the burden of proving that the claims of the 595 Patent are anticipated by or obvious from the prior art by a preponderance of the evidence. I understand that “a preponderance of the evidence” is evidence sufficient to show that a fact is more likely true than it is not.

17. I understand that in this proceeding, the claims should be given their ordinary and accustomed meaning as understood by one of ordinary skill in the art

in view of the patent and its file history. The claims after being construed in this manner are then to be compared to the information in the prior art.

18. I understand that in this proceeding, the information that may be evaluated is limited to patents and printed publications. My analysis below compares the claims to patents and printed publications that are prior art to the claims.

19. I understand that there are various ways in which prior art may render a patent claim unpatentable. First, the prior art can be shown to “anticipate” the claim. Second, the prior art can be shown to have made the claim “obvious” to a person of ordinary skill in the art. Third, I understand that a patent claim may be invalid where the specification of the patent fails to provide a written description adequate to support the claim. Fourth, I understand that a patent claim may be invalid when the claim fails to particularly point out and distinctly claim the subject matter of what the inventor regards as the invention. My understanding of the legal standards is set forth below.

A. Anticipation

20. I understand that the following standards govern the determination of whether a patent claim is “anticipated” by the prior art.

21. I have applied these standards in my evaluation of whether the claims of the 595 Patent would have been anticipated by the prior art.

22. I understand that the “prior art” includes patents and printed publications that existed before the earliest filing date (the “effective filing date”) of the claim in the patent. I also understand that a patent will be prior art if it was filed before the effective filing date of the claimed invention, while a printed publication will be prior art if it was publicly available before that date.

23. I understand that, for a patent claim to be “anticipated” by the prior art, each and every requirement of the claim must be found, expressly or inherently, in a single prior art reference as recited in the claim. I understand that claim limitations that are not expressly described in a prior art reference may still be there if they are “inherent” to the thing or process being described in the prior art. For example, an indication in a prior art reference that a particular process complies with a published standard would indicate that the process must inherently perform certain steps or use certain data structures that are necessary to comply with the published standard.

24. I understand that if a reference incorporates other documents by reference, the incorporating reference and the incorporated reference(s) should be treated as a single prior art reference for purposes of analyzing anticipation.

25. I understand that it is acceptable to consider evidence other than the information in a particular prior art document to determine if a feature is necessarily present in or inherently described by that reference.

B. Obviousness

26. I understand that a claimed invention is not patentable if it would have been obvious to a person of ordinary skill in the field of the invention at the time the invention was made.

27. I understand that the obviousness standard is defined in the patent statute (35 U.S.C. § 103(a)) as follows:

28. A patent may not be obtained although the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be denied by the manner in which the invention was made.

29. I understand that the following standards govern the determination of whether a claim in a patent is obvious. I have applied these standards in my evaluation of whether the asserted claims of the 595 Patent would have been considered obvious as of the priority date of the patent.

30. I understand that to find a claim in a patent obvious, one must make certain findings regarding the claimed invention and the prior art. Specifically, I

understand that the obviousness question requires consideration of four factors (although not necessarily in the following order):

- The scope and content of the prior art;
- The differences between the prior art and the claims at issue;
- The knowledge of a person of ordinary skill in the pertinent art; and
- Whatever objective factors indicating obviousness or non-obviousness may be present in any particular case.

31. In addition, I understand that the obviousness inquiry should not be done in hindsight, but must be done using the perspective of a person of ordinary skill in the relevant art as of the effective filing date of the patent claim.

32. I understand the objective factors indicating obviousness or non-obviousness may include: commercial success of products covered by the patent claims; a long-felt need for the invention; failed attempts by others to make the invention; copying of the invention by others in the field; unexpected results achieved by the invention; praise of the invention by those in the field; the taking of licenses under the patent by others; expressions of surprise by experts and those skilled in the art at the making of the invention; and the patentee proceeded contrary to the accepted wisdom of the prior art. I also understand that any of this evidence must be specifically connected to the invention rather than being associated with the prior art or with marketing or other efforts to promote an invention. I am not presently aware of any evidence of “objective factors”

suggesting the claimed methods are not obvious, and reserve my right to address any such evidence if it is identified in the future.

33. I understand the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I also understand that an example of a solution in one field of endeavor may make that solution obvious in another related field. I also understand that market demands or design considerations may prompt variations of a prior art system or process, either in the same field or a different one, and that these variations will ordinarily be considered obvious variations of what has been described in the prior art.

34. I also understand that if a person of ordinary skill can implement a predictable variation, that variation would have been considered obvious. I understand that for similar reasons, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using that technique to improve the other device would have been obvious unless its actual application yields unexpected results or challenges in implementation.

35. I understand that the obviousness analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, but instead can take account of the “ordinary innovation” and experimentation that

does no more than yield predictable results, which are inferences and creative steps that a person of ordinary skill in the art would employ.

36. I understand that sometimes it will be necessary to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art. I understand that all these issues may be considered to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.

37. I understand that the obviousness analysis cannot be confined by a formalistic conception of the words “teaching, suggestion, and motivation.” I understand that in 2007, the Supreme Court issued its decision in *KSR Int’l Co. v. Teleflex, Inc.*, 550 U.S. 398, 418 (2007), where the Court rejected the previous requirement of a “teaching, suggestion, or motivation to combine” known elements of prior art for purposes of an obviousness analysis as a precondition for finding obviousness. It is my understanding that *KSR* confirms that any motivation that would have been known to a person of skill in the art, including common sense, or derived from the nature of the problem to be solved, is sufficient to explain why references would have been combined.

38. I understand that a person of ordinary skill attempting to solve a problem will not be led only to those elements of prior art designed to solve the

same problem. I understand that under the *KSR* standard, steps suggested by common sense are important and should be considered. Common sense teaches that familiar items may have obvious uses beyond the particular application being described in a reference, that if something can be done once it is obvious to do it multiple times, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle. As such, the prior art considered can be directed to any need or problem known in the field of endeavor and can provide a reason for combining the elements of the prior art in the manner claimed. In other words, the prior art does not need to be directed towards solving the same problem that is addressed in the patent. Further, the individual prior art references themselves need not all be directed towards solving the same problem.

39. I understand that obviousness does not require that the features of a secondary reference be bodily incorporated into the structure of the primary reference. Rather, the test is what the combined teachings of those references would have suggested to a Skilled Artisan. The disclosures of the prior art references need not be physically combinable. Combining the teachings of references should be the focus of the analysis.

40. I understand that an invention that might be considered an obvious variation or modification of the prior art may be considered non-obvious if one or more prior art references discourages or lead away from the line of inquiry

disclosed in the reference(s). A reference does not “teach away” from an invention simply because the reference suggests that another embodiment of the invention is better or preferred. My understanding of the doctrine of teaching away requires a clear indication that the combination should not be attempted (*e.g.*, because it would not work or explicit statements saying the combination should not be made).

41. I understand that a person of ordinary skill is also a person of ordinary creativity.

42. I further understand that in many fields, it may be that there is little discussion of obvious techniques or combination, and it often may be the case that market demand, rather than scientific literature or knowledge, will drive design trends. When there is such a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within their technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense. In that instance the fact that a combination was obvious to try might show that it was obvious. The fact that a particular combination of prior art elements was “obvious to try” may indicate that the combination was obvious even if no one attempted the combination. If the combination was obvious to try (regardless of whether it was actually tried) or

leads to anticipated success, then it is likely the result of ordinary skill and common sense rather than innovation.

III. THE 595 PATENT

A. Effective Filing Date of the 595 Patent

43. The 595 Patent is a continuation of, inter alia, a utility application filed June 14, 2010, and also claims priority to U.S. Provisional Application No. 61/186,799 (EX1008, “the provisional” or “the provisional application”), filed June 12, 2009. EX1001, Face. I have been asked to give my opinion as to whether, from the perspective of a Skilled Artisan, the provisional application shows that the inventor actually invented what is claimed in each of the claims of the 595 patent, and possessed the claimed subject matter, as of the provisional filing date. When considering that question, I have considered whether the provisional explicitly or inherently discloses the elements of the claims. To determine whether the provisional inherently discloses an element, I considered whether any element not explicitly disclosed would be necessarily comprehended in the description provided by a Skilled Artisan. I conclude that certain elements of some claims are not adequately disclosed in the provisional. I understand that in IPR2020-01042, the Board agreed that that each of the limitations below are not adequately disclosed in the provisional. EX1059, 27. As such, the Board agreed that the claims are not entitled to the provisional filing date. EX1059, 27. I understand that in

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related application, IPR2020-01044, the Board also noted that SK hynix
successfully showed that JEDEC qualifies as prior art. EX1062, 31.

1. Unsupported Negative Limitation

44. Each independent claim of the 595 Patent requires the negative limitation that the memory controller not access the module for memory read and write operations while performing training sequences (in some claims referred to as the “second mode” that includes training sequences). *E.g.*, EX1001, 14:63-65 (claim 1: “wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations”), *see also id.*, 16:14-22 (claim 10: “wherein the memory module is operable in at least ... a second mode in which the memory module is not accessed by the memory controller for memory read or write operations”), 17:41-44 (claim 17: “performing operations related to one or more training sequences while the memory module is not accessed by the memory controller for memory read or write operations”), 18:42-46 (claim 21: “wherein the memory module is configurable to perform operations related to one or more training sequences while the memory module is not accessed by the memory controller for memory read or write operations”).

45. The provisional says nothing about the memory controller not accessing the module for read and write operations in a training mode, that is, a mode which includes training sequences. Indeed, it mentions the word “training” in

only one sentence fragment in a legend to a figure, never explains that such training may occur in its own mode, never uses the word “mode” at all, and never says anything about what operations may or may not occur in the training mode. On the contrary, the provisional states: “In the notifying method, the memory subsystem controller sends a signal to the MCH[, e.g., a system memory controller,] when it completes the required or requested operation. This method allows the MCH to execute independent commands while it is waiting for a notification signaling for the memory subsystem controller.” EX1008, 22. Since each independent claim of the ’595 patent requires such notification (providing information/signals related to the training sequences), the claims also allow the possibility of the MCH to execute independent commands. Thus, if anything, this suggests read and write operations very much may be occurring during the disclosed “MB training.”

46. My opinion is that the negative limitation is not “necessarily comprehended” in the provisional’s disclosure. The 595 Patent itself states that both system memory controller memory operations and training sequences can occur during an initialization mode, confirming that both can occur during the same mode. EX1001, 6:26-30, 6:45-56

47. As noted above, the provisional uses the word “training” in only one sentence fragment, as follows: “Error-Out pin: Low during MB training (high

signal indicates that training is done).” EX1008, 25 (Fig. 3 description). To the extent a Skilled Artisan would understand “MB training” as anything more than a generic reference to “training” in the context of memory buffers (and that is all I believe a Skilled Artisan would understand), a Skilled Artisan would, at most, understand “MB training” in the context of the provisional’s reference to “the recent proposal in JEDEC for L[R]-DIMM (Load Reduced DIMM)” which was under development/standardization at the time. EX1008, 22. Although the provisional does not identify the specific “recent proposal in JEDEC,” a Skilled Artisan would have understood at the time that JEDEC was evaluating proposals for training the interfaces of a Memory Buffer used in the then current DDR3 LRDIMMs under development/standardization – a type of register/buffer in DDR3 LRDIMMs that buffered both address and data signals. EX1036, 5 (“Product Description”).

48. It was well-known, however, that some types of memory buffers employed normal memory read and write operations instituted by the system memory controller during the training mode. For instance, JEDEC, a ballot on a draft DDR3 LRDIMM standard discloses a Host-MB training during initialization that employs normal memory read and write operations instituted by the system memory controller. EX1015, 8-9 (“The host performs normal writes to DRAM for write DQ/DQS margining ...[t]he host performs read DQ/DQS margining by using

normal reads from DRAM ...”). On the other hand, “MB-DRAM Training,” also performed during initialization, did not require memory read or write operations by the host. *Id.*, 8 (“Once enabled, the MB assumes autonomous control of the Command/Address, Control and Data/Strobe signals to the DRAMs, without any further assistance from the host. ... No DRAM commands or control word writes (either over the Command/Address and Control buses or via SMBus) can be issued to the MB until the MB-DRAM Interface training is complete and the DODTn inputs must be kept low.”); *see also* EX1039, 7-9, 11 (Inphi’s presentation dated June 4, 2009 disclosing “Host-MB Training” and “MB-DRAM Training” before the June 12, 2009 provisional filing date); *see also* EX1046, 1-2, 21 (June 4, 2009 meeting minutes noting Inphi’s MB Initialization Sequence, EX1039, was discussed). I note that, in MB-DRAM Training, at least one JEDEC document (EX1039, 7-9) at the time suggests the memory buffer performs operations such as pre-charge, but those would not be considered “memory read or write operations” (or “normal memory read or write operations”) per the claims because they are not performed by the system memory controller (rather the memory buffer performed them).

49. As another example, Talbot discloses that during normal operations normal read and writes are stored in FIFO 220 in the buffer, and are then passed on to DRAM. EX1022, ¶¶ [0039], [0043]. Additionally, during training, the controller

may write data, which is also stored in FIFO 220; however, in this case, the data is not passed to DRAM. EX1022, ¶[0053]. Based on this disclosure a Skilled Artisan would conclude that the memory controller is using the same normal write operation in both modes.

50. To the extent Patent Owner might argue that the provisional application also mentions that the MCH (system memory controller or host could be in “standby (idle or wait) while the memory subsystem controller completes its task,” EX1008, 22-23, this disclosure is unrelated to the claimed lack of read or write operations. Instead, as the Board noted in IPR2020-01042, the Patent Owner only “points to language from the provisional application describing the previous art, not the alleged improvement, as support for the claimed negative limitation,” EX1059, 23. Specifically, the provisional application states “[t]he shortcoming of the current ... LR-DIMM proposal is that, instead of adopting the notification, the proposal requires the MCH to be in standby (idle, or wait) while the memory subsystem controller completes its task.” EX1008, 22-23. Thus, a Skilled Artisan would have understood that the provisional application tried to get rid of the “shortcoming” of the prior art LR-DIMM proposal, and that “shortcoming” included the MCH (host) being in the “standby (idle, or wait)” state. Indeed, as discussed above, the provisional expressly states that its advantageous “[notifying]

method allows the MCH to execute independent command while it is waiting for a notification signaling.” Ex1008, 22.

2. **“One or More” Training “Sequences”**

51. Each independent claim of the 595 Patent requires the ability to “perform operations related to one or more training sequences.” *E.g.*, EX1001, 14:65-67 (claim 1: “wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences”), *see also id.*, 16:22-25 (claim 10), 17:41-42 (claim 17), 18:42-43 (claim 21). The independent claims also require providing information or signals “related to the one or more training sequences.” *Id.*

52. The provisional, however, only discloses a single “MB training”, that a Skilled Artisan would understand as a generic disclosure of “training” a memory buffer in some way. It does not disclose any training “sequences,” and particularly not “one or more” training sequences, much less providing information or signals related to such specific “training sequences.” Indeed, the phrases “train sequence” and “training sequences” are completely absent from the provisional. Instead of the specifically claimed “one or more training sequences,” the provisional associates the notifying function of the error-out signal with the generic term “MB training.” EX1008, 25. The provisional application’s passing mention of “initialization

operation sequences,” *id.*, 22, does not disclose “training sequences” either, since a Skilled Artisan would have understood that the term “initialization operation sequences” refers to a generic description of initialization, and is not limited to any specific “training sequences.” A Skilled Artisan would not “necessarily comprehend” the term “one or more training sequences” and its relation with the notification functionality from the bare disclosure of “MB training” as of June 12, 2009, the filing date of the provisional application.

3. “one or more N-bit-wide data signals”

53. Claim 21 requires “wherein the dynamic random access memory elements are configurable to communicate one or more N-bit-wide data signals with the memory controller via the first edge connections in response to the set of address and control signals, where N is at least 32.” EX1001, 18:31-35. However, dynamic random access memory or DRAM is mentioned just once in the provisional, in the following sentence: “This method allows the MCH to work with a non-homogenous memory subsystem, such as mixing of DIMMs with different DIMM density, ranks, DRAM density, speed, DRAM configuration, etc.” EX1008, 23. And the terms “data signal,” “bit,” “width,” and “32” are found nowhere in the provisional, much less the concept of data signals of a certain width, particularly “at least 32.” There is no support for this limitation of this claim in the provisional.

Nor would a Skilled Artisan “necessarily comprehend” such a disclosure from what is included in the provisional.

4. “one or more pins that are not active”

54. Claims 8, 15, 16, 18, and 19 require that “the second edge connections [for address and control signals] include one or more pins that are not active while the memory module is in the second mode [including training sequences],” or a substantially similar “not active” limitation. EX1001, 15:5153; *see also id.* at 17:7-13 (claims 15-16), 17:49-56 (claims 18-19). However, the terms “edge,” “second edge connection[s for address and control signals],” “mode” and “active” appear nowhere in the provisional, much less the concept that pins for address and control signals on an edge connection are not active during certain modes. There is simply no support whatsoever for these claims in the provisional. Nor would a Skilled Artisan “necessarily comprehend” such a disclosure from what is included in the provisional. For example, as discussed above, a Skilled Artisan would have understood that “training,” in general, does not exclude receiving read or write commands, including address and control signals, from the host. *Supra*, ¶¶44-50.

B. Person Of Ordinary Skill in the Art

55. Based on my experience and the prior art I discuss herein, I believe a person of ordinary skill in the art in the field of the 595 Patent would be someone who was familiar with computer memory systems and basic CPU architecture

documented in the computer/memory architecture literature and generally available in commercial systems as of 2009-10. Such literature and commercial systems would have included techniques related to how computer components access a computer's memory, including the role of a memory controller, the basic operation of memory modules and devices, and the techniques used to couple memory devices to the other components of the computer system. They would also include schemes for initialization of computer systems, including initialization/training of memory components. Such a person would also have been familiar with the standards that govern the operation of memory devices. The person of ordinary skill in the art would have had a bachelor's degree in computer engineering, or a related field, and several years of additional experience working with computer memory systems. Alternatively, such a person could have had equivalent combinations with more or less education and less or more experience.

C. Overview of The 595 Patent

56. The 595 Patent states that it describes “a method of establishing a handshake mechanism based on notification signaling.” EX1001, 4:5-7. The 595 Patent explains that “this [handshake] mechanism can be implemented by adding a new interface (notifying) signal between the MCH [i.e., system memory controller] and the memory subsystem controller, or by adding an additional functionality to an existing, non-timing critical signal without altering the memory subsystem

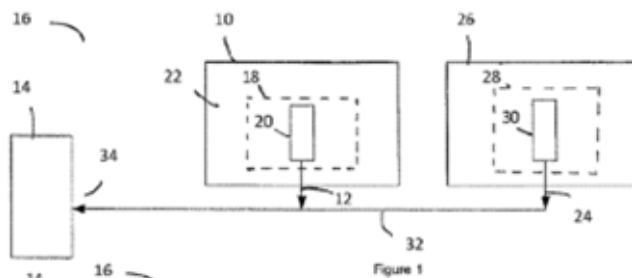
hardware.” EX1001, 4:7-12. The 595 Patent further explains that this interface “can be an open drain signaling from the memory subsystem controller to the MCH [i.e., system memory controller].” EX 1001, 4:12-16.

57. According to the 595 Patent, before the patent “[i]n general, there [was] *no existing method of handshaking* between the MCH (*e.g.*, system memory controller) and a memory subsystem (*e.g.*, memory module) during initialization.” Ex. 1001 (595 Patent) at 2:64-67 (emphasis added). For example, “in conventional systems, the system memory controller does not monitor the error-out signal from the memory subsystem.” *Id.* at 2:67-3:2. The 595 Patent states that the MCH in “typical” servers of the prior art would have “complete control over the initialization procedure” so the lack of handshaking “has not been a serious issue.” *Id.*, 2:65-3:3. For the LR-DIMM (Load Reduced DIMM) of the time, however, the MCH hands over parts of the initialization operations to a memory module, and simply waits a predetermined amount of time assuming that the memory module had completed those initialization operations. EX1001, 3:3-22. In particular, the provisional application, incorporated by reference in its entirety into the ’595 patent, EX1001, 1:17-19, admits that a prior art “LR-DIMM proposal [in JEDEC] requires the MCH to insert a waiting period.” EX1008, 22.

58. The 595 Patent suggests that use of “handshaking” between memory controller and memory module (i.e., exchanging information about the completion

of the initialization procedure) would be a better idea. EX1001, 2:58-63. It states that, generally, “handshaking can be implemented in at least two ways; polling and notifying.” EX1001, 3:43-44. The 595 Patent claims that polling is “generally inefficient because the system memory controller does not know exactly when the memory subsystem will have completed the required or requested operation,” thus causing the controller to “wait longer than necessary to poll the memory subsystem, thereby delaying the overall initialization process.” EX1001, 3:48-54. It further states that “the notifying method is an advantageous handshaking method between the MCH and the memory subsystem controller.” EX1001, 3:63-65.

59. The 595 Patent provides only limited detail on what it purports to be the inventive system. Figure 1, for example (below), depicts an embodiment. That figure shows a computer system including a memory module 10 coupled to a memory controller 14 via “output 12” which is driven by a notification circuit 20 of controller circuit 18.



Ex. 1001 (595 Patent) at 4:24-42, FIG. 1. Another memory module 26 is also shown, and has essentially in the same structure as module 10, coupled to the same

memory controller 14 via “output 24” driven by notification circuit 30 of controller circuit 28. *Id.* at 6:23-44.

60. In one specific example of handshaking described in the 595 Patent, the interface between the memory controller (MCH) and memory subsystem controller (of the memory module) is implemented using a technique called open drain signaling. EX1001, 4:12-16; *see also id.* at 9:47-53, FIGs. 2-3. Specifically, output 12 of module 10 and output 24 of module 26 are both tied to the same bus 32 using an open drain configured transistor. Ex. 1001 (595 Patent) at 4:12-23, 9:51-67, FIGs. 2-3.

61. In that configuration, when starting an initialization procedure, each memory module will drive high the gate of the transistor with the open drain output, placing a logic level low (low impedance) signal on bus 32. When the initialization is complete, the memory module can drive low the gate of the transistor with the open drain output, placing a logic level high (high impedance) signal on bus 32. However, because all of the outputs of multiple memory modules are tied to the same bus 32 in an open drain configuration, the state of bus 32 will remain logic level low (low impedance) until each memory module drives low the gate of the transistor of its open drain output, placing a logic level high (high impedance) on its output, which then allows “the bus 32 [to] be pulled high by the internal pull-up configuration 40 of the system memory controller 14.” Ex. 1001

(595 Patent) at 9:47-10:50. In this manner, the system memory controller may be provided the status of an initialization procedure (*e.g.*, either that it is currently executing or complete) using only a single bus line from multiple memory modules. *Id.* The 595 Patent further states that bus 32 could be tied to a standard-defined (such as JEDEC) error output pin that is not required by the standard to be used during initialization. EX1001, 8:4-33.

62. The patent further states that output 12 can be operatively coupled to the error-out pin of the memory module 10, which is connected to a multiplexor 42 driving the transistor 36 with either of a task_in_progress signal 44 or an error signal 46 (*e.g.*, parity error signal). Ex. 1001 (595 Patent) at 11:19-23, FIG. 3. According to the 595 Patent, “the memory module 10 can be advantageously configured to both perform the standard (*e.g.*, JEDEC-specified) error reporting functionality via the error-out pin during the operational mode and provide the status notification functionality during the system initialization mode.” Ex. 1001 (595 Patent) at 11:29-34.

D. The Prosecution History of The 595 Patent

1. 553 Application (The 595 Patent)

63. The 595 Patent issued from U.S. Patent Application Serial No. 15/857,553 (“553 Application”), which is a continuation of U.S. Patent Application Serial No. 15/088,115 (“115 Application”), filed on April 1, 2016,

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now U.S. Patent No. 9,858,218 (“218 Patent”), which is a continuation of U.S. Patent Application Serial No. 13/942,721 (“721 Application”), filed on July 16, 2013, now U.S. Patent No. 9,311,116, which is a continuation of U.S. Patent Application Serial No. 12/815,339 (“339 Application”), filed on June 14, 2010, which is now U.S. Patent No. 8,489,837 (“837 Patent”), which in turn claims priority to U.S. Provisional Application 61/186,799 filed June 12, 2009. Ex. 1001 (595 Patent) at 1-2.

64. The 553 Application presented 7 claims. Ex. 1002 (595 Patent File History) at 32-33. On August 28, 2018, the examiner rejected claims 1-7 on the ground of “nonstatutory double patenting as being unpatentable over claims 1-18 of U.S. Patent No. 8,489,837; claims 1-20 of U.S. Patent No. 9,311,116; and claims 1-22 of U.S. Patent No. 9,858,218.” Ex. 1002 (595 Patent File History) at 83. The examiner found:

Although the claims at issue are not identical, they are not patentably distinct from each other because the pending claims make obvious the claims of the issued patents and vice versa.

EX1002, 83, ¶3.

65. In response, the applicants of the 553 Application filed a terminal disclaimer on November 28, 2018. Ex. 1002 (595 Patent File History) at 106-107. The applicants further amended claims 4, 5, and 7 and added claims 8-20. Ex. 1002 (595 Patent File History) at 104.

66. On February 6, 2019, the examiner issued a notice of allowance. Ex. 1002 (595 Patent File History) at 121-122.

67. On March 1, 2019, the applicants of the 553 Application filed a Request for Continued Examination along with an Amendment. Ex. 1002 (595 Patent File History) at 145-154. In the Amendment, the applicants amended the claims to remove the term “handshake” from all claims and add other terms. *See, e.g.*, Ex. 1002 (595 Patent File History) at 149, 151.

68. On March 21, 2019, The Board’s final decision in IPR2018-00303 was disclosed in a filed IDS. EX1002, 175.

69. On March 29, 2019, the examiner issued a second notice of allowance. EX1002, 182-183. The Examiner did not cite the March 21 IDS, citing, instead, a March 1 IDS. EX1002, 186. Similarly, the list of references considered by the examiner issued with that Notice of Allowance does not list the final written decision in IPR2018-00303. *See id.*, 194-201

70. On July 1, 2019, the applicants of the 553 Application filed another Request for Continued Examination along with an Amendment. Ex. 1002 (595 Patent File History) at 222-233. In the Amendment, the applicants amended claims 1, 3-8, 10, 12-15, 17-18, 20, and added new claims 21-24. *Id.* at 224-233.

71. On August 9, 2019, the examiner issued a third notice of allowance. EX1002, 243-244.

72. On September 15, 2019, the Examiner filed an IDS with a list of references considered, including, for the first time, the final decision in IPR2018-00303. EX1002, 265.

2. 115 Application (The 218 Patent)

73. The 218 Patent issued from the 115 Application. The 115 Application presented 20 claims, 1-20. Ex. 1005 (115 Application File History) at 30-33 (Application at 20-23). On May 20, 2016, the examiner rejected claims 1-20 on the ground of nonstatutory double patenting as being unpatentable over claims 1-20 of U.S. Patent No. 9,311,116 and claims 1-18 of U.S. Patent No. 8,489,837. Ex. 1005 (115 Application File History) at 49-57. Claims 1-20 were rejected also under 35 U.S.C. 103(a) as being unpatentable over Tanguay (Ex. 1009, US 2010/0042778) in view of Roohparvar (Ex. 1010, US 2003/0115427). *Id.*

74. In response, the applicants of the 115 Application cancelled claims 1-20, and added new claims 21-42. Ex. 1005 at 68-81. The applicants also filed a terminal disclaimer to overcome the nonstatutory double patenting rejections. *Id.*

75. On November 25, 2016, the examiner rejected claims 21-42 as being unpatentable over Moshayedi (Ex. 1011, U.S. 2010/0202240) in view of Fahr (Ex. 1012, U.S. 2008/0256281). Ex. 1005 (115 Application File History) at 100-107.

76. On April 25, 2017, the applicants of the 115 Application filed a Response. Ex. 1005 (115 Application File History) at 132-144. In the Response,

the applicants amended claims 21 and 35 to “address issues with antecedent basis and for better clarity.” *Id.* at 138.

77. The applicants further argued that the Applicant is left to guess what the Examiner’s rationale is in rejecting the claims under Moshayedi in view of Fahr, because Moshayedi shows several outputs including “CACHE_DIRTY, DRAM_AVAILABLE, NVDIMM READY, TEST TX, and VBACK RESET,” that cannot be “an open drain output” outputting “a signal indicating a parity error.” Ex. 1005 at 139-141. The applicants further argue that Moshayedi fails to disclose “configured to receive from the memory controller via the second edge connections address and command signals associated with one or more memory read, write, pre-charge, or refresh operations and to control the memory elements in accordance with the address and command signals,” *id.* at 142, and “wherein the module controller is further configured to process one or more training sequences unrelated to any memory read, write, pre-charge, or refresh operation, and wherein the module controller is further configured to drive a notification signal associated with the one or more training sequences to the memory controller via the open drain output of the module controller and the error edge connection.” *Id.* at 143.

78. The applicants further argued that Fahr does not make up for the deficiency of Moshayedi, because the Fahr describes “two open-drain outputs for two different error signals, /Error (CE) 120 and /Error (UE) 121, respectively,”

while the claim requires “that the module controller ‘outputs to the memory controller a signal indicating a parity error’ AND ‘is further configured to drive a notification signal associated with the one or more training sequences to the memory controller’ **via the same open-drain output.**” Ex. 1005 (115 Application File History) at 143. (emphasis in original).

79. On May 25, 2017, the applicants of the 115 Application further filed an Amendment, amending claims 21, 22, 28-29, 34-36, and 42, responding to the Final Office Action dated November 25, 2016. Ex. 1005 (115 Application File History) at 167-179. In this Amendment, the applicants made similar arguments as in its April 25, 2017 Response. *Id.*

80. On May 31, 2017, the applicants of the 115 Application conducted an interview with the Examiner, discussing “the AFCP 2.0 filed 04/25/17 and potential claim amendments to overcome the art of record.” Ex. 1005 (115 Application File History) at 182.

81. On June 16, 2017, the examiner rejected claims 21-42. Ex. 1005 (115 Application File History) at 184-191. In particular, the examiner rejected claims 21-42 under 35 U.S.C. 112(a), as failing to comply with the written description requirement, because the newly added limitations to claims 21, 29, and 35 (*i.e.*, “‘wherein the one or more training sequences are not associated with any memory read or write operation,’ ‘while the memory module is not performing any memory

read or write operation,’ ‘while the memory module is not performing any memory read or write operation,’” respectively”) are not supported by the original disclosure and constitute new matter. Ex. 1005 (115 Application File History) at 186-187. The examiner further rejected claims 21-42 as being unpatentable over Moshayedi (Ex. 1011, U.S. 2010/0202240) in view of Fahr (Ex. 1012, U.S. 2008/0256281) and Goishi (Ex. 1013, U.S. 2010/0142383). Ex. 1005 (115 Application File History) at 188-190.

82. On July 14, 2017, the applicants of the 115 Application conducted an interview with the Examiner, discussing “the rejection of claims 21-42 under 35 USC 112 first paragraph and 35 USC 103 over Moshayedi (20100202240), Fahr (20080256281), and Goishi (20100142383), as well as potential claim amendments to overcome the pending rejections.” Ex. 1005 (115 Application File History) at 201.

83. On September 18, 2017, the applicants of the 115 Application filed an Amendment, amending claims 21, 27-29, 33-35, and 41-42, responding to the Non-Final Office Action dated June 16, 2017. Ex. 1005 (115 Application File History) at 203-216. In this Amendment, the applicants made similar arguments as in its April 25, 2017 Response with respect to Mosheyedi and Fahr. Ex. 1005 (115 Application File History) at 210-216. The applicants further argued that Goishi

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does not make up for the deficiencies of Moshayedi and Fahr without any substance. Ex. 1005 (115 Application File History) at 216.

84. On October 12, 2017, the examiner issued a notice of allowance, allowing claims 21-42 of the 115 Application. Ex. 1005 (115 Application File History) at 228-232.

3. 745 Application (The 623 Patent)

85. The 623 Patent issued from U.S. Patent Application 15/169,745. The 745 application presented 37 claims. The 745 application was accorded a filing date of June 6, 2016.

86. On July 29, 2016, the claims were rejected “on the ground of nonstatutory double patenting as being unpatentable over claims 1-20” of the 116 Patent, requiring Patent Owner to file a terminal disclaimer to overcome the rejection:

Although the claims at issue are not identical, they are not patentably distinct from each other because the claims ... make obvious the claims of the issued patent and vice versa.

EX1038, 57, ¶3. Patent Owner likewise had to file a terminal disclaimer over the 837 Patent when prosecuting the application that became the 623 Patent. EX1038, 79 (disclaiming over application that issued as ‘218 patent, which disclaims over the ‘837 patent); EX1005, 61.

4. 721 Application (The 116 Patent)

87. The 116 Patent issued from the 721 Application. The 721 Application presented 15 claims, 1-15 (Application at 21-23) Ex. 1006 (721 Application File History) at 27-29.

88. On August 5, 2014, the applicants of the 721 Application filed a Preliminary Amendment amending claims 1 and 11-15, canceling claims 4 and 8-10, and adding new claims 16-24. Ex. 1006 (721 Application File History) at 5460.

89. On May 22, 2015, the examiner rejected claims 1-7 and 11-24 on the ground of nonstatutory double patenting as being unpatentable over claims 1-18 of U.S. Patent No. 8,489,837 (Ex. 1019). Ex. 1006 (721 Application File History) at 64-69.

90. On August 24, 2015, the applicants of the 721 Application filed a terminal disclaimer to overcome the double patenting rejection. Ex. 1006 (721 Application File History) at 74-80, 86.

91. On November 16, 2015, the examiner issued a Final Office Action maintaining the double patenting rejection noting that “the person who signed the terminal disclaimer is not an attorney or agent of record, is not recognized as an officer of the assignee, and has not been established as being authorized to act on behalf of the assignee.” Ex. 1006 (721 Application File History) at 92.

92. On January 21, 2016, the applicants of the 721 Application filed a “properly signed terminal disclaimer” to overcome the double patenting rejection. Ex. 1006 (721 Application File History) at 97, 99-104.

93. On February 24, 2016, the examiner issued a Notice of Allowance, allowing claims 1-3, 5-7, and 11-24 of the 721 Application. Ex. 1006 (721 Application File History) at 115-119.

5. 339 Application (The 837 Patent)

94. The 623 Patent issued from the 339 Application. The 339 Application presented 20 claims, 1-20. Ex. 1007 (339 Application File History) at 28-31. On September 14, 2012, the examiner rejected claims 1-3, 5, 7, 11, 14, and 19, and allowed claims 4, 6, 8-10, 12, 13, 15-18, and 20. Claims 5 and 11 were rejected under 35 U.S.C. 112, first paragraph. Ex. 1007 (339 Application File History) at 60-61. Claims 1-3, 5, 7, 11, 14, and 19 were rejected under 35 U.S.C. 103(a) as being unpatentable over Tanguay (Ex. 1009, US 2010/0042778) in view of Roohparvar (Ex. 1010, US 2003/0115427). Ex. 1007 (339 Application File History) at 61-67.

95. In response, the applicants of the 339 Application noted that the examiner’s 112 rejection must have referred to claims 5 and 14 not 5 and 11, and cancelled claims 5 and 14. EX1007, 90.

96. The applicants of the 339 Application also amended claims 1, 4, 11, and 19. Claim 1 was amended to add “wherein the at least one notification signal triggers the memory controller to execute an interrupt routine,” claim 4 was amended to remove “and the memory controller is responsive the at least one notification signal indicating completion of the at least one initialization sequence by triggering execution of an interrupt routine by the memory controller.” Ex. 1007 at 85. According to the applicants, the amendment to claim 1 rendered claims 1-3 patentable over Tanguay in view of Roohparvar. EX1007, 91.

97. On April 29, 2013, the examiner issued a notice of allowance, allowing claims 1-4, 6-13, and 15-20 of the 339 Application. EX1007, 121.

6. IPR2018-00303

98. U.S. Patent No. 9,535,623 (“623 Patent”) is related to the 595 Patent. Both the 623 Patent and the 595 Patent claims priority to and share the specification of the same parents (*e.g.*, 218 Patent and 837 Patent). The claims of both 595 Patent and 623 Patent are strikingly similar. Just by way of example, claim 1 of both patents arise directed to a memory module on a printed circuit board having various edge connections, including an error edge connection. Ex. 1001 at claim 1; Ex. 1031 at claim 1. Both require that the module operate in two modes, one for normal operation and one for training. *Id.* And both require an open

drain output that is used both for parity error during normal operation and for a notification signal during training. *Id.*

99. SK hynix filed a petition for inter partes review of the 623 Patent based primarily on US Patent Publication 2008/0098277, dated April 24, 2008 (“Hazelzet”) combined separately with several different references, most important for purposes of my analysis here US Patent 8,139,430, issued March 20, 2012 (“Buchmann”). Ex. 1032 (623 IPR Petition) at 61-67.

100. SK hynix’s petition also relied on my analysis and testimony concerning the obvious combination of Hazelzet and Buchman. In particular, I demonstrated in my direct testimony that Hazelzet, Buchmann and the 623 Patent were analogous art, Ex. 1033 (623 Patent IPR Declaration) at ¶172, and that Hazelzet and Buchman could be combined such that the same open drain output of Hazelzet could be used for a parity error signal during normal operations, as disclosed in Hazelzet, and also for a training sequence notification signal, such as “TS0_done,” “TS3_ack,” and “TS3_done,” as disclosed in Buchmann, Ex. 1033 (623 Patent IPR Declaration) at ¶¶167, 170; *see also id.* at ¶¶164-174.

101. I further demonstrated that a person of ordinary skill in the art would have been motivated to make this combination because, among other things, it would have improved overall system reliability, EX1033, ¶173, would have complemented Hazelzet’s existing initialization sequence, *id.* at ¶174, and “would

have been merely a use of prior art techniques for prior art purposes with only expected results,” *id.* at ¶175.

102. The Board issued a Final Written Decision in IPR2018-00303 on March 21, 2019, finding all claims of the 623 Patent unpatentable based on, among other grounds, the obvious combination of Hazelzet and Buchmann. Ex. 1034 (623 Patent IPR, Final Written Decision) at 21. In coming to that conclusion, the Board stated that “we agree with Petitioner’s showing that the combination of Hazelzet and any one of Buchmann or Talbot teaches every limitation of claims 1, 12, and 21 of the ‘623 patent and that a person of ordinary skill in the art would have had reason, with rational underpinning, to combine the references.” Ex. 1034 (623 Patent IPR, Final Written Decision) at 13. In support of that conclusion, the Board stated “[f]urther, we credit Dr. Alpert’s supporting testimony (Ex. 1003 ¶¶ 121–150, 158–186), as it is consistent with the prior art disclosures.” Ex. 1034 (623 Patent IPR, Final Written Decision) at 13.

103. The Board’s Final Written Decision in IPR2018-00303 was provided to the examiner of the 595 Patent, and the examiner indicated that the Final Written Decision was considered. Ex. 1002 (595 Patent File History) at 265. However, no analysis or comments were made by the examiner explaining why the examiner departed from the Board’s conclusion.

104. I have been asked to consider whether the examiner erred in a manner material to the patentability of claims challenged here. In my opinion, the examiner of the 595 Patent erred in permitting the 595 Patent to issue. In particular, the examiner failed to give any reason why he departed from the Board's conclusion that the 623 Patent claims were obvious in view of Hazelzet and Buchmann, as explained in the Final Written Decision of IPR2018-00303. This is remarkable, given that the claims of both 595 Patent and 623 Patent are strikingly similar. The only arguable distinction is that the 623 Patent requires "a notification signal indicating ... status of one or more training sequences" while the 595 Patent requires "information related to one or more training sequences." Ex. 1001 at claim 1; Ex. 1031 at claim 1. However, that distinction cannot justify the examiner's decision to allow the 595 Patent, because the Hazelzet-Buchmann combination which rendered obvious "*a notification signal indicating ... status of one or more training sequences*" in the 623 Patent also renders obvious providing "*information related to one or more training sequences.*"

105. Below, in § V, I repeat my analysis demonstrating that a Skilled Artisan would have found the combination of Hazelzet and Buchmann to be obvious, and motivated by the prior art knowledge of such a person, as evidenced by numerous exhibits not discussed by the examiner of the 595 Patent. I also point out

that the Board has already found such evidence to be credible during the IPR on the 623 Patent.

7. IPR2020-01042

106. SK hynix filed a petition for inter partes review of the 595 Patent on June 8, 2020, based on Hazelzet, JEDEC, and Buchmann, which are the same prior art references asserted in this petition. EX1058. SK hynix's petition relied on my analysis and testimony concerning the obvious combination of Hazelzet and JEDEC and the combination of Hazelzet and Buchmann, which are the same primary combinations asserted in this petition. Below, in § V, I repeat my analysis demonstrating that a Skilled Artisan would have found the Hazelzet-JEDEC and Hazelzet-Buchmann combinations to be obvious, and motivated by the prior art knowledge of such a person, as evidenced by multiple exhibits not discussed by the examiner of the 595 Patent. I also point out that the Board has already found such evidence to show obviousness during the IPR on the 595 Patent, because the Board instituted review on all challenged claims and grounds. EX1059, 45. I understand that IPR2020-01042 was terminated because the parties settled on May 6, 2021 before the Board issued a Final Written Decision. EX1060.

E. Challenged Claims of the 595 Patent

107. This declaration relates to claims 1-24 of the 595 Patent. Those claims read as follows:

Claim	Claim Language
1.a	1. A memory module operable with a memory controller of a host system, comprising:
1.b	a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;
1.c	dynamic random access memory elements on the printed circuit board;
1.d	a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection; and
1.e	[i] wherein the memory module is configurable to operate in any of at least a first mode and a second mode; [ii] wherein the memory module in the first mode is configurable to perform one or more normal memory read or write

Claim	Claim Language
	operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, [iii] wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations, and [iv] wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences;
1.f	[i] wherein the module controller is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations, [ii] wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and [iii] wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal

Claim	Claim Language
	indicating a parity error having occurred while the memory module is in the first mode;
1.g	wherein the module controller in the second mode is further configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection to a first state or to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.
2	2. The memory module of claim 1, wherein the module controller comprises an integrated circuit.
3	3. The memory module of claim 1, wherein the module controller includes a notification circuit comprising a transistor having an open drain coupled to the open drain output and source coupled to the ground.
4	4. The memory module of claim 3, wherein the module controller is configurable to drive a gate of the transistor high so as to drive open drain output and the error edge connection to ground, or to drive the gate of the transistor low so as to drive the open drain output and the error edge connection to the high impedance state.

Claim	Claim Language
5	5. The memory module of claim 4, wherein the module controller is configurable to output the signal indicating a parity error having occurred by driving the gate of the transistor high to provide a low impedance path between the open drain output and the ground.
6	6. The memory module of claim 3, wherein the notification circuit further includes a multiplexor or a logic circuit having a output coupled to a gate of the transistor and configurable to drive the gate of the transistor with either a first signal related to the parity error or a second signal related to the one or more training sequences.
7	7. The memory module of claim 3, wherein the module controller is configurable to provide the information related to the one or more training sequences by driving a gate of the transistor with the second signal so as to drive the open drain output from the high impedance state to ground or from ground to the high impedance state.
8	8. The memory module of claim 1, wherein the second edge connections include one or more pins that are not active while the memory module is in the second mode.
9	9. The memory module of claim 1, wherein the memory module in the second mode is configurable to perform the operations related to

Claim	Claim Language
	the one or more training sequences without communicating data signals via the first edge connections while the memory module is in the second mode.
10.a	10. A memory module operable with a memory controller of a host system, comprising:
10.b	a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;
10.c	dynamic random access memory elements on the printed circuit board;
10.d	a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection and configurable to drive the open drain output from a first state to a

Claim	Claim Language
	second state and from the second state to the first state, one of the first state and the second state being a low logic level, and the other one of the first state and the second state being a high impedance state; and
10.e	wherein the memory module is operable in at least a first mode in which the memory module is configurable to perform one or more memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, and a second mode in which the memory module is not accessed by the memory controller for memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences without communicating data signals via the first edge connections;
10.f	wherein the module controller in the first mode is configurable to receive via the second edge connections the address and control signals associated with the one or more memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and

Claim	Claim Language
	control signals, and wherein the module controller in the first mode is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred in the memory module while the memory module is in the first mode;
10.g	wherein the module controller in the second mode is further configurable to output to the memory controller open-drain signals related to the one or more training sequences via the open drain output and the error edge connection while the memory module is in the second mode.
11	11. The memory module of claim 10, wherein the module controller comprises an integrated circuit.
12.a	12. The memory module of claim 10, wherein the module controller includes a notification circuit having a transistor with an open drain coupled to the open drain output and a source coupled to the ground,
12.b	wherein the module controller is configurable to output to the memory controller the open-drain signals related to the one or more training sequences by driving a gate of the transistor high so as to drive the open drain output and the error edge connection to ground,

Claim	Claim Language
	and by driving the gate of the transistor low as to drive the open drain output and the error edge connection to the high impedance state,
12.c	and wherein the notification circuit is configurable to output the signal indicating a parity error having occurred by driving the gate of the transistor high to provide a low impedance path between the open drain output and ground.
13	13. The memory module of claim 12, wherein the notification circuit further includes a multiplexor or a logic circuit having an output coupled to the gate of the transistor and configurable to drive the transistor with either a first signal related to the parity error or a second signal related to the one or more training sequences.
14	14. The memory module of claim 10, wherein the module controller is configurable to output the open-drain signals related to the one or more training sequences by driving the open drain output from the high impedance state to the low logic level or from the low logic level to the high impedance state.
15	15. The memory module of claim 10, wherein the second edge connections include one or more pins that are not active while the memory module is in the second mode.

Claim	Claim Language
16	16. The memory module of claim 10, wherein the second edge connections include one or more high-order address pins that are not active while the memory module is in the second mode.
17.a	17. A method, comprising:
17.b	at a memory module coupled with a memory controller of a host system, the memory module including a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections, the memory module further including dynamic random access memory elements on the printed circuit board;
17.c	receiving via the second edge connections address and control signals associated with one or more memory read or write operations; controlling the dynamic random access memory elements to communicate data signals corresponding to the one or more memory

Claim	Claim Language
	read or write operations via the first edge connections in response to the address and control signals; outputting via an open drain output coupled to the error edge connection a signal indicating a parity error having occurred in the memory module while the memory module is being accessed by the memory controller for a memory read or write operation;
17.d	performing operations related to one or more training sequences while the memory module is not accessed by the memory controller for memory read or write operations; and outputting to the memory controller via the open drain output and the error edge connection open-drain signals related to the one or more training sequences and unrelated to any memory read or write operation.
18	18. The method of claim 17, wherein the second edge connections include one or more pins that are not active while the memory module is trained with the one or more training sequences.
19	19. The method of claim 18, wherein the second edge connections include one or more high-order address pins that are not active while the memory module is trained with the one or more training sequences.

Claim	Claim Language
20.a	20. The method of claim 17, wherein the memory module includes a notification circuit having a transistor with an open drain coupled to the open drain output and a source coupled to ground,
20.b	wherein outputting via an open drain output coupled to the error edge connection a signal indicating a parity error having occurred in the memory module comprises driving a gate of the transistor high to provide a low impedance path between the open drain output and ground, and
20.c	wherein outputting the open-drain signals related to the one or more training sequences and unrelated to any memory read or write operation comprises driving the gate of the transistor to drive the open drain output from a high impedance state to ground and from ground to the high impedance state.
21.a	21. A memory module operable with a memory controller of a host system, comprising:
21.b	a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an

Claim	Claim Language
	error edge connection in addition to the first edge connections and the second edge connections;
21.c	dynamic random access memory elements on the printed circuit board; and
21.d	a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller including a transistor having a gate and an open drain output coupled to the error edge connection; wherein the module controller is configurable to drive the gate of the transistor so as to drive the open drain output to a first state or a second state, the first state being a low logic level and the second state being a high impedance state;
21.e	[i] wherein the module controller is configurable to receive via the second edge connections memory commands associated with normal memory read or write operations and to output a set of address and control signals for each of the normal memory read or write operations; [ii] wherein the dynamic random access memory elements are configurable to communicate one or more N-bit-wide data signals with

Claim	Claim Language
	the memory controller via the first edge connections in response to the set of address and control signals, where N is at least 32; [iii] wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred during any of the memory read or write operations by driving the open drain output and the error edge connection to the first state;
21.f	wherein the memory module is configurable to perform operations related to one or more training sequences while the memory module is not accessed by the memory controller for memory read or write operations; and wherein the module controller is configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection from one of the first state and the second state to the other one of the first state and the second state.
22	22. The memory module of claim 21, wherein the module controller further includes a multiplexor or a logic circuit having an output coupled to the gate of the transistor, and wherein the module controller is configurable to drive the gate of the transistor with either

Claim	Claim Language
	a first signal related to the parity error or a second signal related to the one or more training sequences.
23.a	23. The memory module of claim 22, wherein the transistor has a source coupled to ground,
23.b	wherein the module controller is configurable to output the signal indicating a parity error having occurred by driving the gate of the transistor high to provide a low impedance path between the open drain output and ground, and
23.c	wherein the module controller is configurable to provide the information related to the one or more training sequences by driving the open drain output from a high impedance state to ground or from ground to the high impedance state.
24	24. The memory module of claim 21, wherein the memory module is configurable to perform the operations related to the one or more training sequences while the memory module is not communicating signals via the first edge connections.

F. Construction of Terms Used in the 595 Patent Claims

108. I understand that claim terms should be given their ordinary and accustomed meaning as understood by one of ordinary skill in the art in view of the

patent and its file history. As detailed in my analysis and set forth below, I have used what I believe to be the ordinary and accustomed meaning of the claim terms as understood by one of ordinary skill in the art in view of the 595 Patent and its file history.

109. I understand that in the Institution Decision for IPR2020-01042, the Board declined to construe SK hynix's asserted terms, which included "*memory read or write operations*," "*normal memory read or write operations*," "*mode*," and "*training sequence*." EX1059, 30. I also understand that in the related district court case, Case No. 6:20-CV-00194, the Western District of Texas the Court construed certain terms in the 595 Patent, namely, "*mode*" / "*first mode*" / "*second mode*," "*one or more training sequences*," "*notification signal associated with the [one or more training sequences]*," "*information related to the [one or more training sequences]*," "*open-drain signals related to the [one or more training sequences]*." EX1061, 2-3. Below I address each of these terms.

1. "memory read or write operations"

110. It is my opinion that a Skilled Artisan would understand the ordinary meaning of "*memory read or write operations*" to be operations used to communicate data between the memory module and the memory controller in the read or write direction in response to commands from the memory controller.

111. In the claims, “*memory read or write operations*” refers to operations used to read or write DRAMs in response to address and control signals received from the system memory controller. EX1001, 16:26-33. For example, claim 10 requires:

the module controller in the first mode is configurable to receive via the second edge connections the **address and control signals** associated with the **one or more memory read or write operations**, wherein the dynamic random access memory elements are configurable to communicate data signals with **the memory controller** via the first edge connections in accordance with the address and control signals, and wherein the module controller in the first mode is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred in the memory module while the memory module is in the first mode

EX1001, 26-38. (emphasis added).

112. Similarly, the 595 Patent specification explains that “[d]uring the read/write operations, the memory module **communicates data** with the memory controller via the data signal pins **in response to second memory commands received via the address and control signal pins.**” EX1001, 1:57-61. (emphasis added).

113. Thus, during read/write operations, the module controller will transmit the command and address signals received from the system memory controller to

the memory devices. EX1001, 5:45-52 (“For example, the controller circuit 18 may receive and process address and command signals (*e.g.*, read, write commands) from the system memory controller 14 and transmit appropriate address and commands to the memory elements in response”). (emphasis added). The intrinsic record therefore confirms that “*memory read or write operations*” refers to operations used to communicate data between the memory module and the memory controller in response to commands from the memory controller.

114. I also understand that in the IPR2020-01042 Institution Decision, the Board declined to construe the term “*memory read or write operations.*” EX1059, 30. To the extent that the Board does not agree with Petitioner’s construction of “*memory read or write operations,*” the Board should take the same approach here in declining to construe the term “*memory read or write operations.*” Regardless, as explained in § V.A, the prior art invalidates the 595 Patent under either construction.

2. **“normal memory read or write operations”**

115. It is my opinion that a Skilled Artisan would understand the ordinary meaning of “*normal memory read or write operations*” to be the same as “*memory read or write operations.*”

116. The original application from which the 595 Patent issued does not use the phrase “*normal.*” Nevertheless, the original claims consistently used the

phrase “*memory read or write operations.*” On July 2019, the Abstract and some of the pending claims were amended to include “*normal* *memory read or write operations.*” EX1002, 224, 240.

wherein the memory module in the first mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and ~~control~~ command-signals received via the second edge connections, wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations, and wherein the memory module in the second mode is configurable to undergo training with ~~configurable to perform operations related to one or more training sequences while the first edge connections are not active;~~

wherein the module controller is configurable to receive via the second edge connections the address and ~~command-control~~ signals associated with the one or more normal memory read or write operations ~~and to control, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge~~

EX1002, 224 (annotated).

117. When making these amendments, the patent applicant explained that “[n]o new matter has been added.” *id.*, 233.

Support for the amendments can be found throughout the specification and drawings of the application as filed (e.g., paragraphs [0016], [0018], [0019], [0035]-[0037], and [0040]). No new matter has been added.

EX1002, 233 (annotated). (emphasis added).

118. Alternatively, “*normal* *memory read or write operations*” should be construed to mean standard operations used by the memory controller to read from or write to memory devices, whether or not they occur in a normal operating mode of a module. For example, the patent states:

For example, the system memory controller 14 may cause the memory module 10 to perform **standard operations such as memory**

read/write, pre-charge, refresh, etc., while in operational mode, although it will be appreciated that one or more of **these operations** **can** also be performed by the memory module 10 while **in initialization mode** in certain embodiments.

EX1001, 6:50-56. (emphasis added).

119. This passage is part of the patent's description of a "normal" "operational mode." EX1001, 6:45-50. It explains that "the **normal** mode of the memory module 10 ... [during which] ... the memory module 10 is generally accessed by the system memory controller 14 of the host computer 16 during standard computer operation not associated with initialization." EX1001, 6:45-50. (emphasis added).

120. Thus, the specification includes an example of memory read and write operations used by the system memory controller to read from or write to memory devices during standard computer operation. However, this part of the specification also explains that "it will be appreciated that **one or more of these operations** can also be **performed** by the memory module 10 while **in initialization mode**." EX1001, 6:53-56. (emphasis added). The 595 Patent therefore states that the disclosed standard memory operations can also be used in non-normal modes, for example, during initialization.

121. As another example, claim limitation [1.e.ii] requires that "normal memory read or write operations" occur in the "first mode," while claim limitation

[1.e.iii] requires that “normal memory read or write operations” not occur in the “second mode” during which “training sequences” occur. If “normal memory read or write operations” were construed to be limited to memory read or write operations only in the “first” (normal) mode, then limitation [1.e.iii] would be meaningless because by construction “normal memory read or write operations” could never occur in the “second” training mode or any other non-normal mode.

122. Likewise, the prosecution history confirms that “normal memory read or write operations” can be used during initialization. The 595 patent claims to be a continuation of U.S. Patent No. 8,489,837 (the “837 Patent”), which was the subject of IPR2017-00548. I understand that the proceedings of that IPR are part of the prosecution history of the 595 Patent and of the intrinsic record for purposes of claim construction. Likewise, the record in IPR2017-00548 was provided to the examiner of the 595 Patent, so it is part of the intrinsic record for that reason as well.

123. In IPR2017-00548, Patent Owner’s expert was questioned about the passage block quoted above (EX1001, 6:50-56), which appears in identical form in the 837 Patent. The expert agreed that a Skilled Artisan would have understood the quote to be accurate, EX1021, 24:8-23, and conceded that the referenced memory commands (*i.e.*, the ones that can be used during initialization) would be considered “normal memory commands that a memory controller or processor

would issue to read and write data out into main memory under standard or regular use of a computer[.]” EX1021, 24:24-25:18. The expert also testified that, aside from initialization, “normal read and writes” can be used in other non-normal modes, such as boot-down sequences. EX1021, 17:24-18:11. I agree with these conclusions of Patent Owner’s expert.

124. I also understand that in the IPR2020-01042 Institution Decision, the Board declined to construe the term “*normal memory read or write operations.*” EX1059, 30. To the extent that the Board does not agree with Petitioner’s construction of “*normal memory read or write operations,*” the Board should take the same approach here in declining to construe the term “*normal memory read or write operations.*” Regardless, as explained in § V.A, the prior art invalidates the 595 Patent under either construction.

125. Thus, the specification and prosecution history of the 595 Patent confirm that “*normal memory read or write operations*” are not limited to operations actually used during standard computer operation or in any particular mode. But that, this phrase should be construed to have the same meaning as “*memory read or write operations*” or, in the alternative, to mean standard operations used to read from or write to memory devices and initiated by the system memory controller, and should explicitly be construed as not limited to occurring only in any normal operating mode of a module.

3. “mode”

126. It is my understanding that a Skilled Artisan would give “*mode*” its plain and ordinary meaning after reviewing the 595 Patent and its prosecution history.

127. The 595 Patent uses the term “*mode*” in accordance with the plain and ordinary meaning. EX1001, Abstract, 1:43-3:15, 4:29-42, 5:66-6:14, 6:45-6:56. I understand that in the course of IPR2017-00548 and the district court case relating to the 595 Patent, Patent Owner sought to have the term “*mode*” interpreted to mean “a distinct behavioral state that a system may be switched to.” EX1035, 7; EX1061, 2. However, such a construction lacks intrinsic support. For example, the specification has no support for Patent Owner’s proposal of limiting “*mode*” to “distinct behavioral state” and requiring “switch[ing]” into such a state, as the Board has already found. EX1035, 7.

128. In addition, based on the word “distinct” Patent Owner argued that that different “modes” must necessarily include mutually exclusive operations. EX1041, 6. However, as the Board also found, EX1035, 7, this is inconsistent with the disclosure of the 595 Patent expressly stating that the disclosed memory operations may be used in both an operational mode and in an initialization mode. EX1001, 6:50-56 (emphasis added):

For example, the system memory controller 14 may cause the memory module 10 to perform standard operations such as memory read/write,

pre-charge, refresh, etc., while **in operational mode**, although it will be appreciated that one or more of these operations can also be performed by the memory module 10 while **in initialization mode** in certain embodiments.

129. I also understand that in IPR2017-00548, the Board rejected Patent Owner's proposed construction but did not expressly construe the term "mode." EX1035, 7. In IPR2020-01042, the Board also declined to construe the word "mode." EX1059, 30. As the intrinsic record here never defines the term "mode" or uses it in any special sense, the Board should take the same approach here. I also understand that the district court in Case No. 6:20-CV-00194 agreed with Petitioner's construction in construing "mode" have its plain and ordinary meaning. EX1061, 2

130. Finally, should a construction be necessary, as I explained in the 623 patent IPR, I agree that the term "mode" is essentially synonymous with the word "state" in the context of the 623 Patent, without all of the implicit limitations Patent Owner sought to have read into the claims in the 837 Patent IPR. For instance, a "second mode" in which the module "perform[s] operations related to one or more training sequences" is a "state" of the module in which operations related to one or more training sequences are performed. That word "state" is consistent with the disclosures of the 595 Patent and the dictionary Patent Owner has provided in the IPR for the parent 837 Patent. While Patent Owner's dictionary

uses the phrase “operational state,” Ex. 1047, 3, it is using “operational” more broadly than the 595 Patent, since the patent explicitly equates the disclosed “operational mode” with normal memory operations and the dictionary includes no such limitation. EX1001, 6:45-50; Ex. 1047, 3. Construing “mode” to mean “state” therefore captures the ordinary meaning of “mode” in the context of the ’595 patent and avoids any confusion from the inconsistent use of the word “operational.” To be clear, I do not believe interpreting “mode” to mean “state” alters the analysis set forth in my declaration, since in my view the two words mean the same thing to a person of skill in the context of the 595 patent.

4. “training sequence”

131. It is my opinion that a Skilled Artisan would understand the ordinary meaning of “*training sequence*” to be a set of operations occurring in a particular order and used for training.

132. Generally, a “sequence” is “a set of related events, movements, or things that follow each other in a particular order.” EX1042, 1.

133. Further, the 595 Patent provides very few details concerning the disclosed “*training sequences*.” What is shown is only that (1) the “*training sequences*” may be controlled by the memory module, EX1001, 3:32-35 (“the MCH according to such a scheme may give control to the local memory controller of a memory subsystem (*e.g.*, memory module) for execution of a training

sequence.”), (2) that a module may carry out more than one training sequences, and (3) that they may be part of an “initialization sequence.” *Id.*, 6:19-23 (“the memory controller 14 issues a first command to the memory module 10, and, in response, the memory module 10 executes an initialization sequence (*e.g.*, one or more training sequences)”).

134. During IPR2018-00303, relating to the 623 Patent (which as noted above shares a specification with the 595 Patent and includes similar claims), the Board found that Buchmann’s TS3 training operations satisfied the “*training sequence*” as claimed in the 623 Patent. EX1034, 11-12. The TS3 operations are a set of operations carried out in a particular order to perform upstream lane training and repair. EX1016, 5:40-44. Indeed, Buchmann explicitly describes his different sets of training operations as “training sequences.” EX1016, 3:49-52, 14:38-41.

135. I also understand that, in the IPR2020-01042 Institution Decision, the Board declined to construe the term “*training sequences*.” EX1059, 30. To the extent the Board does not agree with Petitioner’s construction of “*training sequences*,” the Board can take the same approach here in declining to construe the term “*training sequences*” because a Skilled Artisan would have understood that the prior art relied on discloses “*training sequences*” under any reasonable interpretation. I also understand that the district court in Case No. 6:20-CV-00194 construed “*training sequences*” to mean “operations in a particular order for

preparing a memory system to perform its intended function.” EX1061, 2. Since a Skilled Artisan would have understood that the claimed “training” is “preparing a memory system to perform its intended function” as the Court construed this term, and the prior art discloses “training,” as explained in § V.A, it follows that the prior art teaches the claimed “training sequences” under either construction.

136. Thus, “*training sequence*” should be construed to mean a set of operations occurring in a particular order and used for training.

5. “notification signal associated with the [one or more training sequences]” / “information related to the [one of more training sequences]” / “open-drain signals related to the [one or more training sequences]”

137. A Skilled Artisan would have understood that, in the context of the 595 patent, these phrases refer to unscheduled signal/information/open-drain signals provided without polling that indicate the status of the one or more training sequences. This interpretation is supported throughout the specification. For example, the Summary of the 595 patent explains that the “memory module ... sends a first output signal via the output pin to indicate a status of the at least one initialization sequence to the memory controller.” EX1001, 1:50-54. The specification expressly disparages polling as being “generally inefficient because the system memory controller does not know exactly when the memory subsystem will have completed the required or requested operation,” thus causing the controller to “wait longer than necessary to poll the memory subsystem, thereby

delaying the overall initialization process.” EX1001 (595 Patent), 3:42-62. The specification also explains the advantages of the “notifying method, [in which] the memory subsystem controller sends a signal to the MCH when the memory subsystem controller completes the required or requested operation. This method allows the MCH to execute one or more independent commands while it is waiting for a notification signal from the memory sub system controller.” 3:63-4:4; *see also* 4:36-42, 6:57-63, 8:34-38, 11:29-34, etc. (disclosing unscheduled signals provided without polling to indicate status of training sequences).

138. I understand that the district court in Case No. 6:20-CV-00194 has interpreted the phrases “*notification signal associated with the [one or more training sequences]*” / “*information related to the [one of more training sequences]*” / “*open-drain signals related to the [one or more training sequences]*” to have the construction above for “training sequences,” with the rest of the phrase having its plain and ordinary meaning, which does not encompass polling. EX1061, 2-3. For the reasons discussed above, this construction is consistent with the intrinsic evidence. To the extent there are any differences in scope between the district court’s construction and my proposed construction above, they do not matter for this petition because the prior art discloses either interpretation for the reasons discussed below.

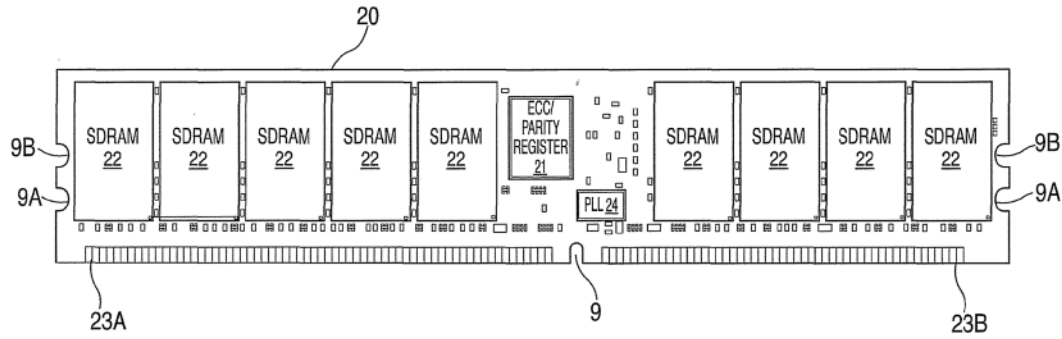
IV. OVERVIEW OF THE PRIOR ART

A. Prior Art

1. U.S. Patent Publication No. 2008/0098277 to Hazelzet (Ex. 1014)

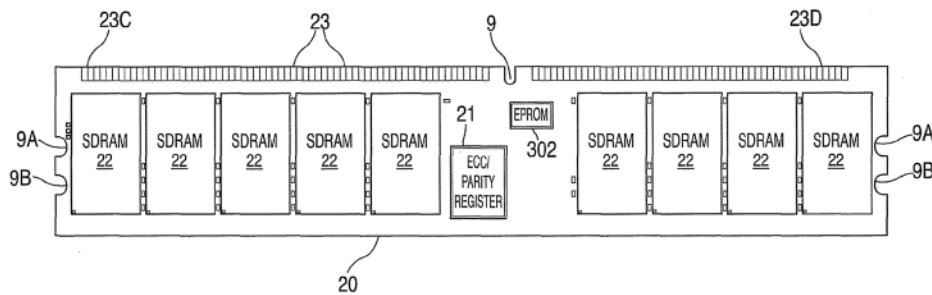
139. U.S. Patent Publication No. 2008/0098277 to Hazelzet (“Hazelzet”) (Ex. 1014) was filed on October 23, 2006 and published on April 24, 2008. I understand that Hazelzet is prior art to the 595 Patent. Hazelzet is entitled “High Density High Reliability Memory Module With Power Gating and a Fault Tolerant Address and Command Bus” and discloses such functionality. Ex. 1014 (Hazelzet) at Title.

140. Hazelzet discloses memory modules that can include up to four ranks of memory devices arranged in a registered DIMM format that is consistent with JEDEC standards. EX1014, [0039-40], [0044], FIGS. 3A-3D (FIG. 3C-3D reproduced below, showing stacked arrangement of memory devices), [0008], [0014], [0016]. Hazelzet discloses that its modules can be initialized in a number of different ways, including those described in related JEDEC standards. EX1014, [0123]-[0125].



FRONT SIDE OF DIMM - 4 HIGH STACK

FIG. 3C



BACK SIDE OF DIMM - 4 HIGH STACK

FIG. 3D

141. Hazelzet's module can operate in an "ECC mode" or a "parity mode."

Ex. 1014 (Hazelzet) at ¶¶[0064],[0069]-[0070]; *see also id.* at FIG. 8, ¶¶[0020], [0022], [0049], [0059]-[0062], [0072], [0075], [0081], [0101]-[0103], [0106]-[0107], [0109].

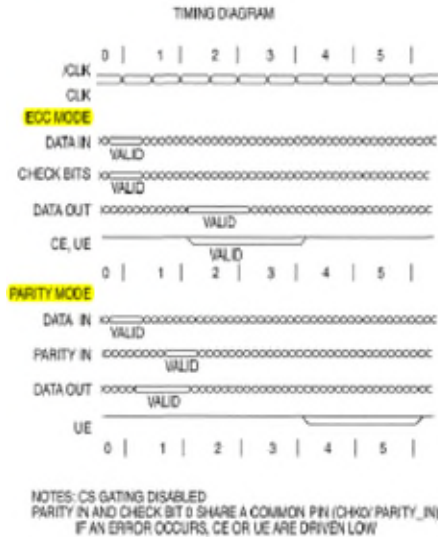


FIG. 8

142. Hazelzet explains that the “ECC mode” is a mode that allows the host system to detect and/or correct “correctable errors” or “uncorrectable errors” (*e.g.*, “double bit error”). Ex. 1014 (Hazelzet) at ¶[0069] (“This ECC logic will ... correct all single bit errors and detect all double bit errors present on the twenty-two chip select gated data inputs.”) In the “ECC mode,” the detected correctable errors would be output through an “/Error (CE)” output pin and any uncorrectable errors (*e.g.*, double bit errors) would be reported through an “/Error (UE)” output pin. Ex. 1014 (Hazelzet) at ¶[0069]. Hazelzet explains that these two outputs (*i.e.*, CE and UE) are “open-drain outputs.” Ex. 1014 (Hazelzet) at ¶¶[0072], [0109].

143. Hazelzet further explains that the “parity operating mode” is a mode that allows the host system to “interrogate the device to determine the error condition” of the memory module. Ex. 1014 (Hazelzet) at ¶[0064] (“A parity operating mode is also provided, in conjunction with error reporting circuitry to

permit the system to interrogate the device to determine the error condition.”).

Hazelzet further explains that such “error condition” in the “parity mode” is also reported to the host “via the Uncorrectable Error (UE) line” when the memory module is in the “parity mode,” Ex. 1014 (Hazelzet) at ¶[0070], which is the open-drain output that is used to report the uncorrectable errors in the “ECC mode.” Ex. 1014 (Hazelzet) at ¶¶[0072], [0109].

144. Hazelzet further explains that its memory module is in the “ECC mode” when the “/ECC Mode” signal becomes “low,” Ex. 1014 (Hazelzet) at ¶[0069], and that the memory module switches to the “parity mode” when the “/ECC Mode” signal becomes “high.” Ex. 1014 (Hazelzet) at ¶[0070].

2. JEDEC LRDIMM Proposal (EX1015)

145. The JEDEC reference is a proposal disclosing modifications to the Memory Buffer (“*module controller*”) functionality of a DDR3 LRDIMM memory module (Load Reduced DIMM), the standards for which were under development at the time of the alleged invention by the standard developing organization called JEDEC. In particular, JEDEC proposed to add training of Memory Buffer in an initialization mode that included training sequences and corresponding handshaking methods, including the ability to output notification signals providing the status of those sequences. I understand that JEDEC is prior art to the 595 Patent. Indeed, I understand that in IPR2020-01042, the Board noted that SK hynix

successfully showed that JEDEC qualifies as prior art to the 595 Patent, EX1059, 27. In addition, in related IPR2020-01044, that Board noted that Patent Owner's Preliminary Response did not dispute SK hynix's assertion that JEDEC was publicly accessible by November 11, 2009. EX1062, 34. The training in the initialization mode included, among others, MB-DRAM Training that entailed training sequences such as Write Leveling Training and Read Enable Training between the Memory Buffer and the DRAMs of the module. EX1015, 8. JEDEC also states that "[n]o DRAM commands or control word writes (either over the Command/Address and Control buses or via SMBus) can be issued to the MB until the MB-DRAM Interface training is complete...." *Id.*

146. In the same description of MB-DRAM Training, JEDEC states that "training completion can be signaled by the assertion of ERROUT#." *Id.*, 8. A Skilled Artisan would understand that "ERROUT#" refers to the parity error out pin on a JEDEC standard LRDIMM module of the time. Specifically, a Skilled Artisan would have understood there were other JEDEC documents defining other aspects of DDR3 LRDIMM at that time, such as EX1036, 1, which is a ballot for the "DDR3 SDRAM LRDIMM Design Specification." Much like Hazelzet's registered memory modules (RDIMMs), the DDR3 LRDIMM memory modules at the time of the alleged invention were disclosed to include a PCB with various edge connections for data signals, address and command signals and an ErrOut_n

pin that, during normal operation, was used to notify the memory controller of parity errors through the use of an open-drain output. EX1036, 5-10, *see, e.g.*, at 8 (penultimate entry in table on page re ErrOut_n). A Skilled Artisan would have understood that the LRDIMM Design Specification's ErrOut_n and JEDEC's ERROUT# referred to the same output/pin on the DDR3 LRDIMMs of the time. *See also* EX1044, 1 (October 2008 TI DDR3 buffer datasheet that discloses ERROROUT# open drain parity error signal).

147. JEDEC therefore discloses training during an initialization mode in which the memory module that buffers address, command and data lines, such as a DDR3 LRDIMM. During initialization, the module can be made to perform operations related to various training sequences, including MB-DRAM Training, which does not include any memory read or write operations in response to memory controller commands, and which outputs a notification signal indicating status (*e.g.*, completion) of the training sequences over the same open drain output used to report parity errors in a normal mode of operation.

3. U.S. Patent No. 8,139,430 to Buchmann (Ex. 1016)

148. U.S. Patent No. 8,139,430 to Buchmann et al. ("Buchmann"), the application for which was filed on July 1, 2008, issued on March 20, 2012. I understand that Buchmann is prior art to the 595 Patent. Buchmann is entitled "Power-On Initialization and Test for a Cascade Interconnect Memory System"

and discloses, among other things, such functionality. Ex. 1016 (Buchmann) at Title.

149. Buchmann discloses power-on initialization of exemplary memory modules (110) where each memory module has a memory buffer (MB, 106) for buffering data, command, and address to and from the memory devices (108).

EX1016, FIGS. 1-2, 4:5-50.

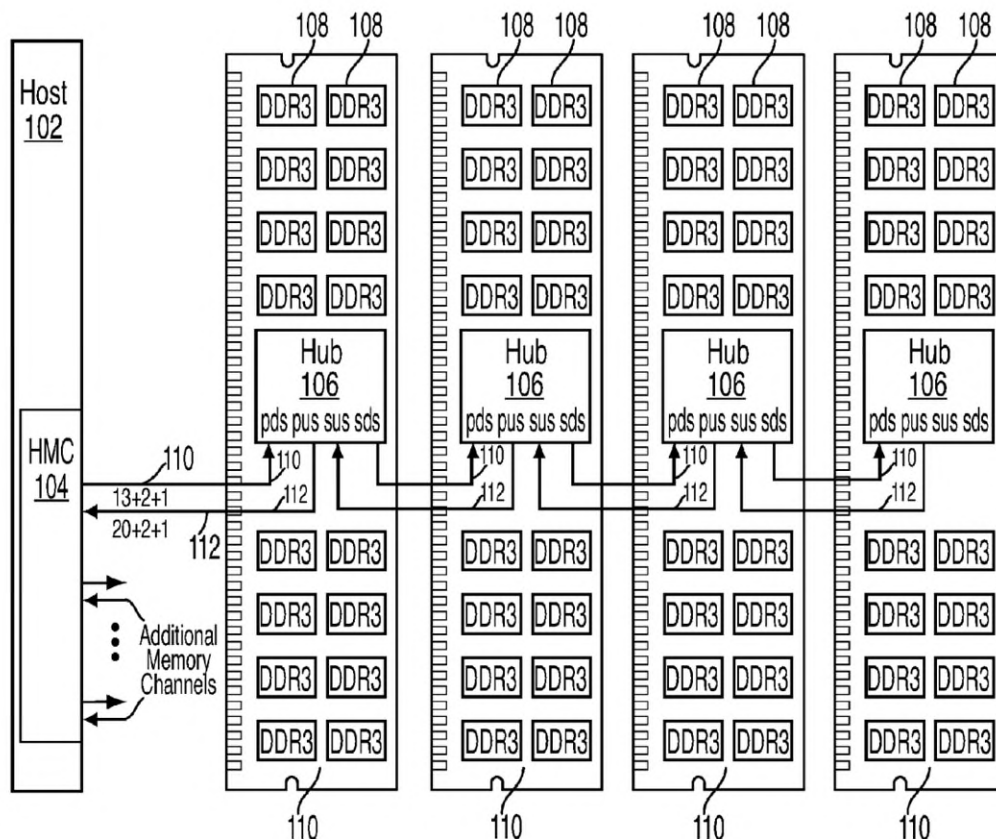


FIG. 1

150. Buchmann discloses two modes of operation (*i.e.*, “SBC mode” and “high-speed mode”), Ex. 1016 (Buchmann) at Abstract, 1:39-44. The “high-speed

mode” is a mode of operation “at a high nominal speed.” Ex. 1016 (Buchmann) at 14:67-15:2. On the other hand, the “SBC mode” is a mode of operation “at a reduced rate” of communication. Ex. 1016 (Buchmann) at 14:65-67. According to Buchmann, before the high-speed bus between the memory controller and the memory module (*e.g.*, downstream bus 110 and upstream bus 112 in FIG. 1) can be used reliably to communicate with the memory modules, the memory module operates in the SBC mode to train the high-speed bus. Ex. 1016 (Buchmann) at 14:5-8, 3:52-54, 3:64-67; *see also id.* at FIG. 1, 4:11-14.

151. In particular, Buchmann discloses executing training and/or initialization sequences in its “SBC mode,” which is also referred to as an “error correcting code protected quasi-static bit communication” mode. Ex. 1016 (Buchmann) at 14:1-15:15; *see also id.* at 3:52-54, 5:6-22, 4:51-12:59. For example, the training and/or initialization sequences taught by Buchmann include “TS0-clock detection, test and repair; TS1-static configuration and calibration; TS2-downstream lane training and repair; TS3-upstream lane training and repair; TS4 packet training; TS5-initiate valid packets; TS6-frame lock; and TS7-read data latency calculation and inter-channel de-skew,” Ex. 1016 (Buchmann) at 5:40-46, FIG. 3.

152. As an example, training sequence TS0 involves “clock detection and repair,” Ex. 1016 (Buchmann) at 5:51-53, which is a training of the clock signal in

the SBC mode. Ex. 1016 (Buchmann) at 5:66-6:22. In particular, the memory buffer MB (*i.e.*, “module controller,” as claimed) enters the TS0 state and initiates the training sequence TS0 of Buchmann (*i.e.*, an example of a “training sequence” in the “second mode”) after receiving the SBC command “TS0_pdsck” from the host. Ex. 1016 (Buchmann) at 6:1-50 (Table 1 and Table 2, explaining that the “TS0_pdsck” command “causes the downstream receiver logic to enter the TS0 state, reset its memory channel PLLs and select the PDSCK clock as the MB reference clock” and that the “Host/MB drives downstream bus clock on SDSCK lane and issues TS0_pdsck SBC.”). Further, during the TS0 training sequence, the memory module generates and outputs various notification signals providing information about the training sequence to the memory controller of the host system, including the status of the TS0 training sequence (*e.g.*, “TS_done,” which notifies the host that the TS0 training is “done.”). Ex. 1016 (Buchmann) at FIG. 4, 5:51-7:2 & Tables 1-2.

153. As another example, training sequence TS3 involves “upstream lane training” and is “used to perform upstream data lane training,” Ex. 1016 (Buchmann) at 8:24-26, in the SBC mode, Ex. 1016 (Buchmann) at 8:27-47 (showing the SBC commands used during TS3 in Table 5). In particular, the memory buffer MB (*i.e.*, “module controller,” as claimed) initiates the “upstream lane training” TS3 of Buchmann (*i.e.*, another example of a “training sequence” in

the “second mode”) after correction/forwarding of the SBC command “TS3_annnc” (i.e., “TS3a announcement SBC”) from the host. Ex. 1016 (Buchmann) at 8:24-27 (“TS3 ... immediately follows TS2 with the host responsible for sending the TS3a announcement SBC.”), Table 5 (“TS3_annnc: This command announces the beginning of TS3a. This SBC is corrected and forwarded by MBs in the memory channel.”). Further, during the “upstream lane training” sequence TS3, the memory module generates and outputs various notification signals providing information about the training schemes to the memory controller of the host system, including the status of the TS3 training sequence, such as “TS3_ack,” which indicates that all downstream MBs have returned the TS3a_ack SBC, and “TS_done,” which notifies the host that the TS3 training sequence is “done.” EX1016, FIG. 6, 8:24-9:18 & Tables 5-6.

154. Buchmann discloses that his training operations may be initiated by power on, reset or initial program load operations, and “may be entered at different states,” which a person of ordinary skill would understand to mean that the his system was configurable to carry out some or all of the disclosed training. EX1016, 3:67-4:4, 4:51-5:12, FIG. 3. Moreover, Buchmann does not disclose the use of memory read and write operations during his TS0 and TS3 sequences during initialization/power-on. Buchmann therefore discloses a training mode (“*second mode*”) in which the memory module can be made to perform operations related to

various training sequences and which does not include any memory read and write operations in response to memory controller commands.

155. Buchmann's implementation involves a daisy chain arrangement among the various modules of his system, resulting in signals from the memory module to the host indicating completion of a training sequence reaching the host only after all modules had completed the sequence. *See, e.g.*, Ex. 1016(Buchmann) at 3:49-52;14:41-43;16:47-50;28:23-26. However, Buchmann also explains that "one or more other bus structure(s) or a combination of bus structures" may be used, including "point-to-point bus(es)," "multi-drop bus(es)," and/or "other shared or parallel bus(es)." *Id.* at 28:26-31.

4. U.S. Patent No. 8,359,521 to Kim (Ex. 1017)

156. United States Patent No. 8,359,521 to Kim et al. ("Kim") was filed on January 22, 2008, the underlying application was published July 23, 2009, and the patent issued January 22, 2013. I understand that Kim is prior art to the 595 Patent. Kim is entitled "Providing a Memory Device Having a Shared Error Feedback Pin" and discloses such functionality. Ex. 1017 (Kim) at Title.

157. Kim discloses a "system and method for providing a memory device having a shared error feedback pin." Ex. 1017 (Kim) at Abstract. Kim discloses that sharing functionality with an error pin is desirable in order maximize use of available bandwidth, simplify the memory controller, Ex. 1017 (Kim) at 4:40-49,

“mak[e] use of unused circuits within the subsystem,” Ex. 1017 (Kim) at 11:31-34, and enable compatibility with standard memory modules, Ex. 1017 (Kim) at 5:49-57. Kim teaches that this shared error feedback pin can be used to provide information such as status and error conditions and information related to initialization. Ex. 1017 (Kim) at 12:18-26. Kim further teaches how this shared error pin can be implemented using an open drain configuration and/or an OR-gate. Ex. 1017 (Kim) at 5:49-57; *see also id.* at 4:40-48; 6:1-16; FIG. 4, FIG. 5.

B. Background Technology

1. Shared Pins

158. By the effective filing date of the 595 Patent, a Skilled Artisan would have known that it was common to design the pins within a memory module such that a single pin is shared for various types of signals for different purposes due to the limited number of pins within the memory module. *See, e.g.*, Ex. 1026 (JESD82-20A) at page 18 (“The data mask signals share pins with the DQS[16:9] pins. ... The following table shows the mapping between DQS pins and data mask pins.”); Ex. 1017 (Kim) at FIG. 5 (showing that the pins related to the open drain transistor (on the right) is shared between the “parity check” circuitry and the “CRC check” circuitry (on the left)).

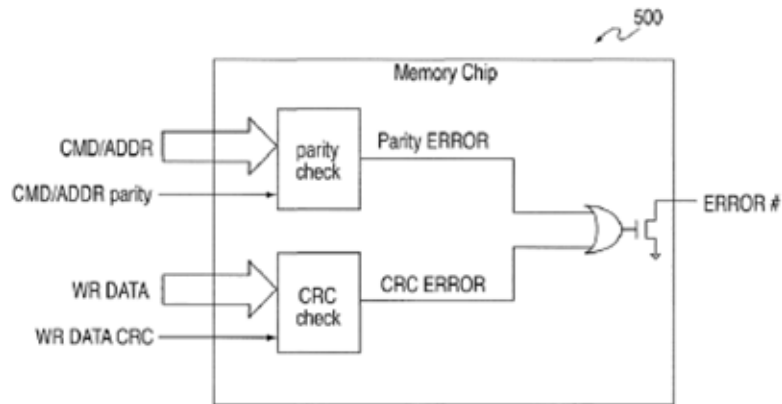


FIG. 5

159. As an example, Kim explains that its “pin [for] reporting CRC errors ... could also be merged with an existing error pin available on many industry standard modules for the reporting of address/command errors.” Ex. 1017 (Kim) at 5:49-55; *see also id.* at 6:13-18 (“In alternate exemplary embodiments, other functions also share the error feedback pin (*e.g.*, parity or CRC error(s) on command and address information).”).

160. A Skilled Artisan also knew that it was customary to use a logic OR circuit, as shown in FIG. 5 of Kim, to implement the shared pin. *See, e.g.*, Ex. 1017 (Kim) at FIG. 5 (showing a logic OR circuit coupled to the gate of the open drain transistor). *See* Ex. 1017 (Kim) at FIG. 5 (annotated to show the logic OR circuit in red), 6:13-16 (“FIG. 5 is a block diagram of a memory device 500 that shares an error feedback pin between data CRC and address parity in accordance with an exemplary embodiment of the present invention.”); *see also* Ex. 1023, US 20080155378 (Amidi) at FIG. 2, FIG. 4, ¶[0018] (“An output device 120

functioning as a logic OR ties the output ends of the error detection module 158 and the transmission memory 156 together such that the error detection module 158 and the transmission memory 156 share the output terminal error-out 168 to transmit signals to the memory controller 110. The output device 120 can be implemented as an OR gate, a wired-OR gate, an open collector, or other device functioning as a logic OR.”); *see also id.* at FIG. 2 (showing that the “error out” signal is output from a “logic OR” element), FIG. 4, claim 17 (“The buffer device of claim 16 wherein the output terminals from the error detection module and the transmission memory are tied using a device functional as a logic OR before being applied to the output terminal for sending the error signal.”).

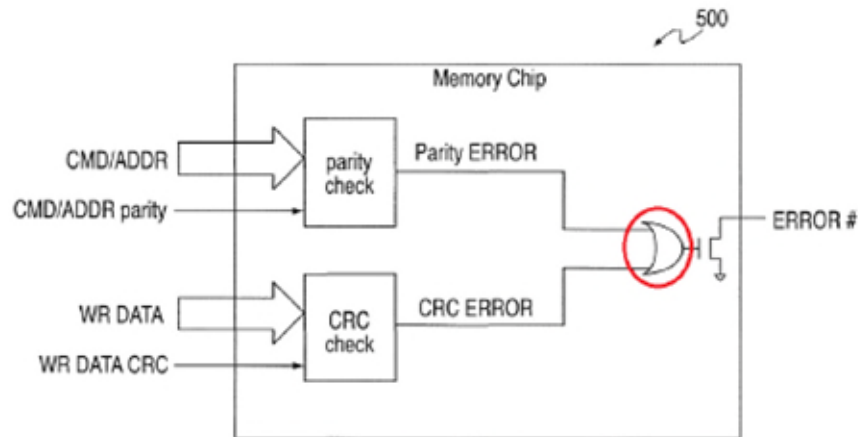


FIG. 5

[FIG. 5 of Kim]

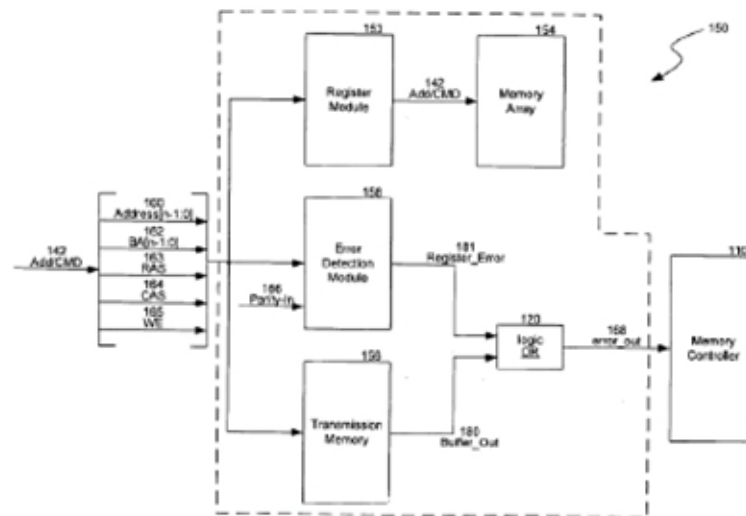


FIG. 2

[FIG. 2 of Amidi]

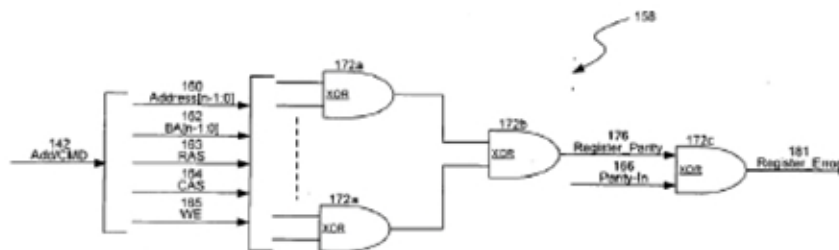


FIG. 4

[FIG. 4 of Amidi]

2. Open-Drain Output

161. By the effective filing date of the 595 Patent, a Skilled Artisan understood that it was common to use an “open drain output” in a memory module to send error signals to the host memory controller. *See, e.g.*, US 8,359,521 to Ex. 1017 (Kim) at FIG. 4 (reproduced below), 4:40-48; 6:1-16; Ex. 1014 (Hazelzet) at ¶¶[0072], [0109].

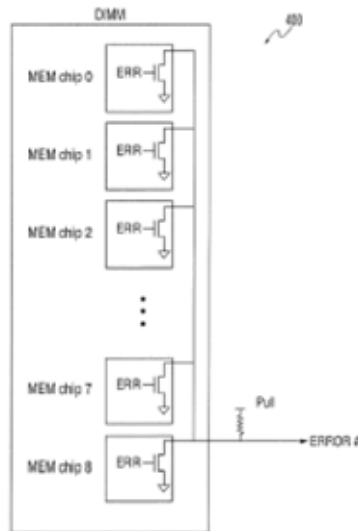


FIG. 4

162. An “open drain output” is an output pin coupled to the drain of a field effect transistor, which includes three ports (*i.e.*, a gate, a source, and a drain). *See, e.g.*, Ex. 1017 (Kim) at FIG. 4. As an example, FIG. 4 of Kim shows an open drain output that is coupled to a pull-up resistor (*i.e.*, connected to a high voltage via a pull-up resistor). FIG. 4 of Kim also shows that the source of the transistor is coupled to ground. Because the source of the transistor is coupled to ground (as opposed to Vdd), a positive voltage at the gate (*i.e.*, ERR in FIG. 4 of Kim) would turn on the transistor. Based on this bias condition, a Skilled Artisan would have understood that Kim’s transistor is an NMOS (*i.e.*, n-channel Metal Oxide Semiconductor) transistor, as opposed to a PMOS (*i.e.*, p-channel Metal Oxide Semiconductor). *See, e.g.*, Ex. 1017 (Kim) at FIG. 4. This is also clear from the symbol. A PMOS transistor would use a symbol with a bubble at the gate. *Id.*

163. A Skilled Artisan would have understood that such open drain outputs (*e.g.*, ERROR# in FIG. 4 of Kim) would be pulled to a high logic level (*i.e.*, the supply voltage connected to the resistor) through the resistor when the gate of the transistor is low, because the transistor would be off. *See, e.g.*, Ex. 1017 (Kim) at FIG. 4. The output would therefore be in an un-driven, high impedance, state. Ex. 1014 (Hazelzet) at ¶[0099]. On the other hand, the open drain output would switch to a low logic level (*e.g.*, ground) when the gate of the transistor is high, because the transistor would be on. *Id.*

C. The Combinations Relied on Here

164. The combinations analyzed here – Hazelzet/JEDEC and Hazelzet/Buchmann – are straightforward. In each, Hazelzet's memory module would be modified to add the functionality of buffering the data signals to the Memory Buffer, similar to that in the DDR3 LRDIMM, and training during initialization mode ("*second mode*") into which the module could be switched and which includes training sequences and which reports completion of those training sequences by a notification/status signal output over an open drain output (*e.g.*, UE 121) of Hazelzet.

165. In the JEDEC combination, the training sequences would be like those described as MB-DRAM Training in JEDEC (*e.g.*, Write Leveling and Read Enable Training), EX1015, 8, and the open drain output signal would be similar to

the signal output on the ERROUT# pin as described in JEDEC, *id.* at 8; *see also* EX1036, 8 (penultimate entry in table on page re ErrOut_n – is an open drain output for parity errors during normal operation). During those training sequences, the memory controller communicates no data with the module and performs no operations to read or write to the memory devices; the training is carried out by memory buffer (module controller) itself. EX1015, 8.

166. In the Buchmann combination, the training sequences would be like those described as TS0, EX1016(Buchmann) at FIG. 4, 5:51-7:2 & Tables 1-2, or alternatively, like those described as TS3, EX1016(Buchmann) at FIG. 6, 8:249:18 & Tables 5-6. The open drain output signals would be TS0_done, in the former case, EX1016(Buchmann) at FIG. 4, 5:51-7:2 & Tables 1-2, and TS3_ack or TS3_done, in the latter case, EX1016(Buchmann) at FIG. 6, 8:24-9:18 & Tables 5-6. Buchmann does not disclose the memory controller communicating any data with the module or performing operations to read or write to the memory devices during either TS0 or TS3 sequences during initialization/power-on.

167. In either combination, the circuitry of Hazelzet's module, in particular the ECC/Parity register, would be modified to implement the training as part of an additional mode to run, for example, at initialization with Hazelzet's other disclosed initialization operations and to use an open drain output of Hazelzet to communicate the new notification signals. EX1014(Hazelzet) at ¶[0123]

(initialization operations); EX1015, 3 (training occurs during initialization); EX1016(Buchmann) at 3:49-60 (same). As explained in more detail below, Hazelzet already uses his UE 121 open drain output for two different signals in two different modes. Thus, this ECC/Parity register necessarily includes circuitry for receiving inputs for each of those signals, and selecting which one to drive on the UE 121 output depending on the mode of the module. It was well within the level of ordinary skill to modify such circuitry such that it accepted three different inputs for three different modes and would select among them depending on the mode, and a Skilled Artisan could have made that modification without undue experimentation and with a reasonable expectation of success.

168. Finally, these combinations would employ known open drain signaling circuitry, which necessarily included a transistor having its source coupled to ground and its drain as the output. That is what a Skilled Artisan would understand the phrase “open drain” to mean. EX1017, FIGs 4&5. A Skilled Artisan would have also known that in order to use open drain signaling to indicate training completion among multiple modules, as here, the open drain output would have to be configured such that the transistor output is driven low (ground) while training is still occurring and driven high upon training completion. This is because, with an open drain configuration shared by multiple modules, any module can individually drive the output low, but it takes the collective action of all

connected modules to drive the output high. Moreover, a Skilled Artisan would also understand that to drive the output low (which would be a low impedance state), the gate of the transistor must be high, causing the transistor to conduct and connect the drain to ground. Conversely, to drive the output high (which would be a high impedance state), the gate of the transistor must be low, turning the transistor off. This is how an open drain output works. EX1014, ¶[0099]; EX1017, FIGs. 4-5, 5:65-6:18.

D. Reasons to Combine

169. All of the prior art relied on in this declaration to combine Hazelzet and JEDEC or Buchmann are analogous art to the 595 Patent because all are in the same field of invention – memory module design, including error detection and correction, initialization, training and the use of pins/paths for multiple purposes during different operations/modes, EX1001(595 Patent) at Abstract, 5:66-6:14;8:4-48 (purported invention is memory module with an operating mode during which parity checking occurs and another mode during which initialization/training occur, and the same errout pin is used to provide notification signals indicating status to the memory controller during both modes, either regarding parity or initialization/training); EX1014(Hazelzet) at Abstract, ¶¶[0007],[0069]-[0070],[0123] (explaining that invention relates to memory modules, with, among other things, two operating modes – ECC mode and parity mode, in which the two

modes share a signal pin for notifying the memory controller of errors – and initialization operations/modes); EX1015, 1, 3, 8 (noting document is JEDEC ballot for “LRDIMM DDR3 Memory Initialization Chapter Proposal”, that includes various training during initialization, including that utilizes the parity ERROUT# pin for multiple purposes including training notifications of status); EX1016, 1:7-9;3:49-60;4:51-5:50;12:60-13:41;14:1-63;20:20-21:19;33:45-67 (explaining that invention relates to memory modules, with, among other things, an SBC mode and a “high-speed” or “functional” mode, wherein the SBC mode combines initialization/training and ECC that runs at power-on initialization and can also be entered from normal (i.e., “high-speed” or “functional”) operation for ECC without full re-initialization/training); EX1022, ¶¶[0004]-[0005],[0032]-[0033],[0052] (explaining that invention relates to memory modules, with, among other things, two modes – “a normal operation mode and a configuration and test mode” (a part of which is called “training mode”) – and, during “training mode,” the “CRC signal path” (normally used for “error detection” and “correct[ion]”) is used to “loop back” “training patterns” sent on the “BCMD signal path” (a command signal) to train the BCMD signal path); EX1025, 15-18 (JEDEC memory module standard for FBDIMM, specifying, in addition to various operating modes, initialization sequences that “must sequence the AMB devices through the Disable, Calibrate, (back to Disable), *Training*, Testing, and Polling

states in order to transition the AMBs into the active channel L0 state” (*e.g.*, operating modes)); EX1027, 1:61-2:19;6:24-25;10:24-45 (discussing importance of training, including for memory modules, and disclosing, in addition to a “standard operating mode,” a “training mode” that occurs before “standard operating mode”); EX1017(Kim) at 1:16-22;5:49-57;6:8-18;11:20-34;12:36-53(explaining that invention relates to memory modules, with, among other things, two operating modes – ECC mode and parity mode, in which the two modes share a signal pin for notifying the memory controller of errors – and initialization operations/modes that includes “completing a training process to establish reliable communication”, and further teaching that “initialization circuitry” “may reside local to the” memory module and that, by doing so, “added performance may be obtained as related to the specific function, often while making use of unused circuits within the subsystem,” and further teaching that, in addition to sharing ECC and parity on the error out pin, “[i]n alternate exemplary embodiments, other functions also share the error feedback pin”), and each is reasonably pertinent to the problem addressed by that patent – increasing memory module capacity, performance, and/or reliability by sharing an output pin/path to perform multiple functions during multiple operations/modes, including initialization/training, EX1001(595 Patent) at Abstract, 5:66-6:14;8:4-48; EX1014(Hazelzet) at Abstract, ¶¶[0007],[0069]-[0070],[0123]; EX1015, 1, 3, 8; EX1016(Buchmann) at 1:7-9;3:49-60;4:51-

5:50;12:60-13:41;14:1-63;20:20-21:19;33:45-67; EX1022(Talbot) at ¶¶[0004]-[0005],[0032]-[0033],[0052]; EX1025, 15-18; EX1027, 1:61-2:19;6:24-25;10:24-45; EX1017(Kim) at 1:16-22;5:49-57;6:8-18;11:20-34;12:36-53.

170. Also, one skilled in the art would have considered each of the combinations analyzed here to be merely an arrangement of old elements with each performing the same function it had been known to perform and yielding no more than what one would expect from such an arrangement. Each of Hazelzet, JEDEC, Buchmann and Kim, for example, is a prior art disclosure employing known signaling and training techniques. Many prior art systems had similarly included such techniques. Combining them as described here would therefore have been well within the level of ordinary skill in the art, would not have resulted in any unpredictable results and could have been readily accomplished without undue experimentation and with a reasonable expectation of success.

171. A Skilled Artisan would have been motivated to make these combinations for at least the following reasons.

1. Motivation to Add Training

172. A Skilled Artisan would have been motivated to add training to the system of Hazelzet. For example, Hazelzet emphasizes the need for “improved overall system reliability.” EX1014(Hazelzet) at ¶[0003] (“Thus the emphasis and need for improved overall system reliability is increasing dramatically and requires

a comprehensive system solution that includes both a high degree of fault tolerance and overall reliability.”); *see also id.* at ¶[0042] (“The ECC/Parity buffer chips 21 on DIMM 20 include unique error correction code (ECC) circuitry that is coupled to the memory interface chip 18 via line 25 to provide even greater significant reliability enhancement to such servers. The inclusion of this new, improved error correction code (ECC) circuitry results in a significant reduction in interconnect failure.”), ¶[0044] (“The novel ECC/ Parity buffer 21 on DIMM 20 thus provides leading-edge performance and reliability and key operational features different from and unavailable from the prior art while retaining timing requirements generally consistent with devices such as the JEDEC 14 bit 1:2 DDR II register.”), Abstract (“A high density high reliability memory module with power gating and a fault tolerant address and command bus.”), ¶[0001] (“This invention relates generally to a high-density, high-reliability memory module with a fault tolerant address and command bus for use as a main memory that will achieve the degree of fault-tolerance and self-healing necessary for autonomic computing systems.”), ¶[0004] (“The present invention provides such a comprehensive system solution that includes the capability of high memory density and a high degree of fault tolerance and the overall differentiated system reliability long desired in the server market.”), ¶[0007] (“The present invention is directed to a high density high reliability memory controller/interface module, provided with a high degree of

compatibility with industry standard solutions, capable of meeting the desired density, performance and reliability requirements and interfacing with the presently available memory modules, as well as with existing or enhanced support devices. The present invention accomplishes all these ends, resulting in a high density and enhanced reliability memory solution at low cost.”). Given Hazelzet’s emphasis on the need for “improved overall system reliability,” one skilled in the art would have been motivated to add training to Hazelzet because it was known that training improved the reliability of a memory module’s operations. EX1027, 1:35-2:12 (discussing importance of training, including for DIMMs, given advent of DDR memory devices and increasing frequencies, and stating “During a training stage, such a memory controller may write certain data to and read certain data from a memory device, for example a DRAM, and shift the data signal in respect to the clock signal within the time domain, such that the data signal arrives at the memory device with a well-defined synchronization to the clock signal. The memory controller may vary this time shift until a written value corresponds to a read value, which indicates that timing is correct. *In this way, a reliable, fast, and efficient exchange of information is enabled.*” (emphasis added)); EX1025, 15-18 (“FBDIMM Architecture and Protocol” standard, specifying initialization sequences that “must sequence the AMB devices through the Disable, Calibrate, (back to Disable), *Training*, Testing, and Polling states in order to transition the

AMBs into the active channel L0 state” and, for training, noting that, “[b]efore the channel is initialized the bit lanes are not aligned to a frame boundary, thus preventing Channel and DRAM commands from being communicated to the AMBs” such that training is required). This is particularly true given the emerging DDR3 applications in the 2009-10 time-frame and their increased speeds. EX1045, 22-24 (2008 Micron technical note explaining need for training for reads and writes). Indeed, Hazelzet discloses that “[i]nitialization of the memory subsystem” should occur, it just does not address training as part of that initialization or provide any details regarding how to go about that aspect of initialization. EX1014, ¶[0123]; EX1017, 12:36-53.

173. Furthermore, the provisional admits that DDR3 LR-DIMMs and initializing LR-DIMMs were known at the time. EX1008, 22 (describing “recent proposal in JEDEC for L[R]-DIMM (load Reduced DIMM) requires the MCH to hand over one or more parts of the initialization operation sequences to the memory subsystem controller”). Although Hazelzet discloses a Registered DIMM (RDIMM), it would have been obvious to update Hazelzet’s RDIMM to a LR-DIMM of JEDEC for the reasons discussed below.

174. Further, JEDEC includes a portion of the draft standard for DDR3 LRDIMMs being voted upon by JEDEC members that specifically addresses “power-up initialization,” requires various training including “MB-DRAM

Training” and explains that, during that training, “[t]he MB performs ‘Write Leveling’ to the DRAMs **to ensure successful writes**, and ‘Read Enable Training’ **to ensure it can capture read data from the DRAMs correctly**, as part of the DRAM interface training,” and further teaches that “MB DRAM interface training must be completed before any MB host interface read or write training **to ensure that the MB DRAM interface is configured optimally for DRAM reads and writes.**” EX1015, 3,8-9 (emphasis added). These statements would have motivated a person of ordinary skill to add training to other systems, such as that of Hazelzet.

175. In particular, Hazelzet discloses a memory module that can include up to four ranks of memory devices. EX1014, Abstract. Hazelzet’s module has a DIMM format and includes a buffer/register (12) that buffers address and command signals, but the data lines are not buffered—an arrangement known at the time as a Registered DIMM. EX1014, FIG. 1, [0036]. In the DDR3 Load Reduced DIMM (LRDIMM), however, the Memory Buffer (MB) buffers data signals in addition to the address and command signals. EX1036, 5 (“Product Description”). The LRDIMM Design Specification explained in detail the advantages of adding the LRDIMM’s data buffering functionality to a Registered DIMM (RDIMM), like Hazelzet’s module, which buffers only address and command signals. *Id.* In particular, the LRDIMM Design Specification explained that “LRDIMM differs from RDIMMs in that the SDRAMs do not connect directly

to the edge connector The Memory Buffer (MB) buffers both address and data. Increased performance is achieved based on the LRDIMM presenting only one load to the system. Increased capacity is achieved since the MB drives only the SDRAMs on the module and therefore a well defined topology and load. The maximum number of SDRAM die is 144. The LRDIMM is intended to function in all RDIMM platforms with appropriate BIOS changes. Systems designed to function with LRDIMMs will be better able to take advantage of LRDIMM features.” *Id.*

176. Thus, a Skilled Artisan would have understood at the time that Hazelzet’s RDIMM can be upgraded with an LRDIMM functionality to buffer the data lines, not just the address and command lines. A Skilled Artisan would have been motivated to make such an upgrade because the LRDIMM’s data buffering increased performance by presenting a single load to the system instead of the multiple load on the data pins of Hazelzet’s module which had multiple ranks coupled to those data pins. The Skilled Artisan would have been further motivated to make such an upgrade because the LRDIMM would have worked even in RDIMM platforms (with appropriate BIOS changes), thus it was possible to achieve these advantages in existing, RDIMM based systems, like in Hazelzet. I note that these advantages of buffering the data lines in addition to buffering the address and command lines of a DIMM, thus isolating the memory devices from

the system bus, were well known to a Skilled Artisan at the time. *See, e.g.*, EX1028 (Ellsberry), [0031] (“Additionally, each memory bank switch 206 and 208 includes signal drivers to drive data signals to and from the memory banks and to and from the DIMM interface 202. This reduces resistive and/or capacitive loading of the data bus coupled to the DIMM interface and the bus...”). Thus, a Skilled Artisan would have understood that buffering the data lines on Hazelzet’s module, like in the LRDIMM format, would advantageously reduce the load of the four memory ranks on the module to a single load.

177. Accordingly, a Skilled Artisan would have been motivated to upgrade Hazelzet’s RDIMM with the functionality of buffering the data lines like in an LRDIMM because it would have increased the performance and allowed higher capacity by decreasing the load on the data lines. The Skilled Artisan would have been also motivated to use the initialization techniques of JEDEC for the upgraded LRDIMM, including MB-DRAM Training, because it ensured that the different interfaces, including the MB-DRAM interface are optimally configured for reading and writing the memory devices. EX1015, 8-9 (“MB DRAM interface training must be completed before any MB host interface read or write training to ensure that the MB DRAM interface is configured optimally for DRAM reads and writes.”). Such a combination would have been well within the level of skill at the time and provided nothing more than expected from the combination: an LRDIMM

with a memory buffer (MB) that buffered data, address and command signals and implemented training, including the notification of the completion of training, to ensure optimal configuration for reading and writing the memory devices.

178. Also, Buchmann's "SBC mode" is a mode of operation where "error correcting code" is provided, EX1016 (Buchmann) at 14:25-32, as well as a "training phase that allows more flexibility and improved control data exchange during start-up," *id.*, 3:64-67, to establish "reliable communication" on the bus, *id.* at 14:28-35 ("Quasi-static bit communication, also referred to as 'static bit communication' or 'SBC', can be used to control the sequence of link initialization and training phases to establish reliable communication on the high-speed bus. When error correction of an SBC sample is performed prior to checking for a static pattern, the error correction may be able to repair errors that would otherwise prevent the pattern from being static over a period of time."); *see also id.* at 14:5-8. Thus, one skilled in the art would have been motivated by Hazelzet's desire to improve reliability to look to systems such as JEDEC's and Buchman's that were designed to do just that.

179. Furthermore, Buchmann discloses a buffer/register that buffers data signals in addition to address and command signals. As I discussed above with reference to JEDEC, a Skilled Artisan would have been motivated to add the functionality of buffering the data signals to Hazelzet's Registered DIMM, because

Hazelzet's module can have up to four ranks of memory devices, each presenting its corresponding load on the data lines, and the Skilled Artisan would have understood that buffering the data lines lowers the load of the module to a single one (that of the buffer), allowing improved performance, higher frequencies of operation, and higher capacity, as discussed above. *Supra*, ¶¶164-168. The Skilled Artisan would have been also motivated to use Buchmann's initialization techniques for the upgraded Hazelzet module, including Buchmann's training and corresponding notifications, because those initialization techniques provided a known, reliable way for efficiently initializing the upgraded module. Accordingly, making the combination of Hazelzet and Buchmann was well within the level of skill at the time and provided nothing more than expected at the time, a DIMM with a buffer to buffer data, address and command signals and efficient training of that buffer during initialization to ensure optimal read and write performance during normal operation.

2. Motivation to Add Training In A Mode Separate from Normal Operations

180. One skilled in the art would also have been motivated to combine Hazelzet and JEDEC or Buchmann by adding training in a mode separate from normal operations because she would have known that memory systems are typically and most efficiently initialized/trained before normal operations occur. For example, it was well-known that training/initialization of a memory module

before normal operation was necessary to minimize errors, by “ensur[ing] successful writes,” and “ensur[ing] [the register on the DIMM] can capture read data from the DRAMs correctly.” EX1015, 8. Indeed, JEDEC’s training is taught to be completed as part of “power-up initialization,” before moving to “Normal Operation.” *Id.* at 3 (listing eight steps, including various training, as part of initialization before listing “Normal Operation” as step 9); *see also* EX1025, 15-18 (“FBDIMM Architecture and Protocol” standard, specifying initialization sequences that “must sequence the AMB devices through the Disable, Calibrate, (back to Disable), *Training*, Testing, and Polling states in order to transition the AMBs into the active channel L0 state” and, for training, noting that, “[b]efore the channel is initialized the bit lanes are not aligned to a frame boundary, thus preventing Channel and DRAM commands from being communicated to the AMBs” such that training sequences are required); EX1022, Fig. 4, ¶¶[0032], [0052],[0088-89]; EX1056, 18, 22, 25-26, 42-44, EX1057, Fig. 5, Abstract, 2:13-34, 2:60-3:3, 9:11-10:44. Likewise, Buchmann’s invention is an “initialization training sequence” completed at “power-on,” EX1016(Buchmann) at Abstract (explaining that its “memory buffer includes logic for executing a power-on and initialization training sequence initiated by the memory controller.”), which would also suggest to a Skilled Artisan that training before normal operation is important.

181. Because the memory system in Hazelzet would be initialized upon power-on, *see, e.g.*, EX1014(Hazelzet) at ¶[0123] (“Initialization of the memory subsystem may be completed via one or more methods, based on the available interface busses, the desired initialization speed, available space, cost/complexity objectives, subsystem interconnect structures, the use of alternate processors (such as a service processor) which may be used for this and other purposes, etc.”); *see also* EX1025, 15-18 (JEDEC memory module standard for FBDIMM, specifying initialization sequences that “must sequence the AMB devices through the Disable, Calibrate, (back to Disable), *Training*, Testing, and Polling states in order to transition the AMBs into the active channel L0 state” (*e.g.*, operating modes)); EX1027, 1:61-2:19; 6:24-25; 10:24-45 (discussing importance of training, including for memory modules, and disclosing, in addition to a “standard operating mode,” a “training mode” that occurs before “standard operating mode”), JEDEC’s and Buchmann’s training (that is disclosed in each to occur at initialization) would have complemented that power-up process as part of Hazelzet’s initialization, and one skilled in the art would have therefore been motivated to combine Hazelzet and JEDEC or Buchmann in a training mode occurring before, and separate from, other, normal operating modes.

182. To the extent Patent Owner might argue that in a prior IPR (IPR2018-00303), the Hazelzet and Buchmann references were combined in a different way,

and that somehow is evidence of hindsight, I disagree. A Skilled Artisan would understand that there are more than one obvious ways to combine references. In particular, a Skilled Artisan would have understood that training can be performed both during initialization and during normal operations. In fact, Buchmann itself discloses the options of utilizing either “memory channel repair and re-initialization” or “fast repair and re-initialization,” during “normal, run-time operation” in addition to initialization. EX1016, 12:60-13:41. Accordingly, it would have been obvious to use Buchmann’s training and notification techniques during either initialization (to correctly set up the system) or normal operation (to repair any errors).

3. Motivation to Use Hazelzet’s Open Drain Signaling for Training Notifications

183. In the obvious combination of Hazelzet and JEDEC or Buchmann analyzed here it would have been further obvious to employ the open-drain parity and ECC signal connections and techniques of Hazelzet to communicate the status of the JEDEC or Buchmann training sequences, any of which satisfies the claimed “*information related to the one or more training sequences*,” since they each indicate some status of the related training operation.

184. To be clear, as to JEDEC, it is my opinion that a Skilled Artisan would have found it obvious to communicate that the MB-DRAM training was completed using the open drain output (*e.g.*, UE 121) of Hazelzet, and, as to

Buchmann, it is my opinion that a Skilled Artisan would have found it obvious to communicate that the TS_done signal of Buchmann for TS0 training, and also obvious to communicate the TS3_ack and/or TS_done signals of Buchmann for TS3 training, using the open drain output (*e.g.*, UE 121) of Hazelzet, for the reasons set forth below.

185. For example, Hazelzet's "ECC mode" is a mode where a notification signal indicating an "uncorrectable error" (*i.e.*, "UE") can be output to the memory controller through the open-drain output line and 121 (*i.e.*, output for uncorrectable error "UE"). EX1014(Hazelzet) at FIG. 4B, ¶¶[0044],[0049],[0059],[0064],[0069],[0072],[0109]. The open-drain output line 121 (or "/Error (UE)" 121) is the same open drain output that is used for the parity error signal. EX1014 (Hazelzet) at FIG. 4B, ¶¶[0044],[0049],[0059], [0064],[0070],[0109]. The open-drain output line 121 is coupled to the memory controller of the host system using error edge connection number 142. EX1014(Hazelzet) at FIG. 7A (indicating "UE" is pin 142). As such, Hazelzet's implementation involves using the same open drain output ("/Error (UE)" 121), in two different modes, to output both a parity error notification signal and an ECC notification signal, depending on which mode the memory module is in. EX1014(Hazelzet) at FIG. 4B, ¶¶[0044],[0049],[0059],[0064],[0069-70],[0072],[0109]. Hazelzet's use of the same output in two different modes would have suggested to, and motivated a person of ordinary skill in the art

to use that same output in the added training mode, particularly when the training mode was implemented separate from, and before, the parity and ECC modes of Hazelzet, as here. In such a system, those modes, which include normal memory operations, would therefore not be using the open drain outputs while the training mode was running during initialization.

186. Similarly, JEDEC employs this same technique, using the same open drain output to communicate parity error and training completion in different modes. Thus, a Skilled Artisan would have viewed JEDEC's technique as a natural fit in the system of Hazelzet, and JEDEC's disclosure would have motivated the use of that technique in other systems, such as with Buchmann.

187. Further, a person of ordinary skill in the art would have been motivated to use the same output to notify error signals and training status because such multiple use of a pin was known, and would have been considered an efficient use of the limited number of output pins on integrated circuits. For instance, Kim, EX1017, is a patent assigned to IBM that shares with Hazelzet a substantial overlap in their disclosures, particularly in the disclosures of open-drain shared outputs and in the latter halves of their specifications. Kim was filed approximately a year and a half after Hazelzet and discloses additional details regarding the use of an open-drain output on a memory module to notify the memory controller of errors during a parity normal operating mode and during an ECC normal operating

mode. EX1017(Kim) at 1:16-22;5:49-57;6:8-16. Kim further teaches initialization operations (initialization/training modes) that include “completing a training process to establish reliable communication,” *id.* at 12:3653, teaches that “initialization circuitry” “may reside local to the” memory module and that, by doing so, “added performance may be obtained as related to the specific function, often while making use of unused circuits within the subsystem,” *id.* at 11:20-34, and further teaching that, in addition to sharing ECC and parity on the error out pin, “[i]n alternate exemplary embodiments, other functions also share the error feedback pin,” *id.* at 6:16-18. Such disclosures would have motivated a Skilled Artisan to use Hazelzet’s “/Error (UE)” 121 open-drain output (corresponding to Kim’s “error feedback pin”) to notify the memory controller that the training was in progress or done.

188. As another example, Talbot discloses memory modules, with, among other things, two modes – “a normal operation mode and a configuration and test mode” (a part of which is called “training mode”). EX1022(Talbot) at ¶¶[0004]-[0005],[0032]-[0033],[0052]. Talbot further discloses that, during the “training mode,” the “CRC signal path” (normally used for “error detection” and “correct[ion]”, *id.* at [0033]) is used to “loop[] back” “training patterns” sent on the “BCMD signal path” (a command signal) to train the BCMD signal path, *id.* at [0052]. Thus, Talbot discloses using a CRC (i.e. ECC) signal path to return signals

relating to training during the training mode when the CRC functionality is off. *Id.* at [0033],[0052]. Such disclosures would have motivated a Skilled Artisan to use Hazelzet's "/Error (UE)" 121 open-drain output (corresponding to Talbot's "CRC signal path") to notify the memory controller that the training was in progress or done.

189. Moreover, a Skilled Artisan would have been motivated to arrange the modified Hazelzet to communicate a signal indicating completion of training only when all memory modules have completed that training, in order to ensure that the entire memory system had been trained before proceeding to normal operation. This would permit training to be completed in an orderly and systematic manner, thereby limiting the complexity of the control circuitry needed to implement the training. EX1043, 7:30-51. Use of an open drain signal in this manner was a known, efficient way to communicate information about multiple circuits because it effectively OR'd the inputs into a single output. EX1017(Kim) at FIG. 4; 5:65-6:12 (illustrating and describing just such a system); *see also* EX1014(Hazelzet) at [0018] ("After holding the error line low for only 2 clock cycles, the driver can be disabled and the output permitted to return to an un-driven state (high impedance) thus allowing this line to be shared by multiple modules."), [0109] ("The error reporting circuitry, of the present invention is included to permit external monitoring of device operation. Two open-drain outputs are available to permit

multiple modules to share a common signal pin for reporting an error that occurred during a valid command (any /CS low) cycle (consistent with the re-driven signals).”).

190. In addition, a Skilled Artisan would have been further motivated to modify Hazelzet as described above, because Hazelzet’s memory system includes multiple memory modules in need of training. In other words, there would be a motivation to delay transitioning to a normal mode of operations until all memory modules had signaled the completion of training. EX1014(Hazelzet) at [0018] (“After holding the error line low for only 2 clock cycles, the driver can be disabled and the output permitted to return to an un-driven state (high impedance) thus allowing this line to be shared by multiple modules.”), [0109] (“The error reporting circuitry, of the present invention is included to permit external monitoring of device operation. Two open-drain outputs are available to permit multiple modules to share a common signal pin for reporting an error that occurred during a valid command (any /CS low) cycle (consistent with the re-driven signals).”); *see also* EX1017(Kim) at FIG. 4; 5:65-6:12; EX1043, 7:30-51. In particular, a Skilled Artisan would have been motivated to use Hazelzet’s open-drain output to notify the host of training status because that technique allows any module in the system to pull the open drain pin to “low” (i.e. to ground) if it is still executing its training sequence, regardless of whether other modules in the system

have completed training and are no longer pulling that pin low. *Id.* As I demonstrate above, an open drain was a known way to signal when multiple circuits were, or were not all, finished performing some operation. See ¶¶158–163.

V. COMPARISON OF THE PRIOR ART TO THE CLAIMS OF THE 595 PATENT

191. My analysis is based on my understanding of the law as set forth above and the ordinary and accustomed meaning of the claim terms as understood by one of ordinary skill in the art in view of the 595 Patent and its file history, including the constructions I presented for five of the claim terms. See ¶¶108–138.

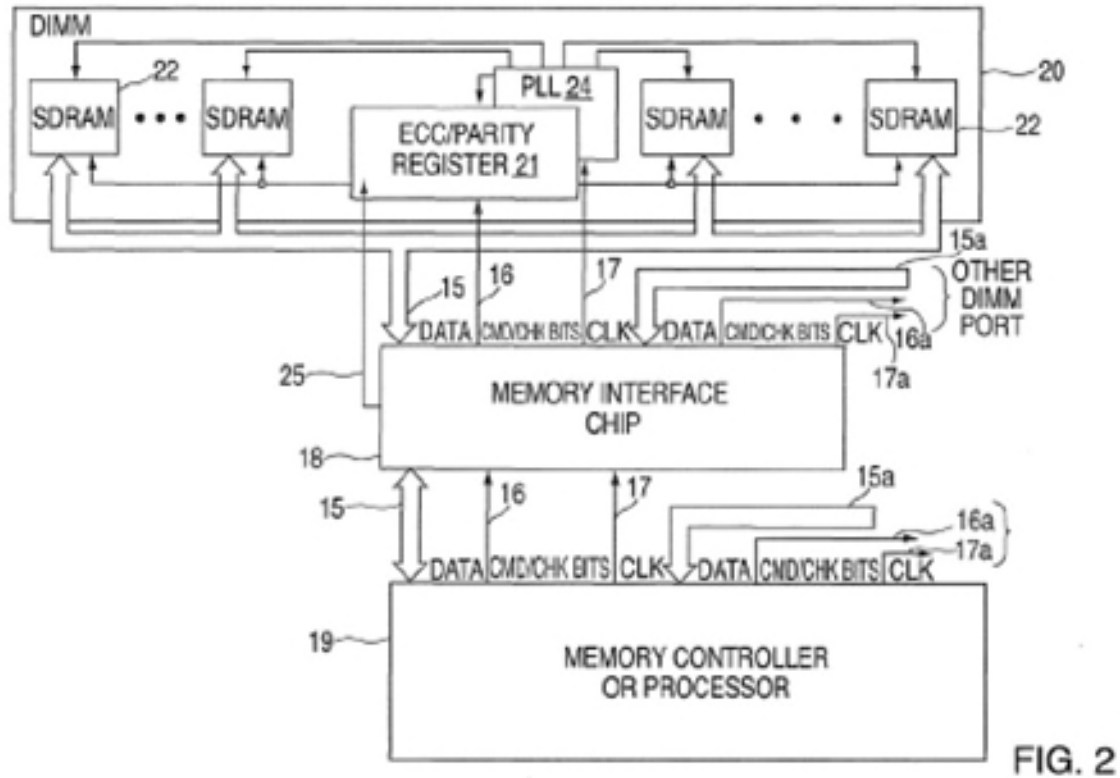
A. Claims 1-24 Are Unpatentable Over Hazelzet and JEDEC or Buchmann, with or without Kim for Certain Claims

1. Claim 1 is Unpatentable

a) [1.a] Preamble

192. The preamble of claim 1 requires “[a] memory module operable with a memory controller of a host system, comprising.”

193. Hazelzet discloses dual inline memory modules 20 (*i.e.*, “DIMMs”) that are configured to operate with the “memory controller” 19 of the host system. Ex. 1014 (Hazelzet) at FIGs. 2, 3A-3D, ¶¶[0037], [0038], [0039]; *see also* Ex. 1014 (Hazelzet) at ¶[0036] (referring to DIMMs as “dual inline memory modules”).



194. Accordingly, Hazelzet satisfies “[a] memory module operable with a memory controller of a host system.”

b) [1.b] Printed Circuit Board Having Edge Connections

195. Claim 1 requires “a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections.”

196. Hazelzet explains that the “DIMM of the present invention is comprised of a printed circuit board having a front side and a back side and a plurality of double data rate (DDR) DRAMs or synchronous dynamic random access memories (SDRAMs) affixed to both the front surface and the back surface,” EX1014, ¶[0015], examples of which are shown in FIGS. 2, 3A, 3B, 3C, and 3D. *See* EX1014, FIGS. 2, 3A-3D; *see also id.* at ¶[0037] (“Turning now to FIGS. 2, 3A, 3B, 3C, 3D, 4A, 4B, 5, 8, 9, 10 and 11, the enhanced server memory arrangement of the present invention will be described.”), ¶[0039], Abstract (“The memory module includes a rectangular printed circuit board having a first side and a second side, a length of between 149 and 153 millimeters and first and second ends having a width smaller than said length.”).

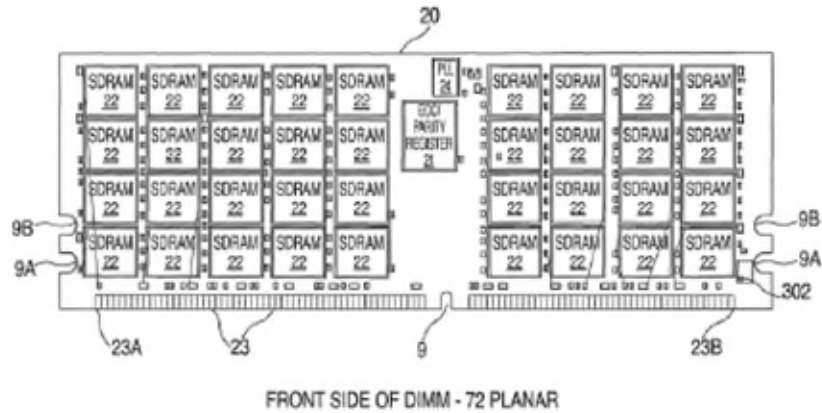


FIG. 3A

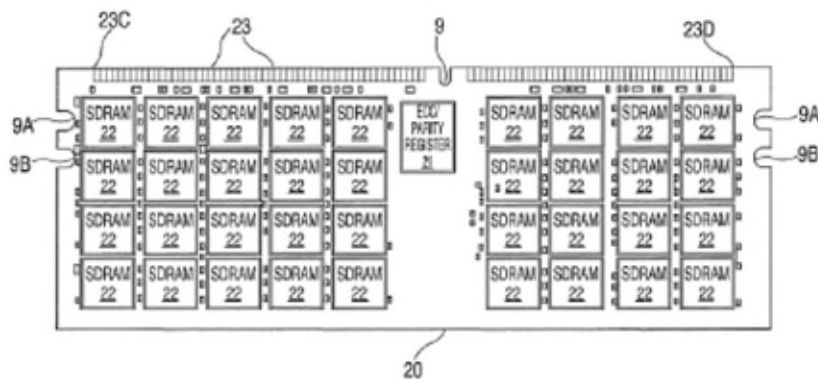


FIG. 3B

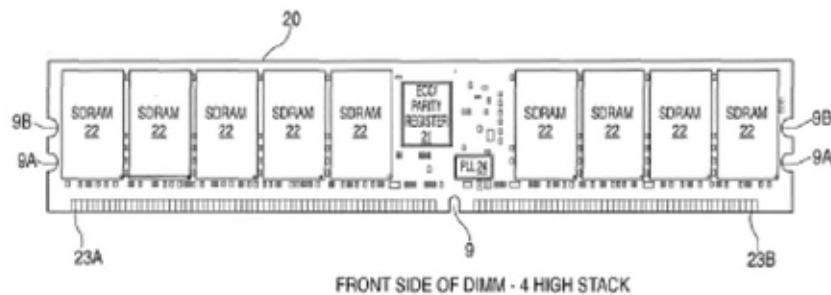


FIG. 3C

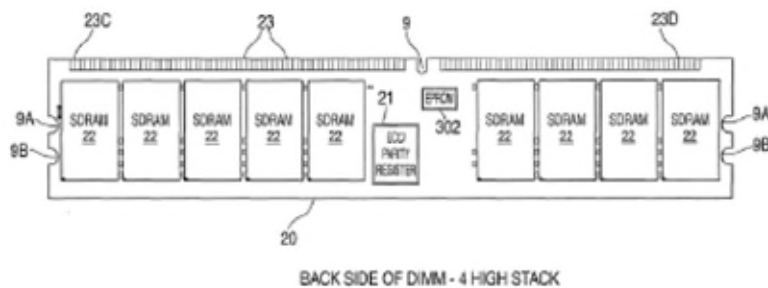
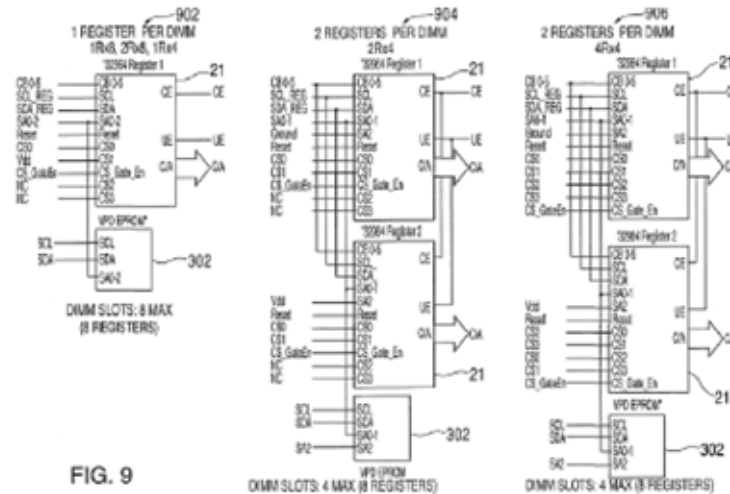


FIG. 3D

197. Hazelzet further explains that its memory modules include “connectors 23 along the edge of both the back and front sides” of the printed circuit board, Ex. 1014 (Hazelzet) at ¶[0039] (“Generally speaking DIMMs are printed circuit cards designed to carry a plurality of DRAMs 22 thereon and the DRAM output pins (not shown) are connected via the printed circuit to selected connectors 23 along the edge of both the back and front sides of the card and are often provided with a single indexing key or notch 9 on the connector edge.”), which are provided to form connections to the memory controller of the host system when the memory module is inserted into a corresponding “slot” of the host system. Ex. 1014 (Hazelzet) at ¶[0097] (“Referring to FIG. 11, column 1102 is the slot in the memory system being occupied by the memory module. ... For memory modules having one buffer chip 21, the IIC address correlates to the slot being occupied by the memory module as shown in column 1106”); *see also id.* at ¶[0032], FIG. 11, FIG. 9 (showing the maximum number of “DIMM slots” for “1, 2, and 4 rank DIMMs.”).



198. Hazelzet therefore discloses “a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller.”

199. Hazelzet further discloses that the printed circuit board has a first set of edge connections for communicating data signals between the memory module and the memory controller of the host system, Ex. 1014 (Hazelzet) at FIGs 7A-7C (showing data edge connections including pins 11, 12, 17, 18, 22, 23, 31, 32, 37, 38), while the memory module is in either the “parity mode” or the “ECC mode,” *id.* at FIG. 8 (showing “Data In” and “Data Out” in both the “parity mode” and the “ECC mode.”) , ¶¶[0015],[0035], [0038],[0041].

200. Hazelzet further discloses that the printed circuit board has a second set of edge connections for communicating address and control signals from the memory controller of the host system. Ex. 1014 (Hazelzet) at FIGs 7A-7C (showing address edge connections including pins 67, 70, 72-75, 82, 205-207, 210-

213, 220, 227 and command edge connections including pins 86, 89, 91, 93), ¶[0072] (referring to “/CS” as commands), ¶[0068] (listing various control signals including “chip select (CS), address (Addr), row address strobe (RAS), column address strobe (CAS) and write enable (WE)” signals); *see also* Ex. 1014 (Hazelzet) at ¶[0038] (“The memory interface chip 18 then sends and receives data, via line 15, to the memory devices or DRAMs 22 and sends address and command information to the register chip 21 via add/cmd line 16 and check bits for error correction purposes to the ECC/ Parity register chip 21 via line 25.”), FIG. 2 (showing address and command line 16), ¶¶[0015],[0035],[0041].

201. Hazelzet further explains that the printed circuit board has an error edge connection coupled to the open drain output of the module controller. Ex. 1014 (Hazelzet) at FIGs 7A (showing an uncorrectable error pin UE (142) of the memory module that is coupled to the open drain output “/Error (UE)” 121); *see also id.* at FIG. 4B, ¶¶[0072], [0109].

202. Accordingly, Hazelzet discloses “*the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections.*”

c) **[1.c] Dynamic Random Access Memory Elements**

203. Claim 1 requires “dynamic random access memory elements on the printed circuit board.”

204. Hazelzet explains that its memory module (DIMM) includes a plurality of “synchronous dynamic random access memories (SDRAMs)” / “DRAMs” on the “printed circuit board,” Ex. 1014 (Hazelzet) at ¶[0015] (“The DIMM of the present invention is comprised of a printed circuit board having a front side and a back side and a plurality of double data rate (DDR) DRAMs or synchronous dynamic random access memories (SDRAMs) affixed to both the front surface and the back surface.”), examples of which are shown in FIGS. 2, 3A, 3B, 3C, and 3D. See Ex. 1014 (Hazelzet) at FIGs. 2, 3A-3D; see also *id.* at ¶[0037], ¶[0039].

205. Accordingly, Hazelzet discloses “dynamic random access memory elements on the printed circuit board.”

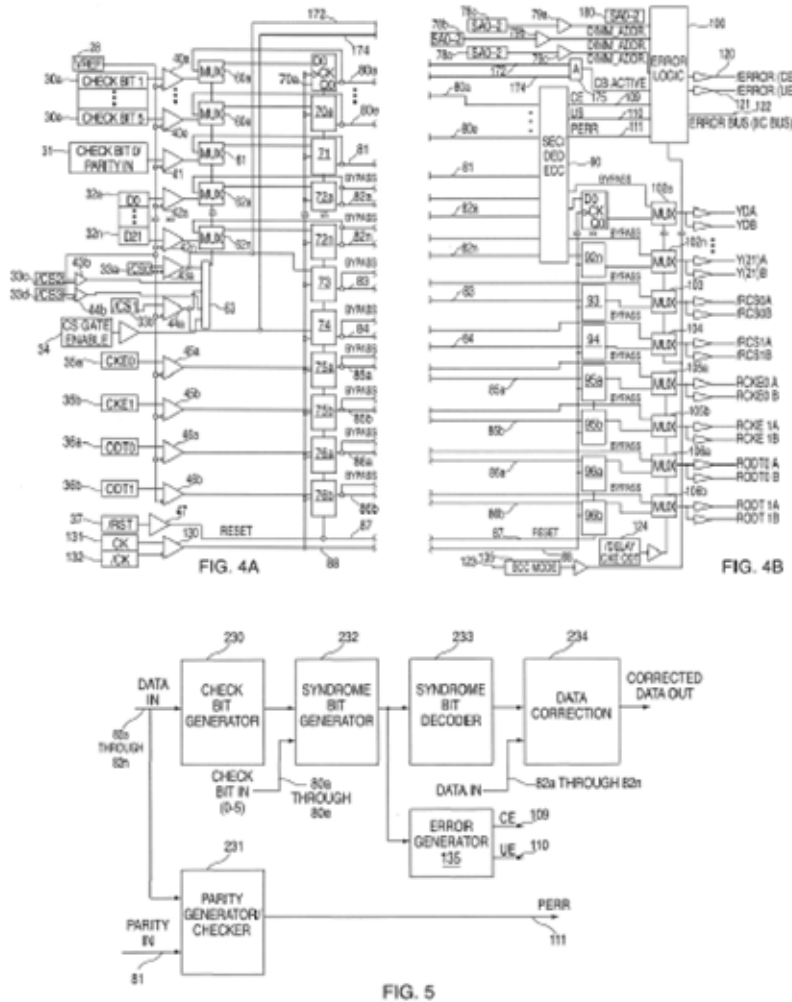
d) [1.d] Module Controller ... Having An Open Drain Output

206. Claim 1 requires “*a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection.*”

207. Hazelzet discloses an “ECC/Parity register,” which is the claimed “*module controller,*”⁹ having an output for uncorrectable errors (shown in FIG. 4B as “/ERROR (UE) 121”), which is the claimed “*open drain output.*” Ex. 1014

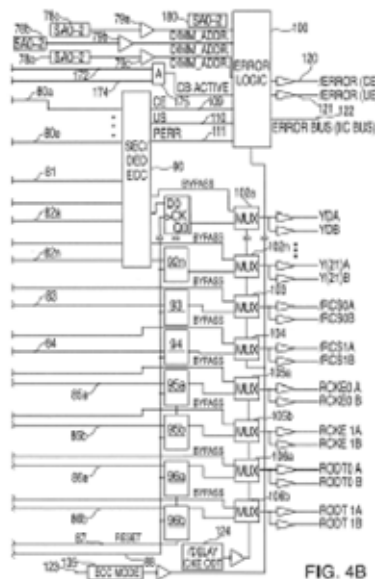
(Hazelzet) at FIGS. 3A-3D, 4A, 4B, 5, ¶¶[0044], [0059], [0072]. As shown in FIGs. 3A, 3B, 3C, and 3D, the “ECC/Parity register” is on the “printed circuit board” and coupled to the “synchronous dynamic random access memories (SDRAMs).” Ex. 1014 (Hazelzet) at FIGs. 3A-3D, ¶[0015] (“The DIMM of the present invention is comprised of a printed circuit board having a front side and a back side and a plurality of double data rate (DDR) DRAMs or synchronous dynamic random access memories (SDRAMs) affixed to both the front surface and the back surface.”), ¶[0039] (“Further, as shown in FIG. 3A on the front of each DIMM 20, in addition to the DRAMs, there is positioned a phase locked loop (PLL) chip 24 and the novel ECC/Parity Buffer chip 21 of the present invention.”), ¶[0042].

208. FIGS. 4A and 4B of Hazelzet show the “ECC/Parity register” of FIGS. 3A-3D in greater detail, and FIG. 5 of Hazelzet shows the “single error correction / double error detection error correction code (SEC/DED ECC) circuit of FIG. 4B.” Ex. 1014 (Hazelzet) at ¶¶[0027], [0028].



209. As shown in FIG. 4B, the “SEC/DED ECC” circuit is coupled to an “ERROR LOGIC” 100, both of which being part of the “ECC/Parity register” (i.e., “module controller,” as claimed). The “ERROR LOGIC” of the “ECC/Parity register” (i.e., “module controller,” as claimed) is coupled to an “error reporting circuitry” with two “open drain outputs,” one for correctable errors “CE” (120 of FIG. 4B) and another for uncorrectable errors “UE” (121 of FIG. 4B). Ex. 1014 (Hazelzet) at FIG. 4B, ¶[0072] (“Error reporting circuitry is included to permit external monitoring of DIMM operation. Two open-drain outputs are available to

permit multiple modules to share a common signal line for reporting an error that occurred during a valid command ($/CS=low$) cycle (consistent with the re-driven signals). These two outputs are driven low for two clocks to allow the memory controller time to sense the error. $/Error$ (CE) indicates that a correctable error occurred and was corrected by the ECC logic, $/Error$ (UE) indicates that an uncorrectable error occurred and depending on the mode selected is an uncorrectable ECC error or a parity error. Note that the timing of $/Error$ (UE) is different in parity mode vs. ECC mode.”). The output for uncorrectable errors (shown in FIG. 4B as “ $/ERROR$ (UE) 121”) is the “*open drain output*,” as claimed.



is coupled to the open drain output “/Error (UE)” 121); *see also id.* at FIG. 4B, ¶¶[0059],[0072].

211. Accordingly, Hazelzet discloses *a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection.*”

e) [1.e] Wherein Clauses

212. Claim 1 requires “*wherein the memory module is configurable to operate in any of at least a first mode and a second mode; wherein the memory module in the first mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences.*”

(1) [1.e.i] Two Modes

213. Hazelzet explains that its memory modules are configurable to operate in (1) a “parity mode,” which is the claimed “*first mode*,” and (2) an “ECC mode.” Ex. 1014 (Hazelzet) at FIG. 8; *see also id.* at ¶¶[0020], [0022], [0049], [0059]-

[0062], [0064], [0069]-[0070], [0072], [0075]. Hazelzet uses the term “mode” in accordance with the plain and ordinary meaning, Ex. 1014 at FIG. 8, ¶¶[0044], [0049], [0059]-[0065], [0069]-[0072], [0075], and therefore its “parity mode” satisfies the plain and ordinary meaning of the claim term “*mode*.” The combination of Hazelzet and Buchmann or, alternatively, Hazelzet and JEDEC DDR3, would add a “*second mode*” as claimed to the module. The combined module would therefore be configurable to operate in either mode, as it would enter either mode when instructed to do so by the appropriate control inputs. See ¶¶164–168.

(2) [1.e.ii] Normal Reads and Writes

214. Hazelzet discloses that “as shown in this FIG. 2, the memory interface chip 18 sends and receives data from the DIMMs via the data line 15 and sends address and commands via line 16.” EX1014, ¶[0038]; FIG. 2. The figure shows line 15 coupling the memory controller and the DRAMs, and line 16 coupling the memory controller and the register 21. *Id.* A Skilled Artisan would also understand from Figure 2 that lines 15 and 16 are coupled to edge connectors for data and address/control, respectively, since those lines coupled the DIMM to the memory controller. EX1014, FIGs. 2, 7A-7B, ¶¶[0015],[0035], [0038],[0041]. Hazelzet therefore discloses that the module is configurable to receive address and control signal via the edge connections included on the module for that purpose.

215. A Skilled Artisan would understand that such operations – communicating data with DRAMs while communicating address and command information with the register – to constitute “*normal memory read or write operations*” because they follow the standard configuration for such operations with a JEDEC compliant device, EX1014, ¶[0044, including sending address and control to the register and data to the DRAMs. EX1024, 1, 14, 16.

216. Furthermore, as I discussed above, it would have been obvious to a Skilled Artisan to add the functionality of buffering the data lines 15 to Hazelzet’s module as taught by JEDEC and Buchmann. *Supra*, ¶¶164-168. The presence of these data buffers, between the edge connectors and the memory devices on data lines 15, does not change the claimed characteristics of read and write operations during normal operation in response to requests from the system memory controller. Indeed, a Skilled Artisan would have understood that the read and write operations during normal operation would be performed like JEDEC defined protocols, as discussed further below. *See also* EX1014, [0044], [0124]; EX1036, 5, Ex. 1024, (JEDEC Standard, Double Data Rate (DDR) SDRAM Specification).

217. Hazelzet additionally explains that its “parity mode” is an “operating mode” with “no correction of errors.” Ex. 1014 (Hazelzet) at ¶[0064] (“A parity operating mode is also provided, in conjunction with error reporting circuitry to permit the system to interrogate the device to determine the error condition.”),

¶[0103] (“A parity operating mode is also provided, in conjunction with error reporting circuitry to permit the system to interrogate the device to determine the error condition.”); *see also id.* at ¶[0020] (“Still further the present invention permits operation of the memory module in parity mode, such that unused ECC check bit inputs are held at a low level thus ensuring that these inputs are at a known and quiescent state.”); ¶[0072] (“Error reporting circuitry is included to permit external monitoring of DIMM operation.”); ¶[0070] (“In addition to the above ECC mode, the same twenty two chip select gated data signals can be operated in ‘parity mode (/ECC Mode high), whereby the signal received on CHK0/Parity in line is received as parity to the register one clock pulse later than the chip select gated data inputs. The received parity bit is then compared to the parity calculated across these same inputs by the register parity logic to verify that the information has not been corrupted. ... No correction of errors will be completed in this mode.”). A Skilled Artisan would understand the phrase “operating mode” to refer to a mode in which the normal memory operations are employed to store data in or read data from the DRAMs of the module.

218. Hazelzet states that “[i]n Parity Mode, the memory interface chip or controller would generate a single parity bit **in conjunction with providing the full address and command field to the module**. The module would re-drive the address and command bits, to the DRAMs, in the next cycle-rather than adding the

additional cycle required in ECC mode. Any error on the address and command bus would be reported to the system at a later time, and the potential for recovery from the fail would be small hence this option is undesirable for many applications. The last mode would be to simply operate the memory in a mode with no parity bits and no ECC bits, with neither the added delay due to ECC nor any means to detect a fault on the address/command bus as per the prior art convention now used for these modules.” Ex. 1014 (Hazelzet) at ¶[0075]. A Skilled Artisan would understand “the full address and command field” in this context to refer to the signals sent to a memory module during a normal read or write operation. *See, e.g.,* Ex. 1024, JEDEC Standard, Double Data Rate (DDR) SDRAM Specification, JESD79 (June 2000) (“JESD79”) at page 14 (“The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–Ai (where i = 7 for x16, 8 for x8 or 9 for x4) selects the starting column location.” “The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–Ai (where i = 7 for x16, 8 for x8 or 9 for x4) selects the starting column location.”), page 16. Such operations include the reception at the module of address and control signals via their respective edge connections, and in response the communication of data signals between the system memory controller and the module DRAMs, which a

Skilled Artisan would understand to occur over the data edge connections of the module, with the DRAM being controlled by the module controller. EX1014, ¶[0038]; EX1024, 1.

219. Moreover, I note that Figure 8 of Hazelzet depicts a timing diagram used with his invention and explicitly discloses “Data In” and “Data Out” in parity mode. A Skilled Artisan would understand such movement of data to occur in the context of normal read and write operations. Ex. 1014 (Hazelzet) at FIG. 8.

220. Hazelzet therefore discloses that the address and control signals received by the module over the address/control edge connections are associated with “*normal memory read or write operations.*”

221. Moreover, Hazelzet relates this configuration to both his ECC and parity mode, EX1014, ¶[0038], so a Skilled Artisan would understand these operations occur in parity mode (*i.e.*, “*first mode,*” as claimed).

222. Accordingly, one skilled in the art would have understood Hazelzet’s parity mode to be a normal operating mode in which the module can be made, via the appropriate signaling, to perform “*one or more normal memory read or write operations,*” which include the communication of data with the memory controller (over edge connections provided for that purpose) and in response to address and control signals (received over edge connections provided for that purpose).

223. Further, FIG. 2 of Hazelzet discloses that address and command bits are driven to the DRAMs from the memory interface chip through the “ECC/Parity register” (*i.e.*, “*module controller*,” as claimed) using the address and command line (*i.e.*, “add/cmd line 16”) regardless of which mode the memory module is in (*i.e.*, including the “parity mode”). Ex. 1014 (Hazelzet) at ¶[0038], FIG. 2, FIGs 7A-7C (showing address edge connections including pins 67, 70, 72-75, 82, 205-207, 210-213, 220, 227 and command edge connections including pins 86, 89, 91, 93), ¶[0072] (referring to “/CS” as commands), ¶[0068] (listing various control signals including “chip select (CS), address (Addr), row address strobe (RAS), column address strobe (CAS) and write enable (WE)” signals); Ex. 1024 (JESD79) at page 13 (TRUTH TABLE 1a).

224. Accordingly, Hazelzet discloses “*wherein the memory module in the first mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections.*”

225. To the extent one might argue that Hazelzet does not sufficiently disclose this wherein clause, it would have been obvious to include those claim requirements in the system of Hazelzet. In fact, Hazelzet describes how its “parity mode” is an “operating mode” with “no correction of errors.” Ex. 1014 (Hazelzet) at ¶[0064], [0070]. In addition, Hazelzet states that “[i]n Parity Mode, the memory

interface chip or controller would generate a single parity bit in conjunction with providing the full address and command field to the module.” Ex. 1014 (Hazelzet) at ¶[0075]. Normal read and write operations were known in the prior art. EX1024, 14, 16. Based on these disclosures, a Skilled Artisan would have at least found it obvious to modify Hazelzet’s “parity mode” into the claimed “*first mode*” involving a normal read or write operation over the claimed edge connections because to do so would have permitted normal memory operations, the ultimate purpose of any memory module, using the existing and therefore convenient connections disclosed in Hazelzet and because it would have been common sense to do so. *See, e.g.*, Ex. 1024 (JESD79) at page 14, page 16. This is confirmed by the passage’s reference to a third mode without ECC or parity where the register would simply be “operat[ing] the memory,” which a Skilled Artisan would also understand to refer to the usual memory operations such as reading and writing. Ex. 1014 (Hazelzet) at ¶¶[0075]; *see also id.* at FIG. 8 (depicting a timing diagram used with his invention and explicitly discloses “Data In” and “Data Out” in parity mode).

226. Accordingly, the “*wherein the memory module in the first mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address*

and control signals received via the second edge connections” limitation would have been obvious in view of Hazelzet.

227. On the other hand, while the memory module is in the “ECC mode,” the “ECC/Parity register” (*i.e.*, “*module controller*,” as claimed) generates a notification signal that is “low, for two clocks,” and outputs the notification signal to the memory controller of the host system through the “/Error (UE)” 121 pin if/when an uncorrectable error is detected. Ex. 1014 (Hazelzet) at ¶[0059] (“When either [correctable] error line (CE) 109 or uncorrectable error line (UE) 110 is low this indicates that an error was identified as being associated with the address and/or command inputs (either correctable or uncorrectable). The error lines 120,121 will be active, *i.e.*, low, for two clock cycles simultaneous with the re-driven address/command data when operating in ECC mode or delayed by two clock cycles when operating in parity mode.”), ¶[0072] (“Two open-drain outputs are available to permit multiple modules to share a common signal line for reporting an error that occurred during a valid command (/CS=low) cycle (consistent with the re-driven signals). These two outputs are driven low for two clocks to allow the memory controller time to sense the error. /Error (CE) indicates that a correctable error occurred and was corrected by the ECC logic, /Error (UE) indicates that an uncorrectable error occurred and depending on the mode selected is an uncorrectable ECC error or a parity error. Note that the timing of /Error (UE)

is different in parity mode vs. ECC mode.”), FIG. 2, FIG. 4B, FIG. 7A (showing that the UE pin of the memory module is coupled to the memory controller of the host system using pin number 142).

228. Hazelzet’s notification signal from the “ECC/Parity register” (*i.e.*, “buffer chip”) indicates the status of the error correction sequence when the memory module is in the “ECC mode,” by indicating (1) whether “an error was identified” and (2) whether the error from the memory module is an “uncorrectable error.” Ex. 1014 (Hazelzet) at ¶¶[0059] (“When either [correctable] error line (CE) 109 or uncorrectable error line (UE) 110 is low this indicates that an error was identified as being associated with the address and/or command inputs (either correctable or uncorrectable). The error lines 120,121 will be active, *i.e.*, low, for two clock cycles simultaneous with the re-driven address/command data when operating in ECC mode or delayed by two clock cycles when operating in parity mode.”), [0069], [0072], FIG. 2, FIG. 4B, FIG. 7A; *see also id.*, at ¶[0092] (“As shown in configuration 902, outputs from the buffer chip 21 include an indication of whether the error is a correctable error (CE) or an uncorrectable error (UE) as well as the corrected (if error is correctable) command and address information, which connect to memory devices 22.”).

(3) [1.e.iii] Not Accessed

229. This claim also requires “wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations.” As noted above, the combinations analyzed here include JEDEC or Buchmann training sequences in a training mode wholly separate from any mode that includes normal memory operations in response to memory controller commands and it would have been obvious to make the combinations in that manner. See ¶¶164–168. Moreover, I note that neither Hazelzet, JEDEC, nor Buchmann disclose normal memory read or write operations in response to memory controller commands occurring in a training mode of the combinations analyzed. The combination therefore satisfies this claim language.

(4) [1.e.iv] Training Sequences

230. As explained above, see ¶¶164–168, the combinations analyzed here includes a separate training mode into which the module can be placed and in which the module can implement various training sequences (*e.g.*, Write Leveling and Read Enable Training per JEDEC/TS0 and TS3 per Buchmann) (“*operations related to one or more training sequences*”). Each of those operations includes a set of operations occurring in a particular order, used for training a memory module. For instance, a Skilled Artisan would understand “‘Write Leveling’ to the DRAMs to ensure successful writes, and ‘Read Enable Training’ to ensure it can

capture read data from the DRAMs correctly,” as each including a set of operations occurring in a particular order to train the memory module. EX1015 at 8; EX1040, 14:1-15:3; EX1018, Fig. 4. For example, a Skilled Artisan would understand operations described on page 8 of EX1039 to be operations performed in a particular order during MB-DRAM Training’s “‘Write Leveling,’” and the operations described on page 9 of EX1039 to be operations performed in a particular order during MB-DRAM Training’s “‘Read Enable Training.’”

Likewise, a Skilled Artisan would understand the various operations set forth in Buchmann as performed during the TS0 and TS3 operations as each including a set of operations occurring in a particular order to train the memory module. EX1016, FIGs. 4,6, 5:51-7:2,8:24-9:18. See for example the operations described in Table 1 of Buchmann, for TS0, and in Table 5 of Buchmann, for TS3. The combinations therefore satisfy this claim element.

f) [1.f] Operation Of Module Controller In the First Mode

231. Claim 1 requires “*wherein the module controller is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller is further*

configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the first mode.”

232. As explained in claim elements [1.b] and [1.e.], Hazelzet’s module can be placed into a parity mode, which is a normal operating mode in which the module is provided, over the edge connections identified for that purpose, address and control signals for performing “*one or more normal memory read or write operations.*” Ex. 1014 (Hazelzet) at FIGs. 2, 7A-7B, ¶¶[0015],[0035],[0038],[0041],[0064], [0070]; *see also* Ex. 1024 (JESD79) at page 14, page 16. For example, Hazelzet discloses providing “the full address and command field to the module” during parity mode, which a Skilled Artisan would understand to refer to the normal signaling that implements a memory read or write from a memory controller. EX1014, ¶[0075]. In addition, as further explained in claim element [1.e.], FIG. 2 of Hazelzet discloses that address and command bits are driven to the DRAMs from the memory interface chip through the “ECC/Parity register” (*i.e.*, “*module controller,*” as claimed) using the address and command line (*i.e.*, “add/cmd line 16”) in the “parity mode.” Ex. 1014 (Hazelzet) at ¶[0038] (“The memory interface chip 18 then sends and receives data, via line 15, to the memory devices, or DRAMs 22 and sends address and command information to the register chip 21 via add/cmd line 16 and check bits for error correction

purposes to the ECC/ Parity register chip 21 via line 25.”), FIG. 2; *see also id.* at FIGs 7A-7C (showing address edge connections including pins 67, 70, 72-75, 82, 205-207, 210-213, 220, 227 and command edge connections including pins 86, 89, 91, 93), ¶[0072] (referring to “/CS” as commands), ¶[0068] (listing various control signals including “chip select (CS), address (Addr), row address strobe (RAS), column address strobe (CAS) and write enable (WE)” signals). Given that the “write enable (WE)” is an exemplary control signal “*associated with the one or more normal memory read or write operations,*” *id.*; Ex. 1024 (JESD79) at page 13 (TRUTH TABLE 1a), Hazelzet satisfies the “*wherein the module controller is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations*” limitation.

233. Moreover, as explained in claim elements [1.b.] and [1.e.], Hazelzet discloses that the printed circuit board has a first set of edge connections for communicating data signals between the dynamic random access memory elements (within the memory module) and the memory controller of the host system, Ex. 1014 (Hazelzet) at FIGs 7A-7C (showing data edge connections including pins 11, 12, 17, 18, 22, 23, 31, 32, 37, 38), while the memory module is in the “parity mode,” *id.* at FIG. 8 (showing “Data In” and “Data Out” in both the “parity mode” and the “ECC mode.”); *see also id.* at FIGs. 3A-3D, ¶[0015] (“The DIMM of the

present invention is comprised of a printed circuit board having a front side and a back side and a plurality of double data rate (DDR) DRAMs or synchronous dynamic random access memories (SDRAMs) affixed to both the front surface and the back surface.”), ¶¶[0035],[0038],[0041]. Further, as explained in claim element [1.e.], data communication between the memory module and the memory controller is “*in accordance with the address and control signals.*” See, e.g., Ex. 1014 (Hazelzet) at FIGs 2,8, ¶¶[0015],[0035],[0038], [0041],[0064],[0070]; Ex. 1024 (JESD79) at page 13 (TRUTH TABLE 1a). Accordingly, Hazelzet satisfies the “*wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals*” limitation.

234. As explained in claim elements [1.b.] and [1.d.], the error edge connection is coupled to the open drain output of the module controller. Ex. 1014 (Hazelzet) at FIGs 7A (showing an uncorrectable error pin UE (142) of the memory module that is coupled to the open drain output “/Error (UE)” 121); see also *id.* at FIG. 4B, ¶¶[0059],[0072].

235. In particular, Hazelzet’s “ECC/Parity register” (i.e., “*module controller,*” as claimed) includes an “SEC/DED ECC” 90. Ex. 1014 (Hazelzet) at FIG. 4B. FIG. 5 of Hazelzet, which is a block diagram of the “SEC/DED ECC” 90

in FIG. 4B, includes a “parity generator/checker circuit 231.” Ex. 1014 (Hazelzet) at ¶¶[0028], [0076], FIG. 5.

236. When the memory module is in the “parity mode” (*i.e.*, “*first mode*,” as claimed), the “parity generator/checker circuit 231” generates and sends the “parity error signal (PERR)” to the “error logic circuit” 100. Ex. 1014 (Hazelzet) at ¶[0076] (“FIG. 5 is a block diagram of the SEC/DED ECC circuit of FIG. 4B. ... The parity generator/checker circuit 231 further has a second input coupled to the parity in signal source 31 via primary latch 71 and output line 81 and depending on the state of the parity input signal on input 31 sends a parity error signal (PERR) on output line 111 to the error logic circuit 100.”), FIG. 5; *see also* Ex. 1014 (Hazelzet) at ¶[0070] (“In addition to the above ECC mode, the same twenty two chip select gated data signals can be operated in ‘parity mode (/ECC Mode high)’, whereby the signal received on CHK0/Parity in line is received as parity to the register one clock pulse later than the chip select gated data inputs. The received parity bit is then compared to the parity calculated across these same inputs by the register parity logic to verify that the information has not been corrupted. The twenty two chip select gated data signals will be latched and re-driven on the first clock pulse and any error will be reported two clock pulses later via the Uncorrectable Error (UE) line (driven low for two clock pulses) and in the Error Bus Registers. No correction of errors will be completed in this mode. The

convention of parity, in this application, is odd parity (odd numbers of 1s [sic] across data and parity inputs equals valid parity).”), FIG. 4B.

237. In the “parity mode” (i.e., “*first mode*,” as claimed), the “parity error signal (PERR)” 111 that is fed into the “error logic circuit” 100 is used to drive the open-drain transistor in “error logic circuit” 100, which outputs to the memory controller through the output line 121 (i.e., output for uncorrectable error “UE”). Ex. 1014 (Hazelzet) at ¶[0059] (“This SEC/DED ECC circuit 90 provides three outputs 109, 110, and 111 to the error logic circuit 100. These outputs are: a correctable error (CE) line 109, an uncorrectable error (UE) line 110 and a parity error bit line 111 fed to the error logic circuit 100 which provides outputs regarding correctable and uncorrectable errors on output lines 120 and 121. When either [correctable] error line (CE) 109 or uncorrectable error line (UE) 110 is low this indicates that an error was identified as being associated with the address and/or command inputs (either correctable or uncorrectable). The error lines 120,121 will be active, i.e., low, for two clock cycles simultaneous with the re-driven address/command data when operating in ECC mode or delayed by two clock cycles when operating in parity mode.”).

238. As explained above, the output line 121 (“UE”) is an open-drain output, Ex. 1014 (Hazelzet) at ¶[0072], which is coupled to the memory controller of the host system using pin number 142. Ex. 1014 (Hazelzet) at FIG. 7A (showing

that the “Server PIN Number 142” corresponds to “DIMM PIN Name UE”), FIG. 2 (showing how the “DIMM 20” is coupled to the “Memory Controller or Processor 19”); *see also id.* at ¶[0016] (“More particularly the server of the present invention comprises a novel DIMM provided with a new and unique ECC/ Parity Register that is operable with 1 to 4 memory ranks, coupled to a memory interface chip which is in turn coupled to a memory controller or processor such that the memory controller sends address and command information to the buffer (or register) via address/command lines together with check bits for error correction purposes to the ECC/ Parity register.”), ¶[0038] (“In this FIG. 2 the server comprises a novel DIMM 20 provided with a novel ECC/Parity Buffer chip 21 (also referred to as a ‘buffer device’) coupled to the memory interface chip 18 which is in turn coupled to the memory controller or processor 19.” “In this configuration, the check bits and/or parity bits associated with the ECC/Parity register chip 21 are developed in the memory interface chip 18, although in other embodiments these bits could be developed in the memory controller or processor 19, be communicated to the memory interface chip as a subset of the information on line 16 and the memory interface would then re-drive this information to the memory module on line 25”).

SERVER DIMM PIN NUMBER PIN NAME	SERVER DIMM PIN NUMBER PIN NAME
1 VREF	139 VREF
2 SCL	140 SCL
3 SDA	141 SDA
4 UE	142 UE
5 CE	143 CE
6 VDD	144 VDD
7 EC-MODE	145 EC-MODE
8 OLY CS#/ODT	146 OLY CS#/ODT
9 CS GATE EN	147 CS GATE EN
10 GND	148 GND
11 GND	149 GND
12 DQ1	150 DQ5
13 GND	151 GND
14 DQ2#	152 DQ9
15 DQ3	153 DQ9#
16 GND	154 GND
17 DQ2	155 DQ6
18 DQ3	156 DQ7
19 GND	157 GND
20 VDD	158 VDD
21 GND	159 GND
22 DQ8	160 DQ12
23 DQ9	161 DQ13
24 GND	162 GND
25 DQ2#	163 DQ13
26 DQ21	164 DQ10#
27 GND	165 GND
28 DQ10	166 DQ14
29 DQ11	167 DQ15
30 GND	168 GND
31 DQ16	169 DQ20
32 DQ17	170 DQ21
33 GND	171 GND
34 DQ2#	172 DQ21#
35 DQ12	173 DQ21#
36 GND	174 GND
37 DQ16	175 DQ22
38 DQ19	176 DQ23
39 GND	177 GND
40 RESET	178 RESET
41 VDD	179 VDD
42 GND	180 GND
43 DQ24	181 DQ28
44 DQ25	182 DQ29
45 GND	183 GND
46 DQ21#	184 DQ12
47 DQ23	185 DQ12#
48 GND	186 GND
49 DQ26	187 DQ30
50 DQ27	188 DQ31
51 GND	189 GND
52 CS#	190 CS#

FIG. 7A

239. Hazelzet explains that the generated parity error signal is driven to the memory controller of the host system. Ex. 1014 (Hazelzet) at ¶[0044], FIG. 2 (showing that the signals generated by the “DIMM 20” is driven to the “Memory Controller or Processor 19” through data paths 15 and 15a), ¶[0036] (“Each DRAM 11 on the DIMM 10 has a plurality of input/output pins that are coupled, via the printed circuitry on the DIMM 10 to the contacts on the DIMM 10 and theses contacts are further coupled, via a data line 15, to a memory interface chip 18 and to a memory controller or processor 19.”); *see also id.* at ¶[0072] (“Two open-drain outputs are available to permit multiple modules to share a common signal line for reporting an error that occurred during a valid command (/CS=low) cycle (consistent with the re-driven signals). These two outputs are driven low for

two clocks to allow the memory controller time to sense the error. /Error (CE) indicates that a correctable error occurred and was corrected by the ECC logic, /Error (UE) indicates that an uncorrectable error occurred and depending on the mode selected is an uncorrectable ECC error or a parity error. Note that the timing of /Error (UE) is different in parity mode vs. ECC mode.”).

240. Hazelzet explains that the “parity operating mode” is a mode that allows the host system to “determine the error condition” of the memory module. Ex. 1014 (Hazelzet) at ¶[0064] (“A parity operating mode is also provided, in conjunction with error reporting circuitry to permit the system to interrogate the device to determine the error condition.”). Hazelzet further explains that such “error condition” is reported to the host “via the Uncorrectable Error (UE) line” when the memory module is in the “parity mode.” Ex. 1014 (Hazelzet) at ¶[0070] (“In addition to the above ECC mode, the same twenty two chip select gated data signals can be operated in ‘parity mode (/ECC Mode high)’, whereby the signal received on CHK0/Parity in line is received as parity to the register one clock pulse later than the chip select gated data inputs. The received parity bit is then compared to the parity calculated across these same inputs by the register parity logic to verify that the information has not been corrupted. The twenty two chip select gated data signals will be latched and re-driven on the first clock pulse and any error will be reported two clock pulses later via the Uncorrectable Error (UE) line”).

(driven low for two clock pulses) and in the Error Bus Registers. No correction of errors will be completed in this mode. The convention of parity, in this application, is odd parity (odd numbers of 1s [*sic*] across data and parity inputs equals valid parity).”). Hazelzet further explains that the error line is driven “low, i.e., ‘0’,” when “an error is detected.” Ex. 1014 (Hazelzet) at ¶[0099] (“Parity error reporting in the present invention is realized by delivering the parity signal one cycle after the address and command to which it applies, and driving the error line low, i.e., ‘0’ two clock cycles after the address and command bits are driven to the DRAMs from the memory interface chip if an error is detected. After holding the error line low for only 2 clock cycles, the driver will be disabled and the output permitted to return to an un-driven state (high impedance) allowing this line to be shared by multiple modules.”), ¶[0018] (“Still another object of the invention is to provide for Parity error reporting in which the parity signal is delivered one cycle after the address and command to which it applies, and the error line be driven low two clocks after the address and command bits are driven to the DRAMs from the register on the DIMM.”), FIG. 8 (explaining that UE is driven low “if an error occurs” in the “parity mode”).

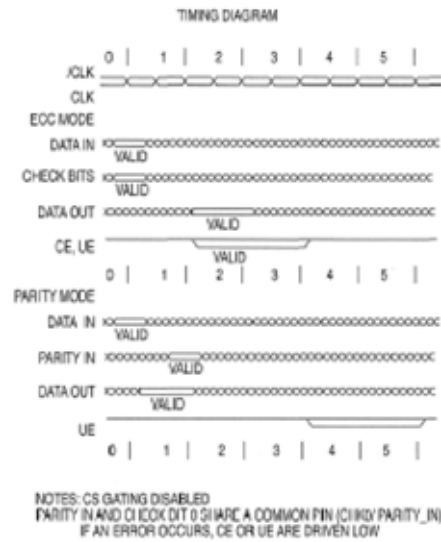


FIG. 8

241. Accordingly, Hazelzet discloses “wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the first mode.”

g) [1.g] Operation Of Module Controller In The Second Mode

242. Claim 1 requires “wherein the module controller in the second mode is further configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection to a first state or to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.”

243. As demonstrated above, ¶¶164–168, in the combinations analyzed here, the Hazelzet module would be modified to be configurable to enter a training

mode and output JEDEC or Buchmann training status signals to the system memory controller via the open drain output UE 121. *Id.* Each of the status signals analyzed above (ERROUT#, TS0_done, TS3_ack, TS3_done) represent “*information related to the one or more training sequences*” because each provides status about the related sequences, such as whether it has been completed or whether all memory buffers have returned an acknowledgement. *Id.* Each of these combinations therefore alternatively satisfies “*wherein the module controller in the second mode is further configurable to provide information related to the one or more training sequences.*”

244. Moreover, Hazelzet’s memory system involves sharing the open drain output so that the memory controller of the host system can receive parity error signals/notification signals from multiple memory modules using the open drain output. *See, e.g.,* Ex. 1014 (Hazelzet) at ¶¶[0018] (“After holding the error line low for only 2 clock cycles, the driver can be disabled and the output permitted to return to an un-driven state (high impedance) thus allowing this line to be shared by multiple modules.”), [0072] (“Two open-drain outputs are available to permit multiple modules to share a common signal line for reporting an error that occurred during a valid command (/CS=low) cycle (consistent with the re-driven signals).”), [0099], [0109]; *see also* ¶¶158–163, *above*.

245. As noted above, in the combinations analyzed here, the training status signals would be at a low logic level (because the gate signals of the transistors in the open drain circuits in all the modules in which the training is ongoing are high) over an open drain output of Hazelzet until such time as the operations they related to completed for all modules of the system and the gate signals to the transistors of all the open drain circuits in all the modules are low, at which time the signals would be at a high impedance state, indicating completion. EX1017, FIG. 4; 5:65-6:12 (illustrating and describing how such a system as is in Hazelzet operates); EX1001, 9:47-10:50 (explaining in same way as Kim functioning of open-drain outputs in memory systems). As I note above, ¶¶164–168, it would have been obvious to use Hazelzet's open drain signaling for these particular training signals because each indicates when operations carried out by multiple modules have completed. The high and low gate signals to the transistors represent “*driving the open drain output and the error edge connection to a first state or to a second state,*” respectively or vice versa.

246. A Skilled Artisan would understand that, in the obvious combinations analyzed here, such open drain signals would be changed from a high impedance state to a low state as the gate of the transistor changes from a low to a high to indicate the related training operations were in progress, and changed from a low state to a high impedance state as the gate of the transistor driving the signal

changes from a high to a low to indicate when the related operations completed in each memory module. Ex. 1014 (Hazelzet) at ¶¶ [0059], [0070], [0072], FIG. 4B; EX1017, FIGs. 4-5; 5:65-6:18 (teaching how a shared error pin can be implemented using an open drain configuration and/or an OR-gate); EX1015 (JEDEC), 8; Ex. 1016 (Buchmann) at 5:51-7:2, Table 1, Table 2, FIG. 4, 8:249:18, Table 5, Table 6, FIG. 6, 8:24-9:17, 3:52-54, 27:18-21, 26:30-32; *see also* ¶¶158–163.

247. Each combination therefore alternatively satisfies “*one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.*”

2. Claim 2 is Unpatentable

248. Claim 2 requires “[t]he memory module of claim 1, wherein the module controller comprises an integrated circuit.”

249. Hazelzet’s “ECC/Parity register” (*i.e.*, “*module controller*,” as claimed) is also referred to as a “buffer device” or a “buffer chip.” Ex. 1014 (Hazelzet) at ¶[0038]. Hazelzet further explains that the module support devices, including “buffers” (*i.e.*, “*module controller*,” as claimed), “registers,” and “PLL” may be comprised of “multiple separate chips” or may be “combined onto a single package or even integrated onto a single device.” Ex. 1014 (Hazelzet) at ¶[0115]; *see also id.* at FIG. 3A-3D, ¶[0039] (“It should be understood that the PLL chip 24

can be eliminated if its circuitry is provided on the buffer chip 21 or within the same package as the buffer chip 21.”), ¶[0042]. Accordingly, Hazelzet discloses that “*the module controller comprises an integrated circuit,*” as claimed.

250. The obvious combinations of Hazelzet and JEDEC or Buchmann therefore satisfy the “*wherein the module controller comprises an integrated circuit*” limitation.

3. Claim 3 is Unpatentable

251. Claim 3 requires “[t]he memory module of claim 1, wherein the module controller includes a notification circuit comprising a transistor having an open drain coupled to the open drain output and source coupled to the ground.”

252. As explained in claim element [1.d.], Hazelzet discloses that the “ECC/Parity register” (i.e., “*module controller,*” as claimed) has “open drain output[s].” Hazelzet further explains that the “ECC/Parity register” has an “error correction code circuit ECC segment 21b,” which is a “*notification circuit,*” as claimed, because it outputs signals notifying the system memory controller of correctable, uncorrectable, and parity errors. Ex. 1014 (Hazelzet) at ¶[0044] (explaining that the “error correction code circuit ECC segment 21b” is within the “ECC/Parity buffer chip 21,” i.e., “ECC/Parity register”). Such “error correction code circuit ECC segment 21b” (within the “ECC/Parity register”) includes the circuitry for determining whether the errors occurred, SEC/DED ECC circuit 90,

and error logic circuit 100 that receives error signals from SEC/DED ECC circuit 90, such as UE 110 and PERR 111, and provides the above-mentioned “open-drain output(s),” such as UE 121. Ex. 1014 (Hazelzet) at FIG 4B, ¶¶[0059],[0072] (“Two open-drain outputs are available to permit multiple modules to share a common signal line for reporting an error that occurred during a valid command (/CS=low) cycle (consistent with the re-driven signals). These two outputs are driven low for two clocks to allow the memory controller time to sense the error. /Error (CE) indicates that a correctable error occurred and was corrected by the ECC logic, /Error (UE) indicates that an uncorrectable error occurred and depending on the mode selected is an uncorrectable ECC error or a parity error. Note that the timing of /Error (UE) is different in parity mode vs. ECC mode.”).

253. Hazelzet discloses that those “open-drain outputs are available to permit multiple modules to share a common signal line for reporting an error,” and further discloses that the “outputs are driven low for two clocks to allow the memory controller time to sense the error. ... /Error (UE) indicates that an uncorrectable error occurred and depending on the mode selected is an uncorrectable ECC error or a parity error.”). Further, Hazelzet explains that its open-drain output is driven “low” (i.e., to ground) when the driver is enabled (i.e., gate receives a high voltage), and further explains that the open-drain “output [is] permitted to return to an un-driven state (high impedance)” when the “driver [is]

disabled.” Ex. 1014 (Hazelzet) at ¶[0099] (“Parity error reporting in the present invention is realized by delivering the parity signal one cycle after the address and command to which it applies, and driving the error line low, i.e., ‘0’ two clock cycles after the address and command bits are driven to the DRAMs from the memory interface chip if an error is detected. After holding the error line low for only 2 clock cycles, the driver will be disabled and the output permitted to return to an un-driven state (high impedance) allowing this line to be shared by multiple modules.”).

254. As noted above, the combinations analyzed here include a field effect transistor. Indeed, a Skilled Artisan would have understood the phrase “open drain” in the context of Hazelzet’s disclosures to necessarily mean the output is driven by a field effect transistor (as opposed to an open collector configuration), and that field effect transistors have three terminals, i.e., gate, source, and drain, that the drain would be connected to a pull-up resistor, the source to ground and the gate to an OR logic element that OR’ed the UE 110 and PERR 111 error signals to drive the gate, as depicted in Figure 5 of Kim. EX1017, FIGs. 4-5, 5:65-6:18; *see also generally* Ex. 1020, U.S. 3,414,781 to Dill (“Dill”), entitled “Field Effect Transistor Having Interdigitated Source And Drain And Overlying, Insulated Gate.” A Skilled Artisan would have thus understood that the disclosed “open drain” output is the output of “*a transistor having an open drain*” while the

“source” of that transistor is “*coupled to the ground.*” See ¶¶158–163; *see also* EX1017 (Kim) at FIG. 4, 5:49-57, 4:40-48; 6:1-16. Furthermore, even if not inherently disclosed, it would have been obvious to a Skilled Artisan to implement in this fashion given the knowledge of a Skilled Artisan regarding open drain outputs. See ¶¶158–163.

255. The obvious combinations of Hazelzet and JEDEC or Buchmann therefore satisfy “the module controller includes a notification circuit comprising a transistor having an open drain coupled to the open drain output and source coupled to the ground” limitation.

256. To the extent one might argue otherwise, claim 3 would have been obvious in view of Hazelzet, JEDEC or Buchmann, and Kim. Kim discloses an “open drain output” that is an output pin coupled to the drain of a transistor, which includes three ports (*i.e.*, a gate, source, and a drain). *See, e.g.*, Ex. 1017 (Kim) at FIG. 4. In particular, FIG. 4 of Kim shows an open drain output that is coupled to a pull-up resistor (*i.e.*, connected to a high voltage via a pull-up resistor). FIG. 4 of Kim also shows that the source of the transistor is coupled to ground and that the gate of the transistor is coupled to “ERR.”

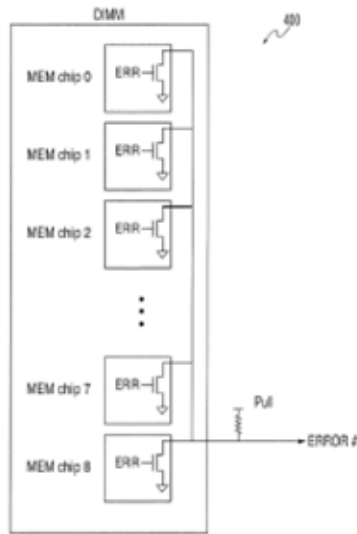


FIG. 4

257. Kim also discloses in Figure 5 the use of a logic element (an OR gate) such that multiple error signals could drive the gate of the open-drain transistor. EX1017, FIG. 5, 6:13-6:18.

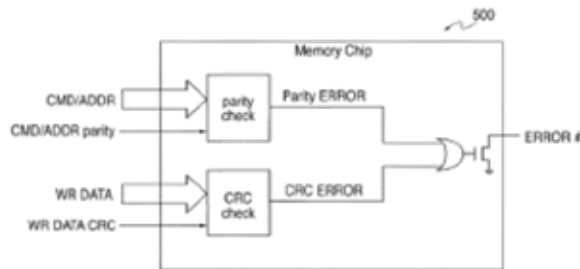
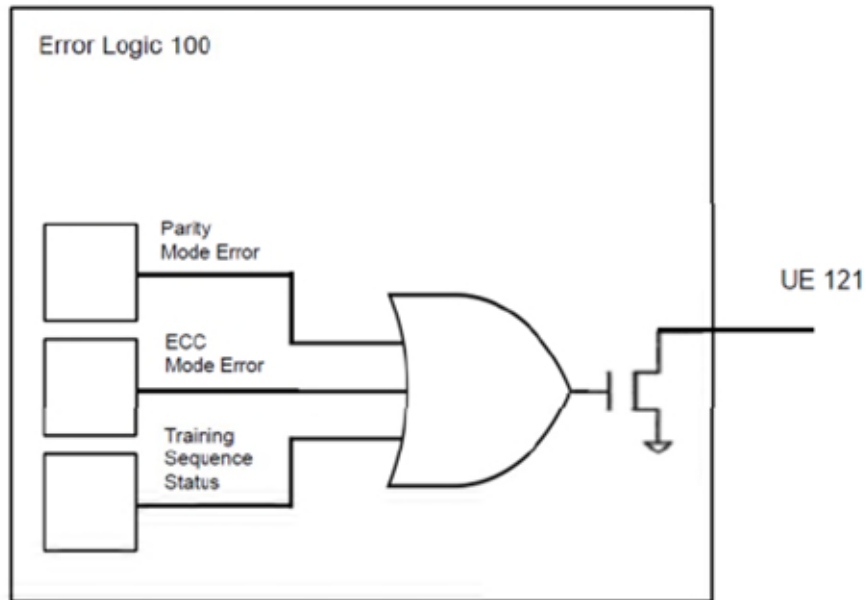


FIG. 5

258. In the combinations analyzed here, Kim's open drain transistor configuration would be included within Hazelzet's error logic 100 (which is part of the ECC segment 21b – a “notification circuit” as claimed) such that signals indicating parity mode error, ECC mode error and training status would be provided to a logic gate, such as an OR gate, as in Kim, which would select among them based on the mode of the module, as in Hazelzet. The output of the OR gate

would be coupled to, and would drive, the gate of an open drain transistor, which itself drives UE 121, as shown in the annotation below:



259. As in Hazelzet, UE 121 is coupled to an error edge connector.

260. As I note above, Hazelzet discloses that UE 121 is used in both Parity Mode and ECC Mode, so there is necessarily logic circuitry within Error Logic 100 for selecting which signal to use to drive the open drain output. Kim uses an OR gate for that function, as in this combination, but a multiplexor would have also worked. It would have been obvious and common sense to use a three input OR gate here, since there are three modes in the modified version of Hazelzet.

261. A Skilled Artisan would understand that, in this combination, each signal input the OR gate would remain low when the module was not in its associated mode, and the signal whose mode was active could be high to indicate the occurrence of the event to be signaled (error in Parity Mode or ECC Mode;

ongoing training in Training Mode), or low to indicate that the event is not occurring (Parity/ECC) or acknowledge/completed (training). The signal whose mode was active would then be passed through the OR gate to drive the gate of the transistor.

262. I note this is how both Hazelzet and JEDEC employ open drain signaling. For example, Hazelzet discloses that the “ECC/Parity register” (*i.e.*, “*module controller*,” as claimed) has “open drain output[s].” Ex. 1014 (Hazelzet) at ¶[0072]. Hazelzet further explains that the “ECC/Parity register” has an “error correction code circuit ECC segment 21b,” which is a “*notification circuit*,” as claimed, because it outputs signals notifying the system memory controller of correctable, uncorrectable, and parity errors. Ex. 1014 (Hazelzet) at ¶[0044]. Such “error correction code circuit ECC segment 21b” (within the “ECC/Parity register”) includes the circuitry for determining whether the errors occurred, SEC/DED ECC circuit 90, and error logic circuit 100 that receives error signals from SEC/DED ECC circuit 90, such as UE 110 and PERR 111, and provides the above-mentioned “open-drain output(s),” such as UE 121. Ex. 1014 (Hazelzet) at FIG 4B, ¶¶[0059],[0072]. Hazelzet discloses that those “open-drain outputs are available to permit multiple modules to share a common signal line for reporting an error,” and further discloses that the “outputs are driven low for two clocks to allow the memory controller time to sense the error. ... /Error (UE) indicates that

an uncorrectable error occurred and depending on the mode selected is an uncorrectable ECC error or a parity error.”). Further, Hazelzet explains that its open-drain output is driven “low” (i.e., to ground) when the driver is enabled (i.e., gate receives a high voltage), and further explains that the open-drain “output [is] permitted to return to an un-driven state (high impedance)” when the “driver [is] disabled.” Ex. 1014 (Hazelzet) at ¶[0099] (“Parity error reporting in the present invention is realized by delivering the parity signal one cycle after the address and command to which it applies, and driving the error line low, i.e., ‘0’ two clock cycles after the address and command bits are driven to the DRAMs from the memory interface chip if an error is detected. After holding the error line low for only 2 clock cycles, the driver will be disabled and the output permitted to return to an un-driven state (high impedance) allowing this line to be shared by multiple modules.”).

263. Based upon these disclosures, a Skilled Artisan would have understood Hazelzet’s open drain outputs to necessarily driven by a field effect transistor (as opposed to an open collector configuration), that field effect transistors have three terminals, i.e., gate, source, and drain, that the drain would be connected to a pull-up resistor, the source to ground and the gate to an OR logic element that OR’ed the UE 110 and PERR 111 error signals to drive the gate, as depicted in Figure 5 of Kim. EX1017, FIGs. 4-5, 5:65-6:18.

264. Also, as explained above, see ¶163, a Skilled Artisan would have understood that an open drain output as set forth in the figure above would be pulled to a high logic level when the gate of the transistor is low, because the transistor would be off. See, e.g., Ex. 1017 (Kim) at FIG. 4. The output would then be in an un-driven, high impedance, state. Ex. 1014 (Hazelzet) at ¶[0099]. On the other hand, the open drain output would switch to a low logic level (e.g., ground), and be put in a low impedance state, when the gate of the transistor is high, because the transistor would be on. *Id.*

265. In this combination, as shown in the annotated figure above, the module controller would therefore include “*a notification circuit comprising a transistor having an open drain coupled to the open drain output and source coupled to the ground.*”

266. A Skilled Artisan would have been motivated to combine Kim into the obviousness combination of Hazelzet and JEDEC or Buchmann for various reasons. Kim was filed approximately a year and a half after Hazelzet and includes some of the same disclosures. It discloses additional details regarding the use of an open-drain output on a memory module to notify the memory controller of errors during a parity normal operating mode and during an ECC normal operating mode. EX1017(Kim) at 1:16-22;5:49-57;6:8-16. To use the output-pin scheme of Kim in the system of Hazelzet would therefore have been only the use of known

techniques for their known purposes to achieve predictable results, *i.e.*, using an open-drain output to provide error or status information from multiple components.

267. Kim and Hazelzet/JEDEC/Buchmann are analogous art to the 595 Patent because each is directed to the field of memory module design, including error detection and correction, initialization, training and the use of pins/paths for multiple purposes during different operations/modes, EX1001, Abstract, 5:66-6:14;8:4-48; EX1014, Abstract, ¶¶[0007],[0069]-[0070],[0123]; EX1015, 1, 3, 8; EX1016, 1:7-9;3:49-60;4:51-5:50;12:60-13:41;14:1-63;20:20-21:19;33:45-67; EX1017, 1:16-22;5:49-57;6:8-18;11:20-34;12:36-53, and also because Kim and Hazelzet/JEDEC/Buchmann are reasonably pertinent to the particular problem the inventor of the 595 Patent was trying to solve, increasing memory module capacity, performance, and/or reliability by sharing an output pin/path to perform multiple functions during multiple operations/modes, including initialization/training, EX1001, Abstract, 5:66-6:14;8:4-48; EX1014, Abstract, ¶¶[0007],[0069]-[0070],[0123]; EX1015, 1, 3, 8; EX1016, 1:7-9;3:49-60;4:51-5:50;12:60-13:41;14:1-63;20:20-21:19;33:45-67; EX1017, 1:16-22;5:49-57;6:8-18;11:20-34;12:36-53.

268. Moreover, a person of ordinary skill in the art would have been motivated to use the open-drain output pin reporting technique of Kim in the combined scheme of Hazelzet and JEDEC or Buchmann because it represented a

well-known (and therefore reliable) and simple technique to provide error and/or status information from a number of memory components. *See, e.g.*, Ex. 1014 (Hazelzet) at ¶[0072], ¶[0122]; EX1017, FIGs. 4-5, 5:65-6:18, 12:18-23. The open-drain interrupt reporting technique of Kim permitted a single signal line with an “OR logic element” to indicate error or status information, thus simplifying the design of the system and saving pins on the various integrated circuits connected to the bus, which necessarily can have only a finite number of pins. Thus, a person of ordinary skill in the art could readily have modified Hazelzet’s open-drain output with the teachings of Kim and would have been motivated to do so.

269. Accordingly, claim 3 would have been obvious in view of Hazelzet, JEDEC or Buchmann, with or without Kim.

270. This same analysis applies to further combining Hazelzet and JEDEC or Buchmann, with Kim to satisfy the elements of claims 4-7, 12-14, 20, 22, or 23, each of which adds limitations going to details of the implementation of the open-drain output disclosed by Hazelzet, details that Kim explicitly discloses are included as part of an open-drain output circuit. I thus cross-reference this analysis for each of those claims.

4. Claim 4 is Unpatentable

271. Claim 4 requires “[t]he memory module of claim 3, wherein the module controller is configurable to drive a gate of the transistor high so as to

drive open drain output and the error edge connection to ground, or to drive the gate of the transistor low so as to drive the open drain output and the error edge connection to the high impedance state.”

272. As demonstrated above, in the combinations analyzed here the open drain output is configured such that the transistor output is driven low (ground) while training is still occurring and driven high upon completion. Moreover, to drive the output low (i.e., ground), the gate of the transistor must be high, causing the transistor to conduct and connect the drain to ground. Conversely, to drive the output high (which would be a high impedance state), the gate of the transistor must be low, turning the transistor off. See ¶168.

273. Similarly Hazelzet explains that its open-drain output is driven “low” (i.e., to ground) when the driver is enabled (i.e., gate receives a high voltage), and further explains that the open-drain “output [is] permitted to return to an un-driven state (high impedance)” when the “driver [is] disabled.” Ex. 1014 (Hazelzet) at ¶[0099] (“Parity error reporting in the present invention is realized by delivering the parity signal one cycle after the address and command to which it applies, and driving the error line low, i.e., ‘0’ two clock cycles after the address and command bits are driven to the DRAMs from the memory interface chip if an error is detected. After holding the error line low for only 2 clock cycles, the driver will be disabled and the output permitted to return to an un-driven state (high impedance)

allowing this line to be shared by multiple modules.”). Accordingly, a Skilled Artisan would have understood that the known open-drain output for such a system, such as disclosed in Kim, was used in Hazelzet, see ¶¶161–163, *above*, and that Hazelzet’s open drain output would be left floating (*i.e.*, high impedance state) when the gate of the transistor is low, because the transistor would be off. Ex. 1014 (Hazelzet) at ¶[0099]; see ¶¶161–163, *above* ; Ex. 1017 (Kim) at FIG. 4. On the other hand, Hazelzet’s open drain output would switch to a low logic level (*e.g.*, ground) when the gate of the transistor is high, because the transistor would be on. *Id.* See ¶¶158–163.

274. Accordingly, one skilled in the art would have known that the open drain output along with the edge connection connected to the open drain output would both be driven to ground when the gate is driven high. See analysis in claim element [1.g.] and claim 3; Ex. 1014 (Hazelzet) at ¶[0099]; see ¶¶158–163; see *also* Ex. 1017 (Kim) at FIGs. 4-5, 5:65-6:18. Likewise, one skilled in the art knew that the open drain output along with the edge connection connected to the open drain output would both be driven to a high impedance state (through the pull up resistor) when the gate is driven low. *Id.*

275. The obvious combinations of Hazelzet and JEDEC or Buchmann therefore satisfy “*the module controller is configurable to drive a gate of the transistor high so as to drive open drain output and the error edge connection to*

ground, or to drive the gate of the transistor low so as to drive the open drain output and the error edge connection to the high impedance state” limitation.

276. To the extent one might argue otherwise, the module controller of the obvious combination of Hazelzet, JEDEC or Buchmann, and Kim, described above, includes a memory module configurable “*to drive a gate of the transistor high so as to drive open drain output and the error edge connection to ground, or to drive the gate of the transistor low so as to drive the open drain output and the error edge connection to the high impedance state*” for the reasons set forth in ¶¶261–264 above.

5. Claim 5 is Unpatentable

277. Claim 5 requires “[t]he memory module of claim 4, wherein the module controller is configurable to output the signal indicating a parity error having occurred by driving the gate of the transistor high to provide a low impedance path between the open drain output and the ground.”

278. As explained in claim element [1.f.], see ¶¶235–240, above, Hazelzet explains that its “ECC/Parity register” (i.e., “module controller”) has “open-drain output[s]” (i.e., Uncorrectable Error (UE) line[s])” capable of utilizing “parity error signals” (PERR) to output signal UE 121 to the host indicating a parity error. See analysis in claim element [1.f.]; EX1014, ¶¶[0059],[0070],[0072], [0076]. Further, as explained in claim element [1.f.], when the memory module is in the “parity

mode” (i.e., “*first mode*,” as claimed), the “parity generator/checker circuit 231” (within SEC/DED ECC circuit 90) generates and sends the “parity error signal (PERR)” to the “error logic circuit” 100. Ex. 1014 (Hazelzet) at FIGs. 4B-5, ¶¶[0059],[0070],[0072],[0076] (“FIG. 5 is a block diagram of the SEC/DED ECC circuit of FIG. 4B. ... The parity generator/checker circuit 231 further has a second input coupled to the parity in signal source 31 via primary latch 71 and output line 81 and depending on the state of the parity input signal on input 31 sends a parity error signal (PERR) on output line 111 to the error logic circuit 100.”).

279. In particular, Hazelzet explains that in the “parity mode,” the parity error “will be reported two clock pulses later via the Uncorrectable Error (UE) line (driven low for two clock pulses).” Ex. 1014 (Hazelzet) at ¶[0070]; *see also id.* at [0018] (“After holding the error line low for only 2 clock cycles, the driver can be disabled and the output permitted to return to an un-driven state (high impedance) thus allowing this line to be shared by multiple modules.”).

280. Further, as explained in claim 4, *see* ¶272, *above*, Hazelzet discloses that its open-drain output is driven “low” (i.e., to ground) when the driver is enabled (i.e., gate receives a high voltage), and further explains that the open-drain “output [is] permitted to return to an un-driven state (high impedance)” when the “driver [is] disabled.” Ex. 1014 (Hazelzet) at ¶[0099] (“Parity error reporting in the present invention is realized by delivering the parity signal one cycle after the

address and command to which it applies, and driving the error line low, i.e., ‘0’ two clock cycles after the address and command bits are driven to the DRAMs from the memory interface chip if an error is detected. After holding the error line low for only 2 clock cycles, the driver will be disabled and the output permitted to return to an un-driven state (high impedance) allowing this line to be shared by multiple modules.”).

281. Accordingly, Hazelzet discloses that the open-drain output (UE 121) in each memory module is configured to “*output the signal indicating a parity error having occurred by driving the gate of the transistor high to provide a low impedance path between the open drain output and the ground.*” See also analysis in claim 4; EX1017, FIGs. 4-5, 5:65-6:18; see ¶¶158–163, above.

282. The obvious combinations of Hazelzet and JEDEC or Buchmann therefore satisfy the “*wherein the module controller is configurable to output the signal indicating a parity error having occurred by driving the gate of the transistor high to provide a low impedance path between the open drain output and the ground*” limitation.

283. To the extent one might argue otherwise, the module controller of the obvious combination of Hazelzet, JEDEC or Buchmann, and Kim, described above, includes a memory module configurable “*to output the signal indicating a parity error having occurred by driving the gate of the transistor high to provide a*

low impedance path between the open drain output and the ground,” for the reasons set forth in ¶¶261–264 above. In particular, the module is “configurable” to output the parity error as claimed because it can be configured to be in the Parity Mode.

6. Claim 6 is Unpatentable

284. Claim 6 requires”[t]he memory module of claim 3, wherein the notification circuit further includes a multiplexor or a logic circuit having a output coupled to a gate of the transistor and configurable to drive the gate of the transistor with either a first signal related to the parity error or a second signal related to the one or more training sequences.”

285. As explained in claim 3, Hazelzet’s “error correction code circuit ECC segment 21b” (within the “ECC/Parity register”) is the “notification circuit,” as claimed. See ¶252, above.

286. FIG. 4B of Hazelzet shows the “error correction code circuit segment 21b.” Ex. 1014 (Hazelzet) at ¶[0044],[0059], FIG. 4B. Within Hazelzet’s error correction code circuit ECC segment 21b is “Error Logic 100.” *Id.* Hazelzet discloses that Error Logic 100 receives the “US [sic] 110” signal and the “PERR 111” signal, and outputs one of these signals to the same “/ERROR (UE)” pin depending on which mode the memory module is in. See Ex. 1014 (Hazelzet) at FIG. 4B (showing an open-drain output “/ERROR (UE) 121” for uncorrectable

error or parity error, depending on the mode of operation), ¶¶[0072] (explaining that “/Error (UE) indicates that an uncorrectable error occurred and depending on the mode selected is an uncorrectable ECC error or a parity error.”), ¶¶[0044],[0059],[0069-71]. As set forth above, see ¶¶162, 167, in the combinations analyzed here, that circuitry would be modified to implement the additional training mode, in which the UE 121 open drain output would, when the module is in the training mode, be used to send the notification/status signals identified above.

287. Hazelzet also discloses that UE 121 is an open drain output, EX1014, [0072], which a Skilled Artisan would necessarily understand is driven by a transistor in an open drain configuration. EX1017, FIGs. 4-5, 5:65-6:18 (depicting in FIG. 5 OR logic gate used for such purpose); see ¶¶158–163, *above*. A Skilled Artisan would understand that such a transistor necessarily has “*a gate*” that can be driven to assert the open drain output. *Id.*

288. Because in the combinations analyzed here, Error Logic 100 receives both “US [sic] 110” signal and the “PERR 111” signal and the training mode notification signals, but uses only one such signal to drive the UE 121 output, depending on mode, a Skilled Artisan would understand that Error Logic 100 would necessarily include logic circuitry (in addition to the open drain transistor) to determine which signal should be used to drive the transistor. EX1017, FIGs. 45,

5:65-6:18 (depicting in FIG. 5 OR logic gate used for such purpose). That additional logic circuitry is the “*logic circuit*,” and necessarily has “*an output coupled to a gate of the transistor*” because that is how a transistor in an open drain configuration is driven (*i.e.*, by a signal driving the gate, *see* EX1017, FIGs. 4-5, 5:65-6:18 (depicting in FIG. 5 OR logic gate used for such purpose); *see* ¶¶158–163, *above*. Moreover, the signal driving that gate is necessarily related to one of the signals input to Error Logic 100 (*e.g.*, “PERR 111” (“*first signal*”) or the training notification signals (“*second signal*”), depending on mode, so the additional logic circuitry is “*configurable to drive the gate of the transistor with either a first signal related to the parity error or a second signal related to the one or more training sequences.*”

289. The obvious combinations of Hazelzet and JEDEC or Buchmann therefore satisfy the “wherein the notification circuit further includes a multiplexor or a logic circuit having a output coupled to a gate of the transistor and configurable to drive the gate of the transistor with either a first signal related to the parity error or a second signal related to the one or more training sequences” limitation.

290. To the extent one might argue otherwise, the notification circuit of the obvious combination of Hazelzet, JEDEC or Buchmann, and Kim, described above, includes “*a multiplexor or a logic circuit having a output coupled to a gate*

of the transistor and configurable to drive the gate of the transistor with either a first signal related to the parity error or a second signal related to the one or more training sequences,” for the reasons set forth in ¶¶258–264 above. In particular, the circuit is “*configurable*” in this manner because it be placed in either the Parity Mode or the Training Mode.

7. Claim 7 is Unpatentable

291. Claim 7 requires “[t]he memory module of claim 3, wherein the module controller is configurable to provide the information related to the one or more training sequences by driving a gate of the transistor with the second signal so as to drive the open drain output from the high impedance state to ground or from ground to the high impedance state.”

292. As demonstrated above, in the combinations analyzed here the open drain output is configured such that the transistor output is driven low (ground) while training is still occurring and driven high upon completion. Moreover, to drive the output low (i.e., ground), the signal at the gate of the transistor (“*the second signal*” when the system is in training mode) must be high, causing the transistor to conduct and connect the drain to ground. On the other hand, to drive the output high (which would be a high impedance state), the gate of the transistor must be low, turning the transistor off. See ¶¶168, 272–274.

293. As explained in claim element [1.g.] and claims 4-6, in either obvious combination of Hazelzet and JEDEC or Buchmann, the open drain signals would be low logic levels (*i.e.*, the logic levels of the open drain output driven low, because the logic level of the gate would be driven high) in the second mode to indicate the training operations (*e.g.*, MB-DRAM/TS0 or TS3) was in progress, and at a high impedance (*i.e.*, the logic level of the open drain output driven high, because the logic level of the gate would be driven low) when that operations completed in each memory module. See ¶¶246, 274, 281, 288, 158–160, *above*.

294. The application of a high signal to the gate of the transistor (which indicates that the training sequence is in progress) is the claimed “*second signal so as to drive the open drain output from the high impedance state to ground*” (*i.e.*, a low logic level). *Id.* The application of a low signal to the gate of the transistor (which indicates the completion of the training sequence) is the claimed “*second signal so as to drive the open drain output ... from ground to the high impedance state.*” *Id.*

295. The obvious combinations of Hazelzet and JEDEC or Buchmann therefore satisfy the “wherein the module controller is configurable to provide the information related to the one or more training sequences by driving a gate of the transistor with the second signal so as to drive the open drain output from the high impedance state to ground or from ground to the high impedance state” limitation.

296. To the extent one might argue otherwise, the notification circuit of the obvious combination of Hazelzet, JEDEC or Buchmann, and Kim, described above, includes “*wherein the module controller is configurable to provide the information related to the one or more training sequences by driving a gate of the transistor with the second signal so as to drive the open drain output from the high impedance state to ground or from ground to the high impedance state,*” for the reasons set forth in ¶¶258–264 above. In particular, the circuit is “*configurable*” in this manner because it can be placed in the Training Mode, and thereby drive the gate of the transistor with the training status signal.

8. Claim 8 is Unpatentable

297. Claim 8 requires “[*t*]he memory module of claim 1, wherein the second edge connections include one or more pins that are not active while the memory module is in the second mode.”

298. As explained in claim element [1.b.], Hazelzet discloses a second set of edge connections for communicating address and control signals from the memory controller of the host system. Ex. 1014 (Hazelzet) at FIGs 7A-7C (showing address edge connections including pins 67, 70, 72-75, 82, 205-207, 210-213, 220, 227 and command edge connections including pins 86, 89, 91, 93), ¶[0072] (referring to “/CS” as commands), ¶[0068] (listing various control signals including “chip select (CS), address (Addr), row address strobe (RAS), column

address strobe (CAS) and write enable (WE)” signals); *see also* Ex. 1014 (Hazelzet) at ¶[0038] (“The memory interface chip 18 then sends and receives data, via line 15, to the memory devices or DRAMs 22 and sends address and command information to the register chip 21 via add/cmd line 16 and check bits for error correction purposes to the ECC/ Parity register chip 21 via line 25.”), FIG. 2 (showing address and command line 16); *see* ¶¶196–201, *above*.

299. In the JEDEC combination analyzed here, JEDEC discloses that during the MB-DRAM training (i.e., the mode that is added to Hazelzet here), “[n]o DRAM commands or control word writes (either over the Command/Address and Control buses or via SMBus) can be issued to the MB until the MB-DRAM Interface training is complete and the DODTn inputs must be kept low.” EX1015, 8. A Skilled Artisan would understand from this that during such training the address/control pins (including the high order address/control pins) would remain inactive as those are pins used to provide “DRAM commands or control word writes,” and no data signals would be communicated on the data pins. *Id.*

300. Similarly, in a Buchmann combination analyzed here, in which only the TS0 training operations are carried out in the training mode (“*second mode*”), one or more of the pins of these edge connections would not be active during that training because TS0 training involves training of the “clock” itself, so a Skilled

Artisan would have understood that no “address” or control signals (including to/from the high order address/control pins) are transmitted between the host and the memory module during TS0 training. Ex. 1016 (Buchmann) at 5:51-7:2.

301. To the extent Patent Owner argues otherwise, a Skilled Artisan would have found it obvious at least not to send any data, control or address signals while the clock is being trained for the same reasons set forth above. For example, a Skilled Artisan would have been motivated to keep the pin(s) for address, control and data inactive to conserve power and/or avoid unreliable operation during periods that the clock may be unstable.

302. Moreover, I understand that a negative limitation is satisfied by silence in the prior art. *Süd-Chemie, Inc. v. Multisorb Technologies, Inc.*, 554 F.3d 1001, 1004-05 (Fed. Cir. 2009). I understand that this claim includes a negative limitation, because it requires “*not active*.” Neither Hazelzet nor JEDEC or Buchmann disclose pins in the second edge connections being inactive while the memory module is in the training modes during initialization/power-on.

303. The obvious combinations of Hazelzet and JEDEC or Buchmann therefore satisfy the “wherein the second edge connections include one or more pins that are not active while the memory module is in the second mode” limitation.

9. Claim 9 is Unpatentable

304. Claim 9 requires “[t]he memory module of claim 1, wherein the memory module in the second mode is configurable to perform the operations *related to the one or more training sequences without communicating data signals via the first edge connections while the memory module is in the second mode.*”

305. According to claim element [1.b.], the “*first edge connections*” are connections “*via which the memory module receives or outputs data signals*” from/to the host. See ¶199, above.

306. In the JEDEC combination analyzed here, JEDEC discloses that during the MB-DRAM training (i.e., the mode that is added to Hazelzet here), “[n]o DRAM commands or control word writes (either over the Command/Address and Control buses or via SMBus) can be issued to the MB until the MB-DRAM Interface training is complete and the DODTn inputs must be kept low.” EX1015, 8. A Skilled Artisan would understand from this that during such training the address/control pins (including the high order address/control pins) would remain inactive as those are pins used to provide “DRAM commands or control word writes,” and no data signals would be communicated on the data pins. *Id.*

307. Similarly, in the obvious combination of Hazelzet and Buchmann, the memory module can execute a training sequence (*e.g.*, TS0 training, which

involves training of the “clock”) in the SBC mode. Ex. 1016 (Buchmann) at 5:51-7:2; *see also* analysis in claim 1. Because this training involves training of the “clock” itself, a Skilled Artisan would have understood that there are no “data” signals being transmitted between the host and the memory module during the TS0 training.

308. To the extent Patent Owner argues otherwise, a Skilled Artisan would have found it at least obvious not to send any data, control or address signals while the clock is being trained for the same reasons set forth above. For example, a Skilled Artisan would have been motivated to keep the pin(s) for address, control and data inactive to conserve power and/or avoid unreliable operation during periods that the clock may be unstable.

309. Moreover, I understand that a negative limitation is satisfied by silence in the prior art. *Süd-Chemie, Inc. v. Multisorb Technologies, Inc.*, 554 F.3d 1001, 1004-05 (Fed. Cir. 2009). I understand that this claim includes a negative limitation, because it requires “*without communicating data signals.*” Neither Hazelzet nor JEDEC or Buchmann disclose communicating data signals while the memory module is in the training mode for the MB-DRAM or TS0 training during initialization/power-on.

310. Accordingly, the obvious combinations of Hazelzet and JEDEC or Buchmann satisfy the “*wherein the memory module in the second mode is*

configurable to perform the operations related to the one or more training sequences without communicating data signals via the first edge connections while the memory module is in the second mode” limitation.

10. Claim 10 is Unpatentable

h) [10.a] Preamble

311. The preamble of claim 10 requires “[a] memory module operable with a memory controller of a host system, comprising.”

312. This limitation is satisfied for the same reasons set forth for claim element [1.a.]. See ¶¶192–194, *above*.

i) [10.b] Printed Circuit Board Having Edge Connections

313. Claim 10 requires “a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections.”

314. This limitation is satisfied for the same reasons set forth for claim element [1.b.]. See ¶¶195–202, *above*.

j) [10.c] Dynamic Random Access Memory Elements

315. Claim 10 requires “*dynamic random access memory elements on the printed circuit board.*”

316. This limitation is satisfied for the same reasons set forth for claim element [1.c.]. See ¶¶203–205, *above*.

k) [10.d] Module Controller ... Having An Open Drain Output

317. Claim 10 requires “*a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection and configurable to drive the open drain output from a first state to a second state and from the second state to the first state, one of the first state and the second state being a low logic level, and the other one of the first state and the second state being a high impedance state.*”

318. This limitation is satisfied for the same reasons set forth for claim elements [1.d.] and [1.g.]. See ¶¶206–211, 242–247, *above*.

319. While claim element [1.g.] requires the module controller to be “configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection **to a first state or to a second state**, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state,” claim element [10.d.] requires the module controller to be “configurable to

drive the open drain output **from a first state to a second state and from the second state to the first state**, one of the first state and the second state being a low logic level, and the other one of the first state and the second state being a high impedance state.”

320. This additional language in claim element [10.d.] is similar to claim 7 and satisfied in the obvious combinations of Hazelzet and JEDEC or Buchmann for similar reasons. In particular, as explained in claim element [1.g.] and claim 7, in either obvious combination of Hazelzet and JEDEC or Buchmann, the open drain signals would be low logic levels (*i.e.*, the logic levels of the open drain output changes from a high impedance state to a low state, because the gate of the transistor changes from a low to a high) to indicate the training sequence (*e.g.*, MB-DRAM/TS0 or TS3) was in progress. On the other hand, the open drain signals would be at a high-impedance (*i.e.*, the logic level of the open drain output changes from a low state to a high impedance state, because the gate of the transistor changes from a high to a low) when that sequence completed in all memory modules. EX1014, FIGs. 4B-5, ¶¶[0059],[0070], [0072],[0076]; EX1017, FIGs. 4-5, 5:65-6:18; Ex. 1016 (Buchmann) at 5:51-7:2, Table 1, Table 2, FIG. 4, 8:24-9:18, Table 5, Table 6, FIG. 6, 8:24-9:17, 3:52-54, 27:18-21, 26:30-32; *see also* ¶¶158–163, *above*.

l) [10.e] Operable In At Least A First Mode And A Second Mode

321. Claim 10 requires “wherein the memory module is operable in at least a first mode in which the memory module is configurable to perform one or more *memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, and a second mode in which the memory module is not accessed by the memory controller for memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences without communicating data signals via the first edge connections.*”

322. This limitation is satisfied for the same reasons set forth for claim element [1.e.] and claim 9. See ¶¶212–230, 304–310, *above*.

323. While claim element [1.e.] requires that “the memory module in the second mode is not accessed by the memory controller for **normal memory read or write operations**, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences” and claim 9 requires a “second mode [that] is configurable to perform the operations related to the one or more training sequences **without communicating data signals via the first edge connections** while the memory module is in the second mode,” claim element [10.e.] requires “a second mode in which the memory module is not accessed by the memory controller for **memory read or write**

operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences **without communicating data signals via the first edge connections.**” As demonstrated above, ¶¶110–125, those phrases should be interpreted to mean the same thing and, regardless, in the combinations analyzed, the “memory module is not accessed **by the memory controller** for memory read or write operations” during MB-DRAM Training, TS0 training or TS3 training because in none of those sequences does the memory controller communicate data with the module or seek to read or write to the memory devices. The analysis of claim element [1.e.] and claim 9 therefore satisfies this claim element.

m) [10.f] Operation Of Module Controller In The First Mode

324. Claim 10 requires “*wherein the module controller in the first mode is configurable to receive via the second edge connections the address and control signals associated with the one or more memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller in the first mode is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred in the memory module while the memory module is in the first mode.*”

325. This limitation is satisfied for the same reasons set for in claim element [1.f.]. See ¶¶231–241, *above*.

n) [10.g] Operation Of Module Controller In The Second Mode

326. Claim 10 requires “*wherein the module controller in the second mode is further configurable to output to the memory controller open-drain signals related to the one or more training sequences via the open drain output and the error edge connection while the memory module is in the second mode.*”

327. This limitation is satisfied for the same reasons set for in claim element [1.g.]. See ¶¶242–247, *above*.

11. Claim 11 is Unpatentable

328. Claim 11 requires “[*t*]he memory module of claim 10, wherein the module controller comprises an integrated circuit.”

329. This claim is satisfied for the same reasons set for in claim 2. See ¶¶248–250, *above*.

12. Claim 12 is Unpatentable

330. Claim 12 requires “[*t*]he memory module of claim 10, wherein the module controller includes a notification circuit having a transistor with an open drain coupled to the open drain output and a source coupled to the ground, wherein the module controller is configurable to output to the memory controller the open-drain signals related to the one or more training sequences by driving a

gate of the transistor high so as to drive the open drain output and the error edge connection to ground, and by driving the gate of the transistor low as to drive the open drain output and the error edge connection to the high impedance state, and wherein the notification circuit is configurable to output the signal indicating a parity error having occurred by driving the gate of the transistor high to provide a low impedance path between the open drain output and ground.”

331. This claim is satisfied for the same reasons set forth for claims 3, 4 and 5. In particular, the analysis for claim 3 satisfies claim element [12.a.], see ¶¶251–270, *above*, the analysis for claim 4 satisfies claim element [12.b.], see ¶¶271–275, and the analysis for claim 5 satisfies claim element [12.c.]. See ¶¶277–282. In an abundance of caution, I note that this includes the alternative obviousness combinations of Hazelzet and JEDEC or Buchmann, in further view of Kim, as explained in Section V.A.3 above, ¶¶256–270.

13. Claim 13 is Unpatentable

332. Claim 13 requires “[t]he memory module of claim 12, wherein the notification circuit further includes a multiplexor or a logic circuit having an output coupled to the gate of the transistor and configurable to drive the transistor with either a first signal related to the parity error or a second signal related to the one or more training sequences.”

333. This claim is satisfied or rendered obvious in further combination with Kim for the same reasons set forth for claims 3 and 6. See ¶¶251–270, 284–289, *above*. In an abundance of caution, I note that this includes the alternative obviousness combinations of Hazelzet and JEDEC or Buchmann, in further view of Kim, as explained in Section V.A.3 above, ¶¶256–270.

14. Claim 14 is Unpatentable

334. Claim 14 requires “[t]he memory module of claim 10, wherein the module controller is configurable to output the open-drain signals related to the one or more training sequences by driving the open drain output from the high impedance state to the low logic level or from the low logic level to the high impedance state.”

335. This claim is satisfied or rendered obvious in further combination with Kim for the same reasons set forth for claims 3 and 7. See ¶¶251–270, 291–295, *above*. In an abundance of caution, I note that this includes the alternative obviousness combinations of Hazelzet and JEDEC or Buchmann, in further view of Kim, as explained in Section V.A.3 above, ¶¶256–270.

15. Claim 15 is Unpatentable

336. Claim 15 requires “[t]he memory module of claim 10, wherein the second edge connections include one or more pins that are not active while the memory module is in the second mode.”

337. This claim is satisfied for the same reasons set forth for claim 8. See ¶¶297–303, *above*.

16. Claim 16 is Unpatentable

338. Claim 16 requires “[t]he memory module of claim 10, wherein the second edge connections include one or more high-order address pins that are not active while the memory module is in the second mode.”

339. This claim element is satisfied for the same reasons I set forth above for claim 8 where I addressed the additional limitation regarding “one or more high-order address pins that are not active” when conducting my claim 8 analysis. See ¶¶297–303, *above*.

17. Claim 17 is Unpatentable

o) [17.a] Preamble

340. The preamble of claim 17 requires “[a] method, comprising”:

341. This limitation is satisfied, because Hazelzet and JEDEC or Buchmann disclose corresponding methods in connection with the operation of the apparatus (analyzed in connection with claim 1). See ¶¶192–194, *above*.

p) [17.b] Printed Circuit Board Having Edge Connections & Dynamic Random Access Memory Elements

342. Claim 17 requires “at a memory module coupled with a memory controller of a host system, the memory module including a printed circuit board having edge connections that fit into a corresponding slot of the host system so as

to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections, the memory module further including dynamic random access memory elements on the printed circuit board.”

343. This limitation is satisfied for the same reasons set forth for claim elements [1.a.], [1.b.] and [1.c.]. See ¶¶192–205, *above*.

q) [17.c] Memory Read or Write Operations

344. Claim 17 requires “*receiving via the second edge connections address and control signals associated with one or more memory read or write operations; controlling the dynamic random access memory elements to communicate data signals corresponding to the one or more memory read or write operations via the first edge connections in response to the address and control signals; outputting via an open drain output coupled to the error edge connection a signal indicating a parity error having occurred in the memory module while the memory module is being accessed by the memory controller for a memory read or write operation.*”

345. This limitation is satisfied for the same reasons set forth for claim elements [1.e.] and [1.f.]. Specifically, as explained there, Hazelzet discloses

normal memory operations that were known to entail the module receiving address and control signals from a system memory controller via the respective address and control edge connections, and in response communicating data between the system memory controller and the module DRAMs via the data edge connections and under the control of the module controller. See ¶214, *above*. Also as explained above, Hazelzet discloses the module outputting, in the “*first mode*,” a parity error signal via an open drain output (UE 121) in connection with memory read and write operations accessing the module. See ¶¶212–241, *above*.

r) [17.d] Operations Related To Training Sequences

346. Claim 17 requires “*performing operations related to one or more training sequences while the memory module is not accessed by the memory controller for memory read or write operations; and outputting to the memory controller via the open drain output and the error edge connection open-drain signals related to the one or more training sequences and unrelated to any memory read or write operation.*”

347. This limitation is satisfied for the same reasons set forth for claim elements [1.e.] and [1.g.]. Specifically, as demonstrated above, the combinations analyzed here includes a module that performs training sequence operations unrelated to memory read or write operations in response to commands from the memory controller. See ¶¶231–241 *above*. Similarly, as explained in claim

elements [1.e] and [1.g.], the module of the combined system outputs to the system memory controller training notification signals (*e.g.*, ERROUT#, TS0_done, TS3_ack, TS3_done) via an open drain output (UE 121), *see* ¶243, *above*, which notification signals are related solely to the JEDEC or Buchmann training sequences (respectively) and not to any memory controller operations that seek to communicate data with the module or seek to read or write to the memory devices, *see* ¶¶164, 180, 229, *above*.

18. Claim 18 is Unpatentable

348. Claim 18 requires “[*t*]he method of claim 17, wherein the second edge connections include one or more pins that are not active while the memory module is trained with the one or more training sequences.”

349. This claim is satisfied for the same reasons set forth for claims 1 and 8. *See* ¶¶242–247, 297–303, *above*.

19. Claim 19 is Unpatentable

350. Claim 19 requires “[*t*]he method of claim 18, wherein the second edge connections include one or more high-order address pins that are not active while the memory module is trained with the one or more training sequences.”

351. This claim is satisfied for the same reasons set forth for claims 1, 10, and 16. *See* ¶¶242–247, 327, 339, *above*.

20. Claim 20 is Unpatentable

352. Claim 20 requires “[t]he method of claim 17, wherein the memory module includes a notification circuit having a transistor with an open drain coupled to the open drain output and a source coupled to ground, wherein *outputting via an open drain output coupled to the error edge connection a signal indicating a parity error having occurred in the memory module comprises driving a gate of the transistor high to provide a low impedance path between the open drain output and ground, and wherein outputting the open-drain signals related to the one or more training sequences and unrelated to any memory read or write operation comprises driving the gate of the transistor to drive the open drain output from a high impedance state to ground and from ground to the high impedance state.*”

353. This claim is satisfied for the same reasons set forth for claims 3, 4, 5. The analysis for claim 3 satisfies claim element [20.a.], the analysis for claim 5 satisfies claim element [20.b.], and the analysis for claim 4 satisfies claim element [20.c.]. Moreover, as demonstrated above for claim element [1.g], in the combinations analyzed here, the open drain signals relating to the training sequences (*e.g.*, ERROUT#, TS0_done, TS3_ack, TS3_done) are “*unrelated to any memory read or write operation*” because they are related solely to the JEDEC or Buchmann training sequences and not to any memory read or write operations,

including because there are no memory read or write operations in response to commands from the memory controller during the training mode analyzed here. See 233-237, 254-256 -257, 260-264, *above*. In an abundance of caution, I note that this includes the alternative obviousness combinations of Hazelzet and JEDEC or Buchmann, in further view of Kim, as explained in Section V.A.3 above, ¶¶256–270.

21. Claim 21 is Unpatentable

a) [21.a] Preamble

354. The preamble of claim 21 requires “[a] memory module operable with a memory controller of a host system, comprising.”

355. This limitation is satisfied for the same reasons set forth for claim element [1.a.]. See ¶¶192–194, *above*.

b) [21.b] Printed Circuit Board Having Edge Connections

356. Claim 21 requires “a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections.”

357. This limitation is satisfied for the same reasons set forth for claim element [1.b.]. See ¶¶195–202, *above*.

c) [21.c] Dynamic Random Access Memory Elements

358. Claim 21 requires “*dynamic random access memory elements on the printed circuit board.*”

359. This limitation is satisfied for the same reasons set forth for claim element [1.c.]. See ¶¶203–205, *above*.

d) [21.d] Module Controller Including A Transistor Having A Gate And An Open Drain Output

360. Claim 21 requires “*a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller including a transistor having a gate and an open drain output coupled to the error edge connection; wherein the module controller is configurable to drive the gate of the transistor so as to drive the open drain output to a first state or a second state, the first state being a low logic level and the second state being a high impedance state.*”

361. This limitation is satisfied for the same reasons set forth for claim elements [1.d.], and claims 3 and 4. Specifically, the combinations analyzed here satisfies “*a module controller on the printed circuit board and coupled to the dynamic random access memory elements*” for the reasons set forth for claim element [1.d.]. See ¶¶206–211 *above*. It satisfies “*the module controller including a transistor having a gate and an open drain output coupled to the error edge*

connection” for the reasons set forth for claim 3. See ¶¶251–270 above. And it satisfies “*wherein the module controller is configurable to drive the gate of the transistor so as to drive the open drain output to a first state or a second state, the first state being a low logic level [e.g., ground] and the second state being a high impedance state*” for the reasons set forth for claim 4. See ¶¶271–275 above.

e) [21.e] Normal Memory Read or Write Operations

362. Claim 21 requires “*wherein the module controller is configurable to receive via the second edge connections memory commands associated with normal memory read or write operations and to output a set of address and control signals for each of the normal memory read or write operations; wherein the dynamic random access memory elements are configurable to communicate one or more N-bit-wide data signals with the memory controller via the first edge connections in response to the set of address and control signals, where N is at least 32; wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred during any of the memory read or write operations by driving the open drain output and the error edge connection to the first state.*”

363. This limitation is satisfied for the same reasons set forth for claim elements [1.f.], with the following additional analysis. See ¶¶231–241, above.

364. As demonstrated above, Hazelzet discloses that the ECC/Parity register is configurable (*e.g.*, when placed in parity mode) to receive address command signals that a Skilled Artisan would understand to be associated with normal memory read and write operations (“*memory commands associated with normal memory read or write operations*”). See ¶214 above; see also EX1014, FIGs. 2, 7A-7B, ¶¶[0015],[0035],[0038], [0041],[0064],[0070]. Hazelzet further discloses that, in response to such commands, the ECC/Parity register outputs associated address and control signals to the DRAMs of the module. EX1014, [0042],[0075]. Hazelzet therefore discloses “*wherein the module controller is configurable to receive via the second edge connections memory commands associated with normal memory read or write operations and to output a set of address and control signals for each of the normal memory read or write operations.*”

365. To the extent one might argue that Hazelzet does not sufficiently disclose this claim element, it would have been obvious to include it in the combined system. In particular, Hazelzet discloses the ECC/Parity register receiving address and command information associated with memory commands. EX1014, FIGs. 2, 7A-7B, ¶¶[0015],[0038],[0041-42],[0064], [0070],[0075]. A Skilled Artisan would have been motivated to configure the register to correspondingly output associated address and control signals to the DRAMs, and

it would have been common sense to do so, because that would be necessary to carry out the memory operations and access the DRAMs.

366. As demonstrated above, Hazelzet discloses that the DRAMs of his module are configurable (*i.e.*, when connected to the address, control, data and PLL lines of the module, as described in Hazelzet, see EX1014, Fig. 2, to communicate data signals with the system memory controller over the disclosed edge connections in response to address and control signals. Moreover, Hazelzet discloses pinout information for one embodiment of his module, which includes 64 data lines (DQ0-DQ63), EX1014, FIGs. 7A-7C, which a Skilled Artisan would understand can communicate a 64-bit wide data signal. Alternatively, Hazelzet discloses a 72 bit wide (*i.e.*, $9 \times 8 = 72$) memory module Ex. 1014 (Hazelzet) at ¶[0092] (disclosing “an exemplary memory module having 9 eight bit wide or 18 four or eight bit wide memory devices and a single 4-rank enabled buffer chip 21.”). Hazelzet therefore discloses “*wherein the dynamic random access memory elements are configurable to communicate one or more N-bit-wide data signals with the memory controller via the first edge connections in response to the set of address and control signals, where N is at least 32.*”

367. To the extent Patent Owner argues that a single “dynamic random access memory element” must be able to “*communicate one or more N-bit-wide data signals ... where N is at least 32,*” to satisfy the limitation in claim element

[21.e.], this limitation would nevertheless have been obvious in the obvious combination of Hazelzet and Buchmann. In particular, while Hazelzet discloses using a memory module having “9 eight bit wide ... memory devices” as an example, Ex. 1014 (Hazelzet) at ¶[0092] (disclosing “an exemplary memory module having 9 eight bit wide or 18 four or eight bit wide memory devices and a single 4-rank enabled buffer chip 21.”), a Skilled Artisan would have understood that modifying the memory system to use SDRAMs with higher bit widths (*e.g.*, 32 bit wide) was not only known (or at least obvious), but also well within the skill of a Skilled Artisan by the effective filing date of the 595 Patent. *See, e.g.*, Ex. 1024 (JESD79) at page i. (“This comprehensive standard defines all required aspects of 64M x4/x8/x16 DDR SDRAMs, including features, functionality, AC and DC parametrics, packages and pin assignments. This scope will subsequently be expanded to formally apply to x32 devices, and higher density devices as well.”); Ex. 1029 (JESD209) at page 1 (demonstrating the prevalence of “x16 and x32 Low Power Double Data Rate SDRAM devices” by 2007); *see also* Ex. 1014 (Hazelzet) at ¶[0113] (disclosing embodiments with “LP RAM (Low Power DRAMs which are often based on the fundamental functions, features and/or interfaces found on related DRAMs.”).

368. Finally, as demonstrated above, the combinations analyzed here discloses “wherein the module controller is further configurable to output via the

open drain output and the error edge connection a signal indicating a parity error having occurred during any of the memory read or write operations by driving the open drain output and the error edge connection to the first state” for the reasons set forth above for claim element [1.f]. See ¶¶231–241, above. Additionally, as explained in claim element [1.e.], one skilled in the art would have understood Hazelzet’s parity mode to be a normal operating mode during which “*one or more normal memory read or write operations*” is/are performed. Ex. 1014 (Hazelzet) at ¶[0064] (“A parity operating mode is also provided, in conjunction with error reporting circuitry to permit the system to interrogate the device to determine the error condition.”), ¶[0103] (“A parity operating mode is also provided, in conjunction with error reporting circuitry to permit the system to interrogate the device to determine the error condition.”); *see also id.* at ¶[0020] (“Still further the present invention permits operation of the memory module in parity mode, such that unused ECC check bit inputs are held at a low level thus ensuring that these inputs are at a known and quiescent state.”); ¶[0072] (“Error reporting circuitry is included to permit external monitoring of DIMM operation.”); ¶[0070] (“In addition to the above ECC mode, the same twenty two chip select gated data signals can be operated in parity mode (/ECC Mode high), whereby the signal received on CHK0/Parity in line is received as parity to the register one clock pulse later than the chip select gated data inputs. The received parity bit is then compared

to the parity calculated across these same inputs by the register parity logic to verify that the information has not been corrupted. ... No correction of errors will be completed in this mode.”); *see also* claim element [1.e.]. Accordingly, a Skilled Artisan would have understood that the parity error signal, would have indicated “*a parity error having occurred during any of the memory read or write operations by driving the open drain output and the error edge connection to the first state,*” as required by the claims. *Id.*

f) [21.f] Operations Related To Training Sequences

369. Claim 21 requires “*wherein the memory module is configurable to perform operations related to one or more training sequences while the memory module is not accessed by the memory controller for memory read or write operations; and wherein the module controller is configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection from one of the first state and the second state to the other one of the first state and the second state.*”

370. This limitation is satisfied for the same reasons set forth for claim elements [1.e.], [1.g.] and [10.e.]. Like claim element [10.e.], this element recites “*memory read or write operations,*” rather than “***normal*** *memory read or write operations*” like claim element [1.e], and is satisfied for those additional reasons. Moreover, I note that the combinations analyzed here disclose “*wherein the*

memory module is configurable to perform operations related to one or more training sequences while the memory module is not accessed by the memory controller for memory read or write operations” for the reasons set forth in ¶¶212–230, 242–247, 321–323 above. The combinations disclose “wherein the module controller is configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection from one of the first state and the second state to the other one of the first state and the second state” for the reasons set forth in ¶¶242–247 above.

22. Claim 22 is Unpatentable

371. Claim 22 requires “[t]he memory module of claim 21, wherein the module controller further includes a multiplexor or a logic circuit having an output coupled to the gate of the transistor, and wherein the module controller is configurable to drive the gate of the transistor with either a first signal related to the parity error or a second signal related to the one or more training sequences.”

372. This claim is satisfied or rendered obvious in further combination with Kim for the same reasons set forth for claims 1, 3, and 6. See ¶¶206–211, 251–270, 284–290, *above*. In an abundance of caution, I note that this includes the alternative obviousness combinations of Hazelzet and JEDEC or Buchmann, in further view of Kim, as explained in Section V.A.3 above, ¶¶256–270.

23. Claim 23 is Unpatentable

373. Claim 23 requires “[t]he memory module of claim 22, wherein the transistor has a source coupled to ground, wherein the module controller is configurable to output the signal indicating a parity error having occurred by driving the gate of the transistor high to provide a low impedance path between the open drain output and ground, and wherein the module controller is configurable to provide the information related to the one or more training sequences by driving the open drain output from a high impedance state to ground or from ground to the high impedance state.”

374. This claim is satisfied for the same reasons set forth for claims 3, 4, 5. The analysis in claim 3 satisfies claim element [23.a.], *see* ¶¶251–270, *above*, the analysis in claim 5 satisfies claim element [23.b.], *see* ¶¶277–282, *above*, and the analysis in claim 4 satisfies claim element [23.c.]. *See* ¶¶271–276, *above*. Moreover, as demonstrated above for claim element [1.g], in the combinations analyzed here, the open drain signals relating to the training sequences (*e.g.*, ERROUT#, TS0_done, TS3_ack, TS3_done) are “*unrelated to any memory read or write operation*” because they are related solely to the JEDEC or Buchmann training sequences and not to any memory read or write operations, including because there are no memory read or write operations during the training mode analyzed here. In an abundance of caution, I note that this includes the alternative

obviousness combinations of Hazelzet and JEDEC or Buchmann, in further view of Kim, as explained in Section V.A.3 above, ¶¶256–270.

24. Claim 24 is Unpatentable

375. Claim 24 requires “[t]he memory module of claim 21, wherein the memory module is configurable to perform the operations related to the one or more training sequences while the memory module is not communicating signals via the first edge connections.”

376. This claim is satisfied for the same reasons set forth for claims 1 and 9. See ¶¶231–241, 304–310, *above*.

* * *

I, Donald Alpert, do hereby declare and state, that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

Executed on: 15-SEP-2021



Donald Alpert