

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD. and
SAMSUNG SEMICONDUCTOR, INC.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2022-00064
Patent 10,474,595 B2

Before JON M. JURGOVAN, SHEILA F. McSHANE, and
KARA L. SZPONDOWSKI, *Administrative Patent Judges*.

JURGOVAN, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314, 37 C.F.R. § 42.4

I. INTRODUCTION

Samsung Electronics Co., Ltd. and Samsung Semiconductor, Inc. (collectively, “Petitioner”) filed a Petition (Paper 1, “Pet.”) to institute an *inter partes* review of claims 1–24 of U.S. Patent 10,474,595 B2, issued on November 12, 2019 (Ex. 1001, “the ’595 patent”). Netlist, Inc. (“Patent

Owner”) filed a Preliminary Response (Paper 7, “Prelim. Resp.”) to the Petition. With our authorization (Paper 8), Petitioner filed a Preliminary Reply to the Preliminary Response (Paper 11, “Prelim. Reply”) and Patent Owner filed a Preliminary Sur-Reply (Paper 12, “Prelim. Sur-Reply”). We have jurisdiction under 35 U.S.C. § 314.

Institution of an *inter partes* review is authorized when “the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a).

Based on the current record, and for the reasons explained below, we determine that Petitioner has established a reasonable likelihood that it would prevail with respect to at least one challenged claim. Accordingly, we institute an *inter partes* review as to all the challenged claims and grounds raised in the Petition.

II. BACKGROUND

A. *Real Parties in Interest*

Petitioner identifies Samsung Electronics Co., Ltd. and Samsung Semiconductor, Inc. as the real parties in interest. Pet. 2. Patent Owner identifies itself as the sole real party in interest. Paper 3, 1.

B. *Related Matters*

The parties advise that the ’595 patent is related to *Samsung Electronics Co., Ltd., et al. v. Netlist, Inc.*, IPR2022-00062; *Samsung Electronics Co., Ltd., et al. v. Netlist, Inc.*, IPR2022-00063; and *Samsung Electronics Co., Ltd. v. Netlist, Inc.*, Case No. 1:21-cv-01453 (D. Del.) (“the parallel litigation”). Pet. 1; Paper 3, 3; Paper 10, 1.

The parties advise that the '595 Patent is related to the following legal proceedings, which are no longer pending: (1) *Netlist v. SK hynix Inc.*, Case No. 6:20-cv-00194-ADA (W.D. Tex.); (2) *Samsung Electronics Co., Ltd. v. Netlist, Inc.*, IPR2020-01042; (3) *SK hynix Inc., et al. v. Netlist, Inc.*, IPR2020-01044; (4) *Netlist, Inc. v. SK hynix Inc., et al.*, Case No. 8:17-cv-01030 (C.D. Ca.); (5) *In the Matter of Certain Memory Modules and Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1089 (International Trade Commission); (6) *SK hynix Inc., et al v Netlist, Inc.*, IPR2018-00303; (7) *Netlist, Inc. v. SK hynix Inc., et al.*, Case No. 8:16-cv-01605 (C.D. Ca.); (8) *In the Matter of Certain Memory Modules and Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1023 (International Trade Commission); and (9) *SK hynix Inc., et al. v. Netlist, Inc.*, IPR2017-00548. Pet. 1–2; Paper 3, 3–4; Paper 10, 1.

C. *The '595 Patent (Ex. 1001)*

The '595 Patent describes a memory module coupled to a memory controller of a host computer system. Ex. 1001, code (57). The memory module operates in two modes, one to perform normal read/write operations, and the other to receive and execute training or initialization sequences to prepare the memory module for normal read/write operation. *Id.* The memory module has an open-drain output pin which it uses to indicate a parity error in the first mode for normal read/write operations. *Id.* In the second mode of operation, however, the memory module uses the same output pin to notify the memory controller of the status of its execution of the training sequence, i.e., whether execution of the training sequence is in progress or has been completed. *Id.* at 6:57–63.

Figure 2 of the '595 Patent, below, illustrates an embodiment with multiple memory modules performing handshaking with a memory controller. *Id.* at 2:37–41.

Specifically, Figure 2 shows host computing system 16 including memory controller 14 connected to first and second memory modules 10, 26. *Id.* at 4:24–29, 9:13–19, 9:47–48. The memory modules 10, 26 include respective controller circuits 18, 28 with notification circuits 20, 30. *Id.* at 9:14–23, 10:30–37. Notification circuits 20, 30 have corresponding transistors 36, 38 with open-drain configurations. *Id.* at 9:49–52. As memory modules 10, 26 carry out their training or initialization sequences, memory modules 10, 26 drive the gates of the transistors 36, 38 high, which pulls their outputs 12, 24 low, signaling to the memory controller 14 via input 34 that the initialization sequences have not been completed. *Id.* at 10:30–50. As each memory module 10, 26 completes its initialization sequence, the module drives the gate of its respective transistor 36 or 38 low, causing its output 12 or 24 to enter a high-impedance state. *Id.* When all modules' transistor outputs are in high-impedance states, input 34 draws high, notifying the system memory controller 14 that the all memory modules have completed their initialization sequences and are ready for normal read/write operation. *Id.*

The memory module may comprise a printed-circuit board (PCB) with dynamic random-access memory (DRAM) elements and a module controller. *Id.* at 4:33–34, 4:43–44. The PCB may have edge connections for data, address and control, and error signals (including parity and notification signals). *Id.* at 5:10–17, 8:26–33. The module controller may be an integrated circuit mounted on the PCB. *Id.* at 4:43–44, 13:45–49.

A multiplexor may be connected to the transistor gate to provide either a parity signal or “signal related to the training sequence” (the notification signal). *Id.* at 11:15–23.

D. Illustrative Claim

Claims 1, 10, 17, and 21 of the '595 Patent are independent. Claims 2–9 depend, directly or indirectly, from claim 1. Claims 11–16 depend from claim 10. Claims 18–20 depend from claim 17. Claims 22–24 depend from claim 21. Claim 1 is set forth below with annotated numbering of elements:

1. [1.a] A memory module operable with a memory controller of a host system, comprising:

[1.b] a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;

[1.c] dynamic random access memory elements on the printed circuit board;

[1.d] a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection; and

[1.e.i] wherein the memory module is configurable to operate in any of at least a first mode and a second mode;

[1.e.ii] wherein the memory module in the first mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections,

[1.e.iii] wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations, and

[1.e.iv] wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences;

[1.f.i] wherein the module controller is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations,

[1.f.ii] wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and

[1.f.iii] wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the first mode;

[1.g] wherein the module controller in the second mode is further configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection to a first state or to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.

Ex. 1001, 14:39–15:21.

E. Evidence

Petitioner relies on the following references (*see* Pet. 4), as well as the Declaration of Dr. Donald Alpert. (Ex. 1003).

Reference	Exhibit No.	Patent/Printed Publication
Hazelzet	1014	U.S. Patent Pub. No. 2008/0098277 A1 to Hazelzet, published April 24, 2008
JEDEC	1015	JEDEC COMMITTEE LETTER BALLOT, LRDIMM DDR3 Memory Initialization Chapter Proposal (Dec. 2009)
Buchmann	1016	U.S. Patent No. 8,139,430 B2 to Buchmann et al., issued March. 20, 2012
Kim	1017	U.S. Patent No. 8,359,521 B2 to Kim et al., issued Jan. 22, 2013

Petitioner also supports its challenges with a declaration from Dr. Donald Alpert. Ex. 1003. Patent Owner supports its arguments with testimony from Mr. Robert Murphy. Ex. 2001.

F. Prior Art and Asserted Grounds

Petitioner asserts that claims 1–24 are unpatentable on the following Grounds (Pet. 4):

Claims Challenged	35 U.S.C. §	References
1–24	103(a)	Hazelzet, JEDEC
1–24	103(a)	Hazelzet, Buchmann
3–7, 12–14, 20, 22, 23	103(a)	Hazelzet, JEDEC or Buchmann, and Kim

III. PRELIMINARY MATTERS

A. *Discretion to Deny Institution Under 35 U.S.C. § 314(a)*

Patent Owner contends that the Board should deny institution under 35 U.S.C. § 314(a) in view of the parallel litigation in the District Court of Delaware. Prelim. Resp. 62–64.

Under § 314(a), the Director has discretion to deny institution of an *inter partes* review. See 37 C.F.R. § 42.4(a) (“The Board institutes the trial on behalf of the Director.”); see *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1367 (Fed. Cir. 2016) (“[T]he [Office] is permitted, but never compelled, to institute an [*inter partes* review] proceeding.”). In exercising that discretion, the Board may consider the state of a parallel district court proceeding, among other considerations, as a “factor that weighs in favor of denying the Petition under § 314(a).” *NHK Spring Co. v. Intrix-Plex Techs., Inc.*, IPR2018-00752, Paper 8 at 20 (PTAB Sept. 12, 2018) (precedential) (“NHK”); *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 5–6 (PTAB Mar. 20, 2020) (precedential) (hereafter, “*Fintiv*”). When considering the impact of parallel litigation, the Board seeks, among other things, to minimize the duplication of work to resolve the same issue. See *NHK*, Paper 8 at 19–20.

The Board has identified a nonexclusive list of factors “relat[ing] to whether efficiency, fairness, and the merits” favor discretionary denial in view of parallel district court litigation. *Fintiv*, Paper 11 at 6. Among the factors is the proximity of the court’s trial date to the Board’s projected statutory deadline for a final written decision. *Id.* at 5–6. No trial date has been set in the parallel litigation (Prelim. Resp. 63), and it appears there is no indication that the trial would precede a final written decision in this

proceeding. The remaining *Fintiv* factors do not sufficiently weigh toward exercising our discretion to deny institution. Consequently, we decline to exercise our discretion to deny institution under § 314(a) in view of the parallel litigation.

B. Discretion to Deny Institution Under 35 U.S.C. § 325(d)

Under § 325(d), in determining whether to institute an *inter partes* review, “the Director may take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments previously were presented to the Office.” In evaluating arguments under § 325(d), we use a two-part framework: (1) whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office; and (2) if either condition of the first part of the framework is satisfied, whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims. *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (PTAB Feb. 13, 2020) (precedential) (“*Advanced Bionics*”). We also consider the non-exclusive factors set forth in *Becton, Dickinson and Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (PTAB Dec. 15, 2017) (precedential in relevant part) (“*Becton, Dickinson*”), which “provide useful insight into how to apply the framework” under § 325(d). *Advanced Bionics*, Paper 6 at 9. Those non-exclusive factors are the following:

- (a) the similarities and material differences between the asserted art and the prior art involved during examination;
- (b) the cumulative nature of the asserted art and the prior art evaluated during examination;

(c) the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection;

(d) the extent of the overlap between the arguments made during examination and the manner in which Petitioner relies on the prior art or Patent Owner distinguishes the prior art;

(e) whether Petitioner has pointed out sufficiently how the Examiner erred in its evaluation of the asserted prior art; and

(f) the extent to which additional evidence and facts presented in the Petition warrant reconsideration of the prior art or arguments.

Becton, Dickinson, Paper 8 at 17–18. “If, after review of factors (a), (b), and (d), it is determined that the same or substantially the same art or arguments previously were presented to the Office, then factors (c), (e), and (f) relate to whether the petitioner has demonstrated a material error by the Office.”

Advanced Bionics, Paper 6 at 10.

1. *Analysis*

a) *Advanced Bionics Part 1 – Whether the Same or Substantially the Same Art Previously was Presented to the Office or Whether the Same or Substantially the Same Arguments Previously Were Presented to the Office*

Patent Owner contends that “Petitioner has not met its burden of showing that the same or substantially the same art and arguments were not already considered and appropriately rejected by the Office.” Prelim.

Resp. 58. Patent Owner points to no authority for the proposition that Petitioner has this burden. Petitioner, on the other hand, contends that the Board rejected Patent Owner’s logic in *Alcatel-Lucent USA Inc. v. Oyster Optics, LLC*, IPR2017-02146, Paper 12 at 12–13 (PTAB Feb. 28, 2018).

Prelim. Reply 4–5. *Alcatel-Lucent* states “we discern no such burden in the statutory requirements for a petition under 35 U.S.C. § 312.” *Alcatel-*

Lucent, Paper 12 at 13. We agree, and determine that Patent Owner has not established that Petitioner bears the burden under § 325(d) to show that the same or substantially the same arguments were not considered and rejected by the Office.

Patent Owner further contends that Hazelzet, Buchmann, and Kim are all cited on the face of the '595 patent and were considered during its examination. Prelim. Resp. 60. Patent Owner also indicates that Hazelzet, Buchmann, and Kim were discussed extensively in *SK Hynix Inc. v. Netlist, Inc.*, IPR2018-00303, Paper 42 (final written decision) and other filings in this case before allowing the claims of the '595 patent.

Hazelzet, Buchmann, and Kim are indeed listed on the face of the '595 patent, and were cited in an Information Disclosure Statement filed March 1, 2019, so these references were previously presented to the Office. Ex. 1001, code (56); Ex. 1002, 194–195. Petitioner contends, however, JEDEC was not before the Office during prosecution of the '595 patent, and Patent Owner does not dispute this contention. Ex. 1001, code (56); Reply 4; *see generally* Preliminary Response.

Since Hazelzet, Buchmann, and Kim were presented to the Office, we proceed to part two of *Advanced Bionics*.

b) Advanced Bionics Part 2 – Whether Petitioner has Demonstrated that the Office Erred in a Manner Material to Patentability of the Challenged Claims

As noted, the March 1, 2019 Information Disclosure Statement listed Hazelzet, Buchmann, and Kim. IPR2022-00064, Ex. 1002, 194–195. However, in a statement accompanying the Notice of Allowability, the examiner of the '595 Patent states as follows:

Applicant's Information Disclosure Statement, filed on 03/01/2019 has been received, and entered into the record.

However, it is impractical for the examiner to review the references thoroughly with the number of references cited. By initializing each of the cited references on the accompanying 1449 forms, the examiner is merely acknowledging the submission of the cited references and merely indicating that only a cursory review has been made of the cited references.

Ex. 1002, 187. Because the prosecution history of the '595 patent indicates that these references were given only "cursory review," the record indicates that the examiner's review may not have adequately considered the prior art at issue. Under the circumstances reflected in this record, we decline to exercise our discretion to deny institution under § 325(d). *See Kayak Software Corp. v. Int'l Bus. Machs. Corp.*, CBM2016-00075, Paper No. 16 at 11 (PTAB Dec. 15, 2016) (informative) ("There could be situations where, for example, the prosecution is not as exhaustive, where there are clear errors in the original prosecution, or *where the prior art at issue was only cursorily considered* that can weigh against exercising the discretion." (emphasis added)).

2. *Conclusion on Discretionary Denial Under 35 U.S.C. § 325(d)*

Since JEDEC was not presented to the Office under part one of *Advanced Bionics*, and since Hazelzet, Buchmann, and Kim may not have been adequately considered under part two of *Advanced Bionics*, we decline to exercise our discretion to deny institution under § 325(d).

IV. ANALYSIS OF CHALLENGED GROUNDS

We turn now to Petitioner’s asserted grounds of unpatentability in the Petition and Patent Owner’s arguments in its Preliminary Response to determine whether Petitioner has met the threshold standard of 35 U.S.C. § 314(a).

A claim is unpatentable under 35 U.S.C. § 103(a) if “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

A patent claim “is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art.” *KSR*, 550 U.S. at 418. An obviousness determination requires finding “both ‘that a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so.’” *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367–68 (Fed. Cir. 2016) (citation omitted); *see also KSR*, 550 U.S. at 418. Further, an assertion of obviousness “cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning

with some rational underpinning to support the legal conclusion of obviousness.” *KSR*, 550 U.S. at 418; *In re NuVasive, Inc.*, 842 F.3d 1376, 1383 (Fed. Cir. 2016) (a finding of a motivation to combine “must be supported by a ‘reasoned explanation’”).

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic*, 815 F.3d at 1363 (citing 35 U.S.C. § 312(a)(3)); *see also Intelligent Bio-Sys.*, 821 F.3d at 1369 (“It is of the utmost importance that petitioners in the IPR proceedings adhere to the requirement that the initial petition identify ‘with particularity’ the ‘evidence that supports the grounds for the challenge to each claim.’” (quoting 35 U.S.C. § 312(a)(3))). Therefore, to prevail in an *inter partes* review, Petitioner must explain how the proposed combinations of prior art would have rendered the challenged claims unpatentable. At this preliminary stage, we determine whether the information presented in the Petition shows there is a reasonable likelihood that Petitioner would prevail in establishing that at least one of the challenged claims would have been obvious over the proposed combinations of prior art.

A. *Level of Ordinary Skill in the Art*

Petitioner asserts a person of ordinary skill in the art “would have had a [B]achelor’s degree in computer engineering, or a related field, and several years of additional experience working with computer memory systems. She would have been familiar with computer memory systems and basic CPU architecture documented in the literature, including standards, and generally available in commercial systems, including how computer components access a computer’s memory, the role of a memory controller,

the basic operation of memory modules and devices, and the techniques used to couple memory devices to the other components of the computer system.” Pet. 10 (citing Ex. 1003 ¶ 55). Patent Owner does not dispute Petitioner’s proposed level of skill at this stage. *See generally* Prelim. Resp.

We find Petitioner’s proposal is consistent with the level of ordinary skill in the art reflected by the ’595 patent and the prior art of record, and, therefore, adopt Petitioner’s proposed level of ordinary skill in the art for purposes of this Decision. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

B. Claim Construction

We construe each claim “in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent,” the same standard used to construe the claim in a civil action. 37 C.F.R. § 42.100(b).

Petitioner proposes the following constructions:

Claim Term	Proposed Construction
memory read and write operations	operations used to communicate data between the memory module and the memory controller in response to commands from the memory controller
normal memory read or write operations	operations used to communicate data between the memory module and the memory controller in response to commands from the memory controller
training sequence	a set of operations occurring in a particular order and used for training
notification signal associated with the [one or more training sequences] / “information related to the [one or more training sequences]” / “open-	unscheduled signal/information/open-drain signals provided without polling that indicate the status of the one or more training sequences

drain signals related to the [one or more training sequences]”	
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Pet. 18–24. Petitioner presents several arguments and support in favor of its proposed constructions. *Id.* Petitioner also argues that the term “mode” does not require construction. *Id.* at 21–22. Patent Owner does not dispute Petitioner’s proposed constructions at this time. Prelim. Resp. 4.

At this stage in the proceeding, we need only construe the claims to the extent necessary to determine whether to institute *inter partes* review. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“[W]e need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))). We determine that, at this stage of this proceeding, there is no need to expressly construe these claim terms in order to determine whether or not to institute review because the parties do not dispute the claimed terms’ meanings, and their ordinary and customary meanings suffice for our analysis.

C. Effective Filing Date of the ’595 Patent’s Claims

The ’595 patent was filed on December 28, 2017, and claims priority through a series of utility applications, including its parent that issued as U.S. Patent 9,858,218 (“the ’218 patent”). Ex. 1001, codes (22), (60), (63). The ’595 patent also claims priority to Provisional Application No. 61/186,799, which was filed on June 12, 2009 (hereafter, “the Provisional”). Ex. 1001, code (60). Petitioner contends that the ’595 patent is not entitled to the benefit of the June 12, 2009 filing date of the Provisional because

certain claim limitations do not have adequate written description support. Pet. 5–10. Patent Owner disagrees. Prelim. Resp. 1, 10–19. If we apply the Provisional’s filing date as the earliest effective filing date of the ’595 patent, the JEDEC reference does not qualify as prior art. This is not dispositive to all Grounds in the Petition, but would be fatal to combinations of the Grounds that include the JEDEC reference.

1. *Legal Background*

For a patent to claim the benefit of the filing date of its provisional application, the specification of the provisional “must ‘contain a written description of the invention and the manner and process of making and using it, in such full, clear, concise, and exact terms,’ 35 U.S.C. § 112 ¶ 1, to enable an ordinarily skilled artisan to practice the invention claimed in the non-provisional application.” *Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (emphases omitted) (quoting *New Railhead Mfg., L.L.C. v. Vermeer Mfg. Co.*, 298 F.3d 1290, 1294 (Fed. Cir. 2002)); *see also* 35 U.S.C. § 119(e)(1).

In evaluating the effective filing date of the ’595 patent to determine whether to institute *inter partes* review, we first address the parties’ respective burdens. In an *inter partes* review, Petitioner bears the ultimate burden of persuasion regarding unpatentability, which never shifts to patent owner. *Dynamic Drinkware*, 800 F.3d at 1379. *Dynamic Drinkware* also establishes that Petitioner has the initial burden of production to show a reference is prior art. *Id.* The burden of production then shifts to Patent Owner to refute Petitioner’s argument by either showing the prior art does not actually render the claims unpatentable or does not qualify as prior art. *Id.* at 1380. The burden of production then shifts back to Petitioner to

respond to Patent Owner’s argument. *Id.* The Board then evaluates all of the evidence and determines whether Petitioner has satisfied its burden of persuasion regarding unpatentability. *Id.* At the institution stage, the Board has applied a similar burden-shifting approach with respect to the effective filing date of the challenged claims. *Polaris Wireless, Inc. v. TruePosition, Inc.*, IPR2013-00323, Paper 9 (PTAB Nov. 15, 2013).

Because the Provisional does not have the same disclosure as the ’595 patent, we do not presume the ’595 patent is entitled to the benefit of the Provisional’s filing date. But because Petitioner has the burden to show a reasonable likelihood of prevailing on a ground of patentability to institute trial, we require Petitioner to show that the art existed as of the date of invention, presumed to be the filing date of an application until an earlier date is proved. *Bausch & Lomb, Inc. v. Barnes-Hind/Hydrocurve, Inc.*, 796 F.2d 443, 449 (Fed. Cir. 1986); *In re Fong*, 378 F.2d 977, 980 (CCPA 1967) (“Appellants’ filing date, no earlier date having been proved, is their date of invention.”). The burden of production then shifts to Patent Owner to respond to Petitioner’s specific arguments to show sufficiently that the ’595 patent claims are entitled to the earlier filing date of the Provisional. We apply this framework when considering whether the parties have met their respective burdens at this stage of the proceeding.

2. *Whether the Provisional Describes the Claimed Invention*

To show sufficient written description under 35 U.S.C. § 112 ¶ 1, “the description must ‘clearly allow persons of ordinary skill in the art to recognize that [the inventor] invented what is claimed.’” *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (en banc)

(quoting *Vas-Cath Inc. v. Mahurkar*, 935 F.2d 1555, 1563 (Fed. Cir. 1991)).

“[T]he hallmark of written description is disclosure,” and

the test requires an objective inquiry into the four corners of the specification from the perspective of a person of ordinary skill in the art. Based on that inquiry, the specification must describe an invention understandable to that skilled artisan and show that the inventor actually invented the invention claimed.

Id.; see also *Vas-Cath*, 935 F.2d at 1563–64 (stating that “the applicant must also convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the invention,” which, “for purposes of the ‘written description’ inquiry, [is] whatever is now claimed” (emphases omitted)). The written description inquiry is a question of fact and, as such, “the level of detail required to satisfy the written description requirement varies depending on the nature and scope of the claims and on the complexity and predictability of the relevant technology.” *Ariad*, 598 F.3d at 1351.

Petitioner shows that Hazelzet, JEDEC, Buchmann, and Kim have filing or publication dates before the ’595 patent’s filing date. Pet. 24, 27–28; Ex. 1001, code (22); Ex. 1014, code (22); Ex. 1015, 1; Ex. 1016, code (22); Ex. 1017, code (22). Petitioner identifies several claim limitations which Petitioner contends are not supported by the Provisional. Pet. 5–10. Patent Owner disagrees and asserts that the Provisional provides written description support for each of the limitations. Prelim. Resp. 11–16.

At the outset, Petitioner contends the standard for whether a provisional supports a nonprovisional is that the provisional must show the inventor was in possession of the invention through written description, and any absent text must be “necessarily comprehended” at the time the

application was filed. Pet. 6 (citing *Hyatt v. Boone*, 146 F.3d 1348, 1354–55 (Fed. Cir. 1998)). Patent Owner contends that Petitioner relies on the wrong standard, and that the provisional application must reasonably convey to those skilled in the art that the inventor has possession of the claimed subject matter as of the filing date. Prelim. Resp. 10 (citing *Ariad Pharm., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010)). Petitioner and Patent Owner both agree the standard requires demonstrating that the inventor was in possession of the invention, and to the extent Petitioner and Patent Owner disagree on the standard concerning absent text, neither party demonstrates that any difference in standards is determinative of the outcome of this issue.

First, Petitioner contends that the limitation “wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations” as recited in claims 10, 17, and 21 is not supported by the Provisional. Pet. 5–8. Petitioner asserts that

The [P]rovisional says nothing about the memory controller not accessing the module for read and write operations in training mode. Indeed, it mentions the word “training” in only one sentence fragment, never explains that such training may occur in its own mode, never uses the word “mode” at all, and never says anything about what operations may or may not occur in training mode.

Id. at 6 (citing Ex. 1003 ¶ 45).

Patent Owner contends that the Provisional (which it refers to as a Priority Application—see Prelim. Resp. 5) supports sharing of a pin between an Error-out and Notifying signal, and that the logic on the shared pin conveys different information depending on whether the training or normal operation is occurring. Prelim. Resp. 11–12. Patent Owner relies on

testimony from its declarant, Mr. Murphy, to support that training over edge connections was known, and was typical, in the art. *Id.* at 13–14 (citing Ex. 2001 ¶¶ 29–32).

On the record before us, we are not persuaded that the portion of the Provisional that Patent Owner relies upon (Ex. 1008, 22–23) sufficiently discloses “wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations,” as recited in claim 1; “wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences without communicating data signals via the first edge connections,” as recited in claim 10; “performing operations related to one or more training sequences while the memory module is not accessed by the memory controller for memory read or write operations,” as recited in claim 17; “wherein the memory module is configurable to perform operations related to one or more training sequences while the memory module is not accessed by the memory controller for memory read or write operation,” as recited in claim 21. Rather, we agree with Petitioner that the portion of the Provisional cited by Patent Owner discusses the shortcomings in the prior art, rather than the claimed invention. *See* Ex. 1008, 22–23 (“The shortcoming of the current the [sic] LR-DIMM proposal is that, instead of adopting the notification, the proposal requires the MCH to be in standby (idle, or wait) while the memory subsystem controller completes its task.”). This portion of the Provisional does not refer to training or edge connections, or provide any indication that the inventor was in possession of the foregoing limitations. *See Lockwood v. American Airlines, Inc.*, 107 F.3d 1565, 1572 (Fed. Cir. 1997) (“It is not sufficient for purposes of the written description

requirement of § 112 that the disclosure, when combined with the knowledge in the art, would lead one to speculate as to modifications that the inventor might have envisioned, but failed to disclose.”). Therefore, on this record and at this stage of the proceeding, we do not find that the evidence demonstrates sufficient written description support as to each of these limitations.

Second, Petitioner contends that claim 1’s limitation that its memory module “perform operations related to one or more training sequences,” and similar limitations in claims 10, 17, and 21, are not disclosed in the Provisional, which only discloses “MB training.” Pet. 8 (citing Ex. 1003 ¶¶ 51–52). Specifically, Petitioner contends that the Provisional does not disclose any training “sequences,” particularly not “one or more” training sequences, and does not provide information or signals related to such specific “training sequences.” *Id.* at 8–9.

We agree with Petitioner. Patent Owner states that one of ordinary skill in the art would have understood that “MB training” and “one or more parts of the initialization operation sequences” are equivalent to “one or more training sequences” as recited in the ’595 patent’s claims. Prelim. Resp. 14 (citing Ex. 2001 ¶¶ 35–38; Ex. 1008, 22). But then Patent Owner states “the training must be performed as during the ‘initialization operation sequences,’” which suggests the training is not equivalent to the initialization operation sequences, but rather is something separate. *Id.* at 15. Patent Owner’s contentions are inconsistent, and thus Patent Owner has not shown persuasively that the Provisional discloses “one or more training sequences.”

Third, Petitioner contends that the Provisional does not support claim 21's limitation "wherein the [DRAMs] are configurable to communicate one or more N-bit-wide data signals with the memory controller . . . , where N is at least 32." Pet. 9. Specifically, Petitioner contends that "DRAM" is mentioned just once in the Provisional, and that the terms "data signal," "bit," "width," and "32" are found nowhere in the Provisional. *Id.*

Patent Owner contends that Petitioner concedes that a person of ordinary skill in the art "would have been aware of the then-current DDR3 LRDIMMs, which supported 64-bit I/O configurations for the communication of data signals. Prelim. Resp. 15 (citing Ex. 2001 ¶ 40). Even assuming one would have known of 64-bit I/O configurations for data signals, that does not provide support for the recited "N-bit-wide data signals" over the entire range of "N" being "at least 32." *See, e.g., In re Lukach*, 442 F.2d 967 (CCPA 1971) (range not supported by written description of specific example within the range). Consequently, Patent Owner has not shown that the Provisional provides sufficient written description support for this limitation.

Petitioner argues that the '595 patent's claims 8, 15, 16, 18, and 19 require that "the second edge connections [for address and command] include one or more pins that are not active while the memory module is in the second mode," or substantially similar "pins not active" limitations. Pet. 9–10. Petitioner notes, however, that the terms "edge," "edge connection[s]," "mode," and "active" do not appear in the Provisional, nor does the Provisional mention pins [for address and command] on an edge

connection are not active during certain modes. *Id.* at 10 (citing Ex. 1003 ¶ 54).

Patent Owner contends that the Provisional discloses a shared pin that is low during MB training and high to indicate training is done. Prelim. Resp. 17. This, however, does not disclose what is claimed—“pins that are not active while the memory module is in the second mode.” Accordingly, on this record and at this stage of the proceeding, we do not find that the evidence demonstrates sufficient written description support for this limitation.

In conclusion, on the record before us, we determine that at this stage of the proceeding, Petitioner has made a sufficient showing that the challenged claims of the ’595 patent do not have written description support in the Provisional, and, therefore, are not entitled to an effective filing date of June 12, 2009. Therefore, Petitioner has sufficiently shown that JEDEC qualifies as prior art.

D. Grounds 1 and 2: Obviousness Over Hazelzet and JEDEC or Buchmann

Petitioner contends claims 1–24 would have been obvious over the combination of Hazelzet and JEDEC or Buchmann, and relies on the Declaration of Dr. Donald Alpert (Ex. 1003) in support. Pet. 40–68. For the reasons that follow, we are persuaded that the evidence, including Dr. Alpert’s testimony, sufficiently supports Petitioner’s arguments and, therefore, establishes a reasonable likelihood of prevailing with respect to this ground at this stage of the proceeding.

1. *Hazelzet (Ex. 1014)*

Hazelzet was published on April 24, 2008 and is titled “High Density High Reliability Memory Module With Power Gating and a Fault Tolerant Address and Command Bus.” Ex. 1014, codes (43), (54). Petitioner asserts that Hazelzet is prior art under 35 U.S.C. §§ 102(a), (b), and (e). Pet. 24.

Hazelzet is generally directed to a high density high reliability memory controller/interface. Ex. 1014 ¶ 7. Figure 2, reproduced below, is a block diagram of the enhanced server memory arrangement:

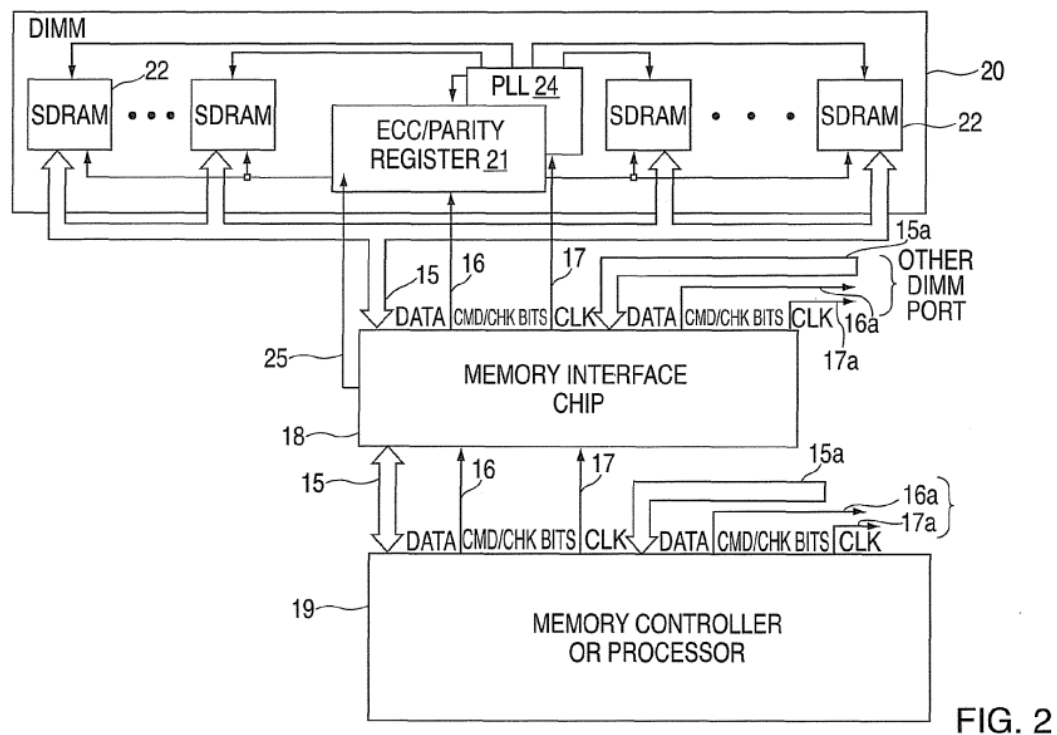


Figure 2 depicts dual inline memory module (“DIMM”) 20 with a “novel ECC/Parity Buffer chip 21” coupled to memory interface chip 18, which is coupled to memory controller or processor 19. *Id.* ¶ 38. Hazelzet describes that “DIMMs are printed circuit cards designed to carry a plurality of DRAMs 22 thereon and the DRAM output pins . . . are connected via the printed circuit to selected connectors 23 along the edge of both the back and

front sides of the card.” *Id.* ¶ 39. Figure 2 shows “the memory interface chip 18 sends and receives data from the DIMMs via the data line 15 and sends address and commands via line 16.” *Id.* ¶ 38. “The memory interface chip 18 then sends and receives data, via line 15, to the memory devices, or DRAMs 22 and sends address and command information to the register chip 21 via add/cmd line 16 and check bits for error correction purposes to the ECC/Parity register chip 21 via line 25.” *Id.*

Hazelzet further describes that the DIMM has “added error correction code logic (ECC) incorporated therein for correcting single bit errors while permitting continuous memory operation independent of the existence of these errors.” *Id.* ¶ 64. Hazelzet also discloses “[a] parity operating mode . . . to permit the system to interrogate the device to determine the error condition.” *Id.* In this way, Hazelzet describes two modes: “ECC Mode (/ECC Mode low)” and “parity mode (/ECC Mode high).” *Id.* ¶¶ 69–70; see also Ex. 1014, Fig. 8. In addition, Hazelzet describes error reporting circuitry, where “[t]wo open-drain outputs are available to permit multiple modules to share a common signal line for reporting an error that occurred during a valid command (/CS=low) cycle (consistent with the re-driven signals).” *Id.* ¶ 72. “/Error (CE) indicates that a correctable error occurred and was corrected by the ECC logic, /Error (UE) indicates that an uncorrectable error occurred and depending on the mode selected is an uncorrectable ECC error or a parity error.” *Id.*

2. JEDEC (Ex. 1015)

JEDEC is titled “LRDIMM DDR3 Memory Initialization Chapter Proposal” and was a proposal to the JEDEC JC-40.4 committee for ballot approval as a standard. Ex. 1015, 1; Ex. 1050 ¶ 7. JEDEC JC40.4 is a

subcommittee for development of standards for “Registered and Fully Buffered Memory Support Logic.”¹ Petitioner presents supporting testimony and evidence that JEDEC was distributed to the members of the JC-40.4 committee on November 11, 2009, and to “numerous interested members of the relevant public” with no obligation of confidentiality, and with the expectation that it would be freely discussed with others in November 2009. Pet. 25–28 (citing Exs. 1048–1050, 1054, 1055). Petitioner, therefore, asserts that JEDEC was publicly accessible by November 11, 2009, and at least before June 13, 2010. Pet. 27. Petitioner asserts that JEDEC is prior art under 35 U.S.C. § 102(a). *Id.*

JEDEC generally describes a “power-up initialization of the Memory Buffer.” Ex. 1015, 3. JEDEC discloses a training mode of MB-DRAM Training that includes two training sequences, “Write Leveling” and “Read Enable Training.” *Id.* at 8. JEDEC states that “[n]o DRAM commands or control word writes (either over the Command/Address and Control buses or via SMBus) can be issued to the MB until the MB-DRAM Interface training is complete and the DODtn inputs must be kept low.” *Id.* JEDEC describes that “training completion can be signaled by the assertion of ERROUT#.” *Id.*

a) *Whether JEDEC is a Printed Publication*

A petitioner may assert unpatentability of a claim of a challenged patent “only on a ground that could be raised under section 102 or 103 and only on the basis of prior art consisting of patents or *printed publications*.” 35 U.S.C. § 311(b) (emphasis added).

¹ <https://www.jedec.org/committees/jc-40>.

In determining whether a reference qualifies as a printed publication, “[t]he key inquiry is whether or not a reference has been made ‘publicly accessible.’” *M&K Holdings, Inc. v. Samsung Elecs. Co.*, 985 F.3d 1376, 1379 (Fed. Cir. 2021) (quoting *In re Klopfenstein*, 380 F.3d 1345, 1350 (Fed. Cir. 2004)); *In re Hall*, 781 F.2d 897, 898–99 (Fed. Cir. 1986). “A reference will be considered publicly accessible if it was ‘disseminated or otherwise made available to the extent that persons interested and ordinarily skilled in the subject matter or art exercising reasonable diligence[] can locate it.’” *Medtronic, Inc. v. Barry*, 891 F.3d 1368, 1380 (Fed. Cir. 2018) (alteration in original) (quoting *Kyocera Wireless Corp. v. Int’l Trade Comm’n*, 545 F.3d 1340, 1350 (Fed. Cir. 2008)); *Acceleration Bay, LLC v. Activision Blizzard Inc.*, 908 F.3d 765, 772 (Fed. Cir. 2018) (citing *Jazz Pharm., Inc. v. Amneal Pharm., LLC*, 895 F.3d 1347, 1355–56 (Fed. Cir. 2018)).

At the institution stage, the operative question is whether a petitioner has established a reasonable likelihood that a reference is a printed publication. *Hulu, LLC v. Sound View Innovations, LLC*, IPR2018-01039, Paper 29, at 21 (PTAB Dec. 20, 2019) (precedential). This differs from the standard in a final written decision, at which point “the petitioner bears the burden of establishing by a preponderance of the evidence that a particular document is a printed publication.” *Nobel Biocare Servs. AG v. Intradent USA, Inc.*, 903 F.3d 1365, 1375 (Fed. Cir. 2018) (citing *Medtronic*, 891 F.3d at 1380).

Patent Owner argues that JEDEC is not a “printed publication.” Prelim. Resp. 6–10. Patent Owner argues Petitioner failed to carry its burden to prove both that (1) the JEDEC proposal was available to persons

of ordinary skill in the art (and not just those who were already JEDEC members) and (2) that persons of ordinary skill in the art could have reasonably found the JEDEC proposal. Prelim. Resp. 6–7.

Specifically, Patent Owner argues that Petitioner did not show that anyone outside of the JC.40.4 subcommittee received the JEDEC proposal or would have been aware of it. Prelim. Resp. 7–8. Petitioner argues the JEDEC proposal was “distributed to twenty-three key members of the interested public, with no obligation of confidentiality.” Reply 1 (quoting Pet. 26). Petitioner argues that Patent Owner misplaces its reliance on the non-precedential decision in *Samsung Electronics Co. v. Rembrandt Wireless Technologies, LP*, IPR2014-00514, Paper 18, at 4–10 (PTAB Sept. 9, 2014). Although the Board there held the reference in question was not publicly accessible because it was known only to members of a standards working group that had developed the reference, Petitioner contends this reasoning was later rejected in *GoPro, Inc. v. Contour IP Holding LLC*, 908 F.3d 690, 694 (Fed. Cir. 2018) where a catalog distributed at a trade show that was not open to the general public nonetheless amounted to a printed publication because interested members of the relevant public could have accessed the catalog with reasonable diligence. Reply 1. Since *GoPro* is precedential, we determine that Petitioner has the better argument on this issue.

Patent Owner further argues that Petitioner did not show that persons of ordinary skill in the art could have reasonably found the JEDEC proposal. Prelim. Resp. 8–10. Petitioner counters that the JEDEC proposal was disseminated in connection with a JEDEC meeting, and thus neither indexing nor searchability was required. Reply 3. Petitioner’s evidence

shows that the JEDEC proposal was distributed without confidentiality obligation to members of twenty-three companies in the field of computer memories. Pet. 26–27 (citing Ex. 1050 ¶¶ 8–9, Ex. C, 21–22). We agree that Petitioner relies on dissemination of the JEDEC proposal, as opposed to indexing or cataloging, to establish public accessibility of the JEDEC proposal. Accordingly, Patent Owner’s argument is unpersuasive.

We determine that Petitioner’s evidence presents a reasonable likelihood that the JEDEC proposal is a printed publication.

3. *Buchmann (Ex. 1016)*

Buchmann was filed on July 1, 2008, issued on March 20, 2012, is titled “Power-On Initialization and Test for a Cascade Interconnect Memory System.” Ex. 1015, codes (22), (45), (54). Petitioner asserts that Buchmann is prior art under 35 U.S.C. § 102(e). Pet. 28.

Buchmann is generally directed to “[a] memory buffer, memory system and method for power-on initialization and test for a cascade interconnect memory system.” Ex. 1015, code (57). Buchmann describes that “the memory buffer includes logic for executing a power-on and initialization training sequence initiated by the memory controller.” *Id.* Buchmann discloses that it “is operable in a static bit communication (SBC) mode and a high-speed mode.” *Id.* at 1:43–55.

Buchmann describes several training sequences, including training sequence TS0, which “is used to perform upstream (US) and downstream (DS) clock detection and repair (if necessary).” *Id.* at 5:51–53. During this training sequence, the memory module outputs various commands, including TS_done, which “indicates the local and all cascaded MBs are done with

TS0.” *Id.* at 6:1–20, Table 1. Buchmann also similarly describes other training sequences, TS2 and TS3. *Id.* at 7:15–8:45.

4. *Analysis of Independent Claim 1*

a) *Limitation 1.a: “A memory module operable with a memory controller of a host system, comprising”*

At this stage of the proceeding, we need not, and do not, determine whether the preamble of claim 1 is limiting, because Petitioner shows sufficiently for purposes of institution that the asserted prior art, specifically, the combination of Hazelzet and JEDEC, teaches the preamble.

In particular, Petitioner contends “Hazelzet discloses dual inline memory modules (‘DIMMs’) configured to operate with the ‘memory controller’ of the host system.” Pet. 41 (citing Ex. 1014, Figs. 2, 3A–3D, ¶¶ 36–39; Ex. 1003 ¶ 193).

On this record, Petitioner has made a sufficient showing that Hazelzet discloses claim 1’s preamble, to the extent it is limiting.

b) *Limitation 1.b: “a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections”*

Petitioner contends Hazelet’s DIMM comprises a printed circuit board which fits in the slot of the host system. Pet. 42–44 (citing Ex. 1014 ¶¶ 15, 37, 39, 97, Figs. 2, 3A–3D, 9, 11; Ex. 1003 ¶¶ 196–198). Petitioner further contends the printed circuit board has a first set of edge connections for

communicating data signals between the module and the memory controller (Pet. 45 (citing Ex. 1014, Figs. 7A–7C, ¶¶ 15, 35, 38, 41; Ex. 1003 ¶ 199)) and a second set of edge connections for communicating address and control signals from the memory controller (Pet. 45 (citing Ex. 1014, Figs. 7A–7C, ¶¶ 15, 35, 38, 41; Ex. 1003 ¶ 200)). Petitioner further contends Hazelzet has an error edge connection coupled to the open drain output of the module controller. Pet. 45–46 (citing Ex. 1014, Figs. 4B, 7A, ¶¶ 72, 109; Ex. 1003 ¶ 201).

Patent Owner does not specifically respond to these arguments. *See generally* Prelim. Resp. Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that Hazelzet teaches this limitation for purposes of institution.

c) Limitation 1.c: “dynamic random access memory elements on the printed circuit board”

Petitioner contends Hazelzet’s memory module includes DRAMs on the printed circuit board. Pet. 46 (citing Ex. 1014 ¶ 15, Figs. 2, 3A–3D; Ex. 1003 ¶ 204).

Patent Owner does not specifically respond to this argument. *See generally* Prelim. Resp. Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that Hazelzet teaches this limitation for purposes of institution.

d) Limitation 1.d: “a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having

an open drain output coupled to the error edge connection”

Petitioner contends Hazelzet’s ECC/parity register discloses a module controller, and has an uncorrectable error output 121, which is an open drain output. Pet. 46 (citing Ex. 1014, Figs. 3A–3D, 4A–4B, ¶¶ 44, 59, 72). Petitioner contends Hazelzet’s ECC/parity register is on the printed circuit board and is coupled to the DRAMs. *Id.* (citing Ex. 1014, Figs. 3A–3D, ¶¶ 39, 42; Ex. 1003 ¶ 207). Petitioner contends Hazelzet’s UE 121 is coupled to the error edge connection of the module. *Id.* (citing Ex. 1014, Figs. 4B, 7A (pin 142), ¶¶ 59, 72; Ex. 1003 ¶¶ 208–211).

Patent Owner does not specifically respond to these arguments. *See generally* Prelim. Resp. Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that Hazelzet teaches this limitation for purposes of institution.

e) Limitation 1.e.i: “wherein the memory module is configurable to operate in any of at least a first mode and a second mode”

Petitioner contends Hazelzet’s memory module operates in the parity mode, corresponding to the claimed first mode, and an ECC mode. Pet. 46–47 (citing Ex. 1014, Fig. 8, ¶¶ 64, 69–72; Ex. 1003 ¶ 213). Petitioner contends JEDEC discloses a second mode in which training of the memory module would be carried out. *Id.*

Patent Owner does not specifically respond to these arguments. *See generally* Prelim. Resp. Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that Hazelzet and JEDEC or Buchmann teaches this limitation for purposes of institution.

f) Limitation 1.e.ii: “wherein the memory module in the first mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections”

Petitioner contends that Hazelzet’s memory module is configurable to receive address and control signals via the edge connections. Pet. 47 (citing Ex. 1014 ¶¶ 15, 35, 38, 41, Figs. 2, 7A–7B; Ex. 1003 ¶ 214). Petitioner further contends Hazelzet’s memory module communicates address and command information normally as a JEDEC compliant device, sending address and control to the register and data to the DRAMs. *Id.* (citing Ex. 1014 ¶¶ 44, 75, Fig. 8; Ex. 1024, 1, 14, 16; Ex. 1003 ¶¶ 215, 219). Petitioner contends Hazelzet discloses that these operations occur during the parity mode, which is a normal mode of operation. *Id.* at 48–50 (citing Ex. 1014 ¶¶ 38, 64, 70, 75; Ex. 1003 ¶¶ 221–223, 225).

Patent Owner does not specifically respond to these arguments. *See generally* Prelim. Resp. Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that Hazelzet and JEDEC or Buchmann teaches this limitation for purposes of institution.

g) Limitation 1.e.iii: “wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations”

Petitioner contends that the combinations include JEDEC’s or Buchmann’s training sequences in a training mode (“second mode”) during initialization separate from any mode that includes memory read and write operations in response to memory controller commands, thereby satisfying

this limitation. Pet. 50 (citing § V.D). Petitioner further argues that none of Hazelzet, JEDEC, and Buchmann disclose memory read and write operations occurring during training operations, so their silence additionally satisfies this limitation. *Id.* (citing Ex. 1003 ¶ 229; *Süd-Chemie, Inc. v. Multisorb Technologies, Inc.*, 554 F.3d 1001, 1004–05 (Fed. Cir. 2009)).

Patent Owner does not specifically respond to these arguments. *See generally* Prelim. Resp. Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that Hazelzet and JEDEC or Buchmann teaches this limitation for purposes of institution.

h) Limitation I.e.iv: “wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences”

Petitioner contends that the proposed combinations include a separate training mode (“second mode”) into which the module can be placed and in which the module can implement (“configurable to perform”) various training sequences (e.g., Write Leveling and Read Enable Training per JEDEC/TS0 and TS3 per Buchmann) (“operations related to one or more training sequences”). Pet 50 (citing § V.D). Petitioner contends that each of these operations includes a set of operations occurring in a particular order, used for training the memory module. *Id.* at 51 (citing Ex. 1015, 8; Ex. 1039, 8–9; Ex. 1016, Figs. 4, 6, 5:51–57, 8:24–9:18; Ex. 1040, 14:1–15.3; Ex. 1018, Fig. 4; Ex. 1003 ¶ 230).

Patent Owner does not specifically respond to these arguments. *See generally* Prelim. Resp. Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that

Hazelzet and JEDEC or Buchmann teaches this limitation for purposes of institution.

i) *Limitation 1.f.i: “wherein the module controller is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations”*

Petitioner contends, as explained for claim limitations [1.b] and [1.e.ii], that Hazelzet’s module receives address and control signals associated with normal memory read and write operations over edge connections. Pet. 51 (citing Ex. 1014, Figs. 2, 7A–7B, ¶¶ 15, 35, 38, 41, 64, 70; Ex. 1024, 13–14, 16; Ex. 1003 ¶ 232).

Patent Owner does not specifically respond to these arguments. See generally Prelim. Resp. Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that Hazelzet and JEDEC or Buchmann teaches this limitation for purposes of institution.

j) *Limitation 1.f.ii: “wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals”*

Petitioner contends, as explained for claim limitations [1.b] and [1.e.ii], that Hazelzet discloses a printed circuit board that has a first set of edge connections for communicating data signals between the DRAM and the system memory controller. Pet. 51 (citing Ex. 1014, Figs. 7A–7C, ¶¶ 15, 35, 38, 41). Petitioner contends the communication of data signals occurs while the memory module is in the “parity mode” and in accordance with the received address and control signals. *Id.* (citing Ex. 1014, Figs. 2, 8, ¶¶ 15,

35, 38, 41, 64, 70). Petitioner contends, as explained for claim limitation [1.e.ii], data communication between the memory module and the memory controller is “in accordance with the address and control signals.” *Id.* at 51–52 (citing Ex. 1014, Figs. 2, 7A–&C, 8 ¶¶ 15, 35, 38, 41, 64, 70; Ex. 1024, 13; Ex. 1003 ¶¶ 214–223, 233).

Patent Owner does not specifically respond to these arguments. *See generally* Prelim. Resp. Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that Hazelzet and JEDEC or Buchmann teaches this limitation for purposes of institution.

k) Limitation 1.f.iii: “wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the first mode”

Petitioner contends, as explained in claim elements [1.b] and [1.d], that the error edge connection (pin 142) is coupled to the open drain output (UE 121) of the ECC/Parity register (“module controller”). Pet. 52 (citing Ex. 1014, Figs. 4B, 7A (pin 142), ¶¶ 59, 72; Ex. 1003 ¶ 234). Petitioner contends the ECC/Parity register includes an “SEC/DED ECC 90” with “parity generator/checker circuit 231.” *Id.* (citing Ex. 1014, ¶¶ 28, 76, Figs. 4B, 5; Ex. 1003 ¶ 235). Petitioner notes that when the memory module is in the parity mode (“first mode”), the “parity generator/checker circuit 231” generates and sends the “parity error signal (PERR)” to the “error logic circuit” 100. *Id.* (citing Ex. 1014, Figs. 4, 5, ¶¶ 70, 76; Ex. 1003 ¶ 236). Petitioner contends the “error logic circuit” 100 outputs the parity error signal (PERR) to the memory controller through the output line UE 121,

which is an open-drain output coupled to the memory controller using pin 142. *Id.* (citing Ex. 1014 ¶¶ 38, 59, 70, 72, Fig. 7A (pin 142); Ex. 1003 ¶¶ 237–240).

Patent Owner does not specifically respond to these arguments. *See generally* Prelim. Resp. Based on our review and consideration of the current record, we determine that Petitioner has shown adequately that Hazelzet and JEDEC or Buchmann teaches this limitation for purposes of institution.

l) Limitation 1.g: “wherein the module controller in the second mode is further configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection to a first state or to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state”

Petitioner contends that in the proposed combinations, the Hazelzet module would be modified to be configurable to enter a training mode and output JEDEC or Buchmann training status signals to the system memory controller via an open drain output UE 121. Pet. 52–53 (citing § V.D). According to Petitioner, each of the status signals analyzed (ERROUT#, TS0_done, TS3_ack, TS3_done) represent the “information related to the one or more training sequences” because each provides status about the related sequences, such as whether it has been completed or whether all memory buffers have returned an acknowledgement. *Id.* at 53. Petitioner contends each of these combinations alternatively satisfies “wherein the module controller in the second mode is further configurable to provide

information related to the one or more training sequences.” *Id.* (citing Ex. 1003 ¶¶ 164–167, 243).

Petitioner further contends Hazelzet’s memory system involves sharing the open drain output so that the memory controller can receive notification signals from multiple modules using the open drain output. *Id.* (citing Ex. 1014 ¶¶ 18, 72, 109; Ex. 1003 ¶ 244). Petitioner states that a person of ordinary skill in the art would understand that, in the combination, the added training status signals would be at a low logic level over Hazelzet’s open drain output (UE 121) until the related operations are completed for all modules of the system and the gate signals to the transistors of all the open drain circuits in all the modules are low, at which time the signals would be in a high impedance state, indicating completion. *Id.* at 53–54 (citing Ex. 1017, Fig. 4, 5:65–6:12; Ex. 1003 ¶ 245). Petitioner contends the high and low gate signals to the transistors represent “driving the open drain output and the error edge connection to a first state or to a second state.” *Id.* at 54 (citing Ex. 1003 ¶ 245).

Petitioner states that open drain signals would be changed from a high impedance state to a low state as the gate of the transistor changes from a low to a high to indicate the related training operations were in progress, and changed from a low state to a high impedance state as the gate of the transistor driving the signal changes from a high to a low to indicate when the related operations complete in each memory module. *Id.* (citing Ex. 1014, Fig. 4B, ¶¶ 59, 70, 72; Ex. 1017, Fig. 4, 5:65–6:12; Ex. 1015, 8; Ex. 1016, Figs. 4, 6, 3:52–54, 5:51–7:2, 8:24–9:18, 26:30–32, 27:18–21; Ex. 1003 ¶ 246). Petitioner contends each combination therefore satisfies “one of the first state and the second state being a low logic level and the

other one of the first state and the second state being a high impedance state.” *Id.*

Patent Owner does not specifically respond to these arguments. *See generally* Prelim. Resp. Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that Hazelzet and JEDEC or Buchmann teaches this limitation for purposes of institution.

m) Combination of Hazelzet with JEDEC or Buchmann

Petitioner, with supporting testimony from Dr. Alpert, argues there is sufficient motivation to combine Hazelzet with JEDEC or Buchmann. Pet. 32–40. Petitioner argues that the combinations are “merely an arrangement of old elements with each performing the same function it had been known to perform and yielding no more than what one would expect from such an arrangement.” *Id.* at 33. Petitioner contends the combinations “would have been well within the level of ordinary skill in the art” and “would not have resulted in any unpredictable results.” *Id.*

Petitioner also provides arguments for why a person of ordinary skill in the art would be motivated to add training, to add training as a separate mode, and to use the same output for the added training mode. Pet. 33–40. First, Petitioner argues that a person of ordinary skill in the art would be motivated to add training to Hazelzet “because it was known that training improved memory module reliability” and “to ensure optimal and correct operation.” Pet. 34–35. Second, Petitioner argues that a person of ordinary skill in the art would be motivated to add training in a separate mode from normal operation “because it was known that training before normal

operation was necessary to minimize errors” in read and write operations. *Id.* at 37–38. Third, Petitioner argues that a person of ordinary skill in the art would be motivated to use the same output for the added training mode because (1) Hazelzet and JEDEC both use the same open drain output in two different modes; and (2) “multiple use of a pin was known, and would have been considered an efficient use of the limited number of output pins on integrated circuits.” *Id.* at 38–39.

Patent Owner contends that a person of ordinary skill in the art would not have combined Hazelzet with JEDEC or Buchmann to arrive at the ’595 patent’s claims. Prelim. Resp. 19–58. First, Patent Owner contends that the Petition fails to demonstrate “(1) motivation to *redesign* Hazelzet’s memory module to add JEDEC’s or Buchmann’s memory buffer to buffer the data signals in addition to the address and control signals, and/or how such proposed combinations could be done in Hazelzet’s system architecture.” *Id.* at 27 (*italics original*).

Patent Owner does not explain sufficiently why redesigning Hazelzet’s memory module to buffer data and strobe signals as well as address and control signals “was uniquely challenging or difficult for one of ordinary skill in the art” in view of JEDEC’s and Buchmann’s teachings. *Leapfrog Enterprises, Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1162 (Fed. Cir. 2007). Patent Owner’s argument (Prelim. Resp. 17–18) relies on Dr. Alpert’s testimony that a buffer would be required for data and strobe signals as well as address and control signals to implement Hazelzet’s RDIMM as JEDEC’s LR DIMM, but Dr. Alpert explains this is what JEDEC teaches. Ex. 2002, 78:6–79:19. Thus, Patent Owner’s argument attacks Hazelzet alone without considering what its combination with

concepts taught by JEDEC or Buchmann would have signified to a person of ordinary skill in the art. “Non-obviousness cannot be established by attacking references individually where the rejection is based upon the teachings of a combination of references.” *In re Merck & Co.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986) (citing *In re Keller*, 642 F.2d 413, 425 (CCPA 1981)).

Patent Owner contends that Petitioner’s reasons of “increased performance and capacity” for upgrading Hazelzet’s RDIMM to the LRDIMM of JEDEC and Buchmann are conclusory. Prelim. Resp. 29–35; Pet. 35. However, Hazelzet explicitly mentions its objectives as a “high density and enhanced reliability memory solution at low cost.” See Ex. 1014 ¶ 7. Patent Owner does not explain why Hazelzet’s enhanced reliability may not be equivalent to increased performance, or why Hazelzet’s higher density may not be equivalent to increased capacity.

Patent Owner further states that memory modules that buffered data signals and performed training sequences already existed at the time of Hazelzet. Prelim. Resp. 32 (citing Ex. 2001 ¶¶ 79–80; Ex. 2004 ¶¶ 23–34, Figs. 4–6). Patent Owner seems to be arguing by implication that one would not start by choosing a memory module like Hazelzet’s, which does not have buffered data signals or use training sequences, and then add JEDEC or Buchmann, which do have those features. The potential that there was a better way for a person of ordinary skill in the art to proceed in making a combination does not necessarily mean that Petitioner’s chosen combination is improper.

Patent Owner further argues that Hazelzet “teaches away from replacing its memory modules with increased performance and capacity

memory modules, focusing instead on improving the system reliability in memory modules for ‘low or midrange server markets’ that used ‘simple, relatively inexpensive’ ‘reduced function memory assemblies’ having an ‘adequate level of asset-protection’ and ‘low cost.’” Prelim. Resp. 31 (citing Ex. 1014 ¶¶ 5–7) (emphasis omitted). Patent Owner further contends Hazelzet teaches “eliminating the need to produce or procure two types of buffer devices or to re-design existing memory modules.” *Id.* (citing Ex. 1014 ¶ 14; Ex. 2001 ¶ 71) (emphasis omitted).

Patent Owner’s “teaching away” argument is unpersuasive. Patent Owner has not shown that Hazelzet “criticizes, discredits, discourages” memory modules with increased performance and capacity. *See Galderma Laboratories, L.P. v. Tolmar, Inc.*, 737 F.3d 731, 738 (Fed. Cir. 2013) (a prior art reference does not teach away if it does not criticize, discredit, or otherwise discourage investigation into the invention claimed). Moreover, Hazelzet states that its memory module is “capable of meeting *desired* density, performance and reliability requirements.” Ex. 1014 ¶ 7 (italics added). Hazelzet thus provides the designer freedom to select density, performance, and reliability according to the designer’s requirements, which may encompass *increased* performance and capacity. Accordingly, it is reasonable in view of Hazelzet’s teaching that Petitioner relies on increased performance and capacity as motivation to combine Hazelzet with JEDEC or Buchmann. Pet. 35.

Patent Owner further argues that Hazelzet’s controller does not have the capability to perform address mirroring. Prelim. Resp. 34 (citing Ex. 2001 ¶ 84). Patent Owner also contends there are numerous problems with LRDIMMs such as complication of memory configuration, mismatch

of signals between host and memory interface, reduced timing margins, and others, that Petitioner does not address. *Id.* As Petitioner has not yet been afforded the opportunity to address these issues, we reserve opinion on these issues pending development of a full record at trial. Briefing would be most helpful for issues that have a bearing on features recited in the '595 patent's claims.

Patent Owner contends that Dr. Alpert's declaration in this preliminary proceeding has changed relative to his declaration in IPR2020-01042. Prelim. Resp. 35–37. Specifically, Patent Owner contends that, unlike his declaration in IPR2020-01042, Dr. Alpert's declaration in this proceeding first modifies Hazelzet's memory module to buffer the data lines, like JEDEC or Buchmann, before adding JEDEC's or Buchmann's training to compliment the power-up process as part of Hazelzet's initialization. *Id.* Patent Owner contends this changed argument constitutes hindsight reasoning. Patent Owner's argument does not address that Petitioner's motivation to add training was “because it was known that training improved memory module reliability” and “to ensure optimal and correct operation.” Pet. 34–35. Assuming that these motivations to add training apply, as we do on this record, Patent Owner does not explain adequately why modifying the memory module to buffer data lines to implement training sequences, as taught by JEDEC or Buchmann, would amount to hindsight.

Patent Owner further argues the Petition fails to demonstrate “(2) motivation to *then add* the kind of alleged training in JEDEC or Buchmann to such redesigned memory module to implement as part of an entirely new type of initialization using JEDEC's or Buchmann's training

sequences in addition to Hazelzet's other disclosed operations." Prelim. Resp. 27. Patent Owner contends that Petitioner's combinations are inoperable, and that Petitioner provided no evidence that adding an entirely new mode of operation would have been obvious and "straightforward." *Id.* at 38. According to Patent Owner, adding a new mode of operation would require substantial reconstruction and redesign of Hazelzet, and extensive testing. *Id.* at 38–39 (citing *In re Ratti*, 270 F.2d 810, 813 (CCPA 1959) (holding combination improper under § 103 due to substantial reconstruction and redesign of elements and change of basic principles under which a reference was designed to operate)). Patent Owner also contends Petitioner did not substantiate its assertion that it would have been well within the level of skill at the time to modify Hazelzet's ECC/Parity register to implement the alleged training as a new initialization mode. *Id.* at 39–40.

Patent Owner fails to consider Petitioner's arguments that, according to the combinations, a person of ordinary skill in the art would be guided by the teachings of JEDEC or Buchmann in adding a training mode to Hazelzet. Patent Owner's arguments focus on what Hazelzet teaches, and do not take into account what Petitioner's combination of Hazelzet with JEDEC or Buchmann would have signified to a person of ordinary skill in the art. See *Keller, supra*. Consequently, we find Patent Owner's arguments unpersuasive.

Patent Owner also argues that Hazelzet's error code correction (ECC) and parity and JEDEC/Buchmann training are fundamentally different solutions to different problems in memory modules. Prelim. Resp. 40–45. Patent Owner explains that training synchronizes data transfer with a clock signal to prevent data errors, whereas ECC and parity are used to detect and

correct errors in data already sent. *Id.* at 38–39. Patent Owner argues Hazelzet uses parity to enhance system performance and ECC to enhance reliability. *Id.* at 42. Patent Owner argues since Hazelzet chose to use ECC and parity among many possible solutions, one would not have been motivated to combine JEDEC/Buchmann training. *Id.* at 43.

Again, Patent Owner looks at Hazelzet in isolation without considering what a person of ordinary skill in the art would have understood from not only Hazelzet, but JEDEC’s and Buchmann’s teachings as well. *See Keller, supra.* Hazelzet states its objectives are to provide a memory module with “desired density, performance and reliability requirements.” *See Ex. 1014 ¶ 7.* A skilled artisan would thus be led not only toward the solutions taught in Hazelzet for achieving those objectives, but also toward solutions like JEDEC’s and Buchmann’s training as different ways of achieving those same objectives. *See Ruiz v. A.B. Chance Co.*, 357 F.3d 1270, 1276–77 (Fed. Cir. 2004) (motivation to combine may be found in nature of problem to be solved, leading one to look to references relating to possible solutions to that problem). Nor do we agree that Petitioner’s combination is the result of hindsight (*see Prelim. Resp.* 44–45) as once the desirability of adding training is recognized to achieve Hazelzet’s objectives, Patent Owner does not show why modifying the ECC/parity register to perform training or adding a data buffer would have been “uniquely challenging or difficult for one of ordinary skill in the art.” *See Leapfrog, supra.*

Patent Owner additionally argues that the Petition fails to demonstrate “(3) a teaching or suggestion as to how to then configure the new patched-up memory module to report completion of the newly inserted training

sequences using Hazelzet’s pre-transformed architecture and UE line.”

Prelim. Resp. 27. Patent Owner argues that “Hazelzet expressly teaches away from using its UE line during initialization—teaching instead to use a bus.” *Id.* at 48. Patent Owner further argues that JEDEC has no UE line, and although Buchmann has a UE line, both JEDEC and Buchmann use a bus to communicate training signals. *Id.*

Petitioner asserts that Hazelzet teaches to share an open drain output to receive notification signals from multiple modules using the open drain output (the UE 121 pin). Pet. 53 (citing Ex. 1014 ¶¶ 18, 72, 109; Ex. 1003 ¶ 244). Hence, Petitioner uses the UE pin not because it indicates uncorrectable errors, but because it is an open drain output connected to multiple memory modules. Patent Owner does not acknowledge or address the stated reason why Petitioner uses the UE 121 pin in its combination. We do not discern any flaw in Petitioner’s motivation to combine.

Patent Owner further contends that “the proposed Hazelzet/Buchmann combination, specifically, further fails because there is simply no teaching or suggestion to provide information related to one or more training sequences by driving the open drain output to a first or second state, and/or to output signals related to one or more training sequences using an open drain output, which is required by the independent claims of the ’595 patent.” Prelim. Resp. 27–28. As noted, Petitioner contends that a person of ordinary skill in the art would have been motivated to use that same output for the added training mode because (1) Hazelzet and JEDEC both use the same open drain output in two different modes; and (2) “multiple use of a pin was known, and would have been considered an efficient use of the limited number of output pins on integrated circuits.” Pet. 38–40. Patent Owner

does not address Petitioner's reasons for combining the references or demonstrate why they may be incorrect.

On the current record, we are persuaded that Petitioner has provided sufficient reasoning to combine Hazelzet with JEDEC or Buchmann. Petitioner has provided the motivation to add JEDEC's or Buchmann's training to Hazelzet in order to improve reliability. Pet. 33–36 (citing Ex. 1014 ¶¶ 1–4, 7, 42, 44, 123; Ex. 1015, 3, 8–9; Ex. 1027, 1:35–2:12; Ex. 1025, 15–18; Ex. 1017, 12:36–53; Ex. 1003 ¶¶ 172–178). Petitioner has also provided sufficient evidence that adding buffering to data signals was a known, reliable technique to improve performance and increase capacity. *Id.* at 35–36 (citing Ex. 1016, Fig. 1; Ex. 1003 ¶¶ 175–177, 179). Petitioner further provides evidence that adding training in an initialization mode before normal operation was necessary to minimize errors and ensure correct read and write operations. *Id.* at 37 (citing Ex. 1014 ¶ 123; Ex. 1015, 3, 8, 9; Ex. 1025, 15–18; Ex. 1022, Fig. 4, ¶¶ 32, 52, 88–89; Ex. 1027, 1:61–2:19, 6:24–25, 10:24–45; Ex. 1056, 18, 22, 25–26, 42–44; Ex. 1057, Fig. 5, Abstract, 2:13–34, 2:60–3:3, 9:11–10:44; Ex. 1003 ¶¶ 180–181). Petitioner further sets forth motivation to communicate training status in an initialization mode using the same open drain output used in other modes/operations. *Id.* at 38–40 (Ex. 1003 ¶¶ 183–185; Ex. 1014, Figs. 4B, 7A, ¶¶ 18, 44, 49, 59, 64, 69, 72, 109; Ex. 1015, 8; Ex. 1036, 9; Ex. 1017, 1:16–22, 5:49–57, 5:65–6:8–18, Fig. 4; Ex. 1022 ¶¶ 4–5, 32–33, 52; Ex. 1043, 7:30–51).

Patent Owner contends that substantial reconstruction and redesign of Hazelzet would be required for upgrade with JEDEC's or Buchmann's training. Pet. 38; Ex. 2001 ¶¶ 90–93. Although Petitioner's declarant

identifies a number of considerations for a redesign Hazelzet to accommodate JEDEC's or Buchmann's training, Patent Owner does not provide an indication of why these modifications would not have been implementable by a person of ordinary skill in the art. The parties may wish to further address these issues during trial.

n) Conclusion for Claim 1

In light of the foregoing discussion, we determine that the information presented in the Petition, and accompanying exhibits and testimony, shows that there is a reasonable likelihood that Petitioner would prevail with respect to claim 1 challenged in the Petition. Petitioner makes a sufficient showing that each limitation of claim 1 is taught or suggested by the combination of Hazelzet and JEDEC or Buchmann, and that a person of ordinary skill in the art had reason to combine the references, with a reasonable expectation of success in arriving at the memory module of claim 1.

5. Analysis of Independent Claim 10

Claim 10 is similar to claim 1 except that it requires the module controller to be “configurable to drive the open drain output from a first state to a second state and from the second state to the first state.” Ex. 1001, 16:8–11. Petitioner contends this limitation is disclosed by Hazelzet's teaching that open drain signals would be low logic levels to indicate the training sequence (MB-DRAM/TS0 or TS3) was in progress, or in a high-impedance state to indicate the training sequence has been completed in all memory modules. Pet. 61–62 (citing Ex. 1014, Figs. 4B–5, ¶¶ 59, 70, 72, 76; Ex. 1003 ¶¶ 147–152, 157, 302, 305).

We have reviewed Petitioner’s evidence, and find that it presents a reasonable likelihood that Petitioner would prevail with respect to claim 10 as challenged in the Petition.

6. *Analysis of Independent Claim 17*

Claim 17 is a method claim reciting similar features as the memory module of claim 1. We have reviewed Petitioner’s evidence (Pet. 64–65) and find that it presents a reasonable likelihood that Petitioner would prevail with respect to claim 17 as challenged in the Petition.

7. *Analysis of Independent Claim 21*

Claim 21 is similar to claim 1 in many respects but recites a “module controller including a transistor having a gate and an open drain output coupled to the error edge connection.” Ex. 1001, 18:17–19. Claim 21 further recites that the DRAM elements “are configurable to communicate one or more N-bit-wide data signals . . . where N is at least 32.” We find no express mention of these features in the combination of Hazelzet and JEDEC, and we decline to reach the question of whether a reasonable likelihood of unpatentability has been presented for these claims.

8. *Dependent Claims*

Petitioner further contends that the combination of Hazelzet and JEDEC or Buchmann teaches the limitations in dependent claims 2–9, 11–16, 18–20, and 22–24. Pet. 54–61, 63–64. Patent Owner does not specifically respond to these arguments. *See generally* Prelim. Resp.

Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that Hazelzet and JEDEC or Buchmann teaches the limitations of dependent claims 2–9, 11–16, and

18–20 for purposes of institution. Thus, we determine that Petitioner has demonstrated a reasonable likelihood that it will prevail on its assertion that claims 2–9, 11–16, and 18–20 of the ’595 patent would have been obvious over the combination of Hazelzet and JEDEC or Buchmann.

For the reasons stated for independent claim 21, we do not reach the issue of whether Petitioner has shown a reasonable likelihood that dependent claims 22–24 would have been obvious over Hazelzet and JEDEC.

E. Ground 3: Obviousness Over Hazelzet, JEDEC or Buchmann, and Kim

Petitioner, alternatively, contends claims 3–7, 12–14, 20, 22 and 23 would have been obvious over the combination of Hazelzet, JEDEC or Buchmann, and Kim. Pet. 69–74. For the reasons that follow, we are persuaded that the evidence, including Dr. Alpert’s testimony, sufficiently supports Petitioner’s arguments and, therefore, establishes a reasonable likelihood of prevailing with respect to this ground at this stage of the proceeding.

1. Kim (Ex. 1017)

Kim was filed on January 22, 2008, issued on January 22, 2013, and is titled “Providing a Memory Device Having a Shared Error Feedback Pin” and issued on January 22, 2013. Ex. 1017, codes (22), (45), (54). Kim is generally directed to a memory device having a shared error feedback pin. Ex. 1017, 1:6–8. Figure 4, reproduced below, is “a block diagram of a memory module [400] having an error feedback pin that is shared among multiple devices.” *Id.* at 3:13–16.

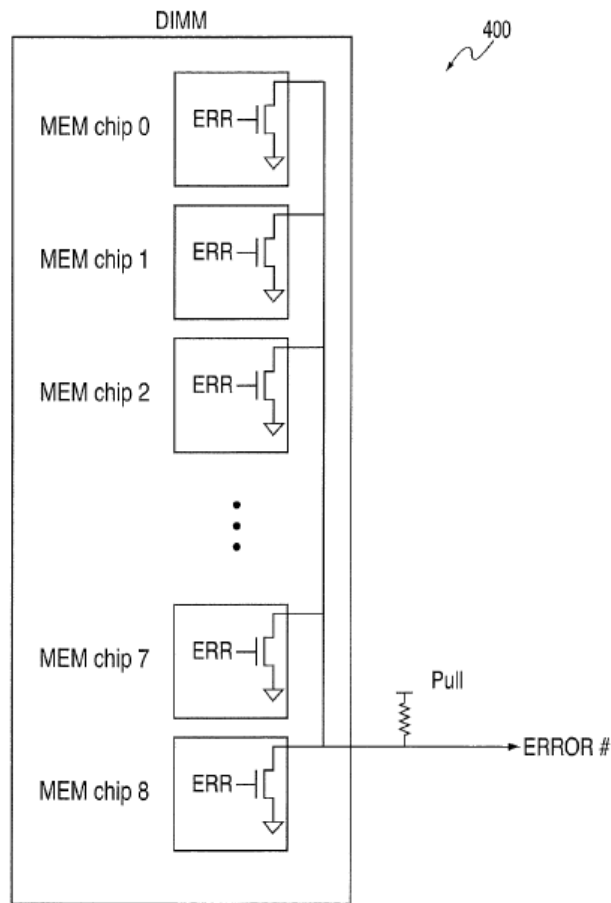


FIG. 4

Figure 4 depicts “the error output line from the memory devices are dotted together via open drain drivers to a single error line that is output from the memory module 400.” *Id.* at 6:1–3.

Figure 5 is reproduced below.

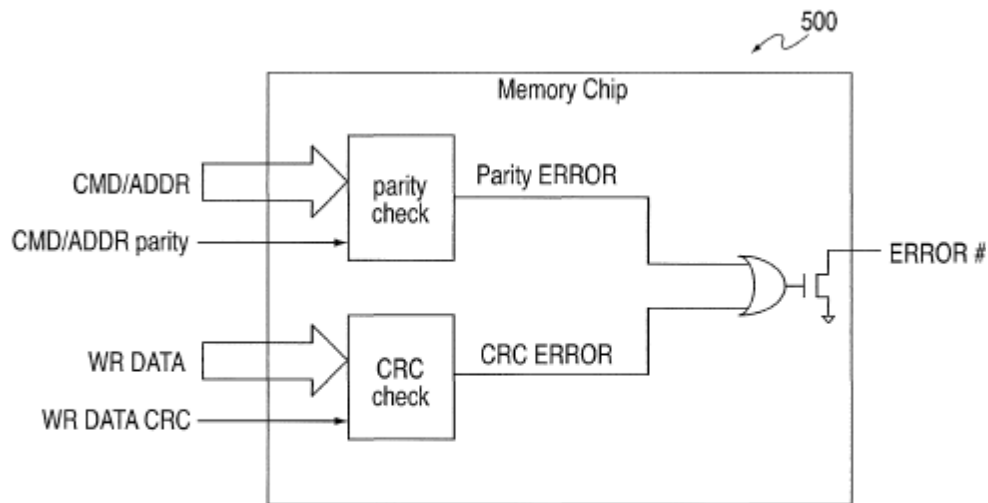


FIG. 5

Figure 5 depicts “a block diagram of a memory device 500 that shares an error feedback pin between data CRC and address parity.” *Id.* at 6:13–15.

2. Analysis

Petitioner contends that Kim teaches an “‘open drain output’ with an output pin coupled to the drain of a transistor, which includes a gate, a source, and a drain.” Pet. 69 (citing Ex. 1017, Fig. 4). Petitioner also contends that Kim discloses “using a logic element (an OR gate) such that multiple error signals could drive the gate of the open-drain transistor.” *Id.* at 70 (citing Ex. 1017, 6:13–18, Fig. 5). Petitioner proposes combining Kim’s “open drain transistor configuration” with Hazelzet’s error logic circuit 100 “such that signals indicating parity mode error, ECC mode error and training status would be provided to a logic gate, such as an OR gate, as in Kim, which would select among them based on the mode of the module, as in Hazelzet.” Pet. 71 (underlining omitted). Petitioner contends the combined circuit would include the transistor configurations recited in

claims 3–5 (Ex. 1003 ¶¶ 265, 276, 283); the multiplexor configuration recited in claims 6, 13, and 22 (Ex. 1003 ¶¶ 161, 180, 196); the open drain training sequence signals of claims 7 and 14 (Ex. 1003 ¶¶ 163, 181; and the transistor signal of claims 12, 20, and 23 (Ex. 1003 ¶¶ 180, 187, 197).

Petitioner contends that a person of ordinary skill in the art would be motivated to combine Kim with Hazelzet and JEDEC or Buchmann because (1) Kim is assigned to the same company as Hazelzet and includes some of the same disclosures, and additional details concerning use of an open-drain output to notify the memory controller of errors during parity and ECC normal operating modes (Ex. 1017, 1:16–22, 5:49–57, 6:8–16); (2) using the output-pin scheme of Kim in the system of Hazelzet would have been “the use of known techniques for their known purposes to achieve predictable results, i.e., using an open-drain output to provide error or status information from multiple components” (Ex. 1003 ¶ 257); (3) “it represented a well-known (and therefore reliable) and simple technique to provide error and/or status information from a number of components and in different modes” (Ex. 1014 ¶¶ 72, 122]; Ex. 1017, Figs. 4–5, 5:65–6:18, 12:18–23; Ex. 1003 ¶ 152); (4) it would “simplify[] the design of the system and sav[e] pins on the various integrated circuits connected to the bus” (Ex. 1003 ¶¶ 251, 268–270, 330–335, 353, 372, 374). *Id.* at 73–74.

Patent Owner does not specifically respond to these arguments. *See generally* Prelim. Resp. Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that Hazelzet in combination with JEDEC or Buchmann and Kim teaches the limitations in claims 3–6, 10–12, and 17–20 for purposes of institution. Thus, we determine that Petitioner has demonstrated a reasonable likelihood

that it will prevail on its assertion that claims 3–7, 12–14, and 20 of the '595 patent would have been obvious over the combination of Hazelzet and JEDEC or Buchmann and Kim.

For the reasons stated for independent claim 21, we do not reach the issue of whether Petitioner has shown a reasonable likelihood that dependent claims 22 and 23 would have been obvious over Hazelzet, JEDEC and Kim.

V. CONCLUSION

After considering the evidence and arguments presented in the Petition, Preliminary Response, Reply, and Sur-Reply, we determine that Petitioner has established a reasonable likelihood of prevailing on its assertion that at least one claim of the '595 patent is unpatentable. Accordingly, we institute an *inter partes* review on all the challenged claims and all of the grounds presented in the Petition. At this stage of the proceeding, we have not made a final determination as to the patentability of these challenged claims.

VI. ORDER

In consideration of the foregoing, it is hereby

ORDERED that pursuant to 35 U.S.C. § 314, *inter partes* review is instituted as to the challenged claims of the '595 patent with respect to all grounds of unpatentability presented in the Petition; and

FURTHER ORDERED that *inter partes* review is commenced on the entry date of this Order, and pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial.

IPR2022-00064
Patent 10,474,595 B2

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