

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

SAMSUNG ELECTRONICS CO., LTD.,	)	
SAMSUNG SEMICONDUCTOR, INC. and	)	
SAMSUNG ELECTRONICS AMERICA,	)	
INC.,	)	
	)	
Plaintiffs,	)	C.A. No. _____
	)	
v.	)	DEMAND FOR JURY TRIAL
	)	
NETLIST, INC.,	)	
	)	
Defendant.	)	

**COMPLAINT FOR DECLARATORY JUDGMENT OF
NON-INFRINGEMENT; BREACH OF CONTRACT**

Plaintiffs Samsung Electronics Co., Ltd. (“SEC”), Samsung Semiconductor, Inc. (“SSI”) and Samsung Electronics America, Inc. (“SEA,” and together with SEC and SSI, “Samsung”) seek a declaration that Samsung does not directly or indirectly infringe United States Patent No. 11,880,319 (the “’319 patent”) (Exhibit 1), either literally or under the doctrine of equivalents; and, alternatively, a ruling that Defendant Netlist, Inc. (“Netlist”) has breached contractual obligations owed to Samsung, including obligations to license its allegedly essential ’319 patent to Samsung and its affiliates on reasonable and non-discriminatory (“RAND”) terms and conditions, as follows:

NATURE OF THE ACTION

1. This is an action for a declaratory judgment and breach of contract arising under the patent laws of the United States, Title 35 of the United States Code, and the Declaratory Judgment Act, 28 U.S.C. § 2201 *et seq.*, and state contract law.

2. This action arises out of Netlist’s repeated assertions of patents against Samsung after Netlist unilaterally attempted to terminate an agreement in which Netlist granted Samsung a perpetual, paid-up, worldwide license to Netlist patents, including the ’319 patent. The U.S. Patent and Trademark Office (“Patent Office”) recently invalidated, in *inter partes* reviews filed by Samsung, all claims of two patents that Netlist accused Samsung of infringing in a related action in this Court. *Samsung Elecs. Co., Ltd. v. Netlist, Inc.*, No. 1:21-cv-1453-RGA-JLH (D. Del.) (“Delaware -1453 Litigation”). Netlist missed the deadline to appeal these decisions, and the Patent Office rejected Netlist’s request to excuse its failure to file timely appeals. Although the Patent Office’s rulings will prevent Netlist from pursuing its infringement claims against Samsung on those two patents, Netlist recently obtained a continuation patent—the ’319 patent—from the same patent family as the invalidated patents.

3. Samsung seeks a declaratory judgment that it does not infringe the ’319 patent. Alternatively, Samsung seeks relief for Netlist’s breaches of contractual obligations owed to Samsung, including obligations to license the ’319 patent to Samsung and its affiliates on RAND terms and conditions. Netlist has insisted that patents in the same family as the ’319 patent are necessarily infringed by the practice of certain standards promulgated by the Joint Electron Device Engineering Council (“JEDEC”) and implemented by the Samsung memory modules at issue in this case. Netlist’s position on the essentiality of these related patents would likewise apply to the ’319 patent.

THE PARTIES

4. Samsung Electronics Co., Ltd. is a corporation organized and existing under the laws of the Republic of Korea, with its principal place of business at 129, Samsung-ro, Yeongtong-gu, Suwon-si, Gyeonggi-do, 443-742, Republic of Korea.

5. Samsung Semiconductor, Inc. is a corporation organized and existing under the laws of the State of California, with its principal place of business at 3655 North First Street, San Jose, California 95134.

6. Samsung Electronics America, Inc. is a corporation organized and existing under the laws of the State of New York, with its principal place of business located at 85 Challenger Road, Ridgefield Park, New Jersey 07660.

7. On information and belief, Netlist, Inc. is a corporation organized and existing under the laws of the State of Delaware, with its principal place of business at 175 Technology Drive, Suite 150, Irvine, California 92618.

JURISDICTION AND VENUE

8. This Court has subject matter jurisdiction over the claim for declaratory judgment of non-infringement (Count I) under 28 U.S.C. §§ 1331, 1338(a), and 2201(a).

9. This Court has subject matter jurisdiction over the breach of contract claim (Count II) pursuant to 28 U.S.C. § 1367. The breach of contract claim forms part of the same case or controversy as the claims for declaratory judgment of non-infringement asserted by Samsung in this action.

10. This Court has personal jurisdiction over Netlist, a corporation organized and existing under the laws of the State of Delaware.

11. Venue is proper in this District under 28 U.S.C. § 1391(b)–(c) because Netlist is subject to personal jurisdiction in this District. In addition, this action arises in part out of Netlist’s allegations in a related case in this District that Samsung infringes two patents related to the ’319 patent.

12. An immediate, real, and justiciable controversy exists between Samsung and Netlist as to whether Samsung has infringed the ’319 patent.

13. For example, shortly after Netlist unilaterally declared that Samsung was no longer licensed to Netlist's patent portfolio, Netlist issued a "Notice of Infringement" letter to Samsung, in which Netlist asserted that certain Samsung memory modules infringe, among others, U.S. Patent Nos. 9,858,218 (the "'218 patent") and 10,474,595 (the "'595 patent"). The '319 patent is in the same family as, and claims priority to, the '595 and '218 patents. The '319 patent is a continuation of United States Patent No. 11,386,024 ("the '024 patent"), which is a continuation of the '595 patent, which is a continuation of the '218 patent.

14. On October 15, 2021, Samsung filed a declaratory judgment action against Netlist in the District of Delaware seeking a declaration that, *inter alia*, the same Samsung products at issue in this case, Load-Reduced Dual Inline Memory Modules ("LRDIMMs") and Registered Dual Inline Memory Modules ("RDIMMs"), do not infringe the '218 and '595 patents. Delaware -1453 Litigation, D.I. 1. Netlist moved to dismiss Samsung's declaratory judgment claims for lack of jurisdiction, arguing that no case or controversy existed because there was no imminent threat of Netlist filing suit against Samsung on the '218 and '595 patents. *Id.*, D.I. 11 at 3–4. The court concluded that there was jurisdiction on the '218 and '595 patents, *id.*, D.I. 37 at 4–5, and Netlist subsequently counterclaimed for infringement of both patents, *id.*, D.I. 40.

15. On October 15, 2021, Samsung filed for *inter partes* review ("IPR") of the '218 and '595 patents with Patent Trial and Appeal Board ("PTAB"). IPR2022-00062; IPR2022-00064. On May 8 and 9, 2023, the PTAB issued its Final Written Decisions for the '218 and '595 patents, finding all claims in both patents unpatentable. IPR2022-00062, Paper No. 54; IPR2022-00064, Paper No. 54. Netlist attempted to appeal the Final Written Decisions—and continue to pursue its infringement claims—but missed the deadline to appeal. Netlist requested that the PTAB

allow Netlist's belated appeal, IPR2022-00062, Paper No. 55; IPR2022-00064, Paper No. 56, but the PTAB rejected Netlist's arguments.

16. On October 2, 2023, Netlist's counsel in the Delaware -1453 Litigation sent an email to Samsung's counsel proposing the filing of (a) "[a]n unopposed motion to dismiss the '218 and '595 patents" from that litigation and (b) a stipulated motion to dismiss the appeals of the PTAB's Final Written Decisions on both patents.

17. On December 20, 2021, the same day Netlist moved to dismiss Samsung's declaratory judgment claims in the Delaware -1453 Litigation for lack of subject matter jurisdiction, Netlist began a patent litigation campaign against Samsung in the U.S. District Court for the Eastern District of Texas, alleging that some of the same Samsung memory modules at issue in the Delaware -1453 Litigation and in this case infringed three other Netlist patents. *Netlist, Inc. v. Samsung Elecs. Co., Ltd. et al.*, No. 2:21-cv-463-JRG (E.D. Tex.) (the "EDTX I Action"), D.I. 1 ¶ 36. Netlist amended its complaint in the EDTX I Action to allege infringement of additional patents.

18. Netlist later filed a second infringement suit against Samsung in the Eastern District of Texas, asserting patents that Netlist had not asserted in the EDTX I Action. *Netlist, Inc. v. Samsung Elecs. Co., Ltd. et al.*, No. 2:22-cv-293-JRG, D.I. 1 (E.D. Tex.) (the "EDTX II Action"). Netlist alleged that the same Samsung memory modules at issue in the Delaware -1453 Litigation and in this case infringed certain Netlist patents. *See id.* D.I. 12 ¶ 34. In both the EDTX I Action and the EDTX II Action, Netlist relied on JEDEC LRDIMM and RDIMM standards to allege infringement. *See, e.g.*, EDTX I, D.I. 1 ¶ 46 (relying on "JEDEC JESD82-32A Standard"); EDTX II, D.I. 12 ¶ 45 (relying on "JEDEC 82-32A Data Buffer Standard").

19. Netlist has also filed suit against Samsung in Germany, asserting two patents against some of the same products at issue in this case. *Netlist, Inc. v. Samsung Electronics Co., Ltd.*, No. 4c O 31/22, 4c O 45/22 (Düsseldorf Regional Court).

20. Netlist previously asserted the '218 and '595 patents in litigation against a competitor of Samsung, SK hynix, alleging that the same type of memory modules at issue in the Delaware -1453 Litigation and in this case infringed the '218 and '595 patents.

21. Netlist has also recently asserted patents in multiple litigations against Micron Technology, Inc. and its affiliates (collectively, "Micron"), which are competitors of Samsung with respect to at least certain of the memory products at issue. *Netlist, Inc. v. Micron Tech., Inc. et al.*, No. 6:21-cv-430 (W.D. Tex.) (the "Micron -430 Litigation"); *Netlist, Inc. v. Micron Tech., Inc. et al.*, No. 6:21-cv-431 (W.D. Tex.) (the "Micron -431 Litigation"); *Netlist, Inc. v. Micron Tech., Inc. et al.*, No. 2:22-cv-203-JRG (E.D. Tex.) (the "Micron -203 Litigation"); *Netlist, Inc. v. Micron Tech., Inc. et al.*, No. 2:22-cv-294-JRG (E.D. Tex.) (the "Micron -294 Litigation"). Netlist also filed suit against Micron in Germany.

22. Netlist has also filed infringement suits against Google, LLC ("Google") in the Northern District of California, *Netlist, Inc. v. Google LLC*, No. 3:090-cv-05718-RS (N.D. Cal.), and in Germany.

23. Furthermore, between May 2020 and the present, Netlist has made demands that Samsung take a second license to Netlist's portfolio of patents based on Netlist's claim that it terminated the fully paid-up, worldwide patent license granted in the Agreement.

24. Netlist has continued to prosecute patent applications in the same family as the '319, '024, '218, and '595 patents on similar subject matter. For instance, on January 16, 2024,

Netlist filed U.S. Patent Application No. 18/413,017, which is a continuation application of the '319 patent.

25. Accordingly, as set forth herein, Netlist has sought to enforce patents in the same patent family as the '319 patent against Samsung products currently being sold and used throughout the United States, and Netlist has accused the same Samsung products of infringing additional patents not related to the '319 patent. Netlist's unsuccessful attempt to appeal the PTAB's Final Written Decisions invalidating the '218 and '595 patents demonstrates Netlist's intent to continue asserting patents in this same family, which includes the '319 patent, against Samsung notwithstanding the PTAB's findings of invalidity. Netlist's prosecution of the application that led to the issuance of the '319 patent and filing of a continuation application of the '319 patent further suggests that Netlist's patent campaign against Samsung concerning this patent family is not over.

26. Because this action presents an actual controversy with respect to the '319 patent, the Court may grant the declaratory relief sought pursuant to 28 U.S.C. § 2201 *et seq.*

BACKGROUND

A. Netlist's Extraordinary License Demand and Infringement Threats

27. On November 12, 2015, Netlist and SEC entered into a Joint Development and License Agreement (the "Agreement"). The Agreement contains cross-license, joint development, and product supply provisions.

28. In the Agreement, Netlist granted SEC and its subsidiaries, including SSI and SEA, a perpetual, paid-up, worldwide, non-exclusive license to all patents owned or controlled by Netlist or any of its subsidiaries having an effective first filing date on or prior to November 12, 2020. The license extends through the expiration of the last to expire of the licensed patents.

29. SEC similarly granted Netlist and its subsidiaries a perpetual, paid-up, worldwide, non-exclusive license to all patents owned or controlled by SEC or any of its subsidiaries having an effective first filing date on or prior to November 12, 2020.

30. The Agreement required SEC to make a payment to Netlist of \$8 million subject to the terms and conditions therein. SEC made this payment to Netlist, except for a portion that was remitted as tax withholding to the Korean tax authorities, which later refunded the withheld portion to Netlist.

31. Since 2020, Netlist has taken extraordinary actions to back out of its grant of a patent license to Samsung.

32. On May 27, 2020, Netlist's Chief Licensing Officer, Marc J. Frechette, wrote to Mr. Seung Min Sung of SEC, and alleged that Samsung materially breached the Agreement by "repeatedly fail[ing] to fulfill Netlist's request for NAND and DRAM products throughout the term of the Agreement" and, allegedly, by improperly deducting withholding taxes. Netlist did not allege, and has never alleged, that Samsung breached the Agreement in any way related to the patent cross-license. In the same letter—which was the first time Netlist raised its breach allegations—Mr. Frechette informed Mr. Sung that Netlist had filed a complaint in U.S. District Court for the Central District of California with respect to the alleged breach by Samsung and provided a copy of the complaint for reference.

33. On May 28, 2020, the U.S. District Court for the Central District of California docketed Netlist's breach of contract complaint against SEC. *Netlist Inc. v. Samsung Elec. Co., Ltd.*, No. 8:20-cv-00993-MCS (C.D. Cal.) ("Breach Action").

34. Netlist subsequently wrote to SEC to terminate the Agreement, including the patent license to SEC and its subsidiaries. On July 15, 2020, Netlist's Chief Licensing Officer,

Marc J. Frechette, wrote to Mr. Seung Min Sung of SEC and stated that “Netlist is hereby terminating, effective immediately, the Agreement including the patent license granted to Samsung”

35. One week later, on July 22, 2020, Netlist amended its complaint in the Breach Action, seeking a declaration that the license it granted Samsung, but not the license Samsung granted Netlist, was terminated. In the Breach Action, Netlist sought monetary damages and a declaration “that Netlist has terminated the Agreement pursuant to Section 13.2 and that Samsung’s licenses and rights under the agreement have ceased.”

36. Netlist then issued a “Notice of Infringement” to Samsung and a demand that Samsung take a second license to Netlist’s patents. Specifically, on October 15, 2020, Netlist stated that because it had terminated the Agreement, “Samsung is no longer licensed to any of Netlist’s portfolio of patents.” Netlist further asserted that its patents relate to LRDIMMs and/or RDIMMs. Netlist then alleged: “Despite the termination of the Joint Development and License Agreement, Samsung continues to unlawfully utilize Netlist’s innovations and to infringe Netlist’s patents, including United States Patent Nos. 10,217,523, 10,474,595, and 9,858,218.” Netlist concluded the letter by demanding that “Samsung and its subsidiaries honor third-party intellectual property rights” and engage in “formal licensing discussions.” Netlist further stated that it “reserves all rights and remedies” with respect to the alleged infringement.

37. Netlist resumed its communications with Samsung in 2021. On February 2, 2021, Netlist’s Chief Licensing Counsel, Mr. Marc J. Frechette, indicated by email that Samsung must take a *second* license, coupled with the demand that Netlist “be made whole” for any alleged breach asserted in the Breach Action.

38. Accordingly, Netlist seeks to double-dip, with a demand that Samsung take a second license to Netlist's patents.

39. On October 14, 2021, the court in the Breach Action issued a confidential order granting summary judgment in favor of Netlist on Netlist's Third Claim for Relief, which sought a declaration that Netlist terminated Samsung's license effective July 20, 2020. *See Netlist Inc. v. Samsung Elec. Co., Ltd.*, No. 8:20-cv-00993-MCS, D.I. 186 (C.D. Cal.). The court also granted summary judgment in Netlist's favor that Samsung was liable for certain alleged breaches of other provisions in the Agreement. *See id.*

40. Beginning on December 1, 2021, the court in the Breach Action held a jury trial on damages for one of the alleged breaches, the alleged failure to fulfill Netlist's orders for NAND and DRAM products. On December 3, 2021, the jury returned a verdict in Samsung's favor, finding that Netlist failed to prove that it suffered any damages for this alleged breach. *See Breach Action*, D.I. 276. The court in the Breach Action concluded that Netlist was not entitled to damages for the remaining alleged breach (the withholding of taxes) as a matter of law and awarded to Netlist nominal damages of \$1.00 for each alleged breach (for a total of \$2.00). *Id.*, D.I. 306, ¶¶ 1–2.

41. Despite losing at trial, Netlist issued a press release claiming to be “very pleased with the overall outcome of the case as it confirmed that Samsung no longer has a valid license to Netlist patents and therefore requires a licensing agreement.” Netlist Provides Update on Action in Federal Court Against Samsung, <https://investors.netlist.com/websites/netlist/English/2120/us-press-release.html?airportNewsID=a661884d-0025-46ea-a055-bae8d8e4570b> (last visited October 3, 2023).

42. SEC challenged the summary judgment ruling in the Breach Action on appeal to the Ninth Circuit. *Netlist Inc. v. Samsung Elecs. Co., Ltd.*, Nos. 22-55209 & 22-55247 (9th Cir.). SEC maintained that it did not breach the Agreement, that the Agreement has not been terminated, and that it continues to hold a paid-up, worldwide, non-exclusive license to Netlist's patents, including the '319 patent. Further, regardless of whether the Agreement was properly terminated (which Samsung disputes), Samsung, its customers, and its end users are not liable for infringement of the '319 patent for any memory modules made, used, sold, offered for sale, or imported before July 20, 2020, the date of which the purported termination became effective.

43. The Ninth Circuit agreed that patent cross-licensing was a distinct aim of the JDLA, independent of the joint development project: "[T]he JDLA has two stated purposes: (1) developing a new NVDIMM-P product (i.e., the [joint development project]), and (2) patent cross-licensing. The title and preamble of the agreement exclusively reference these two topics, and each substantive section corresponds entirely to one of the two goals." D.I. 192, Ex. A at 3–4 (emphasis added). The Ninth Circuit remanded the case to (a) resolve an ambiguity in the supply provision in Section 6.2 of the JDLA, and (b) determine whether any breach of that provision by Samsung was material such that Netlist could terminate the agreement. Following the Ninth Circuit's remand, a jury trial was held. On May 17, 2024, the jury issued its verdict, adopting Netlist's proffered meaning of the disputed provision and finding that Samsung's breach of that provision was material. *See* Breach Action, D.I. 556.

B. Netlist's Patent Infringement Lawsuits

44. Over the past decade, Netlist has pursued a litigation campaign against Samsung and other suppliers of JEDEC standard-compliant memory modules, component suppliers, and users of memory modules (aside from Samsung). During this campaign, Netlist has

alleged infringement of numerous patents, including patents related to the '319 patent, based on the practice of JEDEC memory standards.

1. Netlist's Lawsuits Against Samsung

45. As noted above, on October 15, 2021, Samsung filed a declaratory judgment action against Netlist in this District for a declaration that, *inter alia*, certain Samsung LRDIMM and RDIMM products did not infringe the '218 and '595 patents. Delaware -1453 Litigation, D.I. 1. Netlist moved to dismiss Samsung's declaratory judgment claims, arguing that no case or controversy existed because there was no imminent threat of Netlist filing suit against Samsung on the '218 and '595 patents. *Id.*, D.I. 11 at 3–4. Samsung later amended its complaint, *id.*, D.I. 14, and Netlist moved to dismiss Samsung's First Amended Complaint, *id.*, D.I. 24.

46. On August 1, 2022, the court in the Delaware -1463 Litigation denied in part and granted in part Netlist's motion to dismiss Samsung's declaratory judgment claims. The court found jurisdiction on the '218 and '595 patents because, once the Central District of California granted summary judgment in favor of Netlist in the Breach Action, "Netlist's threats became more immediate." *Id.* D.I. 37 at 4. However, the court dismissed, *inter alia*, Samsung's declaratory judgment claim of non-infringement related to U.S. Patent No. 7,619,912 (the "'912 patent"). *Id.*, D.I. 37. The court reasoned that the patent had been "the subject of litigation in [the Northern District of California] for over a decade," so Samsung's declaratory judgment claim regarding that patent in Delaware was not "an efficient use of judicial resources." *Id.* at 6. In reaching its decision, the Court accepted Netlist's argument that Samsung's "collateral action [in Delaware] should be dismissed in favor of the much more advanced Northern District case." *Id.* at 3; *see also id.*, D.I. 11 at 3–5; D.I. 28 at 1–3, 8–10 (Netlist arguing that litigation on the '912 patent should proceed in the Northern District of California).

47. Following the court’s order in the Delaware -1453 Litigation, Netlist counterclaimed against Samsung for infringement of the ’218 and ’595 patents. Netlist alleged that Samsung infringed the ’218 and ’595 patents by making, using, selling, offering to sell, and/or importing DDR4 LRDIMM and DDR4 RDIMM products. *Id.*, D.I. 40, ¶ 30. Netlist alleged that the ’218 and ’595 patents read on the Clock-to-CA training feature described in a JEDEC standard. *Id.*, D.I. 45 ¶¶ 68–74, 87–93. Specifically, Netlist alleged that “the ALERT_n pin of Samsung Accused Instrumentalities is configurable for indicating a parity error while the memory module operates in the first mode (e.g., a normal mode of operation).” *Id.* ¶¶ 63, 80. Netlist also sought treble damages based on Samsung’s alleged willful infringement. *Id.*, D.I. 45 ¶ 101. Netlist subsequently expanded its infringement allegations to include Samsung’s DDR5 products. *Id.*, D.I. 132.1, Ex. 16 at 2.

48. Netlist later asserted counterclaims against Google in the Delaware -1453 Litigation for infringement of, *inter alia*, the ’218 and ’595 patents. *Id.*, D.I. 45. Netlist’s infringement allegations relate to Google’s use of Samsung’s LRDIMM and RDIMM products.

49. On December 20, 2021, Netlist filed a lawsuit against SEC, SSI, and SEA in the Eastern District of Texas alleging direct and indirect infringement of three patents. EDTX I Action, D.I. 1. Netlist alleged that the defendants infringe in connection with the making, selling, using, and/or importing of DDR4 LRDIMM memory modules, *see id.* ¶¶ 40, 53, and DDR5 LRDIMM, RDIMM, SODIMM, and UDIMM memory modules, *see id.* ¶ 68.

50. Netlist filed the EDTX I Action the same day that it moved to dismiss the Delaware Litigation based on, *inter alia*, an alleged lack of any case or controversy over Samsung’s declaratory judgment claims. *See* Delaware -1453 Litigation, D.I. 11 at 3 (arguing that the case did not involve a “substantial controversy of sufficient immediacy”).

51. Netlist's Complaint in the EDTX I Action stated that Netlist intended to assert against Samsung a patent resulting from a then-pending patent application once it issued from the Patent Office. *See* EDTX I Action, D.I. 1 ¶ 32. The application issued on January 25, 2022, and Netlist subsequently amended its complaint to include the newly issued patent and two additional patents. *Id.*, D.I. 23.

52. Netlist also filed a second suit against Samsung in Texas. The same day the court in the Delaware -1453 Litigation dismissed Samsung's declaratory judgment claims involving the '912 patent—reasoning that litigating the patent in the Northern District of California would be the most efficient use of judicial resources—Netlist filed suit against Samsung on the '912 patent in the Eastern District of Texas. *See* EDTX II Action, D.I. 1. Netlist later amended its complaint to include three additional patents. Netlist alleged that Samsung infringed its patents by making, using, selling, offering to sell, and/or importing DDR4 LRDIMM and DDR4 RDIMM memory modules, the same Samsung LRDIMM and RDIMM memory modules at issue in this action. *Id.* ¶¶ 34.

53. Netlist also filed suit against Samsung in Germany, asserting two patents against Samsung's DDR4 LRDIMM, which is also at issue in this case and the Delaware -1453 Litigation. Delaware -1453 Litigation, D.I. 1. *Netlist, Inc. v. Samsung Electronics Co., Ltd.*, No. 4c O 31/22, 4c O 45/22 (Düsseldorf Regional Court).

54. On October 15, 2021, Samsung filed IPRs on the patents at issue in the Delaware -1453 Litigation, including the '218 and '595 patents. IPR2022-00062; IPR2022-00064. In May 2022, the PTAB found all claims of both the '218 and '595 patents unpatentable in Final Written Decisions. IPR2022-00062, Paper No. 54; IPR2022-00064, Paper No. 54. Netlist attempted to appeal the PTAB's Final Written Decisions for both patents, but Netlist missed the

deadline to file a notice of appeal. Netlist requested that the PTAB allow Netlist's late appeal, IPR2022-00062, Paper No. 55; IPR2022-00064, Paper No. 56, but the PTAB determined that Netlist had failed to demonstrate excusable neglect for missing the deadline.

2. Netlist's Lawsuits Against Third Parties

55. Netlist has also pursued a litigation campaign against other suppliers of JEDEC standard-compliant memory modules, component suppliers, and users of memory modules. For instance, Netlist engaged in a years-long, multi-forum litigation campaign against SK hynix, a competitor of Samsung. Between 2016 and 2020, Netlist filed six patent infringement suits against SK hynix, the first two in the Central District of California. *See Netlist, Inc. v. SK hynix America Inc. et al.*, No. 8:16-cv-1605 (C.D. Cal. 2016); *Netlist, Inc. v. SK hynix, Inc. et al.*, No. 8:17-cv-1030 (C.D. Cal. 2017). Netlist also filed two complaints against SK hynix with the International Trade Commission. *See In re Certain Memory Modules and Components Thereof, and Products Containing the Same*, No. 337-TA-1023 (U.S.I.T.C. 2016); *In re Certain Memory Modules and Components Therefore*, No. 337-TA-1089 (U.S.I.T.C. 2017). Finally, Netlist filed two infringement suits against SK hynix in the Western District of Texas, *Netlist, Inc. v. SK hynix Inc. et al.*, No. 6:20-cv-194 (W.D. Tex. 2020); *Netlist, Inc. v. SK hynix America. et al.*, No. 6:20-cv-525 (W.D. Tex. 2020).

56. In these suits, Netlist accused SK hynix RDIMM and LRDIMM memory modules of infringing certain Netlist patents—including the '218 and '595 patents—based on the practice of certain JEDEC memory standards.

57. Netlist has also accused Google of infringing the '912 patent in connection with DDR4 LRDIMM and RDIMM products. *See Netlist, Inc. v. Google Inc.*, No. 3:09-cv-05718-RS (N.D. Cal.). Netlist seeks an injunction in that case, which would preclude Google from using

the JEDEC-compliant LRDIMM and RDIMM memory modules supplied by SSI to Google. Netlist also seeks an injunction against Google in the Delaware -1453 Litigation. D.I. 127 at 11.

58. Netlist has also asserted the '912 patent against Inphi, a chip supplier, based on the practice of certain JEDEC memory standards. *See Netlist, Inc. v. Inphi Corp.*, No. 2:09-cv-6900 (C.D. Cal. 2009).

59. As noted above, Netlist has also recently asserted patents in multiple litigations in Texas against Micron, which is a competitor of Samsung with respect to at least certain of the memory products at issue. *See* Micron -430 Litigation; Micron -431 Litigation; Micron -203 Litigation; Micron -294 Litigation. In the Micron litigations, Netlist accuses the same type of memory modules at issue in this case based on implementing the same JEDEC standards.

60. Throughout its litigation campaigns, Netlist has demonstrated a pattern of asserting patents, receiving rulings of noninfringement or invalidity, and then asserting continuations of the non-infringed or invalid patents. For example, Netlist asserted U.S. Patent No. 8,489,837 (the "'837 patent"), a grandparent of the '218 and '595 patents, against SK hynix in district court and at the ITC. *Netlist, Inc. v. SK hynix Inc.*, No. 8:16-cv-01605 (C.D. Cal. Aug. 31, 2016), D.I. 1; *In re Certain Memory Modules*, No. 337-TA-1023 (Sept. 1, 2016), Doc. No. 589609. The PTAB subsequently determined that certain claims of the '837 patent were unpatentable, and the ITC determined that SK hynix did not infringe the '837 patent. *See* IPR2017-00548, Paper No. 25 (May 3, 2018); *In re Certain Memory Modules*, No. 337-TA-1023, 2017 WL 11569255, at *135 (Nov. 14, 2017). Shortly before those rulings were issued, Netlist asserted U.S. Patent No. 9,535,623 (the "'623 patent"), a continuation of the '837 patent, against SK hynix in district court and at the ITC. *Netlist, Inc. v. SK hynix Inc.*, No. 8:17-cv-1030 (C.D. Cal.), D.I. 1; *In re Certain Memory Modules*, No. 337-TA-1089 (Oct. 31, 2017), Doc. No. 627249. The PTAB subsequently determined that all claims of the '623 patent were

unpatentable. *See* IPR2018-00303, Paper No. 42 (Mar. 21, 2019). Netlist then asserted the '218 and '595 patents—which are continuations of the '837 and in the same family as the '623 patent—against SK hynix, *Netlist, Inc. v. SK hynix Inc.*, No. 6:20-cv-00194 (W.D. Tex. June 9, 2020), D.I. 33, essentially seeking a third bite at the apple.

C. Netlist Patents and Standard Essential Allegations

61. As noted above, the '319 patent is a continuation patent of the '024, '218, and '595 patents and all share a common specification. During prosecution, the examiner rejected the then-pending claim of the '319 patent for double patenting over the claims of the '024, '595, and '218 patents. Netlist has asserted that the '218 and '595 patents are essential to one or more of (a) JEDEC standards JESD79-4C, JESD82-31, and JEDEC82-31A, (“the DDR4 Standards”), which were developed by the JEDEC JC-40 committee (JESD82-31), JC-40.4 committee (JESD82-31A), and JC-42.3C committee (JESD79-4C), and (b) JESD301.1, JESD82-511, and JESD79-5 (“the DDR5 Standards”), which were developed by the JEDEC JC-40.1 committee (JESD301.1), JC-40.4 committee (JESD82-511), and JC-42.3 committee (JESD79-5). Netlist has further asserted that the '218 and '595 patents are essential to one or more of the standards encompassed by JESD21-C (together with the DDR4 Standards and the DDR5 Standards, “the JEDEC Standards”).

62. In its October 15, 2020 “Notice of Infringement” letter, Netlist asserted that it owns “over 100 patents and patent applications related to memory technologies,” including LRDIMM and RDIMM, and accused Samsung of infringing the '218 and '595 patents. Further, Netlist has contended in the Delaware -1453 Litigation that the '218 and '595 patents are essential to JEDEC DDR4 LRDIMM and RDIMM and DDR5 RDIMM standards, as Netlist’s infringement contentions mapped various claim limitations to the JEDEC DDR4 and DDR5 Standards and contended that the '218 and '595 patent would necessarily be infringed by any DDR4 LRDIMM

or RDIMM or DDR5 RDIMM products “made, sold, offered for sale, imported and/or used by Samsung that are JEDEC-standard compliant memory modules.” Delaware -1453 Litigation, D.I. 132-1 at 1.

63. Netlist also contended that each of the patents asserted in previous litigation against SK hynix is essential to certain DDR4 Standards. *See Netlist, Inc. v. SK hynix Inc.*, No. 6:20-cv-00194 (W.D. Tex.), D.I. 1, ¶¶ 27, 37; *id.*, D.I. 1-5 (’218 Claim Chart for DDR4 LRDIMM); *id.*, D.I. 1-6 (’218 Claim Chart for DDR4 RDIMM); *id.*, D.I. 1-10 (’595 Claim Chart for DDR4 LRDIMM); *id.*, D.I. 1-11 (’595 Claim Chart for DDR4 RDIMM). In asserting the ’218 and ’595 patents against SK hynix, Netlist’s complaint included claim charts for each patent, in which Netlist similarly mapped various claim limitations to the DDR4 Standards. *See id.*

64. In the present action, Samsung seeks declarations that Samsung’s LRDIMM and RDIMM memory modules that comply with the DDR4 Standards or any standard requiring materially similar functionality (“Samsung DDR4 Memory Modules”), and Samsung’s RDIMM memory modules that comply with the DDR5 Standards or any standard requiring materially similar functionality (“Samsung DDR5 Memory Modules” and together with the Samsung DDR4 Memory Modules, the “Samsung Memory Modules”), do not infringe the ’319 patent.

65. If, as Netlist contends, the ’319 patent is essential to any of the JEDEC Standards (which they are not), Netlist is obligated to license the patent on RAND terms. As discussed below, Netlist has failed to offer such a license to Samsung.

D. Overview of the ’319 Patent

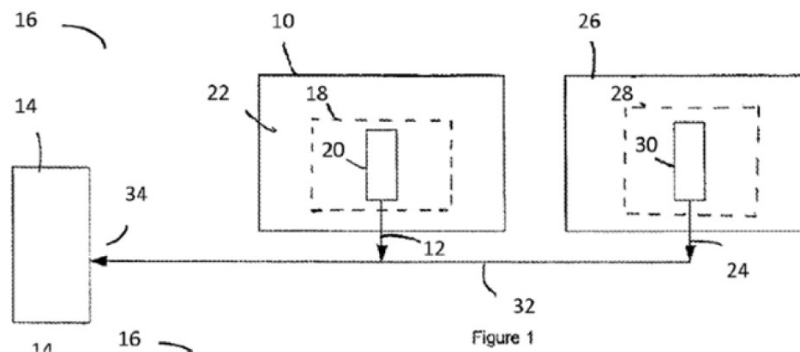
66. The ’319 patent issued on January 23, 2024, from U.S. Appl. No. 17/840,593, which was filed on June 14, 2022. The ’319 patent claims priority to a chain of continuation applications, including the applications leading to the issuance of the aforementioned ’024, ’218, and ’595 patents. The first full patent application was U.S. Appl. No. 12/815,339,

which was filed on June 14, 2010, and claimed priority to a provisional application that was filed on June 12, 2009.

67. The '319 patent describes “a method of establishing a handshake mechanism based on notification signaling” that “can be implemented by adding a new interface (notifying) signal between the MCH [i.e., system memory controller] and the memory subsystem controller,” Ex. 1 ('319 Patent) at 4:6–14, and this interface “can be an open drain signaling from the memory subsystem controller to the MCH.” *Id.* at 4:13–17.

68. According to the '319 patent, “there [was] no existing method of handshaking between the MCH (*e.g.*, system memory controller) and a memory subsystem (*e.g.*, memory module) during initialization.” *Id.* at 2:65–3:1. And “in conventional systems, the system memory controller does not monitor the error-out signal from the memory subsystem.” *Id.* at 3:1–3. The '319 patent states that “[i]n a typical server (*e.g.*, an Intel or AMD or other chipset based server), the lack of any handshaking between the MCH and the memory subsystem during the server initialization period has not been a serious issue since the MCH generally has complete control over the initialization procedure.” *Id.* at 3:4–9.

69. Figure 1 shows a computer system including memory module 10, coupled to a memory controller 14 via “output 12,” which is driven by notification circuit 20 of controller circuit 18.



Id. at 4:24–5:42, FIG. 1. Memory module 26 is also shown, and has essentially the same structure as module 10, having “output 24” driven by notification circuit 30 of controller circuit 28. *Id.* at 9:13–46.

70. In one specific example of handshaking, the interface between the memory controller (MCH) and memory subsystem controller is implemented using a technique called open drain signaling. *Id.* at 4:13–17, 9:47–10:4, Figs. 2–3. Specifically, output 12 of module 10 and output 24 of module 26 are both tied to the same bus 32 using an open drain configured transistor. *Id.*

71. In that configuration, when starting an initialization procedure, each memory module will drive the gate of the transistor of its open drain output high, placing a logic level low (low impedance) signal on bus 32. When the initialization is complete, the memory module can drive the gate of the transistor, placing a logic level high (high impedance) signal on bus 32. However, because all of the outputs of multiple memory modules are tied to the same bus 32 in an open drain configuration, the state of bus 32 will remain logic level low (low impedance) until each memory module drives the gate of the transistor of its open drain output low, placing a logic level high (high impedance) on its output, which then allows “the bus 32 [to] be pulled high by the internal pull-up configuration 40 of the system memory controller 14.” *Id.* at 10:8–15. In this manner, the system memory controller may be provided a notification signal, notifying that the module is currently executing or has completed initialization. *Id.* at 10:15–24.

72. Netlist alleges that the Clock-to-CA training, as described in JESD82-31, practices one or more claims of the ’218 and ’595 patents, the earlier parents to the ’319 patent. Delaware -1453 Litigation, D.I. 40 ¶¶ 57, 59, 74–75, and 78 (Aug. 22, 22) (identifying Clock-to-CA training as one of the accused modes). According to the JEDEC standard, “[i]n Clock-to-CA

training mode the DDR4RCD01 ORs all enabled Dn inputs every other cycle together and loops back the result to the ALERT_n output pin.” Ex. 2 (JESD82-31) at 44 (emphasis in original). “In this mode, the DPAR input is sampled at the same time as the other Dn inputs,” and “[t]he ALERT_n latency relative to the DQn inputs is the same 3 cycles as in the normal parity mode.” *Id.*

73. As explained above, the ’319 patent claims priority to the applications leading to the ’024, ’595, and ’218 patents. Claim 1 of the ’024, ’595, and ’218 patents are directed a “memory module operable with a memory controller of a host system.” All three patents include the same structural elements: “a printed circuit board having edge connections that fit into a corresponding slot of the host system,” “dynamic random access memory elements on the printed circuit board,” and “a module controller on the printed circuit board” with “an open drain . . . coupled to the error edge connection.” In addition, the claims of all three patents require the module controller to use the open drain to indicate a “parity error” during a “normal memory read or write operation” or a signal “related to one or more training sequences” “when the memory module performs operations associated with one or more training sequences.” The allowed claims of the ’319 patent contain the same structural elements and include substantially the same operations.

74. For at least the reasons explained in Count I, the Samsung Memory Modules do not infringe the claims of the ’319 patent.

E. Netlist Has Breached Contractual Obligations Owed to Samsung

1. JEDEC and Semiconductor Memory Standards

75. JEDEC is an independent, non-profit semiconductor engineering trade association and standardization body based in the United States. Over 300 companies in the

computer and electronics industries are currently members of JEDEC, including Samsung and Netlist.

76. JEDEC has become the global leader in developing open standards and publications for a broad range of semiconductor technologies, including memory products. As relevant here, JEDEC develops standards for semiconductor memory chips and modules, including standards implemented by Samsung's products.

77. JEDEC's semiconductor memory standards enable interoperability, *i.e.*, the ability of memory products made by different manufacturers to work together with computer and electronic devices made by others. JEDEC standards are widely implemented, and, for many types of semiconductor memory products, it is imperative that they comply with JEDEC standards in order to be commercially viable.

78. Member companies participate in JEDEC's standard-setting process through over 50 committees and subcommittees that address various technological areas. Through a collaborative process, members contribute to and vote on technical proposals for incorporation into JEDEC standards. Upon committee and board approval, new standards are promulgated and made available to the public.

79. In some cases, JEDEC members own patents covering the technology they or others seek to have included in a JEDEC standard. A patent that includes a claim or claims that would necessarily be infringed by the use, sale, offer for sale, or disposition of a portion of a product in order to be compliant with an industry standard is referred to as a "standard essential patent" or an "SEP."

80. Each owner of an SEP can, unless restrained, demand and obtain exorbitant royalties for the use of its patent, far in excess of the value, if any, that the patented technology

would command had it not been incorporated into a standard. If unwilling to pay such excessive royalties, firms wishing to implement the standard face the risk of being foreclosed from using any portion of the standard, including unpatented and public domain technologies. This threat of foreclosure, if left unchecked, puts a manufacturer's investment in developing standard-compliant products at risk and, in effect, permits the possibility that the SEP holder may capture up to the value of the standard as a whole for each unique implementer, rather than the true value of its specific contribution to the standard, independent of the incorporation of the technology into the standard. The exploitation of SEPs to extract unreasonable or discriminatory royalties is referred to as patent "hold-up."

81. The problem of "hold-up" is exacerbated in the context of standards, like those at issue here, as to which there are large numbers of SEPs and many different firms that claim to hold SEPs. The problem is likewise compounded when the products at issue, like those at issue here, may be required to implement multiple standards. The resulting problem of excessive aggregate royalties is referred to as "royalty stacking."

82. In order to mitigate these risks, JEDEC—like many other standard-setting organizations—has adopted a Patent Policy that seeks to ensure that owners of SEPs license those patents to manufacturers of standard-compliant products on RAND terms and conditions. Every firm that is a member of a JEDEC committee or a participant in a JEDEC committee meeting, including Netlist, agrees to abide by the JEDEC Patent Policy.

All Committee Members, as a condition of committee membership or committee Participation, agree to abide by JEDEC rules and procedures, including this JEDEC patent policy ("Patent Policy").

Ex. 3 (JEDEC Manual No. 21T) § 8.2.2.1.

83. Pursuant to the JEDEC Patent Policy, as a condition of committee membership or participation, all JEDEC committee members agree to disclose “Potentially Essential Patents” relevant to the work of the committee:

All Committee Members must Disclose Potentially Essential Patents, known to their Representative(s) to be Potentially Essential Patents that are owned or controlled by that Committee Member

Id. § 8.2.3.

84. The requirement to disclose “Potentially Essential Patents” extends to disclosing pending patent applications. *Id.* § 8.2.1.

85. JEDEC committee members also agree to license “Essential Patent Claims” on RAND terms and conditions:

All Committee Members, as a condition of committee membership or committee Participation, agree to Disclose Potentially Essential Patents, as set forth more fully in 8.2.3, and to offer to license their Essential Patent Claims to all Potential Licensees on RAND terms and conditions, if and as consistent with 8.2.3 and 8.2.4.

Id. § 8.2.2.1.

86. JEDEC committee members also agree to license on RAND terms any “Essential Patent Claims” included in their patent applications:

For any Essential Patent Claims held or controlled by the entity, pending[,] or anticipated to be filed, which are or may be required to implement a Standard that may result from the JEDEC Standard Activity, the entity hereby makes one of the following commitments: . . . A license will be offered . . . under reasonable terms and conditions that are free of any unfair discrimination.

Id. § 8.2.5 (emphasis added).

87. The JEDEC Patent Policy defines “Potentially Essential Patent” as a patent that is reasonably believed to contain one or more Essential Patent Claims. *Id.* § 8.2.1. “Essential Patent Claim” is further defined as those “Patent claims the use of which would necessarily be

infringed by the use, sale, offer for sale or other disposition of a portion of a product in order to be compliant with the required portions of a final approved JEDEC standard.” *Id.*

88. The JEDEC Patent Policy provides that the disclosure of Potentially Essential Patents “shall be made as early as reasonably possible” and documented by submission to JEDEC of either a “License Assurance/Disclosure Form” or a “Notice of Refusal.” *Id.* § 8.2.3.

89. A License Assurance/Disclosure Form (also known as a “Letter of Assurance” or “LOA”) states that the committee member commits to license its SEPs to all potential licensees on RAND terms. On the contrary, a Notice of Refusal states that the member is not “willing to offer to license Essential Patent Claims . . . on RAND terms to all Potential Licensees.” *Id.* § 8.2.3.1. In order to be effective, any such LOA or Notice of Refusal must be delivered to the JEDEC Legal Department within thirty (30) calendar days of a draft specification’s completion. *Id.*

90. Member companies who disclose and agree to license their patents on RAND terms do so via the aforementioned “LOA” identifying the relevant JEDEC standard(s) and making one of the two following commitments specified by the JEDEC Patent Policy:

For any Essential Patent Claims held or controlled by the entity, pending or anticipated to be filed, which are or may be required to implement a Standard that may result from the JEDEC Standard Activity, the entity hereby makes one of the following commitments:

- (i) *A license will be offered, without compensation, under reasonable terms and conditions that are free of any unfair discrimination to applicants desiring to utilize the license for the purpose of implementing the JEDEC Standard, subject to the terms and conditions in 8.2.4; or*
- (ii) *A license will be offered, to applicants desiring to utilize the license for the purpose of implementing the JEDEC Standard under reasonable terms and conditions that are free of any unfair discrimination, subject to the terms and conditions in 8.2.4.*

Id. § 8.2.5.

91. According to JEDEC's Patent Policy, disclosures and commitments with respect to one patent are deemed to include all patents claiming priority to the same filing. *Id.* § 8.2.1. Committee members are therefore obligated to license on RAND terms later-issuing SEPs that claim priority to patents disclosed to JEDEC.

92. If a committee member who owns or controls patents essential (or potentially essential) to JEDEC standards does not disclose and agree to license them before the ballot closes, or notify the committee of an intention not to license through a "Notice of Refusal," the committee member will be deemed to have agreed to offer licenses on RAND terms:

If a Committee Member, at its discretion, elects not to submit a License Assurance/Disclosure Form (see Annex A.3) at or before the time the ballot closes and does not otherwise provide notice of an unwillingness to license in accordance with 8.2.3.1, the Committee Member and its Affiliates will be deemed to have agreed to offer to grant licenses on RAND terms and conditions for all of its Essential Patent Claims of the balloted Standard, if and as consistent with 8.2.4.

Id. § 8.2.5.

93. The JEDEC Patent Policy provides that it is to be interpreted and governed under the laws of the State of New York. *Id.* § 8.2.10. Although the JEDEC Manual 21 has been updated and amended from time to time, upon information and belief, all of the relevant provisions of the JEDEC Patent Policy have been materially the same at all times relevant hereto.

2. Netlist's RAND Commitments

94. Netlist alleges that it owns over 100 patents and patent applications related to memory technologies.

95. Netlist is also a member of JEDEC and has joined a number of JEDEC technical committees over time. After years of membership in JEDEC, Netlist withdrew from

membership in JEDEC briefly in 2011 after submitting Notices of Refusal for a number of Netlist patents. JEDEC reinstated Netlist later in 2011 following Netlist's submission of LOAs for the same patents Netlist had previously refused to license on RAND terms.

96. Netlist again withdrew from membership in JEDEC committees JC-40, JC-42, and JC-45 in 2015, after submitting notices of refusal for many of its patents. In May 2018, Netlist requested from the JEDEC board of directors that Netlist be reinstated in those committees. The JEDEC board of directors approved the request on the condition that Netlist would agree to be bound by the JEDEC Patent Policy regarding work conducted in JC-40, JC-42, and JC-45 during the time Netlist had not participated in the committees, since and including February 27, 2015. Netlist agreed in writing to the JEDEC board of directors' terms, and JEDEC reinstated Netlist on August 14, 2018, retroactive to February 27, 2015.

97. Upon information and belief, therefore, at the time that the JEDEC Standards were drafted and approved by JEDEC, Netlist was a member, attended the meetings, and/or was deemed a member of the JC-40, JC-42, and JC-45 committees that developed those standards.

98. To date, and on information and belief, Netlist has disclosed that at least 42 of its patents are essential or potentially essential to JEDEC standards.

99. Netlist is obligated to license the '319 patent on RAND terms to implementers of certain DDR4 and DDR5 Standards, to the extent the '319 patent is essential to those standards. In fact, Netlist committed to license the '319 patent on RAND terms to implementers of certain DDR4 Standards. Upon information and belief, Netlist submitted a Letter of Assurance for U.S. Patent No. 8,489,837 (the "'837 patent") on April 7, 2016, related to JEDEC committee JC-40 and DDR4 LRDIMM and RDIMM components. Ex. 4 ('837 LOA). The '319

patent is a continuation of the '837 patent. Therefore, under the JEDEC Patent Policy, the commitments in the '837 Letter of Assurance extend to the '319 patent. Ex. 3 (JEDEC Manual No. 21T) § 8.2.1.

100. The commitments that Netlist has made to license its SEPs on RAND terms constitute binding contractual obligations that may be enforced by firms seeking to implement the JEDEC standards, such as Samsung.

3. Netlist's Failure to Comply with Its RAND Obligations

101. Although Netlist accepted the benefits of its membership in JEDEC to induce JEDEC to incorporate technologies over which Netlist claims to have patents into JEDEC standards, Netlist has failed to fulfill its corresponding contractual commitments. Despite voluntarily undertaking the obligation to license its alleged SEPs on RAND terms, Netlist has made licensing demands of Samsung that violate its RAND commitment.

102. For instance, by email dated February 2, 2021, Netlist demanded that Samsung enter a second license to patents that Samsung previously licensed from Netlist, coupled with a demand to "be made whole" for any alleged breach under the Agreement. Specifically, Netlist stated that "Samsung will require a new license to our patent portfolio" and requested "[d]amages that Netlist has incurred as a result of Samsung's material decrease of product supply to Netlist following Q1 2017 and how Netlist might be made whole."

103. Further, Netlist has brought counterclaims against Google in Delaware based on Google's use of Samsung DDR4 Memory Modules. Netlist has also stated that it seeks an injunction against Google for infringement of the '218 and '595 patents in the Delaware -1453 Litigation. *See* D.I. 127 at 11. Such an injunction request violates Netlist's commitment to license its alleged SEPs on RAND terms and conditions.

104. Accordingly, and as discussed elsewhere herein, Netlist has breached its obligations under the JEDEC Patent Policy.

105.

COUNT I
(Declaration of Non-Infringement of the '319 Patent)

106. Samsung restates and incorporates by reference the preceding paragraphs as if fully set forth herein.

107. The Patent Office issued the '319 patent, titled "Memory Module Having Open-Drain Output for Error Reporting and for Initialization," on January 23, 2024. On information and belief, Netlist claims to own all rights, title, and interest in the '319 patent. A true and correct copy of the '319 patent is attached hereto as Exhibit 1.

108. The '319 patent has two independent claims, 1 and 11. For example, claim 1 reads as follows:

Element	Claim Language
preamble	A memory subsystem operable with a system memory controller of a host system, comprising:
(a)	dynamic random access memory elements on a printed circuit board and configurable to communicate data signals with the system memory controller; and
(b)	a memory subsystem controller on the printed circuit board and coupled to the dynamic random access memory elements, the memory subsystem controller having an open drain output, wherein the memory subsystem is configured to provide a first signaling interface via the open drain output during normal operations and a second signaling interface via the open drain output during an initialization operation including initialization operation sequences, wherein the second signaling interface is distinct from the first signaling interface and the initialization operation is distinct from any of the normal operations;
(c)	wherein, during the normal memory read or write operations, the memory subsystem controller is configured to receive address and command signals associated with the memory read or write operations and to control the dynamic random access memory elements in accordance with the address and command signals, and the memory subsystem controller is further configured to output via the open drain output a parity error signal

Element	Claim Language
	in response to a parity error having occurred during the normal memory read or write operations; and
(d)	wherein, during the initialization operation, the memory subsystem controller is configured to output via the open drain output a signal related to one or more parts of the initialization operation sequences.

109. Samsung has not directly or indirectly infringed any claim of the '319 patent, either literally or under the doctrine of equivalents, at least because the Samsung Memory Modules do not employ, incorporate, or otherwise make use of all of the limitations of the claim of the '319 patent.

110. For example, claims 1 and 11 require “a first signaling interface via the open drain output during normal operations and a second signaling interface via the open drain output during an initialization operation including initialization operation sequences, wherein the second signaling interface is distinct from the first signaling interface and the initialization operation is distinct from any of the normal operations.” The Samsung Memory Modules do not satisfy the requirements of claims 1 and 11 for at least the reason that the second signaling interface is not distinct from the first signaling interface.

111. The Samsung Memory Modules do not infringe any of claims 2–10 and 12–20 at least because these claims depend directly or indirectly from claims 1 and 11.

112. Samsung, its customers, and its end users are not liable for infringement of the '319 patent for any Samsung Memory Modules made, imported, or sold under license from Netlist.

113. A substantial, immediate, and real controversy exists between Samsung and Netlist regarding whether Samsung or its customers or end users infringe the '319 patent by making, using, selling, and/or offering for sale the Samsung Memory Modules in the United States,

or by importing the Samsung Memory Modules into the United States. A judicial declaration is necessary to determine the parties' respective rights regarding the '319 patent.

114. Samsung seeks a judgment declaring that Samsung and its customers and end users do not infringe the '319 patent, either literally or under the doctrine of equivalents, by making, using, selling, and/or offering for sale the Samsung Memory Modules in the United States, or by importing the Samsung Memory Modules into the United States, either directly under 35 U.S.C. § 271(a) or indirectly under 35 U.S.C. § 271(b)–(c).

COUNT II
(Breach of Contract)

115. Samsung restates and incorporates by reference the preceding paragraphs as if fully set forth herein.

116. Under the JEDEC Patent Policy, Netlist has a contractual commitment to offer implementers of the JEDEC Standards, including Samsung, licenses to any Essential Patent Claims (as defined in the JEDEC Patent Policy) on RAND terms and conditions. This contractual commitment is on-going. Netlist continues to have an obligation to license its SEPs to Samsung on RAND terms, notwithstanding any breach of the Agreement or any termination of the license contained therein. Having entered the Agreement, Samsung showed that it is a willing licensee.

117. Netlist submitted Letters of Assurance to the JC-40, JC-42, and JC-45 committees in which Netlist promised to make available to implementers of the DDR4 Standards a license to the '837 patent "under reasonable terms and conditions that are demonstrably free of any unfair discrimination." Ex. 4 ('837 LOA). Under the JEDEC Patent Policy, those commitments extend to the claims of the '319 patent, to the extent they are essential to the DDR4 Standards.

118. The JEDEC Patent Policy and/or Letters of Assurance constitute a valid and binding contract between Netlist and JEDEC.

119. Samsung is a third-party beneficiary to the JEDEC Patent Policy and/or Letters of Assurance, and to Netlist's RAND obligations thereunder. Participation in JEDEC committees and the standard-setting process is expressly conditioned on a commitment to license essential patents to third-party implementers on RAND terms. Ex. 3 (JEDEC Manual No. 21T) § 8.2.2.1. The JEDEC Patent Policy is therefore intended to benefit third-party implementers of JEDEC standards, such as Samsung, and the obligations under the JEDEC Patent Policy, including the RAND obligations, are intended to be enforceable by third-party implementers of the JEDEC standards. Third-party implementers, such as Samsung, are also the only parties who could recover for Netlist's breach of its obligations under the JEDEC Patent Policy.

120. Samsung has relied on the JEDEC Patent Policy and/or Letters of Assurance, including the RAND obligations set forth therein, in designing, manufacturing, and selling standard-compliant products, including the Samsung Memory Modules, and Samsung has supported the JEDEC standard based on its understanding and expectation that JEDEC members, including Netlist, will abide by their obligations.

121. In ongoing litigation, Netlist and Samsung dispute whether Samsung has a license to Netlist's patents, including the '319 patent, under the Agreement. Netlist has taken the position that Samsung's license under the Agreement has been terminated, while Samsung maintains that the termination was not effective and that it has a license to the '319 patent. In any event, Netlist has failed to offer Samsung a license to patents that Netlist alleges are essential to the JEDEC Standards, including the '319 patent, on RAND terms and conditions. To the extent the '319 patent is essential to any of the JEDEC Standards (which Samsung submits it is not), Netlist has breached its contractual obligations to license such patent to Samsung on RAND terms and conditions.

122. As a result of Netlist's breaches of contract, Samsung has been injured in its business or property because it has been denied access to a license to Netlist's claimed SEP on RAND terms, a license that can only be obtained from Netlist. Netlist's conduct threatens Samsung with imminent loss of customers and potential customers, loss of goodwill and product image, loss of sales, litigation costs, uncertainty in business planning, and uncertainty among customers and potential customers.

JURY DEMAND

Samsung demands a jury trial on all issues and claims so triable.

PRAYER FOR RELIEF

WHEREFORE, Samsung prays for judgment and relief as follows:

- (a) Declare that Samsung does not directly or indirectly infringe the '319 patent, either literally or under the doctrine of equivalents, and that it is not liable for damages or injunctive relief based on any claim in the '319 patent;
- (b) Declare that Netlist is liable for breach of contract;
- (c) Grant injunctive relief requiring Netlist to offer a license to the '319 patent—to the extent it is found to be essential to the JEDEC standards—on reasonable terms and conditions that are demonstrably free from any unfair discrimination;
- (d) Enjoin Netlist from further demanding excessive, non-RAND royalties from Samsung for alleged infringement of the '319 patent;
- (e) Declare that Netlist is barred from seeking and/or enforcing injunctive relief against Samsung (including its affiliates) or its direct or indirect customers and end-users in any jurisdiction with respect to any alleged infringement of the '319 patent;

(f) Enjoin Netlist from seeking and/or enforcing injunctive relief against Samsung (including its affiliates) or its direct or indirect customers and end users in any jurisdiction with respect to any alleged infringement of the '319 patent;

(g) Compensate Samsung for all damages caused by Netlist's breaches of contract, including breaches of its RAND obligations;

(h) Declare that judgment be entered in favor of Samsung and against Netlist on each of Samsung's claims;

(i) Find that this is an exceptional case under 35 U.S.C. § 285;

(j) Award Samsung pre-judgment and post-judgment interest;

(k) Award Samsung its costs and attorneys' fees in connection with this action; and

(l) Such further and additional relief as the Court deems just and proper.

MORRIS, NICHOLS, ARSHT & TUNNELL LLP

/s/ Rodger D. Smith II

OF COUNSEL:

Brian Nester
Peter Swanson
COVINGTON & BURLING LLP
One CityCenter
850 Tenth Street, NW
Washington, DC 20001-4956
(202) 662-6000

Alice J. Ahn
COVINGTON & BURLING LLP
Salesforce Tower
415 Mission Street, Suite 5400
San Francisco, CA 94105-2533
(415) 591-6000

May 22, 2024

Jack B. Blumenfeld (#1014)
Rodger D. Smith II (#3778)
1201 North Market Street
P.O. Box 1347
Wilmington, DE 19899
(302) 658-9200
jblumenfeld@morrisnichols.com
rsmith@morrisnichols.com

Attorneys for Plaintiffs

EXHIBIT 1



US011880319B2

(12) **United States Patent**
Lee

(10) **Patent No.:** **US 11,880,319 B2**
(45) **Date of Patent:** **Jan. 23, 2024**

(54) **MEMORY MODULE HAVING OPEN-DRAIN OUTPUT FOR ERROR REPORTING AND FOR INITIALIZATION**

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(71) Applicant: **Netlist, Inc.**, Irvine, CA (US)

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(Continued)

(72) Inventor: **Hyun Lee**, Ladera Ranch, CA (US)

(73) Assignee: **Netlist, Inc.**, Irvine, CA (US)

FOREIGN PATENT DOCUMENTS

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(21) Appl. No.: **17/840,593**

Inter Partes Review of U.S. Pat. No. 9,858,218, Case No. IPR2022-00062, Exhibit 1067—Oct. 15, 2021 Complaint, filed Oct. 15, 2021.

(22) Filed: **Jun. 14, 2022**

(Continued)

(65) **Prior Publication Data**

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Primary Examiner — Mardochee Chery

(74) *Attorney, Agent, or Firm* — USCH Law, PC

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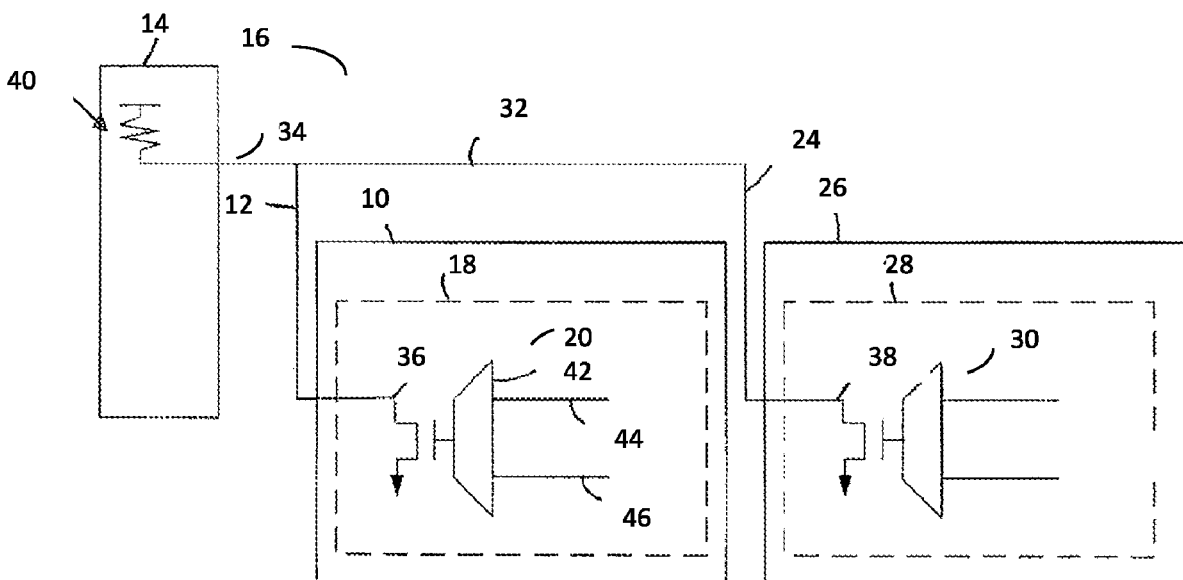
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CPC **G06F 13/1694** (2013.01); **G06F 3/0619** (2013.01); **G06F 3/0632** (2013.01);
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(Continued)

(57) **ABSTRACT**

According to certain aspects, a memory subsystem is coupled to a memory controller of a host computer system via an interface. The memory subsystem comprises dynamic random access memory elements and a memory subsystem controller. During a normal memory read or write operation, the memory subsystem controller is configured to receive address and command signals associated with the memory read or write operations and to control the dynamic random access memory elements in accordance with the address and command signals. The memory subsystem controller is further configured to output via the open drain output a parity error signal in response to a parity error having occurred during the memory read or write operation. During an initialization operation, the memory subsystem controller is configured to output via the open drain output a signal related to one or more parts of initialization operation sequences.

20 Claims, 3 Drawing Sheets



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Related U.S. Application Data

continuation of application No. 15/857,553, filed on Dec. 28, 2017, now Pat. No. 10,474,595, which is a continuation of application No. 15/088,155, filed on Apr. 1, 2016, now Pat. No. 9,667,001, which is a continuation of application No. 13/942,721, filed on Jul. 16, 2013, now Pat. No. 9,311,116, which is a continuation of application No. 12/815,339, filed on Jun. 14, 2010, now Pat. No. 8,489,837.

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 See application file for complete search history.

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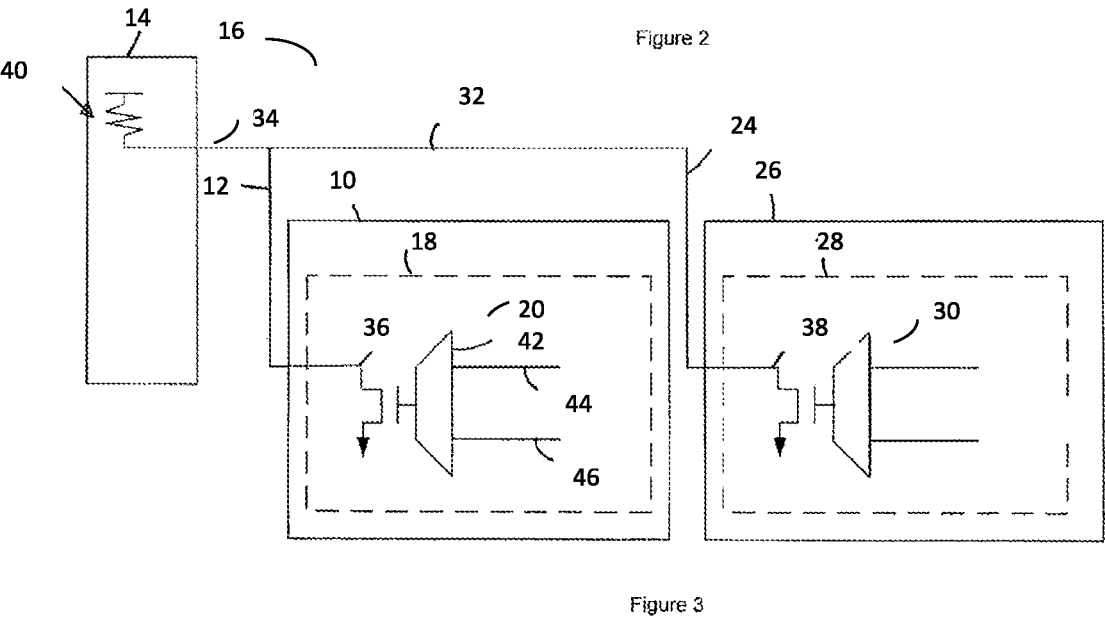
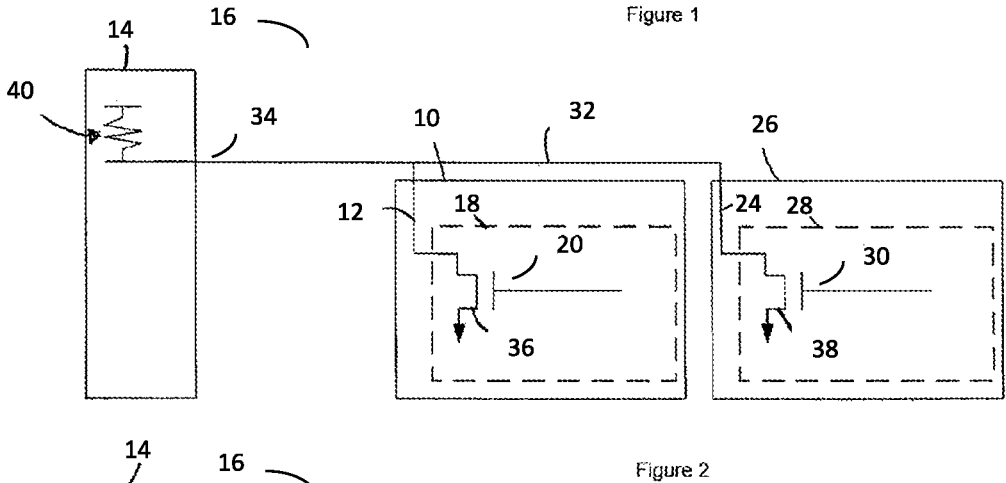
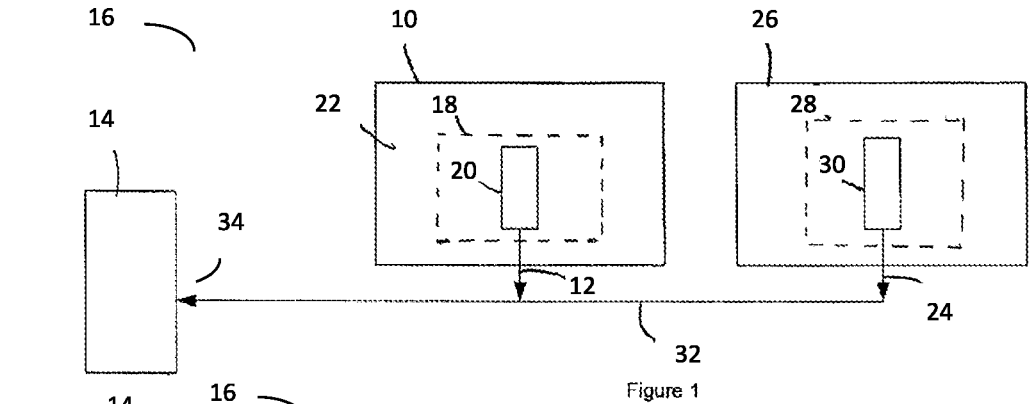
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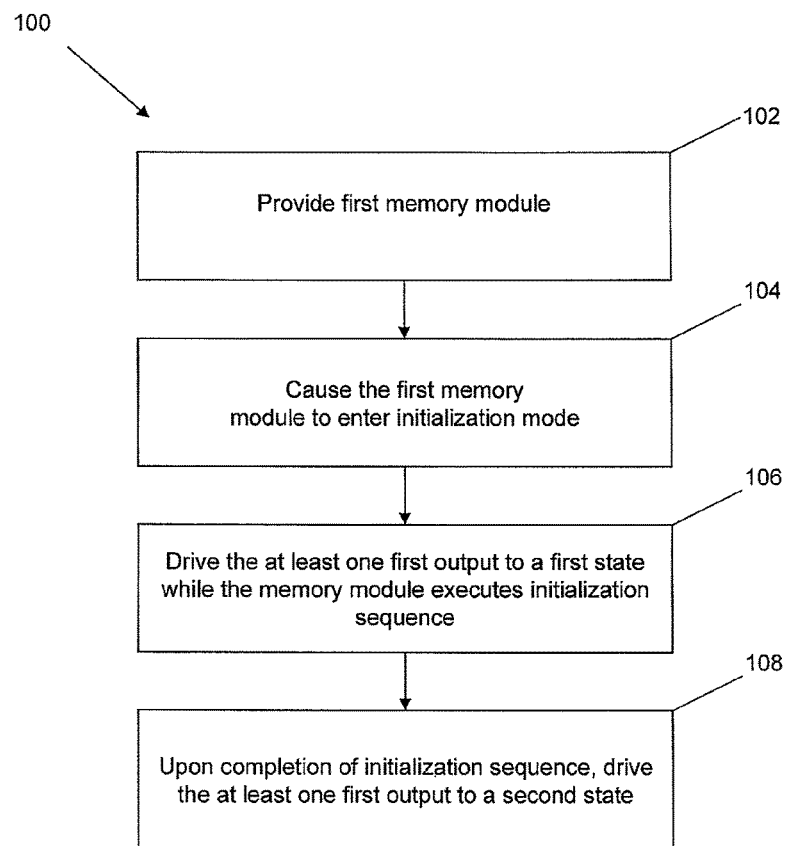


Figure 4

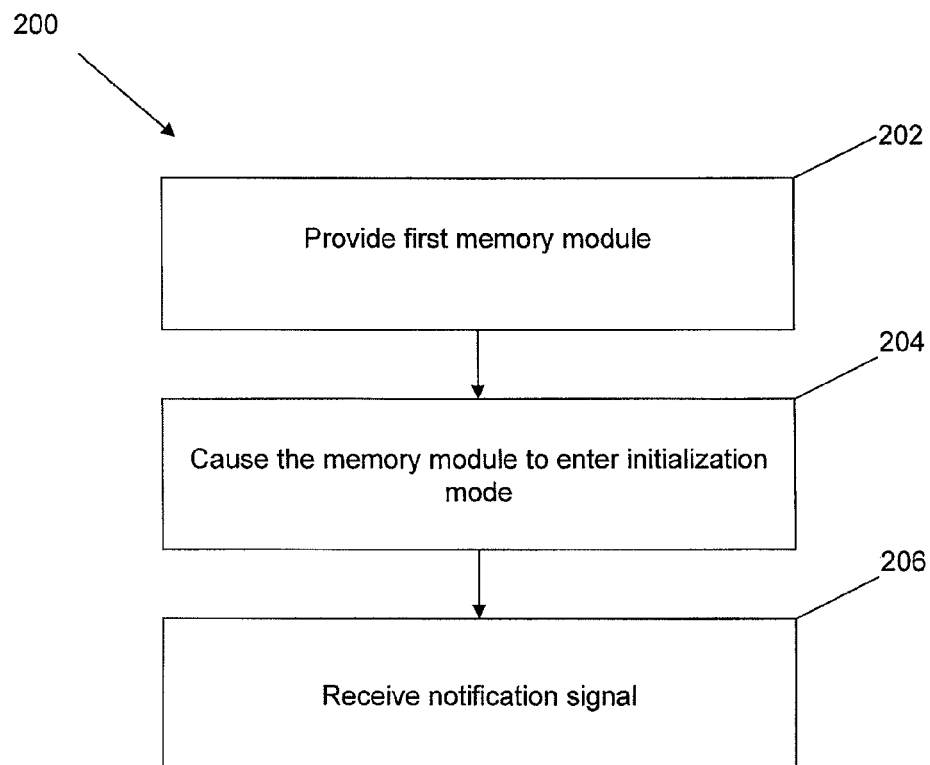


Figure 5

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MEMORY MODULE HAVING OPEN-DRAIN OUTPUT FOR ERROR REPORTING AND FOR INITIALIZATION

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation of U.S. application Ser. No. 16/680,060, filed Nov. 11, 2019, which is a continuation of U.S. application Ser. No. 15/857,553, filed Dec. 28, 2017, now U.S. Pat. No. 10,474,595, which is a continuation of U.S. application Ser. No. 15/088,155, filed Apr. 1, 2016, now U.S. Pat. No. 9,858,218, which is a continuation of U.S. application Ser. No. 13/942,721, filed Jul. 16, 2013, now U.S. Pat. No. 9,311,116, which is a continuation of U.S. application Ser. No. 12/815,339, filed Jun. 14, 2010, now U.S. Pat. No. 8,489,837, which claims the benefit of priority from U.S. Provisional App. No. 61/186,799, filed Jun. 12, 2009, each of which is incorporated in its entirety by reference herein.

FIELD OF THE DISCLOSURE

The present disclosure relates to the operation of memory modules. Specifically, the present disclosure relates to systems and methods for handshaking with a memory module during or upon completion of initialization.

BACKGROUND OF THE DISCLOSURE

Memory subsystems such as memory modules are generally involved in the initialization procedure for computer systems, including servers, personal computers, and the like. For example, during system-wide initialization, the memory subsystems may undergo internal initialization procedures, or the system memory controller may otherwise interact with the memory subsystems during the initialization procedure. As part of this interaction, the system memory controller may request that the memory subsystem perform one or more requested tasks during system initialization.

SUMMARY

According to certain aspects, a memory module is coupled to a memory controller of a host computer system via an interface. The interface includes data, address and control signal pins and an output pin in addition to the data, address and control signal pins. The memory module receives a first command from the memory controller via the address and control signal pins, and enters a first mode in response to the first command. The memory module in the first mode responds to at least one initialization sequence, and sends a first output signal via the output pin to indicate a status of the at least one initialization sequence to the memory controller. The memory module enters a second mode in which the memory module performs memory operations including memory read/write operations according to an industry standard. During the read/write operations, the memory module communicates data with the memory controller via the data signal pins in response to second memory commands received via the address and control signal pins. The memory module may output a second output signal related to the read/write operations via the output pin.

According to certain aspects, a memory module is coupled to a memory controller of a host computer system via an interface. The interface includes data, address and

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control signal pins and an output pin in addition to the data, address and control signal pins. The memory module performs an internal procedure in a first mode in response to a first command from the memory controller whereby the memory controller hands off control of the internal procedure to the first memory module. The memory module sends a first output signal via the output pin to indicate a status of the internal procedure to the memory controller. The memory module enters a second mode in which the memory module performs standard operations including one or more of memory read/write, pre-charge, refresh operations according to an industry standard. The memory module may output a second output signal related to the standard operations via the output pin.

In another aspect, a memory module is operable in a first mode and in a second mode. The memory module operates according to an industry standard in the second mode by performing standard operations including memory read/write operations in response to address and control signals from a memory controller of a host computer system. The memory module comprises a standard interface including data, address and control signal pins and an output pin in addition to the data, address and control signal pins. The memory module enters the first mode in response to a first command from the memory controller, in which the memory module responds to at least one initialization sequence. The memory module further comprises a notification circuit to output a notification signal indicating a status of the at least one initialization sequence to the memory controller via the output pin.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows an example host computer system including an example memory module configured to perform handshaking with a memory controller of the host computer system according to certain embodiments described herein.

FIG. 2 shows an example host computer system including example first and second memory modules configured to perform handshaking with a system memory controller of the host computer system according to certain embodiments described herein.

FIG. 3 shows a host computer system including example first and second memory modules configured to perform handshaking with a memory controller of the host system, where the notification circuits of the first and second memory modules have another example configuration according to certain embodiments described herein.

FIG. 4 and FIG. 5 show example methods of using at least one memory module according to certain embodiments described herein.

DETAILED DESCRIPTION

Existing initialization schemes have certain inefficiencies which lead to wasted time and expense. Thus, there is a need to reduce the time and complexity involved in system memory controller interactions with memory subsystems during initialization. Certain embodiments described herein advantageously satisfy at least a portion of this need by providing a system and method which utilizes a feedback path from a memory subsystem such as a memory module to a system memory controller, such as a Memory Controller Hub (MCH) of a computer system during initialization.

In general, there is no existing method of handshaking between the MCH (e.g., system memory controller) and a memory subsystem (e.g., memory module) during initial-

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ization. For example, in conventional systems, the system memory controller does not monitor the error-out signal from the memory subsystem. This causes the MCH to perform blind execution. In a typical server (e.g., an Intel or AMD or other chipset based server), the lack of any handshaking between the MCH and the memory subsystem during the server initialization period has not been a serious issue since the MCH generally has complete control over the initialization procedure. However, one possible configuration for LR-DIMM (Load Reduced DIMM) includes the MCH handing over one or more parts of the initialization operation sequence to the memory subsystem. This raises an unprecedented issue not addressed in conventional systems because, in such proposed configurations, the system can benefit from the MCH handshaking with the memory subsystem controller, as described more fully below.

Such an LR-DIMM configuration may have the MCH inserting a waiting period of predetermined length during which the MCH is idle and the memory subsystem controller undergoes initialization. However, one shortcoming of this LR-DIMM configuration would be that it requires the MCH to be in standby (idle, or wait) while the memory subsystem controller completes its task. Under such an arrangement, since the time to complete a task can be dependent on the density, speed and configuration of the memory subsystem, and these parameters may be unknown to the MCH, the MCH may have to insert a single, predetermined standby period. In addition, if there are multiple occasions that the MCH needs to hand off control to the memory subsystem controller, the required MCH wait periods can be different from one occasion to another, and it complicates the correlation between the MCH and the memory subsystem controller. For example, the MCH according to such a scheme may give control to the local memory controller of a memory subsystem (e.g., memory module) for execution of a training sequence. The MCH may wait for a pre-determined period of time and then assume that the local memory controller has completed the training sequence. However, depending on the memory subsystem parameters (e.g., memory capacity, speed, number of ranks, etc.), the time for actually completing the training sequence may vary and may be longer or shorter than predetermined period of time.

In general, handshaking can be implemented in at least two ways; polling and notifying. In the polling method, the MCH reads a status register in the memory subsystem controller to find out if the memory subsystem controller has completed the required or requested operation. For example, a status register may be read out through a serial interface such as System Management Bus (SMBus). However, a register polling method is generally inefficient because the system memory controller does not know exactly when the memory subsystem will have completed the required or requested operation. Thus, the system memory controller may wait longer than necessary to poll the memory subsystem, thereby delaying the overall initialization process. Additionally, the problem may be compounded because multiple training sequences or other initialization sequences may be run on the memory subsystem during a particular initialization period, resulting in accumulation of such unnecessary delays. Moreover, polling generally involves scheduling polling intervals during which the system memory controller is not performing other operations, resulting in further inefficiency.

Alternatively, the notifying method is an advantageous handshaking method between the MCH and the memory subsystem controller. According to a notifying method, the memory subsystem controller sends a signal to the MCH

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when the memory subsystem controller completes the required or requested operation. This method allows the MCH to execute one or more independent commands while it is waiting for a notification signal from the memory subsystem controller.

Certain embodiments described herein provide a method of establishing a handshake mechanism based on notification signaling. In certain embodiments, this mechanism can be implemented by adding a new interface (notifying) signal between the MCH and the memory subsystem controller, or by adding an additional functionality to an existing, non-timing critical signal without altering the memory subsystem hardware. In either case, the interface between the MCH and the memory subsystem controller of certain embodiments can be an open drain signaling from the memory subsystem controller to the MCH, although a variety of other configurations are possible. As will be appreciated by persons skilled in the art, the terms MCH, system memory controller, and memory subsystem are used generally interchangeable throughout this disclosure, and the terms memory module, memory subsystem controller, and local memory controller are used generally interchangeably throughout this disclosure.

FIG. 1 illustrates an example host computer system 16 including an example memory module 10 according to certain embodiments described herein. The memory module 10 can comprise at least one output 12 configured to be operatively coupled to a system memory controller 14 of the host computer system 16. In certain embodiments, the memory module 10 is configured to operate in at least two modes comprising an initialization mode during which the memory module 10 executes at least one initialization sequence, and an operational mode. The memory module 10 may further include a controller circuit 18. In some embodiments, the controller circuit 18 is configured to cause the memory module 10 to enter the initialization mode. The memory module 10 can further include a notification circuit 20 configured to drive the at least one output 12 while the memory module 10 is in the initialization mode to provide at least one notification signal to the memory controller 14 indicating at least one status of the at least one initialization sequence.

The memory module 10 may comprise a printed-circuit board (PCB) 22. In certain embodiments, the memory module 10 has a memory capacity of 512-MB, 1-GB, 2-GB, 4-GB, 8-GB, 16-GB, or higher. Other memory capacities are also compatible with certain embodiments described herein. In addition, memory modules 10 having widths of 4 bytes, 8 bytes, 16 bytes, 32 bytes, or 32 bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein. The PCB 22 can have an industry-standard form factor. For example, the PCB 22 can have a low profile (LP) form factor with a height of 30 millimeters and a width of 133.35 millimeters. In certain other embodiments, the PCB 20 has a very high profile (VHP) form factor with a height of 50 millimeters or more. In certain other embodiments, the PCB 22 has a very low profile (VLP) form factor with a height of 18.3 millimeters. Other form factors including, but not limited to, small-outline (SO-DIMM), unbuffered (UDIMM), registered (RDIMM), fully-buffered (FBDIMM), mini-DIMM, mini-RDIMM, VLP mini-DIMM, micro-DIMM, and SRAM DIMM are also compatible with certain embodiments described herein. In other embodiments, certain non-DIMM form factors are possible such as, for example, single in-line memory module (SIMM), multi-media card (MMC), and small computer system interface (SCSI).

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In certain embodiments, the memory module 10 is operatively coupled to (e.g., in electrical communication with) the host computer system 16. In certain other embodiments, the memory module 10 may communicate with the host computer system 16 using some other type of communication, such as, for example, optical communication. Examples of host computer systems 16 include, but are not limited to, blade servers, 1 U servers, personal computers (PCs), and other applications in which space is constrained or limited. The PCB 22 can comprise an interface (not shown) that is configured to be in electrical communication with the host computer system 16. For example, the interface can comprise a plurality of edge connections which fit into a corresponding slot connector of the host system 16. The interface of certain embodiments provides a conduit for power voltage as well as data, address, and control signals between the memory module 10 and the host system 16. For example, the interface can comprise a standard 240-pin DDR2 edge connector. The at least one output 12 may be routed over the interface, for example.

The memory module 10 may also comprise one or more memory elements (not shown), such as dynamic random-access memory (DRAM) elements, for example. Types of DRAM elements compatible with certain embodiments described herein include, but are not limited to, DDR, DDR2, DDR3, DDR4, and synchronous DRAM (SDRAM). In addition, memory elements having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with certain embodiments described herein. Memory elements compatible with certain embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BGA), fine-pitch BGA (FBGA), micro-BGA (μ BGA), mini-BGA (mBGA), and chip-scale packaging (CSP). In certain embodiments, the memory module 10 may also include one or more non-volatile memory elements, such as one or more flash memory elements. Types of flash memory elements compatible with certain embodiments described herein include, but are not limited to, NOR flash, NAND flash, ONE-NAND flash, and multi-level cell (MLC).

The controller circuit 18 of certain embodiments generally controls the operation of the memory module 10. For example, the controller circuit 18 may control the memory elements of the memory module 10 and/or communicate with the system memory controller 14. For example, the controller circuit 18 may receive and process address and command signals (e.g., read, write commands) from the system memory controller 14 and transmit appropriate address and commands to the memory elements in response. See, e.g., U.S. Pat. Appl. Publ. Nos. 2006/0062047 A1 and 2006/0262586 A1, each of which is incorporated in its entirety by reference herein. In certain embodiments, the controller circuit 18 comprises a local memory controller. Additionally, depending on the architecture of the memory module 10, such as for an FB-DIMM, the controller circuit 18 may comprise an advanced memory buffer (AMB). The controller circuit 18 can comprise one or more of a field-programmable gate array (FPGA), a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a custom-designed semiconductor device, and a complex programmable logic device (CPLD), for example. In certain embodiments, the controller circuit 18 comprises various discrete electrical elements, while in certain other embodiments, the controller circuit 18 comprises one or more integrated circuits.

As discussed, the memory module 10 is configured to operate in at least two modes comprising an initialization

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mode during which the memory module 10 executes at least one initialization sequence, and an operational mode. In one embodiment, for example, the at least one initialization sequence may comprise one or more training sequences. The initialization sequence (e.g., comprising one or more training sequences) may be initiated by the system memory controller 14. In some embodiments, the controller circuit 18 is configured to cause the memory module 10 to enter the initialization mode. For example, the controller circuit 18 may be configured to execute a routine implementing the at least one initialization sequence when the appropriate signal or command is received from the memory controller 14 or is otherwise received from the host computer system 16 (e.g., upon receipt of a reset signal).

In certain embodiments, for example, the computer system 16 is coupled to a plurality of memory modules 10, 26 including the memory module 10 and at least a second memory module 26, and the memory controller 14 (e.g., MCH) trains each module 10, 26 separately, in series. In one example scenario, the memory controller 14 issues a first command to the memory module 10, and, in response, the memory module 10 executes an initialization sequence (e.g., one or more training sequences). Upon completion of the initialization sequence, the first memory module 10 advantageously issues a notification to the memory controller 14 in accordance with embodiments described herein. In response, the memory controller 14 issues a second command, this time to the memory module 26, and, in response, the memory module 26 executes an initialization sequence (e.g., one or more training sequences). Upon completion of the initialization sequence, the second memory module 26, similar to the first memory module 10, advantageously issues a notification to the memory controller 14 in accordance with embodiments described herein. In response, where there are more than two memory modules 10, 26, the memory controller 14 issues a third command to a third memory module (not shown), and so forth. One example computer system 16 capable of implementing such a scenario is configured to execute an Intel Basic Input/Output System (BIOS), and comprises a plurality of memory modules 10, 26 having an LRDIMM configuration. In such an example system, the Intel BIOS causes the system memory controller 14 to initialize the LRDIMM memory modules 10, 26 serially.

The operational mode is the normal mode of the memory module 10. For example, during the operational mode, the memory module 10 is generally accessed by the system memory controller 14 of the host computer 16 during standard computer operation not associated with initialization. For example, the system memory controller 14 may cause the memory module 10 to perform standard operations such as memory read/write, pre-charge, refresh, etc., while in operational mode, although it will be appreciated that one or more of these operations can also be performed by the memory module 10 while in initialization mode in certain embodiments.

The notification circuit 20 can be configured to drive the at least one output 12, while the memory module 10 is in the initialization mode or after the memory module 10 completes one or more initialization sequences, to provide the at least one notification signal to the memory controller 14 indicating at least one status of the at least one initialization sequence. While shown in FIGS. 1-3 as forming a part of the controller circuit 18, the notification circuit 20 may be a physically and/or logically separate circuit in certain embodiments. While a variety of configurations are possible, the notification circuit 20 may comprise one or more tran-

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sistors, one or more logic elements (e.g., AND, OR, NOR, NAND, XOR gates, and the like), or a combination thereof. In some embodiments, the notification circuit 20 may additionally or alternatively comprise one or more of an FPGA, PLD, CPLD, ASIC, custom-designed semiconductor device, discrete electrical elements, and an integrated circuit.

The at least one status of certain embodiments comprises completion of the at least one initialization sequence, such that the at least one notification signal is indicative of the completion of the at least one initialization sequence. The at least one status of certain embodiments comprises execution of the at least one initialization sequence. For example, the at least one status may indicate that the at least one initialization sequence is currently being executed. In some embodiments, the at least one status may provide an indication that a certain task has been completed by the memory module 10, such as a training task requested by the system memory controller 14. In certain embodiments, the notification circuit 20 can be configured to drive the at least one output 12 to a first state indicative of execution of the at least one initialization sequence or to a second state indicative of completion of the at least one initialization sequence. As one example, the first state may be a high or low logic level, and the second state may be a high impedance state. In another case, the first state is a high or low logic level, and the second state is the inverse logic level of the first state.

The at least one output 12 of certain embodiments is configured to be operatively coupled to at least one interrupt of the system memory controller 14, and the system memory controller 14 is responsive to the at least one notification signal indicating completion of the at least one initialization sequence. For example, the system memory controller 14 may trigger execution of an interrupt routine upon receipt of the notification signal on the output 12. The interrupt routine generally executes the appropriate operations for the at least one status indicated by the at least one notification signal. For example, if the at least one status indicates that the at least one initialization sequence is complete, execution of the interrupt routine may cause the system memory controller 14 to notify the host computer system 16 that the system initialization, or a portion thereof, is completed. In one embodiment, for example, the execution of the interrupt routine causes the system memory controller 14 to initiate a subsequent training sequence for the memory module 10 or on another memory module connected to the host system 16. For example, in one embodiment, a central processing unit (CPU) of the host system 16 (not shown) enters a "Wait" state after issuing a command to the memory module 10 to enter the initialization mode. Receipt of the at least one notification signal on the output 12 triggers execution of the interrupt routine, which interrupts the CPU, causing the "Wait" state to be aborted and allowing the host system 16 to continue operation. In this manner, generation of the interrupt on the at least one output 12 can allow completion of the at least one initialization sequence to receive generally immediate attention from the CPU and/or memory controller 14 of the host system 16. As will be appreciated, the CPU and memory controller 14 of the host system 16 may comprise separate modules, or may alternatively comprise a single integrated module, depending on the architecture of the host system 16 chip-set.

In certain embodiments, execution of the interrupt routine causes the system memory controller 14 to cause the memory module 10 to exit the initialization mode and to enter the operational mode. In another embodiment, the memory module 10 automatically enters the operational

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mode upon completion of the at least one initialization sequence without intervention from the memory controller 14.

In some embodiments, the at least one output 12 is operated in conformance with a standard (e.g., an industry standard) when the memory module 10 is in the operational mode, but is not operated in conformance with the standard when the memory module 10 is in the initialization mode. An example of a standard in accordance with certain embodiments described herein is one or more of the industry standard promulgated by the Joint Electronic Devices Engineering Counsel (JEDEC). For example, the operation and behavior of the at least one output 12 may conform to an industry standard when the memory module 10 is in the operational mode, but the operation and behavior of the at least one output 12 may not conform to the industry standard when the memory module 10 is in the initialization mode. Because the at least one output 12 does not conform to the standard during initialization mode, an existing (e.g., JEDEC-specified) pin may be utilized to provide the at least one notification signal to the system memory controller 14 from the memory module 10 during the initialization mode. In one embodiment, for example, the at least one output 12 comprises an error-out pin of the memory module 10. In conventional systems, the operation of the error-out pin is undefined by the standard during initialization. However, in certain embodiments described herein, during the operational mode, the error-out pin may be used according to a conventional industry standard (e.g., a JEDEC standard) to indicate a parity error has occurred in the memory module 10. During the initialization mode, the error-out pin can be used to transmit the at least one notification signal to the system memory controller 14.

It is advantageous to use the error-out pin for initialization status notification according to certain embodiments because the error-out pin can be asserted by the memory module 10 independent from system memory controller 14 requests or commands. Also, because the error-out pin is a JEDEC-specified pin, design cost and complexity are reduced because additional pin-outs and interrupt design changes can be avoided (e.g., in cases where such changes in hardware or chipset may not be feasible to provide the at least one status to the system memory controller 14). However, in certain other embodiments, providing the at least one status may be implemented by adding one or more pins to the system memory controller 14 (e.g., MCH) and to the controller circuit 18 (e.g., local memory controller), thereby utilizing changes in hardware or the chipset.

Moreover, the error-out pin may be coupled to an interrupt of the system memory controller 14 (e.g., according to the JEDEC standard). Thus, where the error-out pin is used, from the system point of view in accordance with certain embodiments, the notification of completion of the required or requested task from the memory module 10 (e.g., by the local memory controller) generates an interrupt communicated to the system during the initialization period and indicative of completion of the required or requested task. Assertion of the same pin during normal (non-initialization) operation upon an error occurring, on the other hand, generates an interrupt communicated to the system during the normal operation indicative of the occurrence of the error condition. Thus, in certain embodiments, the error-out pin and corresponding signal memory module 10 can be used to support the notifying function and to provide the at least one status generally without changing hardware. Certain other such embodiments involve modifying the basic input/output system (BIOS) or other programming change.

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For example, the BIOS may be modified to indicate to the system memory controller 14 how to respond to the notification signal (e.g., to the error_out signal or the interrupt corresponding thereto).

In certain other embodiments, the at least one output 12 may include other existing (e.g., JEDEC specified) pins instead of, or in addition to, the error-out pin. In yet other configurations, at least one additional (e.g., non-JEDEC specified) pin may be employed. In general, any pin not otherwise active during the initialization mode may be used (e.g., high-order address pins, read/write pins, data pins, etc.).

The at least one output 12 can further be configured to be operatively coupled to at least one second output 24 of a second memory module 26 in some embodiments, as schematically illustrated in FIGS. 1-3. The second memory module 26 may be generally similar in structure and function to the memory module 10, and may comprise a controller circuit 28 and a notification circuit 30, for example. The second memory module 26 may be generally identical to the first memory module 10, or may have a different memory capacity, form factor, etc., than the first memory module 10. More than two such memory modules may be present in certain embodiments. As described above, the second memory module 26 can be configured to operate in at least two modes comprising an initialization mode during which the second memory module 26 executes at least one initialization sequence, and an operational mode. For example, the initialization and operational modes may be similar to those describe above in relation to the first memory module 10.

The second memory module 26 can also be configured to drive the at least one second output 24 to a third state indicative of execution of at least one initialization sequence of the second memory module 26 or to a fourth state indicative of completion of the at least one initialization sequence of the second memory module 26. Additionally, in some embodiments, the at least one first output 12 of the first memory module 10 and the at least one second output 24 of the second memory module 26 are operatively coupled together by a bus 32 which is also operatively coupled to at least one input 34 of the system memory controller 14. In other embodiments (not shown), the at least one first output 12 and the at least one second output 24 are not coupled together, and are coupled to two separate inputs of the system memory controller 14.

FIG. 2 shows an example host computer system 16 including example first and second memory modules 10, 26. As shown, the notification circuits 20, 30 of the first and second memory modules 10, 26 each comprise at least one transistor 36, 38. The at least one transistor 36, 38 can be in an open-drain configuration, as shown, although other configurations are possible. In certain such embodiments, the first state of the at least one first output 12 is a first logic level, the second state of the at least one first output 12 is a high-impedance state, the third state of the at least one second output 24 is the first logic level, and the fourth state of the at least one second output 24 is the high-impedance state. In the illustrated example, while the at least one initialization sequence is in progress, the first and second memory modules 10, 26 drive the gates of the respective transistors 36, 38 high. Thus, the transistors 36, 38 are respectively low impedance while the memory modules 10, 26 are executing each section of the initialization sequence, thereby pulling the first and second outputs 12, 24 low. Thus, the first state and the third state are low logic levels (ground) in the example configuration. Also, because the first and

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second outputs 12, 24 are coupled together by the bus 32, if the at least one initialization sequence of either one of the first and second memory modules 10, 26 are in progress, the bus 32 will be pulled to a low logic level.

As each of the two memory modules 10, 26 completes its at least one initialization sequence, it can drive the corresponding at least one first and second outputs 12, 24 respectively to a high impedance state. For example, once the at least one initialization sequence on each of the first and second memory modules 10, 26 is completed, the first and second memory modules 10, 26 can drive the gates of the respective transistors 36, 38 low, resulting in a high-impedance state on the at least one first and second outputs 12, 24 causing the bus 32 to be pulled high by the system memory controller 14. Accordingly, only once the at least one initialization sequence of both the first and second memory modules 10, 26 are complete, the bus 32 will be pulled high by the internal pull-up configuration 40 of the system memory controller 14. The second state and the fourth state are therefore high-impedance values in the example embodiment. Thus, the system memory controller 14 can monitor the value on the bus 32 via the first input 34 to determine when both of the memory modules 10, 26 have completed the at least one initialization sequence. As discussed, in other configurations the at least one first and second outputs 12, 24 may be received on separate inputs of the system memory controller 14, and the status of the at least one initialization sequence of each memory module 10, 26 may be monitored independently.

As discussed above, in certain embodiments in which more than one memory module 10, 26 is connected to the system memory controller 14, each memory module 10, 26 or associated controller circuit 18 (e.g., local memory controller) causes the corresponding notification circuit 20, 30 to drive the at least one output 12, 24 to the high impedance state from the low impedance state when it completes the requested or required operation. Thus, in certain such embodiments, the system memory controller 14 (e.g., MCH) can only pull the notifying signal high when all memory modules 10, 26 or associated controller circuits (e.g., local memory controllers) have completed the required or requested operation (e.g., initialization sequence). This configuration allows the system memory controller 14 (e.g., MCH) to work with a non-homogenous memory subsystem. For example, the system memory controller 14 may be able to monitor the progress of multiple memory modules 10, 26 including a mix of DIMMs or other memory modules having differing characteristics, such as DIMM density, rank configurations, DRAM density, speed, DRAM configuration, etc.

Additionally, the at least one output 12 of the first memory module 10 and the at least one second output 24 of the second memory module 26 are configured to be operatively coupled to at least one interrupt of the system memory controller 14 in certain embodiments. In certain such embodiments, the system memory controller 14 can be responsive to the second state of the first memory module 10 and the fourth state of the second memory module 26 by triggering execution of an interrupt routine by a processor of the system memory controller 14. For example, in the example system of FIG. 2, when the bus 32 is pulled high by the pull-up configuration 40 indicating the second state of the first memory module 10 and the fourth state of the second memory module 26, the system memory controller 14 triggers execution of the interrupt routine.

In some embodiments, in which the at least one first output 12 and the at least one second output 24 are opera-

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tively coupled to separate inputs of the system memory controller **14**, the at least one first output **12** and the at least one second output **24** may be operatively coupled to two separate interrupts. For example, the system memory controller **14** may be responsive to the second state of the first memory module **10** by triggering execution of a first interrupt routine associated with a first interrupt, and may be responsive to the fourth state of the second memory module **26** by triggering execution of a second interrupt routine associated with the second interrupt. In yet other embodiments, the separate inputs of the memory controller **14** are internally operatively coupled to the same interrupt, or are operatively coupled to separate interrupts which trigger the same interrupt routine.

FIG. 3 shows a host computer system **16** including an example memory module **10** where the notification circuit **20** of the memory module **10** has another example configuration in accordance with certain embodiments described herein. In the example configuration of FIG. 3, the at least one first output **12** is operatively coupled to an error-out pin of the memory module **10**, and a multiplexor **42** drives the transistor **36** with either of a task_in_progress signal **44** or an error signal **46** (e.g., parity error signal). In one embodiment, for example, the multiplexor **42** may be configured to drive the transistor **36** with the task_in_progress signal **44** when the memory module **10** is in the initialization mode or is executing the at least one initialization sequence, and with the error signal **46** when the memory module **10** is in the operational mode. Thus, the memory module **10** can be advantageously configured to both perform the standard (e.g., JEDEC-specified) error reporting functionality via the error-out pin during the operational mode and provide the status notification functionality during the system initialization mode, as described herein. As shown in FIG. 3, a second memory module **26** including a similar configuration can also be operatively coupled to the host computer system **16**. In certain embodiments, the at least one second output **24** of the second memory module **26** can be operatively coupled to the at least one first output **12** by the bus **32**, as described above (e.g., with respect to FIG. 2).

FIG. 4 shows an example method **100** of using the at least one memory module **10** in accordance with certain embodiments described herein. While the description below of the method **100** refers to structure shown in FIGS. 1-3, other structures may also be used in accordance with certain embodiments described herein. At block **102**, the method **100** of certain embodiments comprises providing a first memory module **10** comprising at least one first output **12** operatively coupled to a memory controller **14** of a host computer system **16**. The first memory module **10** can be configured to operate in at least two modes comprising an initialization mode during which the first memory module **10** executes at least one initialization sequence, and an operational mode. For example, the at least one initialization sequence may comprise one or more steps of a series of steps associated with an initialization procedure of the host computer system **16**.

At block **104**, the method **100** in some embodiments comprises causing the first memory module **10** to enter the initialization mode. At block **106**, the method **100** of certain embodiments comprises driving the at least one first output **12** to a first state while the memory module **10** executes the at least one initialization sequence. Upon completion of the at least one initialization sequence, the method of certain embodiments comprises driving the at least one first output **12** to a second state different than the first state. In certain embodiments, the first state is a first logic level and the

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second state is a high impedance state. Additionally, in certain embodiments, the at least one first output **12** is operatively coupled to at least one interrupt of the memory controller **14** such that driving the at least one output **12** to the second state triggers the memory controller to execute an interrupt routine.

In certain embodiments, the at least one output **12** is operated in conformance with JEDEC standard when the first memory module **10** is in the operational mode, but is not operated in conformance with the JEDEC standard when the first memory module **10** is in the initialization mode. The at least one first output **12** of certain embodiments include an error-out pin of the first memory module, for example.

The method **100** can further include providing a second memory module **26** comprising at least one second output **24** operatively coupled to the memory controller **14**. The second memory module **26** can be configured to operate in one of at least two modes comprising an initialization mode, during which the second memory module **26** executes at least one initialization sequence, and an operational mode. The method **100** can further include causing the second memory module **26** to enter the initialization mode. In certain embodiments, the method **100** also includes driving the at least one second output **24** of the second memory module **26** to a third state while the second memory module **26** executes the at least one initialization sequence. Upon completion of the at least one initialization sequence, the method **100** can further include driving the at least one second output **24** of the second memory module **26** to a fourth state different from the third state.

In certain embodiments, the at least one first output **12** of the first memory module **10** and the at least one second output **24** of the second memory module **26** are operatively coupled together by a bus **32** which is also operatively coupled to at least one input **34** of the memory controller **14**. In certain other embodiments, the at least one first output **12** of the first memory module **10** is operatively coupled to a first input **34** of the memory controller **14** and the at least one second output **24** of the second memory module **26** is operatively coupled to a second input (not shown) of the memory controller **14**.

FIG. 5 shows another example method **200** of using at least one memory module **10** in accordance with certain embodiments described herein. At block **202**, the method **200** may include providing a memory module **10** comprising at least one output **12** operatively coupled to a memory controller **14** of a host computer system **16**. The memory module **10** may be configured to operate in at least two modes comprising an initialization mode, during which the memory module **10** executes at least one initialization sequence, and an operational mode.

The method **200** can further include causing the memory module **10** to enter the initialization mode at block **204**. At block **206**, the method **200** can include receiving a notification signal from the at least one output **12** of the memory module **10**. The notification signal may indicate that the memory module **10** has completed the initialization sequence, for example. In certain embodiments, the method **200** further comprises executing an interrupt routine by the memory controller **14** in response to the notification signal.

Terminology/Alternative Embodiments

Embodiments have been described in connection with the accompanying drawings. However, it should be understood that the figures are not drawn to scale. Distances, angles, etc. are merely illustrative and do not necessarily bear an exact

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relationship to actual dimensions and layout of the devices illustrated. In addition, the foregoing embodiments have been described at a level of detail to allow one of ordinary skill in the art to make and use the devices, systems, etc. described herein. A wide variety of variation is possible. Components, elements, and/or steps can be altered, added, removed, or rearranged. While certain embodiments have been explicitly described, other embodiments will become apparent to those of ordinary skill in the art based on this disclosure.

Conditional language used herein, such as, among others, “can,” “could,” “might,” “may,” “e.g.,” and the like, unless specifically stated otherwise, or otherwise understood within the context as used, is generally intended to convey that certain embodiments include, while other embodiments do not include, certain features, elements and/or states. Thus, such conditional language is not generally intended to imply that features, elements and/or states are in any way required for one or more embodiments or that one or more embodiments necessarily include logic for deciding, with or without author input or prompting, whether these features, elements and/or states are included or are to be performed in any particular embodiment.

Depending on the embodiment, certain acts, events, or functions of any of the methods described herein can be performed in a different sequence, can be added, merged, or left out all together (e.g., not all described acts or events are necessary for the practice of the method). Moreover, in certain embodiments, acts or events can be performed concurrently, e.g., through multi-threaded processing, interrupt processing, or multiple processors or processor cores, rather than sequentially.

The various illustrative logical blocks, modules, circuits, and algorithm steps described in connection with the embodiments disclosed herein can be implemented as electronic hardware, computer software, or combinations of both. To clearly illustrate this interchangeability of hardware and software, various illustrative components, blocks, modules, circuits, and steps have been described above generally in terms of their functionality. Whether such functionality is implemented as hardware or software depends upon the particular application and design constraints imposed on the overall system. The described functionality can be implemented in varying ways for each particular application, but such implementation decisions should not be interpreted as causing a departure from the scope of the disclosure.

The various illustrative logical blocks, modules, and circuits described in connection with the embodiments disclosed herein can be implemented or performed with a general purpose processor, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general purpose processor can be a microprocessor, but in the alternative, the processor can be any conventional processor, controller, microcontroller, or state machine. A processor can also be implemented as a combination of computing devices, e.g., a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration.

The blocks of the methods and algorithms disclosed in connection with the embodiments disclosed herein can be embodied directly in hardware, in a software module executed by a processor, or in a combination of the two. A software module can reside in RAM memory, flash memory,

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ROM memory, EPROM memory, EEPROM memory, registers, a hard disk, a removable disk, a CD-ROM, or any other form of computer-readable storage medium known in the art. An exemplary storage medium is coupled to a processor such that the processor can read information from, and write information to, the storage medium. In the alternative, the storage medium can be integral to the processor. The processor and the storage medium can reside in an ASIC. The ASIC can reside in a user terminal. In the alternative, the processor and the storage medium can reside as discrete components in a user terminal.

Certain embodiments described herein are compatible with a memory system including memory devices with various attributes (see, e.g., FIGS. 2 and 3). For example, the memory system of certain embodiments may include various data slice sizes (e.g., two, four, eight, or 16 bit data slices) and corresponding memories (e.g., memories having two, four, eight, or 16 bit data widths).

Although certain embodiments and examples are discussed above, it is understood that the inventive subject matter extends beyond the specifically disclosed embodiments to other alternative embodiments and/or uses of the invention and obvious modifications and equivalents thereof. It is intended that the scope of the inventions disclosed herein should not be limited by the particular disclosed embodiments. Thus, for example, in any method or process disclosed herein, the acts or operations making up the method/process may be performed in any suitable sequence and are not necessarily limited to any particular disclosed sequence.

Various aspects and advantages of the embodiments have been described where appropriate. It is to be understood that not necessarily all such aspects or advantages may be achieved in accordance with any particular embodiment. Thus, for example, it should be recognized that the various embodiments may be carried out in a manner that achieves or optimizes one advantage or group of advantages as taught herein without necessarily achieving other aspects or advantages as may be taught or suggested herein.

What is claimed is:

1. A memory subsystem operable with a system memory controller of a host system, comprising:

dynamic random access memory elements on a printed circuit board and configurable to communicate data signals with the system memory controller; and

a memory subsystem controller on the printed circuit board and coupled to the dynamic random access memory elements, the memory subsystem controller having an open drain output, wherein the memory subsystem is configured to provide a first signaling interface via the open drain output during normal operations and a second signaling interface via the open drain output during an initialization operation including initialization operation sequences, wherein the second signaling interface is distinct from the first signaling interface and the initialization operation is distinct from any of the normal operations;

wherein, during the normal memory read or write operations, the memory subsystem controller is configured to receive address and command signals associated with the memory read or write operations and to control the dynamic random access memory elements in accordance with the address and command signals, and the memory subsystem controller is further configured to output via the open drain output a parity error signal in response to a parity error having occurred during the normal memory read or write operations; and

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wherein, during the initialization operation, the memory subsystem controller is configured to output via the open drain output a signal related to one or more parts of the initialization operation sequences.

2. The memory subsystem of claim 1, wherein the memory subsystem controller includes a transistor having an open drain coupled to the open drain output, a source coupled to ground, and a gate;

wherein the memory subsystem controller is configurable to apply a first signal to the gate of the transistor to indicate a parity error having occurred during the normal memory read or write operations; and

wherein the memory subsystem controller is further configurable to apply a second signal related to one or more parts of the initialization operation sequences to the gate of the transistor during the initialization operation.

3. The memory subsystem of claim 2, wherein the second signal drives the open drain output from a first state to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.

4. The memory subsystem of claim 3, wherein the second signal drives the open drain output from the high impedance state to the low logic level and from the low logic level to the high impedance state.

5. The memory subsystem of claim 3, wherein the second signal drives the gate of the transistor high so as to drive the open drain output to the low logic level, and drives the gate of the transistor low so as to drive the open drain output to the high impedance state.

6. The memory subsystem of claim 5, wherein the first signal drives the gate of the transistor high to provide a low impedance path between the open drain output and ground.

7. The memory subsystem of claim 2, wherein the memory subsystem controller comprises an integrated circuit that includes the transistor.

8. The memory subsystem of claim 2, wherein the memory subsystem controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein the memory subsystem controller is configurable to couple the first input to the output during the normal memory read or write operations, and to couple the second input to the output during the initialization operation.

9. The memory subsystem of claim 1, wherein the dynamic random access memory elements are not accessed for any normal memory read or write operations by the system memory controller during the initialization operation.

10. The memory subsystem of claim 1, wherein the printed circuit board has edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the system memory controller, the edge connections including first edge connections via which the memory subsystem communicates data with the system memory controller, second edge connections via which the memory subsystem receives command/address signals from the system memory controller, and an open drain output pin coupled to the open drain output.

11. A method of operation in a host system having a system memory controller, comprising:

at a memory subsystem coupled to the system memory controller, the memory subsystem including a printed circuit board, a memory subsystem controller on the printed circuit board, and dynamic random access memory elements on the printed circuit board, the

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memory subsystem controller having an open drain output, wherein the memory subsystem is configured to provide a first signaling interface via the open drain output during normal operations and a second signaling interface via the open drain output during an initialization operation including initialization operation sequences, wherein the second signaling interface is distinct from the first signaling interface and the initialization operation is distinct from any of the normal operations,

performing the normal memory read or write operations, including receiving address and command signals associated with the memory read or write operations, controlling the dynamic random access memory elements in accordance with the address and command signals, and outputting via the open drain output a parity error signal in response to a parity error having occurred during the normal memory read or write operations; and

performing the initialization operation, including outputting via the open drain output a signal related to one or more parts of the initialization operation sequences.

12. The method of claim 11, wherein

the memory subsystem controller includes a transistor having an open drain coupled to the open drain output, a source coupled to ground, and a gate;

outputting via the open drain output a parity error signal includes applying a first signal to the gate of the transistor to indicate the parity error having occurred during the normal memory read or write operations; and

outputting via the open drain a signal related to one or more parts of the initialization operation sequences includes applying a second signal related to the one or more training sequences to the gate of the transistor during the initialization operation.

13. The method of claim 12, wherein the open drain output is driven by the second signal from a first state to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.

14. The method of claim 12, wherein the open drain output is driven by the second signal from the high impedance state to the low logic level and from the low logic level to the high impedance state.

15. The method of claim 12, wherein the second signal drives the gate of the transistor high so as to drive the open drain output to the low logic level, and drives the gate of the transistor low so as to drive the open drain output to the high impedance state.

16. The method of claim 15, wherein the first signal drives the gate of the transistor high to provide a low impedance path between the open drain output and ground.

17. The method of claim 12, wherein the memory subsystem controller comprises an integrated circuit that includes the transistor.

18. The method of claim 12, wherein the memory subsystem controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, the method further comprising coupling the first input to the output during the normal memory read or write operations, and coupling the second input to the output during the initialization operation.

19. The method of claim 11, wherein the dynamic random access memory elements are not accessed for any normal

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memory read or write operations by the system memory controller during the initialization operation.

20. The method of claim 11, wherein the printed circuit board has edge connections that fit into a corresponding slot of the host system so as to be in electrical communication 5 with the system memory controller, the edge connections including first edge connections via which the memory subsystem communicates data with the system memory controller, second edge connections via which the memory subsystem receives command/address signals from the sys- 10 tem memory controller, and an open drain output pin coupled to the open drain output.

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