

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner

Case IPR2025-00002

Patent 11,880,319

**PETITIONER'S AUTHORIZED
REPLY TO PATENT OWNER'S PRELIMINARY RESPONSE**

EXHIBIT LIST

Exhibit #	Description
1001	U.S. Patent No. 11,880,319
1002	File History of U.S. Patent No. 11,880,319
1003	Declaration of Donald Alpert
1004	Curriculum Vitae of Donald Alpert
1005	File History of U.S. Patent Application No. 15/088,115 (i.e., U.S. Patent No. 9,858,218)
1006	File History of U.S. Patent Application No. 13/942,721 (i.e., U.S. Patent No. 9,311,116)
1007	File History of U.S. Patent Application No. 12/815,339 (i.e., U.S. Patent No. 8,489,837)
1008	U.S. Provisional App. No. 61/186,799
1009	U.S. Patent Publication No. 2010/0042778 to Tanguay et al.
1010	U.S. Patent Publication No. 2003/0115427 to Roohparvar
1011	U.S. Patent Publication No. 2010/0202240 to Moshayedi et al.
1012	U.S. Patent Publication No. 2008/0256281 to Fahr et al.
1013	U.S. Patent Publication No. 2010/0142383 to Goishi et al.
1014	U.S. Patent Publication No. 2008/0098277 to Hazelzet
1015	JEDEC COMMITTEE LETTER BALLOT, LRDIMM DDR3 Memory Initialization Chapter Proposal (Dec. 2009) (“JEDEC”)
1016	U.S. Patent No. 8,139,430 to Buchmann et al.
1017	U.S. Patent No. 8,359,521 to Kim et al.
1018	U.S. Patent No. 8,407,441 to Giovannini et al.

Exhibit #	Description
1019	U.S. Patent No. 8,489,837 to Lee
1020	U.S. Patent No. 3,414,781 to Dill
1021	<i>SK hynix Inc. et al. v. Netlist, Inc.</i> , IPR2017-00548, Exhibit 1021, (PTAB December 11, 2017) (Deposition of Robert J. Murphy in 837 Patent IPR)
1022	U.S. Patent Application Pub. 2008/0147897 to Talbot
1023	U.S. Patent Application Pub. 2008/0155378 to Amidi
1024	JEDEC Standard, Double Data Rate (DDR) SDRAM Specification, JESD79 (June 2000) (“JESD79”)
1025	JEDEC Standard, FBDIMM: Architecture and Protocol (January 2007) (“JESD206”)
1026	JEDEC Standard, FBDIMM Advanced Memory Buffer (AMB) (March 2009) (“JESD82-20A”)
1027	U.S. Patent No. 7,411,862 to Hein et al.
1028	US Patent App. Publication No. 2006/0277355 by <u>Ellsberry</u> et al.
1029	JEDEC Standard, Low Power Double Data Rate (LPDDR) SDRAM Specification (August 2007) (“JESD209”)
1030	U.S. Patent Pub. No. 2007/0008791 to Butt
1031	U.S. Patent No. 9,535,623 (623 Patent)
1032	<i>SK hynix, Inc. et al. v. Netlist, Inc.</i> , IPR2018-00303, Paper No. 1 (PTAB December 14, 2017) (623 Patent IPR Petition)
1033	<i>SK hynix, Inc. et al. v. Netlist, Inc.</i> , IPR2018-00303, Exhibit 1003 (PTAB December 14, 2017) (Alpert Declaration in 623 Patent IPR)
1034	<i>SK hynix, Inc. et al. v. Netlist, Inc.</i> , IPR2018-00303, Paper No. 42 (PTAB March 21, 2019) (623 Patent Final Written Decision)

Exhibit #	Description
1035	<i>SK hynix Inc. et al. v. Netlist, Inc.</i> , IPR2017-00548, Paper No. 25 (PTAB May 3, 2018) (837 Patent Final Written Decision)
1036	JEDEC COMMITTEE LETTER BALLOT, DDR3 LRDIMM Design Specification Body (Dec. 2009)
1037	JEDEC, Compilation of Tallies for JC-40 CMOS Digital Logic and point committees (Dec. 4, 2009)
1038	File History of U.S. Patent Application No. 15/169,745 (i.e., U.S. Patent No. 9,535,623)
1039	Inphi Corporation, “MB Initialization sequence Item 142.35,” June 4, 2009
1040	U.S. Patent No. 8,386,737 to Jeon et al.
1041	Petitioner’s Reply, <i>SK hynix Inc. et al. v. Netlist, Inc.</i> , IPR2017-00548, Paper 14 (PTAB December 11, 2017).
1042	“Sequence,” https://www.lexico.com/en/definition/sequence
1043	U.S. Patent No. 7,222,213 to James
1044	Texas Instruments, “28-Bit to 56-Bit Registered Buffer with Address Parity Test One Pair to Four Pair Differential Clock PLL Driver” (October 2008)
1045	Micron, “ <i>High-Speed DRAM Controller Design</i> ” (2008)
1046	JEDEC, “ <i>Minutes of Meeting No. 158 JC-40 Digital Logic Committee</i> ” (June 4, 2009)
1047	<i>SK hynix Inc. et al. v. Netlist, Inc.</i> , IPR2017-00548, Exhibit 2009, (PTAB September 6, 2017)
1048	JEDEC, JEDEC Manual of Organization and Procedure, JM21P (Rev. of JM21N, May 2008) (May 2010)

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1049	JEDEC, JEDEC Manual of Organization and Procedure, JM21N (Rev. of JM21M, December 2006) (May 2008)
1050	Declaration of Julie Carlson
1051	JEDEC, “Committee Letter Ballot, JC-40.4-09-320, Item 142.35,” (Dec. 2009)
1052	JEDEC, “Committee Letter Ballot, JC-45.4-09-321, Item 2192.44,” (Dec. 2009)
1053	JEDEC, “Tally of Votes, Committee Letter Ballot, JC-45.4-09-321, 2192.44” (Dec. 9, 2009)
1054	Declaration of John Halbert
1055	Declaration of Sung Joo Park
1056	JEDEC Standard, DDR3 SDRAM, JESD79-3C (November 2008) (“JESD79-3C”)
1057	U.S. Patent No. 7,647,467 to Hutsell et al.
1058	<i>SK hynix Inc. et al. v. Netlist, Inc.</i> , IPR2020-1042, Paper No. 1 (PTAB June 8, 2020) (595 Patent Petition)
1059	<i>SK hynix Inc. et al. v. Netlist, Inc.</i> , IPR2020-1042, Paper No. 14 (PTAB December 17, 2020) (595 Patent Institution Decision)
1060	<i>SK hynix Inc. et al. v. Netlist, Inc.</i> , IPR2020-1042, Paper No. 25 (PTAB May 6, 2021) (595 Patent Termination Order)
1061	<i>Netlist, Inc. v. SK hynix Inc. et al.</i> , 6-20-cv-00194-ADA (W.D. Tex. March 12, 2021) (Claim Construction Order)
1062	<i>SK hynix Inc. et al. v. Netlist, Inc.</i> , IPR2020-1044, Paper No. 1 (PTAB June 8, 2020) (218 Patent Institution Decision)
1063	Netlist’s 8-K announcing patent cross license with Samsung on November 12, 2015

Exhibit #	Description
1064	Defendant Samsung's Motion for Judgment on the Pleadings in <i>Netlist Inc. v. Samsung Electronics Co., Ltd.</i> , No. 8:20-cv-00993, ECF No. 60 (C.D. Cal. June 22, 2021)
1065	Order denying Samsung's Motion for Judgment on the Pleadings in <i>Netlist Inc. v. Samsung Electronics Co., Ltd.</i> , No. 8:20-cv-00993, ECF No. 120 (C.D. Cal. Aug. 5, 2021)
1066	Plaintiff Netlist's Motion for Partial Summary Judgment in <i>Netlist Inc. v. Samsung Electronics Co., Ltd.</i> , No. 8:20-cv-00993, ECF No. 145 (C.D. Cal. Aug. 16, 2021)
1067	Complaint for Declaratory Judgment of Non-Infringement in <i>Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.</i> , No. 1:21-cv-01453 (D. Del. filed Oct. 15, 2021)
1068	First Amended Complaint for Declaratory Judgment of Non-Infringement and Unenforceability; Breach of Contract, <i>Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.</i> , No. 1:21-cv-01453 (D. Del. filed Jan. 18, 2022)
1069	Tektronix Application Note, <i>Electrical Verification of DDR Memory</i> (2009)
1070	Bruce Jacob et al., <i>Memory Systems: Cache, DRAM, Disk</i> (2008)
1071	JEDEC's 2009 Meeting Schedule (Apr. 6, 2009), https://web.archive.org/web/20090406143859/http://www.jedec.org/service_members/Meetings/09Sch.cfm
1072	JEDEC's Catalogue (Apr. 21, 2009), http://web.archive.org/web/20090421000459/http://www.jedec.org/Catalog/display.cfm
1073	Join JEDEC (Apr. 10, 2009), https://web.archive.org/web/20090410060243/http://www.jedec.org/join_jedec/default.cfm

Exhibit #	Description
1074	JEDEC Member Companies (May 5, 2009), https://web.archive.org/web/20090505225114/http://www.jedec.org/service_members/New_Members/memberco.cfm
1075	JEDEC Benefits (Apr. 13, 2009), https://web.archive.org/web/20090413045324/http://www.jedec.org/join_jedec/benefits.cfm
1076	Declaration by the Internet Archive for Exhibits 1071–75 (Aug. 5, 2022)
1077	Transcript of Deposition of Robert J. Murphy (Oct. 27, 2022)
1078	Redline comparing Declaration of Robert J. Murphy in IPR2022-00064 (595 Patent) [Ex. 1106] to Declaration of Robert J. Murphy in IPR2022-00062 (218 Patent) [Ex. 1105]
1079	Netlist’s Technology Tutorial
1080	[Replaced by Exhibit 1081] Annotation of DDR3 LRDIMM showing location of (1) Host Interface CA Clk-to-CMD Training, (2) MB Initialization, (3) MB-DRAM Training, and (4) Host-MB Training
1081	<u>Corrected</u> annotation of DDR3 LRDIMM showing location of (1) Host Interface CA Clk-to-CMD Training, (2) MB Initialization, (3) MB-DRAM Training, and (4) Host-MB Training
1082	Petitioner’s Demonstratives for Oral Argument on February 15, 2023
1083	JEDEC 21-C Standard, DDR SDRAM Registered DIMM (Jan. 2002)
1084	JESD79-2B, JEDEC DDR2 SDRAM Standard (Jan. 2005)
1085	JESD79-3, JEDEC DDR3 SDRAM Standard (June 2007) (Exhibit 1037 in IPR2018-00303)
1086	JEDEC’s Catalogue (July 27, 2004), https://web.archive.org/web/20040727032111/http://www.jedec.org/Catalog/display.cfm

Exhibit #	Description
1087	JEDEC download page for JESD99A.01 (Nov. 26, 2003), https://web.archive.org/web/20031126173530/ http://www.jedec.org/download/search/jesd99a01.pdf
1088	JEDEC Standard JESD99A.01, <i>Terms, Definitions, and Letter Symbols for Microelectronics Devices</i> (May 2003)
1089	Harold S. Stone, <i>Microcomputer Interfacing</i> (1982)
1090	U.S. Patent No. 8,386,722 to Wang et al.
1091	Deposition of John Bentley Halbert, III (July 22, 2022) [Exhibit 2022 in IPR2022-00062 and -00064]
1092	Deposition of Julie Carlson (July 22, 2022) [Exhibit 2024 in IPR2022-00062 and -00064]
1093	Deposition of Sung Joo Park (July 28, 2022) [Exhibit 2025 in IPR2022-00062 and -00064]
1094	U.S. Patent No. 9,311,116 (issued Apr. 12, 2016)
1095	U.S. Patent No. 9,858,218 (issued Jan. 2, 2018)
1096	File History of U.S. Patent No. 10,474,595
1097	U.S. Patent No. 10,474,595
1098	Petition of <i>Inter Partes</i> Review of U.S. Patent No. 9,858,218, IPR2022-00062, Paper No. 1 (PTAB Oct. 15, 2021)
1099	Declaration of Dr. Donald Alpert Regarding U.S. Patent No. 9,858,218, IPR2022-00062, Exhibit 1003 (PTAB Oct. 15, 2021)
1100	Petition of <i>Inter Partes</i> Review of U.S. Patent No. 10,474,595, IPR2022-00064, Paper No. 1 (PTAB Oct. 15, 2021)
1101	Declaration of Dr. Donald Alpert Regarding U.S. Patent No. 10,474,595, IPR2022-00064, Exhibit 1003 (PTAB Oct. 15, 2021)

Exhibit #	Description
1102	Final Written Decision, IPR2022-00062, Paper No. 54 (PTAB May 8, 2023) (U.S. Patent No. 9,858,218)
1103	Final Written Decision, IPR2022-00064, Paper No. 54 (PTAB May 9, 2023) (U.S. Patent No. 10,474,595)
1104	Order dismissing appeals of IPR2022-00062 and -00064, <i>Netlist, Inc. v. Samsung Electronics Co., Ltd.</i> , No. 23-2182 (Fed. Cir. Oct. 19, 2023)
1105	Declaration of Robert J. Murphy, Ex. 2027 in IPR2022-00062 (218 Patent)
1106	Declaration of Robert J. Murphy, Ex. 2027 in IPR2022-00064 (595 Patent)
1107	Deposition of Steven Przybylski (Feb. 15–16, 2024)
1108	Institution Decision, IPR2022-00062, Paper No. 14 (PTAB May 16, 2022) (U.S. Patent No. 9,858,218)
1109	Institution Decision, IPR2022-00064, Paper No. 14 (PTAB May 16, 2022) (U.S. Patent No. 10,474,595)
1110	U.S. Patent Application No. 12/144,396 to Wang (filed June 23, 2008)
1111	U.S. Patent No. 11,386,024
1112	File History of U.S. Patent No. 11,386,024
1113	<i>Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation</i> (June 21, 2022)
1114	Complaint for Declaratory Judgment of Non-Infringement in <i>Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.</i> , No. 1:23-cv-01122 (D. Del. filed Oct. 9, 2023) (U.S. Patent No. 11,386,024)

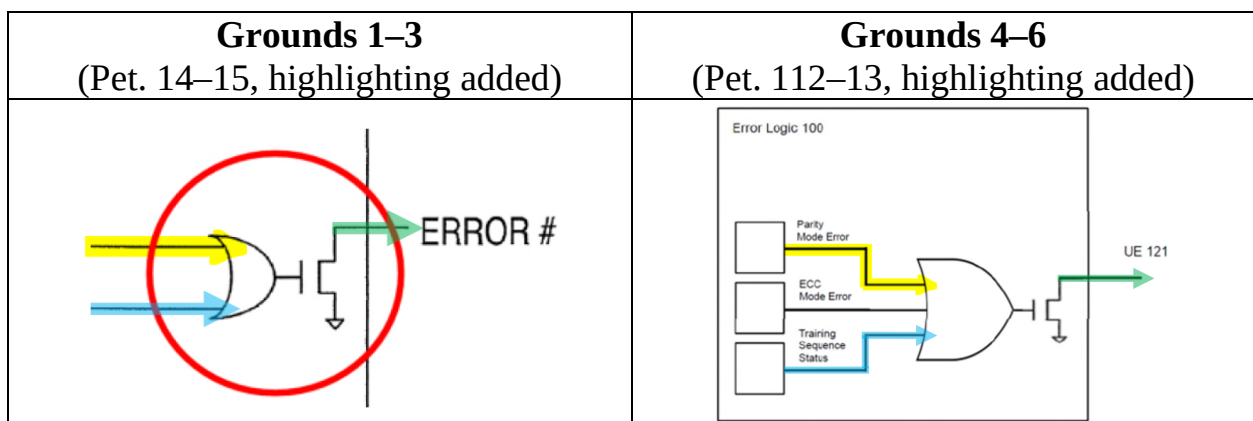
Exhibit #	Description
1115	Complaint for Declaratory Judgment of Non-Infringement in <i>Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.</i> , No. 1:24-cv-00614 (D. Del. filed May 22, 2024) (U.S. Patent No. 11,880,319)
1116	“Minutes of Meeting No. 160 JC-40 Digital Logic Committee,” December 10, 2009 [original non-confidential version of Exhibit 2002]
1117	“Simplified File Naming: JEDEC Meeting Presentations,” JEDEC, December 2010 [original non-confidential version of Exhibit 2005]
1118	JEDEC File Naming Convention, JM19.02 (Dec. 2005), <i>available at</i> < https://web.archive.org/web/20081118133245/http://www.jedec.org/Home/manuals/default.cfm >, < https://web.archive.org/web/20061210110839/http://www.jedec.org/Home/manuals/jm19-02.PDF >
2001	JESD82-30, “LRDIMM DDR3 Memory Buffer (MB) Version 1.0,” JEDEC, October 2014
2002	“Minutes of Meeting No. 160 JC-40 Digital Logic Committee,” December 10, 2009 [marked CONFIDENTIAL by Netlist]
2003	<i>Samsung Elecs. Co. v. Netlist, Inc.</i> , IPR2020-00062, Exhibit 2026 (P.T.A.B. Aug. 15, 2022)
2004	<i>Samsung Elecs. Co. v. Netlist, Inc.</i> , IPR2020-00062, Paper 53 (P.T.A.B. Mar. 8, 2023)
2005	“Simplified File Naming: JEDEC Meeting Presentations,” JEDEC, December 2010 [marked CONFIDENTIAL by Netlist]
2006	Email to JEDEC Request LRDIMM DDR3 Memory Initialization Chapter Proposal, January 2025

REPLY TO PATENT OWNER’S PRELIMINARY RESPONSE

For § 325(d), Netlist argues the Examiner did not materially err in allowing the 319 claims because they supposedly are “patentably distinct” from the cancelled ’623, ’218, and ’595 claims, POPR 20 (citing POPR 8–10), given the 319 claim language requiring “distinct” signaling interfaces (blue and yellow below), POPR 8–10. But Netlist ignores the express claim language requiring the *same* “open drain output” (green below) for *both* signaling interfaces:

319 claim language EX1001, 14:49–:56	Pet. 21 (highlighting added) (discussing Fig. 3 of the 319 Patent)
[1.d.1] wherein the memory subsystem is configured to provide a first signaling interface via the open drain output during normal operations and [1.d.2] a second signaling interface via the open drain output during an initialization operation including initialization operation sequences, wherein the second signaling interface is distinct from the first signaling interface	Figure 3 illustrates an exemplary memory module (10) with an open-drain output (12) whose transistor (36) is controlled by a multiplexor (42) driving the transistor’s gate with either (i) a task_in_progress signal (44) “when the memory module 10 is in the initialization mode or is executing the at least one initialization sequence,” or (ii) an error signal (46) to report parity errors during operational mode. EX1001, Fig.3 (below), 11:15-:34; EX1003, ¶59. The diagram shows a memory module 10 enclosed in a dashed box. An open-drain output 12 is shown as a green line exiting the module. Inside, a transistor 36 is connected to the output 12. The gate of transistor 36 is connected to a multiplexor 42. The multiplexor 42 has two inputs: a blue line labeled 44 (task_in_progress signal) and a yellow line labeled 46 (error signal). The output of the multiplexor 42 is connected to the gate of transistor 36. A label 18 points to the internal circuitry of the module.

Thus, the “interface (notifying) signal[s]” (EX1001, 4:9) above are materially identical to those in the cancelled ’218, ’595, and ’623 claims, which all claim **one** open drain output for two different signals as shown in Figure 3 above, *see* Pet. 21, 63–74, 110–15, which the Board has repeatedly found obvious in light of Grounds 2 and 5 here, *see* EX1102, 6–8, 51–53, 66–67, 71–75; EX1103, 6–9, 50–52, 71–73, 78–82; EX1034, 3–6, 9–21. Netlist argues the **individual** references in Grounds 1–2 and 4–5 were “cited” to the Examiner, POPR 14–16, but there was no discussion of the **combinations** here, so § 325(d) does not apply, Pet. 115–16. In particular, Netlist argued to the Examiner that Hazelzet **alone** “does not output any signals via the open drain outputs . . . for any purpose other than reporting [parity] errors during . . . normal . . . operations,” EX1002, 103–04, and thus Hazelzet **alone** does not teach the claim language above, *id.* 105. But neither Netlist nor the Examiner analyzed the **combinations** here, *see* Pet. 115–16, which all add a distinct “**second signaling interface** [blue arrow below] *via the open drain output* [green below]” to report training status, Pet. 14–15, 48 (citing pp.12–15), 67–69, 82–83, 112–15:



The Examiner then allowed the 319 claims on May 3, 2023, *see* EX1002, 120, a few days **before** the '218 and '595 Final Written Decisions invalidated materially identical claims as discussed above, *see* EX1003, ¶¶ 149–54; Pet. 116. The Examiner “materially erred” by issuing the 319 claims without “any analysis . . . of the Board’s decisions” and while being “silent” about Grounds 1–6. Pet. 116.

For Grounds 3 and 6, Netlist is incorrect that Wang is “cumulative.” POPR 17–20. Wang provides the motivation for a “*second signaling interface*” (e.g., via interface circuit 250) to report training status (blue arrows above), Pet. 42–44, 67–74, which is missing from Hazelzet as discussed above. Netlist argues JESD206 taught training, POPR 18–19, but during prosecution Netlist admitted that JESD206 (referred to as “JEDEC”) did **not** teach any “*second signaling interface*,” EX1002, 105; EX1003, ¶¶ 148–49. Wang is not cumulative to JEDEC in Grounds 1 and 4 given Netlist’s contention that JEDEC is “not prior art” and given Netlist’s admission that the Examiner “did not apply” JEDEC to the claims. POPR 19 n.4. And Wang is not cumulative to JEDEC or Buchmann in Grounds 1–2 and 4–5 because Wang **expressly** discloses a **motivation** for adding “buffering [of] data” and “corresponding training” to Hazelzet (e.g., to “provide higher memory performance,” “reduce or eliminate idle time,” and “higher capacity”), Pet. 43, which Netlist says is missing from JEDEC and Buchmann, EX1105, ¶¶ 111–18.

For Grounds 1 and 4, Netlist introduces new exhibits to argue that JEDEC

was not “publicly accessible.” POPR 32–54 (citing **EX2001–06**).

Netlist argues JEDEC (EX1015) “was never adopted by JEDEC—rather, a modified version [**EX2001**] was adopted,” POPR 34, 36–37 (citing **EX2002**/1116, 15), but Netlist fails to identify any substantive changes, *compare* **EX2001**, 65–72, *with* EX1015. Netlist merely points to non-substantive “editorial” changes, POPR 34, rather than any “technical modifications,” EX1049, 16, 18.

Netlist relies on a declaration suggesting that JEDEC (EX1015) was “confidential,” POPR 36 (citing **EX2003**, ¶¶20-21); *see also* POPR 41, but that declaration is “entitled to little or no weight,” 37 C.F.R. § 42.65(a), because it contradicts the official JEDEC Manual stating that “[o]pen discussion of balloted material is permitted and encouraged,” EX1048, 17; EX1049, 16, and it contradicts the testimony of Netlist’s technical expert that a POSITA (not just a member of JEDEC) would have “known about the contents of presentations and proposals to JEDEC relevant to memory modules and memory devices,” EX1077, 55:8–:20. Netlist’s declaration is highly misleading because it focuses on whether “**ballots** were treated as confidential,” POPR 36 (emphasis added); *see also* POPR 44–45, rather than whether the contents of the **proposal** being voted on were confidential, which is the relevant question for EX1015. In any democracy, the ballots and tally of votes are commonly kept confidential until the polls close, *cf.* **EX2003**, ¶ 20, but the **subject matter** of the vote (whether a JEDEC proposal, or a candidate for U.S.

President) is publicly accessible long before the polls open, so that interested members of the public can decide ahead of time how to vote. The same was true for EX1015, as explained in the Petition: “[A]s was typical, EX1015’s contents were discussed within JEDEC for months before the formal vote in November/December 2009, including at weekly ‘task group’ (TG) meetings where EX1015 was distributed and approved. EX1046, 1-2, 21-22 (#142.35); EX1091, 13:25-14:11, 26:4-27:13, 51:20-52:14; EX1093, 28:2-:13, 32:23-33:10, 35:11-:16.” Pet. 38–39; **EX2003**, ¶ 10. And EX1015 certainly was not confidential after being approved by vote as shown in the December 2009 minutes. **EX2002**/1116, 15.

Netlist also disputes that “anyone could join JEDEC,” POPR 43 (citing **EX2003**, ¶ 8), and complains that JEDEC would not give away free copies of its documents to a “third-party researcher” who was not a JEDEC member, POPR 52 (citing **EX2006**). But “anyone” is not the standard for public accessibility; “interested members of the relevant public” is the standard, Pet. 35–37 & n.6. Netlist argues membership at JEDEC is “*company based*,” POPR 43, but JEDEC also permitted “individual” members, EX1048, 1 & n.2; EX1049, 1 & n.2, and any POSITA “can create a company” to join JEDEC, **EX2004**, 23:23–25:10.

Netlist argues JEDEC “did *not* have search . . . until 2010,” POPR 50 (citing **EX2005**/1117, 3), but that is wrong, *see* Pet. 38 (“Search our Documents”).

Dated: Mar. 14, 2025

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CERTIFICATE OF COMPLIANCE

I hereby certify that this **Petitioner's Authorized Reply to Patent Owner's Preliminary Response**, excluding the parts of the brief exempted by 37 C.F.R. § 42.24, complies with the page limits provided by the Board's email on March 12, 2025, which stated: "Petitioner is authorized to file, within 5 business days, a 5 page pre-institution reply, limited to three pages addressing Patent Owner's arguments about discretionary denial under § 325(d), and 2 pages addressing the six exhibits filed by Patent Owner about the public accessibility of the JEDEC reference in Ground 1. Patent Owner is authorized to file, within 5 business days after Petitioner files the pre-institution reply, a 5-page pre-institution sur-reply, limited to three pages addressing Petitioner's arguments about discretionary denial under § 325(d), and 2 pages addressing Petitioner's arguments about the public accessibility of the JEDEC reference in Ground 1."

Dated: Mar. 14, 2025

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that on this 14th day of March, 2025, **Petitioner's Authorized Reply to Patent Owner's Preliminary Response** was served by email on the following counsel for Patent Owner:

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