UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

RUNERGY USA INC. ET AL.,

Petitioners,

v.

TRINA SOLAR CO., LTD.,

Patent Owner.

Case No. IPR2025-00006
U.S. Patent No. 10,230,009

DECLARATION OF DR. MARTIN PECKERAR

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I, Dr. Martin Peckerar declare as follows:

I. INTRODUCTION

1. I have been retained by Trina Solar Co., Ltd. ("Trina") as an independent expert consultant in this proceeding before the United States Patent and Trademark Office ("PTO"). I am not an employee of Trina or any affiliate or subsidiary of Trina.

2. I have been asked to consider whether certain references teach or suggest the features recited in certain claims of U.S. Patent No. 10,230,009, which I refer to herein as the "'009 patent."

3. My opinions and the bases for my opinions are set forth below.

4. I am being compensated at my ordinary and customary rate for my work, plus reimbursement for any reasonable expenses. My compensation is based solely on the amount of time that I devote to activity related to this case and is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other financial interest in this proceeding.

II. EDUCATION BACKGROUND, PROFESSIONAL EXPERIENCE, AND OTHER QUALIFICATIONS

5. My curriculum vitae ("CV") is attached hereto and provides an accurate identification of my background and experience.

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6. I am a specialist in the areas of materials science and technology and have applied these skills to the development of microelectronic circuits, specializing in light-matter interaction. I have applied these skills to the development of photoelectric devices such as radiation sensors, solar cells and camera chips.

7. I received a B.S. from SUNY Stony Brook in 1968, a M.S. from the University of Maryland in 1971, and a Ph.D. from the University of Maryland in 1975.

8. I began my career working in electronic circuit reliability assurance and failure analysis. Specifically, from 1968-1973, I was a Physicist at NASA Goddard, Greenbelt, MD. I performed component reliability studies for the first manned lunar program. At NASA's Goddard Space Flight Center, I developed e-beam characterization techniques for identifying failure mechanisms occurring in Schottky solar cells. I developed the first successful theory explaining the role of insulating films in open-circuit voltage enhancement of Schottky solar cells. Then, from 1973-1976, I was a Physicist at the Naval Research Laboratory, Washington, DC. I worked in x-ray spectroscopy (largely aimed at detecting environmental pollutants).

9. From 1976-1981, I was a Fellow Engineer at the Westinghouse Electric Company's Advanced Technology Laboratory, Baltimore, MD. At Westinghouse, I headed the Advanced MOS Technology Group. I designed and developed non-

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volatile memory systems and radiation-hardened components. I also invented the plasma source for EUV and x-ray lithography. I was lead process engineer on the Block Organized Random Access Memory chip. This was the first "radiation hard" memory system to be deployed in a nuclear battle environment. I developed a surface implant technology that eliminated the so-called "backside dead layer" impeding efficient UV sensing in rear-surface illuminated UV imagers. I am the inventor of the deep-depletion CCD imager used in x-ray and in short wavelength IR imaging. I developed the first CCD imager and read-out electronics demonstrated to be radiation hard out to 1 MRAD:Si while operating at 77K. This has been enabling technology in satellite imaging.

10. In 1980, I was appointed lecturer in the ECE department at the University of Maryland (College Park Campus). From 1981 to the present, a have been a Professor of microelectronic process technology and analog systems design. I am the author of the textbook Electronic Materials: Science and Technology (S.P. Murarka, co-author), the Korean Electronics Economy (with Mike Pecht) and Synthetic Microstructures for Biological Research (with Joel Schnur). From 1981-2002, I held joint appointments at the University and at the Naval Research Laboratory. Since 2002, I have been a full-time tenured Professor, and am currently a Professor Emeritus.

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11. From 1981-2002, I worked as a Branch Chief at the Naval Research Laboratory, Washington, DC. I headed the Interface and Thin Films Branch. My responsibilities included management of the Nanoelectronics Processing Facility as well as the Laboratory for Advanced Materials Synthesis. Here, I developed sensor materials for visible, IR, UV and x-ray imaging. I also was Navy Manager of the DARPA Advanced Lithography Program. I pioneered in the development of e-beam proximity effect correction – an enabling technology for today's microelectronic patterning technology.

12. From 2012 to the present, I have also co-founded two small businesses: FlexEl Battery, LLC and VersaVolt, LLC. FlexEl produced flexible power devices for empowering wearable electronic systems; VersaVolt is a consulting company working in the area of ultralow power electronic system design and development.

13. Across my career, I have had a number of additional experiences with semiconductors and silicon solar cell technology. These have included obtaining awards, authoring books, chapters, and journals, speaking at conferences, and serving as an expert witness in other matters.

III. ASSIGNMENT AND MATERIALS CONSIDERED

14. I have been asked to assess the '009 patent, including the state of the art when the '009 patent application was filed. I have also been asked to consider, analyze, and explain certain prior art to the '009 patent, including how that art relates

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to the challenged claims of the ’009 patent and to provide my opinion on the validity of certain of the claims in the ’009 patent.

15. The opinions expressed in this declaration are not exhaustive of opinions I may offer in the future regarding the claims of the ’009 patent. Therefore, the fact that I do not address a particular point should not be understood to indicate an agreement on my part with any position taken by Petitioner or its expert Dr. Banerjee in this proceeding.

16. I reserve the right to amend and supplement this declaration in light of additional evidence, arguments, or testimony presented during this IPR or related proceedings on the ’009 patent.

17. In forming the opinions set forth in this declaration, I have considered and relied upon my education, knowledge of the relevant field, knowledge of scientific and engineering principles, and my experience. I have also reviewed and considered the ’009 patent (Ex. 1001), the ’009 patent’s prosecution history (Ex. 1002), the Petition (Paper 1), the Board’s institution decision (Paper 11), and the following additional materials:

Exhibit	**Description**
Ex. 1003	Declaration of Dr. Sanjay Banerjee
Ex. 1005	File History of U.S. Patent No. 9,722,104
Ex. 1006	File History of U.S. Patent No. 10,014,419

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Ex. 1009	U.S. Patent App. Publication No. 2013/0056051 to Y. Jin, et al. ("Jin")
Ex. 1010	F.A. Lindholm, et al., Heavily Doped Polysilicon-Contact Solar Cells, IEE Electron Device Letters, Vol. EDL-6, No. 7, (IEEE 1985) ("Lindholm")
Ex. 1011	Y.H. Kwark, et al., N-Type SIPOS and Poly-Silicon Emitters, Solid-State Electronics, Vol. 30, No. 11, 1121-l 125 (1987) ("Kwark")
Ex. 1012	F. Feldmann, et al., "Passivated rear contacts for high-efficiency n-type Si solar cells providing high interface passivation quality and excellent characteristics," Solar Energy Materials & Solar Cells 120 (2014) 270-274 (2013 Elsevier B.V.) ("Feldmann")
Ex. 1013	U.S. Patent App. Publication No. 2014/0299187 to J. Chang, et al. ("Chang")
Ex. 1014	Japanese Patent App. Publication No. JP 2010-186862 to T. Watabe, et al. ("Watabe") with certified translation
Ex. 1015	U.S. Patent No. 8,647,914 to K. Seo, et al. ("Seo")
Ex. 1021	M. Quirk, et al., Semiconductor Manufacturing Technology (Prentice-Hall Inc. 2001)
Ex. 1022	A. Luque, et al., Handbook of Photovoltaic Science and Engineering (John Wiley & Sons Ltd. 2003)
Ex. 1023	Trina Solar n-type TOPCon Advanced technology steps onto the world stage, with efficiency reaching 26% in mass production and 700W+ in module power, available at https://www.trinasolar.com/us/trina-solar-n-type-vertex-to-reach-700gw (last visited August 19, 2024)
Ex. 1024	Y. H. Kwark, et al. SIPOS Heterojunction contacts to silicon, 1984 International Electron Devices Meeting (1984): 742-745 ("Kwark II")

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Ex. 1025	SY Lien, et al., Tri-layer antireflection coatings (SiO2/SiO2—TiO2/TiO2) for silicon solar cells using a sol-gel technique, Solar Energy Materials & Solar Cells 90, 2710-2719 (2006)
Ex. 1026	D. Kray, et al., Study on the edge isolation of industrial silicon solar cells with waterjet-guided laser, Solar Energy Materials & Solar Cells, 91, 1638–1644 (2007)
Ex. 1027	Merriam-Webster's Collegiate Dictionary, 10th Ed. (Merriam-Webster, Inc. 1998) (definition of "periphery")
Ex. 1028	S. Duttagupta, et al., Progress in Surface Passivation of Heavily Doped n-Type and p-Type Silicon by Plasma-Deposited AlOx/SiNx Dielectric Stacks, IEEE Journal of Photovoltaics, Vol. 3, No. 4 (October 2013)
Ex. 1029	Oxford College Dictionary, 2nd Ed. (Oxford University Press, Inc. 2002)
Ex. 1030	B. Streetman and S. Banerjee, Solid State Electronic Devices, 6th Ed. (Prentice-Hall Inc. 2006)
Ex. 1031	M. Scherff, Novel method for preparation of interdigitated back contacted a-Si:H/c-Si heterojunction solar cells, 26th European Photovoltaic Solar Energy Conference and Exhibition (2011)
Ex. 1032	W. Decker, et al., "Novel low pressure sputtering source and improved vacuum deposition of small patterned features using precision shadow masks," 59th Annual Technical Conference Proceedings (Society of Vacuum Coaters 2016)
Ex. 1033	H. Okuyama, et al., Position-selective growth of carbon nanotubes on Ni catalysts/Mo underlayers by thermal chemical vapor deposition, J. Mater. Res., Vol. 21, No. 11 (Materials Research Society 2006)
Ex. 1034	T. Saga, Advances in crystalline silicon solar cell technology for industrial mass production, NPG Asia Materials, Volume 2, 96–102 (2010)
Ex. 1036	U.S. Patent Pub. No. 2012/0003781 to Yun, et al. ("Yun")

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Ex. 2002	Transcript from the June 20, 2025 Deposition of Dr. Sanjay Banerjee
Ex. 2003	U.S. Patent No. 5,989,718 to Smith et al.
Ex. 2004	Yousuf et al., "A Review on TOPCon Solar Cell Technology," Current Photovoltaic Research 9(3) 75-83 (2021)
Ex. 2005	Yousuf et al., "Tunnel Oxide Deposition Techniques and Their Parametric Influence on Nano-Scaled SiO_x Layer of TOPCOn Solar Cell: A Review," Energies 2022
Ex. 2006	Glunz et al., "Silicon-based passivating contacts: The TOPCon route," Prog Photovolt Res Appl. 2021: 1-19 (2021)
Ex. 2007	Kreig et al., "Wet Chemical Poly-Si(n) Wrap-Around Removal for TOPCon Solar Cells," EPJ Photovoltaics 15, 9 (2024).
Ex. 2008	Yamaguchi et al., "Characterization of Tunnel Oxide Passivated Contact Fabricated by Sputtering and Ion Implantation Technique," Japanese Journal of Applied Physics 62 SK1024 (2023)
Ex. 2009	Christiansen, "Thermal Oxidation of structured Silicon Dioxide," ECS Journal of Solid State Science and Technology, 3 (5) N63-N68 (2014)

IV. UNDERSTANDING OF THE LAW

18. I am not an attorney, but I have been informed of several legal principles concerning patent validity, which I have employed in forming my opinions in this declaration.

19. I have been informed and understand that each patent claim is considered separately for purposes of validity and that a dependent claim that depends from another claim includes all of the limitations of the claim it depends from.

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20. I understand that the first step in comparing an asserted claim to the prior art is for the claim to be properly construed. I address how a person of ordinary skill in the art (a "POSITA") would have understood the claims of the alleged invention in Section V below.

21. I understand that a patent claim is only "obvious" when the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains.

22. In making an obviousness determination, I understand that there are several factors that must be considered: (1) the scope and content of the prior art; (2) the level of ordinary skill in the art at the time the invention was made; (3) the differences between the claimed invention and the prior art, if any, and (4) objective considerations, if any exist, such as any commercial success, copying, prior failure by others, licenses, longstanding need, and unexpected results.

23. I understand that a patent claim composed of several elements is not proved obvious merely by demonstrating that each of its elements was independently known in the prior art, whether those references were set forth in a single reference or in a combination of references. Instead, it must have been obvious to arrange those elements in the same way as the elements in the claim.

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24. I understand that either a single reference or multiple references may be the basis for finding that a claim is obvious. But the mere presence of claimed elements in the prior art is not enough. A patent challenger must show that there is a reason, suggestion, or motivation that would lead one of ordinary skill in the art to either modify the single reference or combine prior art references to arrive at the claimed subject matter.

25. I understand that there is no single way to define the line between true inventiveness on the one hand (which is patentable) and the application of common sense and ordinary skill to solve a problem on the other hand (which may not be patentable). Thus, when assessing obviousness, a number of different inquiries can be made and considered. For instance, market forces or other design incentives may be what produced a change in the technology of the prior art, rather than true inventiveness. I further understand that explicit teachings or suggestions in the prior art to make the modification or combination of elements claimed in the patent may be evidence of obviousness. Further, an innovation may be obvious if it applies a known technique that had been used to improve a similar device or method in a similar way. I understand that a claimed invention may be found to be obvious to try if the claimed innovation was one of a relatively small number of possible approaches to the problem with a reasonable expectation of success by those skilled in the art. But again, in all cases there must be a reason to arrive at the claimed

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subject matter. Likewise, reasons not to arrive at the claimed subject matter weigh against obviousness.

26. I also understand that it is improper to engage in hindsight when trying to determine the obviousness of a patent claim. Many true inventions might seem obvious with the benefit of hindsight. I understand that the obviousness inquiry must be conducted from the standpoint of a person of ordinary skill in the field at the time the claimed invention was made. What is known today, and what is learned from the teachings and disclosures of the patent itself containing the claim under analysis, should not be considered. Nor should one use the patent claim as a guide to picking out elements of the prior art for combination.

27. I understand that if a claim is not obvious, then the claims that depend from it are not obvious.

28. I provide my opinions in this declaration based on the guidelines set forth above.

V. LEVEL OF SKILL IN THE ART

29. I have been informed and understand that the level of ordinary skill in the relevant art at the time of the invention is relevant to inquiries such as the meaning of claim terms, the meaning of disclosures found in the prior art, and the reasons a POSITA may have for combining references.

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30. I have been informed and understand that factors that may be considered in determining the level of ordinary skill include: (1) the education of the inventor; (2) the type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) education level of active workers in the relevant field. I have been further informed and understand that a person of ordinary skill in the art (POSITA) is also a person of ordinary creativity.

31. I understand that Petitioner has proposed that a POSITA in the field of the ’009 patent would have had would have been someone with an advanced degree involving the disciplines of electrical engineering, applied physics, chemistry, or materials science, and at least two years of experience designing, developing, or researching in the field. Alternatively, that person would have had a bachelor’s degree in electrical engineering, applied physics, or materials science, and at least three years of experience designing, developing, or researching in the field. I have been asked to employ this definition.

32. Based on my education, training, and professional experience in the field of the claimed invention, as discussed in Section II, I am a person of more than the ordinary level of skill in the art.

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33. In forming my opinion, I have drawn on my academic background and professional experience. My opinions herein, however, were formed using the perspective of an ordinarily skilled artisan.

VI. THE '009 PATENT

A. Effective Filing Date

34. I understand that Petitioner and Dr. Banerjee have taken the position that the '009 patent has an effective filing date of August 31, 2015. I have been instructed to also employ this date.

35. My opinions in this declaration were formed from the perspective of a POSITA as of August 31, 2015, including both the knowledge of a POSITA at that time as well as how a POSITA would have understood the prior art.

B. Overview

36. The '009 patent relates to "a solar cell and a method for manufacturing the same." (Ex. 1001, 1:22-23.)

37. Solar cells "generates electric power from solar energy…." (*Id.*, 1:29-30.)

38. The '009 patent notes that prior art solar cells "include[] substrates made of semiconductors having different conductive types, such as a p type and an n type, a second conductive type semiconductor region (or emitter layer), and electrodes respectively connected to the substrates and the second conductive type semiconductor region." (*Id.*, 1:33-38.)

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39. This forms a "p-n junction" at the interface of the substrate and the second conductive type semiconductor region." (*Id.*, 1:38-40.)

40. When light strikes the solar cell, "a plurality of electron-hole pairs are generated from the semiconductors." (*Id.*, 1:41-42.) The electrons and holes move toward the n type and p type semiconductor regions, respectively, and are collected by electrodes electrically connected to the substrates and the second conductive type semiconductor region. (*Id.* 1:42-50.)

41. "The electrodes are connected by lines, thereby obtaining power." (*Id.* 1:50-51.)

42. The solar cell of the '009 patent also include a silicon oxide tunnel layer between the first surface of the semiconductor substrate and the first conductive type semiconductor region. (*Id.* 1:55-60.)

43. "Such a tunnel layer **160** may generate a tunneling effect. More specifically, the tunnel layer **160** may function as a kind of barrier for electrons and holes." (*Id.* 7:62-64.) "That is, the tunnel layer **160** may not transmit minority carriers. After the minority carriers are accumulated in a portion neighboring the tunnel layer **160**, only majority carriers having energy of a specific level or higher may pass through the tunnel layer **160**. The majority carriers having energy of a specific level or higher may easily pass through the tunnel layer **160** by a tunneling effect." (*Id.* 7:65-8:4.)

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44. The tunnel layer increases efficiency by preventing recombination of the electron and holes within semiconductor region. Solar cells with a tunnel layer like that in the '009 patent are often referred to as "TOPCon" or "Tunnel Oxide Passivated Contact" solar cells.

45. While TOPCon solar cells were known in the art before the '009 patent was filed, the patent discloses an improved TOPCon structure and method of manufacture.

46. In particular, in the '009 patent a "tunnel layer **160** can be easily formed because a separate patterning process is not required." (*Id.* 7:59-60).

47. When forming the solar cell, "the first conductive type semiconductor region **170** may be formed on the back surface of the tunnel layer **160**…." (*Id.* 8:50-53).

48. The '009 patent explains that when manufacturing a solar cell this way, the first conductive type semiconductor region **170** might contact second conductive type semiconductor region **120**, which can create a short-circuit where the electrons and holes recombine (rather than be collected) and, thus, reduce the efficiency of the solar cell:

> That is, when the second conductive type semiconductor region **120** is formed, the impurities of the second conductive type may be diffused into the side of or the edge of the back surface of the semiconductor substrate **100**, and thus the first conductive type semiconductor region

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> **170** and the second conductive type semiconductor region **120** may be unwantedly short-circuited in the side of or the edge of the back surface of the semiconductor substrate **100**.

(*Id.* 13:28-35.)

49. To avoid this, the patent goes on to describe—and then claim—a solution to prevent this unwanted short-circuit: an "isolation portion" that prevents contact between the opposite conductive type semiconductor regions.

50. "In the present embodiment, such a problem can be fundamentally prevented by removing the first conductive type semiconductor region **170** from the edge of the back surface of the semiconductor substrate **100**." (*Id.* 13:35-39.)

51. A key part of this is that the tunnel oxide is also excluded from this isolation portion. (*Id.*, 7:54-56 ("Such a tunnel layer **160** may be generally formed in portions other than an isolation portion I in the back surface of the semiconductor substrate **100**.")))

52. The '009 patent illustrates an example of this inventive TOPCon solar cell in FIG. 2, which is reproduced in annotated form below.

53. The solar cell may include base region **110** and emitter region **120** [shown in green].

54. In the claims of the '009 patent, silicon substrate **100** and emitter region **120** are of opposite conductive types (*e.g.*, if base region **110** is n-type then emitter region **120** is p-type). "The second conductive type semiconductor region **120**

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having the second conductive type has a conductive type different from that of the base region **110** and may form an emitter region forming a pn junction along with the base region 110." (*Id.* 10:18-22.)

55. First conductive n-type semiconductor region **170** [shown in red] is at the opposite side of the solar cell.

56. Tunnel layer **160** [shown in blue] separates the first conductive type semiconductor region **170** from base region **110**.

57. Because, as explained above, the manufacturing process of the '009 patent can result in second conductive type semiconductor region **120** extending along the sides of the solar cell (described in the specification but not shown in FIG. 2), the inventors included an isolation portion **I** (shown in the magnified portion of FIG. 2) that prevents contact by excluding both tunnel layer **160** and first conductive type semiconductor region **170**:

> That is, when the second conductive type semiconductor region **120** is formed, the impurities of the second conductive type may be diffused into the side of or the edge of the back surface of the semiconductor substrate **100**, and thus the first conductive type semiconductor region **170** and the second conductive type semiconductor region **120** may be unwantedly short-circuited in the side of or the edge of the back surface of the semiconductor substrate **100**. In the present embodiment, such a problem can be fundamentally prevented by removing the first

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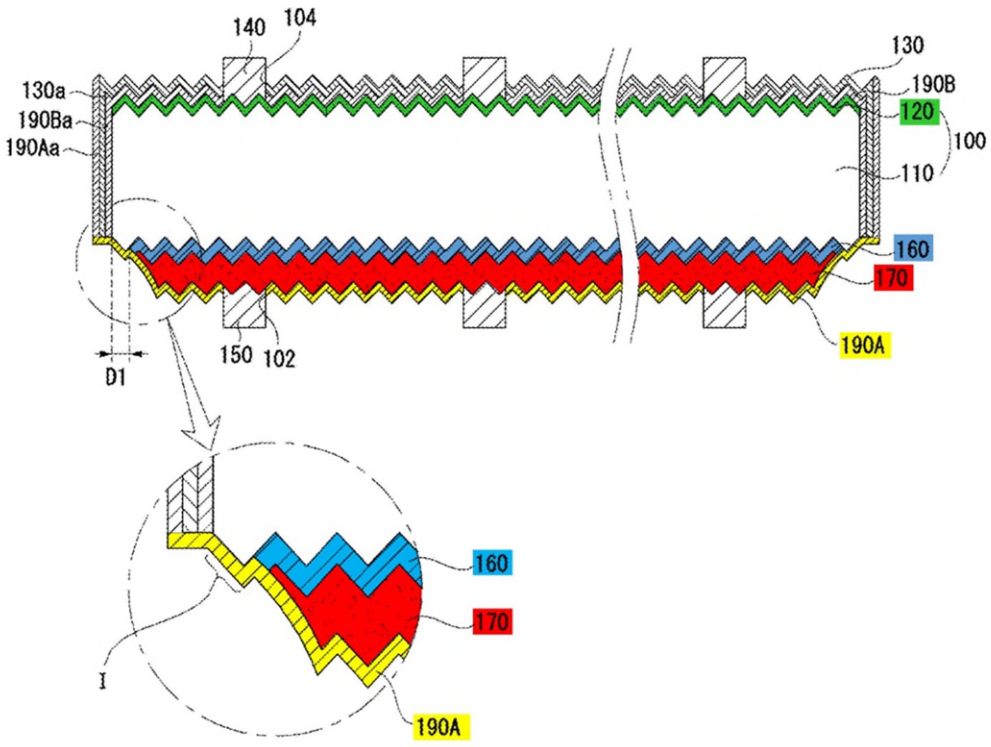
conductive type semiconductor region **170** from the edge of the back surface of the semiconductor substrate **100**.

(*Id.* 13:28-39).

58. Importantly, "tunnel layer **160** may be generally formed in portions other than an isolation portion I in the back surface of the semiconductor substrate **100**" and, thus, is also excluded in this isolation portion. (*Id.*, 7:54-56; *see also* 13:3-16.)

59. A first passivation film **190A** [shown in yellow] covers at least the isolation portion.

FIG. 2



(*Id.*, Fig. 2 (annotated).)

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60. All the ’009 patent claims require an “isolation portion [that] excludes the oxide layer and the polysilicon layer….” (Ex. 1001, 38:19-20.).

C. Claims

61. For reference, claims 1-17 of the ’009 patent are reproduced below. Of these, claim 1 is independent.

> **1**. A solar cell, comprising:
>
> a silicon semiconductor substrate having a first conductive type;
>
> an oxide layer on a first surface of the silicon semiconductor substrate;
>
> a polysilicon layer on the oxide layer and having the first conductive type;
>
> an emitter region at a second surface of the silicon semiconductor substrate opposite to the first surface and having a second conductive type opposite to the first conductive type;
>
> a first passivation film on the polysilicon layer;
>
> a first electrode connected to the polysilicon layer through an opening formed in the first passivation film;
>
> a second passivation film on the emitter region;
>
> a second electrode connected to the emitter region through an opening formed in the second passivation film; and
>
> an isolation portion for preventing a contact between the polysilicon layer and the emitter region,

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wherein the isolation portion excludes the oxide layer and the polysilicon layer, and is in an edge portion of the first surface of the silicon semiconductor substrate, and

the first passivation film covers the first surface of the silicon semiconductor substrate and the isolation portion together.

2. The solar cell of claim **1**, wherein the first electrode comprises a plurality of first finger electrodes spaced apart from each other and extended in parallel in a first direction, and

the second electrode comprises a plurality of second finger electrodes spaced apart from each other and extended in parallel in the first direction.

3. The solar cell of claim **2**, wherein the first electrode further comprises a first bus bar connected to the plurality of first finger electrodes, and

the second electrode further comprises a second bus bar connected to the plurality of second finger electrodes.

4. The solar cell of claim **1**, wherein the silicon semiconductor substrate is single-crystal silicon semiconductor substrate.

5. The solar cell of claim **1**, wherein the emitter region is formed by diffusing the impurities of the second conductive type into the second surface of the semiconductor substrate.

6. The solar cell of claim **1**,

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wherein the isolation portion is formed on at least one of the first surface, a side surface, or the second surface of the silicon semiconductor substrate.

7. The solar cell of claim **6**, wherein a width of the isolation portion is 1 nm to 1 mm.

8. The solar cell of claim **1**, wherein a thickness of the edge portion in the polysilicon layer progressively decreases toward the isolation portion.

9. The solar cell of claim **1**, wherein the first passivation film comprises a side portion extending up a side surface of the silicon semiconductor substrate.

10. The solar cell of claim **9**, wherein the second passivation film comprises a side portion formed on the side surface of the silicon semiconductor substrate, and

the side portion of the first passivation film on the side surface of the silicon semiconductor substrate is on the side portion of the second passivation film.

11. The solar cell of claim **1**, wherein the second surface of the silicon semiconductor substrate is a light incident surface, the first surface of the silicon semiconductor substrate is a back surface of the silicon semiconductor substrate, and the polysilicon layer forms a back surface field region.

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12. The solar cell of claim **3**, wherein all of the plurality of first finger electrodes and the first bus bar are connected to the polysilicon layer through the first passivation film.

13. The solar cell of claim **12**, wherein all of the plurality of first finger electrodes and the first bus bar have a single layer or double layer structure.

14. The solar cell of claim **12**, wherein:

the plurality of first finger electrodes have a single layer structure, and

the first bus bar has a double layer structure.

15. The solar cell of claim **1**, wherein the first and second passivation film are formed of a plurality of layers.

16. The solar cell of claim **1**, wherein a thickness of the polysilicon layer is more than a thickness of the first passivation film.

17. The solar cell of claim **1**, wherein a contact area in which the first electrode is connected to the polysilicon layer includes a plurality of metal crystals.

VII. CLAIM CONSTRUCTION

62. I am not a legal expert or an attorney and offer no opinions on the law. I understand that claim construction is a matter of law.

63. However, I have been informed by counsel of the legal standards that apply to claim construction in an *inter partes* review, and I have applied them in

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forming my opinions. I understand that during an *inter partes* review, the same claim construction standard used in federal district court is applied when addressing the meaning of claim terms.

64. I have been informed that the words of a claim are generally given the ordinary and customary meaning that the term or phrase would have to POSITA at the time of the invention in view of the surrounding claim language, the specification and the file history (collectively, the "intrinsic evidence" or "intrinsic record").

65. I also understand that courts may consider extrinsic evidence, such as expert and inventor testimony, dictionaries, and learned treatises (collectively, the "extrinsic evidence" or the "extrinsic record"), but that such extrinsic evidence should be given less weight than the intrinsic evidence.

66. In my opinion, the terms of the '009 patent's claims do not require further construction and can be afforded their plain and ordinary meaning for purposes of the analysis of the prior art that I am conducting in this declaration.

VIII. THE CLAIMS OF THE '009 PATENT ARE NOT OBVIOUS

67. As stated above, I understand that, under the law, in order for a patent to be found invalid as obvious, the differences between the claimed subject matter and the prior art are such that the subject matter as a whole must have been obvious at the time the invention was made to a POSITA.

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68. As I discuss below, it is my opinion that as of the effective filing date of the ’009 patent, a POSITA would have considered claims 1-17 of the ’009 patent to be non-obvious and patentable, including over the prior art identified by the Petition and Dr. Banerjee.

A. Identified Prior Art

69. The following paragraphs provide an overview of the main prior art references I discuss throughout this declaration.

1. Jin (Ex. 1009)

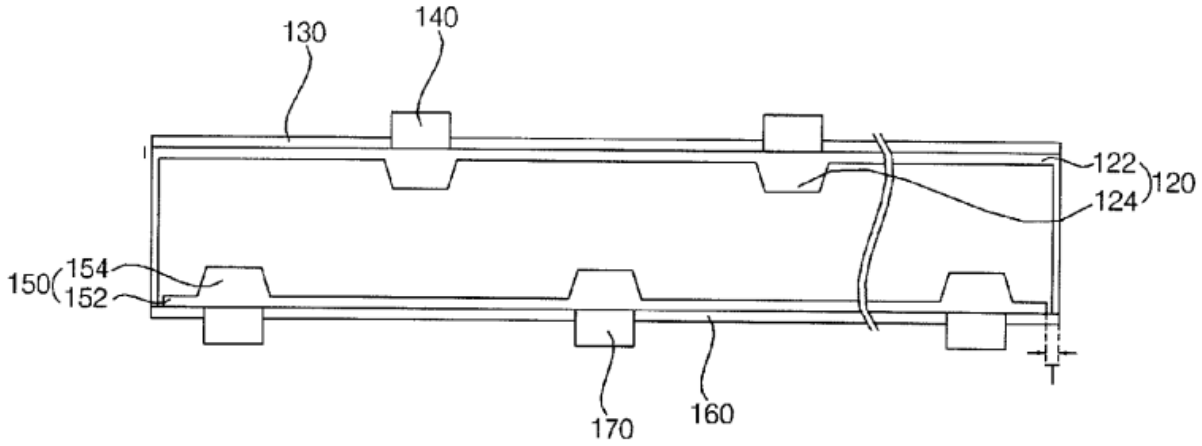
70. Jin (Ex. 1009) does not disclose a TOPCon solar cell or include a TOPCon oxide layer or polysilicon layer on the substrate.

71. Instead, Jin describes an old-fashioned solar cell where regions on the front and back-side of a semiconductor substrate (110) are doped with different impurities to create “an emitter layer **120** disposed on one surface of the substrate **110**… [and] a back surface field layer **150** on the other surface of the substrate **110**….” Emitter 120 and back surface field layer **150** are of opposite conductive types. (*Id.*, [0026].)

72. Figure 3 below provides an example of this:

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FIG. 3



(*Id.*, Fig. 3.)

73. Because it forms the front emitter and back field layer by directly doping the substrate, Jin is also able to include shallow doping areas in the emitter and back surface filed layers.

74. As Jin teaches, "it is very important to improve the efficiency" of solar cells (*id.* [0006]) and "[t]o achieve this and other objectives… the emitter [region] includes at least a first shallow doping area and the back surface field layer includes at least a second shallow doping area…." (*Id.*, [0008].)

75. Jin also recognized a tradeoff between the amount of impurities in the doped regions and the efficiency of the solar cell. As Jin explained, "where photons are converted to electron-hole pairs, it is advantageous to have a relatively low impurity density" but "where separated electrons or holes move toward the… finger

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lines…, it is more desirable to have a relatively high impurity density to reduce contact resistance." (*Id.*, [0031].)

76. To account for this, Jin included a shallow doped region where the photons are converted into electron-hole pairs (most of the solar cell surface) and a deeper doped region below the contacts to reduce contact resistance:

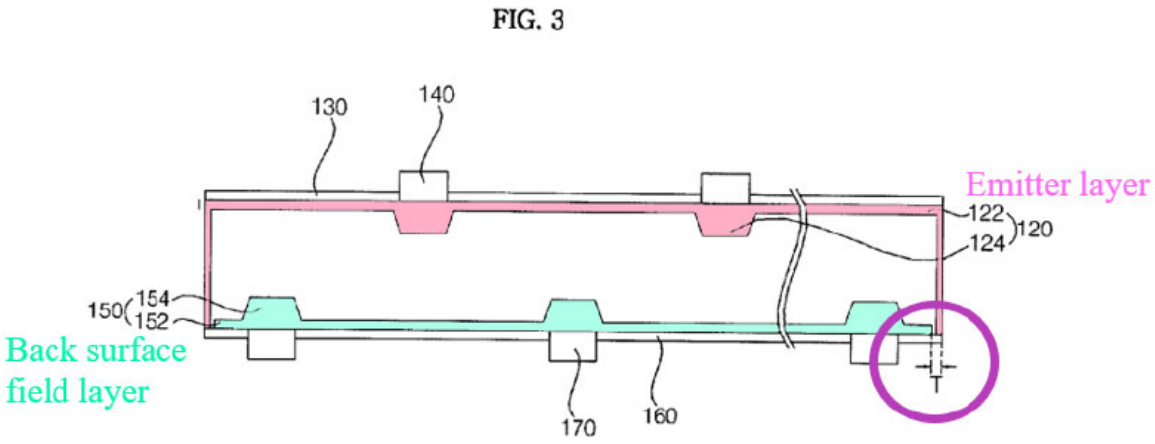
> [S]ince the doping density of the third area **154** of the back surface field layer **150** is larger than that of the fourth area **152**, contact resistance between the third area **154** and the rear finger lines **170** is reduced, and since the fourth area **152** is formed throughout the rear surface of the substrate **110**, recombination of electrons and holes may be effectively prevented or reduced. Therefore, since loss due to recombination of electrons and holes is reduced and at the same time, transfer of electrons and holes generated by the photovoltaic effect to the rear finger lines **170** is further expedited, photovoltaic conversion efficiency of the solar cell **100** may be greatly improved.

(*Id.* [0043].)

77. All of Jin's claims require that "the back surface field layer includes at least a second shallow doping area…." (*Id.*, claims 1, 12.)

78. Figure 3 of Jin, which Dr. Banerjee annotated and relied upon, shows the shallow doping areas (**152)** and thicker doping areas (**154**) in the back surface layer:

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Ex. 1003, ¶ 80 (reproducing and annotating Jin, Fig. 3).

79. Jin also uses masks to form the doped regions within its solar cell substrate. (Jin, [0077-0090].)

80. Use of a mask when doping the substrate allows Jin to form a gap T—circled in purple above—between back surface field (**150**) and the edge of substrate (**110**). (*Id.*, [0057]). This gap is formed within the substrate. (*See id.*, Fig. 3.)

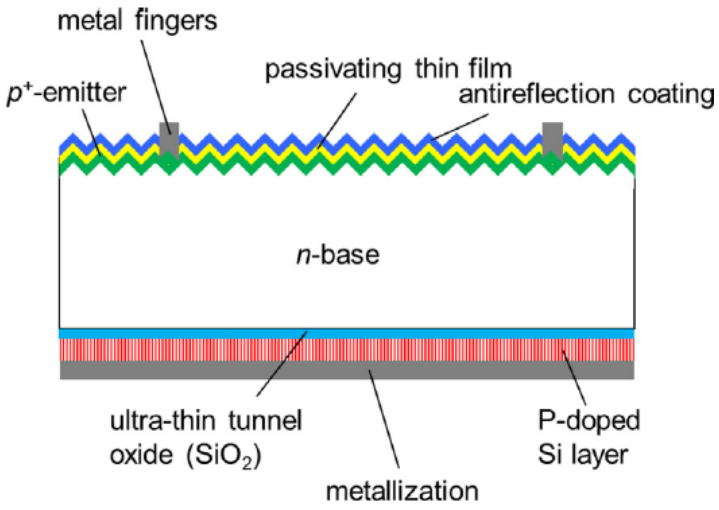
81. Jin does not disclose or suggest that its masks could be used to shape regions grown or deposited onto (not within) the substrate.

2. Feldmann (Ex. 1012)

82. In contrast to Jin, Feldmann (Ex. 1012) relates to an entirely different type of solar cell that "is based on an ultra-thin tunnel oxide (SiO_2) and a phosphorus-doped silicon layer." (Feldmann, Abstract).

83. According to Feldmann, this "significantly reduce the surface recombination at the metal-semiconductor interface." (*Id.*) Feldmann depicts this cell in the figure below:

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(Id. at 272.)

84. As depicted, Feldmann's "p^+-emitter" is completely separated from the "P-doped Si layer" and, consequently, these doped layers are not short-circuited and there is no need for an additional isolation portion.

85. Feldmann named this depicted solar cell "TOPCon (Tunnel Oxide Passivated Contact)" and identified three prerequisites that "are to be met: (i) excellent interact passivation, (ii) efficiently doped layers to maintain the quasi-Fermi level separation in c-Si (high V_{oc}), and (iii) an efficient majority carrier transport (high FFs)." (*Id.* at 270.)

86. Feldmann explains that the "tunnel oxide is a vital part" of the cell "that it is required to achieve excellent interface passivation for both open-circuit and maximum power point (MPP) conditions…." (*Id.*, Abstract).

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87. "Notably, the tunnel oxide is crucial to obtain very high passivation quality, since lifetime samples solely passivated by an as-deposited Si layer or an annealed Si layer (red circles in Fig. 1) yield very low iV_{oc} values." (*Id.* at 271.)

88. In contrast, "[t]he reduced passivation quality of the unpassivated lifetime samples (without tunnel oxide) leads thus not only to a lower iV_{oc} but also to a reduced iFF of about 83%." (*Id.*) "As expected, the V_{oc} of the solar cells with an unpassivated contact (without tunnel oxide layer) is drastically decreased to 638 mV due to a high J_{ob}=593 fA/cm^2." (*Id.* at 272).

89. As shown, Feldmann's TOPCon solar cell has metal finger contacts on its front (sun) facing surface but does not have point contacts on the backside. Instead, Feldmann has a "metallization" layer across that surface.

90. Feldmann explains that using such a metallization layer rather than point contacts increases the cell's efficiency. (*Id.* at 272 ("While the passivated contact's specific contact resistance takes a value of about 10 mΩ cm^2, its contribution to RS can be neglected since the rear is fully metallized. Thus, the relatively small loss in FF due to series resistance can be solely attributed to the solar cell's front side.")

91. Feldmann further explains that its metallization layer is important to the third "prerequisite" of high FFs: "Contrary to point contact rear side passivation schemes… its one-dimensional design facilitates processing (no structuring and

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alignment) and enables high FFs above 82% while maintaining a high V_{oc}." (*Id.* at 274.)

92. Feldmann also explicitly criticizes earlier approaches such as PERL cells "which feature a thick dielectric layer with a low index of refraction" with openings through which metal contacts connect to the doped region. As Feldmann explains, "the application of any insulating dielectric layer [between the metal and P-doped Si layer] would contradict the idea of our TOPCon structure and, thus, it would lose the inherent FF advantage of the one-dimensional junction design." (*Id.* at 273.)

3. Chang (Ex. 1013)

93. Chang (Ex. 1013) relates to a "solar cell including a semiconductor substrate." (Chang, [0003].)

94. Like Feldmann, Chang's solar cell includes "conductive type areas **20** and **30**" at opposite sides of the solar cell. (*Id.*, [0036].)

95. The cell also includes a "tunneling layer **40**" that is "interposed between the semiconductor substrate **10** and at least one of the conductive type areas **20** and **30**." (*Id.*)

96. This is shown in Figures 1 and 8 which are reproduced below:

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FIG. 1

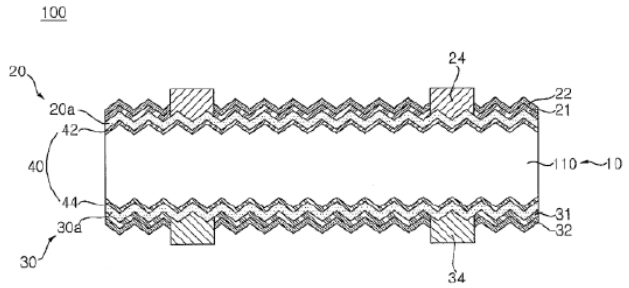
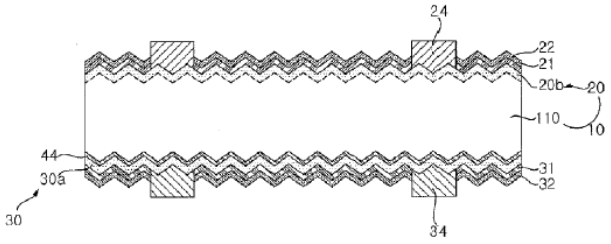


FIG. 8



(*Id.*, Figs. 1, 8.)

97. Chang also specifically teaches that "[b]ecause the emitter area **20** and the back surface field area **30** are not adjacent to each other, the necessity of performing an isolation process when the emitter area **20** and the back surface field area **30** are formed to be adjacent to each other is eliminated." (*Id.*, [0076].)

98. Chang recites the advantages of this: because no isolation process is required, the solar cell "manufacturing process is simplified and cost is thus reduced." (*Id.*)

B. <u>Summary of Opinions</u>

99. The Petition—and the Board's institution decision—references two primary combinations of prior art: (1) the combination of Jin and Feldmann and (2) the combination of Chang and Jin.

100. In combination (1)—discussed in Ground 1—the Petition argues that a POSITA would have replaced Jin's existing back surface field layer—which is

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formed by doping its substrate—with Feldmann's deposited tunnel oxide and doped polysilicon layers while applying Jin's backside "gap (or distance) T" to both of these layers. *See* Petition at 24-25.

101. In combination (2)—discussed in Ground 3—the Petition argues that a POSITA would have applied Jin's "gap (or distance) T" to Chang. *See* Petition at 53.

102. It is my opinion that both of these arguments are fundamentally flawed. They fail to take into account the actual teachings in the prior art, relevant technological limitations, and a POSITA's knowledge regarding tunnel oxides and TOPCon solar cells. Instead, they amount to nothing more than a hindsight based (and entirely improbable and impractical) attempt to reconstruct the '009 patent's claimed subject matter using the '009 patent itself as a guide.

C. Detailed Assessment of Ground 1

1. Jin and Feldmann Do Not Teach a Solar Cell with the Claimed "Isolation Portion"

103. To begin, Dr. Banerjee purports to combine two different types of references. Feldmann describes TOPCon solar cells. But Feldmann does not include the claimed ***"isolation portion."*** So, Dr. Banerjee relies on another reference that he believes includes the isolation portion (*e.g.*, Jin). But Jin does not relate to or describe TOPCon solar cells. Dr. Banerjee appears to ignore the fact that each of these references work without the modifications he now alleges would be obvious.

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There is no reason a POSITA would have been motivated to attempt to combine the references in the manner that Dr. Banerjee assumes.

104. Further, none of the cited prior art describes any problem that would be solved by the combination that Dr. Banerjee suggests. Specifically, Feldmann (Dr. Banerjee's TOPCon reference) does not describe or suggest a need to include the claimed isolation portion. And Jin (the reference Dr. Banerjee believes describes the claimed isolation portion) does not describe or suggest a need to include the TOPCon elements. Moreover, a POSITA at the time of the invention would not have been motivated to attempt to combine the references Dr. Banerjee identifies and, even if they were, that combination would not result in the structure that Dr. Banerjee assumes.

105. More specifically, Jin teaches a "solar cell and a manufacturing method for a solar cell" where "a thickness of an emitter layer and a thickness of a back surface field layer are different from each other." (Jin, [0003].)

106. Jin's emitter layer and back surface field layers are formed directly in the solar cell's silicon substrate by process of diffusion.

107. The annotated version of Figure 3 from Jin that is reproduced below provides examples of this.

108. According to Jin, "FIG. 3 is a cross-sectional view … along line B-B'" of Jin's solar cell. (*Id.*, [0025].)

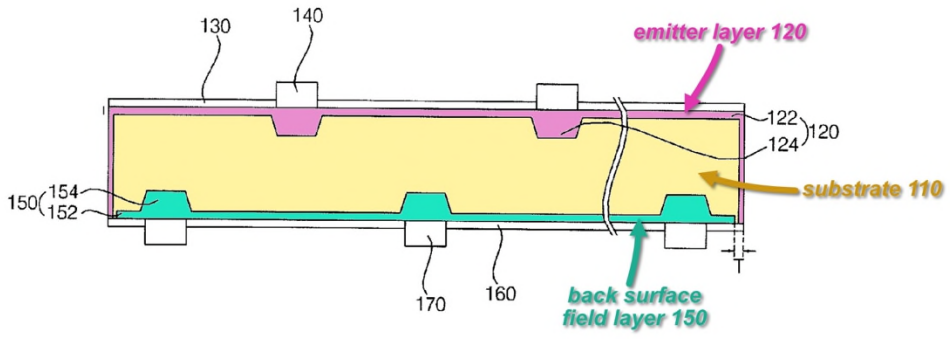
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109. As shown in this figure, the solar cell **100** includes "a silicon semiconductor substrate **110** of a first conductive type" (yellow annotation). (*Id.*, [0026].)

110. An "emitter layer **120**" is "formed" by "dop[ing]" the top surface of the "substrate **110**" "with a first impurity of a second conductive type opposite to that of the substrate **110**" (pink annotation). (*Id.*, [0029].) In one example, the "substrate **110** is a P-type" and "the emitter layer **120** is doped with an N-type impurity…." (*Id.*)

111. "The back surface field layer **150** is a high density doping area" (cyan annotation) formed in the substrate back "using a second impurity of the first conductive type which is the same type as the substrate **110**." (*Id.*, [0041].)

FIG. 3



(*Id.*, Fig. 3 (annotated).)

112. Jin also discusses the process of manufacturing this solar cell.

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113. Both the emitter layer and back surface field layer are formed by doping substrate **110** itself via "a heat diffusion method, a laser doping method, or an ion implantation method." (*Id.*, [0078], [0083]-[0084]; *see also id.*, Figs. 7-11.)

114. Moreover, because back surface field layer **150** is formed by doping the same substrate that already includes the emitter layer, Jin explains that it uses a "mask 410" when forming the back surface field layer to "cover[] or overlap[] a distance T measured from the edge part of the rear surface of the substrate 110." (*Id.*, [0083]-[0085].)

115. According to Jin, employing this distance T when doping Jin's substrate both (1) "prevent[ing] contact" between the back surface field layer 150 and emitter layer 120 (*see id.*, [0090]), and (2) inhibiting the impurities used during doping from "diffus[ing]" into the portion of the substrate between the layers (*id.*, [0058]-[0059]).

116. This in turn allows the "the back surface field layer 150 and the emitter layer 120" to "be kept from being shorted." (*Id.*, [0058].)

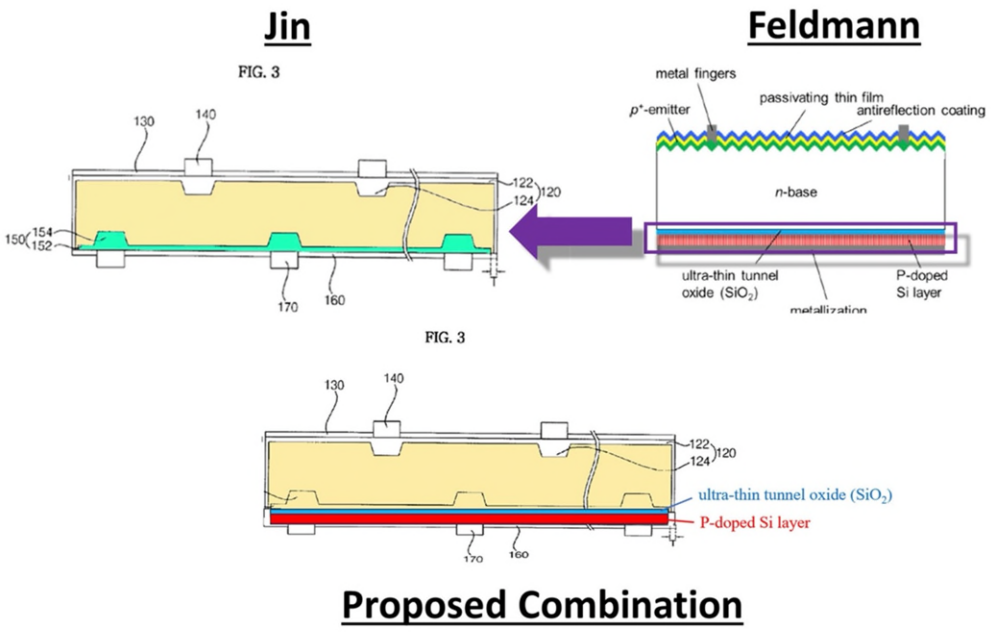
117. Jin explains that the "gap (or distance T)" should be in "the range from 2 to 300 μm." (*Id.*, [0060].)

118. Dr. Banerjee's (and Petitioner's) proposed a modified version of Jin that eliminates Jin's existing back surface field layer **150**.

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119. Rather than performing a doping process on the back side of the substrate, Petitioner and Dr. Banerjee argue that a POSITA would follow Feldmann's teachings and successively form a tunnel oxide layer and then a polysilicon layer on top of the substrate. *See* Petition at 24-25 (noting that a "tunnel oxide layer" and "polysilicon layer" have been applied to the "backside of Jin's solar cell substrate"); 27 (noting that both the "tunnel oxide layer" and "polysilicon layer" are "form[ed]" using a deposition process like "PECVD"); *see also* Ex. 1003, ¶ 108.

120. An example of this is shown below:



(Ex. 1003, ¶ 108.)

121. The Petition argues that—despite the differences between Jin and Feldmann (one employs substrate doping, the other layers formed on top of the substrate by some deposition technique)—a "metal shadow mask" would still be

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employed when forming the backside layers, causing the tunnel oxide and polysilicon layers to not be deposited in Jin's existing "gap-T isolation region." Petition at 27.

122. Feldmann's tunnel oxide is formed from silicon oxide (SiO_2). (Feldmann at Abstract.)

123. This tunnel oxide layer is "grown" on the rear surface of the substrate using a "wet chemical" process. (*Id.* at 271.)

124. The polysilicon—or "phosphorus-doped Si layer"—is then "deposited" on top of the already grown oxide. (*Id.*) Feldmann does not discuss masks.

125. In my opinion, a POSITA would not have combined Jin and Feldmann in the way identified in the Petition and by Dr. Banerjee.

126. As I noted above, Jin identifies two purposes for its gap (or distance) T.

127. First, the gap prevents layer **150** (which is created by doping the backside of the substrate) from physically contacting layer **120** (which is also created by doping the frontside of the substrate).

128. Second, the gap addresses impurities from layer **150** diffusing into the portion of the substrate located between layer **150** and layer **120** (which again are formed in and by doping opposing sides of the same substrate).

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129. Once layer 150 has been eliminated (as it is in Petitioner's and Dr. Banerjee's combination), there is no longer a doped layer in the backside of the substrate. Rather than being within the substrate, the backside polysilicon layer in the combination is no longer located in the substrate. Now, it is on top of it. Moreover, there is also a layer of tunnel oxide interposed between Jin's substrate and the polysilicon layer.

130. Because of this structural change, the two expressed reasons for including Jin's gap (or distance) T no longer directly apply.

131. First, there is no longer physical contact between a doped layer on the back of Jin's substrate and the frontside emitter layer **120**. Instead, there is now a tunnel oxide layer located between and physically separating the two layers.

132. Second, the ability of impurities in the polysilicon to diffuse into Jin's substrate (including into the space between the frontside emitter layer 120 and the backside layers) will be limited. Silicon dioxide is a well-known diffusion barrier. (Ex. 2003, 2:41-46 (explaining that an "oxide layer substantially prevents diffusion of dopants out of" one layer into another layer).) So, the tunnel oxide layer between the polysilicon layer and the substrate will operate to limit the diffusion of impurities into Jin's substrate.

133. Both Jin and Feldmann also teach that it is important to maximize the size of the solar cell's backside layer for efficiency purposes.

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134. According to Jin the "size of the back surface field layer" is "reduced," the "efficiency of the solar cell" is "degrade[d.]" (*See* Jin, [0060].) Doing this would be problematic as "it is very important" to design solar cells in a way that "improve[s] the efficiency." (*Id.*, [0006].)

135. Feldmann similarly explains that a solar cell must be designed to employ "highly efficient passivated contacts." (Feldmann at 270.) As part of this, Feldmann employs a "tunnel oxide" and "P-doped Si layer" that covers the entire rear surface of its "solar cell structure." (Feldmann at 272.)

136. Moreover, in addition to facilitating charge transport, the tunnel oxide has other benefits.

137. In particular, a POSITA would have understood that the layer "passivates the surface of the semiconductor substrate 10 having many recombination sites and facilities transfer of carriers through a tunneling effect." (Chang, [0057]; *see also id.* [0010] ("damage to the semiconductor substrate is prevented and recombination sites on the back surface of the semiconductor substrate are thus efficiently removed."). A POSITA would have understood that leaving the layer in place—and not removing it from the substrate edge—would have resulted in an improved device by better passivating the substrate's rear surface.

138. In my opinion, in view of all of this, a POSITA would not have removed Feldmann's tunnel oxide from Jin's gap (or distance) T. Instead, a POSITA would

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have formed the tunnel oxide such that it covers the ***entire*** rear surface of the substrate.

139. In my opinion, a POSITA would have recognized that maintaining the tunnel oxide across the entire substrate backside would have furthered Jin's expressed purposes for the gap (or distance) T. Leaving the tunnel oxide in place would have (1) better ensured that there is no physical contact between the polysilicon layer and the emitter layer 120 (the interposed oxide would prevent the polysilicon layer from ever reaching or touching the substrate surface) and (2) better limited diffusion of the impurities in the polysilicon layer into the substrate (as the oxide layer will act as a diffusion barrier).

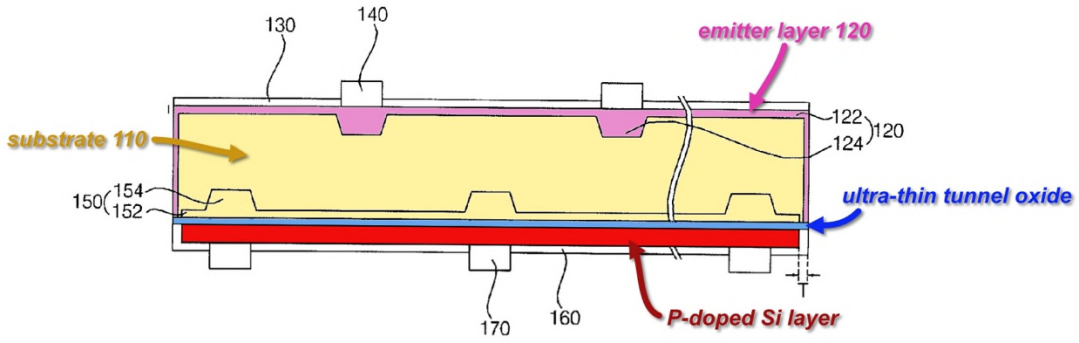
140. Moreover, because both Jin and Feldmann emphasize the importance of maximizing the efficiency of a solar cell, a POSITA would not have unnecessarily reduced the physical extent of the backside layers in the Jin and Feldman combination as Petitioner and Dr. Banerjee proposed.

141. A POSITA would instead would have maximized the size of the tunnel oxide such that it covers the entire rear surface of Jin's substrate. Doing so would have increased the efficiency of the combined solar cell as both Jin and Feldmann desire. Removing tunnel oxide from portions of the backside, however, would have resulted in unwanted surface recombination and reduced charge transport to the backside layer.

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142. A POSITA also would have recognized that as a general rule in semiconductor process technology, a bare silicon surface should not be left unpassivated after processing. Elemental silicon is highly chemically reactive. As such, the bare surface is a "magnet" for defects and contamination. Leaving the tunnel oxide in place across the entire substrate backside would reduce this problem.

143. The below demonstrative shows how a POSITA would have applied Feldmann to Jin. As shown, the new doped polysilicon layer has the same physical extent as the replaced doped backside layer 150 from Jin. The tunnel oxide covers the entire backside of the substrate as Feldmann teaches:



144. This structure does not satisfy the claims. The ***"oxide layer"*** is not ***"exclude[d]"*** from the ***"isolation portion"*** at the ***"edge"*** of the substrate as required.

145. Dr. Banerjee's explanation regarding why a POSITA would purportedly have removed the tunnel oxide layer from the "isolation portion" also lacks support.

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146. Dr. Banerjee first alleges that "Feldmann's solar cell, like Jin's is susceptible to shorting between the emitter and back surface field." (Ex. 1003, ¶ 116.)

147. According to Dr. Banerjee, because of this "the modified Jin/Feldmann solar cell would benefit from Jin's gap-T isolation region to prevent shorting." (*Id.*)

148. Dr. Banerjee provides no explanation of why he believes this would be the case. He cites nothing, includes no annotated figures, and offers no further details explaining why any purported "shorting" would occur.

149. I disagree that Feldmann's solar cell will necessarily be "susceptible to shorting" like that discussed in Jin. As I have explained, Feldmann's backside layers are not doped into Feldmann's substrate. Thus, the type of shorting discussed in Jin can no longer occur.

150. Moreover, the mechanism by which charge is transported through a tunnel oxide like that discussed in Feldmann is both complicated and subject to significant debate. Thin silicon oxide films can exhibit four types of structural anomalies that have a bearing on charge transport:

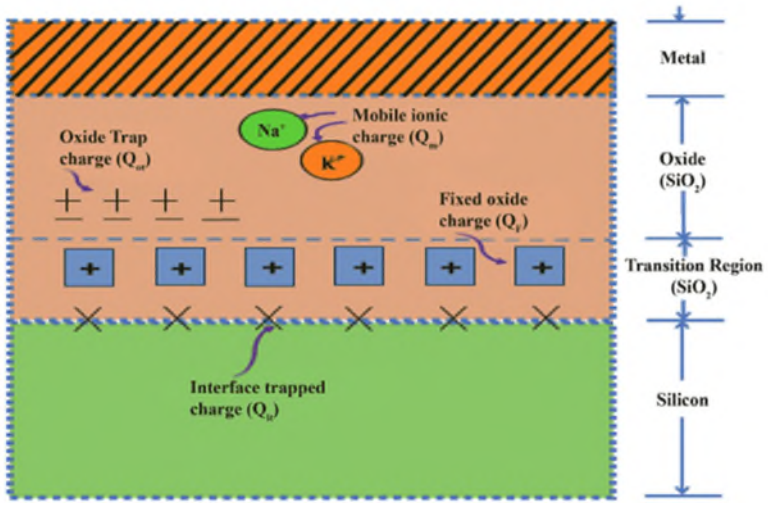
- Oxide trapped charge (Q_{ot}): These are generally oxygen vacancies (known as E' centers). E' center are oxygen defects in the bulk of the oxide. These charges are deep in the oxide bulk and cannot interact directly with charge stores of the semiconductor. The

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charge is "frozen" and will not move or respond to changes in electric field.

- Oxide fixed charge (Q_f): These are the same as the oxide trapped charges, but they are close to the oxide-semiconductor interface and can interact with the semiconductor bulk charge, changing charge state (slowly) as the bias is changed.
- Mobile charge (Q_m): These are extrinsic defects, like sodium, that carry some charge (positive in the case of sodium) and move under the influence of applied electric field.
- Interface charge: These, too, are oxygen vacancies. But they are at the oxide-semiconductor interface. They are frequently referred to as Pb centers. The interface states are "amphoteric" and can take on either positive or negative characteristics, depending on the nature of the local electric field (e.g., what is known as the "band bending" associated with this field).

These are all illustrated in the figure below (which is part of a book I authored in 1989 entitled "Electronic Materials: Science and Technology"):



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The nature, impact, and number of these different types of charge depends critically on the process used to create the silicon oxide layer. Time, temperature, thickness and ambient impurities create layers of different electrical conductivity and different surface generation recombination rates. So, it is not true that a tunnel oxide layer will necessarily (or even likely) create a "short" with Jin's topside emitter layer. Instead, this will occur only if the tunnel oxide is specifically manufactured in a way that allows this to happen (for instance, by including a significant amount of mobile charge carriers). No reasonable POSITA would have understood Feldmann's tunnel oxide to be formed in a way that would allow such "shorting" to occur.

151. Even if shorting were a concern in the combined structure, in my opinion a POSITA would have reduced the size of only Feldman's polysilicon layer while maintaining the tunnel oxide across the entire backside surface of the substrate.

152. Again, as I have explained, the manner by which charge is transported through a tunnel oxide can be controlled by adjusting manufacturing parameters such as time, temperature, thickness, and ambient impurities. A POSITA would plainly have adjusted these parameters to ensure that the tunnel oxide operates as intended (*i.e.*, minimizes recombinant losses while transporting charge carriers to the backside of the solar cell) while avoiding undesirable leakage current. Because

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unwanted leakage charge can be avoided via other means during manufacture, there would have been no reason to reduce the physical extent of the tunnel oxide.

153. Moreover, if the combined structure of Jin and Feldmann is implemented as shown above (with tunnel oxide existing in Jin's gap or distance T), there will be no short circuit.

154. Current cannot possibly flow from the doped polysilicon, through the tunnel oxide in the gap (or distance) T, and on to the frontside emitter. Jin's gap (or distance) T is "from 2 to 300 μm" (or 2000 to 300,000 nm). (Jin, [0060].) According to Feldmann, "tunnelling becomes inefficient" when the distance to be tunneled exceeds 20 Å (or 2 nm). (Feldmann, p, 271.) In other words, for there to be a short circuit, charge would need to tunnel towards the exterior of the solar cell over a distance that is orders of magnitude longer than possible. This, of course, will not occur.

155. Dr. Banerjee also opines that "[i]f the tunnel oxide layer were to extend to the edge, the exposed portions of the oxide could trap impurities and create negative fixed oxide charges, which could then create a p-type inversion in the n-type based substrate, leading to a leakage path to the p-type emitter on the front of the solar cell." (Ex. 1003, ¶ 116.)

156. Dr. Banerjee cites nothing in support of this proposition. None of the prior art or other references cited in the Petition say anything at all about "trap[ping]

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impurities," "negative fixed oxide charges," or "p-type inversion" associated with tunnel oxide layers.

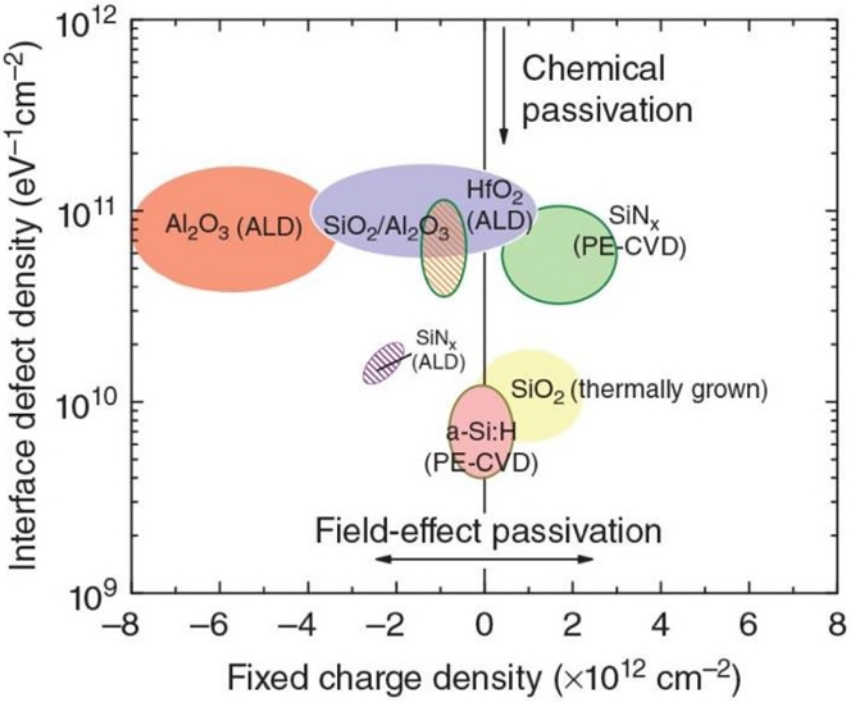
157. Not only is this unsupported, but it is also wrong.

158. To begin, the "exposed portions of the oxide" referenced by Dr. Banerjee is the approximately 1.4 nm thick layer of tunnel oxide visible on the side of the solar cell. This is an infinitesimally thin area whose geometry is too thin to allow lateral conduction.

159. Dr. Banerjee also appears to be arguing that incorporation of impurities into the oxide will produce a MOSFET-like structure, with the contaminated oxide acting as a MOS gate oxide leading to enhanced leakage. However, for there to be such a structure, the source and drain areas would need to be of the same type (i.e., both n-type or both p-type). Here, the tunnel oxide layer is located between an n-type polysilicon layer and p-type frontside emitter layer. No MOSFET-like structure can form because the source and drain are of different types. This is yet another reason why leaving the tunnel oxide in place (instead of removing it as Dr. Banerjee proposes) will operate to better block leakage current.

160. Next, Feldmann's tunnel oxide layer is formed from thermally grown silicon oxide. Thermally grown silicon oxide tends to have a positive fixed charge density:

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(available at https://www.researchgate.net/figure/Schematic-overview-for-interface-defect-D-it-and-fixed-charge-Q-f-densities-of_fig4_343280299)

161. This positive fixed charge will be maintained even if a small amount of impurities are absorbed resulting in negative oxide trapped charges. It would require significant impurity absorption to result in any meaningful negative fixed charge density. This is exceedingly unlikely given the process controls employed during solar cell manufacture. It is also unlikely given the exceedingly small amount of "exposed" tunnel oxide.

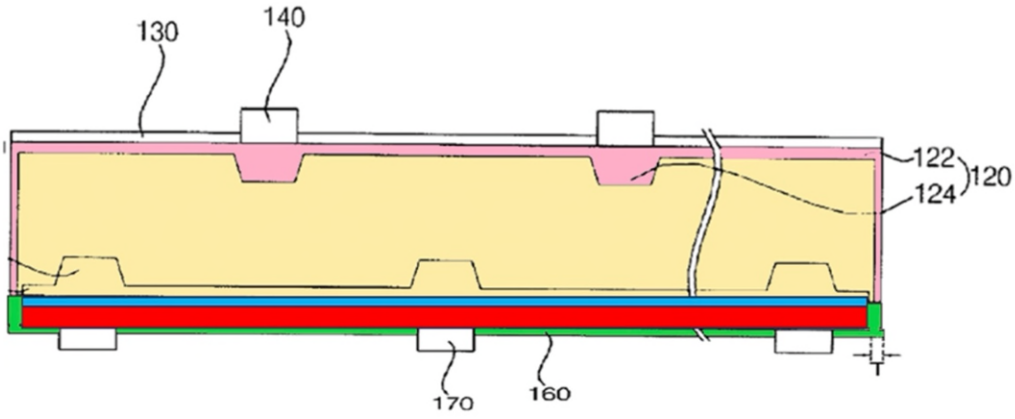
162. Moreover, aluminum oxide is also routinely used as a passivation layer in solar cells. (*See, e.g.,* Jin, [0050]; *see also* Ex. 1003, ¶ 173.) As shown above, aluminum oxide has a high negative fixed charge density (much higher than any

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negative fixed charge that would result if "impurities" are trapped in more positively charged silicon oxide). This shows that the type of "p-type inversion" referenced by Dr. Banerjee is entirely speculative and likely non-existent. If it were not, the art would not employ aluminum oxide passivation layers (as those layers have negative charge densities and would cause the type of issues Dr. Banerjee references). But the art does employ such passivation layers.

163. Next, in Dr. Banerjee's combination, the backside of the combined Jin / Feldmann structure is coated with a passivation film 160. The passivation film (shown in in green in Dr. Banerjee's demonstrative below) is located between the doped polysilicon layer (shown in red) and frontside emitter 120 (shown in pink):

Combination of Jin and Feldmann



(Ex. 1003, ¶ 138.)

164. Jin explains that this layer 160 can be formed from, among other things, a "silicon oxide." (Jin, [0050].)

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165. Because this passivation film is present in the gap (or distance) T, even if there were some sort of impurity trapping issue that somehow creates a "leakage path" (there is not as I have explained above), removing the tunnel oxide would not eliminate the issue. Instead, it would be equally present in the Petition's and Dr. Banerjee's proposed combination as silicon oxide would still be present in the same area.

166. Removing the tunnel oxide from the gap (or distance T) and replacing it with passivation film made from silicon oxide would have no impact whatsoever on any impurity trapping or "p-type inversion." Silicon oxide would be present in the gap (or distance T) in either case. And again, the charge state of this oxide would depend on the processing parameters used (e.g., time, temperature, ambient composition, etc.) It is unlikely that it would be negative, as the main type of oxide defect tends to be the E´ center, a positively charged oxygen vacancy.

167. Thus, removing Feldmann's tunnel oxide from the periphery of the combined device would not resolve the hypothetical problem identified by Dr. Banerjee: oxide would still be present in the same area and would still trap impurities resulting in the very same problems.

168. Put another way, Dr. Banerjee proposes removing one layer (the tunnel oxide) from a portion of the backside of Jin's substrate only to replace it with another

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layer (the antireflection/passivation layer 160) that exhibits the same problems and gives rise to the same concern.

169. So, not only has Dr. Banerjee pointed to a speculative, non-existent problem ("p-type inversion" resulting from impurity trapping) but his proposed solution does not even address that problem. This further confirms Dr. Banerjee's use of hindsight: he has identified no meaningful reason to remove the tunnel oxide from Jin's gap (or distance) T.

2. The Petition Proposes Use of a Technologically Infeasible Manufacturing Method

170. Next, in my opinion the Petition also proposes a technologically infeasible manufacturing method.

171. According to the Petition, a POSITA would have purportedly formed the combined structure of Jin and Feldmann by using a "metal shadow mask, in the shape of Jin's Fig. 9 mask, on the substrate to cover the periphery before forming the tunnel oxide and phosphorous-doped polysilicon layers using PECVD." Petition at 27.

172. It is use of this specific process that Petitioner argues would have resulted in "oxide and polysilicon layers" covering the entire substrate backside "with the exception of the gap-T isolation region." *Id.*

173. Dr. Banerjee does discuss a series of different manufacturing methods in his declaration. None of these are referenced in the Petition. I will discuss the

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Petition's proposed manufacturing method, and then address the other methods discussed by Dr. Banerjee.

174. A POSITA would not have employed a "metal shadow mask" at all when forming Feldmann's tunnel oxide and polysilicon layers. A POSITA most certainly would not have used the same mask during both deposition steps as Petitioner argues.

175. To begin, Feldmann itself does not employ such a process: Feldmann's tunnel oxide is "grown" on the rear surface of the substrate using a "wet chemical" process. (Feldmann at 271.)

176. The polysilicon—or "phosphorus-doped Si layer"—is then "deposited" on top of the already grown oxide. (*Id.*)

177. No mask is employed in either step.

178. While Jin does employ a metal mask, its mask is meant to facilitate "ion implantation" of an "impurity doped region" in a silicon substrate, not a CVD deposition process. (*E.g.*, Jin, [0009], [0079].)

179. A POSITA would have known that masks were also not routinely employed in the art during the formation of TOPCon solar cells.

180. "TOPCon solar cells mainly employ[ed] … PECVD oxidation, chemical oxidation, and ozone oxidation processes" to "deposit the thin layer of SiO_x" that forms the tunneling layer. (Ex. 2004 at 4.)

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181. The "polysilicon layer" was deposited over the entire substrate via "low-pressure chemical vapor deposition (LPCVD) … plasma-enhanced CVD (PECVD) … inline atmospheric pressure CVD (APCVD) … and sputtering…." (*Id.*)

182. This same manufacturing method—*i.e.*, thermal development of the tunnel oxide layer followed by deposition of the polysilicon layer using chemical vapor deposition without the use of a mask—is referenced repeatedly. (*See* Ex. 2004 at 76 (explaining that a TOPCon cell's "tunneling SiO_x" layer was typically "thermally developed" and the "poly silicon layer" was "accumulated in a LPCVD system."); Ex. 2006 at 3 (explaining that "[t]he n-TOPCon structure … was realized by growing a thin interfacial oxide in HNO_3" and then "depositing a phosphorus-doped Si Rich SiOx layer by plasma-enchanced chemical vapor deposition (PECVD)"); Ex. 2008 at 4 (similar).)

183. Not only was masking not routinely used when the '009 patent was filed, as late as 2024 the use of masks during deposition of a TOPCon cell's thicker polysilicon layer was still considered to be in the "idea" phase. (*See, e.g.*, Ex. 2007 at 1.)

184. Thus, even today a POSITA would not consider the use of such a process, or expect to succeed when doing so. A POSITA would most certainly have

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not employed masks in the way the Petition and Dr. Banerjee allege when the '009 patent was filed in 2015.

185. Next, as I have noted, Feldmann's tunnel oxide layer tunnel oxide is "grown" on the rear surface of the substrate. (Feldmann at 271.) Tunnel oxide layers were also thermally developed. (*See, e.g.*, Ex. 2004 at 76.) Even if a mask were employed, neither process would result in a tunnel oxide with the physical dimensions referenced by Petitioner and Dr. Banerjee.

186. As Dr. Banerjee recognizes, during a "metal 'shadow' mask process[,] … a metal mask is placed very close to the surface of the substrate but remains detachable." (Ex. 1003, ¶ 161.) Moreover, "[a] Skilled Artisan would have understood, the metal mask is not perfectly abutting against the substrate surface, but rather is a very small distance from the surface." (*Id.*, ¶ 162.) This allows material to "collect" beneath the mask. (*Id.*)

187. Because the tunnel oxide layer is not deposited via either chemical vapor deposition or sputtering—instead it is grown from the silicon substrate surface—a metal shadow mask will have minimal impact on the shape of the tunnel oxide.

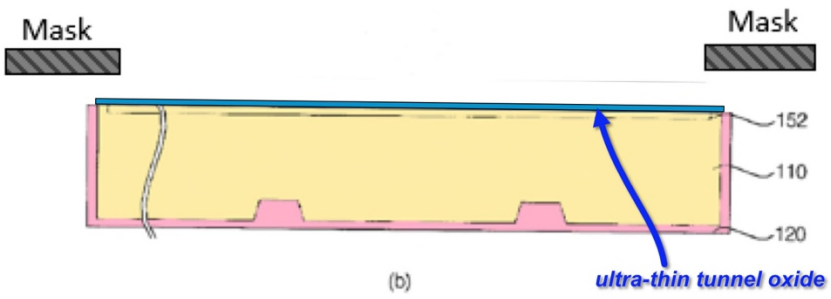
188. So, for instance, using the wet chemical process of Fetterman, liquid will proceed under the mask resulting in tunnel oxide forming over the entire

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exposed surface of the silicon substrate (including the gap or distance T covered by the mask).

189. Likewise, if the tunnel oxide is thermally grown, oxide will form over any portion of the silicon substrate exposed to an oxygen-containing atmosphere, including the portion of the substrate under the mask (including the gap or distance T covered by the mask).

190. This is shown in the demonstrative below:



191. As I have explained, this is not what the claims require. The tunnel oxide is located in the ***"isolation portion"*** it is not ***"exclude[d]"*** from it.

192. Next, a POSITA would have considered it technologically infeasible to attempt to deposit the tunnel oxide layer through a mask using chemical vapor deposition or another similar process rather than growing or developing this layer directly on the substrate surface.

193. Indeed, in my opinion a POSITA would have considered the use of a shadow mask to form a TOPCon cell's tunnel oxide layer to be virtually impossible.

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194. Masks can be used to form, for instance, "~10 μm thick … layers" on solar cells. (*E.g.*, Ex. 1031 at 2126; *see also* Ex. 2009 at N63 (referencing the formation of "205 ± 12 nm thick oxide in [an] etched mask window[]").)

195. The tunnel oxide layer is "an extremely thin coating of approximately 2 nm." (Ex. 2005 at 9.) Relying on a shadow mask to pattern such a layer is infeasible for reasons discussed below.

196. A POSITA would have recognized that use of a shadow mask when forming the tunnel oxide layer would likely result in significant layer variation around the mask edges, caused by variation in the thickness of the separation between the mask and the work-piece. This would worsen device uniformity and performance. A shadow mask would not provide the requisite degree of control and repeatability, especially given the dimension of the isolation portion, which could be as little as 1 nm. (*E.g.*, Ex. 1001, 2:34-35.) It simply would not have been possible to control the layer's physical extent in the manner proposed by Petitioner and Dr. Banerjee.

197. Showing this, no TOPCon cell manufacturer or researcher had—or even could have—employed a masking process that even remotely resembles that proposed by Petitioner and Dr. Banerjee. This is reflected by the various exhibits I discuss above summarizing known TOPCon cell manufacturing processes. (*See* Exs. 2004, 2006, 2008.)

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198. Because Petitioner and Dr. Banerjee proposed use of a process that was not only unlikely to result in the claimed subject matter, but was also atypical, not used in the industry, and presented significant technological hurdles, Petitioner and Dr. Banerjee have failed to show that a POSITA would have had a reasonable expectation of success.

199. Rather than employing the convoluted process Petitioner proposes, in my opinion, a POSITA would have instead manufactured the combined TOPCon cell of Jin and Feldmann using the processes actually taught in the art.

200. First, a tunnel oxide would be formed over the entire backside of the substrate in a separate, maskless processing step (such as thermal oxidation). This process would be carefully controlled to ensure uniformity and proper layer thickness. This process would be carefully controlled to ensure uniformity and proper layer thickness and optimized to minimize defects and impurities in the layer thus provided.

201. Then, the polysilicon layer would have been formed over the entire substrate backside in another maskless processing step (such as CVD deposition).

202. While a POSITA may have etched away excess polysilicon from the top and sides of the solar cell after deposition, this etching process would have left the tunnel oxide behind. (*See, e.g.*, Ex. 2007 at 3 (noting that only "the poly-Si layer" is removed from unwanted areas of the solar cell).)

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203. Indeed, despite its thin nature, the silicon oxide layer would act as an etching mask during this process. (*See id.* at 2.) The fact that polysilicon can be selectively etched over thin silicon dioxide is witnessed by the fact that gate sidewall spacer technology (routinely used in CMOS gate processes to minimize hot electron damage) relies on this selectivity for its success.

204. The resultant device would lack the claimed ***"isolation portion"*** that ***"excludes"*** the "***oxide layer."***

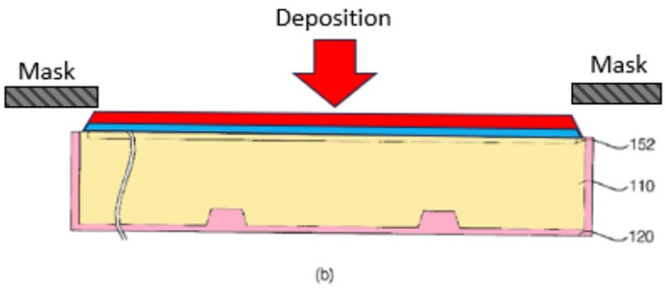
205. Instead, there would be tunnel oxide located within the edge region of the substrate. (*See id.*)

206. Next, even if a POSITA did somehow manage to overcome the technological hurdles of depositing an ultra-thin tunnel oxide layer through a metal shadow mask, the Petition's and Dr. Banerjee's proposed manufacturing method would ***still*** be unlikely to result in the type of structure depicted in the Petition and by Dr. Banerjee.

207. As both the Petition and Dr. Banerjee recognize, when depositing layers through a mask, "overspray" occurs at the mask boundary. *See* Petition at 71-72; Ex. 1003, ¶¶ 161-162. This "overspray" results in deposited layers accumulating "beneath the edge of the mask." *Id.*

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208. Petitioner's expert Dr. Banerjee included the following figure in his declaration which attempts to show this "overspray" when Feldmann's layers are applied to Jin:



(Ex. 1003, ¶ 165.)

209. When depositing a layer using deposition techniques like CVD or sputtering, layer thickness is controlled primarily via deposition time. A thicker layer is achieved by depositing the same material for a longer time. A thinner layer is achieved by depositing the material for a shorter time.

210. Ultra-thin layers—like Feldmann's tunnel oxide—will thus require only very short deposition times.

211. Thicker layers—like Feldmann's polysilicon layer—will thus require much longer deposition times.

212. Further, Dr. Banerjee testified during his deposition that the "overspray" that occurs under mask edges will continue to increase until the mask aperture (*i.e.*, the opening into which material is being deposited) is filled. (*See* Ex. 2002, 59:10-60:16.) I agree with this testimony: a deposited layer will increasingly

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penetrate under a mask, resulting in more overspray, until the layer reaches the bottom surface of the mask and fills the mask's opening.

213. Because the amount of "overspray" can increase with deposition time, if one did somehow manage to use the same shadow mask when producing Feldmann's ultra-thin tunnel oxide and much thicker doped polysilicon layer as the Petition and Dr. Banerjee propose, this would likely have resulted in a polysilicon layer extending ***over*** the tunnel oxide layer.

214. This is because the shorter deposition time of the silicon oxide will result in less overspray than the longer deposition time of the polysilicon layer.

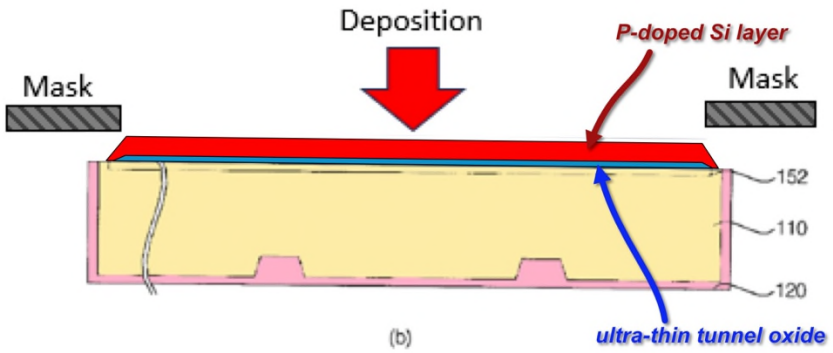
215. More specifically, Feldmann's tunnel oxide is very thin (~14 Å or 1.4 nm). (Feldmann at 271.) The polysilicon layer is much thicker (20 nm). (*See id.*)

216. The ultra-thin tunnel oxide will fill only a portion of the mask's aperture. There will be little overspray due to the layer's thinness and shorter deposition time.

217. The thicker polysilicon layer requires a longer deposition time and will fill the mask's aperture. This will result in more overspray.

218. Thus (and once again if this type of process were even possible, which it is not), rather than producing the layered structure referenced in the Petition and by Dr. Banerjee, the following would be more likely result:

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219. As shown, the thicker polysilicon layer with increased overspray results in the very thing the Petition seeks to avoid: polysilicon on the substrate in close proximity to Jin's emitter layer 120.

220. A POSITA would have recognized that forming the tunnel oxide without a mask and across the entire substrate surface (again, as I have explained, this was routinely done in the prior art) would have eliminated this risk of polysilicon-to-emitter 120 contact. In my opinion, this is plainly the more sensible path that a POSITA would have followed.

221. But again, such a structure would lack the claimed ***"isolation portion"*** that ***"excludes"*** the ***"oxide layer."***

222. As I have noted, while the Petition references only the use of a metal shadow mask, Dr. Banerjee does list other potential manufacturing methods in his declaration.

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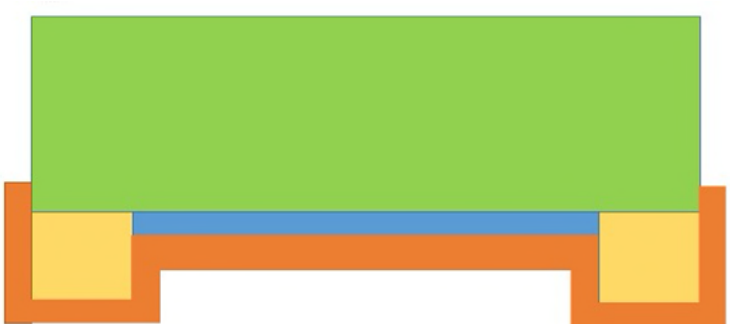
223. While the Petition does not explain how these other methods would result in the claimed subject matter, I will nonetheless address them in the paragraphs below.

224. Dr. Banerjee first suggests a POSITA could "first deposit a silicon nitride (SiNx) layer on the entire back surface of the substrate" and then use a dry etch process to etch out the center portion of the silicon nitride layer. (Ex. 1003, Banerjee Report, ¶ 121.) Dr. Banerjee then posits that both the tunnel oxide and polysilicon could be formed within the etched center portion. (*Id.*)

225. Dr. Banerjee further assumes the POSITA would thermally grow the tunneling layer and deposit the polysilicon back surface field. But, as Dr. Banerjee recognizes, this will result in the polysilicon covering the SiNx. (*See id.*, ¶ 121.) So, it is unclear how Dr. Banerjee expects a POSITA to first "use a chemical wet etch to etch out the silicon nitride mask" (under the polysilicon back surface field area) and "then mechanically remove the portion of the polysilicon back surface field area that was deposited over the silicon nitride mask" as Dr. Banerjee describes. Etching cannot be performed without removing the polysilicon. And the polysilicon cannot be selectively removed from over a silicon nitride mask (which can be as small as 1 nm wide) without a separate masking and patterning step. A POSITA would not even have attempted this process, let alone had a reasonable expectation that it would succeed.

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226. By way of further clarification, after depositing the regional tunneling layer (blue below) with a silicon nitride mask (yellow below, with significantly exaggerated size), when the doped silicon is deposited using the method advocated by the respondent, the doped polysilicon (orange below) will have a conformal structure around the silicon nitride as shown below:



227. If Dr. Banerjee's proposed etching method is to be used to remove the edge of the silicon nitride, then it will be necessary to first selectively remove the doped polysilicon at the edge and side first to expose the silicon nitride mask. But in so doing, it is not guaranteed that the doped polysilicon in the back field area will not be destroyed and only the doped polysilicon in the edge area will be removed. Again, a separate masking and etching process would have to be performed to achieve the necessary structure.

228. Dr. Banerjee third suggestion combines a SiNx mask to form tunneling layer **44**, a separate SiNx mask removal process, and then use of yet another metal shadow mask to form back surface field area 30. (Ex. 1003, ¶ 122.)

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229. This process is inordinately complicated requiring many discrete steps, including multiple separate masking steps, which will add significant time and expense to the manufacturing process. A POSITA would have absolutely no reason to incur such expense given the fact that an isolation portion is unneeded (and in particular an isolation portion that excludes the tunnel oxide).

230. Moreover, this third suggestion combines the problems of Dr. Banerjee's prior manufacturing suggestions. The process of removing the silicon nitride mask risks damage to the tunnel oxide. And because the polysilicon is deposited through a metal shadow mask over the already in place tunnel oxide, it is likely to overspray and contact the silicon substrate, thus increasing the risks of the very problems Dr. Banerjee is attempting to avoid by including the isolation portion. Once again, this problem could be avoided simply by including the tunnel oxide in the isolation portion. A POSITA would not have attempted this process or have had a reasonable expectation that it would succeed.

231. Further, a POSITA would understand that when the etching method described by Dr. Banerjee is used to remove the edge silicon nitride, the side of the tunneling layer will be irregular and different every time the process is attempted (due to the "overspray" and possible misalignment problems outlined above).

232. Thus, it would be virtually impossible to perfectly match a metal shadow mask to the tunnel oxide, resulting in areas both (1) where the polysilicon

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does not cover the tunnel oxide and (2) where the polysilicon extends beyond the tunnel oxide. This would in turn both reduce solar cell efficiency and give rise to the other problems I have outlined above (i.e., unwanted diffusion of impurities into the substrate, possible contact between the polysilicon and the frontside emitter). As before, this could be entirely avoided by allowing the tunnel oxide to cover the entire rear surface of the substrate.

233. In Dr. Banerjee's "fourth example," he proposes removing the nitride mask immediately after depositing the tunnel oxide, depositing the polysilicon over both the tunnel oxide and the remainder of the backside of the substrate, using a "reverse of the mask shown in Fig. 9 of Jin … to protect the polysilicon over the tunnel oxide," and then removing the remaining polysilicon "using a wet etch or a plasma etch." (Ex. 1003, ¶ 123.)

234. Once again, Dr. Banerjee fails to explain why a POSITA would have unnecessarily increased the time and expense needed for manufacturing by employing this many discrete steps without any associated benefit. Moreover, as with Dr. Banerjee's other proposals, when etching away the silicon nitride mask, the edges of the tunnel oxide would become irregular contributing to solar cell inefficiencies.

235. Dr. Banerjee's "fifth example" deposits tunnel oxide and polysilicon over the entire backside of the substrate without a mask. (Ex. 1003, ¶ 124.) As I

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note above, this is consistent with how these layers were applied in the prior art. But Dr. Banerjee then goes on to explain that "a reverse mask shown in Fig. 9 of Jin" would be applied, and then the "polysilicon and tunnel oxide in the edge portion… would then be removed using an etch such as a wet etch." (*Id.*). The issue with this proposal is the types of etches employed in the art to effectuate this removal were selective, and designed to remove only the polysilicon and not the tunnel oxide. So, this method would not result in the type of structure the claims require: there would still be tunnel oxide in the "isolation portion."

236. Thus, it is my opinion that a POSITA would not have been motivated to attempt to combine Jin and Feldmann, would not have had a reasonable expectation of success had they been motivated, and any resulting combination would not have had the structure that Dr. Banerjee assumes and alleges renders the claims obvious.

3. The Petition Improperly Eliminates the Efficiency Benefits of Both Jin's and Feldmann's Solar Cells

237. There are still further reasons why a POSITA would not have been motivated to combine Jin and Feldmann in the manner discussed in the Petition and Dr. Banerjee.

238. In particular, the combination eliminates—without providing any commensurate benefit—nearly all the solar cell efficiency benefits these two references identify.

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239. According to Jin, "it is very important to improve the efficiency" of a solar cell." (Jin, [0006].)

240. One of the ways that Jin accomplishes this is "by reduc[ing] surface resistance" between its electrode "finger lines" and the underlying emitter and back surface field layers. (*Id.*, [0032].)

241. To do so, Jin both increases "doping density" and the "doping thickness" of its layers **120** and **150** in the area of the finger electrodes. (*Id.*, [0032], [0042].) So, by forming shallow areas **152** and thicker, more highly doped areas **154** on its back surface, Jin explains that "recombination of electrons and holes may be effectively prevented or reduced." (*Id.*, [0043].)

242. Feldmann similarly explains that its solar cell is designed to employ "highly efficient passivated contacts." (Feldmann at 270.)

243. One of the efficiency gains Feldmann proposes results from the use of "an appropriate rear metallization." (*Id.*) According to Feldmann, in its solar cell "the requirement for the rear contact in terms of internal reflection is quite high." (*Id.* at 273.) Thus, Feldmann employs an "ITO/Ag stack and AG single layer respectively" to "significantly increase" the "rear side reflection[.]" (*Id.*) This metallization layer covers the entire rear surface of Feldmann's solar cell. (*See id.* at 272.)

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244. Feldmann also specifically criticizes solar cells employing point contacts: "[c]ontrary to point contact rear side passivation schemes… [Feldmann's] one-dimensional design facilitates processing (no structuring and alignment) and enables high FFs above 82% while maintaining a high V_{oc}." (*Id.* at 274.)

245. The Petition's and Dr. Banerjee's proposed combination of Jin and Feldmann eliminates all of these efficiency benefits.

246. The Petition and Dr. Banerjee's proposed combination includes a P-doped Si layer with a uniform thickness on the rear-side of the substrate. Thus, the efficiency benefit identified in Jin is no longer present: the combined structure does not reduce surface resistance between the finger electrodes and the back-side layer and does not prevent recombination of electrons and holes in the same way discussed in Jin. Nor can this feature be included. The interposed tunnel oxide prevents it.

247. The efficiency benefits identified in Feldmann have also been lost: because it employs finger electrodes on its backside surface, the combined structure no longer significantly increases rear side reflection. Moreover, the proposed combination uses the very type of rear side contact Feldmann criticizes: a point contact. This will make the solar cell less suitable for use on a non-reflective surface (like an asphalt shingle, rolled tar paper, or membrane covered roof).

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248. Neither the Petition nor Dr. Banerjee even attempt to explain why a POSITA would modify Jin in a way that eliminates its primary efficiency benefit: the use of increased doping density and thickness in the area of the electrodes.

249. The Petition and Dr. Banerjee also do not explain why a POSITA would allegedly have abandoned Feldmann's teachings regarding the importance of more extensive backside metallization.

250. In my opinion, considering Jin and Feldmann as a whole, a POSITA attempting to combine these references would have been motivated to ***include*** Feldmann's entire rear-metallization layer.

251. Jin references the use of point contacts (170) but attributes no significance to them. (*See, e.g.,* Jin, [0026], [0041]-[0043], [0052]-[0055].)

252. It also does not criticize the use of a rear-side metallization layer like that employed by Feldmann.

253. Feldmann, however, teaches that use of rear metallization is a necessary "prerequisite" for "high FFs." (Ex. 1012 at 270.)

254. Given this, a POSITA would have been particularly motivated to use Feldmann's rear metallization when applying Feldmann's teachings to Jin.

255. A POSITA would have recognized that doing so would help compensate for the elimination of Jin's back surface field layer with its efficiency boosting highly doped areas **154**.

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256. This structure lacks the claimed ***"first electrode connected to the polysilicon through an opening formed in the first passivation film."***

257. Rather than seeking to maximize the efficiency of the combined structure, the Petition and Dr. Banerjee ignore Jin's and Feldmann's clear teachings regarding importance of efficiency (and the manner in which the references achieve this) and instead choose a ***less efficient*** design option. A POSITA reviewing these references would not have done the same.

4. Jin and Feldmann Do Not Teach What Claim 8 Requires

258. Dependent claim 8 of the '009 patent requires that ***"a thickness of the edge portion in the polysilicon layer progressively decreases toward the isolation portion."***

259. According to the Petition, when "Feldmann's polysilicon layer" is formed using "a metal 'shadow' mask configured like Jin's Fig. 9," "small amounts of polysilicon" will "deposit beneath the edge of the mask … resulting in a taper of the polysilicon" in this area. Petition at 43. Dr. Banerjee says the same thing. (Ex. 1003, ¶¶ 161-165.

260. This is not what this limitation requires. Jin explains that the mask shown in Figure 9 "covers or overlaps a distance T measured from the edge part of the rear surface of the substrate 110." (Jin, [0085].)

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261. Because the mask "covers" Jin's gap (or distance) T, to the extent there is any tapering of polysilicon as alleged by the Petition, the tapered polysilicon will be present ***within*** the gap T. Tapered polysilicon within Jin's gap (or distance) T does not ***"progressively decrease toward the isolation portion."***

262. Nor does such a structure satisfy claim 1's requirement that the ***"polysilicon layer"*** be ***"exclude[d]"*** from the ***"isolation portion."***

263. This claim requires that there be ***no*** polysilicon within the ***"isolation portion"*** at all. The claim also requires that the polysilicon thickness ***"progressively decrease"*** as it gets closer to the bounds of the ***"isolation portion."***

264. In my opinion, by extending polysilicon into the ***"isolation portion,"*** Jin and Feldmann fail to teach what is required.

D. Detailed Assessment of Ground 3: Chang and Jin Fail to Teach What the Claims Require

265. In my opinion, Chang and Jin fail to teach the claimed ***"isolation portion" "in an edge portion"*** of the ***"substrate" "for preventing a contact between the polysilicon layer and the emitter region."***

266. Chang by itself does not teach what is required. And a POSITA would have had no reason to apply Jin's gap (or distance) T to Chang: this gap is meant to address issues arising when doping the backside of a solar cell substrate. Chang does not dope the backside of its substrate.

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267. The Petition and Dr. Banerjee begin by pointing to Chang alone. Dr. Banerjee notes that in Chang's figures, "the rear conductive type area" and "rear tunnel layer" are shown as covering the entirety of the rear side of the substrate. (Ex. 1003, ¶ 210.) This is exactly what the Examiner held during prosecution of the parent application. (Ex. 1006 at 254.)

268. Figures 1 and 8 of Chang (which are representative of all of Chang's figures when it comes to the extent of Chang's various layers) are reproduced below:

FIG. 1

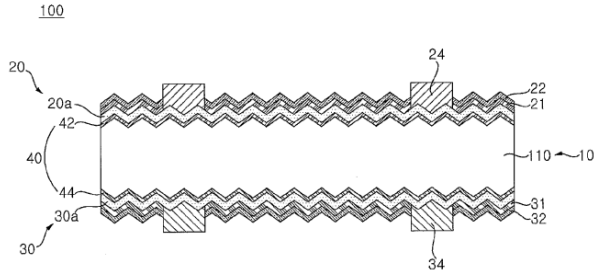
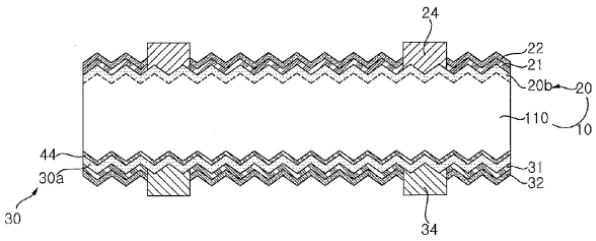


FIG. 8



(Chang, Figs. 1, 8.)

269. Both figures show similar solar cells with a conductive "emitter area **20** and a back surface field area **30**…." (Chang, [0036].) These areas are of opposite conductivity types. "One of the emitter area 20 and the back surface field area 30 is referred to as a 'first conductive type area' and the other is referred to as a 'second conductive type area'." (*Id.*, [0037].)

270. Chang teaches that, as illustrated in the figures, "the emitter area **20** and the back surface field area **30** may be disposed at different sides of the semiconductor substrate **10** to form a double-surface light-receiving type structure." (*Id.*, [0076].

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271. Because these conductive regions are "disposed at different sides" of the substrate, they cannot form a short-circuit. As a result, Chang has no need for an isolation portion, as required by claim 1 "***for preventing a contact between the polysilicon layer and the emitter region.***"

272. According to Dr. Banerjee, even though Chang's front and backside conductive layers are located on opposite sides of the substrate and cannot short circuit, Chang still "discloses an isolation region at the periphery of the substrate that excludes the tunnel oxide and polysilicon layer." (Ex. 1003, ¶ 210.)

273. That is not correct. There is no such disclosure or teaching in Chang. Chang does not describe use of an isolation portion like that required by claim 1 of the '009 patent.

274. Instead, Chang says the opposite. Chang explains that "[b]ecause the emitter area 20 and the back surface field area 30 are not adjacent to each other, the necessity of performing an isolation process when the emitter area 20 and the back surface field area 30 are formed to be adjacent to each other ***is eliminated***." (Chang, [0076]. (emphasis added).)

275. According to Chang eliminating the need to perform an isolation process is beneficial because the "manufacturing process is simplified and cost is thus reduced." (*Id.*)

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276. Moreover, Chang states that tunneling layer **44** is "entirely formed" over the back surface of substrate **10** (*id.*, [0056]), while its back surface field area **30** is "entirely formed" over the second tunneling layer **44** (*id.*, [0062]).

277. Dr. Banerjee points out a statement in Chang to the effect that "[a]s used herein, the expression 'entirely formed' means that an element such as a layer is formed over an entire surface without an empty area or a non-coverage area, or is formed in an entire area excluding pre-designated or inevitably formed regions such as periphery region, isolation region or the like." (*Id.*, [0056], [0062].)

278. Dr. Banerjee uses this statement to argue that this reference to a "periphery region" or an "isolation region" means that Chang teaches the specific isolation portion required by claim 1 of the '009 patent. (*See, e.g.*, Ex. 1003, ¶¶ 210-211.)

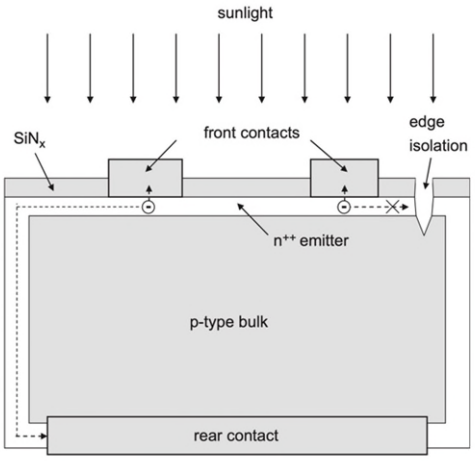
279. In my opinion, this fails to account for what Chang's actually discloses. Again, Chang specifically describes that one benefit of its structure is that ***no*** such isolation portion is required. (Chang, [0076].) Including such a region would be contrary to Chang and result in a solar cell that is more complicated to manufacture (which Chang is attempting to avoid).

280. Moreover, Chang notes that layers are present everywhere except in "pre-designated or inevitably formed regions." There are no such "pre-designated" or "inevitably formed" regions in Figures 1 or 8 (or in any of Chang's other

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embodiments. Moreover, as I have explained not only does Chang not "pre-designate" or "inevitably form" an isolation portion, but it explicitly notes that such a structure is not needed in is solar cell.

281. Next, in the event a portion of Chang's layer is omitted, Chang specifies that this be in an "isolation region" or "periphery region." There is no requirement, however, that layers be excluded from the ***"edge portion"*** of a semiconductor substrate as the '009 patent's claims require. While both an "isolation region" and "periphery region" may be near a substrate edge, they are not required to be at the edge. This is exemplified by the very art on which Dr. Banerjee relies. One such reference provides an example (reproduced below) of "edge isolation" formed ***within the boundaries*** of the substrate surface:



(Ex. 1026 at 1639.)

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282. There is nothing in Chang that precludes this type of structure. The isolation structure shown above is in the peripheral "region" of the substrate even though it is not located at the substrate edge

283. This is not what the claims require. To satisfy the '009 patent's claims, the ***"isolation portion"*** must be ***"in an edge portion"*** of the ***"substrate."*** It is not enough to simply be in the region of or near the edge. This is all Chang says.

284. Next, even if Dr. Banerjee is correct regarding Chang's backside layers. Chang also states that the layers formed on its front surface can be similarly "exclude[ed]" from "pre-designated or inevitably formed regions such as periphery region, isolation region or the like." (*Id.*, [0045], [0051].)

285. So, if Chang's reference to "inevitably formed regions" means that no layers are located in a region around the edge of the substrate, ***none*** of Chang's layers will be located in the substrate's edge regions. This includes the layers on ***both*** the front and the backside of Chang's substrate.

286. It follows that Chang lacks the claimed ***"isolation portion" "for preventing a contact between the polysilicon layer and the emitter region."*** Because both the front and backside layers are not present in the edge regions of the substrate (at least under Dr. Banerjee's interpretation of Chang), there can be no contact between the layers. Any "isolation portion" does not "prevent[] a contact"

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because the frontside layers have the same extent (and are excluded from the same portions of the substrate frontside) as the backside layers.

287. Next, I also disagree with Dr.Banerjee's opinion that a POSITA would have applied Jin's gap (or distance) T to Chang.

288. Like Jin and Feldmann, Chang and Jin are very different references. Chang relates to a TOPCon solar cell, while Jin relates to a PERC solar cell. Chang has no need for (ad explicitly excludes) an isolation portion. Jin employs a gap (or distance) T to account for the particular manufacturing method and device structure it employs. Dr. Banerjee fails to account for these differences.

289. More specifically, as explained when addressing Ground 1 above, Jin employs this gap because it forms both its emitter layer 120 and back surface field layer 150 by doping the front and backside of the same substrate. The gap (or distance) T prevents the layers from contacting each other through the substrate, and also addresses impurities diffusing through the portion of the substrate located between the layers.

290. Unlike Jin, Chang does not employ a back surface field layer 150 that is formed by doping the substrate itself.

291. Instead, Dr. Banerjee points to tunnel oxide and polysilicon layers that are deposited ***on top*** of the substrate's back surface.

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292. Putting aside this structural difference (which itself shows that Jin's distance or gap T is not required), Chang also explains that (i) its emitter and BSF regions are "not adjacent to each other" and are instead on opposite sides of a substrate (and, thus, cannot short), (ii) the need for "performing an isolation process is eliminated," and (iii) not performing an (unnecessary) isolation process results in a "simplified" manufacturing process and "reduced" cost. (Chang, [0076].)

293. Given all this, a POSITA would not have been motivated to modify Chang and add an unnecessary, complicated, and expensive isolation step. Instead, just as Chang itself discloses and depicts in its figures, Chang's backside layers would be extended over the entire rear surface of its substrate.

294. Put another way, Chang does not have the problems the gap (or distance) T is meant to address.

295. Moreover, even if a POSITA were to try to exclude Chang'e polysilicon layer from the gap (or distance) T, there is absolutely no reason to also exclude the tunnel oxide from this area.

296. In my opinion, doing so would be entirely unnecessary (as the tunnel oxide is insulating and acts as a diffusion barrier), non-sensical (as the space occupied this layer would later be filled with an oxide in any event), and give rise to the very same manufacturing difficulties and device performance issues discussed

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in connection with Ground 1. Thus, a POSITA would neither be motivated to make this change, or expect to succeed when doing so.

297. Instead, at best, a POSITA would have extended Chang's tunnel oxide over the entire rear surface of the substrate, while reducing the physical extent of only the polysilicon layer.

298. Not only would this improve device performance and avoid the manufacturing issues discussed in Ground 1, but it would further Chang's own goals. According to Chang, the tunnel layer "passivates the surface of the semiconductor substrate 10 having many recombination sites and facilitates transfer of carriers through a tunneling effect." (Chang, [0057]; *see also id.*, [0010] ("damage to the semiconductor substrate is prevented and recombination sites on the back surface of the semiconductor substrate are thus efficiently removed."). So, a POSITA would understand that Chang's tunnel layer provides numerous beneficial effects, including passivating defects in the silicon surface. This further shows that to the extent a POSITA were motivated to attempt to add an isolation portion to Chang (despite the instruction that this is unnecessary), the tunnel layer would remain in place so as to continue to provide these expressed benefits.

299. So, in my opinion, the combination of Chang and Jin fails to render obvious (i) "***an isolation portion for preventing a contact between the polysilicon layer and the emitter region***" and (ii) "***wherein the isolation portion excludes the***

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oxide layer and the polysilicon layer, and is in an edge portion of the first surface of the silicon semiconductor substrate."

300. This combination of prior art also fails to teach claim 8's ***"thickness of the edge portion in the polysilicon layer"*** that ***"progressively decreases toward the isolation portion."*** The Petition and Dr. Banerjee once again points to "small amounts of polysilicon" extending into Jin's gap (or distance) T. *See* Petition at 71-72. This is not what this limitation requires for the same reasons I explained when discussing claim 8 in Ground 1.

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I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willfully false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1101 of Title 18 of the United States Code.

Date: 28 July 2025

Location: Washington, D.C.

Signature: Martin Peckerar

Dr. Martin Peckerar

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ATTACHMENT A

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Martin Peckerar, Ph.D: Curriculum Vita

12917 Buccaneer Road
Silver Spring, MD 20904
301-257-2767

Overview: Dr. Peckerar is a specialist in the areas of materials science and technology. He has applied these skills to the development of microelectronic circuits. He began his career working in electronic circuit reliability assurance and failure analysis. At NASA's Goddard Space Flight Center, he developed e-beam characterization techniques for identifying failure mechanisms occurring in Schottky solar cells. He developed the first successful theory explaining the role of insulating films in open-circuit voltage enhancement of Schottky solar cells.

He then joined the Westinghouse Electric Company's Advanced Technology Laboratory. Here, he was lead process engineer on the Block Organized Random Access Memory chip. This was the first "radiation hard" memory system to be deployed in a nuclear battle environment. He developed a surface implant technology that eliminated the so-called "backside dead layer" impeding efficient UV sensing in rear-surface illuminated UV imagers. He is the inventor of the deep-depletion CCD imager used in x-ray and in short wavelength IR imaging. He developed the first CCD imager and read-out electronics demonstrated to be radiation hard out to 1 MRAD:Si while operating at 77K. This has been enabling technology in satellite imaging. He developed the first CCD imager and read-out electronics demonstrated to be radiation hard out to 1 MRAD:Si while operating at 77K. This has been enabling technology in satellite imaging.

Professor Peckerar's work at the University of Maryland has, most recently, involved development of resistive random-access memories (ReRAMs) with enhanced endurance and long-term stability. He has also co-founded two small businesses: FlexEl Battery, LLC and VersaVolt, LLC. FlexEl produced flexible power devices for empowering wearable electronic systems; VersaVolt is a consulting company working in the area of ultralow power electronic system design and development.

Education:

1971-1975 Ph.D., University of

Maryland 1968-1971 M.S,

University of Maryland 1964-

1968 B.S., SUNY Stony Book

Professional Experience:

1. 2012-present Dr. Peckerar has co-founded two small businesses. The first, FlexEl LLC is a manufacturer of flexible electronic components and batteries. This company has partnered in the creation of non-flammable (lithium-free) power supplies for e-cigarettes and with medical electronics corporations for manufacturing ultrathin, flexible power sources. In addition, Dr. Peckerar was a co-founder of VersaVolt LLC, a company specializing in the creation of reserve batteries for underwater applications (such as extending the life of flight data recorders.)

2. 1981-present Professor, University of Maryland (College Park Campus). Dr. Peckerar is

Professor of microelectronic process technology and analog systems design. He is author of the textbook Electronic Materials: Science and Technology (S.P. Murarka, co-author), the Korean Electronics Economy (with Mike Pecht) and Synthetic Microstructures for Biological Research (with Joel Schnur.) In 1980, Professor Peckerar was appointed lecturer in the ECE department. From 1981-2002, he was professor part-time, holding joint appointments at the university and at the Naval Research Laboratory. He became tenured professor (full time) in 2002, and he is currently professor, emeritus.

3. 1981-2002 Branch Chief, Naval Research Laboratory, Washington, DC. Dr. Peckerar headed the Interface and Thin Films Branch. His responsibilities included management of the Nanoelectronics Processing Facility as well as the Laboratory for Advanced Materials Synthesis. Here, he developed sensor materials for visible, IR, UV and x-ray imaging. He also was Navy Manager of the DARPA Advanced Lithography Program. He pioneered in the development of e-beam proximity effect correction – an enabling technology for today's microelectronic patterning technology.

4. 1976-1981 Fellow Engineer, Westinghouse Corporation, Baltimore, MD. Dr. Peckerar headed the Advanced MOS Technology Group. He designed and developed non-volatile memory systems and radiation-hardened components. At Westinghouse he invented the plasma source for EUV and x-ray lithography.

5. 1973-1976 Physicist, Naval Research Laboratory, Washington, DC. Dr. Peckerar worked in the area of x-ray spectroscopy (largely aimed at detecting environmental pollutants.)

6. 1968-1973 Physicist, NASA Goddard, Greenbelt, MD. Dr. Peckerar performed component reliability studies for the first manned lunar program

Expert Witness work and Paid Consultancies:

1. Expert Witness, DRAM technology, Milbank, Tweed Hadley McCloy, 2007-2010 (patent infringement on the physical implementation of the DDR3 specification.) Working with Jim Klaiber, now at Pryor Cashman. ITC Trial designation: Certain Dynamic Random Access Memory Devices and Products Containing Same.) Investigation Number: 337-TA-595. **Deposed twice. Testified before the ITC for three days.**

2. Expert Witness, battery technology, Finnegan 2011 (relating to battery applications in power tool technology.) Working on **IPR** with Tom Irving, representing Hitachi. IPR

3. Expert Witness, Non-Volatile Memory Technology, Winston Strawn 2014. Working with Vivian Kuo, J.C. Mascullo, David Enzminger and Dave Martens. ITC Trial designation: In the Matter of Certain Non-Volatile Memory Devices and Products Containing Same. This work included simulations of the chemical-mechanical polishing process for wafer planarization in integrated circuit fabrication technology. Investigation Number: 337-TA-909. **Deposed twice. Testified before the ITC for two days.**

4. Expert Witness, Matters relating to the layout and design of static random access memories, nvidia vs Samsung, working for Latham Watkins. IPR2015-01065. POCs Thomas Yeh and Bob Rosenberg, begun May 2015 and concluded in May, 2016**. IPR. Deposed once.**

5. Expert Witness, worked on an IPR in the matter of Postec and the validity of Milwaukee

Tools patent on a lithium battery powered power tool. I worked for Middleton and Reutlinger (Robert H. Eichenberger, lead attorney.) Concluded June, 2017.

6. Expert Witness, in support of Nikon Corporation, Nikon Precision Inc., and Nikon Research Corporation of America, Inv. No. 337-TA-1137, defending against claims by ASML Netherlands. Concluded February 2019. Lead attorney: Sorin Zaharia.

7. Expert witness in support of VARTA Battery defending against claims by a variety of earbud distributers, concluding in January 2023. Deposed three times. I worked in support of Leydig, Voit and Meyer. Lead attorney: Wesley Mueller.

8. Technical Consultant: National Institute of Aerospace, consulting in power distribution systems.

Personal Awards:

1. Fellow, IEEE 1994: For Contributions to and Leadership in X-ray and Microlithography.

2. Outstanding Invention of the year (2008) in physical sciences, presented by the Maryland Office of Technology Commercialization: for a thin, conformable high energy storage density battery.

3. First place in the University of Maryland's $75K Business Plan Competition for thin, flexible batteries (2009).

4. Maryland Technology Enterprise Institute (MTECH/SAIC) $25K grants for battery development 2009

5. Maryland State Incubator Company (FlexEl Batteries, LLC) of the Year Award, May 2010

6. Inaugural University System of Maryland's Inaugural Entrepreneurship Award in 2013 for work developing FlexEl, LLC.

Books authored.

1. S.Murarka, M. Peckerar, Electronic Materials Science and Technology, Academic Press, 1989.

2. M. Pecht, J. Bernstein, Daemon Searles and M.Peckerar, The South Korean Electronics Industry, CRC Press, 1997.

Books edited.

1. M. Peckerar, M., J. Schnur and H. Stratton, Synthetic Microstructures in Biological Research, Plenum Press, New York, 1993. Re-issued in 2004.

2. M. Peckerar, "Electron-Beam X-Ray and Ion Beam Submicrometer Lithographies for Manufacturing II", Vol 1671 SPIE, San Jose, CA, 1992.

3. M. Peckerar, "Electron-Beam, X-Ray, and Ion Beam Lithographies For Manufacturing," SPIE Proc. Vol. 1465 SPIE, San Jose, CA, 1991.

4. M. Peckerar and M. Postek, "Nanostructure Science, Metrology and Technology," (With Mike Postek) SPIE Press, March 2002.

Chapters in books.

1. M.Peckerar, R. Neidert, "High-Speed Microelectronics for Military Applications in the IEEE Press Anthology VLSI Engineering, V. Wohlfarth, W. Grobman, eds. (1985)

2. C. Marrian, M. Peckerar and Y. Pati "Electronic Neural Nets For Solving Ill- Posed Problems With An Entropy Regulariser," (with C. Marrian and Y. Pati), in Maximum Entropy And Bayesian Methods, J. Skilling (ed.), D. Reidel, Dordrecht, pp. 371-376 (1989).

3. M. Peckerar, P.T. Ho, R. Chen, "High Resolution Lithography For Optoelectronics," in McGraw Hill Handbook On Optoelectronics, R. Waynant, Ed.(1992). Martin Peckerar and Milton Rebbert, "Advanced Materials Processes for Bio- Probes," in Synthetic Microstructures in Biological Research, Plenum Press, Edited M. Peckerar, J. M. Schnur H. Stratton, Pages 3-16, 1992.

4. M. Peckerar, F. Perkins, E. Dobisz, and O. Glembocki "Issues in Nanolithography for Quantum Effect Device Manufacture," (with in, The Handbook of Microlithography, Micromachining and Microfabrication P. Rai-Choudhury, ed., SPIE Press (1997).

5. E. Dobisz, F. Perkins, M. Peckerar "E-Beam and Proximal Probe Processes for Nanolithography," in Microlithography: Science and Technology, J.R. Sheats and B.W. Smith, eds. Marcel Dekker, New York, 1998. Re-issued in 2007.

6. M. Peckerar, "Nanolithography With Electron Beams: Theory and Practice," in: Direct-Write Technologies for Rapid Prototyping Applications, A. Pique andD. Chrissey (eds.), Academic Press, San Diego, CA(2001)

7. F.Yesilkoy, C.Ropp, Z.Cummins, R.Probst, E.Waks, **B.Shapiro**, M.Peckerar*, "New Applications and Emerging Technologies", editor M.Feldman, chapter in "Nanolithograpy: The Art of Fabricating Nanoelectronic, Nanophotonic, and Nanobiologic Devices and Systems", Woodhead Publishing LTD, Cambridge, 2012.

8. **Yesilkoy F**, Potbhare S, Kratzmeier N, Akturk A, Goldsman N, Peckerar M, Dagenais M. A Mid- IR antenna integrated with a geometrically asymmetrical metal-insulator-metal rectifying diode *Rectenna Solar Cells*. 2147483647: 163-188, 2013 DOI: 10.1007/978-1-4614-3716-1_8

Articles in Refereed Journals.

1. M. Peckerar "Electron Beam Studies of Schottky Barrier Detector Surfaces", IEEE Trans. Nuc. Sci NS-20, 383 (1973).
2. M. Peckerar "On the Origin of the Increase in Schottky Barrier Height with Increasing Interfacial Oxide Thickness", J. Appl. Phys. 45, 4652 (1974).
3. D. B. Brown, J. V. Gilfrich, M. Peckerar, "Measurement and Calculation of Absolute Intensities of X-ray Spectra", J. Appl., Phys., 46, 4537 (1975).
4. M. Peckerar, S. Mak, L. Skolnick, "The Role of Electron Trapping in the Plasma Anodization of Aluminum", Journal of the Electrochemical Society, 123, 190C (1976).

5. M.H. White, J. Dzimianski and M. Peckerar, "Endurance of Thin-Oxide Non-Volatile MNOS Memory Transistors", IEEE Trans. Electron Devices, ED-24 577 (1977) .
6. M. Peckerar, D. Nagel, "X-Ray Imaging with Charge-Coupled Devices", J. of Appl. Physics, 48, 2565 (1977).
7. R. McLouski, M. Peckerar and J. Schruers, "The Effect of HCl Residual Treatment on MNOS Memory Transistors", J. Electrochemical Soc., 125, 985 (1978).
8. D. Nagel and M. Peckerar, "Lithography and High Resolution Radiography with Pulsed X-rays" Jap. Jour. Appl. Phys., 472 (1978).
9. M. Peckerar, P. Blaise and R. Fulton, "Radiation Effects in MOS Devices Caused by X- ray and E- beam Lithography", JVST 16, 1658 (1979).
10. D. Nagel and M. Peckerar, "Pulsed X-ray Lithography" Electron Letters, 14 781 (1979).
11. M. Peckerar and N. Bluzer, "Hydrogen Annealed Nitride/Oxide Structures for Radiation Hardness", IEEE Trans. Nuc. Sci., NS-27 1193 (1980).
12. H. Stein, P. Peercy and M. Peckerar, "Properties of Magnetron Sputtered Amorphous Hydrogenated Silicon" Journal of Mat'l Sci., 10 797 (1981).
13. M. Peckerar, D. Nagel and D. Baker, "X-Ray Imaging with CCDs", Appl. Phys. Lttrs. 3955 (1981).
14. R. Williams, J. Rife, D. Nagel, and M. Peckerar, "Instrumentation for X-UV Lithography at SURF II," Nuc. Instr. and Methods, 195 267 (1982).
15. M. Peckerar, C. Dozier, D. Brown, D. Patterson, D. McCarthy and D. Ma, "Radiation Effects Introduced By X-Ray Lithography in MOS Devices", IEEE Trans. Nuc. Sci. 29(6), pp. 1697- 1701(1982).
16. D. Brown, D. Ma, C. Dozier and M. Peckerar, "Thermal Annealing of Radiation Induced Defects – A Diffusion Limited Process," IEEE Trans. Nuc. Sci. 30(6), 4059(1983).
17. M. Peckerar and D. Ma "Modeling Total Dose Effects in Narrow Channel Devices," IEEE Trans. ED., ED-30, p. 1159, (1983).
18. M. Peckerar and R. Neidert, "High Speed Microelectronics for Military Applications", Proc. IEEE 71, p. 657, (1983).
19. R.R. Whitlock, M.H. Emery, J.A. Stamper, E.A. McLean, S.P. Obenschain and M. Peckerar, "Observation of Rayleigh-Taylor-Like Structures in a Laser-Accelerated Foil", Phys. Rev. Ltrs., 52, 819 (1984).
20. D.J. Nagel, M. Peckerar, C.M. Brown, M.L. Ginter, T.A. Robinson, T.J. McIlrath, and
21. D.N. Carroll "Repetitively Pulsed-plasma Soft X-ray Source," Appl. Optics 23, 1428 (1984).
22. P. Gohil, H. Kapoor, D. Ma, M. Peckerar, T.J. McIlrath, M.L. Ginter "Soft X-ray Lithography Using Radiation from Laser-Produced Plasmas", Appl. Optics 24, p. 2024 (1985).
23. Christou and M. Peckerar, "Planar MOCVD GaA1As/GaAs High-Frequency Mixer Diodes," Elect. Ltrs. 21(7) pp. 505-507 (1985).
24. P. Gohil, H. Kapoor, D. Ma, T. McIlrath, M. Ginter and M. Peckerar, "Soft X-Ray Lithography Using Radiation From Laser Produced Plasmas", Appl Opt. 24, p. 2024 (1985).
25. M. Pepin, P. Alaterre, M. Chaker, R. Fabbro, B. Faral, I. Toubhans, D. Nagel and M. Peckerar, "X-ray Sources for Microlithography Created by Laser Radiation at l = 0.26 mm," JVST B 5(1), 27 (1987).
26. J. Bosier, M. Peckerar, D. McCarthy, N. Saks, D. Michels "Modeling UV Response of Rear Surface Sensitized Charge-Coupled Devices," Appl. Phys. Letters, 50(18), 1295 (1987).
27. D. Ma, S. Qadri, and M. Peckerar "Double Crystal X-Ray Topographic Determination of Local Strain In Metal-Oxide-Semiconductor Devices," Appl. Phys. Letters 51(22) 1827 (1987).
28. P. Dutta, G. Candela, D. Chandler-Horowitz and M. Peckerar, " Non-Destructive Characterization of Oxygen-Implanted Silicon-on-Insulator Films Using Multiple Angle Ellipsometry," Jour. Appl. Phys. 64(5) 2754(1988).
29. C. T. Yao, M. Peckerar, D. Friedman, H. Hughes, "On the Effect of Hot Carrier Stressing on MOSFET Terminal Capacitances," IEEE Trans. ED, 35(b), 304 (1988).

30. D. Ma, S. Qadri and M. Peckerar, “Characterization of Thin Boron-Doped Membranes by Double Crystal X-Ray Topography, JVST-B 7(6) 1594(1989).
31. Culhane, M.Peckerar, and C. Marrian, “A Neural Net Approach to Discrete Hartley and Fourier Transforms,” IEEE Trans. Circ. Syst. 36(5) 695 (1989).
32. C.R.K. Marrian and M. Peckerar, “Electronic “Neural” Net Algorithm for Maximum Entropy Solution of Ill-Posed Problems,” IEEE Trans. Circ. Syst. 36(2) 288(1989).
33. C.R.K. Marrian and M. Peckerar, “Electronic “Neural” Net Algorithm for Maximum Entropy Solution of Ill-Posed Problems - Part II: Multiply Connected Electronic Circuit Implementation,” IEEE Trans. Circ. Syst. 37(1) 110(1990).
34. M. Peckerar, J. Goldhar, P.T. Ho, and K. Rhee, “A Novel Test Structure for Grating Pitch Determination With Near Ångstrom Accuracy”, Jour. Appl. Phys. 68(10), 5381(1990).
35. Y. Pati, A. Teolis, D. Park, R. Bass, K. Rhee, B. Bradie, and M. Peckerar, “An Error Measure for Dose Correction in E-Beam Nanolithography,” JVST B 8(6), p. 1882, 1990
36. Barouch, E..,Hollerbach, U.; Orszag, S.A., Bradie, B., Peckerar, M., “Modeling process latitude in UV projection lithography,” Electron Device Letters, 12(10)513 - 514 (1991)
37. S.AS. Shamma, M. Rebbert, J. Kossokowski, P. Isaacson, M.Peckerar, “Passive Microelectrode Arrays For Recording Of Neural Signals: A Simplified Process,” Rev. Sci Instrum., 62(9), 2276(1991).
38. J. Calvert, M-S. Chen, C. Dulcey, J. Georger, J. Schnur, P. Schoen and M. Peckerar, "Deep Ultraviolet Imaging Of Monolayer Films For High Resolution Lithography," JVST-B 9(6), 3447(1991).
39. K. Rhee, M. Peckerar, A. Ting, L. Shirey, K. Foster, J. Andrews, Y.-C. Ku, "Patterning Tungsten Films with An Electron Beam Lithography System At 50 KeV For X-Ray Mask Applications," JVST B 9(6), 3282(1991).
40. C. Marrian, L. Dobisz and M. Peckerar, “Nanostructure Patterning,” Proc. IEEE 79(8), 1149(1991).
41. J. Calvert, C.S. Dulcey, J. Schnur, J. Georger, M. Peckerar, G. Calabrese, P. Sricharoenchaikit, “New Surface Imaging Techniques For Sub-0.5 Micrometer Optical Lithography,” J. Sol. St. Technol. 34(10), 77(1991).
42. D. Ma, G.J. Campisi, and S.B. Qadri and M. Peckerar, "Characterization Of Silicon On Insulator Substrates Using Reflection Mode Double Crystal X-ray Topography," Thin Solid Films, vol. 206, 27(1991).
43. D. Ma, S.B. Qadri, M. Peckerar and D. McCarthy "Double Crystal X-Ray Topography Characterization Of An Electrical Bias Induced Stress Variation In Metal-Oxide-Semiconductor Field Effect Transistors," Thin Solid Films 206, p. 18 (1991).
44. M. Jacunski and Martin C. Peckerar, "A Model for Radiation Induced Edge Leakage in Bulk Silicon nMOS Transistors", IEEE Transactions on Nuclear Science, 39(6), December 1992.
45. R. A. Ghanbari, M. Burkhardt, D. A. Antoniadis, H. I. Smith, M. R. Melloch, K. W Rhee, M. C. Peckerar "Comparative Mobility Degradation in Modulation-Doped GaAs Devices After E-Beam and X-Ray Lithography," JVST B10(6), pp. 2890-2892, (1992).
46. Kee Woo Rhee, David Ma, M. C. Peckerar, "Proximity Effect Reduction in X-Ray Mask Making Using Thin Insulating Layers," JVST B10(6), Page 3062-3066, Nov/Dec 1992.
47. R. A. Ghanbari, W.Chu, M. Burkhardt, M. L.Schattenburg, K. W. Rhee, R. Bass, M. Peckerar and M. R. Melloch, "Fabrication of Parallel Quasi-One-Dimensional Wires Using a Novel Conformable X-Ray Mask Technology", JVST B10(6), pp. 3196-3199 (1992).
48. W. Chu, C. Eugster, A Moel, E. E. Moon, J. A. del Alamo, M. L. Schattenburg, K. W. Rhee, M. R. Melloch. "Conductance Quantization in a GaAs Electron Waveguide Device Fabricated by X-Ray Lithography", JVST B 10(6), Page 2966-2969, (1992).
49. Eric A. Sprangle, John M. Andrews and M. Peckerar, "Dielectric Breakdown Strength of SiO2 Using a Stepped-Field Method,” J. Electrochem. Soc. 139(9), p.2617(1992)
50. M.Peckerar, Milton Rebbert and Ganesh Gopalakrishnan, "Apparent Super Resolution in High- Contrast Photoresists,” Appl. Phys. Lett 61 (17), p. 2037(1992).
51. Calvert, J.M., Georger, J.H., Schnur, J.M., Schoen, P.E., Peckerar, M.C., Pehrsson,P.E.,”

Deep UV photochemistry and patterning of self-assembled monolayer films," Thin Solid Films 210- 211(pt1), pp. 359-363(1992).
52. Y.C. Pati, Krishnaparasad and M.Peckerar, "An Analog Neural Network Solution To The Inverse Problem Of Early Taction", IEEE Trans. Robotics And Automation. 8(2), p.196(1992).
53. Ma, D.I. Campisi, G.J. Qadri, S.B. and Peckerar, M.C "Nondestructive evaluation of silicon-on- insulator substrates using X-ray double crystal topography," JVST A (Vacuum, Surfaces, and Films) 10(4), p.1006(1992).
54. Ma, D.I., Qadri, S.B., Peckerar, M.C. and McCarthy, D. "Characterization of the electrical bias induced strain variation in metal-oxide-semiconductor field effect transistors using X-ray double crystal topography," JVST A (Vacuum, Surfaces, and Films) 10(4) p1012(1992).
55. M.Peckerar and J.R. Maldonado "X-Ray-Lithography - An Overview," Proc. IEEE, 81(9), p1249(1993).
56. Dobisz-EA, Marrian-CRK, Salvino-RE, Ancona-MA, Rhee-KW, and M. Peckerar "Thin Silicon- Nitride Films to Increase Resolution in E-Beam Lithography," Opt. Eng. 32(10), p. 2452 (1993).
57. Calvert-JM, Koloski-TS, Dressick-WJ, Dulcey-CS, Peckerar-MC, Cerrina-F, Taylor- JW, Suh-DW, Wood-OR, Macdowell-AA and Dsouza-R, "Projection X-Ray Lithography With Ultrathin Imaging Layers and Selective Electroless Metallization," Opt. Eng. 32(10), p. 2437 (1993).
58. K.W. Rhee and M. Peckerar "Proximity Effect Reduction Using Thin Insulating Layers," Appl. Phys. Lett., 62(5) pp 533-534(1993).
59. M. Peckerar and J. R. Maldonado, "The Advanced Lithography Program - Governments Role in X- Ray-Development," Solid State Technology 37(6), pp 44,(1994).
60. Witczak, S.C., Gaitan, M., Suehle, J.S., Peckerar, M.C., Ma, D.I., "The interaction of stoichiometry, mechanical stress, and interface trap density in LPCVD Si-rich SiNx---;Si structures," Solid-State Electronics 37(10), pp. 1695-1704(1994).

61. Chu-W, Foster-KW, Shirey-LM, Rhee-KW, Kosakowski-J, Isaacson-IP, Mccarthy-D., Eddy-CR, Dobisz-EA, Marrian-CRK and M. Peckerar, "Reactive Ion Etching of High- Aspect-Ratio 100 nm Linewidth Features in Tungsten" Appl. Phys. Lett., Vol 64 Iss 16 pp 2172-2174 (1994).
62. Rebbert-M, Isaacson-P, Fischer-J, Greenhouse-MA, Grossman-J, Smith-HA and M. Peckerar, "Microstructure Technology for Fabrication of Metal-Mesh Grids," Appl. Opt., 13(7), pp 1286- 1292 (1994).
63. Burkhardt-M, Smith-HI, Antoniadis-DA, Orlando-TP, Melloch-MR, Rhee-KW) andM. Peckerar, "Fabrication Using X-Ray Nanolithography and Measurement of Coulomb-Blockade in a Variable- Sized Quantum-Dot," JVST B 12(6) pp 3611-3613 (1994.)
64. Eddy-CR, Kosakowski-J, Shirey-LM, Dobisz-EA, Rhee-KW, Chu-W, Foster-KW, Marrian-CRK and M. Peckerar, "Effects of Etch Chemistry on SF6-Based Tungsten Etching by Electron-Cyclotron- Resonance Reactive Ion Etching" JVST B 12(6) pp 3351-3355 (1994).
65. Owens-AL, Denison-TJ, Versnel-H, Rebbert-M, Shamma-SA and M. Peckerar, "Multielectrode Array for Measuring Evoked-Potentials from Surface of Ferret Primary Auditory-Cortex," Jour. Neurosci. Method., 58(1-2) , pp 209-220 (1995).
66. Grossman, K., Peckerar, M.C., "Active Current Limitation for Cold-Cathode Field Emitters," Nanotechnology 5(4), p. 179-182(1994).
67. M. Peckerar, S. Chang and C.R.K. Marrian, "Proximity Correction Algorithms and a Co-Processor Based on Regularized Optimization. Part I Description of the Algorithm," JVST B, 13(6), p. 2518(1995).
68. M.Burkhardt, S. Silverman, H. I. Smith, K.Rhee and M. Peckerar, "Gap Control In Fabrication of Quantum Effect Devices Using X-Ray Nanolithography," Microelectronic Engineering 7(1-4), 307(1995).
69. C.Marrian, S. Chang and M. Peckerar, Proximity Correction for Electron Beam Lithography, Opt. Eng., 35(9), 2685(1996).

70. M. Peckerar, C. Marrian and F.K. Perkins "Feature Contrast in Dose-Equalization Schemes Used for Electron-Beam Proximity Control," JVST B 14(6), 3880(1996).
71. M. Peckerar, "South Korea: A New Tiger Faces New Technology Issues," Solid State Technology, p. 77 Sept. 1996.
72. C.R.K. Marrian, F.K. Perkins, D.W. Park, E.A. Dobisz, K.W. Rhee, R. Bass and M. Peckerar, "Modeling of Electron Elastic and Inelastic Scattering," JVST B 14(6), 3864(1996).
73. Wang, W.; Chang, C.; Ma, D.; Peckerar, M.; Berry, I.; Goldsman, N.; Melngailis, J., "Self-aligned sub- channel implant complementary metal-oxide semiconductor devices fabrication," JVST B (Microelectronics and Nanometer Structures) 15(6), pp. 2816-20(1997).
74. F.K. Perkins, C.R.K. Marrian and M. Peckerar, "Novel Technique for Improving Pattern Placement in Membrane Mask Making," JVST B 15(6) 2218(1997).
75. Shen, C.C., Murguia, J., Goldsman, N. Peckerar, M.C., Melngailis, J., "Use Of Focused Ion Beams and Modeling to Optimize Sub-micron MOSFET Characteristics, , IEEE Trans. ED 45(2), 453(1998).
76. Perkins, F.K., Peckerar, M.C., McCarthy, D. M. and Marrian, C.R.K., "Improving Electron Beam pattern placement with Through-the-Membrane Signal Monitoring," JVST-B 16(6)3567(1998).
77. Wang, W. McCarthy, D. Park, D. Ma, D. Marrian, C. Peckerar, M. Goldsman, N., Melngailis, J. and Berry, I.L., "Fabrication and characterization of buried sub-channel implant n-metal-oxide- semiconductor transistors," JVST B (Microelectronics and Nanometer Structures), 16(6), 3812- 16(1998).
78. Grun J, Fischer RP, M. Peckerar, D.W. Donnelly and B.C. Covington, "Athermal annealing of phosphorus-ion-implanted silicon," Appl. Phys. Lett. 77 (13) (2000).
79. M. Peckerar, R. Bass and K.-W.Rhee "Sub-0.1 mu electron-beam lithography for nanostructure development," JVST B 18(6) 3143(2000).
80. Grun J, Fischer RP, M. Peckerar, D.W. Donnelly and B.C. Covington, "Athermal Annealing of Silicon Implanted With phosphorus and Arsenic," in Electrochemical Society Proceedings Vol. 2000-9 (Rapid Thermal and Other Short-Time Processing Technologies) 107(2000).
81. D.W. Donnelly and B.C. Covington, Grun J, Fischer RP and M. Peckerar, "Athermal Annealing of Low-Energy Boron Implants in Silicon," Appl. Phys. Lett 78 (14), 2002 (2001).
82. Peckerar, M.; Perkins, F.K.; Hodge-Miller, A.; Ehrlich, R.; Fertig, S.; Tender, L. "Sensor Sensitivity Training," In IEEE Circuits and Devices Magazine 19(2), pp. 17-24(2003): IEEE, Journal Paper. (AN: 7594389)
83. M. Peckerar, "Addressing Myths Of Science And Public Policy In The United States. Part I," In IEEE Technology and Society Magazine 22(1), pp. 23-33(2003): IEEE, Journal Paper. (AN: 7556264)
84. M. Peckerar, "Addressing myths of science and public policy: Part II" In IEEE Technology and Society Magazine 23(1) pp. 29-35(2004) : IEEE, Journal Paper. (AN: 7996446)
85. M. Peckerar, "Preface to the 49th International Conference on Electron, Ion, Photon Beam and Nanofabrication Conference," JVST-B, 23(6), 2577(2005).
86. C.R. Eddy, Jr., M.A. Mastro, N.D. Bassim, M.E. Twigg, R.L. Henry, R.T. Holm, J.C. Culbertson, O.J. Glembocki, J.D. Caldwell, P.G. Neudeck, A.J. Trunek, J.A. Powell,
87. M.C. Peckerar, Y. Ngu, F. Yan and S. Babu, "Approaches to Reduced-Defect Active Regions for III-N Devices," ECS Transactions 3, 117-123 (2006).

88. C. Eddy, R. Holm, R. Henry, M. Twigg, N. Bassim, L. Shirey, O. Glembocki, J. Culbertson, F. Perkins, M. Peckerar, Y. Ngu, F. Yan, " Improved GaN Materials and Devices through Confined Epitaxy, Appl. Phys. Lettrs. 90, 162101 (2007).
89. Y. Ngu, M.Peckerar, N. Goldsman, M. Khbeis, G. Metze, "An Electrochemical Cell with Capacitance-Enhanced Double Layer," ECS Transactions Volume 3, "Intercalation Compounds for Batteries and Hybrid Supercapacitors."
90. Akturk, A., Allnutt, J., Dilli, Z., Goldsman, N., Peckerar, M., "Device Modeling at Cryogenic Temperatures: Effects of Incomplete Ionization," IEEE Transactions on Electron Devices 54(11), pp. 2984 – 2990(2007).
91. Y. Ngu, M. Peckerar, X. Liu, M. Dagenais, J. Barry, and B. Dutt. "Lithography, Plasmonics and Subwavelength Aperture Exposure Technology," JVST-B 25(6), pp. 2471 - 2475 (2007).
92. M. Peckerar, D.Sanders, A. Foli A. Srivastava and U. Vishkin"Recent Advances in Proximity Effect Correction for Electron Beam and Optical Lithography," JVST-B 25(6), pp. 2288 – 2294(2007).
93. Dilli, Z., Goldsman, N., Peckerar, M., Akturk, A., Metze,G., "Design and testing of a self-powered 3D integrated SOI CMOS system," Microelectronic Engineering 85(2), pp. 388-394(2008).
94. Adl, S. Peckerar, M., "Low-Noise Signal Processing Chain for High Capacitance Sensors," IEEE Sensors Journal 8(11), pp.1864 – 1870(2008).
95. Chung-Ching Shen, Kupershtok, R., Adl, S., Bhattacharyya, S.S., Goldsman, N., Peckerar, M., "Sensor Support Systems for Asymmetric Threat Countermeasures," IEEE Sensors Journal 8(6), pp. 682 – 692(2008).
96. Currano, L.J., Bauman, S., Churaman,W., Peckerar, M., Wienke, W., Kim, S., Yu, M., Balachandran,B., "Latching ultra-low power MEMS shock sensors for acceleration monitoring," Sensors and Actuators A: Physical 147(2), pp. 490-497(2008).
97. Kanyogoro, E., Peckerar, M., Hughes, H., Liu M., "Band gap engineered resistor for mitigating linear energy transfer sensitivities in scaled submicron CMOS technology SRAM cells," Solid-State Electronics 52(10), pp. 1555-1562(2008).
98. Seokjin Kim, Elkis, R., Peckerar, M., "Device Verification Testing of High-Speed Analog-to-Digital Converters in Satellite Communication Systems," IEEE Transactions on Instrumentation and Measurement, 58(2), pp. 270 – 280(2009)
99. Salter, T., Choi, K., Peckerar, M., Metze, G., Goldsman, N., "RF energy scavenging system utilising switched capacitor DC-DC converter," Electronics Letters 45(7), pp. 374-376(2009).
100. Lauritzen, K. C., Talisa, S. H. , Peckerar, M. ," Impact of de-correlation Techniques on Sampling Noise in Radio-Frequency Applications," IEEE Trans. Instrumentation and Measurement 59(9), pp.2272-2279(2010).
101. Y.Ngu, M.Peckerar, D. Sander, C. Eddy, M. Mastro, J. Hite, R. Holm, R. Henry, and A. Tuchman, "Array of Two UV-Wavelength Detector Types," IEEE Trans. ED 57(6), pp. 1224-1229(2010).
102. Akturk, M. Holloway, S. Potbhare, D. Gundlich, B. Li, N.Goldsman, M. Peckerar, K. Cheung, "Compact and Distributed Modeling of Cryogenic Bulk MOSFET Operation," IEEE Trans. ED 57(6), pp. 1334-1342(2010).
103. C.K Choi, F. Yesikloy, A. Cryssis, M. Dagenais and M. Peckerar, "New Process Development for Planar-Type SIS Tunnel Diodes," Electr. Dev. Lettrs 31(8), pp 809-811(2010).
104. F. Yesilkoy,, K. Choi, M. Dagenais, and M. Peckerar, "Implementation of E-Beam Proximity Effect Correction using linear programming techniques for the fabrication of asymmetric bow-tie antennas," Solid-State Electronics 54(10), pp. 1211-1215(2010).

105. Akturk, M. Peckerar, K. Eng, J. Hamlet, S. Potbhare, E. Longoria, R. Young, T. Gurrieri, M. S. Carroll, N. Goldsman, "Compact Modeling of 0.35 mm SOI CMOS Technology Node for 4 K DC Operation using Verilog-A," Microelectronic Engineering 87(12) 2518-2524(2010.)
106. Liu G, Wen B, Xie T, et al. Top-down fabrication of horizontally-aligned gallium nitride nanowire arrays for sensor development. *Microelectronic engineering*. 2015;142:58-63. doi:10.1016/j.mee.2015.08.004
107. Liu G, Lowy DA, Kahrim A, Chao Wang, Zeynep Dilli, Nick Kratzmeier, Wei Zhao, Martin Peckerar. A low cost micro-heater for aerosol generation applications. *Microelectronic engineering*. 2014;129:46-52. doi:10.1016/j.mee.2014.07.011
108. Wang C, Liu G, Dilli Z, Peckerar M, Park M, Zhao W. An ultra-low power regulator system for wSNs powered by energy harvesting. *Solid-State electronics*. 2014;101:38-43. doi:10.1016/jsse.2014.06.015
109. Zhao W, Choi K, Bauman S, et al. An energy harvesting system surveyed for a variety of unattended electronic applications. *Solid state electronics*. 2013;79:233-237. doi:10.1016/j.sse.2012.09.008
110. Zhao W, Bauman S, Dilli Z, Peckerar M, Choi K, Salter T. A radio-frequency energy harvesting scheme for use in low-power ad hoc distributed networks. *IEEE transactions on circuits and systems iI: express briefs*. 2012;59(9):573-577. doi:10.1109/TCSII.2012.2206935
111. Yesilkoy F, Mittal S, Goldsman N, Dagenais M, Peckerar M, Berlin 20110919-20110923 Berlin 20110919-20110923. A new process for the fabrication of planar antenna coupled ni-NiOx-Ni tunnel junction devices. *Microelectronic engineering*. 2012;98:329-333. doi:10.1016/j.mee.2012.07.078
112. Wei Zhao, Kwangsik Choi, Bauman S, Dilli Z, Salter T, Peckerar M. A radio-frequency energy harvesting scheme for use in low-power ad hoc distributed networks. *IEEE transactions on circuits and systems iI: express briefs*. 2012;59(9). doi:10.1109/TCSII.2012.2206935
113. Wright J, Trotter DC, Zortman W, *Anthony*, L. Lentine, Eric Shaner, Michael R. Watts, Akin Akturk, Marty Peckerar, Advanced Photonics Congress. In: *Cryogenic Operation of Silicon Photonic Modulators*. OSA; 2012:5. doi:10.1364/IPRSN.2012.IM2A.5
114. Li B, Zhai Y, Yang B, Salter T, Peckerar M, Goldsman N. Ultra low power phase detector and phase-locked loop designs and their application as a receiver. *Microelectronics journal*. 2011;42(2):358-364. doi:10.1016/j.mejo.2010.10.010
115. Maldonado JR, Peckerar M.," X-ray lithography: some history, current status and future prospects," *Microelectronic engineering*. 2016;161:87-93. doi:10.1016/j.mee.2016.03.052
116. Jensen KL, Shiffler DA, Peckerar M, Harris JR, Petillo JJ. Current from a nano-gap hyperbolic diode using shape-factors: theory. *Journal of applied physics*. 2017;122(6):064501-064501. doi:10.1063/1.4997457
117. X.Sun,Y.Zhang,P-C Huang, N.Acharjee, M.Dagenais, M.Peckerar,"Correcting the Proximity Effect in Nanophotonic Phased Arrays," in *IEEE Transactions on Visualization and Computer Graphics*, vol. 26, no. 12, pp. 3503-3513, Dec. 2020, doi: 10.1109/TVCG.2020.3023601.

Refereed conference proceedings:

1. M. Peckerar, H.C. Lin and R. Kocher, "Open Circuit Voltage of MIS Schottky Diode Solar Cells", Proc. IEEE IEDM, 213 (1975).

2. M. Peckerar, P. Pai, H.C. Lin, and R. Kocher, "Ion Implanted Schottky Solar Cells", Proceeding of 1976 IEDM

3. M. H. White, J. Dzimianski, and M. Peckerar, "Influence of Electric Field Strength and Oxide Composition on Charge Retentivity and Endurance of Thin-Oxide, Non-Voltage MNOS Memory Transistors", Proceeding of 1976 IEDM.

4. M. Peckerar, "X-Ray Quantum Efficiencies of CCD's", Proceeding of the NASA/JPL Conference on Charge-Coupled Device Technology and Applications, Nov. 30 - Dec. 2, 1976, p. 106.

5. M. Peckerar, "Self-Aligned CMOS Processing with Rh and Ag L-Line X-ray Sources", Proc. IEEE IEDM 1978.

6. M. Peckerar, "High Speed X-ray Lithography with Radiation from Laser-Produced Plasma", Proc. Symp. Elect. Ion Beam Tech. Electrochem. Soc. Pub. 78-5 432 (1978).

7. D. Nagel and M. Peckerar, "Laser-Plasma Source for Pulsed X-ray Lithography", Proc. SPIE, 246 (1978).

8. M. Peckerar and D. McCarthy, "Area Array X-ray Sensor," Proc. SPIE , 217, #15 (1979).

9. M. Peckerar, "Radiation Effect in Semiconductor Devices with Regard to Synchrotron Lithography", Lithography/Microscopy Beamline Design Workshop, Stanford Synchrotron Rep't. 79-02, 110 (1979). Invited

10. M. Peckerar, "Deep Depletion CCDs for X-ray and IR Sensing", IEEE IEDM, 144 (1979)

11. M. Peckerar, K. Galloway, "Informal Survey of Federal Government Microelectronics Processing Facilities", Symp. Proc. University/Gov't Industry Microelectronics, Starksville, Miss. III-24 (1981).

12. M. Peckerar, C. H. Dozier and D. Brown, "X-ray and E-beam Lithography Effects on Short and Narrow Channel MOSFETs," Proceedings 1982 GOMAC Conference.

13. M. Peckerar and D. Nagel, "X-ray Lithography with Laser Driven Plasmas", IEEE Workshop on Micrometer and Submicrometer Lithography (1984).

14. M. Peckerar and D. Nagel, "Picosecond Laser Plasma X-ray Source", Nagel) Proc. Ion Electron Photon Beams Conf., Tarrytown, NY, May (1984).

15. M. Peckerar, "Current Status of Solid-State X-ray Systems", Proc. 43rd Annual Meeting of the Electron Microscopy Society of America, Bailey, G.H. (ed.) San Francisco Press, (1985).

16. Christou, A., Tseng, W., Peckerar, M., Anderson, W.T., McCarthy, D.M., Buot, F.A., Campbell, A.B., Knudson, A.R., 23rd Annual Reliability Physics Symposium, March 1985 pp. 54 – 59(1985).

17. J.T. Bosiers, M. Peckerar, N.S. Saks, D.J. Michels, D. McCarthy , "Deep-Depletion CCDs for UV and X-ray Imaging for Astronomy", (with) Proc. CICC85, pp. 124-127, Portland, OR (1985)
18. M. Peckerar, J.F. Brown, E.C. Soltani "Fabrication of Gas-Liquid Control Device for Sorting/Cloning Animal Cells", Proc. IEEE Synthetic Microstructures in Biological Research Conf. Airlie, VA, Mar. 23-26 (1986).

19. M. Peckerar, A.P. Oliver, R.J. Wyatt, and D.L. Peterson "Fabricated Array Microelectronics in a System for Study of Cultured Nerve Cells", published Proc. IEEE Synthetic Microstructures in Biological Research Conf. Airlie, VA, Mar. 23-26 (1986).

20. M. Peckerar, D.J. Michels, N.S. Saks, J.T. Bosiers, D. McCarthy "CCD for High Resolution Imaging in the Far and Near Ultraviolet", Proc. SPIE 30th Annual Inter. Tech. Symp. 17-22 Aug. 1986/San Diego, CA.

21. C.T. Yao, M. Peckerar, D. Friedman and H. Hughes, "Hot Electron Effect on MOSFET Terminal Capacitances" (with) Proc. IEEE 1586 CICC86, p. 208 (1986).

22. C. Yao, M. Peckerar, J. Wasilik, C. Amazeen, S. Bishop "A Novel Three Dimensional Microstructure Fabrication Technique For A Triaxial Profile Sensor Array," Proc. IEEE Microrobots and Teleoperators Workshop, Hyannis, MA, (1987).

23. C. Marrian and M. Peckerar, "An Electronic Neural Net Algorithm For Maximum Entropy Deconvolution", Proc. 1st Annual IEEE International Conf. on Neural Networks, San Diego, CA. (1987).

24. Dutta, P., Candela, G.A., Chandler-Horowitz, D.; Peckerar, M.C., "Spectroscopic ellipsometry of oxygen-ion-implanted silicon-on-insulator annealed at different temperatures," Proceedings of the1988 IEEE SOS/SOI Technology Workshop, p. 34, 3-5 Oct. 1988.

25. Pati, Y.C.; Friedman, D.; Krishnaprasad, P.S.; Yao, C.T.; Peckerar, M.C.; Yang, R.; Marrian, C.R.K. and M. Peckerar, "Neutral networks for tactile perception,".Proceedings of the 1988 International Conference on Robotics and Automation, 24-29 April 1988 Page(s):134 - 139 vol.1

26. R. Rakhit, C. Yao and M. Peckerar, "An Investigation of the Time Dependence of Current Degradation in MOS Devices," Proc. Proc. IEEE 1989 International Reliability Physics Symposium, 103 (1989).

27. Schnur, J.M. Calvert, J. Peckerar, M. Schoen, P. Marrian, C. Price, R. Singh, A. Rudolph, Georger, J., Stockton, W., Dulcey, C. and Testoff, M., "Bio/technological and biomaterial applications of self-assembly," Engineering in Medicine and Biology Society, 1989. Images of the Twenty-First Century. Proceedings of the Annual International Conference of the IEEE Engineering, 9-12 Nov. 1989 Page(s):1373 - 1374 vol.4

28. Campisi, G.J., Ma, D.I., Quadri, S.B. and Peckerar, M.C., "X-ray characterization of

silicon on insulator substrates," SOS/SOI Technology Conference, 1990., 1990 IEEE 2-4 Oct. 1990
Page(s):75 – 76.

29. E. Barouch, S.A.Orszag, Brian Bradie, U. Hollerbach, and M.Peckerar, "Modeling Process Latitude in Deep UV And X-ray Lithography," Proc. SPIE Ion, Electron And Photon Beams, vol. 1465, p. 254 (1991).

30. J. Calvert, M.-S. Chen, C. Dulcey, J. Georgier, J. Schnur, P. Schoen and M. Peckerar, "Deep UV Lithography Of Monomer Films With Selective Metallization," (With), in ULSI Science and Technology/1991, Electrochemical Society Proc. Vol 91-11, J. Andrews, G. Celler, eds., p145 (1991).

31. Ting, A.C., Tang, C.M., Ma, D.; McCarthy, D.; Peckerar, M., and Swyden, T.A.; "Field Emitter Arrays With Current Saturation And Current Control Capabilities," Plasma Science, 1991. IEEE Conference Record - Abstracts., 1991 IEEE International Conference 3-5 June 1991 Page(s):94 – 95

32. Tipton, C.W. and Peckerar, M. "SPICE simulation of thin-film SOI IGFETs Using the BSIM2 model," IEEE International SOI Conference Proceedings, IEEE International 1-3 Oct. 1991 Page(s): 68 – 69

33. Eytan Barouch, Uwe Hollerbach, Steven A. Orszag, Martin Peckerar and Milton Rebbert," Simulation Fidelity in Microlithography", Electron-Beam, X-Ray, and Ion-Beam Submicrometer Lithographies for Manufacturing II, Proc. SPIE 1671, edited by Martin Peckerar, 8-9 March 1992, San Jose, CA. (1992).

34. J. M. Calvert, P. E. Pehrsson, C. S. Dulcey, and M. C. Peckerar, "Selective Metallization of CVD Diamond Films", Mat. Res. Soc. Symp. Proc. Vol 260, 1992, Materials Research Society.

35. Barouch, E. Coifman, R. Ma, J. Peckerar, M.C. and Rokhlin, V., "Advanced transformational analysis applied to e-beam proximity effect correction," Proceedings of the SPIE - The International Society for Optical Engineering 1993, vol.1924, pp. 150-70

36. M. Peckerar, M. Rebbert, and G. Gopalakrishnan, "High Aspect Ratio Resist Structures for Optoelectronic (and Other) Applications," Proc. SPIE - Int. Soc. Opt. Eng. (USA), Proc. of the SPIE - The International Society for Optical Engineering, vol.2045, p. 298-305(1993).

37. E.A. Dobisz, M. C. Peckerar, W. Chu, K. Rhee, L.S. Shirey, C.R.K. Marrian, R.E. Salvino, K. Foster and John Kosokowski, "Materials Issues In X-Ray Lithography", Mat. Res. Soc. Symp. Proc. Vol 306, p. 3, 1993, Materials Research Society.

38. Chang, S., Peckerar, M. and Marrian, C.; "Maximum entropy co-processor for computed tomography," Proceedings of the IEEE Custom Integrated Circuits Conference, 1-4 May 1994 Page(s):343 – 346

39. Glembocki, O.J., Tuchman, J.A., Holm, R.T., Peckerar, M.C., "Fourier transform analysis of

Franz- Keldysh oscillations in electromodulation spectroscopy," IEEE Lasers and Electro-Optics Society Annual Meeting, LEOS '94 Conference Proceedings. 2, pp. 214 - 215 vol.231 Oct.-3 Nov. 1994

40. C.R.K. Marrian and M. Peckerar, "Error Measure Comparison of Currently Employed Dose- Modulation Schemes for e-Beam Proximity Effect Control, " Proc. SPIE, Vol. 2437, in Electron- Beam, X-Ray, EUV and Ion-Beam Submicrometer Lithographies for Manufacturing, J..M. Warlaumont, ed., p. 222(1995).

41. C.R.K. Marrian, S. Chang and M. Peckerar, "Proximity Correction for e-Beam Lithography," Proc. 15th Annual Symposium of Photomask Technology and Management (BACUS Conference), Appearing as SPIE vol. 2621, 2(1995).

42. D. Prather, J. Mait, M.C. Peckerar and A. Christou, "Design and Fabrication of an Off-Axis Fresnel Generator as a Module for Optical Inerconnects, Army Coference on Photonics, US Missile Command, Redstone Arsenal, AL, April 1995.

43. M. Peckerar, C.R.K. Marrian "Pattern Density Dependent Contrast In Commonly Used Dose- Equalization Schemes," D. Seeger, ed., Proc. SPIE. Vol. 2723, p. 134(1996).

44. F.K. Perkins, S. McCarthy and C.R.K. Marrian and M. Peckerar, "Position Measurement of High- Energy e-Beams for Pattern Placement Improvement," D. Seeger, ed., Proc. SPIE. Vol. 2723, p. 91(1996).

45. M. Peckerar, "Active Sensor Arrays for Biomarker Detection (in vivo and in vitro)", presented at the NIH BECON Nanoscience and Nanotechnology Symposium - June 25-26, 2000, Bethesda, MD

46. M. Peckerar, "GaN UV Detectors," in X-rays to X-Band, Space Astrophysics Detectors and Detector Technologies,", presented 26 June – 30 June, 2000, at the Space Telescope Science Institute, Johns Hopkins University, Baltimore, MD Invited

47. F.K. Perkins and M. Peckerar, "An Active Microelectronic Transducer for Enabling Label-Free Miniature Macromolecule Sensors," IEEE International Electron Devices Meeting, Dec. 4, 2000, San Francisco, CA.

48. M. Peckerar, "The National Nanoscience Innitiative (NNI)," SEMI Technology Symposium 2001, Dec. 5-5 (2001) Tokyo, JP. Invited.

49. Scribner, D., Humayun, M., Justus, B., Merritt, C., Klein, R., Howard, J.G., Peckerar, M., Perkins, F., Johnson, L., Bassett, W., Skeath, P., Margalit, E., Kah-Guan Au Eong, Weiland, J., de Juan, E.; Finch, J., Graham, R., Trautfield, C., Taylor, S., "Intraocular retinal prosthesis test device," Proceedings of the 23rd Annual International Conference of the IEEE Engineering in Medicine and Biology Society 4, pp. 3430 – 3435, 25-28 Oct. 2001.

50. Donnelly, D.W., Covington, B.C., Grun, J., Fischer, R.P., Peckerar, M., Felix, C.L., Djordjevic, B.B., Mignogna, R., Meyer, J.R., Ting, A., Manka, C.K., "Athermal annealing of ion-implanted silicon," 9th International Conference on RTP 2001 Advanced Thermal Processing of Semiconductors,
pp. 133 – 144, 25-29 Sept. 2001.

51. Yongsunthon, R., Williams, E.D., Stanishevsky, A., McCoy, J., Pego, R., Rous, P.J., and Peckerar, M. , "Magnetic Force Microscopy Signatures Of Defects In Current-Carrying Lines," M. Edited by: Gerhardt, R.A., Washabaugh, A.P., Alim, M.A., Choi, G.M. In Electrically Based Microstructural Characterization III. Symposium (Materials Research Society Symposium Proceedings Vol.699), 2002, pp. 107-12, xi+356 pp. USA, Warrendale, PA : Mater. Res. Soc, Conference Paper. (AN: 7625708)

52. Scribner, D.A.; Humayun, M.S.; Justus, B.L.; Merritt, C.D.; Klein, R.B.; Howard, J.G.; Peckerar, M.C.; Perkins, F.K.; Johnson, L.J.; Bassett, W.; Skeath, P.; Weiland, J.; de Juan, E., Jr.; Finch, J.A.; Graham, R.W.; Trautfield, W.C.; Taylor, S.M. "Toward A Retinal Prosthesis For The Blind: Advanced Microelectronics Combined With A Nanochannel Glass Electrode Array," In Proceedings of the SPIE - The International Society for Optical Engineering, 2002, vol.4608,
pp. 239-44 : SPIE-Int. Soc. Opt. Eng, Journal Paper. (AN: 7673141)

53. Perkins, F.K., Tender, L.M., Fertig, S.J., and Peckerar, M.C. "Sensing Macromolecules With Microelectronics," In Proceedings of the SPIE - The International Society for Optical Engineering, 2002, vol.4608, pp. 251-65 : SPIE-Int. Soc. Opt. Eng,, Journal Paper. (AN: 7673143)

54. M. Peckerar, "Nanoscience: A New Thrust For Science In The 21st Century?" Peckerar, M.C. In Proceedings of the SPIE - The International Society for Optical Engineering, 2002, vol.4608, pp. 1-18: SPIE-Int. Soc. Opt. Eng,; Journal Paper. (AN: 7673112)

55. Hodge-Miller, A., Perkins, F.K., Peckerar, M., Fertig, S. and Tender, L. "Gateless depletion mode field effect transistor for macromolecule sensing," Proceedings of the 2003 International Symposium on Circuits and Systems - ISCAS '03 3, 25-28 May, pp. III-918 - III-921(2003).

56. Scribner, D., Johnson, L., Klein, R., Bassett, W., Howard, J.G., Skeath, P., Wasserman, L., Wright, B., Perkins, F., Peckerar, M., Finch, B.J., Graham, R., Trautfield, C., Taylor, S., Humayun, M., "A retinal prosthesis device based on an 80×40 hybrid microelectronic-microwire glass array," Proceedings of the IEEE 2003 Custom Integrated Circuits Conference, pp. 517 – 520, 21-24 Sept. 2003.

57. Hu Huang, Bernstein, J.B., Peckerar, M. and Ji Luo "Combined Channel Segmentation And Buffer Insertion For Routability And Performance Improvement Of Field Programmable Analog Arrays In Proceedings. IEEE International Conference on Computer Design: VLSI in Computers and Processors, 2004, pp. 490-5, xviii+578 pp. USA, Los Alamitos, CA : IEEE Comput. Soc, Conference Paper. (AN: 8381255)

58. Dilli, Z., Goldsman, N., Peckerar, M. and Metze, G. "Realization Of Self-Powered Electronics By 3D Integration," In 2005 International Semiconductor Device Research Symposium (IEEE Cat. No.05EX1272C), 2005, 2 pp., CD-ROM pp. USA, Piscataway, NJ, IEEE, Conference Paper. (AN: 8931886)

59. M. Peckerar, "SiGe Design Techniques for High-Speed Analog-to-digital Conversion," DARPA Trusted Foundry Circuit Designers Meeting, 2-3 August 2006, Burlington, VT. Invited.

60. M. Peckerar, “Cost Issues Relating To The Production of Military Electronics,” Invited Talk, DARPA/MTO Nanofab Workshop, November 6,7, 2006 Midway Utah. Invited.

61. C. R. Eddy, M. Mastro, N. Bassim, M. Twigg, R. Henry, R. Holm, J. Culbertson, O. Glembocki, J. D. Caldwell, P. Neudeck, A. Trunek, J. Powell, M. Peckerar, Y. Ngu, F. Yan and S. Babu, “Approaches to Reduced-Defect Active Regions for III-N Devices,” 210th ECS Meeting - Cancun, Mexico, October 29 -November 03, 2006,E14 - State-of- the-Art Program on Compound Semiconductors 45 (SOTAPOCS 45).

62. M.Peckerar and F. Cerrina, "Patterning and Metrology With FEL Light," University of Wisconsin/NSF Workshop, Madison, Wisconsin, October 18-19, 2006. Invited

63. Xinhua He, Weixin Kong, Firestone, T., Newcomb, R., Peckerar, M. "Phase noise optimization of a symmetric CMOS LC VCO," In 2006 IEEE International Symposium on Industrial Electronics, 2006, pp. 2820-3, CD-ROM pp. USA, Piscataway, NJ : IEEE, Conference Paper.

64. S. Adl and M. Peckerar, “ A Low Noise Pre-Amplifier/Amplifier Chain for High Capacitance Sensor Arrays,” To appear in the Proceedings of the 2007 IEEE Sensor Applications Symposium. This paper won the best student paper award.

65. Seokjin Kim, Elkis, R., Peckerar, M.C., “Device verification tests for high speed analog to digital converters used in satellite communication systems,” IEEE Autotestcon 2007, pp. 445 – 454, 17-20 Sept. 2007. (Won Best Student Paper Award).

66. Y. Ngu, M. Peckerar, X. Liu, M. Dagenais, J. Barry, M. Messina, Z. Shao and B. Dutt.,, “Lithography, Plasmonics and Subwavelength Aperture Exposure Technology,” Presented at the 2007 CLEO meeting in Baltimore Md, May 2007.

67. M. Peckerar, A. Foli and A. Srivastava, “Recent Advances in Proximity Effect Correction for Electron Beam and Optical Lithography,” Presented at the 2007 Electron, Ion, Photon Beam and Nanofabrication Conference, Denver, CO, June 2007.

68. P-H Chen and M. Peckerar, “A 5-Bit Interpolating Flash ADC in 0.13mm SiGe BiCMOS Technology,” Presented at and accepted for publication in the proceedings of the IEEE ICICDT conference, May 2007.

69. C.-C. Shen, R. Kupershtok, S. Adl, S. Battacharyya, N. Goldsman, M. Peckerar, "Sensor Support Systems for Asymmetric Threat Countermeasures," Presented at the 2007 Nano-electronic Devices for Defense and Security Conference, Crystal City, VA, 18-21 June 2007.

70. Ngu, Y.T., Dilli, Z., Peckerar, M., Goldsman, N., “High capacitance battery for powering distributed networks node devices,” 2007 International Semiconductor Device Research Symposium, pp.1 – 2, 12-14 Dec. 2007

71. Kanyogoro, E., Peckerar, M., Hughes, H., Liu, M., “High resistivity material for mitigating linear energy transfer sensitivities in highly scaled Cmos Sram cells,” 2007 International Semiconductor Device Research Symposium, pp. 1 – 2, 12-14 Dec. 2007.

72. Seokjin Kim, Peckerar, M.C., "High speed analog-to-digital converter design verification tests in satellite receivers," International Symposium on Communications and Information Technologies - ISCIT '07, pp. 110-115(2007).

73. Seokjin Kim, Kwangsik Choi, Peckerar, M., Christou, A., "Line-spike induced failure mechanism in integrated circuit bond-wires," IEEE International Reliability Physics Symposium - IRPS 2008, pp. 647 – 648, April 27-May 1 2008.

74. Seokjin Kim, Peckerar, M., "High-speed ADC dynamic performance validation: The impact of skew-corner lot testing," 2008 IEEE AUTOTESTCON, pp. 29 – 32, 8-11 Sept. 2008. Won Best Student Paper (second year in a row!)

75. K. Choi, M.Dagenais, M. Peckerar, "Fabrication Of A Thin Film Asymmetric Tunneling Diode Using Geometric Field Enhancement," International Semiconductor Device Research Symposium, 2009. ISDRS '09. Digital Object Identifier: 10.1109/ISDRS.2009.5378297, pp. 1 – 2(2009).

76. M. Park, K. Choi, S. Singh, S. Aslam, M Peckerar, " Low leakage current technology in P+N silicon photodiode detector," International Semiconductor Device Research Symposium, 2009. ISDRS '09. Digital Object Identifier: 10.1109/ISDRS.2009.5378119, pp. 1 – 2(2009).

77. F. Yesilkoy, M. Peckerar, International Semiconductor Device Research Symposium, 2009. ISDRS '09. Digital Object Identifier: 10.1109/ISDRS.2009.5378016, pp. 1 – 2(2009)

78. M. Park; K. Choi; Peckerar, "Ultra-low power series pass element voltage regulator for RF-DC energy harvesting," International Semiconductor Device Research Symposium, 2009. ISDRS '09. Digital Object Identifier: 10.1109/ISDRS.2009.5378128, pp. 1 – 2(2009).

79. Akturk, A. Holloway, M. Gundlach, D. Potbhare, S. Li, B. Goldsman, N. Peckerar, M. Cheung, K.P., "Distributed numerical modeling of low temperature MOSFET operation," International Semiconductor Device Research Symposium, 2009. ISDRS '09. Digital Object Identifier: 10.1109/ISDRS.2009.5378004, pp. 1 – 2(2009)

80. Akturk, A., Peckerar, M. ,Dornajafi, M. , Goldsman, N. ; Eng, K. ; Gurrieri, T. , Carroll, M.S. , "Impact Ionization and Freeze-Out Model for Simulation of Low Gate Bias Kink Effect in SOI-MOSFETs Operating at Liquid He Temperature," in the proceedings of the International Conference on the Simulation of Semiconductor Processes and Devices, Digital Object Identifier: 10.1109/SISPAD.2009.5290227, Publication Date : 9-11 Sept. 2009 .

81. M. Peckerar, M. Dornajafi, Z. Dilli, N. Goldsman and M. Dagenais, "Power Distribution Systems for Distributed Sensor Networks and Pervasive Computing," 35th Annual GOMACTech Conference , MARCH 22-25, 2010 - Reno, NV (invited.)

82. K. Choi, G. Ryu, F. Yesilkoy, A. Chryssis, M. Dagenais, N. Goldsman, M. Peckerar,

"Surface Plasmon and Geometry Enhanced Asymmetric Rectifying Tunneling Diodes, 54th International Conference on Electron Ion and Photon Beam Technology and Nanofabrication, Anchorage, AK, 3June 2010.

83. M. Peckerar, "New Uses for Ruthenium: Future Material Demands," Materials Information Seminar, US Geological Survey, Reston, VA 9June2009 (invited.)

84. Zhao W, Peckerar M, 2012 IEEE 55th International Midwest Symposium on Circuits and Systems MWSCAS 2012 2012 IEEE 55th International Midwest Symposium on Circuits and Systems, MWSCAS 2012 Boise, ID, USA 2012 08 05 - 2012 08 08. A novel tunable neural oscillator for biological rhythmic behaviors. *Midwest symposium on circuits and systems*. 2012;77-80:77-80. doi:10.1109/MWSCAS.2012.6291961

85. Holness A, Steins E, Bruck H, Peckerar M, Gupta S.K, ASME 2016 International Design Engineering Technical Conferences and Computers and Information in Engineering Conference IDETC/CIE 2016 ASME 2016 International Design Engineering Technical Conferences and Computers and Information in Engineering Conference, IDETC/CIE 2016 2016 08 21 - 2016 08

86. Holness A, Steins E, Bruck H, Peckerar M, Gupta S.K, Performance characterization of multifunctional wings with integrated flexible batteries for flapping wing unmanned air vehicles. *Proceedings of the ASME design engineering technical conference*. 2016;5a-2016. doi:10.1115/DETC2016-60379

87. Holness A, Steins E, Bruck H, Peckerar M, Gupta SK, ASME 2016 International Design Engineering Technical Conferences and Computers and Information in Engineering Conference ASME 2016 International Design Engineering Technical Conferences and Computers and Information in Engineering Conference Charlotte, North Carolina, USA. Volume 5a: 40th Mechanisms and Robotics Conference. In: *Performance Characterization of Multifunctional Wings with Integrated Flexible Batteries for Flapping Wing Unmanned Air Vehicles*. ASME; 2016:073. doi:10.1115/DETC2016-60379

88. Jensen KL, Shiffler DA, Peckerar M, Harris JR, Petillo JJ, 2017 30th International Vacuum Nanoelectronics Conference (IVNC) 2017 30th International Vacuum Nanoelectronics Conference (IVNC) Regensburg, Germany 2017 July 10 - 2017 July 14. 2017 30th International Vacuum Nanoelectronics Conference (ivnc). In: *Nanogap Diode Current Using Shape Factor Methods*. IEEE; 2017:18-19. doi:10.1109/IVNC.2017.8051533

89. Sun, Xuetong and Zhang, Yang and Huang, Po-Chun and Acharjee, Niloy and Dagenais,Mario and Peckerar, Martin and Varshney, Amitabh "Proximity Effect Correction for Fresnel Holograms on Nanophotonic Phased Arrays," *2021 IEEE Virtual Reality and 3D User Interfaces (VR)*, Lisboa, Portugal, 2021, pp. 353-362,doi:10.1109/VR50410.2021.00058.

90. S. Jabbireddy, Y. Zhang, M. Peckerar, M. Dagenais and A. Varshney, "Sparse Nanophotonic Phased Arrays for Energy-Efficient Holographic Displays," *2022 IEEE Conference on Virtual Reality and 3D User Interfaces (VR)*, Christchurch,

New Zealand, 2022, pp. 553-562, doi: 10.1109/VR51125.2022.00075.

91. P. -C. Huang, Y. Zhang, X. Sun, A. Varshney, M. Dagenais and M. Peckerar, "A Novel Compact Current Driver Circuit with Temperature Feedback Control for 2D Nanophotonic Phased Arrays," *2023 IEEE International Symposium on Circuits and Systems (ISCAS)*, Monterey, CA, USA, 2023, pp. 1-5, doi: 10.1109/ISCAS46773.2023.10181923.

92. M.Peckerar,P-C Huang, R.Jamil, B. Jacob, D.Yeung, L.Peckerar, "Xritical Issues on Advanced ReRAM Development," MEMSYS '23: Proceedings of the International Symposium on Memory Systems Article No.: 24, Pages 1 – 4, 2023. doi.org/10.1145/3631882.3631906

Fellowships, Prizes, and Awards:

Elected Fellow of the IEEE for contributions to Microlithography (1994), Life Fellow (2013)

Editorships, Editorial Boards, Providing Peer Reviews and Other Professional Activities:

Until January 2017, I was the US editor of the International Microelectronic Engineering Journal, an Elsevier Press publication with an impact factor of 1.583 (approximately equal to the 1.60 factor achieved by IEEE Transactions on Electron Devices, a journal with a similar target readership.)

I am on the advisory of the annual Electron, Ion and Photon Beams and Nanoscience Conference. This is an American Vacuum Society sponsored conference – perhaps the premier conference in nanoscience fabrication technology in the world, with over 500 attendees per meeting. It is holding its 54th conference this year. I was also on the steering committee for 5 years and served as conference technical chair in 2005.

Two Edison Patent Awards for best invention of the year while at NRL:

"Pulsed X-Ray Lithography," patent # 4,184,078. Licensed to Hampshire Instruments, Marlborough Massachusetts, 1992.

"High Resolution Patterning on Solid Substrates," US Patent # 5,079,600. Licensed by Shipley Corporation, 1992

Work with federal agencies:

Technical manager, US Advanced Lithography Program (1989-2000).

Navy Delegate to the Wassenaar Treaty on Limiting Proliferation of Electronic Weapon Systems (1997-2003).

Navy Delegate to the Controlled Commodities (CoCOM) Committee of the Department of Defense.

Government representative to the National Academy of Sciences panel on Materials for High Density Electronic Packaging and Interconnection (NMAB report 449) 1990.

Numerous NSF panels. Most recently the Nanomanufacturing Unsolicited Proposal Panel P061211, May 18-19, 2006 and Nano-, Micro-electronics Materials and Devices, 12-14 May 2010

MARTIN PECKERAR, Ph.D. - LITIGATION ADDENDUM

Expert Witness work and Paid Consultancies:

1. Expert Witness, DRAM technology, Milbank, Tweed Hadley McCloy, 2007-2010 (patent infringement on the physical implementation of the DDR3 specification.) Working with Jim Klaiber, now at Pryor Cashman. ITC Trial designation: Certain Dynamic Random Access MemoryDevices and Products Containing Same.) Investigation Number: 337-TA-595. Deposed twice.Testified before the ITC for three days.

2. Expert Witness, battery technology, Finnegan 2011 (relating to battery applications in powermtool technology.) Working on IPR with Tom Irving, representing Hitachi. IPR

3. Expert Witness, Non-Volatile Memory Technology, Winston Strawn 2014. Working with Vivian Kuo, J.C. Mascullo, David Enzminger and Dave Martens. ITC Trial designation: In the Matter of Certain Non-Volatile Memory Devices and Products Containing Same. This work included simulations of the chemical-mechanical polishing process for wafer planarization in integrated circuit fabrication technology. Investigation Number: 337-TA-909. Deposed twice. Testified before the ITC for two days.

4. Expert Witness, Matters relating to the layout and design of static random access memories,nvidia vs Samsung, working for Latham Watkins. IPR2015-01065. POCs Thomas Yeh and Bob Rosenberg, begun May 2015 and concluded in May, 2016. IPR. Deposed once.

5. Expert Witness, worked on an IPR in the matter of Postec and the validity of Milwaukee Tools patent on a lithium battery powered power tool. I worked for Middleton and Reutlinger (Robert H. Eichenberger, lead attorney.) Concluded June, 2017.

6. Expert Witness, in support of Nikon Corporation, Nikon Precision Inc., and Nikon Research Corporation of America, Inv. No. 337-TA-1137, defending against claims by ASML Netherlands. Concluded February 2019. Lead attorney: Sorin Zaharia.

7. Expert witness in support of VARTA Battery defending against claims by a variety of earbud distributers, concluding in January 2023. Deposed three times. I worked in support of Leydig, Voit and Meyer. Lead attorney: Wesley Meuller.

8. Technical Consultant, National Institute of Aerospace in the area of power distribution systems