



Characterization of tunnel oxide passivated contact fabricated by sputtering and ion implantation technique

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Tunnel oxide passivated contact (TOPCon) structures using highly doped n-type polycrystalline silicon were fabricated using facing target sputtering and ion implantation techniques for a SiH₄-free fabrication process of high-efficiency silicon solar cells. We investigated the structural and electrical properties of the highly doped n-type poly-Si layers to optimize the ion implantation process. We also investigated the surface passivation quality of our TOPCon structure. An effective carrier lifetime of 2.01 ms and an implied open circuit voltage of 704 mV were obtained for our sample annealed at 950 °C. The sample also exhibits a low contact resistance of $3.22 \times 10^{-3} \Omega \text{ cm}^{-2}$. Our results open the way for SiH₄-free fabrication of silicon solar cells with a TOPCon structure. © 2023 The Author(s). Published on behalf of The Japan Society of Applied Physics by IOP Publishing Ltd

1. Introduction

Tunnel oxide passivated contact (TOPCon) solar cells are highly efficient silicon solar cells that use an ultra-thin oxide layer and a highly phosphorus-doped polycrystalline Si (poly-Si) layer as a passivation structure.^{1–4} A conversion efficiency of 25.8% was achieved by Fraunhofer ISE in 2017^{3,5} for laboratory-scale-size solar cells, and a conversion efficiency of more than 24% was achieved for a large-area solar cell (244 cm²) fabricated using mass production technology.^{4,6,7} As of 2022, the passivated emitter and rear cell (PERC) structure^{8,9} is the mainstream of silicon solar cells. The production line of PERC solar cells can be easily upgraded to a production line of TOPCon solar cells by adding a few additional processes.¹⁰ Therefore, PERC solar cells are expected to be replaced by TOPCon solar cells, because a higher conversion efficiency is expected for TOPCon solar cells. The structures of PERC and TOPCon solar cells are shown in Fig. 1.

Currently, low-pressure CVD (LPCVD) is employed to deposit the poly-Si layer of a TOPCon solar cell in the mass production process. However, there are two drawbacks in the deposition of the poly-Si layer by LPCVD. The first drawback is that the poly-Si layer is deposited on both sides of the silicon wafer simultaneously in the LPCVD process.¹¹ In the TOPCon solar cell, the poly-Si layer is used only for the rear side of the solar cell. Therefore, an additional etching process of poly-Si deposited on the front side is required.¹² The second drawback is the use of explosive monosilane (SiH₄) gas. SiH₄ gas is the source of silicon in the LPCVD process, but it is desirable to avoid the use of high-pressure, toxic and explosive gases, such as SiH₄, in the mass production process for safety reasons. The deposition of highly phosphorus-doped amorphous silicon by plasma enhanced CVD (PECVD) and its subsequent thermal annealing for crystallization¹³ is a solution to the first drawback, since one-sided deposition is possible using PECVD. However, PECVD also requires SiH₄ and so this does not solve the second drawback. To solve both drawbacks, we investigate

the application of sputtering as the fabrication technique of the poly-Si layer in the TOPCon solar cell. There have only been a few reports on the fabrication of TOPCon structures using the sputtering technique.^{14,15} Therefore, it is important to intensively investigate the application of the sputtering technique for the fabrication of TOPCon structures.

To fabricate the poly-Si layer in TOPCon solar cells, we can use the thermal crystallization process of an amorphous silicon layer instead of the direct deposition of a poly-Si layer. In our previous study, we found that it is important to suppress the sputtering damage to the silicon wafer during the deposition of the amorphous silicon layers to obtain a good surface passivation quality of the TOPCon structure.¹⁶ Therefore, we employ facing target sputtering (FTS) as an alternative deposition technique for amorphous silicon in this study. In our previous publications, we reported the deposition of amorphous silicon by FTS under low sputtering damage conditions.^{17–19} FTS employs two facing sputtering targets, and the plasma is confined between the targets. This results in very low sputtering damage to the c-Si wafer. In addition, the targets are uniformly sputtered during the amorphous silicon deposition process, resulting in a long sputtering target lifetime compared with standard magnetron sputtering.

For the n-type doping, we employ the ion implantation technique instead of the standard phosphorus thermal diffusion process using phosphorus trichloride (POCl₃).¹¹ In previous publications, the application of ion implantation methods for fabricating TOPCon structures was reported.^{20–23} Ion implantation has the advantage of patterning the doping area and doping profile. This is very important to optimize the doping density of the TOPCon structure. In addition, it is important for the application of the TOPCon structure to interdigitated back contact (IBC) solar cells.^{24,25} At present, the fabrication process of TOPCon-IBC solar cells is very complicated due to the patterning of the n-type and p-type regions, both of which are located at the rear side of the solar cell. There are many studies aiming to reduce the fabrication cost of TOPCon-IBC



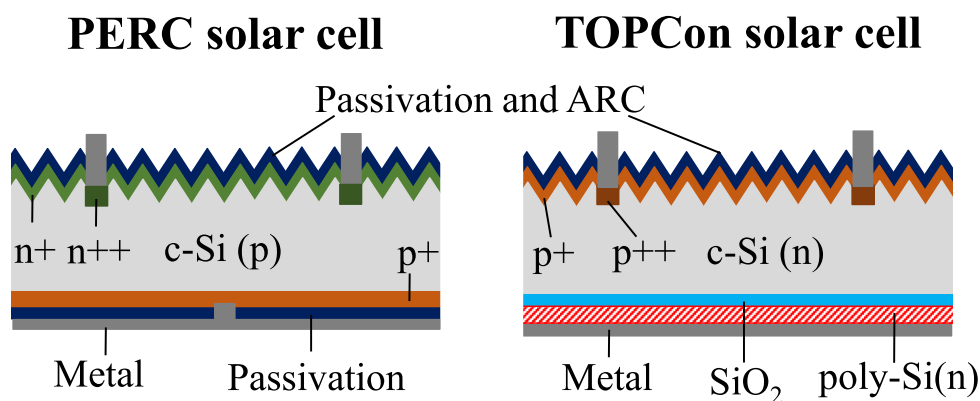


Fig. 1. Schematic illustrations of basic structures of PERC and TOPCon solar cells.

structures,^{26–31)} but the patterning is an obstacle to reducing the cost of TOPCon-IBC solar cells. One of the solutions is to use ion implantation. Generally, mass-separated beamline ion implantation systems are used in integrated circuit manufacturing processes, but this type of system requires a huge footprint and the system cost is very high. In addition, the small beam diameter requires beam scanning during implantation, which leads to low throughput in the mass production process of solar cells. Therefore, we employed a plasma immersion ion implantation (PIII) system.³²⁾ The PIII system can realize high-throughput ion implantation by using a large-area extraction electrode and without using a mass separation system. This leads to a cost reduction of the ion implantation process. ULVAC, Inc. (Kanagawa, Japan) has been conducting research on ion implantation processes using mechanical hard masks since around 2000,^{33–35)} and has supplied commercially available PIII systems equipped with mechanical hard masks for solar cell manufacturing. By applying the ion implantation technique using the PIII system and mechanical hard mask, a cost reduction of the TOPCon-IBC solar cell manufacturing process is expected.

As mentioned above, the application of FTS and the PIII system to the fabrication process of TOPCon solar cells has the potential to improve the safety of the production line and reduce the production cost. However, the feasibility of the TOPCon solar cell fabrication process, including the combination of amorphous silicon deposited by FTS and ion implantation using the PIII system, has not been investigated. Therefore, we investigate the fabrication and properties of TOPCon structures using highly phosphorus-doped poly-Si in this study.

2. Experimental methods

The sample fabrication and characterization sequence is shown in the flowchart in Fig. 2. A float-zone double-side polished n-type monocrystalline silicon (100) wafer with a thickness of 280 μm and a resistivity of about 3 $\Omega\text{ cm}$ was used in this study. A 4 inch wafer cut into quarters was used for sample fabrication. The wafer was dipped in 1% hydrofluoric acid for about 60 s to remove the native oxide on the surface. Nitric acid oxidation using nitric acid at a concentration of 15.7 mol l^{-1} was performed at 100 $^{\circ}\text{C}$ for 10 min. This process produced approximately 1.5 nm thick SiO_2 on the surface of the c-Si wafer. The thickness of the SiO_2 layer was measured by spectroscopic ellipsometry.

Subsequently, a hydrogenated amorphous silicon (i-a-Si:H) layer was deposited on both sides of the wafer at RT by DC-superimposed RF FTS using a two-step deposition method. Details of the i-a-Si:H deposition by FTS were reported elsewhere.¹⁸⁾ As mentioned in the Results and Discussion section, the use of i-a-Si:H leads to a large surface roughness. Therefore, we also applied unhydrogenated amorphous silicon (i-a-Si) for the TOPCon structure. We used argon (Ar) and hydrogen (H_2) mixture ($\text{Ar}/\text{H}_2 = 30/1.2$ sccm) for i-a-Si:H deposition, and only Ar (30 sccm) was used for i-a-Si deposition. The sputtering targets were n-type monocrystalline silicon with a resistivity in the range of 57 to 75 $\Omega\text{ cm}$. The first layer was deposited at a RF/DC power of 300/56 W for 5 s and the second layer was deposited at a RF/DC power of 600/56 W for 400 s. The thickness of the i-a-Si was about 90 nm. We also deposited i-a-Si:H layers on one side of a quartz substrate to confirm the crystallization and to investigate the electrical properties.

After the deposition of i-a-Si, phosphorus implantation by the PIII system was performed at RT. The source of the phosphorus was phosphine (PH_3), and the acceleration voltage was 5 keV. We changed the implantation dose from 3×10^{15} to $1 \times 10^{16} \text{ cm}^{-2}$ to investigate the effect of the dose on the electrical and passivation quality. After the implantation for both sides, the samples were annealed at 850 $^{\circ}\text{C}$ –1000 $^{\circ}\text{C}$ for 30 min in a nitrogen (N_2) atmosphere to crystallize the phosphorus implanted amorphous silicon. After the annealing, the amorphous silicon was crystallized and the poly-Si layer was formed.

It is well known that the hydrogenation process is very important to improve the passivation quality of the TOPCon structure. For this purpose, we deposited 10 nm thick aluminum oxide (Al_2O_3) on both sides of the sample by thermal atomic layer deposition using trimethylaluminum and water vapor at 150 $^{\circ}\text{C}$. The Al_2O_3 layer contains a large amount of hydrogen due to the relatively low temperature deposition; therefore, the hydrogen in the Al_2O_3 layer can diffuse into the poly-Si layer during subsequent forming gas annealing (FGA) above 450 $^{\circ}\text{C}$. We investigated the effect of the annealing temperature on hydrogenation by changing the annealing temperature from 450 $^{\circ}\text{C}$ to 550 $^{\circ}\text{C}$ for 10 min.

For a selected sample, we investigated the carrier transport through the TOPCon structure. Before the hydrogenation process using Al_2O_3 deposition and FGA, we cut a small piece of the sample and deposited aluminum electrodes on

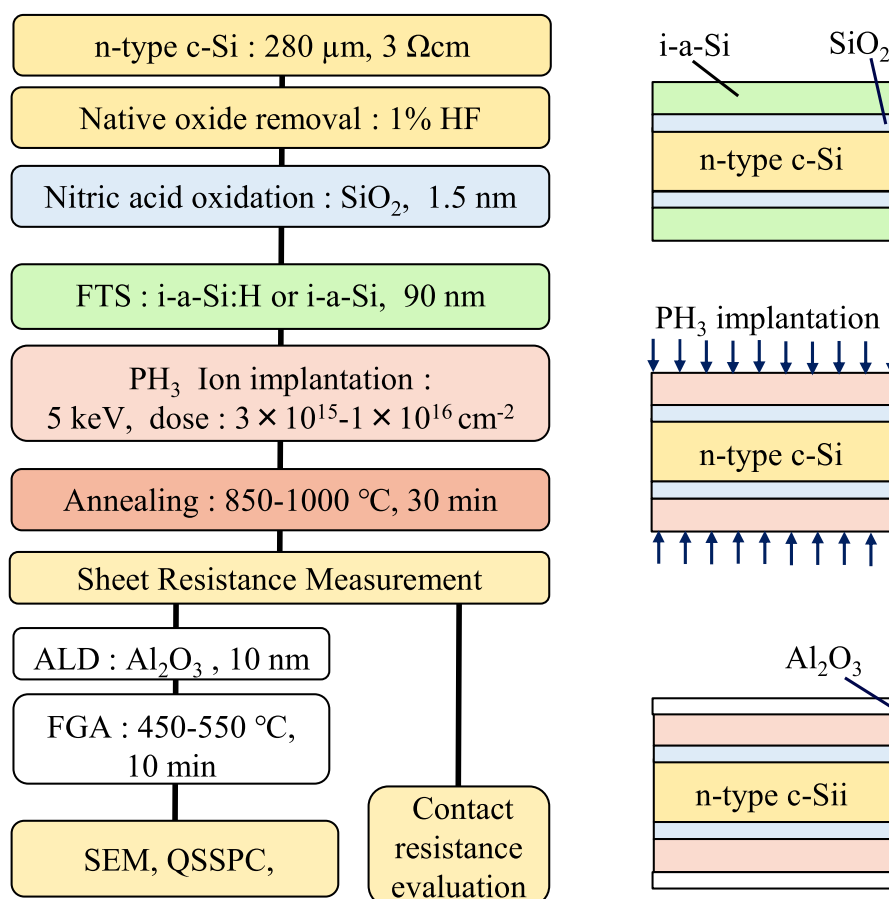


Fig. 2. Process flow of TOPCon structures fabricated using FTS and PIII systems.

both sides of the sample. After annealing to improve the contact, the Cox–Strack method³⁶⁾ was applied to evaluate the contact resistance of the sample.

3. Results and discussion

Before characterization of the TOPCon structure, we investigated the structural and electrical properties of highly phosphorus-doped poly-Si layers fabricated on quartz substrate. Figure 3 shows the Raman scattering spectra of the samples fabricated with different implantation doses. The peak located at about 520 cm^{-1} corresponds to the c-Si TO phonon mode,³⁷⁾ indicating that all samples were crystallized. This peak is very similar to the reference spectrum obtained from highly phosphorus-doped poly-Si fabricated from thermal annealing of phosphorus-doped i-a-Si:H deposited by PECVD. We also clearly observed a reduction of the peak intensity for the sample with a dose of $3 \times 10^{16} \text{ cm}^{-2}$. This clearly indicates that an excess amount of phosphorus implantation suppresses the crystallization of i-a-Si:H. This suggests that a large number of defects related to the non-activated phosphorus are generated in the sample with a dose of $3 \times 10^{16} \text{ cm}^{-2}$. This leads to a deterioration of the passivation quality. Therefore, it is important to use a dose less than $2 \times 10^{16} \text{ cm}^{-2}$ to realize high-quality highly phosphorus-doped poly-Si. We also investigated the effect of the annealing temperature on the crystallization. The crystallinity of the samples increased with the increasing annealing temperature. Sufficient crystallinity was obtained at annealing temperatures above 900 $^\circ\text{C}$. Table I shows a summary of the electrical properties. We investigated the

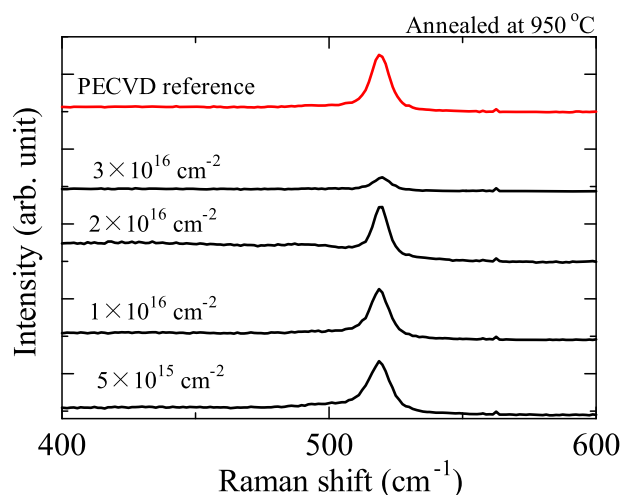


Fig. 3. Raman scattering spectra of highly phosphorus-doped poly-Si layers fabricated from i-a-Si:H layers implanted with different ion doses. The annealing temperature of the samples was 950 $^\circ\text{C}$. The spectra of the highly phosphorus-doped poly-Si layer fabricated from highly phosphorus-doped a-Si:H deposited by PECVD are also shown as a reference.

effect of the implantation dose and annealing temperature. The electrical conductivity is strongly influenced by the annealing temperature. A higher annealing temperature leads to a higher conductivity. The implantation dose also has a big impact on the electrical conductivity. A high conductivity of above 200 S cm^{-1} was obtained when the dose was larger than $1 \times 10^{16} \text{ cm}^{-2}$. With the exception of the sample fabricated with the dose of $5 \times 10^{15} \text{ cm}^{-2}$, the samples

Table I. Electrical properties of highly phosphorus-doped poly-Si layers on quartz substrates fabricated with i-a-Si:H deposited by FTS and ion implantation by PIII. The electrical properties of the highly phosphorus-doped poly-Si layer fabricated from highly phosphorus-doped a-Si:H deposited by PECVD is also shown as a reference.

Dose (cm ⁻²)	Annealing temperature (°C)	Conductivity (S cm ⁻¹)	Carrier density (cm ⁻³)
5×10^{15}	950	6.60×10^1	3.7×10^{19}
1×10^{16}	900	1.38×10^2	1.3×10^{20}
1×10^{16}	950	2.40×10^2	1.2×10^{20}
1×10^{16}	1000	3.60×10^2	3.5×10^{20}
2×10^{16}	950	2.86×10^2	1.9×10^{20}
3×10^{16}	950	3.08×10^2	1.6×10^{20}
PECVD reference	950	1.56×10^3	1.2×10^{21}

showed a sufficiently high electron density of about $1\text{--}2 \times 10^{20} \text{ cm}^{-3}$, and this value is an acceptable level for the application of the TOPCon structure. Compared with the PECVD reference sample, our poly-Si samples fabricated by the combination of FTS and ion implantation showed about one order of magnitude lower conductivity. To further improve the conductivity, we need to optimize the i-a-Si:H deposition conditions as well as the annealing conditions.

We applied these highly phosphorus-doped poly-Si layers to the TOPCon structure. However, the TOPCon structure fabricated with i-a-Si:H shows a very large surface roughness and partial peeling of the film. Figure 4(a) shows a scanning electron microscope (SEM) image of the surface of a TOPCon sample fabricated with i-a-Si:H. Many micrometer-size bubble-like structures are observed on the surface. This hydrogen-induced blistering was reported in previous studies.^{38–41)} To improve this problem, we fabricated a TOPCon structure using i-a-Si. The SEM image of the surface of the TOPCon structure fabricated with i-a-Si is shown in Fig. 4(b). Suppression of the blistering was clearly observed. In our PIII process, all ions generated from PH₃ (PH₃⁺, PH₂⁺, PH⁺, P⁺, H⁺) were implanted to the i-a-Si layer, but the dominant ions generated in our PIII system were PH₃⁺ and PH₂⁺ because an RF power source with a frequency of 13.56 MHz was employed to generate the plasma. The amount of H⁺ ions is expected to be about 5% of the total implanted ions. For an acceleration voltage of

5 keV, H⁺ can be implanted deep into the i-a-Si layer, but this small amount of hydrogen in the i-a-Si layer does not contribute to the blistering. Hydrogen was also implanted in the i-a-Si layer by PH₃⁺ and PH₂⁺ ions. The hydrogen originating in these ions was implanted only near the surface of the i-a-Si. The hydrogen near the surface can easily escape from the i-a-Si layer during thermal annealing. This is the reason why blistering was suppressed even when our PIII process implanted all the ions generated from PH₃. As mentioned later, the blistering deteriorated the surface passivation quality of the TOPCon structure. Therefore, we employed i-a-Si for detailed characterization of the TOPCon structure.

Figure 5(a) shows the dependence of the sheet resistances of the TOPCon structures on the annealing temperature. We can estimate the sheet resistance of the TOPCon structures fabricated with i-a-Si:H from the conductivity of the poly-Si layer shown in Table I, the thickness of the poly-Si layer and the sheet resistance of the wafer. The estimated sheet resistances for 900 °C, 950 °C, and 1000 °C annealing are 82.7, 74.9, and 64.1 Ω sq⁻¹, respectively. At the annealing temperature of 900 °C, the estimated sheet resistance is almost the same as the measured value; however, the measured sheet resistance is lower than the estimated value when the annealing temperature is higher than 950 °C. This clearly indicates that phosphorus diffusion into the wafer is not negligible for an annealing temperature higher than 950 °C. This was also confirmed by secondary ion mass spectroscopy (SIMS), as shown in Fig. 6. In addition, the sheet resistance of the TOPCon structures fabricated with i-a-Si also showed a similar tendency. The SIMS results indicate the existence of a phosphorus-rich region (10–20 nm) near the surface. Our SIMS measurements also revealed a small silicon concentration and large oxygen concentration at a depth of 10–15 nm (data not shown). Therefore, this region is considered to be phosphorus oxide with a small amount of silicon, which was formed by oxidation of the phosphorus layer. Our preliminary experiments demonstrated that an approximately 2 nm thick phosphorus layer was formed on the surface. Therefore, the above-mentioned phosphorus oxide layer was probably formed by the reaction of the phosphorus layer with water vapor in the atmosphere during the sample transfer from the PIII system to the annealing furnace. As shown in Fig. 6, the phosphorus concentration in this phosphorus-rich region

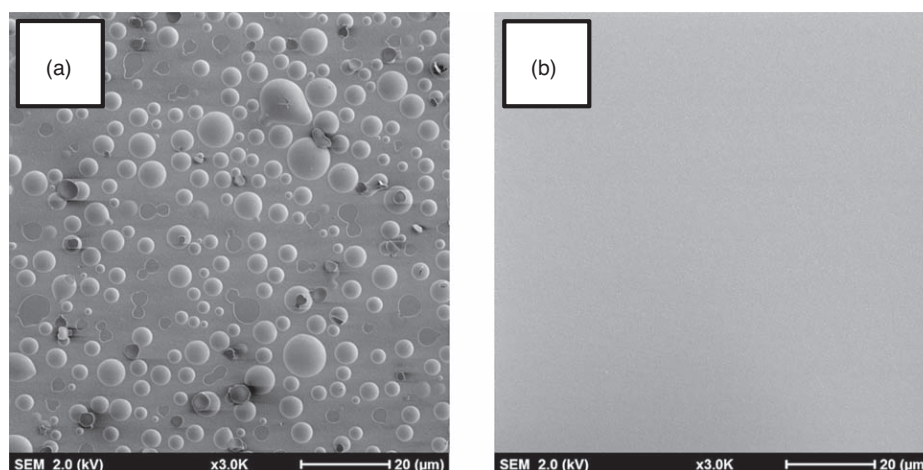


Fig. 4. Surface SEM images of TOPCon structure fabricated using (a) i-a-Si:H and (b) i-a-Si. For both samples, the implantation dose and annealing temperature were $1 \times 10^{16} \text{ cm}^{-2}$ and 950 °C, respectively.

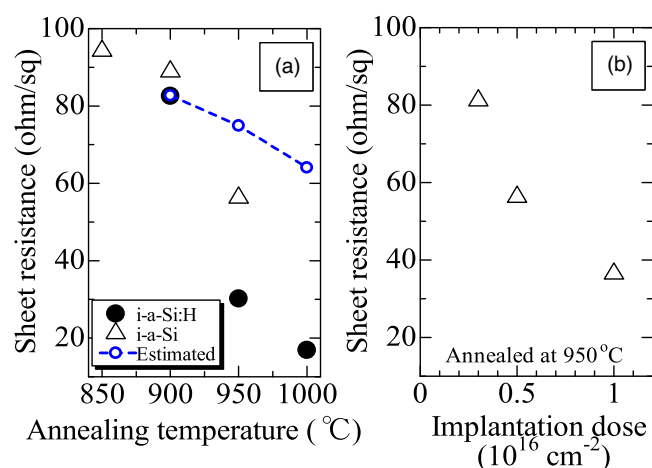


Fig. 5. Dependence of sheet resistances of TOPCon structures on (a) annealing temperature, and (b) implantation dose. For the annealing temperature dependence, TOPCon structures fabricated with i-a-Si:H (dose: $1 \times 10^{16} \text{ cm}^{-2}$) and i-a-Si (dose: $5 \times 10^{15} \text{ cm}^{-2}$) were used. The data indicated with “Estimated” is the estimated sheet resistance from the conductivity data shown in Table I. For the dose dependence, only TOPCon structures fabricated with i-a-Si were used.

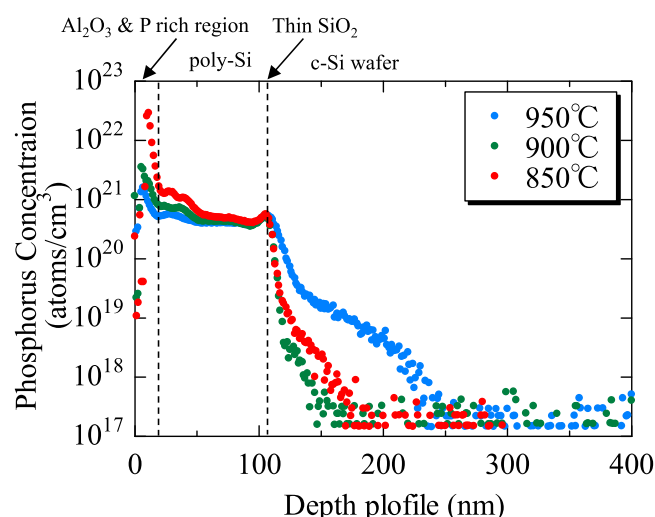


Fig. 6. SIMS depth profile of phosphorus in the TOPCon structures fabricated with i-a-Si. The implantation dose of $5 \times 10^{15} \text{ cm}^{-2}$ is the same for all samples.

decreased with the increasing annealing temperature. This is probably due to the out-diffusion during the annealing process. The SIMS results also indicate the existence of a high concentration of phosphorus, oxygen and silicon at a depth of 15–20 nm. This layer is a slightly oxidized phosphorus-rich silicon layer, which was probably formed during thermal annealing due to the residual oxygen in the furnace or oxygen in the above-mentioned phosphorus oxide layer. In the poly-Si region (20–110 nm), there is a slightly phosphorus-rich region (20–40 nm), indicating that phosphorus atoms were implanted only in this region during the ion implantation process. We performed a simulation of the depth profile of the implanted ions using the stopping and range of ions in matter (SRIM) simulation.⁴²⁾ The depth of phosphorus implantation estimated by the SRIM simulation software was very similar to the depth of the above-mentioned slightly higher phosphorus concentration region in the SIMS measurement. The SIMS profiles also show that phosphorus sufficiently diffused into the poly-Si during

annealing at 850 °C. It should be noted that a small amount of phosphorus diffusion into the c-Si wafer was observed for the annealing at 850 °C and 900 °C. Slightly deeper phosphorus diffusion was observed for the annealing at 850 °C. This counterintuitive behavior of phosphorus diffusion is probably due to the phosphorus concentration in the phosphorus-rich region (10–20 nm). As mentioned above, the phosphorus concentration in the phosphorus-rich region decreased when increasing the annealing temperature due to the out-diffusion of phosphorus. The phosphorus in this phosphorus-rich region is expected to act as a phosphorus source for the phosphorus diffusion during the annealing, and this phosphorus source concentration was higher for the 850 °C annealing. This is the reason why the phosphorus diffusion into the c-Si wafer is slightly higher for the 850 °C annealing compared to the 900 °C annealing. The enhancement of phosphorus diffusion by using a higher-concentration phosphorus source was previously reported.²⁰⁾ The SIMS measurement clearly indicates that there is a small amount of phosphorus diffusion into the c-Si wafer even when the annealing temperature is below 900 °C, but our sheet resistance measurement also revealed that this small amount of phosphorus diffusion for annealing temperatures below 900 °C has a negligible effect on the sheet resistance of the TOPCon structures.

We also investigated the effect of the implantation dose on the sheet resistance of TOPCon structures fabricated with i-a-Si. The sheet resistance of the TOPCon structures can also be controlled by the implantation dose. The results indicate that the sufficiently low sheet resistance (less than 100–150 ohm sq^{-1} for a bifacial TOPCon solar cell)^{43–45)} can be obtained by controlling the annealing temperature and the implantation dose regardless of the amorphous silicon layer (i-a-Si:H or i-a-Si) used for fabricating the TOPCon structures. When the TOPCon structure is used for bifacial-type silicon solar cells, the sheet resistance should be at the same level as that of a standard emitter layer (100–150 ohm sq^{-1}) because a grid electrode is formed as well as the emitter side. When the TOPCon structure is applied to the bottom cell of a silicon-based tandem solar cell⁴⁾ with a monofacial-type structure or TOPCon-IBC solar cell, a sheet resistance much higher than 100–150 ohm sq^{-1} can be used since most of the n-type poly-Si region is covered with a metal electrode. For all solar cell structures, the n-type poly-Si layer is required to have sufficiently high carrier concentration to form a good electrical contact with the metal electrode. The sheet resistance obtained in our study is of an acceptable level because the sheet resistance of about 80 ohm sq^{-1} as shown in Fig. 5(b) is sufficiently lower than the target value of 100–150 ohm sq^{-1} for the bifacial-type silicon solar cell with TOPCon structure.

To investigate the surface passivation quality, we measured the effective carrier lifetime (τ_{eff}) of the TOPCon structures. At the beginning, we measured the τ_{eff} of the TOPCon structure fabricated with i-a-Si:H; however, we obtained a relatively small τ_{eff} of 0.61 ms (annealing temperature: 950 °C, dose: $1 \times 10^{16} \text{ cm}^{-2}$, before hydrogenation process). This is due to the blistering, as mentioned in Fig. 4(a). For the TOPCon structure using i-a-Si, we obtained a τ_{eff} of 1.1 ms (annealing temperature: 950°C, dose: $1 \times 10^{16} \text{ cm}^{-2}$, before hydrogenation process). Therefore, we focused on the characterization of the TOPCon structure fabricated with i-a-Si. Figure 7 shows the dependence of

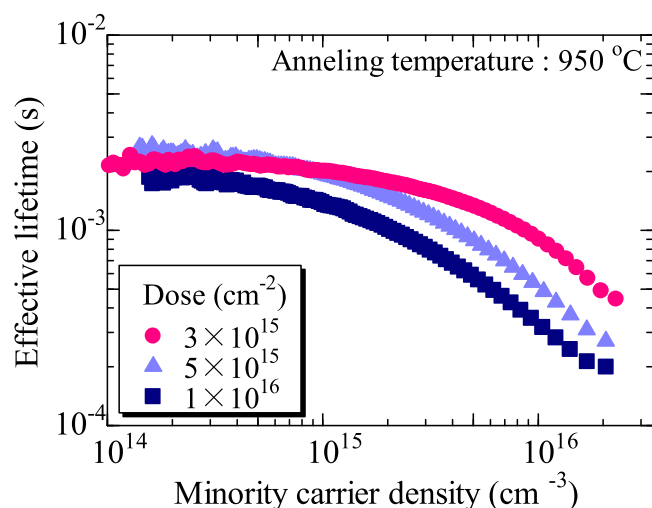


Fig. 7. Dependence of τ_{eff} on minority carrier density of the TOPCon structures fabricated using different implantation doses.

τ_{eff} on the minority carrier density measured by quasi-steady-state photoconductance. For this measurement, we applied the hydrogenation process for the TOPCon structures. For a small minority carrier density, τ_{eff} showed a similar value regardless of the implantation dose. However, τ_{eff} for a high minority carrier density is strongly influenced by the implantation dose. The smaller dose samples show a higher τ_{eff} . As mentioned in the previous part related to Figs. 5 and 6, non-negligible phosphorus diffusion into the wafer was observed at the annealing temperature of 950 °C. The SIMS depth profile shown in Fig. 6 indicates that there is an approximately 90 nm thick phosphorus diffusion region (P concentration $> 3 \times 10^{18} \text{ cm}^{-3}$) for the sample with a $5 \times 10^{15} \text{ cm}^{-2}$ implantation dose annealed at 950°C. The phosphorus diffusion region has the back-surface field (BSF) effect, but this region is a small minority carrier lifetime region. The potential barrier for holes formed by the phosphorus diffusion region is expected to be about 0.2 eV by considering the doping density of the c-Si wafer. At high minority carrier densities, electrons accumulate in the phosphorus diffusion layer side and the potential barrier for holes decreases, resulting in a reduction of the BSF effect. Therefore, holes can diffuse into the phosphorus diffusion region and recombine with electrons. In addition, a higher dose leads to a smaller sheet resistance, as shown in Fig. 5(b). This suggests that a higher dose leads to more phosphorus diffusion into the c-Si wafer. This is the reason for the small τ_{eff} at a high minority carrier density for the samples fabricated under higher dose conditions.

Figure 8 summarizes τ_{eff} at the minority carrier density of 10^{15} cm^{-3} and the implied open circuit voltage ($i\text{-}V_{\text{oc}}$) under 1 Sun conditions. It is clear that smaller dose conditions show a better passivation quality. A relatively high τ_{eff} of 2.01 ms and $i\text{-}V_{\text{oc}}$ of 704 mV were obtained at an annealing temperature of 950 °C and an implantation dose of $3 \times 10^{15} \text{ cm}^{-2}$. The τ_{eff} and $i\text{-}V_{\text{oc}}$ obtained in this study were found to be slightly inferior to those reported in previous studies^{20,46)} of TOPCon structures using LPCVD and PECVD amorphous silicon. The main reasons for our slightly smaller τ_{eff} are the differences in the annealing temperature and hydrogenation process. In the above-mentioned publication, an annealing

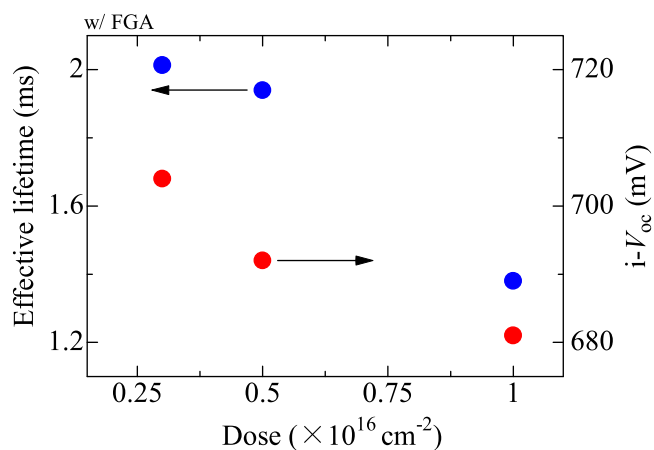


Fig. 8. Dependence of τ_{eff} at a minority carrier density of 10^{15} cm^{-3} and $i\text{-}V_{\text{oc}}$ (under 1 Sun) on the implantation dose. These values are extracted from the data shown in Fig. 7.

temperature of around 900 °C and remote-plasma hydrogenation were employed. It is known that the degradation of the SiO_2 layer produced by nitric acid oxidation starts at 950 °C. As mentioned above, a significant amount of phosphorus diffusion into the c-Si wafer was observed in our samples. In addition, our hydrogenation process has not yet been optimized. Therefore, the passivation effect is expected to be further improved by optimizing the annealing temperature and the hydrogenation process.

The contact resistance of the TOPCon structure fabricated with i-a-Si (annealing temperature: 950 °C, dose: $5 \times 10^{15} \text{ cm}^{-2}$, before hydrogenation process) was estimated using the Cox–Strack method. In the Cox–Strack method, the resistance of the vertical structure as shown in the inset of Fig. 9 was measured for electrodes with different sizes. By analyzing the relationship between the electrode size and the resistance by considering the spread resistance, we can obtain the contact resistance. Figure 9 shows the current–voltage ($I\text{-}V$) characteristics of the vertical direction for different electrode sizes. All the $I\text{-}V$ curves show very good ohmic

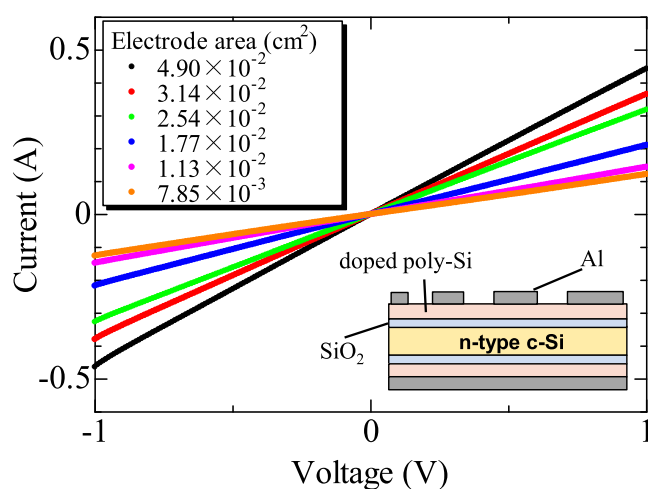


Fig. 9. $I\text{-}V$ characteristics of the TOPCon structure fabricated with i-a-Si. The implantation dose and annealing temperature were $5 \times 10^{15} \text{ cm}^{-2}$ and 950 °C, respectively. The $I\text{-}V$ measurements were performed using top and bottom electrodes (vertical direction). The top electrodes with different electrode sizes were used to analyze contact resistance.

characteristics. The extracted contact resistance was $3.22 \times 10^{-3} \Omega \text{ cm}^2$, which is small enough for device application.

Finally, we would like to discuss the potential of the combination of i-a-Si deposited by FTS and ion implantation by the PIII system. As mentioned before, the passivation quality of our TOPCon structure is still slightly inferior to the TOPCon structure fabricated using LPCVD and PECVD. However, there is room for improvement of the passivation quality by optimizing the annealing condition for the i-a-Si crystallization and hydrogenation process. Detailed optimization of the ion implantation conditions will also contribute to further improvement of the passivation quality. Therefore, there is potential for the application of our new process from the viewpoint of passivation quality. In this paper, we only investigated the TOPCon structure using n-type poly-Si, but one of the authors, Yamaguchi, already investigated the boron ion implantation to LPCVD poly-Si using the PIII system and found that a similar level of passivation quality to the TOPCon structure using a highly phosphorus-doped poly-Si layer was obtained from the p-type poly-Si/SiO₂/n-type c-Si wafer/SiO₂/p-type poly-Si structure.³⁵⁾ In addition, the selective ion implantation process using a hard mask in the PIII system was also reported.⁴⁷⁾ Further investigation of the passivation quality of p-type poly-Si/SiO₂/n-type c-Si wafer/SiO₂/p-type poly-Si structure fabricated with i-a-Si deposited by FTS and boron implantation by the PIII system is required, but there is a possibility of applying our process to fabricate TOPCon-IBC solar cells. From the viewpoint of productivity, the throughput of the process is important. The deposition rates of i-a-Si by FTS, poly-Si by LPCVD, and doped amorphous silicon by PECVD are about 13 nm min^{-1} , $1\text{--}5 \text{ nm min}^{-1}$ ⁴⁸⁾ and 90 nm min^{-1} ¹³⁾, respectively. The deposition rate of LPCVD poly-Si is lower than the others, but multiple wafers (>1000 wafers per tube) can be processed simultaneously, leading to high throughput. Therefore, further improvement of the deposition rate of i-a-Si deposited by FTS is required for the industrial application of our process. At present, the deposition rate of about 13 nm min^{-1} for i-a-Si deposited by FTS is limited by the maximum output power of our RF power source. Therefore, the improvement of the deposition rate of i-a-Si is basically possible, and intensive efforts to improve the deposition rate are also important in future studies.

4. Conclusions

We evaluated the basic properties of TOPCon structures fabricated using FTS and PIII systems to realize a SiH₄-free process and more precise doping control and doping area patterning. The sheet resistance analysis indicates that the sheet resistance can be controlled by the implantation dose and annealing temperature. A sufficiently high electron density was obtained from the thermally crystallized phosphorus implanted i-a-Si:H deposited by FTS, but there is still room for improvement of the conductivity. We also found that it is important to use i-a-Si (unhydrogenated) to avoid the blistering problem during thermal crystallization. This is a key factor to obtaining high-quality passivation. At present, the best sample showed a τ_{eff} of 2.01 ms at a minority carrier density of 10^{15} cm^{-3} and i-Voc of 704 mV under 1 Sun conditions. A sufficiently small contact resistance of $3.22 \times 10^{-3} \Omega \text{ cm}^2$ was also confirmed. From the viewpoint of the passivation quality, our current results are slightly inferior to the TOPCon structures fabricated by the standard process. However, there is still room for the

optimization of various parameters, such as the annealing temperature, implantation dose and i-a-Si sputtering condition.

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