

CHARGES AND DEFECTS IN SiO_2 FILMS DEPOSITED BY PLASMA-ENHANCED CHEMICAL VAPOR DEPOSITION AT LOW TEMPERATURES

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Abstract—Charges and defects in SiO_2 films deposited by plasma-enhanced chemical vapor deposition (PECVD) have been studied. The SiO_2 films were used to form MOS (aluminum- SiO_2 - n -type silicon) devices. After the devices were annealed in a forming gas at 400°C for 30 min, the oxide fixed charge Q_f measured using the capacitance-voltage (C - V) method was in the low $10^{10} \text{ q cm}^{-2}$, and the mobile ion charge Q_m measured using the bias-temperature aging test in conjunction with the C - V method was also in the low $10^{10} \text{ q cm}^{-2}$. Both Q_f and Q_m are practically independent of substrate deposition temperature for the temperature range of 225 – 350°C used in this investigation. The midgap interface trap density D_{it} and the oxide trapped charge Q_{ot} have also been measured using the high-low frequency C - V method with the devices annealed at various temperatures for a fixed anneal time or at various anneal times for a fixed anneal temperature. The value of D_{it} is of the order of $10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$. The SiO_2 film consists of positive and negative oxide trapped charges which are of the order of $10^{17} \text{ q cm}^{-3}$ prior to post metallization anneal (PMA) at 400°C . The anneal chemistry of the defects in PECVD SiO_2 films is compared with that in thermal SiO_2 .

1. INTRODUCTION

Several investigators[1–4] have recently reported that high quality SiO_2 films can be produced by plasma-enhanced chemical vapor deposition (PECVD) at a temperature around 300°C , and that after a post-metallization anneal (PMA) at 400°C the films exhibit good physical properties and electrical integrity which are close to those for high quality thermal oxides fabricated at 1000°C in dry oxygen. Much effort has been devoted to improve the electrical integrity by optimizing the deposition parameters such as gas pressure, gas composition, power transfer, substrate surface cleanliness, etc. However, little has been reported on the annealing kinetics of various defects and the behavior of various charges in PECVD SiO_2 films. Griscom[5], Plummer *et al.*[6], and Reed and Plummer[7] have studied various charges and defects in MOS devices through the analysis of the annealing chemistry but the SiO_2 in the devices for their studies were either thermal oxides or silica whose defect structure and content might be very different from PECVD oxides. The purpose of this paper is to report our recent study on the annealing kinetics of charges and defects in PECVD SiO_2 deposited at substrate temperatures in the range of 225 – 350°C .

2. EXPERIMENTAL

The SiO_2 films used for this investigation were deposited by a modified radio frequency (13.56 MHz)

PECVD process at six different substrate temperatures using a gas mixture of 2% SiH_4 in He and pure N_2O at the IBM Thomas J. Watson Research Center[2]. The details of the deposition process have been reported earlier[1,2]. The substrates were n -type silicon wafers of resistivity 1 – $2 \Omega\text{-cm}$. One hundred aluminum counter electrodes of 0.025 cm^2 in area each were vacuum-deposited through a shadow mask to form MOS capacitors, the oxide thickness being 500 – $600 \text{ \AA}$. All measurements were made at room temperature before and after the devices had been subjected to post metallization anneal (PMA) at 400°C in a forming gas (10% H_2 in N_2) for 30 min. After the back oxide was removed, indium gallium paste was used to make electrical contacts to the silicon substrate.

The high frequency (1 MHz) capacitance-voltage (C - V) and the quasi-static C - V characteristics were measured using a linear voltage ramp with the ramp rate of 50 mV s^{-1} . For the measurements at negative gate polarity (depletion mode for n -Si) the MOS capacitor was illuminated with light to avoid deep depletion.

3. RESULTS AND DISCUSSION

A. The oxide fixed charge

Since the interface trapped charge and the oxide trapped charge would be removed after a low temperature PMA, the net charge inside the MOS device

after PMA can be considered to be mainly the oxide fixed charge Q_f which can be determined by

$$Q_f = \frac{\epsilon_{ox}(V_{fb} - \phi_{ms}/q)}{d} \quad (1)$$

where V_{fb} is the flatband voltage corresponding to the voltage required to make the band edge of n -Si flat to the SiO_2 -Si interface, ϕ_{ms} is the work function difference between the gate metal work function and the n -Si work function, q is the electronic charge, and ϵ_{ox} and d are, respectively, the permittivity and the thickness of the oxide.

To determine Q_f , we have to know V_{fb} and ϕ_{ms} which can be obtained from the high frequency C - V characteristics for the MOS devices before and after PMA with the SiO_2 deposited at substrate temperatures of 250°C and 350°C are shown in Fig. 1. From these characteristics we obtain the oxide capacitance C_{ox} , the minimum capacitance of the device C_{min} , and the flatband capacitance C_{fb} . With these known parameters we can easily calculate the donor concentration in n -Si, N_d , the thickness d and ϕ_{ms} using standard relations[8,9]. V_{fb} is the parallel shift of the C - V curve. The results of Q_f calculated from eqn (1) show that the oxide fixed charge density is in the low $10^{10} \text{ q cm}^{-2}$ and is practically independent of the substrate temperature for the substrate temperature range under this investigation. It is interesting to note

that Q_f for the thermal oxide depends strongly on the oxidation temperature[10] while Q_f in our PECVD oxide is practically independent of the substrate deposition temperature. If the ionic silicon resulting from the incomplete oxidation at the interface is the major source for Q_f [10], these results indicate that our PECVD oxide should contain little unoxidized silicon at the interface.

B. The mobile ionic charge

Using the method[11] commonly used for the determination of mobile ionic charge, we have measured the mobile ionic charge in our MOS devices. With this method a high frequency C - V characteristic of an MOS device after PMA is first measured, and then this device is heated to about 150°C to mobilize the ions and at the same time a bias of 8 V corresponding to about 1.5 MV cm^{-1} across the oxide is applied to the gate for about 30 min in order to drive all of the ions either to the SiO_2 -Si interface when the bias is positive, or to the SiO_2 -metal interface when the gate is negative. After this bias temperature aging (BTA), the device is then cooled down to the room temperature before the measurement of its C - V characteristic. The parallel shift of this C - V characteristic from that before BTA is the measure of the mobile ions drifted to the interfaces forming a charge sheet there with a density Q_m given by

$$Q_m = (V'_{fb} - V_{fb})C_{ox} \quad (2)$$

where V_{fb} and V'_{fb} are, respectively, the flatband voltages before and after BTA. Typical results are shown in Fig. 2. In general, the flatband shift is small showing that our PECVD SiO_2 films contain mobile ions in the order of $4 \times 10^{10} \text{ cm}^{-2}$. Curve 1 (prior to BTA (and curve 3 (after BTA with a positive gate bias) are almost identical indicating that the ions are of ionized alkali atoms such as sodium and potassium, and of positive charge; and that they do not

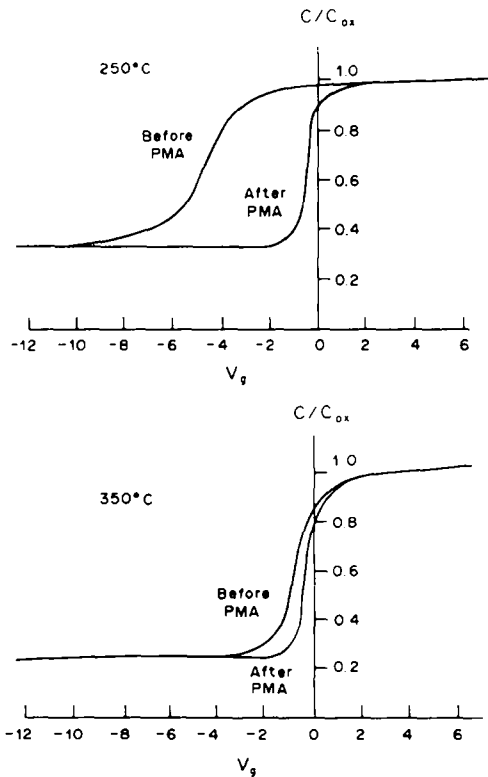


Fig. 1. Typical high frequency C - V characteristics of the PECVD SiO_2 films before and after PMA, deposited at 250°C and at 350°C .

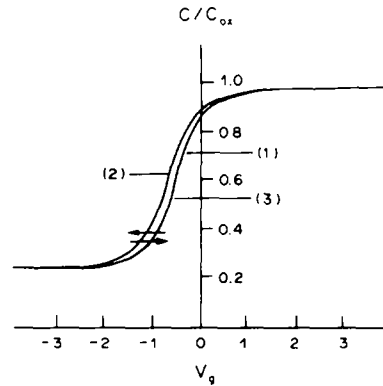


Fig. 2. The shift of the high frequency C - V curve after bias-temperature aging (BTA) for the PECVD SiO_2 deposited at 300°C . Curve (1): the initial C - V prior to BTA, curve (2): the C - V curve after BTA at 150°C and +8 V bias for 30 min, and curve (3): the C - V curve after BTA at 150°C and -8 V bias for 30 min.

exchange charge with either the gate metal or the silicon and do not become discharged even though they pile up to within a tunneling distance at the interfaces. Again, Q_m is practically independent of the substrate deposition temperature for the temperature range of 225–350°C, because the origin of such ions is mainly due to the contamination during fabrication processing such as gate or contact metallization and general handling of the substrate cleaning process, etc.

C. The interface trap density

We have found that the oxide fixed charge and the mobile ionic charge densities are small in our PECVD devices. Therefore, the shift of the C - V curves before and after PMA as shown in Fig. 1 can be considered to be mainly due to the interface trap density D_{it} and the oxide trapped charge density Q_{ot} . It is thus interesting to investigate how fast and how much these charges can be annealed out at a fixed annealing temperature and a fixed anneal time.

The high frequency and the quasi static C - V characteristics (normalized to the oxide capacitance) as shown in Fig. 3 can be used to evaluate D_{it} as a function of the gate bias V_g according to the following relation[9].

$$D_{it} = \frac{C_{ox} V_g}{q} \left[\left(\frac{C_{ox}}{C_{LF}} - 1 \right)^{-1} - \left(\frac{C_{ox}}{C_{HF}} - 1 \right)^{-1} \right] \quad (3)$$

where C_{HF} and C_{LF} denote the high frequency and the low frequency (quasi static) capacitances, respectively. Normally, we want to see D_{it} as a function of energy level in the interface band gap. To convert D_{it} as a function of V_g to D_{it} as a function of $E_c - E$, we use the following relations[8]

$$E_c - E = \frac{E_g}{2} + \psi_s - \phi_b \quad (4)$$

$$\psi_s = \int_{V_b}^{V_g} (C_{ox} - C_{LF}) dV \quad (5)$$

where E_c is the conduction band edge energy, E_g is the band gap energy, E is the energy level in the gap, ϕ_b is the difference between the thermal equilibrium Fermi level and the intrinsic Fermi level in the silicon bulk, ψ_s is the surface potential energy at the SiO₂-Si interface. Using an IBM computer program, we have computed and plotted D_{it} as a function of $(E_c - E)$ based on eqns (3)–(5), and from this plot we have determined the mid-gap D_{it} which is the value of D_{it} at 0.55 eV below E_c (the mid-gap based on $E_g = 1.1$ eV for Si at room temperature).

To study the anneal mechanism, we annealed our PECVD devices in two ways. The first way was that the devices were annealed at different temperatures, namely, 225, 250, 275, 300, 325 and 350°C with a fixed anneal time of 30 min. The second way was that the devices were annealed at a fixed temperature of 400°C but with different anneal times, namely, 10, 30,

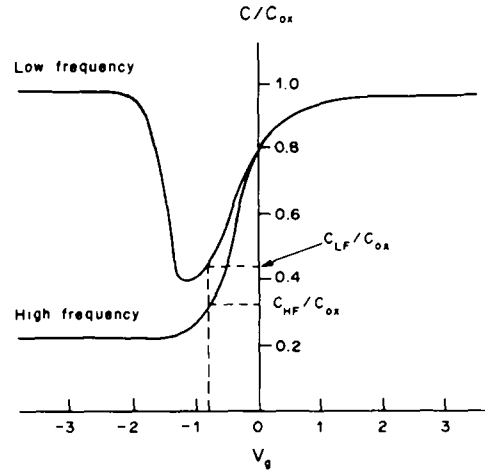
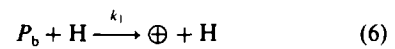


Fig. 3. The high and low frequency C - V characteristics for determination of D_{it} .

100, 1000 and 1800 s. At least 4 MOS devices were selected for each annealing temperature and for each substrate deposition temperature. Although it was found that the anneal time could be accumulated[7], we used a new set of devices (at least 4 per set) for each anneal time to avoid any possible errors. After annealing the devices were allowed to cool down to room temperature prior to the high frequency and the quasi static C - V measurements.

To model the defect annealing chemistry we have used models developed by Reed and Plummer[7]. On the basis of the nonconsumptive two reaction models put forward by Reed and Plummer[7], the dimerization of hydrogen occurs in the bulk of the oxide but hydrogen is not consumed during annealing. The two reactions can be described by



and the corresponding differential equations are

$$\frac{d}{dt} [Si^*] = -k_1 [Si^*][H] \quad (8)$$

$$\frac{d}{dt} [H] = -2k_2 [H]^2 \quad (9)$$

where P_b is the interface trap centre before anneal, $\oplus$ is the annealed P_b , and k_1 and k_2 are the reaction rate constants, $[Si^*]$ and $[H]$ are, respectively, the concentrations of the trivalently bonded silicon atoms and the hydrogen atoms at the SiO₂-Si interface. The solution of eqns (8) and (9) gives

$$[Si^*] = \frac{[Si^*]_0}{\{1 + 2k_2 [H]_0 t\}^n} \quad (10)$$

where $[Si^*]_0$ and $[H]_0$ are, respectively, the initial concentration of the trivalently bonded silicon atoms

and the hydrogen atoms at the SiO₂-Si interface, t is the anneal time, and

$$n = k_1/2k_2 \quad (11)$$

$$k_1 = 2\pi\rho_1 D_H \quad (12)$$

$$k_2 = 4\pi\rho_2 D_H \quad (13)$$

in which D_H is the diffusion coefficient of the hydrogen atoms, which can be expressed as

$$D_H = D_0 \exp(-E_H/kT) \quad (14)$$

and ρ_1 and ρ_2 are the reaction radii which are given by

$$\rho_1 = r_{si} + r_H \quad (15)$$

$$\rho_2 = 2r_H \quad (16)$$

where D_0 is the diffusion coefficient for $T = 0$ K which is $1 \times 10^{-5} \text{ cm}^2 \text{ s}^{-1}$. E_H is the activation energy for diffusion which is about 0.75 eV [12]. r_H and r_{si} are, respectively, the radius of a hydrogen atom which is about 0.5 Å and the capture radius of an interface trap which is not known. By assuming that r_{si} is at least equal to the silicon tetrahedral radius which is 1.2 Å and possibly up to 50% larger, then we have [7]

$$0.4 < n < 0.58. \quad (17)$$

The value of $[H]_0$ depends very much on the reaction between the gate aluminum and traces of water [12], the oxide thickness, and the amount of OH groups available. On the following assumptions: (i) the amount of OH groups is sufficient for reaction (ii) the gate aluminum reacts efficiently with OH within the range of temperatures under this investigation, and (iii) the transport of atomic hydrogen through the oxide is not rate-limited, $[H]_0$ can be estimated by [7]

$$[H]_0 = N_{OH} \exp(-E_g/kT) \quad (18)$$

where N_{OH} is the number of OH groups on the SiO₂ surface which is estimated [7] to be $1.67 \times 10^{23} \text{ cm}^{-2}$, and E_g is the activation energy for reaction which is 0.46 eV.

Substituting eqns (13), (14) and (18) into eqn (10) with $E_H = 0.75 \text{ eV}$, $E_R = 0.46 \text{ eV}$, $N_{OH} = 1.67 \times 10^{23} \text{ cm}^{-2}$ and $D_0 = 1 \times 10^{-5} \text{ cm}^2 \text{ s}^{-1}$, we obtain

$$[Si^*] = [Si^*]_0 (4.2 \times 10^{12} t)^{-n} \exp(-nE_{si}/kT) \quad (19)$$

where $E_{si} = E_H + E_R = 1.21 \text{ eV}$. If the interface traps are mainly the trivalently bonded silicon atoms, then we can consider $D_{it} = [Si^*]$.

C.1. Annealing temperature dependence of D_{it} . By letting $t = 30 \text{ min} = 1800 \text{ s}$, eqn (19) becomes:

$$D_{it} = [Si^*] = [Si^*]_0 (7.5 \times 10^{14})^n \exp(-nE_{si}/kT). \quad (20)$$

This is the equation to show how D_{it} depends on the annealing temperature T . There are two unknown parameters, $[Si^*]_0$ and n in eqn (20). Using a computer plotting program, we have tried to perform curve fitting based on eqn (20) to our experimental data. We first chose one value of n and used various values

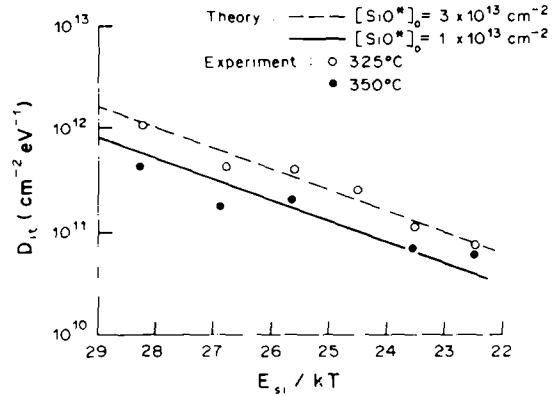


Fig. 4. Midgap D_{it} as a function of annealing temperature for a fixed time of 1800 s for the PECVD SiO₂ films deposited at 325°C and 350°C. Curve fitting based on eqn (20) with $n = 0.81$ and $[Si^*]_0 = 3 \times 10^{13} \text{ cm}^{-2}$ for films deposited at 325°C and $[Si^*]_0 = 1 \times 10^{13} \text{ cm}^{-2}$ for films deposited at 350°C.

of $[Si^*]_0$ to compute D_{it} as a function of T . This computing process was repeated with other values of n within the range of 0.43–0.58, until the best fit was obtained for all MOS devices with the SiO₂ deposited at six different substrate temperatures. Figure 4 shows typical $D_{it} - E_{si}/kT$ characteristics of the SiO₂ deposited at substrate temperatures of 325°C and 350°C. With $n = 0.51$, our experimental data for all six substrate temperatures fit well to eqn (20) if a value of $[Si^*]_0$ within the range from 1×10^{13} to $5 \times 10^{13} \text{ cm}^{-2}$ is chosen.

The value of n obtained in our work is in good agreement with the value of 0.55 reported by Reed and Plummer [7]. Our results strongly support the two reaction models from another angle because Reed and Plummer are mainly concerned with the time parameter while we have arrived at the same results from a temperature parameter. This implies that eqn (20) can actually describe the anneal chemistry of the interface traps. However, one might argue that the oxides used by Reed and Plummer are different from ours and the comparison may be questionable.

C.2. Anneal time dependence of D_{it} . By letting $T = 673 \text{ K}$, eqn (19) becomes

$$D_{it} = [Si^*] = [Si^*]_0 (371t)^{-n}. \quad (21)$$

Again, with $n = 0.51$ our experimental data for all six substrate temperatures fit well to eqn (21) with $[Si^*]_0$ of the order 10^{13} cm^{-2} . Typical $D_{it} - t$ characteristics for the SiO₂ deposited at substrate temperatures of 325°C and 350°C are shown in Fig. 5. These results are also consistent with the results shown in Fig. 4 supporting the validity of the two reaction models for our PECVD SiO₂ films.

The index n from this work is less than that of Reed and Plummer by less than 10%. We cannot say that the radius of the interface trap center in our PECVD SiO₂ films is smaller than that in the thermal oxide. As a matter of fact, there is no good reason why the interface traps of these two kinds of oxides are

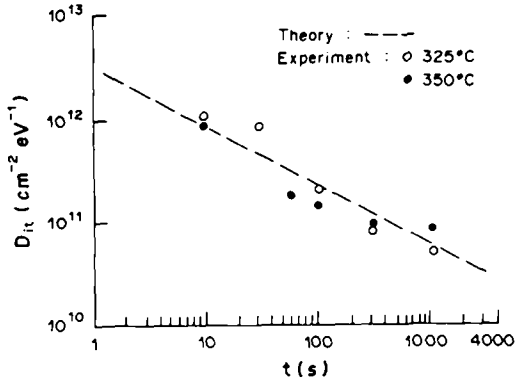


Fig. 5. Midgap D_{it} as a function of anneal time for a fixed annealing temperature of 400°C for the PECVD SiO₂ films deposited at 325°C and 350°C. Curve fitting based on eqn (21) with $n = 0.51$ and $[Si^*]_0 = 1 \times 10^{13} \text{ cm}^{-2}$.

different. Of course, one may argue that the difference is due to the growing temperature which could make the silicon surface of the thermal oxide expand to a greater extent. However, on the basis of our work we can only conclude that there is no detectable difference in the interface traps between the PECVD oxide and the thermal oxide.

In terms of interface traps the major difference between the PECVD oxide and the thermal oxide is the initial amount of interface traps. The PECVD oxide which is deposited at low temperatures is subjected to a certain degree of random bonding. This randomness no doubt creates a large amount of unbonded silicon atoms which make the value of D_{it} for the as-deposited SiO₂ films higher than that of the thermal oxide. However, these interface traps can be reduced to an acceptable level simply by a low temperature anneal.

D. The oxide trapped charge

We use the same $C-V$ curves obtained for the devices annealed at the temperature range from 225°C to 350°C for 1800 s, and annealed at 400°C for the anneal time from 10 to 1800 s as described in the previous subsection for the analysis of the oxide trapped charge. But this time we are interested only in the shift of the high frequency $C-V$ curves.

We use the midgap voltage method[13,14] for the present analysis. We first have to locate the gate bias V_{mg} corresponding to the midgap energy level using eqns (4) and (5), and then translate the ideal $C-V$ curve along the voltage axis until the two curves meet at V_{mg} as shown in Fig. 6. We use the $C-V$ curve after PMA shown in Fig. 1 as the ideal $C-V$ curve because the oxide fixed charge is negligibly small. The flat-band shift V_{fb} given by the ideal $C-V$ curve consists of a voltage shift due to ϕ_{ms} , Q_f and Q_{ot} . Thus the oxide trapped charge density Q_{ot} can be expressed as

$$Q_{ot} = \frac{2\epsilon_{ox}}{d^2} \left(V_{fb} - \frac{dQ_f}{\epsilon_{ox}} - \frac{\phi_{ms}}{q} \right). \quad (22)$$

The possible candidates for positive oxide trapped

charges are trivalent silicon and E' center-like defects. Since trivalent silicon is likely to exist at the interface and E' center is very much associated with plasma chemistry, we believe that E' center-like defects are the major source of positive charge. On the other hand, the only possible defect that may create negative trapped charge is the nonbridging oxygen which is again very much related to plasma chemistry. Since we have assumed that the transport of atomic hydrogen through oxide is not the rate limiting step in annealing the MOS devices, the anneal chemistry of bulk defects and interface traps would be considered similar. Therefore, we shall again use the two reaction models to analyze the bulk defects in the anneal experiment. By assuming that the two bulk defects during anneal take on the nonconsumptive reaction process, then the reactions may be written as



The corresponding differential equations are

$$\frac{d}{dt} [Si^*] = -k_2 [Si^*][H] \quad (27)$$

$$\frac{d}{dt} [H] = -k_2 [Si^*][H] - 2k_3 [H]^2 \quad (28)$$

$$\frac{d}{dt} [SiO^*] = -k_2 [SiO^*][H] \quad (29)$$

$$\frac{d}{dt} [H] = -k_2 [SiO^*][H] - 2k_4 [H]^2. \quad (30)$$

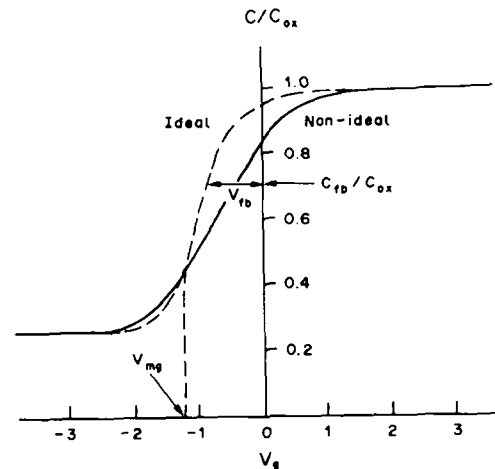


Fig. 6. The midgap voltage method for the determination of V_{fb} .

For simplicity, we assume that $[H]$ is large enough so that the first term of eqns (28) and (30) can be neglected. This results in the nonconsumptive case. Thus the solution of eqns (27)–(30) gives

$$[Si^*] = \frac{[Si^*]_0}{\{1 + 2k_2[H]_0 t\}^{n_1}} \quad (31)$$

which is similar to eqn (10), and

$$[SiO^*] = \frac{[SiO^*]_0}{\{1 + 2k_2[H]_0 t\}^{n_2}} \quad (32)$$

Using the same method for estimating n in Section 3C, we obtain the ranges of n_1 and n_2 as follows:

$$0.41 < n_1 < 0.69 \quad (33)$$

$$0.29 < n_2 < 0.43. \quad (34)$$

D.1. Annealing temperature dependence of Q_{ot} . By letting $t = 1800$ s, we can obtain the net oxide trapped charge Q_{ot} as a function of annealing temperature T , which is the difference of eqns (31) and (32). Thus we can write

$$Q_{ot} = N^+ (7.5 \times 10^{14})^{-n_1} \exp(-n_1 E_{si}/kT) - N^- (7.5 \times 10^{14})^{-n_2} \exp(-n_2 E_{si}/kT) \quad (35)$$

where N^+ and N^- denote the initial contents of the positive charge (i.e. $[Si^*]_0$) and the negative charge (i.e. $[SiO^*]_0$), respectively. There are four undetermined parameters in eqn (35) which make it difficult to visualize the shape of the curves. Worse still, it is not easy to curve fit to our data because they involve both the positive and the negative quantities. However, eqn (35) does predict the relative magnitude of N^+ and N^- , and n_1 and n_2 .

We know that the net oxide trapped charge for the as-deposited SiO_2 films before anneal is positive, i.e. N^+ is greater than N^- in all cases. And from eqns (33) and (34), n_1 is always greater n_2 . A plot of Q_{ot} as a function of E_{si}/kT as shown in Fig. 7 with $n_1 = 0.60$, $n_2 = 0.36$ and $N^+ > N^-$ fits well to our data. Curves based on $n_1 < n_2$ and $N^+ < N^-$ deviate from our data. However, the two reaction model does predict, to a certain extent, the correct trend of our data

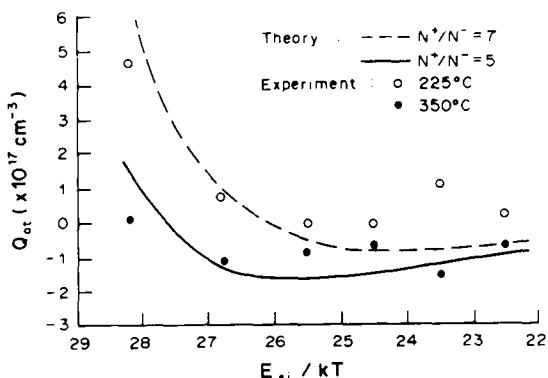


Fig. 7. Q_{ot} as a function of annealing temperature T for a fixed anneal time $t = 1800$ s, with $n_1 = 0.60$ and $n_2 = 0.36$ and various N^+/N^- ratios.

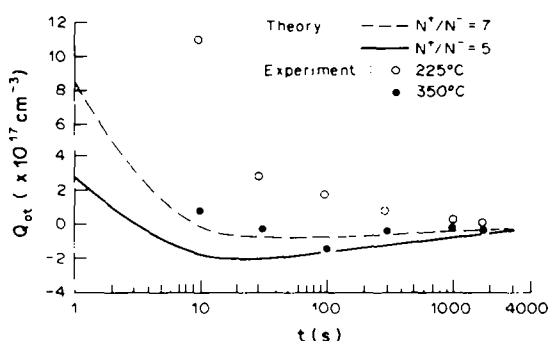


Fig. 8. Q_{ot} as a function of anneal time t for a fixed annealing temperature $T = 637$ K with $n_1 = 0.60$ and $n_2 = 0.36$ and various N^+/N^- ratios.

though a precise description of the contents of the positive and negative charges is not possible.

D.2. Anneal time dependence of Q_{ot} . With $T = 673^\circ\text{C}$ we can express the net oxide trapped charge as a function of anneal time as

$$Q_{ot} = N^+ (371t)^{-n_1} - N^- (371t)^{-n_2}. \quad (36)$$

Again, a plot of Q_{ot} as a function of anneal time t with $n_1 = 0.60$, $n_2 = 0.36$ and $N^+ > N^-$ as shown in Fig. 8 fit to our data reasonably well. The not so distinct turn-round phenomenon in this case as compared with the previous case based on eqn (35) is due to the difference between the exponential function and the power function.

The major difficulty in the analysis is the mixing of the positive and the negative charges inside the bulk. We can determine only the net charge from the $C-V$ analysis, but we are unable to find the actual amounts of the positive and the negative charges. An E' center-like defect which may be a deficit of an oxygen atom could capture an oxygen atom, if available, instead of a hydrogen for passivation. The possibility of this mechanism has been discussed by Reed and Plummer[7]. The nonbridging oxygen, on the other hand, might not form a hydroxyl group with hydrogen because its stability is doubtful. Instead, the bond rearrangement between the oxygen and neighboring silicon is more probable alternative. Again, this mechanism does not consume any hydrogen at the end. All of these propositions, no doubt, will require further research for verification.

In terms of bulk trapped charge, the PECVD SiO_2 film contains in general a higher concentration of negative trapped charge than the thermal oxide. This may be attributed to a higher concentration of nonbridging oxygen defects because the random bonding of the plasma species has a higher chance of missing their neighboring atoms, thus creating a large amount of unbonded oxygen.

It should be noted that the conventional bimolecular one reaction model[7] and the simple hydrogen molecular diffusion model[5] have also been studied but they fail to fit our experimental data. The solution of the two reaction model is different from the

solutions of the other models in that the former contains a temperature-independent index n . The results given in Sections 3C and 3D indicate clearly that n is indeed independent of temperature. Therefore, we can conclude that the two reaction model is an appropriate model for the description of the anneal chemistry of MOS devices.

Recently, some exciting work has shown that the oxide trapped charge in the PECVD films cannot be correlated with the E' center[15]. The above defects have annealing behavior that can be explained in some respects by the E' center but are not E' centers. This leaves much further work to be done in the identification of these defects.

It should also be noted that all the SiO₂ films under this investigation were stoichiometric with hydrogen concentration less than 1 at % based on our Rutherford back scattering spectroscopy and IR absorption results, and that hydrogen was mainly incorporated as Si-OH, no Si-H presence being detected[1]. The bulk traps in SiO₂ films are known to be related to hydrogen or water incorporation[16], but they can be reduced by a proper anneal. However, in terms of electrical integrity the PECVD films are as good as the high quality thermal oxide, but in other properties they are different, such as the etch rate and the Si-O stretching frequency. The present experimental work does not provide information about the factors responsible for this difference. We would believe that due to the quite different fabrication processes the two kinds of films would be different in local bonding structure, void content as well as film stress.

4. CONCLUSIONS

On the basis of our study described above, the following conclusions are drawn:

- (1) The r.f. PECVD SiO₂ films contain only small amounts of oxide fixed charge and mobile ionic charge, both charges being in the low 10^{10} q cm⁻² level. The concentration of both charges after PMA is practically independent of the substrate deposition temperature in the temperature range of 225–350°C, and their presence does not affect the content of the interface traps and the oxide trapped charge.
- (2) The interface trap density is around 10^{12} cm⁻² eV⁻¹ before PMA and is reduced to the mid- 10^{10} cm⁻² eV⁻¹ level after PMA. There is no detectable difference in interface

traps between the r.f. PECVD oxide and the thermal oxide in terms of annealing kinetics.

- (3) The concentrations of the positive and the negative oxide trapped charges are of the order of 10^{17} q cm⁻³ before PMA but they can be reduced to an acceptable level after PMA. The positive oxide trapped charge may be associated with the oxygen vacancy, while the negative oxide trapped charge with the nonbridging oxygen.
- (4) The two reaction model can explain well the annealing processes for interface traps and oxide bulk traps. As the oxide trapped charge consists of both the positive and the negative charges, it is not possible to determine the actual concentrations of these two kinds of charges.

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