

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

RUNERGY ALABAMA INC. and RUNERGY USA INC.,
Petitioners,

v.

TRINA SOLAR CO., LTD.
Patent Owner.

Patent No. 10,230,009

Issued: March 12, 2019

Filed: June 1, 2018

Inventor: Jungmin Ha, *et al.*

Title: Solar Cell and Method for Manufacturing the Same

Inter Partes Review No. IPR2025-00006

SUPPLEMENTAL DECLARATION OF JAMES L. MULLINS, PH.D

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I. INTRODUCTION

I, James L. Mullins, Ph.D., am above the age of majority and hereby declare under penalty of perjury:

1. I have been retained by Petitioner Runergy USA, Inc. and Runergy Alabama Inc. (“Runergy U.S.”) to provide expert opinions in connection with petitions requesting *inter partes* review (IPR) of U.S. Patent Nos. 9,722,104 and 10,230,009 which are owned by Trina Solar Co. Ltd and Trina Solar (U.S.), Inc., (“Trina”). In this declaration, I opine on the authenticity of certain documents referenced herein and explain when and how these documents were disseminated or otherwise made publicly available to the extent that persons interested and ordinarily skilled in the subject matter or art, exercising reasonable diligence, could have located each document. The following is my written testimony on these topics, which supplements my previous testimony I understand has been submitted in this proceeding as EX1035.

2. My background, qualifications, and compensation are set forth in my first declaration and CV. See EX1035, §II and Attachment A.

II. DOCUMENTS

A. **Exhibit 1039. Yablonovitch, E., et al., “A 720 mV Open Circuit Voltage SiO_x:cSi:SiO_x Double Heterostructure Solar Cell,” *Applied Physics Letters*, Volume 47, December 1, 1985, 1211 – 1213. (“Yablonovitch”)**

3. I have been asked to opine on an article authored by E. Yablonovitch, et al., titled “A 720 mV Open Circuit Voltage SiO_x:cSi:SiO_x Double Heterostructure Solar Cell,” published in *Applied Physics Letters*, volume 47, December 1, 1985, on pages 1211 – 1213. (“Yablonovitch”)

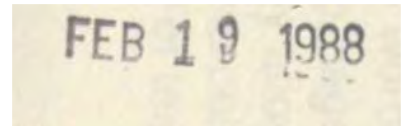
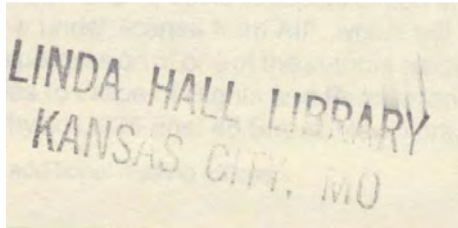
4. For the purposes of this declaration, Yablonovitch, will apply when referring to the article titled: “A 720 mV Open Circuit Voltage SiO_x:cSi:SiO_x Double Heterostructure Solar Cell,” published in *Applied Physics Letters*, volume 47, December 1, 1985, dependent on the context within this declaration.

1. Authenticity of Yablonovitch

5. Exhibit 1039, Attachment A-1, Yablonovitch, has been provided to me by counsel for Runergy U.S. I see no evidence that any alteration or inclusion of pages, etc., were made to Exhibit 1039, Yablonovitch, Attachment A-1. Therefore, I affirm, after verifying it against Attachment A-2 and Attachment A-3, Exhibit 1039, Yablonovitch, is a complete and accurate version of Yablonovitch.

6. Attachment A-2 includes scans from the print copy held by the Linda Hall Library. Attachment A-2 includes: front cover issue cover of *Applied Physics*

Letters, Volume 47, December 1, 1985; journal information page; [Contents] with a stamp that reads “Linda Hall Library, Kansas City, MO”, and a date stamp that reads “FEB 19 1988” as shown below; second [Contents] page and the Yablonovitch article on pages 1211-1213.



7. All identifying characteristics, such as the stamp on Attachment A-3, are consistent with library practice and procedure that I have observed during my career as a professional librarian, specifically with those items held by the Linda Hall Library. I have no cause for concern about the authenticity or accuracy of these identifying attributes.

8. In addition, Yablonovitch was found within the custody of a library, the Linda Hall Library, one of the most likely locations for an authentic publication to be located. Evidence of the ownership of Yablonovitch by the Linda Hall Library will be explored further and detailed in the section below on public access.

Attachment A-3 is a download of Yablonovitch I made on August 4, 2025 through the Purdue University Libraries at URL:

<https://sso.purdue.edu/idp/profile/SAML2/Redirect/SSO?execution=e1s2>

Yablonovitch is available for a fee at URL:

<https://pubs.aip.org/aip/apl/article/47/11/1211/50742/A-720-mV-open-circuit-voltage-C-SiOx-c-Si-SiOx>

9. After my comparison between Exhibit 1039, Attachment A-1, Yablonovitch, with corresponding pages in Attachment A-2, and Attachment A-3, I found no difference between Exhibit 1039 and Attachments A-2 and A-3. Therefore, upon finding Yablonovitch in the Linda Hall Library, and was able to access Yablonovitch through the Purdue University Libraries, I have determined that Exhibit 1039, Yablonovitch is an authentic document.

10. I conclude and affirm that Yablonovitch, Exhibit 1039, Attachment A-1, is an authentic document.

2. Public Accessibility of Yablonovitch

11. Attachment A-4 is a true and correct copy of the *WorldCat* entry for Yablonovitch. I obtained Attachment A-4 by completing a search on *WorldCat* on August 5, 2025 by searching in Missouri.

12. Attachment A-4 shows that Yablonovitch is the document associated with this *WorldCat* entry, as verified by journal title: *Applied Physics Letters*; and publisher: American Institute of Physics. When I searched *WorldCat* for holdings of

Yablonovitch in Missouri, the Linda Hall Library was third on the list among the 1,741 libraries shown as holding editions of *Applied Physics Letters* worldwide.

13. When Yablonovitch was published in 1985 it was prior to online searchable bibliographic databases, such as *WorldCat*, or a disciplinary database such as *Engineering Village*, described above in this declaration. From my experience at that time, the 1980s, *Applied Physics Letters* (Yablonovitch) would have, more likely than not, been found in a print index such as *Engineering Index* described above in this declaration.

14. Attachment A-5 is a download I made from the Linda Hall Library OPAC (online catalog) on August 5, 2025. The document cataloged in this record is Yablonovitch as verified by the OPAC record fields including title: *Applied Physics Letters*; and publisher: American Institute of Physics.

15. The record of holdings of: *Applied Physics Letters* by the Linda Hall Library is shown in the section titled: “Locations” that reads as shown below:

LOCATION ITEMS

Linda Hall Library

Available, Closed Stacks - Serials ; Applied physics letters.

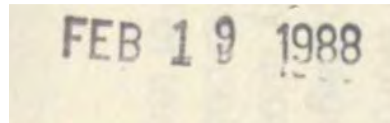
Holdings: v.1:no.1(1962:Sep.)-v.107:no.26(2015:Dec.28)-

Indexes: v.72(1998:Jan.)-v.104:no.3(2014:Jan.20.)-

Note: Index received separately.

16. Yablonovitch could have been located in the Linda Hall Library by searching for the title: *Applied Physics Letters*. As mentioned above, in the 1980s there were no online databases only print indices which would provide access to a citation to Yablonovitch, on the Linda Hall Library OPAC record it lists multiple print indices that *Applied Physics Letters* would have been indexed, more likely than not among the indices, *Current Physics Index* or *Physics Abstracts* would be most likely to index Yablonovitch, would then provide the citation to the journal issue and be able to retrieve Yablonovitch from the print journal held by the Linda Hall Library or any of the 1,741 libraries that now show as holding *Applied Physics Letters*.

17. The date stamped on Attachment A-2 of February 19, 1988 (as shown below) indicates receipt of Yablonovitch by the Linda Hall Library, after which it would have been processed and shelved.



18. The physical copy of Yablonovitch, *Applied Physics Letters*, Volume 47, December 1, 1985 at the Linda Hall Library would have been available for public access, more likely than not, within one week to ten days after it was received on February 19, 1988. Therefore, Yablonovitch would have been accessible to the

public in the Linda Hall Library no later than and be available to a researcher on February 29, 1988.

3. Conclusion - Yablonovitch

19. I conclude that Yablonovitch, Exhibit 1039, is an authentic document and would have been publicly accessible in the Linda Hall Library, more likely than not, February 29, 1988.

B. Exhibit 1044. K. Ip, et al, Charges and Defects in SiO₂ Films Deposited by Plasma-Enhanced Chemical Vapor Deposition at Low Temperatures, *Solid-State Electronics* Vol. 34, No. 2, pp. 123-129, February 1991. (“Ip”)

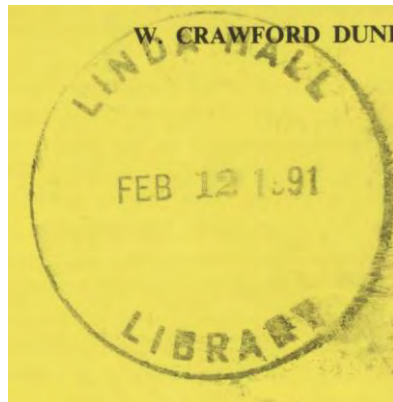
20. I have been asked to opine on an article authored by K. Ip, et al, Charges and Defects in SiO₂ Films Deposited by Plasma-Enhanced Chemical Vapor Deposition at Low Temperatures, published in *Solid-State Electronics*, volume 34, number 2 on pages 123-129, in the February 1991 issue. (“Ip”).

21. For the purposes of this declaration, Ip, will apply when referring to the article titled: Charges and Defects in SiO₂ Films Deposited by Plasma-Enhanced Chemical Vapor Deposition at Low Temperatures, as well as *Solid-State Electronics*, volume 34, number 2, February 1991 issue dependent on the context within this declaration.

1. Authenticity of Ip.

22. Exhibit 1044, Attachment B-1, Ip has been provided to me by counsel for Runergy U.S. I see no evidence that any alteration or inclusion of pages, etc., were made to Exhibit 1044, Ip Attachment B-1. Therefore, I affirm, after verifying it against Attachment B-2 and Attachment B-3, Exhibit 1044, Ip is a complete and accurate version of Ip.

23. Attachment B-2 includes scans from the print copy held by the Linda Hall Library. Attachment B-2 includes: front issue cover of *Solid-State Electronics*, volume 34, number 2, February 1991, with a stamp that reads “LINDA HALL LIBRARY FEB 12 1991”, as shown below; journal information page; “List of Contents” pages iii-xvi; and the Ip article on pages 123-129.



24. All identifying characteristics, such as the stamp on Attachment B-2, are consistent with library practice and procedure that I have observed during my career as a professional librarian, specifically with those items held by the Linda Hall Library. I have no cause for concern about the authenticity or accuracy of these identifying attributes.

25. In addition, Ip was found within the custody of a library, the Linda Hall Library, one of the most likely locations for an authentic publication to be located. Evidence of the ownership of Ip by the Linda Hall Library will be explored further and detailed in the section below on public access.

26. Attachment B-3 is a download of Ip that I made on October 15, 2025 through the Purdue University Libraries at URL:

<https://www.sciencedirect.com/science/article/pii/003811019190077C>

Ip is available for a fee at the same URL:

<https://www.sciencedirect.com/science/article/pii/003811019190077C>

27. After my comparison between Exhibit 1044, Attachment B-1, Ip with corresponding pages in Attachment B-2, and Attachment B-3, I found no difference between Exhibit 1044 and Attachments B-2 and B-3. Therefore, upon finding Ip in the Linda Hall Library, and the ability to access and retrieve Ip through the Purdue

University Libraries, I have determined that Exhibit 1044, Ip is an authentic document.

28. I conclude and affirm that Ip Exhibit 1044, Attachment B-1, is an authentic document.

2. Public Accessibility of Ip

29. Attachment B-4 is a true and correct copy of the *WorldCat* entry for Ip. I obtained Attachment B-4 by completing a search for *Solid-State Electronics* on *WorldCat* on October 16, 2025 by searching the geographic location ‘Missouri.’

30. Attachment B-4 shows that Ip is the document associated with this *WorldCat* entry, as verified by journal title: *Solid-State Electronics*; and publisher: American Institute of Physics. When I searched *WorldCat* for holdings of Ip in Missouri, the Linda Hall Library was first on the list among the 592 libraries shown as holding editions of *Solid-State Electronics* worldwide.

31. When Ip was published in 1991 it was prior to online searchable bibliographic databases, such as *WorldCat*, or a disciplinary database such as *Engineering Village*, described above in this declaration. From my experience at that time, the 1990s, *Solid-State Electronics* (Ip) would have, more likely than not, been found in a print index such as *Engineering Index* described above in this declaration.

32. Attachment B-5 is a download I made from the Linda Hall Library OPAC (online catalog) on October 17, 2025. The document cataloged in this record is Ip as verified by the OPAC record fields including title: *Solid-State Electronics*; and publisher: Pergamon Press.

33. The record of holdings of: *Solid-State Electronics* by the Linda Hall Library is shown in the section titled: “Locations” that reads, v.1-(1960)-v.39(1996)...”, as shown below, inclusive of v.34, number 2, February 1991:

LOCATIONS

Linda Hall Library

Available , Closed Stacks - Serials ; Solid-state electronics.

Holdings:

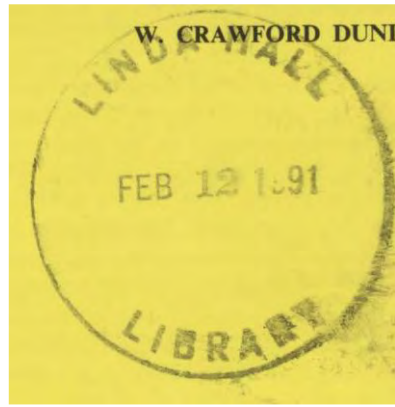
v.1(1960)-v.39(1996); v.40:n.1-8(1996);

v.41(1997)-v.90(2013:Dec.)-

34. Ip could have been located in the Linda Hall Library by searching for the title: *Solid-State Electronics*. As mentioned above, in the 1990s there were no online databases only print indices which would provide access to a citation to Ip. On the Linda Hall Library OPAC record it lists multiple print indices that *Solid-State Electronics* would have been indexed, more likely than not among the indices, *Applied Science and Technology Index* would have been most likely to index Ip and would have provided the citation to the journal issue to retrieve Ip from the print

journal held by the Linda Hall Library or any of the 592 libraries that now show as holding *Solid-State Electronics*.

35. The date stamped on Attachment B-2 of February 12, 1991 (as shown below) indicates receipt of Ip by the Linda Hall Library, after which it would have been processed and shelved.



36. The physical copy of Ip, *Solid-State Electronics*, Volume 34, Number 2, February 12, 1991 at the Linda Hall Library would have been available for public access, more likely than not, within one week to ten days after it was received on February 12, 1991. Therefore, Ip would have been accessible to the public in the Linda Hall Library no later than and be available to a researcher on February 22, 1991.

3. Conclusion - Ip

37. I conclude that Ip Exhibit 1044 is an authentic document and would have been publicly accessible in the Linda Hall Library, more likely than not, February 22, 1991.

III. AVAILABILITY FOR CROSS-EXAMINATION

38. In signing this Declaration, I recognize that this Declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the U.S. Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

IV. RIGHT TO SUPPLEMENT

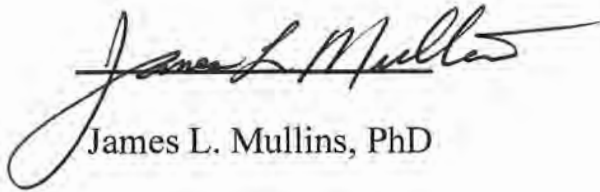
39. I reserve the right to supplement my opinions in the future to respond to any arguments that the Patent Owner raises and to take into account new information as it becomes available to me.

V. JURAT

40. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the full knowledge that willful false statements

and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the U.S. Code.

Dated: October 17, 2025



James L. Mullins, PhD

ATTACHMENT A-1



A 720 mV open circuit voltage SiO_x:cSi:SiO_x double heterostructure solar cell

E. Yablonovitch, T. Gmitter, R. M. Swanson, and Y. H. Kwart

Citation: *Applied Physics Letters* **47**, 1211 (1985); doi: 10.1063/1.96331

View online: <http://dx.doi.org/10.1063/1.96331>

View Table of Contents: <http://scitation.aip.org/content/aip/journal/apl/47/11?ver=pdfcov>

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This is a promotional banner for Agilent Technologies' Engineering Education & Research Resources DVD 2014. The banner has a red top section with the text 'Agilent's Electronic Measurement Group is becoming Keysight Technologies.' Below this is a row of ten colorful icons representing various engineering and research fields: a green circle with a white 'u' (university), a blue checkmark, a blue graduation cap, a green book, a yellow sun, a green network of nodes, a blue antenna, a purple microchip, a green sine wave, an orange circuit board, and a red starburst. To the left of these icons is a circular image of the DVD itself, which also features the Agilent logo and the text 'Agilent Technologies Engineering Education & Research Resources DVD 2014'. Below the icons, the text 'Engineering Education & Research Resources DVD 2014' is written in a large, bold, black font. Underneath this, the phrase 'Agilent is the key to your test and measurement needs' is displayed in a smaller black font, followed by a red button with the white text 'Order yours'. The bottom of the banner is a solid blue section containing the Agilent Technologies logo (a stylized starburst) and the company name 'Agilent Technologies' in white.

A 720 mV open circuit voltage $\text{SiO}_x\text{:c-Si:SiO}_x$ double heterostructure solar cell

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(Received 29 July 1985; accepted for publication 10 September 1985)

For maximal performance solar cells should resemble semiconductor lasers, i.e., they should be constructed in the form of a double heterostructure. We have found rather good performance in SIPOS-crystalline silicon-SIPOS double heterostructure solar cells, where $\text{SIPOS} \equiv \text{SiO}_x$. The processing of these solar cells gives insights into the truly outstanding performance of the n^+ -SIPOS: p -Si heterojunction which has a forward saturation current coefficient $J_0 = 10^{-14} \text{ A/cm}^2$, or equivalently an "emitter Gummel number" $G_e = 3.3 \times 10^{15} \text{ s/cm}^4$. This suggests that crystalline silicon solar cells can be much more efficient than had been suspected.

It has been recognized for some time that the structure of an ideal solar cell should resemble that of a semiconductor laser. The solar cell should be built in the form of a double heterostructure. In this configuration a narrow band-gap active layer is sandwiched between two wide band-gap layers of opposite doping. An example of a double heterostructure biased at a forward voltage V is shown in Fig. 1. The wide band-gap materials may be called "minority-carrier mirrors" although this term is more frequently applied to the high-low doping homojunctions at the rear of solar cells.

It is usually assumed that the wide band-gap heterocontact layers must be single crystal and lattice matched to the active layer to assure high performance. While this has been very successful for the III-V class of semiconductors, it is not actually a necessary condition. The wide band-gap layers need only be of sufficient electronic quality to support the quasi-Fermi level separation in the high quality narrow-gap active layer. Due to its larger band gap, the heterocontact material may be disordered and of poor quality and still be able to support the voltage generated in the active layer. That is the key point. The other main point is that the interface states at the heterocontacts must be passivated.

Since crystalline silicon has no useful lattice-matched heterocontacts, we turn to a disordered semiconductor heterojunction material, SIPOS (originally named semi-insulating polycrystalline silicon). In its annealed form it is a poorly understood mixture of microcrystalline silicon and silicon dioxide (SiO_x). The interface states between SIPOS and crystalline silicon (c -Si) seem to be passivated as well as the high quality interface between thermally grown SiO_2 and c -Si.

The first indication of a superior quality heterojunction using SIPOS came in the pioneering¹ work at Sony. Matsushita *et al.*¹ showed that SIPOS heterojunction emitters incorporated as part of a bipolar transistor structure showed greatly enhanced current gains. A more direct measure of heterojunction quality is the forward saturation current J_0 , where the forward current is given by $J = J_0 \exp(qV/kT)$, where J_0 should be as small as possible. An equivalent figure

of merit² is the "emitter Gummel number" $G_e = qn_i^2/J_0$ which should be as large as possible. (Here q is the electronic charge and n_i is the intrinsic carrier density.)

As a result of the fabrication sequence to be discussed below we now routinely produce $J_0 = 10^{-14} \text{ A/cm}^2$ for n^+ -SIPOS heterocontacts on p -Si (or equivalently $G_e = 3.3 \times 10^{15} \text{ s/cm}^4$). This is about two orders of magnitude superior to a conventional homojunction. Unfortunately we have been unable thus far to achieve a correspondingly good figure of merit for p -type SIPOS. Our best value of forward saturation current on p -type SIPOS is $J_0 = 8 \times 10^{-14} \text{ A/cm}^2$, which is nevertheless superior to that of a homojunction. Due to the lower quality of p -type SIPOS the solar cell we will describe falls short of the ideal of Fig. 1, in that both faces of the silicon wafer will be covered with n^+ -SIPOS.

To achieve the highest possible open circuit voltage, electron-hole recombination in a solar cell must be minimized. There are two major recombination paths; on the surface of the active region and in the bulk of the active region. The purpose of a heterojunction contact is to minimize electron-hole recombination on the surface where electrical contact to one of the carriers is made. Equally important is the bulk recombination. This is minimized by using the highest quality silicon in as thin a crystal as permitted by optical absorption considerations. Recently, a quantitative analysis³ of light trapping in semiconductor sheets showed that the effective internal path length for light rays in textured sheets was $4n^2 \approx 50$ times greater than the sheet thick-

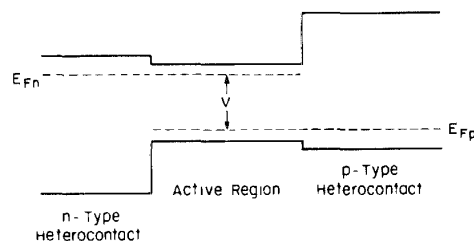


FIG. 1. Ideal solar cell would be in the form of a double heterostructure, by analogy with semiconductor lasers. $V = E_{Fn} - E_{Fp}$ represents the quasi-Fermi level separation.

^{a)}Part of this work was performed while the first two authors were with Exxon Research & Eng'g. Co., Annandale, NJ 08801.

TABLE I. Properties of silicon wafer material.

Orientation	(100)
Resistivity	0.5 Ω cm <i>p</i> -type
Doping concentration	$2.5 \times 10^{16}/\text{cm}^3$
Bulk minority-carrier lifetime	450 μs
Minority-carrier mobility	700 cm^2/Vs
Diffusion length	0.9 mm
Thickness	50 μm
J_0 of <i>n</i> ⁺ -SIPOS heterocontact	10^{-14} A/cm ² at 27 °C
Emitter Gummel number	3.3×10^{15} s/cm ⁴

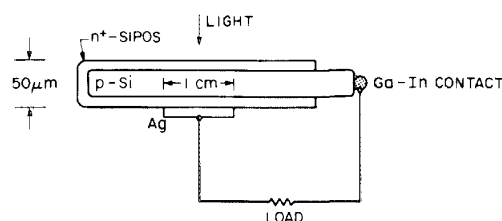
ness (where n is the index of refraction). Accordingly, the optimum⁴ thickness of silicon solar cells is $\approx 50 \mu\text{m}$, much thinner than would be the case without light trapping.

In this work we used float zone *p*-type silicon wafers of 0.5 Ω cm resistivity which were chemically thinned to 50 μm . The material properties are summarized in Table I, and the sequence of processing steps for the SIPOS deposition in Table II. Step (2) in Table II is critical in achieving a bulk minority-carrier lifetime of 450 μs . The as-received material is only about half as good.

The silicon wafers, which were coated on both faces with 1000 Å of *n*⁺-SIPOS, were fabricated into devices as shown in Fig. 2. The *n*⁺-SIPOS was contacted with a 0.5 cm $\times$ 1 cm evaporated silver electrode. The *p*-Si was contacted by Ga-In metal at one edge of the wafer. No attempt was made to optimize the current collection or the fill factor in this design. The series resistance was dominated by the bulk resistance of the wafer itself between the edge contact and the active region. This limited the fill factor to about 0.5.

The open circuit voltage was measured under a simulator at 1.3 suns. The light intensity was calibrated by two separate standard solar cells obtained from SERI. An intensity slightly above one sun was chosen in order to partially compensate for the absence of an antireflection coating on the silicon wafer and to simulate one sun absorbed internally. The measured open circuit voltage⁵ was 720 mV at 25 °C, with relatively small variations from run to run.

This outstanding voltage performance is made possible both by the excellent bulk quality of the crystalline silicon and the excellent surface passivation of the *n*⁺-SIPOS heterocontact. The bulk leakage current is 1.5×10^{-14} A/cm² for the bulk parameters in Table I while the surface component of 10^{-14} A/cm² must be multiplied by 2 for the two faces of

FIG. 2. Test configuration for the SIPOS : *c*-Si : SIPOS double heterostructure solar cells. In this design the fill factor was limited by the bulk resistance of the *p*-Si wafer itself.

the wafer. This gives an overall $J_0^{\text{tot}} = 3.5 \times 10^{-14}$ A/cm², which is responsible for the observed open circuit voltage.

The forward saturation current J_0 of the SIPOS heterocontact was checked in two ways in addition to the implicit check associated with the measured open circuit voltage. One method was to fabricate bipolar transistors using SIPOS emitters⁶ and to measure the transistor characteristics. Another method was to measure the photoconductivity decay lifetime⁷ on wafers with known⁸ excellent bulk lifetime and known bulk doping density. Especially for thin wafers, surface recombination will dominate and the resulting data can be used to determine J_0 . The connection is expressed by $J_0 = qn_i^2 S / p^b$, where S is the observed surface recombination velocity and p^b is the bulk majority-carrier density. All these diagnostic methods agree and give $J_0 = 10^{-14}$ A/cm² for wafers subjected to the processing sequence in Table II.

Of critical importance in achieving this performance level is the oxidation step (6). In omitting that one step the "emitter Gummel number" figure of merit degrades by almost an order of magnitude. We found that purging with high-purity cylinder gas (<0.5 ppm O₂ and H₂O) helps to reproducibly control this oxidation step. In some published^{1,9,10} results on SIPOS heterojunction emitters and polysilicon emitters this step has been omitted, but we believe that oxidation frequently occurs inadvertently and is necessary toward achieving the most favorable figure of merit. Dewar nitrogen gas is notoriously unreliable in regard to oxygen concentration and was avoided. Likewise it was helpful to load the silicon into a cold furnace to prevent inadvertent oxidation.

The annealing step (9) follows SIPOS deposition. This step is necessary to precipitate microcrystalline silicon grains within the material and to activate the phosphorus dopant. In addition during this step the phosphorus diffuses about 20–50 Å into the silicon wafer as measured by secondary ion mass spectrometry. This produces a very shallow *n*⁺ accumulation layer which is transparent to minority carriers; i.e., the holes from the bulk "see" the Si-SiO₂ interface. Recent studies¹¹ of electron-hole recombination at thermally grown Si-SiO₂ interfaces have shown that under accumulation the recombination current is $\exp(qV/kT) \times 10^{-14}$ A/cm², which is consistent with the performance level achieved with the SIPOS emitter structure in Fig. 3.

Oxide thickness between 25 and 40 Å was found to be equally favorable with respect to the "emitter Gummel number." Therefore, differential tunneling between electrons and holes does not appear to be playing a major role because

TABLE II. Processing sequence.

1. Thin silicon wafers to 50 μm in aqueous KOH.
2. Getter in an oxidation furnace containing substantial chlorine.
3. Strip gettering oxide in HF acid.
4. Immediately load into cold APCVD furnace while purging with N ₂ .
5. Ramp up to 650 °C while maintaining N ₂ purge.
6. Oxidize for 5 min with 100 ppm O ₂ .
7. Deposit SIPOS from 1000 ppm SiH ₄ , 50 ppm PH ₃ , and 10 ppm O ₂ .
8. Ramp furnace to 900 °C.
9. Anneal for 15 min.
10. Ramp furnace down to 450 °C.
11. Anneal in forming gas for 2 h.
12. Pull wafers from cold furnace.

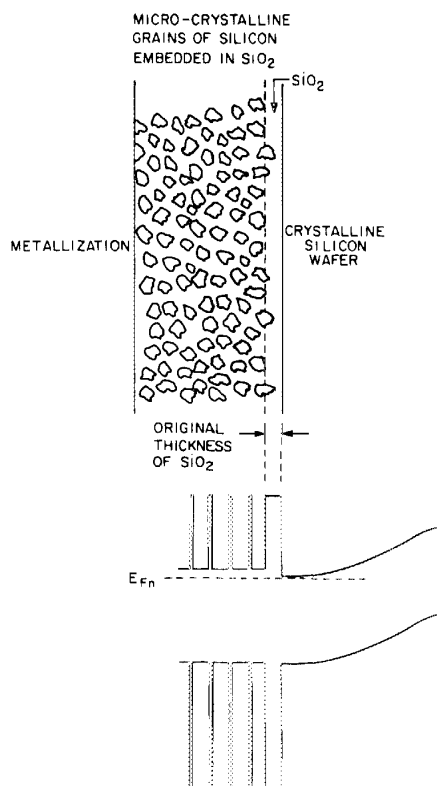


FIG. 3. Model for the metallurgical configuration of the SIPOS-Si heterojunction. Electron conduction is thought to proceed via the microcrystalline grains which protrude into the thin oxide layer.

over part of this range the oxide is too thick for electron tunneling. We believe the majority-carrier electrical contact is by individual microcrystalline grains which occasionally protrude into the oxide as shown in Fig. 3, i.e., electrical contact is via thin spots and pinholes in the SiO_2 . The chemical mixture in step (7) of Table II results in a SIPOS formulation with only 5% oxygen incorporation as determined by x-ray fluorescence. At such low levels of oxygen concentration one might ask what distinguishes a SIPOS heterojunction from a polysilicon emitter. Indeed the resistivity of the n^+ -SIPOS ($\rho = 10^{-3} \Omega \text{ cm}$) is similar to that of doped polysilicon. We believe the importance of the 5% oxygen concentration is metallurgical rather than electrical. The small concentration of oxygen inhibits grain growth and causes a

microcrystalline structure with a significant surface density of individual grains protruding into the thin oxide layer. In polysilicon the grains are much larger, reducing the density of potential contacting points and causing reproducibility and repeatability problems.

We see then that the functioning of the n^+ -SIPOS heterojunction shown in Fig. 3 is complex. The individual contacts provide more than enough conductivity for majority-carrier electrons, but the small fractional contact area acts to block minority-carrier holes from recombining in the SIPOS. Differential tunneling probability between electrons and holes is probably not playing a major role, since such a process would be very sensitive to oxide thickness contrary to what we observe. The functional mechanism of the n^+ -SIPOS: p -Si heterojunction emitter will be discussed at greater length in a forthcoming¹² publication.

The results in this letter suggest that a nonconcentrator crystalline silicon solar cell can be designed to achieve an efficiency of 24% under air mass 1 illumination. This design would rely on superior heterojunction emitters to improve the voltage and on light trapping³ to improve the current in a thin device. The recent achievement¹³ of 25% efficiency in a c -Si concentrator cell (without the benefit of light trapping) should be regarded as further encouragement along these lines.

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ATTACHMENT A-2

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A 720 mV open circuit voltage $\text{SiO}_x\text{:c-Si:SiO}_x$ double heterostructure solar cell

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(Received 29 July 1985; accepted for publication 10 September 1985)

For maximal performance solar cells should resemble semiconductor lasers, i.e., they should be constructed in the form of a double heterostructure. We have found rather good performance in SIPOS-crystalline silicon-SIPOS double heterostructure solar cells, where $\text{SIPOS} \equiv \text{SiO}_x$. The processing of these solar cells gives insights into the truly outstanding performance of the n^+ -SIPOS: p -Si heterojunction which has a forward saturation current coefficient $J_0 = 10^{-14} \text{ A/cm}^2$, or equivalently an "emitter Gummel number" $G_e = 3.3 \times 10^{15} \text{ s/cm}^4$. This suggests that crystalline silicon solar cells can be much more efficient than had been suspected.

It has been recognized for some time that the structure of an ideal solar cell should resemble that of a semiconductor laser. The solar cell should be built in the form of a double heterostructure. In this configuration a narrow band-gap active layer is sandwiched between two wide band-gap layers of opposite doping. An example of a double heterostructure biased at a forward voltage V is shown in Fig. 1. The wide band-gap materials may be called "minority-carrier mirrors" although this term is more frequently applied to the high-low doping homojunctions at the rear of solar cells.

It is usually assumed that the wide band-gap heterocontact layers must be single crystal and lattice matched to the active layer to assure high performance. While this has been very successful for the III-V class of semiconductors, it is not actually a necessary condition. The wide band-gap layers need only be of sufficient electronic quality to support the quasi-Fermi level separation in the high quality narrow-gap active layer. Due to its larger band gap, the heterocontact material may be disordered and of poor quality and still be able to support the voltage generated in the active layer. That is the key point. The other main point is that the interface states at the heterocontacts must be passivated.

Since crystalline silicon has no useful lattice-matched heterocontacts, we turn to a disordered semiconductor heterojunction material, SIPOS (originally named semi-insulating polycrystalline silicon). In its annealed form it is a poorly understood mixture of microcrystalline silicon and silicon dioxide (SiO_x). The interface states between SIPOS and crystalline silicon ($c\text{-Si}$) seem to be passivated as well as the high quality interface between thermally grown SiO_2 and $c\text{-Si}$.

The first indication of a superior quality heterojunction using SIPOS came in the pioneering¹ work at Sony. Matsushita *et al.*¹ showed that SIPOS heterojunction emitters incorporated as part of a bipolar transistor structure showed greatly enhanced current gains. A more direct measure of heterojunction quality is the forward saturation current J_0 , where the forward current is given by $J = J_0 \exp(qV/kT)$, where J_0 should be as small as possible. An equivalent figure

of merit² is the "emitter Gummel number" $G_e = qn_i^2/J_0$ which should be as large as possible. (Here q is the electronic charge and n_i is the intrinsic carrier density.)

As a result of the fabrication sequence to be discussed below we now routinely produce $J_0 = 10^{-14} \text{ A/cm}^2$ for n^+ -SIPOS heterocontacts on $p\text{-Si}$ (or equivalently $G_e = 3.3 \times 10^{15} \text{ s/cm}^4$). This is about two orders of magnitude superior to a conventional homojunction. Unfortunately we have been unable thus far to achieve a correspondingly good figure of merit for p -type SIPOS. Our best value of forward saturation current on p -type SIPOS is $J_0 = 8 \times 10^{-14} \text{ A/cm}^2$, which is nevertheless superior to that of a homojunction. Due to the lower quality of p -type SIPOS the solar cell we will describe falls short of the ideal of Fig. 1, in that both faces of the silicon wafer will be covered with n^+ -SIPOS.

To achieve the highest possible open circuit voltage, electron-hole recombination in a solar cell must be minimized. There are two major recombination paths; on the surface of the active region and in the bulk of the active region. The purpose of a heterojunction contact is to minimize electron-hole recombination on the surface where electrical contact to one of the carriers is made. Equally important is the bulk recombination. This is minimized by using the highest quality silicon in as thin a crystal as permitted by optical absorption considerations. Recently, a quantitative analysis³ of light trapping in semiconductor sheets showed that the effective internal path length for light rays in textured sheets was $4n^2 \approx 50$ times greater than the sheet thick-

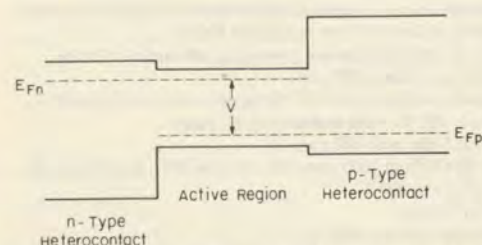


FIG. 1. Ideal solar cell would be in the form of a double heterostructure, by analogy with semiconductor lasers. $V = E_{Fn} - E_{Fp}$ represents the quasi-Fermi level separation.

^{a)}Part of this work was performed while the first two authors were with Exxon Research & Eng'g. Co., Annandale, NJ 08801.

TABLE I. Properties of silicon wafer material.

Orientation	(100)
Resistivity	0.5 Ω cm <i>p</i> -type
Doping concentration	$2.5 \times 10^{16}/\text{cm}^3$
Bulk minority-carrier lifetime	450 μs
Minority-carrier mobility	700 cm^2/Vs
Diffusion length	0.9 mm
Thickness	50 μm
J_0 of <i>n</i> ⁺ -SIPOS heterocontact	10^{-14} A/cm ² at 27 °C
Emitter Gummel number	3.3×10^{15} s/cm ⁴

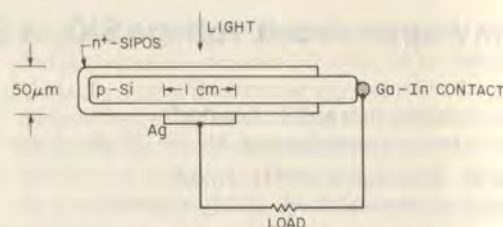
ness (where n is the index of refraction). Accordingly, the optimum⁴ thickness of silicon solar cells is $\approx 50 \mu\text{m}$, much thinner than would be the case without light trapping.

In this work we used float zone *p*-type silicon wafers of 0.5 Ω cm resistivity which were chemically thinned to 50 μm . The material properties are summarized in Table I, and the sequence of processing steps for the SIPOS deposition in Table II. Step (2) in Table II is critical in achieving a bulk minority-carrier lifetime of 450 μs . The as-received material is only about half as good.

The silicon wafers, which were coated on both faces with 1000 Å of *n*⁺-SIPOS, were fabricated into devices as shown in Fig. 2. The *n*⁺-SIPOS was contacted with a 0.5 cm $\times$ 1 cm evaporated silver electrode. The *p*-Si was contacted by Ga-In metal at one edge of the wafer. No attempt was made to optimize the current collection or the fill factor in this design. The series resistance was dominated by the bulk resistance of the wafer itself between the edge contact and the active region. This limited the fill factor to about 0.5.

The open circuit voltage was measured under a simulator at 1.3 suns. The light intensity was calibrated by two separate standard solar cells obtained from SERI. An intensity slightly above one sun was chosen in order to partially compensate for the absence of an antireflection coating on the silicon wafer and to simulate one sun absorbed internally. The measured open circuit voltage⁵ was 720 mV at 25 °C, with relatively small variations from run to run.

This outstanding voltage performance is made possible both by the excellent bulk quality of the crystalline silicon and the excellent surface passivation of the *n*⁺-SIPOS heterocontact. The bulk leakage current is 1.5×10^{-14} A/cm² for the bulk parameters in Table I while the surface component of 10^{-14} A/cm² must be multiplied by 2 for the two faces of

FIG. 2. Test configuration for the SIPOS : c-Si : SIPOS double heterostructure solar cells. In this design the fill factor was limited by the bulk resistance of the *p*-Si wafer itself.

the wafer. This gives an overall $J_0^{\text{tot}} = 3.5 \times 10^{-14}$ A/cm², which is responsible for the observed open circuit voltage.

The forward saturation current J_0 of the SIPOS heterocontact was checked in two ways in addition to the implicit check associated with the measured open circuit voltage. One method was to fabricate bipolar transistors using SIPOS emitters⁶ and to measure the transistor characteristics. Another method was to measure the photoconductivity decay lifetime⁷ on wafers with known⁸ excellent bulk lifetime and known bulk doping density. Especially for thin wafers, surface recombination will dominate and the resulting data can be used to determine J_0 . The connection is expressed by $J_0 = qn_i^2 S / p^b$, where S is the observed surface recombination velocity and p^b is the bulk majority-carrier density. All these diagnostic methods agree and give $J_0 = 10^{-14}$ A/cm² for wafers subjected to the processing sequence in Table II.

Of critical importance in achieving this performance level is the oxidation step (6). In omitting that one step the "emitter Gummel number" figure of merit degrades by almost an order of magnitude. We found that purging with high-purity cylinder gas (<0.5 ppm O₂ and H₂O) helps to reproducibly control this oxidation step. In some published^{1,9,10} results on SIPOS heterojunction emitters and polysilicon emitters this step has been omitted, but we believe that oxidation frequently occurs inadvertently and is necessary toward achieving the most favorable figure of merit. Dewar nitrogen gas is notoriously unreliable in regard to oxygen concentration and was avoided. Likewise it was helpful to load the silicon into a cold furnace to prevent inadvertent oxidation.

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Oxide thickness between 25 and 40 Å was found to be equally favorable with respect to the "emitter Gummel number." Therefore, differential tunneling between electrons and holes does not appear to be playing a major role because

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5. Ramp up to 650 °C while maintaining N ₂ purge.
6. Oxidize for 5 min with 100 ppm O ₂ .
7. Deposit SIPOS from 1000 ppm SiH ₄ , 50 ppm PH ₃ , and 10 ppm O ₂ .
8. Ramp furnace to 900 °C.
9. Anneal for 15 min.
10. Ramp furnace down to 450 °C.
11. Anneal in forming gas for 2 h.
12. Pull wafers from cold furnace.

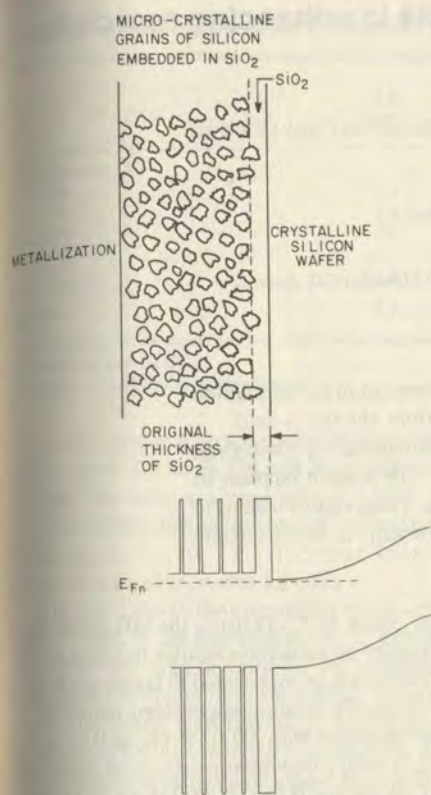


FIG. 3. Model for the metallurgical configuration of the SIPOS-Si heterojunction. Electron conduction is thought to proceed via the microcrystalline grains which protrude into the thin oxide layer.

over part of this range the oxide is too thick for electron tunneling. We believe the majority-carrier electrical contact is by individual microcrystalline grains which occasionally protrude into the oxide as shown in Fig. 3, i.e., electrical contact is via thin spots and pinholes in the SiO_2 . The chemical mixture in step (7) of Table II results in a SIPOS formulation with only 5% oxygen incorporation as determined by x-ray fluorescence. At such low levels of oxygen concentration one might ask what distinguishes a SIPOS heterojunction from a polysilicon emitter. Indeed the resistivity of the n^+ -SIPOS ($\rho = 10^{-3} \Omega \text{ cm}$) is similar to that of doped polysilicon. We believe the importance of the 5% oxygen concentration is metallurgical rather than electrical. The small concentration of oxygen inhibits grain growth and causes a

microcrystalline structure with a significant surface density of individual grains protruding into the thin oxide layer. In polysilicon the grains are much larger, reducing the density of potential contacting points and causing reproducibility and repeatability problems.

We see then that the functioning of the n^+ -SIPOS heterojunction shown in Fig. 3 is complex. The individual contacts provide more than enough conductivity for majority-carrier electrons, but the small fractional contact area acts to block minority-carrier holes from recombining in the SIPOS. Differential tunneling probability between electrons and holes is probably not playing a major role, since such a process would be very sensitive to oxide thickness contrary to what we observe. The functional mechanism of the n^+ -SIPOS: p -Si heterojunction emitter will be discussed at greater length in a forthcoming¹² publication.

The results in this letter suggest that a nonconcentrator crystalline silicon solar cell can be designed to achieve an efficiency of 24% under air mass 1 illumination. This design would rely on superior heterojunction emitters to improve the voltage and on light trapping³ to improve the current in a thin device. The recent achievement¹³ of 25% efficiency in a c -Si concentrator cell (without the benefit of light trapping) should be regarded as further encouragement along these lines.

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ATTACHMENT A-3

RESEARCH ARTICLE | DECEMBER 01 1985

A 720 mV open circuit voltage $\text{SiO}_x\text{:c-Si:SiO}_x$ double heterostructure solar cell

E. Yablonovitch; T. Gmitter; R. M. Swanson; Y. H. Kwark



Appl. Phys. Lett. 47, 1211–1213 (1985)

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A 720 mV open circuit voltage $\text{SiO}_x\text{:c-Si:SiO}_x$ double heterostructure solar cell

E. Yablonovitch and T. Gmitter^{a)}

Bell Communications Research, Murray Hill, New Jersey 07974

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Stanford University, Stanford, California 94305

(Received 29 July 1985; accepted for publication 10 September 1985)

For maximal performance solar cells should resemble semiconductor lasers, i.e., they should be constructed in the form of a double heterostructure. We have found rather good performance in SIPOS-crystalline silicon-SIPOS double heterostructure solar cells, where $\text{SIPOS} \equiv \text{SiO}_x$. The processing of these solar cells gives insights into the truly outstanding performance of the n^+ -SIPOS: p -Si heterojunction which has a forward saturation current coefficient $J_0 = 10^{-14} \text{ A/cm}^2$, or equivalently an "emitter Gummel number" $G_e = 3.3 \times 10^{15} \text{ s/cm}^4$. This suggests that crystalline silicon solar cells can be much more efficient than had been suspected.

It has been recognized for some time that the structure of an ideal solar cell should resemble that of a semiconductor laser. The solar cell should be built in the form of a double heterostructure. In this configuration a narrow band-gap active layer is sandwiched between two wide band-gap layers of opposite doping. An example of a double heterostructure biased at a forward voltage V is shown in Fig. 1. The wide band-gap materials may be called "minority-carrier mirrors" although this term is more frequently applied to the high-low doping homojunctions at the rear of solar cells.

It is usually assumed that the wide band-gap heterocontact layers must be single crystal and lattice matched to the active layer to assure high performance. While this has been very successful for the III-V class of semiconductors, it is not actually a necessary condition. The wide band-gap layers need only be of sufficient electronic quality to support the quasi-Fermi level separation in the high quality narrow-gap active layer. Due to its larger band gap, the heterocontact material may be disordered and of poor quality and still be able to support the voltage generated in the active layer. That is the key point. The other main point is that the interface states at the heterocontacts must be passivated.

Since crystalline silicon has no useful lattice-matched heterocontacts, we turn to a disordered semiconductor heterojunction material, SIPOS (originally named semi-insulating polycrystalline silicon). In its annealed form it is a poorly understood mixture of microcrystalline silicon and silicon dioxide (SiO_x). The interface states between SIPOS and crystalline silicon ($c\text{-Si}$) seem to be passivated as well as the high quality interface between thermally grown SiO_2 and $c\text{-Si}$.

The first indication of a superior quality heterojunction using SIPOS came in the pioneering¹ work at Sony. Matsu-shita *et al.*¹ showed that SIPOS heterojunction emitters incorporated as part of a bipolar transistor structure showed greatly enhanced current gains. A more direct measure of heterojunction quality is the forward saturation current J_0 , where the forward current is given by $J = J_0 \exp(qV/kT)$, where J_0 should be as small as possible. An equivalent figure

of merit² is the "emitter Gummel number" $G_e = qn_i^2/J_0$ which should be as large as possible. (Here q is the electronic charge and n_i is the intrinsic carrier density.)

As a result of the fabrication sequence to be discussed below we now routinely produce $J_0 = 10^{-14} \text{ A/cm}^2$ for n^+ -SIPOS heterocontacts on $p\text{-Si}$ (or equivalently $G_e = 3.3 \times 10^{15} \text{ s/cm}^4$). This is about two orders of magnitude superior to a conventional homojunction. Unfortunately we have been unable thus far to achieve a correspondingly good figure of merit for p -type SIPOS. Our best value of forward saturation current on p -type SIPOS is $J_0 = 8 \times 10^{-14} \text{ A/cm}^2$, which is nevertheless superior to that of a homojunction. Due to the lower quality of p -type SIPOS the solar cell we will describe falls short of the ideal of Fig. 1, in that both faces of the silicon wafer will be covered with n^+ -SIPOS.

To achieve the highest possible open circuit voltage, electron-hole recombination in a solar cell must be minimized. There are two major recombination paths; on the surface of the active region and in the bulk of the active region. The purpose of a heterojunction contact is to minimize electron-hole recombination on the surface where electrical contact to one of the carriers is made. Equally important is the bulk recombination. This is minimized by using the highest quality silicon in as thin a crystal as permitted by optical absorption considerations. Recently, a quantitative analysis³ of light trapping in semiconductor sheets showed that the effective internal path length for light rays in textured sheets was $4n^2 \approx 50$ times greater than the sheet thick-

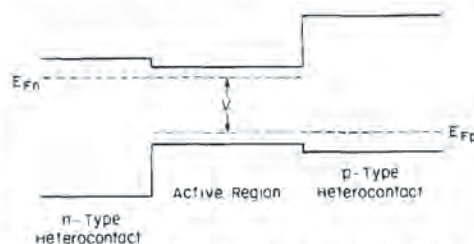


FIG. 1. Ideal solar cell would be in the form of a double heterostructure, by analogy with semiconductor lasers. $V = E_{Fn} - E_{Fp}$ represents the quasi-Fermi level separation.

^{a)} Part of this work was performed while the first two authors were with Exxon Research & Eng'g. Co., Annandale, NJ 08801.

TABLE I. Properties of silicon wafer material.

Orientation	(100)
Resistivity	0.5 Ω cm <i>p</i> -type
Doping concentration	$2.5 \times 10^{16}/\text{cm}^3$
Bulk minority-carrier lifetime	450 μs
Minority-carrier mobility	700 cm^2/Vs
Diffusion length	0.9 mm
Thickness	50 μm
J_0 of n^+ -SIPOS heterocontact	10^{-14} A/cm ² at 27 °C
Emitter Gummel number	3.3×10^{15} s/cm ⁴

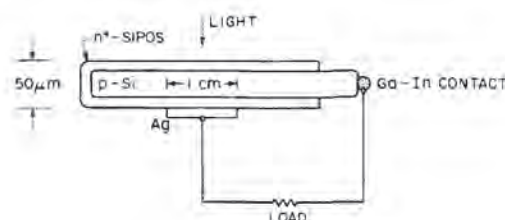
ness (where n is the index of refraction). Accordingly, the optimum⁴ thickness of silicon solar cells is $\approx 50 \mu\text{m}$, much thinner than would be the case without light trapping.

In this work we used float zone *p*-type silicon wafers of 0.5 Ω cm resistivity which were chemically thinned to 50 μm . The material properties are summarized in Table I, and the sequence of processing steps for the SIPOS deposition in Table II. Step (2) in Table II is critical in achieving a bulk minority-carrier lifetime of 450 μs . The as-received material is only about half as good.

The silicon wafers, which were coated on both faces with 1000 Å of n^+ -SIPOS, were fabricated into devices as shown in Fig. 2. The n^+ -SIPOS was contacted with a 0.5 cm $\times$ 1 cm evaporated silver electrode. The *p*-Si was contacted by Ga-In metal at one edge of the wafer. No attempt was made to optimize the current collection or the fill factor in this design. The series resistance was dominated by the bulk resistance of the wafer itself between the edge contact and the active region. This limited the fill factor to about 0.5.

The open circuit voltage was measured under a simulator at 1.3 suns. The light intensity was calibrated by two separate standard solar cells obtained from SERI. An intensity slightly above one sun was chosen in order to partially compensate for the absence of an antireflection coating on the silicon wafer and to simulate one sun absorbed internally. The measured open circuit voltage⁵ was 720 mV at 25 °C, with relatively small variations from run to run.

This outstanding voltage performance is made possible both by the excellent bulk quality of the crystalline silicon and the excellent surface passivation of the n^+ -SIPOS heterocontact. The bulk leakage current is 1.5×10^{-14} A/cm² for the bulk parameters in Table I while the surface component of 10^{-14} A/cm² must be multiplied by 2 for the two faces of

FIG. 2. Test configuration for the SIPOS : c-Si : SIPOS double heterostructure solar cells. In this design the fill factor was limited by the bulk resistance of the *p*-Si wafer itself.

the wafer. This gives an overall $J_0^{\text{tot}} = 3.5 \times 10^{-14}$ A/cm², which is responsible for the observed open circuit voltage.

The forward saturation current J_0 of the SIPOS heterocontact was checked in two ways in addition to the implicit check associated with the measured open circuit voltage. One method was to fabricate bipolar transistors using SIPOS emitters⁶ and to measure the transistor characteristics. Another method was to measure the photoconductivity decay lifetime⁷ on wafers with known⁸ excellent bulk lifetime and known bulk doping density. Especially for thin wafers, surface recombination will dominate and the resulting data can be used to determine J_0 . The connection is expressed by $J_0 = qn_i^2 S / p^b$, where S is the observed surface recombination velocity and p^b is the bulk majority-carrier density. All these diagnostic methods agree and give $J_0 = 10^{-14}$ A/cm² for wafers subjected to the processing sequence in Table II.

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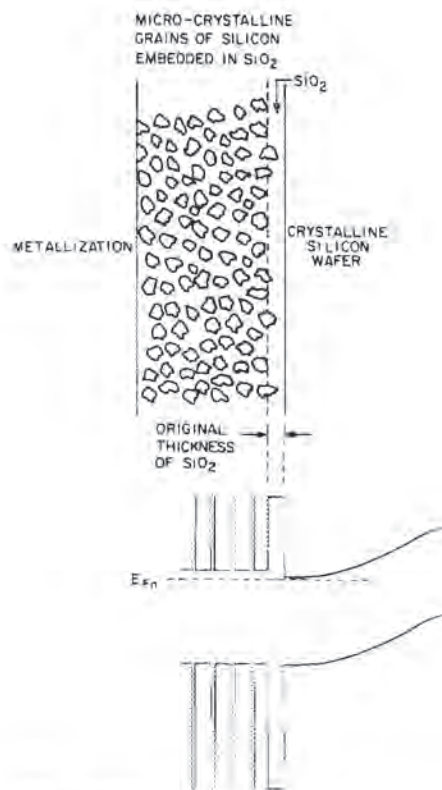


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ATTACHMENT A-4





Applied physics letters

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Journal, Magazine, English, 1962

Edition: [View all formats and editions](#)

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Genre:	Zeitschrift
Physical Description:	volumes illustrations 27 cm
ISSN:	0003-6951, 1520-8842
OCLC Number / Unique Identifier:	1580952
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Publisher	New York : American Institute of Physics Began publication with: Volume 1 (September 1962).
Creation date	1962-
Format	volumes : illustrations ; 27-28 cm
Frequency	Weekly, 1986-
General notes	Issued as companion to: Journal of applied physics, ISSN 0021-8979.
Citations/References	Electronics and communications abstracts journal (Riverdale), ISMEC bulletin, Pollution abstracts with indexes, Safety science abstracts journal, International aerospace abstracts, GeoRef, Metals abstracts, World aluminum abstracts, SPIN, Current physics index, Chemical abstracts, Energy research abstracts, Computer & control abstracts, Electrical & electronics abstracts, Physics abstracts. Science abstracts. Series A,
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ATTACHMENT B-1

CHARGES AND DEFECTS IN SiO_2 FILMS DEPOSITED BY PLASMA-ENHANCED CHEMICAL VAPOR DEPOSITION AT LOW TEMPERATURES

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(Received 23 December 1989; in revised form 2 July 1990)

Abstract—Charges and defects in SiO_2 films deposited by plasma-enhanced chemical vapor deposition (PECVD) have been studied. The SiO_2 films were used to form MOS (aluminum- SiO_2 - n -type silicon) devices. After the devices were annealed in a forming gas at 400°C for 30 min, the oxide fixed charge Q_f measured using the capacitance-voltage (C - V) method was in the low $10^{10} \text{ q cm}^{-2}$, and the mobile ion charge Q_m measured using the bias-temperature aging test in conjunction with the C - V method was also in the low $10^{10} \text{ q cm}^{-2}$. Both Q_f and Q_m are practically independent of substrate deposition temperature for the temperature range of 225 – 350°C used in this investigation. The midgap interface trap density D_{it} and the oxide trapped charge Q_{ot} have also been measured using the high-low frequency C - V method with the devices annealed at various temperatures for a fixed anneal time or at various anneal times for a fixed anneal temperature. The value of D_{it} is of the order of $10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$. The SiO_2 film consists of positive and negative oxide trapped charges which are of the order of $10^{17} \text{ q cm}^{-3}$ prior to post metallization anneal (PMA) at 400°C . The anneal chemistry of the defects in PECVD SiO_2 films is compared with that in thermal SiO_2 .

1. INTRODUCTION

Several investigators[1–4] have recently reported that high quality SiO_2 films can be produced by plasma-enhanced chemical vapor deposition (PECVD) at a temperature around 300°C , and that after a post-metallization anneal (PMA) at 400°C the films exhibit good physical properties and electrical integrity which are close to those for high quality thermal oxides fabricated at 1000°C in dry oxygen. Much effort has been devoted to improve the electrical integrity by optimizing the deposition parameters such as gas pressure, gas composition, power transfer, substrate surface cleanliness, etc. However, little has been reported on the annealing kinetics of various defects and the behavior of various charges in PECVD SiO_2 films. Griscom[5], Plummer *et al.*[6], and Reed and Plummer[7] have studied various charges and defects in MOS devices through the analysis of the annealing chemistry but the SiO_2 in the devices for their studies were either thermal oxides or silica whose defect structure and content might be very different from PECVD oxides. The purpose of this paper is to report our recent study on the annealing kinetics of charges and defects in PECVD SiO_2 deposited at substrate temperatures in the range of 225 – 350°C .

2. EXPERIMENTAL

The SiO_2 films used for this investigation were deposited by a modified radio frequency (13.56 MHz)

PECVD process at six different substrate temperatures using a gas mixture of 2% SiH_4 in He and pure N_2O at the IBM Thomas J. Watson Research Center[2]. The details of the deposition process have been reported earlier[1,2]. The substrates were n -type silicon wafers of resistivity 1 – $2 \Omega\text{-cm}$. One hundred aluminum counter electrodes of 0.025 cm^2 in area each were vacuum-deposited through a shadow mask to form MOS capacitors, the oxide thickness being 500 – $600 \text{ \AA}$. All measurements were made at room temperature before and after the devices had been subjected to post metallization anneal (PMA) at 400°C in a forming gas (10% H_2 in N_2) for 30 min. After the back oxide was removed, indium gallium paste was used to make electrical contacts to the silicon substrate.

The high frequency (1 MHz) capacitance-voltage (C - V) and the quasi-static C - V characteristics were measured using a linear voltage ramp with the ramp rate of 50 mV s^{-1} . For the measurements at negative gate polarity (depletion mode for n -Si) the MOS capacitor was illuminated with light to avoid deep depletion.

3. RESULTS AND DISCUSSION

A. The oxide fixed charge

Since the interface trapped charge and the oxide trapped charge would be removed after a low temperature PMA, the net charge inside the MOS device

after PMA can be considered to be mainly the oxide fixed charge Q_f which can be determined by

$$Q_f = \frac{\epsilon_{ox}(V_{fb} - \phi_{ms}/q)}{d} \quad (1)$$

where V_{fb} is the flatband voltage corresponding to the voltage required to make the band edge of n -Si flat to the SiO_2 -Si interface, ϕ_{ms} is the work function difference between the gate metal work function and the n -Si work function, q is the electronic charge, and ϵ_{ox} and d are, respectively, the permittivity and the thickness of the oxide.

To determine Q_f , we have to know V_{fb} and ϕ_{ms} which can be obtained from the high frequency C - V characteristics. Typical high frequency C - V characteristics for the MOS devices before and after PMA with the SiO_2 deposited at substrate temperatures of 250°C and 350°C are shown in Fig. 1. From these characteristics we obtain the oxide capacitance C_{ox} , the minimum capacitance of the device C_{min} , and the flatband capacitance C_{fb} . With these known parameters we can easily calculate the donor concentration in n -Si, N_d , the thickness d and ϕ_{ms} using standard relations[8,9]. V_{fb} is the parallel shift of the C - V curve. The results of Q_f calculated from eqn (1) show that the oxide fixed charge density is in the low $10^{10} \text{ q cm}^{-2}$ and is practically independent of the substrate temperature for the substrate temperature range under this investigation. It is interesting to note

that Q_f for the thermal oxide depends strongly on the oxidation temperature[10] while Q_f in our PECVD oxide is practically independent of the substrate deposition temperature. If the ionic silicon resulting from the incomplete oxidation at the interface is the major source for Q_f [10], these results indicate that our PECVD oxide should contain little unoxidized silicon at the interface.

B. The mobile ionic charge

Using the method[11] commonly used for the determination of mobile ionic charge, we have measured the mobile ionic charge in our MOS devices. With this method a high frequency C - V characteristic of an MOS device after PMA is first measured, and then this device is heated to about 150°C to mobilize the ions and at the same time a bias of 8 V corresponding to about 1.5 MV cm^{-1} across the oxide is applied to the gate for about 30 min in order to drive all of the ions either to the SiO_2 -Si interface when the bias is positive, or to the SiO_2 -metal interface when the gate is negative. After this bias temperature aging (BTA), the device is then cooled down to the room temperature before the measurement of its C - V characteristic. The parallel shift of this C - V characteristic from that before BTA is the measure of the mobile ions drifted to the interfaces forming a charge sheet there with a density Q_m given by

$$Q_m = (V'_{fb} - V_{fb})C_{ox} \quad (2)$$

where V_{fb} and V'_{fb} are, respectively, the flatband voltages before and after BTA. Typical results are shown in Fig. 2. In general, the flatband shift is small showing that our PECVD SiO_2 films contain mobile ions in the order of $4 \times 10^{10} \text{ cm}^{-2}$. Curve 1 (prior to BTA) (and curve 3 (after BTA with a positive gate bias) are almost identical indicating that the ions are of ionized alkali atoms such as sodium and potassium, and of positive charge; and that they do not

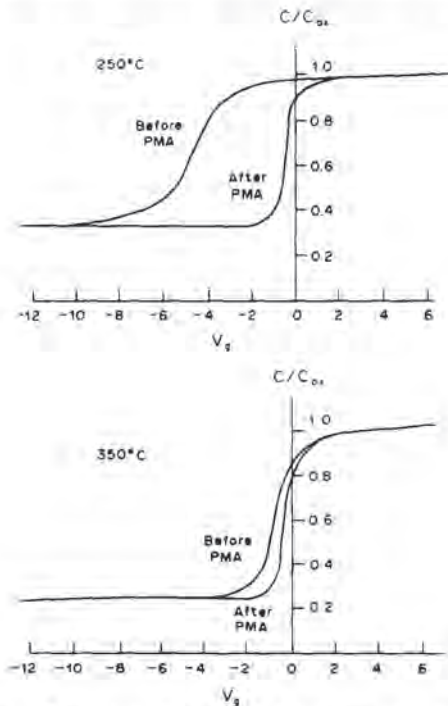


Fig. 1. Typical high frequency C - V characteristics of the PECVD SiO_2 films before and after PMA, deposited at 250°C and at 350°C.

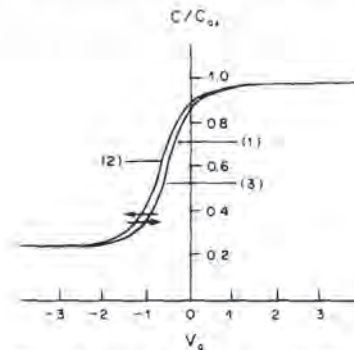


Fig. 2. The shift of the high frequency C - V curve after bias-temperature aging (BTA) for the PECVD SiO_2 deposited at 300°C. Curve (1): the initial C - V prior to BTA, curve (2): the C - V curve after BTA at 150°C and +8 V bias for 30 min, and curve (3): the C - V curve after BTA at 150°C and -8 V bias for 30 min.

exchange charge with either the gate metal or the silicon and do not become discharged even though they pile up to within a tunneling distance at the interfaces. Again, Q_m is practically independent of the substrate deposition temperature for the temperature range of 225–350°C, because the origin of such ions is mainly due to the contamination during fabrication processing such as gate or contact metallization and general handling of the substrate cleaning process, etc.

C. The interface trap density

We have found that the oxide fixed charge and the mobile ionic charge densities are small in our PECVD devices. Therefore, the shift of the $C-V$ curves before and after PMA as shown in Fig. 1 can be considered to be mainly due to the interface trap density D_{it} and the oxide trapped charge density Q_{ox} . It is thus interesting to investigate how fast and how much these charges can be annealed out at a fixed annealing temperature and a fixed anneal time.

The high frequency and the quasi static $C-V$ characteristics (normalized to the oxide capacitance) as shown in Fig. 3 can be used to evaluate D_{it} as a function the gate bias V_g according to the following relation[9].

$$D_{it} = \frac{C_{ox} V_g}{q} \left[\left(\frac{C_{ox}}{C_{LF}} - 1 \right)^{-1} - \left(\frac{C_{ox}}{C_{HF}} - 1 \right)^{-1} \right] \quad (3)$$

where C_{HF} and C_{LF} denote the high frequency and the low frequency (quasi static) capacitances, respectively. Normally, we want to see D_{it} as a function of energy level in the interface band gap. To convert D_{it} as a function of V_g to D_{it} as a function of $E_c - E$, we use the following relations[8]

$$E_c - E = \frac{E_g}{2} + \Psi_s - \phi_b \quad (4)$$

$$\Psi_s = \int_{V_b}^{V_g} (C_{ox} - C_{LF}) dV \quad (5)$$

where E_c is the conduction band edge energy, E_g is the band gap energy, E is the energy level in the gap, ϕ_b is the difference between the thermal equilibrium Fermi level and the intrinsic Fermi level in the silicon bulk, Ψ_s is the surface potential energy at the SiO₂-Si interface. Using an IBM computer program, we have computed and plotted D_{it} as a function of $(E_c - E)$ based on eqns (3)–(5), and from this plot we have determined the mid-gap D_{it} which is the value of D_{it} at 0.55 eV below E_c (the mid-gap based on $E_g = 1.1$ eV for Si at room temperature).

To study the anneal mechanism, we annealed our PECVD devices in two ways. The first way was that the devices were annealed at different temperatures, namely, 225, 250, 275, 300, 325 and 350°C with a fixed anneal time of 30 min. The second way was that the devices were annealed at a fixed temperature of 400°C but with different anneal times, namely, 10, 30,

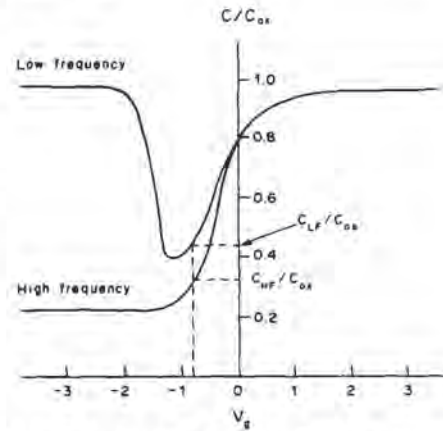
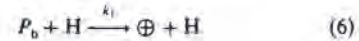


Fig. 3. The high and low frequency $C-V$ characteristics for determination of D_{it} .

100, 1000 and 1800 s. At least 4 MOS devices were selected for each annealing temperature and for each substrate deposition temperature. Although it was found that the anneal time could be accumulated[7], we used a new set of devices (at least 4 per set) for each anneal time to avoid any possible errors. After annealing the devices were allowed to cool down to room temperature prior to the high frequency and the quasi static $C-V$ measurements.

To model the defect annealing chemistry we have used models developed by Reed and Plummer[7]. On the basis of the nonconsumptive two reaction models put forward by Reed and Plummer[7], the dimerization of hydrogen occurs in the bulk of the oxide but hydrogen is not consumed during annealing. The two reactions can be described by



and the corresponding differential equations are

$$\frac{d}{dt} [Si^*] = -k_1 [Si^*][H] \quad (8)$$

$$\frac{d}{dt} [H] = -2k_2 [H]^2 \quad (9)$$

where P_b is the interface trap centre before anneal, $\oplus$ is the annealed P_b , and k_1 and k_2 are the reaction rate constants, $[Si^*]$ and $[H]$ are, respectively, the concentrations of the trivalently bonded silicon atoms and the hydrogen atoms at the SiO₂-Si interface. The solution of eqns (8) and (9) gives

$$[Si^*] = \frac{[Si^*]_0}{\{1 + 2k_2[H]_0 t\}^n} \quad (10)$$

where $[Si^*]_0$ and $[H]_0$ are, respectively, the initial concentration of the trivalently bonded silicon atoms

and the hydrogen atoms at the SiO_2 -Si interface. t is the anneal time, and

$$n = k_1/2k_2 \quad (11)$$

$$k_1 = 2\pi\rho_1 D_H \quad (12)$$

$$k_2 = 4\pi\rho_2 D_H \quad (13)$$

in which D_H is the diffusion coefficient of the hydrogen atoms, which can be expressed as

$$D_H = D_0 \exp(-E_H/kT) \quad (14)$$

and ρ_1 and ρ_2 are the reaction radii which are given by

$$\rho_1 = r_{si} + r_{H1} \quad (15)$$

$$\rho_2 = 2r_{H1} \quad (16)$$

where D_0 is the diffusion coefficient for $T = 0$ K which is $1 \times 10^{-5} \text{ cm}^2 \text{ s}^{-1}$. E_H is the activation energy for diffusion which is about 0.75 eV [12]. r_{H1} and r_{si} are, respectively, the radius of a hydrogen atom which is about 0.5 Å and the capture radius of an interface trap which is not known. By assuming that r_{si} is at least equal to the silicon tetrahedral radius which is 1.2 Å and possibly up to 50% larger, then we have [7]

$$0.4 < n < 0.58. \quad (17)$$

The value of $[\text{H}]_0$ depends very much on the reaction between the gate aluminum and traces of water [12], the oxide thickness, and the amount of OH groups available. On the following assumptions: (i) the amount of OH groups is sufficient for reaction (ii) the gate aluminum reacts efficiently with OH within the range of temperatures under this investigation, and (iii) the transport of atomic hydrogen through the oxide is not rate-limited, $[\text{H}]_0$ can be estimated by [7]

$$[\text{H}]_0 = N_{\text{OH}} \exp(-E_R/kT) \quad (18)$$

where N_{OH} is the number of OH groups on the SiO_2 surface which is estimated [7] to be $1.67 \times 10^{23} \text{ cm}^{-2}$, and E_R is the activation energy for reaction which is 0.46 eV.

Substituting eqns (13), (14) and (18) into eqn (10) with $E_H = 0.75 \text{ eV}$, $E_R = 0.46 \text{ eV}$, $N_{\text{OH}} = 1.67 \times 10^{23} \text{ cm}^{-2}$ and $D_0 = 1 \times 10^{-5} \text{ cm}^2 \text{ s}^{-1}$, we obtain

$$[\text{Si}^*] = [\text{Si}^*]_0 (4.2 \times 10^{12} t)^{-n} \exp(-nE_{si}/kT) \quad (19)$$

where $E_{si} = E_H + E_R = 1.21 \text{ eV}$. If the interface traps are mainly the trivalently bonded silicon atoms, then we can consider $D_{it} = [\text{Si}^*]$.

C.1. Annealing temperature dependence of D_{it} . By letting $t = 30 \text{ min} = 1800 \text{ s}$, eqn (19) becomes:

$$D_{it} = [\text{Si}^*] = [\text{Si}^*]_0 (7.5 \times 10^{14})^{-n} \exp(-nE_{si}/kT). \quad (20)$$

This is the equation to show how D_{it} depends on the annealing temperature T . There are two unknown parameters, $[\text{Si}^*]_0$ and n in eqn (20). Using a computer plotting program, we have tried to perform curve fitting based on eqn (20) to our experimental data. We first chose one value of n and used various values

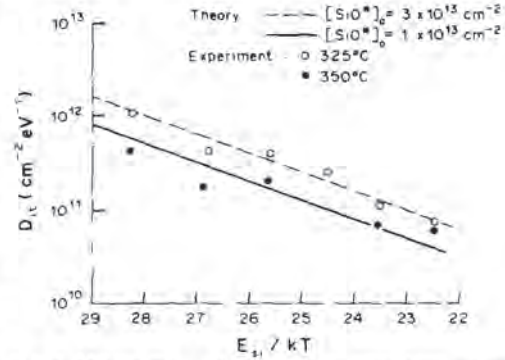


Fig. 4. Midgap D_{it} as a function of annealing temperature for a fixed time of 1800 s for the PECVD SiO_2 films deposited at 325°C and 350°C. Curve fitting based on eqn (20) with $n = 0.81$ and $[\text{Si}^*]_0 = 3 \times 10^{13} \text{ cm}^{-2}$ for films deposited at 325°C and $[\text{Si}^*]_0 = 1 \times 10^{13} \text{ cm}^{-2}$ for films deposited at 350°C.

of $[\text{Si}^*]_0$ to compute D_{it} as a function of T . This computing process was repeated with other values of n within the range of 0.43–0.58, until the best fit was obtained for all MOS devices with the SiO_2 deposited at six different substrate temperatures. Figure 4 shows typical $D_{it} - E_{si}/kT$ characteristics of the SiO_2 deposited at substrate temperatures of 325°C and 350°C. With $n = 0.51$, our experimental data for all six substrate temperatures fit well to eqn (20) if a value of $[\text{Si}^*]_0$ within the range from 1×10^{13} to $5 \times 10^{13} \text{ cm}^{-2}$ is chosen.

The value of n obtained in our work is in good agreement with the value of 0.55 reported by Reed and Plummer [7]. Our results strongly support the two reaction models from another angle because Reed and Plummer are mainly concerned with the time parameter while we have arrived at the same results from a temperature parameter. This implies that eqn (20) can actually describe the anneal chemistry of the interface traps. However, one might argue that the oxides used by Reed and Plummer are different from ours and the comparison may be questionable.

C.2. Anneal time dependence of D_{it} . By letting $T = 673 \text{ K}$, eqn (19) becomes

$$D_{it} = [\text{Si}^*] = [\text{Si}^*]_0 (371t)^{-n}. \quad (21)$$

Again, with $n = 0.51$ our experimental data for all six substrate temperatures fit well to eqn (21) with $[\text{Si}^*]_0$ of the order 10^{13} cm^{-2} . Typical $D_{it} - t$ characteristics for the SiO_2 deposited at substrate temperatures of 325°C and 350°C are shown in Fig. 5. These results are also consistent with the results shown in Fig. 4 supporting the validity of the two reaction models for our PECVD SiO_2 films.

The index n from this work is less than that of Reed and Plummer by less than 10%. We cannot say that the radius of the interface trap center in our PECVD SiO_2 films is smaller than that in the thermal oxide. As a matter of fact, there is no good reason why the interface traps of these two kinds of oxides are

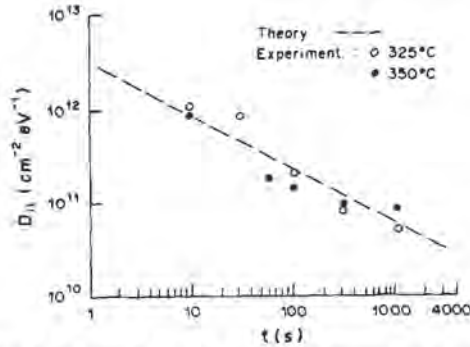


Fig. 5. Midgap D_{it} as a function of anneal time for a fixed annealing temperature of 400°C for the PECVD SiO₂ films deposited at 325°C and 350°C. Curve fitting based on eqn (21) with $\alpha = 0.51$ and $[Si^*]_0 = 1 \times 10^{13} \text{ cm}^{-2}$.

different. Of course, one may argue that the difference is due to the growing temperature which could make the silicon surface of the thermal oxide expand to a greater extent. However, on the basis of our work we can only conclude that there is no detectable difference in the interface traps between the PECVD oxide and the thermal oxide.

In terms of interface traps the major difference between the PECVD oxide and the thermal oxide is the initial amount of interface traps. The PECVD oxide which is deposited at low temperatures is subjected to a certain degree of random bonding. This randomness no doubt creates a large amount of unbonded silicon atoms which make the value of D_{it} for the as-deposited SiO₂ films higher than that of the thermal oxide. However, these interface traps can be reduced to an acceptable level simply by a low temperature anneal.

D. The oxide trapped charge

We use the same $C-V$ curves obtained for the devices annealed at the temperature range from 225°C to 350°C for 1800 s, and annealed at 400°C for the anneal time from 10 to 1800 s as described in the previous subsection for the analysis of the oxide trapped charge. But this time we are interested only in the shift of the high frequency $C-V$ curves.

We use the midgap voltage method [13,14] for the present analysis. We first have to locate the gate bias V_{mg} corresponding to the midgap energy level using eqns (4) and (5), and then translate the ideal $C-V$ curve along the voltage axis until the two curves meet at V_{mg} as shown in Fig. 6. We use the $C-V$ curve after PMA shown in Fig. 1 as the ideal $C-V$ curve because the oxide fixed charge is negligibly small. The flat-band shift V_{fb} given by the ideal $C-V$ curve consists of a voltage shift due to ϕ_{ms} , Q_f and Q_{ox} . Thus the oxide trapped charge density Q_{ox} can be expressed as

$$Q_{ox} = \frac{2\epsilon_{ox}}{d^2} \left(V_{fb} - \frac{dQ_f}{\epsilon_{ox}} - \frac{\phi_{ms}}{q} \right). \quad (22)$$

The possible candidates for positive oxide trapped

charges are trivalent silicon and E' center-like defects. Since trivalent silicon is likely to exist at the interface and E' center is very much associated with plasma chemistry, we believe that E' center-like defects are the major source of positive charge. On the other hand, the only possible defect that may create negative trapped charge is the nonbridging oxygen which is again very much related to plasma chemistry. Since we have assumed that the transport of atomic hydrogen through oxide is not the rate limiting step in annealing the MOS devices, the anneal chemistry of bulk defects and interface traps would be considered similar. Therefore, we shall again use the two reaction models to analyze the bulk defects in the anneal experiment. By assuming that the two bulk defects during anneal take on the nonconsumptive reaction process, then the reactions may be written as



The corresponding differential equations are

$$\frac{d}{dt} [Si^*] = -k_2 [Si^*][H] \quad (27)$$

$$\frac{d}{dt} [H] = -k_2 [Si^*][H] - 2k_3 [H]^2 \quad (28)$$

$$\frac{d}{dt} [SiO^*] = -k_2 [SiO^*][H] \quad (29)$$

$$\frac{d}{dt} [H] = -k_2 [SiO^*][H] - 2k_4 [H]^2 \quad (30)$$

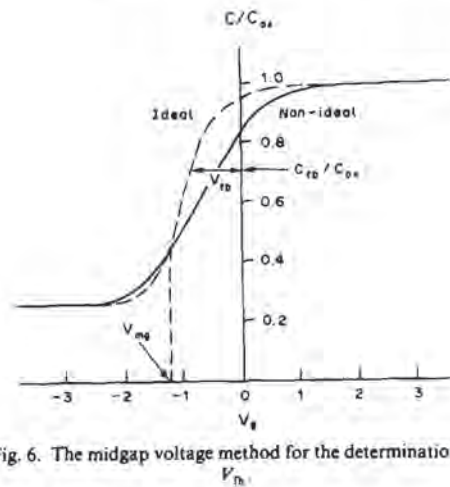


Fig. 6. The midgap voltage method for the determination of V_{fb} .

For simplicity, we assume that $[H]$ is large enough so that the first term of eqns (28) and (30) can be neglected. This results in the nonconsumptive case. Thus the solution of eqns (27)–(30) gives

$$[Si^*] = \frac{[Si^*]_0}{\{1 + 2k_2[H]_0 t\}^{n_1}} \quad (31)$$

which is similar to eqn (10), and

$$[SiO^*] = \frac{[SiO^*]_0}{\{1 + 2k_2[H]_0 t\}^{n_2}} \quad (32)$$

Using the same method for estimating n in Section 3C, we obtain the ranges of n_1 and n_2 as follows:

$$0.41 < n_1 < 0.69 \quad (33)$$

$$0.29 < n_2 < 0.43 \quad (34)$$

D.1. Annealing temperature dependence of Q_{ot} . By letting $t = 1800$ s, we can obtain the net oxide trapped charge Q_{ot} as a function of annealing temperature T , which is the difference of eqns (31) and (32). Thus we can write

$$Q_{ot} = N^+ (7.5 \times 10^{14})^{-n_1} \exp(-n_1 E_{ot}/kT) - N^- (7.5 \times 10^{14})^{-n_2} \exp(-n_2 E_{ot}/kT) \quad (35)$$

where N^+ and N^- denote the initial contents of the positive charge (i.e. $[Si^*]_0$) and the negative charge (i.e. $[SiO^*]_0$), respectively. There are four undetermined parameters in eqn (35) which make it difficult to visualize the shape of the curves. Worse still, it is not easy to curve fit to our data because they involve both the positive and the negative quantities. However, eqn (35) does predict the relative magnitude of N^+ and N^- , and n_1 and n_2 .

We know that the net oxide trapped charge for the as-deposited SiO_2 films before anneal is positive, i.e. N^+ is greater than N^- in all cases. And from eqns (33) and (34), n_1 is always greater n_2 . A plot of Q_{ot} as a function of E_{ot}/kT as shown in Fig. 7 with $n_1 = 0.60$, $n_2 = 0.36$ and $N^+ > N^-$ fits well to our data. Curves based on $n_1 < n_2$ and $N^+ < N^-$ deviate from our data. However, the two reaction model does predict, to a certain extent, the correct trend of our data

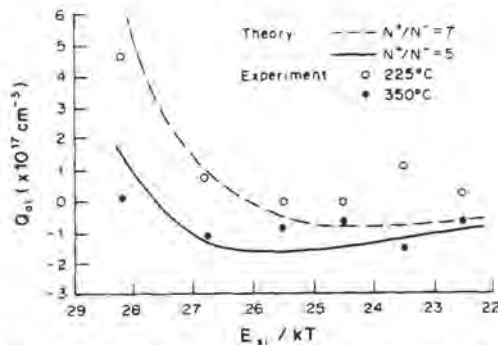


Fig. 7. Q_{ot} as a function of annealing temperature T for a fixed anneal time $t = 1800$ s, with $n_1 = 0.60$ and $n_2 = 0.36$ and various N^+/N^- ratios.

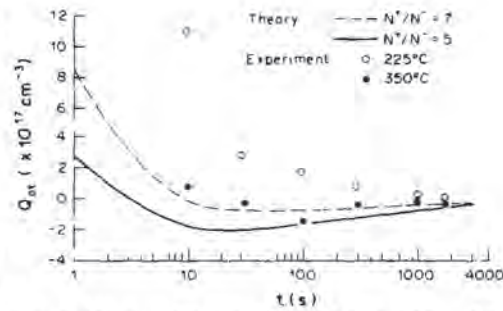


Fig. 8. Q_{ot} as a function of anneal time t for a fixed annealing temperature $T = 637$ K with $n_1 = 0.60$ and $n_2 = 0.36$ and various N^+/N^- ratios.

though a precise description of the contents of the positive and negative charges is not possible.

D.2. Anneal time dependence of Q_{ot} . With $T = 673^\circ\text{C}$ we can express the net oxide trapped charge as a function of anneal time as

$$Q_{ot} = N^+ (371t)^{-n_1} - N^- (371t)^{-n_2} \quad (36)$$

Again, a plot of Q_{ot} as a function of anneal time t with $n_1 = 0.60$, $n_2 = 0.36$ and $N^+ > N^-$ as shown in Fig. 8 fit to our data reasonably well. The not so distinct turn-round phenomenon in this case as compared with the previous case based on eqn (35) is due to the difference between the exponential function and the power function.

The major difficulty in the analysis is the mixing of the positive and the negative charges inside the bulk. We can determine only the net charge from the $C-V$ analysis, but we are unable to find the actual amounts of the positive and the negative charges. An E' center-like defect which may be a deficit of an oxygen atom could capture an oxygen atom, if available, instead of a hydrogen for passivation. The possibility of this mechanism has been discussed by Reed and Plummer[7]. The nonbridging oxygen, on the other hand, might not form a hydroxyl group with hydrogen because its stability is doubtful. Instead, the bond rearrangement between the oxygen and neighboring silicon is more probable alternative. Again, this mechanism does not consume any hydrogen at the end. All of these propositions, no doubt, will require further research for verification.

In terms of bulk trapped charge, the PECVD SiO_2 film contains in general a higher concentration of negative trapped charge than the thermal oxide. This may be attributed to a higher concentration of nonbridging oxygen defects because the random bonding of the plasma species has a higher chance of missing their neighboring atoms, thus creating a large amount of unbonded oxygen.

It should be noted that the conventional bimolecular one reaction model[7] and the simple hydrogen molecular diffusion model[5] have also been studied but they fail to fit our experimental data. The solution of the two reaction model is different from the

solutions of the other models in that the former contains a temperature-independent index n . The results given in Sections 3C and 3D indicate clearly that n is indeed independent of temperature. Therefore, we can conclude that the two reaction model is an appropriate model for the description of the anneal chemistry of MOS devices.

Recently, some exciting work has shown that the oxide trapped charge in the PECVD films cannot be correlated with the E' center [15]. The above defects have annealing behavior that can be explained in some respects by the E' center but are not E' centers. This leaves much further work to be done in the identification of these defects.

It should also be noted that all the SiO₂ films under this investigation were stoichiometric with hydrogen concentration less than 1 at % based on our Rutherford back scattering spectroscopy and IR absorption results, and that hydrogen was mainly incorporated as Si-OH, no Si-H presence being detected [1]. The bulk traps in SiO₂ films are known to be related to hydrogen or water incorporation [16], but they can be reduced by a proper anneal. However, in terms of electrical integrity the PECVD films are as good as the high quality thermal oxide, but in other properties they are different, such as the etch rate and the Si-O stretching frequency. The present experimental work does not provide information about the factors responsible for this difference. We would believe that due to the quite different fabrication processes the two kinds of films would be different in local bonding structure, void content as well as film stress.

4. CONCLUSIONS

On the basis of our study described above, the following conclusions are drawn:

- (1) The r.f. PECVD SiO₂ films contain only small amounts of oxide fixed charge and mobile ionic charge, both charges being in the low 10^{10} q cm⁻² level. The concentration of both charges after PMA is practically independent of the substrate deposition temperature in the temperature range of 225–350°C, and their presence does not affect the content of the interface traps and the oxide trapped charge.
- (2) The interface trap density is around 10^{12} cm⁻² eV⁻¹ before PMA and is reduced to the mid- 10^{10} cm⁻² eV⁻¹ level after PMA. There is no detectable difference in interface

traps between the r.f. PECVD oxide and the thermal oxide in terms of annealing kinetics.

- (3) The concentrations of the positive and the negative oxide trapped charges are of the order of 10^{17} q cm⁻³ before PMA but they can be reduced to an acceptable level after PMA. The positive oxide trapped charge may be associated with the oxygen vacancy, while the negative oxide trapped charge with the nonbridging oxygen.
- (4) The two reaction model can explain well the annealing processes for interface traps and oxide bulk traps. As the oxide trapped charge consists of both the positive and the negative charges, it is not possible to determine the actual concentrations of these two kinds of charges.

Acknowledgements—We wish to thank the Natural Sciences and Engineering Research Council of Canada for supporting this research, the IBM Thomas Watson Research Center for supplying the SiO₂ samples for this investigation, and Drs D.A. Buchanan and P. Wagner for their helpful discussions.

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ATTACHMENT B-2

ISSN 0038-1101

VOLUME 34 NUMBER 2
FEBRUARY 1991

SOLID-STATE ELECTRONICS

An International
Journal

Editor-in-Chief

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West Newton, MA

Regional Editors

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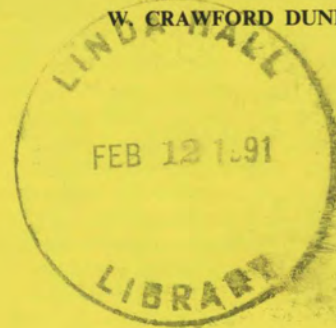
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Annual Subscription Rates for 1991: Annual institutional subscription rate (1991) DM 1060.00; 2-year institutional rate (1991/92) DM 2014.00; personal subscription rate for those whose library subscribes at the regular rate available on application. Subscription rates for Japan include despatch by air and prices are available on application. Prices are subject to amendment without notice.

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AIMS AND SCOPE

It is the function of this Journal to bring together in one publication outstanding papers reporting original work in the following areas: (1) applications of solid-state physics in such fields as transistor technology, including theory and design, crystal growth, measurement and evaluation, preparation of junctions and measurement techniques; (2) applications of computer and numerical methods to the modeling of and simulation of solid-state devices; (3) physics and design of ultra-small (submicron) microelectronic devices (VLSI), including methods of processing, measurement and evaluation. Also of interest are applications of intermetallic and binary and ternary semiconductors, the design and performance of power semiconductor devices, solar cells, photoconductors, thermoelectric and ferroelectric devices, galvanomagnetic devices, and electroluminescent devices, including semiconductor lasers. Of particular interest are solid-state optical devices for storage and transfer of information. Papers covering novel topics extending the frontiers of solid-state technology are of course invited. Review papers covering important topics in solid-state electronics will be presented at intervals. Papers will be published in the formats of regular Research Papers, Notes, and Letters to the Editor.

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CHARGES AND DEFECTS IN SiO_2 FILMS DEPOSITED BY PLASMA-ENHANCED CHEMICAL VAPOR DEPOSITION AT LOW TEMPERATURES

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(Received 23 December 1989; in revised form 2 July 1990)

Abstract—Charges and defects in SiO_2 films deposited by plasma-enhanced chemical vapor deposition (PECVD) have been studied. The SiO_2 films were used to form MOS (aluminum- SiO_2 - n -type silicon) devices. After the devices were annealed in a forming gas at 400°C for 30 min, the oxide fixed charge Q_f measured using the capacitance-voltage (C - V) method was in the low $10^{10} \text{ q cm}^{-2}$, and the mobile ion charge Q_m measured using the bias-temperature aging test in conjunction with the C - V method was also in the low $10^{10} \text{ q cm}^{-2}$. Both Q_f and Q_m are practically independent of substrate deposition temperature for the temperature range of 225 – 350°C used in this investigation. The midgap interface trap density D_{it} and the oxide trapped charge Q_{ot} have also been measured using the high-low frequency C - V method with the devices annealed at various temperatures for a fixed anneal time or at various anneal times for a fixed anneal temperature. The value of D_{it} is of the order of $10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$. The SiO_2 film consists of positive and negative oxide trapped charges which are of the order of $10^{11} \text{ q cm}^{-3}$ prior to post metallization anneal (PMA) at 400°C . The anneal chemistry of the defects in PECVD SiO_2 films is compared with that in thermal SiO_2 .

1. INTRODUCTION

Several investigators[1–4] have recently reported that high quality SiO_2 films can be produced by plasma-enhanced chemical vapor deposition (PECVD) at a temperature around 300°C , and that after a post-metallization anneal (PMA) at 400°C the films exhibit good physical properties and electrical integrity which are close to those for high quality thermal oxides fabricated at 1000°C in dry oxygen. Much effort has been devoted to improve the electrical integrity by optimizing the deposition parameters such as gas pressure, gas composition, power transfer, substrate surface cleanliness, etc. However, little has been reported on the annealing kinetics of various defects and the behavior of various charges in PECVD SiO_2 films. Griscom[5], Plummer *et al.*[6], and Reed and Plummer[7] have studied various charges and defects in MOS devices through the analysis of the annealing chemistry but the SiO_2 in the devices for their studies were either thermal oxides or silica whose defect structure and content might be very different from PECVD oxides. The purpose of this paper is to report our recent study on the annealing kinetics of charges and defects in PECVD SiO_2 deposited at substrate temperatures in the range of 225 – 350°C .

2. EXPERIMENTAL

The SiO_2 films used for this investigation were deposited by a modified radio frequency (13.56 MHz)

PECVD process at six different substrate temperatures using a gas mixture of 2% SiH_4 in He and pure N_2O at the IBM Thomas J. Watson Research Center[2]. The details of the deposition process have been reported earlier[1,2]. The substrates were n -type silicon wafers of resistivity 1 – $2 \Omega\text{-cm}$. One hundred aluminum counter electrodes of 0.025 cm^2 in area each were vacuum-deposited through a shadow mask to form MOS capacitors, the oxide thickness being 500 – $600 \text{ \AA}$. All measurements were made at room temperature before and after the devices had been subjected to post metallization anneal (PMA) at 400°C in a forming gas (10% H_2 in N_2) for 30 min. After the back oxide was removed, indium gallium paste was used to make electrical contacts to the silicon substrate.

The high frequency (1 MHz) capacitance-voltage (C - V) and the quasi-static C - V characteristics were measured using a linear voltage ramp with the ramp rate of 50 mV s^{-1} . For the measurements at negative gate polarity (depletion mode for n -Si) the MOS capacitor was illuminated with light to avoid deep depletion.

3. RESULTS AND DISCUSSION

A. The oxide fixed charge

Since the interface trapped charge and the oxide trapped charge would be removed after a low temperature PMA, the net charge inside the MOS device

after PMA can be considered to be mainly the oxide fixed charge Q_f which can be determined by

$$Q_f = \frac{\epsilon_{ox}(V_{fb} - \phi_{ms}/q)}{d} \quad (1)$$

where V_{fb} is the flatband voltage corresponding to the voltage required to make the band edge of n -Si flat to the SiO_2 -Si interface, ϕ_{ms} is the work function difference between the gate metal work function and the n -Si work function, q is the electronic charge, and ϵ_{ox} and d are, respectively, the permittivity and the thickness of the oxide.

To determine Q_f , we have to know V_{fb} and ϕ_{ms} which can be obtained from the high frequency C - V characteristics. Typical high frequency C - V characteristics for the MOS devices before and after PMA with the SiO_2 deposited at substrate temperatures of 250°C and 350°C are shown in Fig. 1. From these characteristics we obtain the oxide capacitance C_{ox} , the minimum capacitance of the device C_{min} , and the flatband capacitance C_{fb} . With these known parameters we can easily calculate the donor concentration in n -Si, N_d , the thickness d and ϕ_{ms} using standard relations[8,9]. V_{fb} is the parallel shift of the C - V curve. The results of Q_f calculated from eqn (1) show that the oxide fixed charge density is in the low $10^{10} \text{ q cm}^{-2}$ and is practically independent of the substrate temperature for the substrate temperature range under this investigation. It is interesting to note

that Q_f for the thermal oxide depends strongly on the oxidation temperature[10] while Q_f in our PECVD oxide is practically independent of the substrate deposition temperature. If the ionic silicon resulting from the incomplete oxidation at the interface is the major source for Q_f [10], these results indicate that our PECVD oxide should contain little unoxidized silicon at the interface.

B. The mobile ionic charge

Using the method[11] commonly used for the determination of mobile ionic charge, we have measured the mobile ionic charge in our MOS devices. With this method a high frequency C - V characteristic of an MOS device after PMA is first measured, and then this device is heated to about 150°C to mobilize the ions and at the same time a bias of 8 V corresponding to about 1.5 MV cm^{-1} across the oxide is applied to the gate for about 30 min in order to drive all of the ions either to the SiO_2 -Si interface when the bias is positive, or to the SiO_2 -metal interface when the gate is negative. After this bias temperature aging (BTA), the device is then cooled down to the room temperature before the measurement of its C - V characteristic. The parallel shift of this C - V characteristic from that before BTA is the measure of the mobile ions drifted to the interfaces forming a charge sheet there with a density Q_m given by

$$Q_m = (V'_{fb} - V_{fb})C_{ox} \quad (2)$$

where V_{fb} and V'_{fb} are, respectively, the flatband voltages before and after BTA. Typical results are shown in Fig. 2. In general, the flatband shift is small showing that our PECVD SiO_2 films contain mobile ions in the order of $4 \times 10^{10} \text{ cm}^{-2}$. Curve 1 (prior to BTA (and curve 3 (after BTA with a positive gate bias) are almost identical indicating that the ions are of ionized alkali atoms such as sodium and potassium, and of positive charge; and that they do not

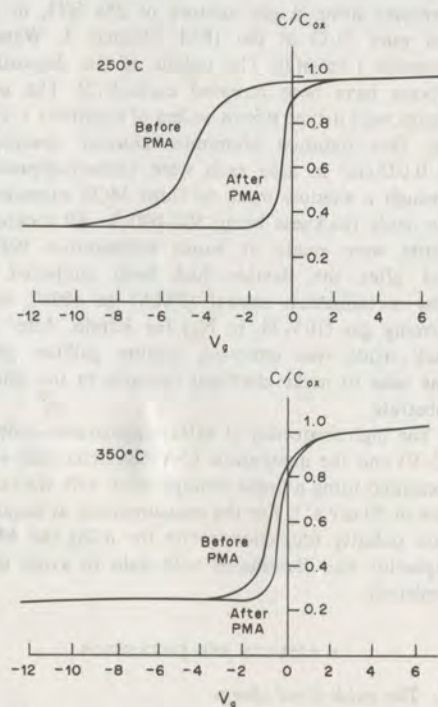


Fig. 1. Typical high frequency C - V characteristics of the PECVD SiO_2 films before and after PMA, deposited at 250°C and at 350°C .

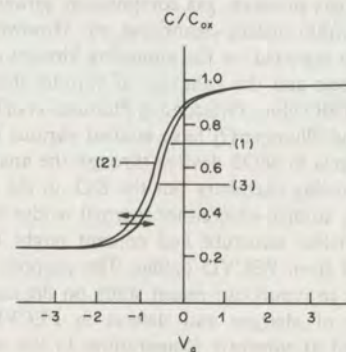


Fig. 2. The shift of the high frequency C - V curve after bias-temperature aging (BTA) for the PECVD SiO_2 deposited at 300°C . Curve (1): the initial C - V prior to BTA, curve (2): the C - V curve after BTA at 150°C and +8 V bias for 30 min, and curve (3): the C - V curve after BTA at 150°C and -8 V bias for 30 min.

exchange charge with either the gate metal or the silicon and do not become discharged even though they pile up to within a tunneling distance at the interfaces. Again, Q_m is practically independent of the substrate deposition temperature for the temperature range of 225–350°C, because the origin of such ions is mainly due to the contamination during fabrication processing such as gate or contact metallization and general handling of the substrate cleaning process, etc.

C. The interface trap density

We have found that the oxide fixed charge and the mobile ionic charge densities are small in our PECVD devices. Therefore, the shift of the $C-V$ curves before and after PMA as shown in Fig. 1 can be considered to be mainly due to the interface trap density D_{it} and the oxide trapped charge density Q_{ot} . It is thus interesting to investigate how fast and how much these charges can be annealed out at a fixed annealing temperature and a fixed anneal time.

The high frequency and the quasi static $C-V$ characteristics (normalized to the oxide capacitance) as shown in Fig. 3 can be used to evaluate D_{it} as a function the gate bias V_g according to the following relation[9].

$$D_{it} = \frac{C_{ox} V_g}{q} \left[\left(\frac{C_{ox}}{C_{LF}} - 1 \right)^{-1} - \left(\frac{C_{ox}}{C_{HF}} - 1 \right)^{-1} \right] \quad (3)$$

where C_{HF} and C_{LF} denote the high frequency and the low frequency (quasi static) capacitances, respectively. Normally, we want to see D_{it} as a function of energy level in the interface band gap. To convert D_{it} as a function of V_g to D_{it} as a function of $E_c - E$, we use the following relations[8]

$$E_c - E = \frac{E_g}{2} + \psi_s - \phi_b \quad (4)$$

$$\psi_s = \int_{V_b}^{V_g} (C_{ox} - C_{LF}) dV \quad (5)$$

where E_c is the conduction band edge energy, E_g is the band gap energy, E is the energy level in the gap, ϕ_b is the difference between the thermal equilibrium Fermi level and the intrinsic Fermi level in the silicon bulk, ψ_s is the surface potential energy at the SiO₂-Si interface. Using an IBM computer program, we have computed and plotted D_{it} as a function of $(E_c - E)$ based on eqns (3)–(5), and from this plot we have determined the mid-gap D_{it} which is the value of D_{it} at 0.55 eV below E_c (the mid-gap based on $E_g = 1.1$ eV for Si at room temperature).

To study the anneal mechanism, we annealed our PECVD devices in two ways. The first way was that the devices were annealed at different temperatures, namely, 225, 250, 275, 300, 325 and 350°C with a fixed anneal time of 30 min. The second way was that the devices were annealed at a fixed temperature of 400°C but with different anneal times, namely, 10, 30,

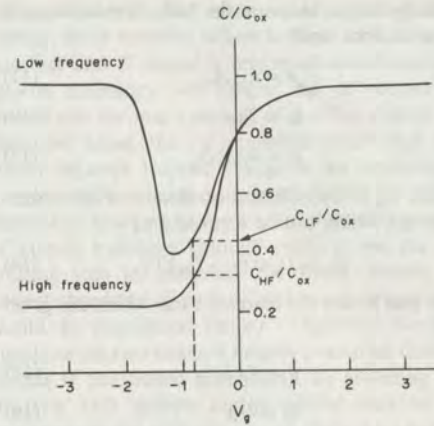
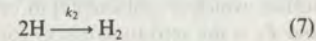
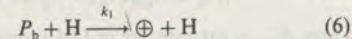


Fig. 3. The high and low frequency $C-V$ characteristics for determination of D_{it} .

100, 1000 and 1800 s. At least 4 MOS devices were selected for each annealing temperature and for each substrate deposition temperature. Although it was found that the anneal time could be accumulated[7], we used a new set of devices (at least 4 per set) for each anneal time to avoid any possible errors. After annealing the devices were allowed to cool down to room temperature prior to the high frequency and the quasi static $C-V$ measurements.

To model the defect annealing chemistry we have used models developed by Reed and Plummer[7]. On the basis of the nonconsumptive two reaction models put forward by Reed and Plummer[7], the dimerization of hydrogen occurs in the bulk of the oxide but hydrogen is not consumed during annealing. The two reactions can be described by



and the corresponding differential equations are

$$\frac{d}{dt} [Si^*] = -k_1 [Si^*][H] \quad (8)$$

$$\frac{d}{dt} [H] = -2k_2 [H]^2 \quad (9)$$

where P_b is the interface trap centre before anneal, $\oplus$ is the annealed P_b , and k_1 and k_2 are the reaction rate constants, $[Si^*]$ and $[H]$ are, respectively, the concentrations of the trivalently bonded silicon atoms and the hydrogen atoms at the SiO₂-Si interface. The solution of eqns (8) and (9) gives

$$[Si^*] = \frac{[Si^*]_0}{\{1 + 2k_2[H]_0 t\}^n} \quad (10)$$

where $[Si^*]_0$ and $[H]_0$ are, respectively, the initial concentration of the trivalently bonded silicon atoms

and the hydrogen atoms at the SiO₂-Si interface, t is the anneal time, and

$$n = k_1/2k_2 \quad (11)$$

$$k_1 = 2\pi\rho_1 D_H \quad (12)$$

$$k_2 = 4\pi\rho_2 D_H \quad (13)$$

in which D_H is the diffusion coefficient of the hydrogen atoms, which can be expressed as

$$D_H = D_0 \exp(-E_H/kT) \quad (14)$$

and ρ_1 and ρ_2 are the reaction radii which are given by

$$\rho_1 = r_{si} + r_H \quad (15)$$

$$\rho_2 = 2r_H \quad (16)$$

where D_0 is the diffusion coefficient for $T = 0$ K which is $1 \times 10^{-5} \text{ cm}^2 \text{ s}^{-1}$, E_H is the activation energy for diffusion which is about 0.75 eV[12], r_H and r_{si} are, respectively, the radius of a hydrogen atom which is about 0.5 Å and the capture radius of an interface trap which is not known. By assuming that r_{si} is at least equal to the silicon tetrahedral radius which is 1.2 Å and possibly up to 50% larger, then we have[7]

$$0.4 < n < 0.58. \quad (17)$$

The value of $[H]_0$ depends very much on the reaction between the gate aluminum and traces of water[12], the oxide thickness, and the amount of OH groups available. On the following assumptions: (i) the amount of OH groups is sufficient for reaction (ii) the gate aluminum reacts efficiently with OH within the range of temperatures under this investigation, and (iii) the transport of atomic hydrogen through the oxide is not rate-limited, $[H]_0$ can be estimated by[7]

$$[H]_0 = N_{OH} \exp(-E_g/kT) \quad (18)$$

where N_{OH} is the number of OH groups on the SiO₂ surface which is estimated[7] to be $1.67 \times 10^{23} \text{ cm}^{-2}$, and E_R is the activation energy for reaction which is 0.46 eV.

Substituting eqns (13), (14) and (18) into eqn (10) with $E_H = 0.75 \text{ eV}$, $E_R = 0.46 \text{ eV}$, $N_{OH} = 1.67 \times 10^{23} \text{ cm}^{-2}$ and $D_0 = 1 \times 10^{-5} \text{ cm}^2 \text{ s}^{-1}$, we obtain

$$[Si^*] = [Si^*]_0 (4.2 \times 10^{12} t)^{-n} \exp(-nE_{si}/kT) \quad (19)$$

where $E_{si} = E_H + E_R = 1.21 \text{ eV}$. If the interface traps are mainly the trivalently bonded silicon atoms, then we can consider $D_{it} = [Si^*]$.

C.1. Annealing temperature dependence of D_{it} . By letting $t = 30 \text{ min} = 1800 \text{ s}$, eqn (19) becomes:

$$D_{it} = [Si^*] = [Si^*]_0 (7.5 \times 10^{14})^n \exp(-nE_{si}/kT). \quad (20)$$

This is the equation to show how D_{it} depends on the annealing temperature T . There are two unknown parameters, $[Si^*]_0$ and n in eqn (20). Using a computer plotting program, we have tried to perform curve fitting based on eqn (20) to our experimental data. We first chose one value of n and used various values

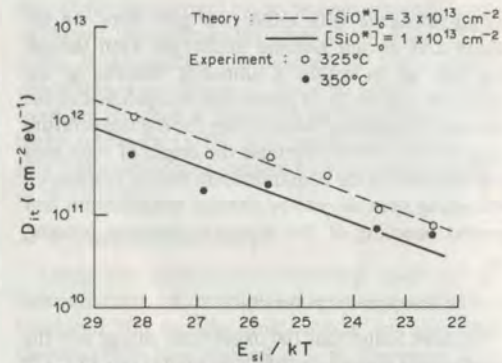


Fig. 4. Midgap D_{it} as a function of annealing temperature for a fixed time of 1800 s for the PECVD SiO₂ films deposited at 325°C and 350°C. Curve fitting based on eqn (20) with $n = 0.81$ and $[Si^*]_0 = 3 \times 10^{13} \text{ cm}^{-2}$ for films deposited at 325°C and $[Si^*]_0 = 1 \times 10^{13} \text{ cm}^{-2}$ for films deposited at 350°C.

of $[Si^*]_0$ to compute D_{it} as a function of T . This computing process was repeated with other values of n within the range of 0.43–0.58, until the best fit was obtained for all MOS devices with the SiO₂ deposited at six different substrate temperatures. Figure 4 shows typical $D_{it} - E_{si}/kT$ characteristics of the SiO₂ deposited at substrate temperatures of 325°C and 350°C. With $n = 0.51$, our experimental data for all six substrate temperatures fit well to eqn (20) if a value of $[Si^*]_0$ within the range from 1×10^{13} to $5 \times 10^{13} \text{ cm}^{-2}$ is chosen.

The value of n obtained in our work is in good agreement with the value of 0.55 reported by Reed and Plummer[7]. Our results strongly support the two reaction models from another angle because Reed and Plummer are mainly concerned with the time parameter while we have arrived at the same results from a temperature parameter. This implies that eqn (20) can actually describe the anneal chemistry of the interface traps. However, one might argue that the oxides used by Reed and Plummer are different from ours and the comparison may be questionable.

C.2. Anneal time dependence of D_{it} . By letting $T = 673 \text{ K}$, eqn (19) becomes

$$D_{it} = [Si^*] = [Si^*]_0 (371t)^{-n}. \quad (21)$$

Again, with $n = 0.51$ our experimental data for all six substrates temperatures fit well to eqn (21) with $[Si^*]_0$ of the order 10^{13} cm^{-2} . Typical $D_{it} - t$ characteristics for the SiO₂ deposited at substrate temperatures of 325°C and 350°C are shown in Fig. 5. These results are also consistent with the results shown in Fig. 4 supporting the validity of the two reaction models for our PECVD SiO₂ films.

The index n from this work is less than that of Reed and Plummer by less than 10%. We cannot say that the radius of the interface trap center in our PECVD SiO₂ films is smaller than that in the thermal oxide. As a matter of fact, there is no good reason why the interface traps of these two kinds of oxides are

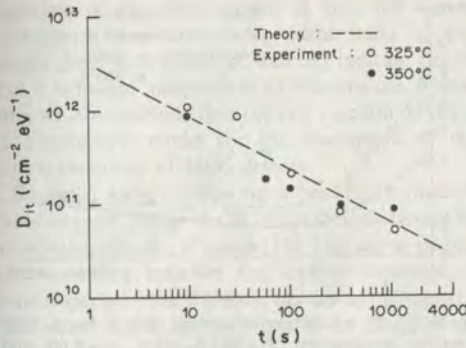


Fig. 5. Midgap D_{it} as a function of anneal time for a fixed annealing temperature of 400°C for the PECVD SiO₂ films deposited at 325°C and 350°C. Curve fitting based on eqn (21) with $n = 0.51$ and $[Si^*]_0 = 1 \times 10^{13} \text{ cm}^{-2}$.

different. Of course, one may argue that the difference is due to the growing temperature which could make the silicon surface of the thermal oxide expand to a greater extent. However, on the basis of our work we can only conclude that there is no detectable difference in the interface traps between the PECVD oxide and the thermal oxide.

In terms of interface traps the major difference between the PECVD oxide and the thermal oxide is the initial amount of interface traps. The PECVD oxide which is deposited at low temperatures is subjected to a certain degree of random bonding. This randomness no doubt creates a large amount of unbonded silicon atoms which make the value of D_{it} for the as-deposited SiO₂ films higher than that of the thermal oxide. However, these interface traps can be reduced to an acceptable level simply by a low temperature anneal.

D. The oxide trapped charge

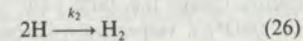
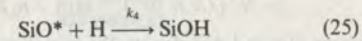
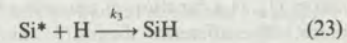
We use the same $C-V$ curves obtained for the devices annealed at the temperature range from 225°C to 350°C for 1800 s, and annealed at 400°C for the anneal time from 10 to 1800 s as described in the previous subsection for the analysis of the oxide trapped charge. But this time we are interested only in the shift of the high frequency $C-V$ curves.

We use the midgap voltage method [13,14] for the present analysis. We first have to locate the gate bias V_{mg} corresponding to the midgap energy level using eqns (4) and (5), and then translate the ideal $C-V$ curve along the voltage axis until the two curves meet at V_{mg} as shown in Fig. 6. We use the $C-V$ curve after PMA shown in Fig. 1 as the ideal $C-V$ curve because the oxide fixed charge is negligibly small. The flat-band shift V_{fb} given by the ideal $C-V$ curve consists of a voltage shift due to ϕ_{ms} , Q_f and Q_{ot} . Thus the oxide trapped charge density Q_{ot} can be expressed as

$$Q_{ot} = \frac{2\epsilon_{ox}}{d^2} \left(V_{fb} - \frac{dQ_f}{\epsilon_{ox}} - \frac{\phi_{ms}}{q} \right). \quad (22)$$

The possible candidates for positive oxide trapped

charges are trivalent silicon and E' center-like defects. Since trivalent silicon is likely to exist at the interface and E' center is very much associated with plasma chemistry, we believe that E' center-like defects are the major source of positive charge. On the other hand, the only possible defect that may create negative trapped charge is the nonbridging oxygen which is again very much related to plasma chemistry. Since we have assumed that the transport of atomic hydrogen through oxide is not the rate limiting step in annealing the MOS devices, the anneal chemistry of bulk defects and interface traps would be considered similar. Therefore, we shall again use the two reaction models to analyze the bulk defects in the anneal experiment. By assuming that the two bulk defects during anneal take on the nonconsumptive reaction process, then the reactions may be written as



The corresponding differential equations are

$$\frac{d}{dt} [Si^*] = -k_2 [Si^*][H] \quad (27)$$

$$\frac{d}{dt} [H] = -k_2 [Si^*][H] - 2k_3 [H]^2 \quad (28)$$

$$\frac{d}{dt} [SiO^*] = -k_2 [SiO^*][H] \quad (29)$$

$$\frac{d}{dt} [H] = -k_2 [SiO^*][H] - 2k_4 [H]^2. \quad (30)$$

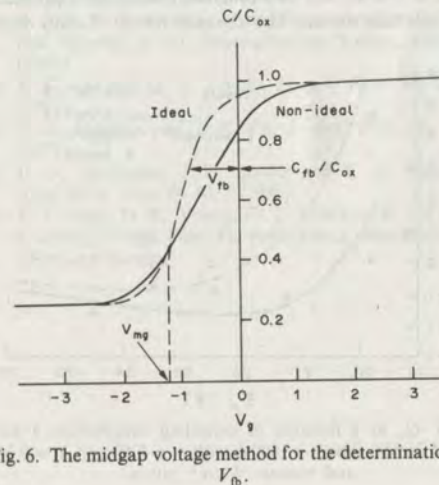


Fig. 6. The midgap voltage method for the determination of V_{fb} .

For simplicity, we assume that $[H]$ is large enough so that the first term of eqns (28) and (30) can be neglected. This results in the nonconsumptive case. Thus the solution of eqns (27)–(30) gives

$$[Si^*] = \frac{[Si^*]_0}{\{1 + 2k_2[H]_0 t\}^{n_1}} \quad (31)$$

which is similar to eqn (10), and

$$[SiO^*] = \frac{[SiO^*]_0}{\{1 + 2k_2[H]_0 t\}^{n_2}} \quad (32)$$

Using the same method for estimating n in Section 3C, we obtain the ranges of n_1 and n_2 as follows:

$$0.41 < n_1 < 0.69 \quad (33)$$

$$0.29 < n_2 < 0.43. \quad (34)$$

D.1. Annealing temperature dependence of Q_{ot} . By letting $t = 1800$ s, we can obtain the net oxide trapped charge Q_{ot} as a function of annealing temperature T , which is the difference of eqns (31) and (32). Thus we can write

$$Q_{ot} = N^+(7.5 \times 10^{14})^{-n_1} \exp(-n_1 E_{si}/kT) - N^-(7.5 \times 10^{14})^{-n_2} \exp(-n_2 E_{si}/kT) \quad (35)$$

where N^+ and N^- denote the initial contents of the positive charge (i.e. $[Si^*]_0$) and the negative charge (i.e. $[SiO^*]_0$), respectively. There are four undetermined parameters in eqn (35) which make it difficult to visualize the shape of the curves. Worse still, it is not easy to curve fit to our data because they involve both the positive and the negative quantities. However, eqn (35) does predict the relative magnitude of N^+ and N^- , and n_1 and n_2 .

We know that the net oxide trapped charge for the as-deposited SiO_2 films before anneal is positive, i.e. N^+ is greater than N^- in all cases. And from eqns (33) and (34), n_1 is always greater than n_2 . A plot of Q_{ot} as a function of E_{si}/kT as shown in Fig. 7 with $n_1 = 0.60$, $n_2 = 0.36$ and $N^+ > N^-$ fits well to our data. Curves based on $n_1 < n_2$ and $N^+ < N^-$ deviate from our data. However, the two reaction model does predict, to a certain extent, the correct trend of our data

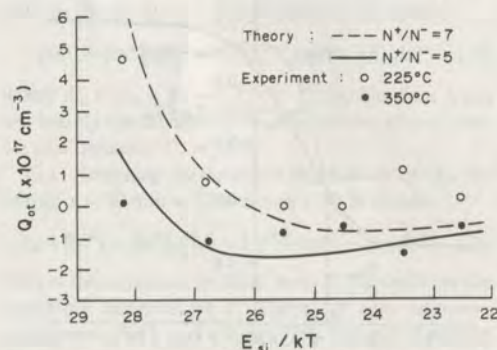


Fig. 7. Q_{ot} as a function of annealing temperature T for a fixed anneal time $t = 1800$ s, with $n_1 = 0.60$ and $n_2 = 0.36$ and various N^+/N^- ratios.

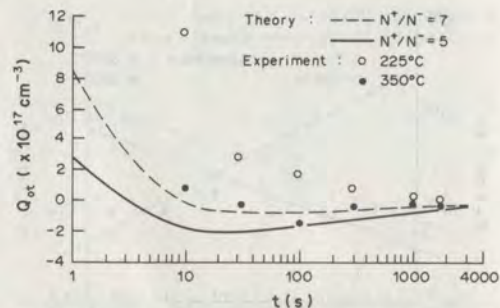


Fig. 8. Q_{ot} as a function of anneal time t for a fixed annealing temperature $T = 637$ K with $n_1 = 0.60$ and $n_2 = 0.36$ and various N^+/N^- ratios.

though a precise description of the contents of the positive and negative charges is not possible.

D.2. Anneal time dependence of Q_{ot} . With $T = 673^\circ\text{C}$ we can express the net oxide trapped charge as a function of anneal time as

$$Q_{ot} = N^+(371t)^{-n_1} - N^-(371t)^{-n_2}. \quad (36)$$

Again, a plot of Q_{ot} as a function of anneal time t with $n_1 = 0.60$, $n_2 = 0.36$ and $N^+ > N^-$ as shown in Fig. 8 fit to our data reasonably well. The not so distinct turn-round phenomenon in this case as compared with the previous case based on eqn (35) is due to the difference between the exponential function and the power function.

The major difficulty in the analysis is the mixing of the positive and the negative charges inside the bulk. We can determine only the net charge from the $C-V$ analysis, but we are unable to find the actual amounts of the positive and the negative charges. An E' center-like defect which may be a deficit of an oxygen atom could capture an oxygen atom, if available, instead of a hydrogen for passivation. The possibility of this mechanism has been discussed by Reed and Plummer[7]. The nonbridging oxygen, on the other hand, might not form a hydroxyl group with hydrogen because its stability is doubtful. Instead, the bond rearrangement between the oxygen and neighboring silicon is more probable alternative. Again, this mechanism does not consume any hydrogen at the end. All of these propositions, no doubt, will require further research for verification.

In terms of bulk trapped charge, the PECVD SiO_2 film contains in general a higher concentration of negative trapped charge than the thermal oxide. This may be attributed to a higher concentration of nonbridging oxygen defects because the random bonding of the plasma species has a higher chance of missing their neighboring atoms, thus creating a large amount of unbonded oxygen.

It should be noted that the conventional bimolecular one reaction model[7] and the simple hydrogen molecular diffusion model[5] have also been studied but they fail to fit our experimental data. The solution of the two reaction model is different from the

solutions of the other models in that the former contains a temperature-independent index n . The results given in Sections 3C and 3D indicate clearly that n is indeed independent of temperature. Therefore, we can conclude that the two reaction model is an appropriate model for the description of the anneal chemistry of MOS devices.

Recently, some exciting work has shown that the oxide trapped charge in the PECVD films cannot be correlated with the E' center[15]. The above defects have annealing behavior that can be explained in some respects by the E' center but are not E' centers. This leaves much further work to be done in the identification of these defects.

It should also be noted that all the SiO₂ films under this investigation were stoichiometric with hydrogen concentration less than 1 at % based on our Rutherford back scattering spectroscopy and IR absorption results, and that hydrogen was mainly incorporated as Si-OH, no Si-H presence being detected[1]. The bulk traps in SiO₂ films are known to be related to hydrogen or water incorporation[16], but they can be reduced by a proper anneal. However, in terms of electrical integrity the PECVD films are as good as the high quality thermal oxide, but in other properties they are different, such as the etch rate and the Si-O stretching frequency. The present experimental work does not provide information about the factors responsible for this difference. We would believe that due to the quite different fabrication processes the two kinds of films would be different in local bonding structure, void content as well as film stress.

4. CONCLUSIONS

On the basis of our study described above, the following conclusions are drawn:

- (1) The r.f. PECVD SiO₂ films contain only small amounts of oxide fixed charge and mobile ionic charge, both charges being in the low 10^{10} q cm⁻² level. The concentration of both charges after PMA is practically independent of the substrate deposition temperature in the temperature range of 225–350°C, and their presence does not affect the content of the interface traps and the oxide trapped charge.
- (2) The interface trap density is around 10^{12} cm⁻² eV⁻¹ before PMA and is reduced to the mid- 10^{10} cm⁻² eV⁻¹ level after PMA. There is no detectable difference in interface traps between the r.f. PECVD oxide and the thermal oxide in terms of annealing kinetics.
- (3) The concentrations of the positive and the negative oxide trapped charges are of the order of 10^{17} q cm⁻³ before PMA but they can be reduced to an acceptable level after PMA. The positive oxide trapped charge may be associated with the oxygen vacancy, while the negative oxide trapped charge with the nonbridging oxygen.
- (4) The two reaction model can explain well the annealing processes for interface traps and oxide bulk traps. As the oxide trapped charge consists of both the positive and the negative charges, it is not possible to determine the actual concentrations of these two kinds of charges.

Acknowledgements—We wish to thank the Natural Sciences and Engineering Research Council of Canada for supporting this research, the IBM Thomas Watson Research Center for supplying the SiO₂ samples for this investigation, and Drs D.A. Buchanan and P. Wagner for their helpful discussions.

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ATTACHMENT B-3

CHARGES AND DEFECTS IN SiO₂ FILMS DEPOSITED BY PLASMA-ENHANCED CHEMICAL VAPOR DEPOSITION AT LOW TEMPERATURES

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(Received 23 December 1989; in revised form 2 July 1990)

Abstract—Charges and defects in SiO₂ films deposited by plasma-enhanced chemical vapor deposition (PECVD) have been studied. The SiO₂ films were used to form MOS (aluminum-SiO₂-*n*-type silicon) devices. After the devices were annealed in a forming gas at 400°C for 30 min, the oxide fixed charge Q_f measured using the capacitance-voltage (*C-V*) method was in the low 10¹⁰ q cm⁻², and the mobile ion charge Q_m measured using the bias-temperature aging test in conjunction with the *C-V* method was also in the low 10¹⁰ q cm⁻². Both Q_f and Q_m are practically independent of substrate deposition temperature for the temperature range of 225–350°C used in this investigation. The midgap interface trap density D_{it} and the oxide trapped charge Q_{ot} have also been measured using the high-low frequency *C-V* method with the devices annealed at various temperatures for a fixed anneal time or at various anneal times for a fixed anneal temperature. The value of D_{it} is of the order of 10¹⁰ cm⁻² eV⁻¹. The SiO₂ film consists of positive and negative oxide trapped charges which are of the order of 10¹⁷ q cm⁻³ prior to post metallization anneal (PMA) at 400°C. The anneal chemistry of the defects in PECVD SiO₂ films is compared with that in thermal SiO₂.

1. INTRODUCTION

Several investigators[1–4] have recently reported that high quality SiO₂ films can be produced by plasma-enhanced chemical vapor deposition (PECVD) at a temperature around 300°C, and that after a post-metallization anneal (PMA) at 400°C the films exhibit good physical properties and electrical integrity which are close to those for high quality thermal oxides fabricated at 1000°C in dry oxygen. Much effort has been devoted to improve the electrical integrity by optimizing the deposition parameters such as gas pressure, gas composition, power transfer, substrate surface cleanliness, etc. However, little has been reported on the annealing kinetics of various defects and the behavior of various charges in PECVD SiO₂ films. Griscom[5], Plummer *et al.*[6], and Reed and Plummer[7] have studied various charges and defects in MOS devices through the analysis of the annealing chemistry but the SiO₂ in the devices for their studies were either thermal oxides or silica whose defect structure and content might be very different from PECVD oxides. The purpose of this paper is to report our recent study on the annealing kinetics of charges and defects in PECVD SiO₂ deposited at substrate temperatures in the range of 225–350°C.

2. EXPERIMENTAL

The SiO₂ films used for this investigation were deposited by a modified radio frequency (13.56 MHz)

PECVD process at six different substrate temperatures using a gas mixture of 2% SiH₄ in He and pure N₂O at the IBM Thomas J. Watson Research Center[2]. The details of the deposition process have been reported earlier[1,2]. The substrates were *n*-type silicon wafers of resistivity 1–2 Ω-cm. One hundred aluminum counter electrodes of 0.025 cm² in area each were vacuum-deposited through a shadow mask to form MOS capacitors, the oxide thickness being 500–600 Å. All measurements were made at room temperature before and after the devices had been subjected to post metallization anneal (PMA) at 400°C in a forming gas (10% H₂ in N₂) for 30 min. After the back oxide was removed, indium gallium paste was used to make electrical contacts to the silicon substrate.

The high frequency (1 MHz) capacitance-voltage (*C-V*) and the quasi-static *C-V* characteristics were measured using a linear voltage ramp with the ramp rate of 50 mV s⁻¹. For the measurements at negative gate polarity (depletion mode for *n*-Si) the MOS capacitor was illuminated with light to avoid deep depletion.

3. RESULTS AND DISCUSSION

A. The oxide fixed charge

Since the interface trapped charge and the oxide trapped charge would be removed after a low temperature PMA, the net charge inside the MOS device

after PMA can be considered to be mainly the oxide fixed charge Q_f which can be determined by

$$Q_f = \frac{\epsilon_{ox}(V_{fb} - \phi_{ms} \cdot q)}{d} \tag{1}$$

where V_{fb} is the flatband voltage corresponding to the voltage required to make the band edge of n -Si flat to the SiO_2 -Si interface, ϕ_{ms} is the work function difference between the gate metal work function and the n -Si work function, q is the electronic charge, and ϵ_{ox} and d are, respectively, the permittivity and the thickness of the oxide.

To determine Q_f , we have to know V_{fb} and ϕ_{ms} , which can be obtained from the high frequency C - V characteristics. Typical high frequency C - V characteristics for the MOS devices before and after PMA with the SiO_2 deposited at substrate temperatures of 250°C and 350°C are shown in Fig. 1. From these characteristics we obtain the oxide capacitance C_{ox} , the minimum capacitance of the device C_{min} , and the flatband capacitance C_{fb} . With these known parameters we can easily calculate the donor concentration in n -Si, N_d , the thickness d and ϕ_{ms} using standard relations[8,9]. V_{fb} is the parallel shift of the C - V curve. The results of Q_f calculated from eqn (1) show that the oxide fixed charge density is in the low $10^{10} \text{ q cm}^{-2}$ and is practically independent of the substrate temperature for the substrate temperature range under this investigation. It is interesting to note

that Q_f for the thermal oxide depends strongly on the oxidation temperature[10] while Q_f in our PECVD oxide is practically independent of the substrate deposition temperature. If the ionic silicon resulting from the incomplete oxidation at the interface is the major source for Q_f [10], these results indicate that our PECVD oxide should contain little unoxidized silicon at the interface.

B. The mobile ionic charge

Using the method[11] commonly used for the determination of mobile ionic charge, we have measured the mobile ionic charge in our MOS devices. With this method a high frequency C - V characteristic of an MOS device after PMA is first measured, and then this device is heated to about 150°C to mobilize the ions and at the same time a bias of 8 V corresponding to about 1.5 MV cm^{-1} across the oxide is applied to the gate for about 30 min in order to drive all of the ions either to the SiO_2 -Si interface when the bias is positive, or to the SiO_2 -metal interface when the gate is negative. After this bias temperature aging (BTA), the device is then cooled down to the room temperature before the measurement of its C - V characteristic. The parallel shift of this C - V characteristic from that before BTA is the measure of the mobile ions drifted to the interfaces forming a charge sheet there with a density Q_m given by

$$Q_m = (V'_{fb} - V_{fb})C_{ox} \tag{2}$$

where V_{fb} and V'_{fb} are, respectively, the flatband voltages before and after BTA. Typical results are shown in Fig. 2. In general, the flatband shift is small showing that our PECVD SiO_2 films contain mobile ions in the order of $4 \times 10^{10} \text{ cm}^{-2}$. Curve 1 (prior to BTA (and curve 3 (after BTA with a positive gate bias) are almost identical indicating that the ions are of ionized alkali atoms such as sodium and potassium, and of positive charge; and that they do not

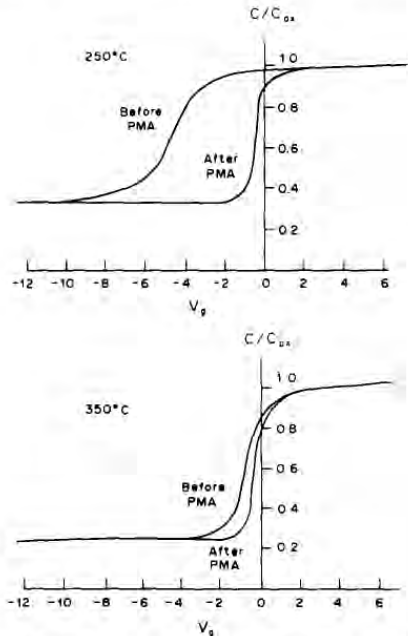


Fig. 1. Typical high frequency C - V characteristics of the PECVD SiO_2 films before and after PMA, deposited at 250°C and at 350°C .

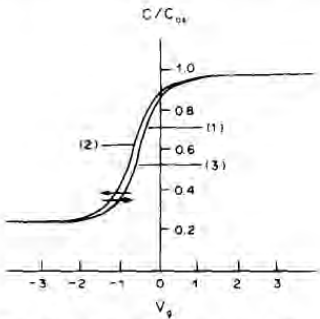


Fig. 2. The shift of the high frequency C - V curve after bias-temperature aging (BTA) for the PECVD SiO_2 deposited at 300°C . Curve (1): the initial C - V prior to BTA, curve (2): the C - V curve after BTA at 150°C and $+8 \text{ V}$ bias for 30 min, and curve (3): the C - V curve after BTA at 150°C and -8 V bias for 30 min.

exchange charge with either the gate metal or the silicon and do not become discharged even though they pile up to within a tunneling distance at the interfaces. Again, Q_m is practically independent of the substrate deposition temperature for the temperature range of 225–350°C, because the origin of such ions is mainly due to the contamination during fabrication processing such as gate or contact metallization and general handling of the substrate cleaning process, etc.

C. The interface trap density

We have found that the oxide fixed charge and the mobile ionic charge densities are small in our PECVD devices. Therefore, the shift of the C - V curves before and after PMA as shown in Fig. 1 can be considered to be mainly due to the interface trap density D_{it} and the oxide trapped charge density Q_{ot} . It is thus interesting to investigate how fast and how much these charges can be annealed out at a fixed annealing temperature and a fixed anneal time.

The high frequency and the quasi static C - V characteristics (normalized to the oxide capacitance) as shown in Fig. 3 can be used to evaluate D_{it} as a function the gate bias V_g according to the following relation[9].

$$D_{it} = \frac{C_{ox} V_g}{q} \left[\left(\frac{C_{ox}}{C_{LF}} - 1 \right)^{-1} - \left(\frac{C_{ox}}{C_{HF}} - 1 \right)^{-1} \right] \quad (3)$$

where C_{HF} and C_{LF} denote the high frequency and the low frequency (quasi static) capacitances, respectively. Normally, we want to see D_{it} as a function of energy level in the interface band gap. To convert D_{it} as a function of V_g to D_{it} as a function of $E_c - E$, we use the following relations[8]

$$E_c - E = \frac{E_g}{2} + \Psi_s - \phi_b \quad (4)$$

$$\Psi_s = \int_{V_b}^{V_g} (C_{ox} - C_{LF}) dV \quad (5)$$

where E_c is the conduction band edge energy, E_g is the band gap energy, E is the energy level in the gap, ϕ_b is the difference between the thermal equilibrium Fermi level and the intrinsic Fermi level in the silicon bulk, Ψ_s is the surface potential energy at the SiO₂-Si interface. Using an IBM computer program, we have computed and plotted D_{it} as a function of $(E_c - E)$ based on eqns (3)–(5), and from this plot we have determined the mid-gap D_{it} which is the value of D_{it} at 0.55 eV below E_c (the mid-gap based on $E_g = 1.1$ eV for Si at room temperature).

To study the anneal mechanism, we annealed our PECVD devices in two ways. The first way was that the devices were annealed at different temperatures, namely, 225, 250, 275, 300, 325 and 350°C with a fixed anneal time of 30 min. The second way was that the devices were annealed at a fixed temperature of 400°C but with different anneal times, namely, 10, 30,

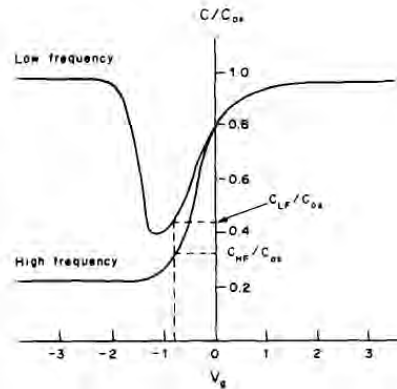
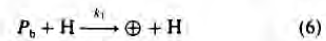


Fig. 3. The high and low frequency C - V characteristics for determination of D_{it} .

100, 1000 and 1800 s. At least 4 MOS devices were selected for each annealing temperature and for each substrate deposition temperature. Although it was found that the anneal time could be accumulated[7], we used a new set of devices (at least 4 per set) for each anneal time to avoid any possible errors. After annealing the devices were allowed to cool down to room temperature prior to the high frequency and the quasi static C - V measurements.

To model the defect annealing chemistry we have used models developed by Reed and Plummer[7]. On the basis of the nonconsumptive two reaction models put forward by Reed and Plummer[7], the dimerization of hydrogen occurs in the bulk of the oxide but hydrogen is not consumed during annealing. The two reactions can be described by



and the corresponding differential equations are

$$\frac{d}{dt} [Si^*] = -k_1 [Si^*][H] \quad (8)$$

$$\frac{d}{dt} [H] = -2k_2 [H]^2 \quad (9)$$

where P_b is the interface trap centre before anneal, $\oplus$ is the annealed P_b , and k_1 and k_2 are the reaction rate constants, $[Si^*]$ and $[H]$ are, respectively, the concentrations of the trivalently bonded silicon atoms and the hydrogen atoms at the SiO₂-Si interface. The solution of eqns (8) and (9) gives

$$[Si^*] = \frac{[Si^*]_0}{\{1 + 2k_2 [H]_0 t\}^n} \quad (10)$$

where $[Si^*]_0$ and $[H]_0$ are, respectively, the initial concentration of the trivalently bonded silicon atoms

and the hydrogen atoms at the SiO₂-Si interface. t is the anneal time, and

$$n = k_1/2k_2 \quad (11)$$

$$k_1 = 2\pi\rho_1 D_H \quad (12)$$

$$k_2 = 4\pi\rho_2 D_H \quad (13)$$

in which D_H is the diffusion coefficient of the hydrogen atoms, which can be expressed as

$$D_H = D_0 \exp(-E_H/kT) \quad (14)$$

and ρ_1 and ρ_2 are the reaction radii which are given by

$$\rho_1 = r_a + r_H \quad (15)$$

$$\rho_2 = 2r_H \quad (16)$$

where D_0 is the diffusion coefficient for $T = 0$ K which is $1 \times 10^{-5} \text{ cm}^2 \text{ s}^{-1}$. E_H is the activation energy for diffusion which is about 0.75 eV [12]. r_H and r_a are, respectively, the radius of a hydrogen atom which is about 0.5 Å and the capture radius of an interface trap which is not known. By assuming that r_a is at least equal to the silicon tetrahedral radius which is 1.2 Å and possibly up to 50% larger, then we have [7]

$$0.4 < n < 0.58. \quad (17)$$

The value of $[H]_0$ depends very much on the reaction between the gate aluminum and traces of water [12], the oxide thickness, and the amount of OH groups available. On the following assumptions: (i) the amount of OH groups is sufficient for reaction (ii) the gate aluminum reacts efficiently with OH within the range of temperatures under this investigation, and (iii) the transport of atomic hydrogen through the oxide is not rate-limited, $[H]_0$ can be estimated by [7]

$$[H]_0 = N_{OH} \exp(-E_R/kT) \quad (18)$$

where N_{OH} is the number of OH groups on the SiO₂ surface which is estimated [7] to be $1.67 \times 10^{23} \text{ cm}^{-2}$, and E_R is the activation energy for reaction which is 0.46 eV.

Substituting eqns (13), (14) and (18) into eqn (10) with $E_H = 0.75 \text{ eV}$, $E_R = 0.46 \text{ eV}$, $N_{OH} = 1.67 \times 10^{23} \text{ cm}^{-2}$ and $D_0 = 1 \times 10^{-5} \text{ cm}^2 \text{ s}^{-1}$, we obtain

$$[Si^*] = [Si^*]_0 (4.2 \times 10^{12} t)^{-n} \exp(-nE_a/kT) \quad (19)$$

where $E_a = E_H + E_R = 1.21 \text{ eV}$. If the interface traps are mainly the trivalently bonded silicon atoms, then we can consider $D_H = [Si^*]$.

C.1. Annealing temperature dependence of D_H . By letting $t = 30 \text{ min} = 1800 \text{ s}$, eqn (19) becomes:

$$D_H = [Si^*] = [Si^*]_0 (7.5 \times 10^{14})^{-n} \exp(-nE_a/kT). \quad (20)$$

This is the equation to show how D_H depends on the annealing temperature T . There are two unknown parameters, $[Si^*]_0$ and n in eqn (20). Using a computer plotting program, we have tried to perform curve fitting based on eqn (20) to our experimental data. We first chose one value of n and used various values

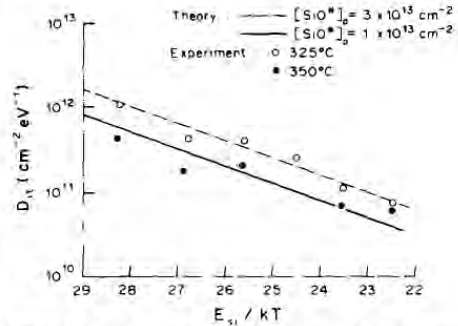


Fig. 4. Midgap D_H as a function of annealing temperature for a fixed time of 1800 s for the PECVD SiO₂ films deposited at 325°C and 350°C. Curve fitting based on eqn (20) with $n = 0.81$ and $[Si^*]_0 = 3 \times 10^{13} \text{ cm}^{-2}$ for films deposited at 325°C and $[Si^*]_0 = 1 \times 10^{13} \text{ cm}^{-2}$ for films deposited at 350°C.

of $[Si^*]_0$ to compute D_H as a function of T . This computing process was repeated with other values of n within the range of 0.43–0.58, until the best fit was obtained for all MOS devices with the SiO₂ deposited at six different substrate temperatures. Figure 4 shows typical $D_H - E_a/kT$ characteristics of the SiO₂ deposited at substrate temperatures of 325°C and 350°C. With $n = 0.51$, our experimental data for all six substrate temperatures fit well to eqn (20) if a value of $[Si^*]_0$ within the range from 1×10^{13} to $5 \times 10^{13} \text{ cm}^{-2}$ is chosen.

The value of n obtained in our work is in good agreement with the value of 0.55 reported by Reed and Plummer [7]. Our results strongly support the two reaction models from another angle because Reed and Plummer are mainly concerned with the time parameter while we have arrived at the same results from a temperature parameter. This implies that eqn (20) can actually describe the anneal chemistry of the interface traps. However, one might argue that the oxides used by Reed and Plummer are different from ours and the comparison may be questionable.

C.2. Anneal time dependence of D_H . By letting $T = 673 \text{ K}$, eqn (19) becomes

$$D_H = [Si^*] = [Si^*]_0 (371t)^{-n}. \quad (21)$$

Again, with $n = 0.51$ our experimental data for all six substrate temperatures fit well to eqn (21) with $[Si^*]_0$ of the order 10^{13} cm^{-2} . Typical $D_H - t$ characteristics for the SiO₂ deposited at substrate temperatures of 325°C and 350°C are shown in Fig. 5. These results are also consistent with the results shown in Fig. 4 supporting the validity of the two reaction models for our PECVD SiO₂ films.

The index n from this work is less than that of Reed and Plummer by less than 10%. We cannot say that the radius of the interface trap center in our PECVD SiO₂ films is smaller than that in the thermal oxide. As a matter of fact, there is no good reason why the interface traps of these two kinds of oxides are

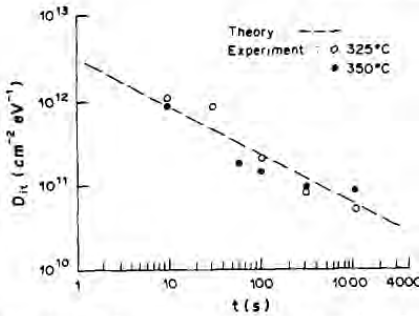


Fig. 5. Midgap D_{it} as a function of anneal time for a fixed annealing temperature of 400°C for the PECVD SiO₂ films deposited at 325°C and 350°C. Curve fitting based on eqn (21) with $n = 0.51$ and $[Si^*]_0 = 1 \times 10^{13} \text{ cm}^{-2}$.

different. Of course, one may argue that the difference is due to the growing temperature which could make the silicon surface of the thermal oxide expand to a greater extent. However, on the basis of our work we can only conclude that there is no detectable difference in the interface traps between the PECVD oxide and the thermal oxide.

In terms of interface traps the major difference between the PECVD oxide and the thermal oxide is the initial amount of interface traps. The PECVD oxide which is deposited at low temperatures is subjected to a certain degree of random bonding. This randomness no doubt creates a large amount of unbonded silicon atoms which make the value of D_{it} for the as-deposited SiO₂ films higher than that of the thermal oxide. However, these interface traps can be reduced to an acceptable level simply by a low temperature anneal.

D. The oxide trapped charge

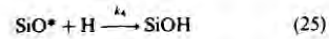
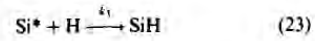
We use the same $C-V$ curves obtained for the devices annealed at the temperature range from 225°C to 350°C for 1800 s, and annealed at 400°C for the anneal time from 10 to 1800 s as described in the previous subsection for the analysis of the oxide trapped charge. But this time we are interested only in the shift of the high frequency $C-V$ curves.

We use the midgap voltage method[13,14] for the present analysis. We first have to locate the gate bias V_{mg} corresponding to the midgap energy level using eqns (4) and (5), and then translate the ideal $C-V$ curve along the voltage axis until the two curves meet at V_{mg} as shown in Fig. 6. We use the $C-V$ curve after PMA shown in Fig. 1 as the ideal $C-V$ curve because the oxide fixed charge is negligibly small. The flat-band shift V_{fb} given by the ideal $C-V$ curve consists of a voltage shift due to ϕ_{ms} , Q_f and Q_{ot} . Thus the oxide trapped charge density Q_{ot} can be expressed as

$$Q_{ot} = \frac{2\epsilon_{ox}}{d^2} \left(V_{fb} - \frac{dQ_f}{\epsilon_{ox}} - \frac{\phi_{ms}}{q} \right). \quad (22)$$

The possible candidates for positive oxide trapped

charges are trivalent silicon and E' center-like defects. Since trivalent silicon is likely to exist at the interface and E' center is very much associated with plasma chemistry, we believe that E' center-like defects are the major source of positive charge. On the other hand, the only possible defect that may create negative trapped charge is the nonbridging oxygen which is again very much related to plasma chemistry. Since we have assumed that the transport of atomic hydrogen through oxide is not the rate limiting step in annealing the MOS devices, the anneal chemistry of bulk defects and interface traps would be considered similar. Therefore, we shall again use the two reaction models to analyze the bulk defects in the anneal experiment. By assuming that the two bulk defects during anneal take on the nonconsumptive reaction process, then the reactions may be written as



The corresponding differential equations are

$$\frac{d}{dt} [Si^*] = -k_1 [Si^*][H] \quad (27)$$

$$\frac{d}{dt} [H] = -k_2 [Si^*][H] - 2k_3 [H]^2 \quad (28)$$

$$\frac{d}{dt} [SiO^*] = -k_4 [SiO^*][H] \quad (29)$$

$$\frac{d}{dt} [H] = -k_2 [SiO^*][H] - 2k_4 [H]^2 \quad (30)$$

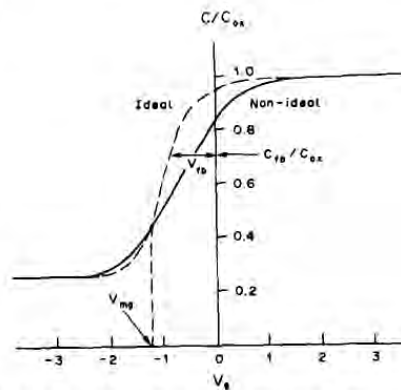


Fig. 6. The midgap voltage method for the determination of V_{fb} .

For simplicity, we assume that $[H]$ is large enough so that the first term of eqns (28) and (30) can be neglected. This results in the nonconsumptive case. Thus the solution of eqns (27)–(30) gives

$$[Si^*] = \frac{[Si^*]_0}{\{1 + 2k_2[H]_0 t\}^{n_1}} \tag{31}$$

which is similar to eqn (10), and

$$[SiO^*] = \frac{[SiO^*]_0}{\{1 + 2k_2[H]_0 t\}^{n_2}} \tag{32}$$

Using the same method for estimating n in Section 3C, we obtain the ranges of n_1 and n_2 as follows:

$$0.41 < n_1 < 0.69 \tag{33}$$

$$0.29 < n_2 < 0.43. \tag{34}$$

D.1. Annealing temperature dependence of Q_{ot} . By letting $t = 1800$ s, we can obtain the net oxide trapped charge Q_{ot} as a function of annealing temperature T , which is the difference of eqns (31) and (32). Thus we can write

$$Q_{ot} = N^+ (7.5 \times 10^{14})^{-n_1} \exp(-n_1 E_a/kT) - N^- (7.5 \times 10^{14})^{-n_2} \exp(-n_2 E_a/kT) \tag{35}$$

where N^+ and N^- denote the initial contents of the positive charge (i.e. $[Si^*]_0$) and the negative charge (i.e. $[SiO^*]_0$), respectively. There are four undetermined parameters in eqn (35) which make it difficult to visualize the shape of the curves. Worse still, it is not easy to curve fit to our data because they involve both the positive and the negative quantities. However, eqn (35) does predict the relative magnitude of N^+ and N^- , and n_1 and n_2 .

We know that the net oxide trapped charge for the as-deposited SiO_2 films before anneal is positive, i.e. N^+ is greater than N^- in all cases. And from eqns (33) and (34), n_1 is always greater n_2 . A plot of Q_{ot} as a function of E_a/kT as shown in Fig. 7 with $n_1 = 0.60$, $n_2 = 0.36$ and $N^+ > N^-$ fits well to our data. Curves based on $n_1 < n_2$ and $N^+ < N^-$ deviate from our data. However, the two reaction model does predict, to a certain extent, the correct trend of our data

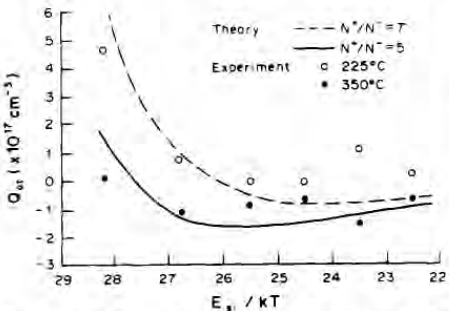


Fig. 7. Q_{ot} as a function of annealing temperature T for a fixed anneal time $t = 1800$ s, with $n_1 = 0.60$ and $n_2 = 0.36$ and various N^+/N^- ratios.

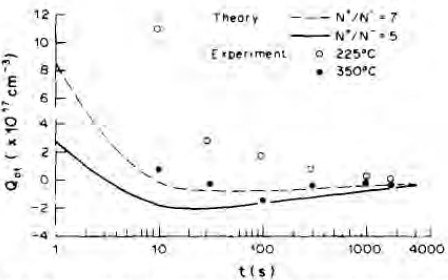


Fig. 8. Q_{ot} as a function of anneal time t for a fixed annealing temperature $T = 637$ K with $n_1 = 0.60$ and $n_2 = 0.36$ and various N^+/N^- ratios.

though a precise description of the contents of the positive and negative charges is not possible.

D.2. Anneal time dependence of Q_{ot} . With $T = 673^\circ\text{C}$ we can express the net oxide trapped charge as a function of anneal time as

$$Q_{ot} = N^+ (371t)^{-n_1} - N^- (371t)^{-n_2}. \tag{36}$$

Again, a plot of Q_{ot} as a function of anneal time t with $n_1 = 0.60$, $n_2 = 0.36$ and $N^+ > N^-$ as shown in Fig. 8 fit to our data reasonably well. The not so distinct turn-round phenomenon in this case as compared with the previous case based on eqn (35) is due to the difference between the exponential function and the power function.

The major difficulty in the analysis is the mixing of the positive and the negative charges inside the bulk. We can determine only the net charge from the $C-V$ analysis, but we are unable to find the actual amounts of the positive and the negative charges. An E' center-like defect which may be a deficit of an oxygen atom could capture an oxygen atom, if available, instead of a hydrogen for passivation. The possibility of this mechanism has been discussed by Reed and Plummer[7]. The nonbridging oxygen, on the other hand, might not form a hydroxyl group with hydrogen because its stability is doubtful. Instead, the bond rearrangement between the oxygen and neighboring silicon is more probable alternative. Again, this mechanism does not consume any hydrogen at the end. All of these propositions, no doubt, will require further research for verification.

In terms of bulk trapped charge, the PECVD SiO_2 film contains in general a higher concentration of negative trapped charge than the thermal oxide. This may be attributed to a higher concentration of non-bridging oxygen defects because the random bonding of the plasma species has a higher chance of missing their neighboring atoms, thus creating a large amount of unbonded oxygen.

It should be noted that the conventional bimolecular one reaction model[7] and the simple hydrogen molecular diffusion model[5] have also been studied but they fail to fit our experimental data. The solution of the two reaction model is different from the

solutions of the other models in that the former contains a temperature-independent index n . The results given in Sections 3C and 3D indicate clearly that n is indeed independent of temperature. Therefore, we can conclude that the two reaction model is an appropriate model for the description of the anneal chemistry of MOS devices.

Recently, some exciting work has shown that the oxide trapped charge in the PECVD films cannot be correlated with the E' center[15]. The above defects have annealing behavior that can be explained in some respects by the E' center but are not E' centers. This leaves much further work to be done in the identification of these defects.

It should also be noted that all the SiO₂ films under this investigation were stoichiometric with hydrogen concentration less than 1 at % based on our Rutherford back scattering spectroscopy and IR absorption results, and that hydrogen was mainly incorporated as Si-OH, no Si-H presence being detected[1]. The bulk traps in SiO₂ films are known to be related to hydrogen or water incorporation[16], but they can be reduced by a proper anneal. However, in terms of electrical integrity the PECVD films are as good as the high quality thermal oxide, but in other properties they are different, such as the etch rate and the Si-O stretching frequency. The present experimental work does not provide information about the factors responsible for this difference. We would believe that due to the quite different fabrication processes the two kinds of films would be different in local bonding structure, void content as well as film stress.

4. CONCLUSIONS

On the basis of our study described above, the following conclusions are drawn:

- (1) The r.f. PECVD SiO₂ films contain only small amounts of oxide fixed charge and mobile ionic charge, both charges being in the low 10^{10} q cm⁻² level. The concentration of both charges after PMA is practically independent of the substrate deposition temperature in the temperature range of 225–350°C, and their presence does not affect the content of the interface traps and the oxide trapped charge.
- (2) The interface trap density is around 10^{12} cm⁻² eV⁻¹ before PMA and is reduced to the mid- 10^{10} cm⁻² eV⁻¹ level after PMA. There is no detectable difference in interface traps between the r.f. PECVD oxide and the thermal oxide in terms of annealing kinetics.
- (3) The concentrations of the positive and the negative oxide trapped charges are of the order of 10^{17} q cm⁻³ before PMA but they can be reduced to an acceptable level after PMA. The positive oxide trapped charge may be associated with the oxygen vacancy, while the negative oxide trapped charge with the nonbridging oxygen.
- (4) The two reaction model can explain well the annealing processes for interface traps and oxide bulk traps. As the oxide trapped charge consists of both the positive and the negative charges, it is not possible to determine the actual concentrations of these two kinds of charges.

Acknowledgements—We wish to thank the Natural Sciences and Engineering Research Council of Canada for supporting this research, the IBM Thomas Watson Research Center for supplying the SiO₂ samples for this investigation, and Drs D.A. Buchanan and P. Wagner for their helpful discussions.

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Solid-state electronics

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https://catalog.lindahall.org/discovery/fulldisplay?docid=alma992683223405961&context=L&vid=01LINDAHALL_INST:LHL&lang=en&search_scope=MyInstitution&adaptor=Local%20Search%20Engine&tab=LibraryCatalog&query=any,contains,solid%20state%20electronics&mode=simple&offset=0

The screenshot displays the OPAC interface for the journal "Solid-state electronics". At the top, a book icon is next to the text "JOURNAL Solid-state electronics 1960". Below this, a status bar indicates "Available at Linda Hall Library Closed Stacks - Serials (Solid-state electronics,) and other locations". A sidebar on the left contains navigation links: "Top", "Send to", "Get It", "Details", "Virtual Browse", and "Links". The "Send to" section includes icons for Email, QR, Permalink, Citation, EasyBib, Export RIS, and Export to Excel. The "Get It" section is currently selected, showing a "LOCATIONS" list. This list contains two entries for "Linda Hall Library": one for "Closed Stacks - Serials" with holdings from 1960 to 1996 and a note about the annual index, and another for "Compact Storage Microfilm" with holdings from 1978 to 1985. Each entry has a "Go to Location Items" link.

JOURNAL
Solid-state electronics
1960

Available at Linda Hall Library Closed Stacks - Serials (Solid-state electronics,) and other locations

Top
Send to
Get It
Details
Virtual Browse
Links

Send to

Email QR Permalink Citation EasyBib Export RIS Export to Excel

Get It

LOCATIONS

Linda Hall Library
Available , Closed Stacks - Serials ; Solid-state electronics.
Holdings: v.1(1960)-v.39(1996); v.40:n.1-8(1996);...
Note: Annual index in last issue of volume.1997 received separately.
[View more](#)
[Go to Location Items](#)

Linda Hall Library
Available , Closed Stacks - Compact Storage Microfilm
Holdings: Vol. 21-28 (1978-1985)
[Go to Location Items](#)

Screen capture created by J L Mullins from Linda Hall Library OPAC on October 17, 2025 at URL:

https://catalog.lindahall.org/discovery/fulldisplay?docid=alma992683223405961&context=L&vid=01LINDAHALL_INST:LHL&lang=en&search_scope=MyInstitution&adaptor=Local%20Search%20Engine&tab=LibraryCatalog&query=any,contains,solid%20state%20electronics&mode=simple&offset=0

Details	
Title	Solid-state electronics
Other title	Solid-state electron. Solid-state electronics Solid state electronics Applied superconductivity.
Subjects	Semiconductors >
Identifier	ISSN : 0038-1101 OCLC : (OCoLC)1765978
Related title	Later title : Applied superconductivity. > Later title : Materials science in semiconductor processing. >
Publisher	Oxford, New York, Pergamon Press. v. 1- Mar. 1960-
Creation date	1960
Format	v. ill., diagrs. 25 cm.
Frequency	Monthly, <Nov. 1975->
General notes	May and October 1998 include a section, Materials science in semiconductor processing, vol. 1, no. 1-2; v.1, no.3- published separately, which see for Library's holdings. Editor: Mar. 1960-<Nov. 1975> W.C. Crawford.
Citations/References	Applied science & technology index, Computer & control abstracts, Electrical & electronics abstracts, Physics abstracts, Chemical abstracts, Engineering index annual (1968), Engineering index bioengineering abstracts, Engineering index energy abstracts, Engineering index monthly (1984), International aerospace abstracts, Engineering index monthly, Nuclear science abstracts,