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NOVEL METHODE FOR PREPARATION OF INTERDIGITATED BACK CONTACTED a-Si:H/c-Si HETEROJUNCTION SOLAR CELLS

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ABSTRACT: We present a **novel method for structuring** Emitter and BSF areas **of interdigitated back contacted silicon heterojunction solar cells** (IBC-HJ). The **method combines** the **benefits of in-line capability** with **vacuum processes only**, **reusable masks**, **self alignment** and furthermore an easy and **extreme safe wafer handling**. It is based on plasma etching of passivation layers and a following layer deposition procedure via openings in a **mechanical masking**. The exceptional way how the reusable masks are attached to the sample provides accurate masking over large area. By overlaying two masks the wafer can remain underneath the lower masking, which also works as a sample holder during all the structuring steps while, if necessary, the upper mask is exchanged for each particular process step. This provides an **extreme safe wafer handling** along all the IBC-HJ specific process steps, highly recommended **for very thin wafers**. This allows processing the different layers (e.g. emitter, BSF, TCO, metal) structures without the need to touch the wafer after each step. Furthermore a **mechanical self aligning** of the mask-stacks can be applied in mass production. First test structures are shown and cost estimation for IBC-HJ solar cells is presented.
Keywords: heterojunction, IBC, a-Si/c-Si

1 Introduction

IBC-HJ solar cells have a very high efficiency potential of more than 24% on p-type [1]. and more than 25% on n-type, respectively [2]. They combine the most efficient silicon solar cell technologies available on the market, namely the interdigitated back contacted back junction solar cell known from SUNPOWER and the HIT solar cell from SANYO. The IBC-HJ cell structure consists of a contactless and well passivated front side with any kind of light capturing features. On the back side the highly diffused emitter and BSF areas are substituted by the amorphous/crystalline silicon (*a*-Si:H/*c*-Si) heterojunction contact structures (figure 1), which are deposited at temperatures of less than 200°C. These *a*-Si:H/*c*-Si structures are very low recombinative and cause the very high voltages potential of these kind of cell. During the last years a rapid efficiency increase with an actual maximum of 20,2% [3] and 22,2% [10] is observed. Different approaches how to structure the emitter and base contacts of silicon heterojunction (HJ) contact patterns on the cell rear side are known: a) with photolithography like in [1] or like in the RECASH or PRECASH method [5], b) with screen printing a resist plus etching steps [6], c) by putting a hard mask on the sample like in the BEHIND procedure [7], or by using a hard mask in small distance to the sample [8].

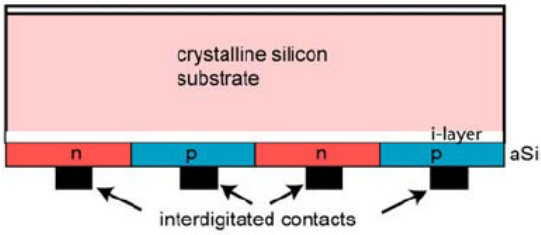

Figure 1: Side cut of a common IBC-HJ solar cell [4].

The first two production methods (a, b) suffer from the unpleasant procedures like depositing and hardening plus in the case of photolithography illuminating and developing a resist, as well as etching of the uncovered areas and wet chemically removing the resist. All these steps are associated to unfortunate handling steps and switching between in-line and batch procedures. This kind of processing is expensive and rather uncomfortable for very thin substrates (e.g. 100µm thickness). Furthermore, wet chemical residuals have to be carefully removed from the wafer surface since they would be located in the very sensitive space charge region of the heterojunction contacts and would strongly reduce the performance of the final device. All these aspects are cost effective.

The BEHIND concept benefits from the cheap and reusable mask as well as form the high V_{OC} potential (695mV) due to the full area emitter deposition in the beginning of the procedure [5]. On the other hand it suffers from accurate mask adjustment after the first structuring step. Furthermore in mass production a hard mask tends to mechanically damage the thin underlying passivation or heterojunction layers due to local mechanical contact. Also problems can appear due to plasma penetration below the mask if the sample or the mask is not flat or deformed by continuous use. Later on in figure 5 a comparable process flow (BEHIND-like) is presented, which uses the stacked masks and the novel method with foils.

The mentioned problem of plasma penetration below the mask turns up extremely by keeping the mask in small distance to the sample like presented in [8]. The effect is very sensitive to the applied distance and does not allow exact structuring as penetration of the plasma below the mask appears everywhere and is detrimental to the cell performance.

2 Cell processing using the novel method:

The new approach combines the benefits of in-line capability with vacuum processes only, reusable masks, self alignment plus easy and save wafer handling. It is based on a plasma etching and layer deposition procedure via openings in stacks of mechanical masks. The procedure how the reusable masks are attached to the sample provides accurate masking over large areas. By using this thin films instead of thick hard masks surface damage is avoided, especially if the film is soft or a soft coat is applied. Furthermore plasma penetration below the mask, due to incomplete proximity of the mask to the wafer, is avoided. This proximity is achieved by using a non-planar holder with a curved surface, on which the

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cell precursor is bended by pressing the tensed mask onto it.

In the following three different kinds of samples and an exemplary process flow are presented. First *a*-Si:H structures which were deposited and etched via one mask. Then transparent conductive oxide (TCO) layers are deposited via this mask. Afterwards an exemplary process flow is presented and finally a structure is shown, which uses a stack of masks, where the upper masks are exchanged for emitter and BSF structures, respectively.

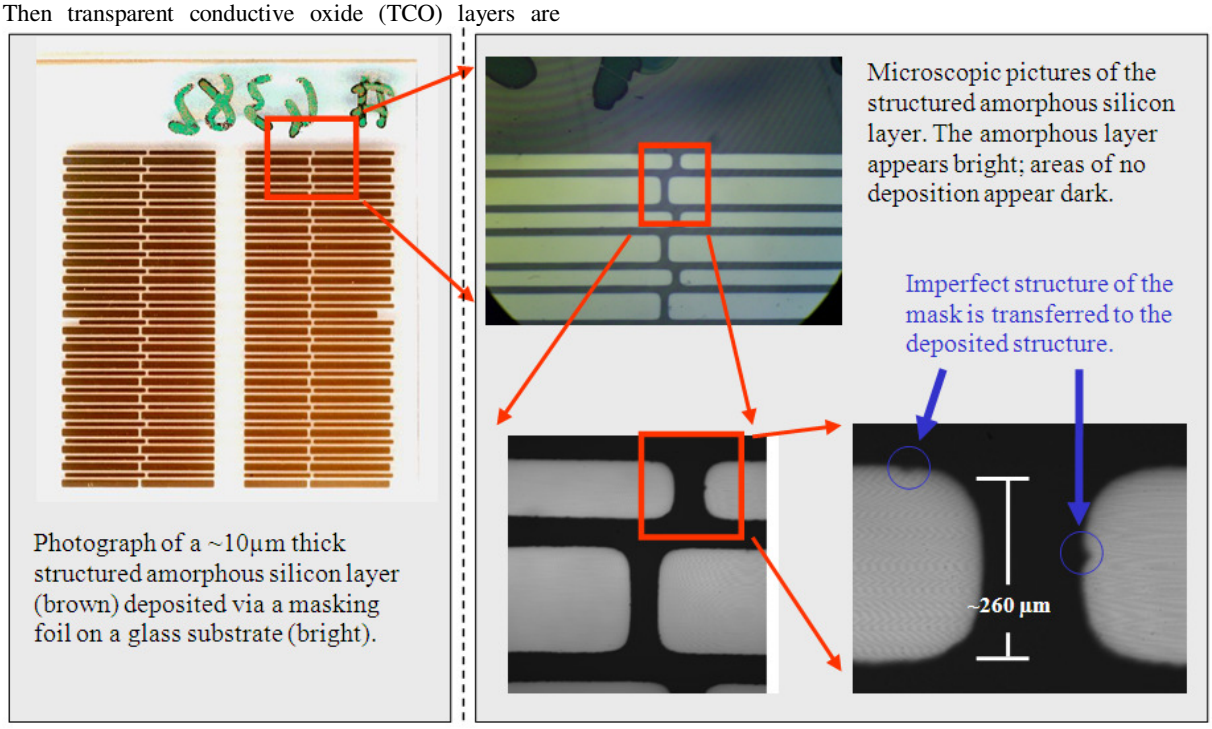

Figure 2: Structured *a*-Si:H layer deposited through a flexible mask according to the novel method.

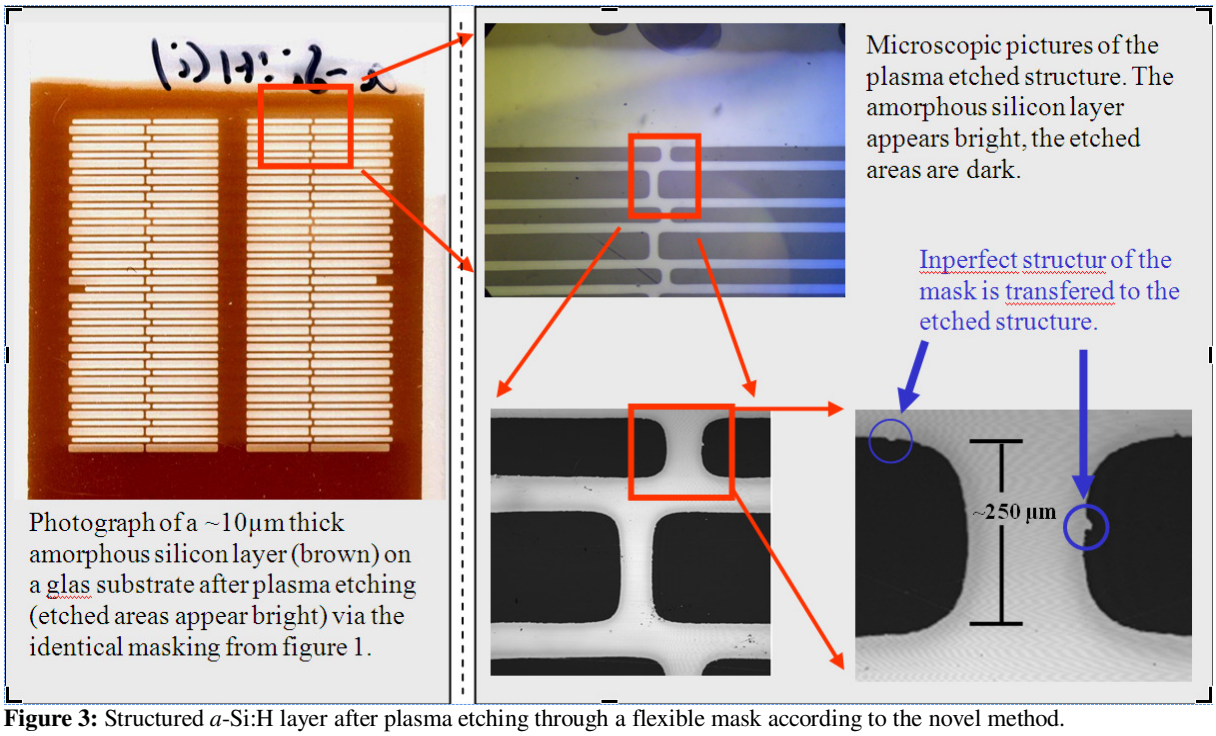

Figure 3: Structured *a*-Si:H layer after plasma etching through a flexible mask according to the novel method.

2.1 Test sample using one mask

As test sample a ~10µm thick amorphous silicon layers is shown, which was deposited through openings in a flexible mask onto a glass substrate according to the novel method (in figure 2). The *a*-Si:H was deposited in a standard parallel plate PECVD setup at an excitation frequency of 13.56MHz. Due to the absorption of the *a*-Si:H in the wavelength range up to 600nm the layer appears brown. Even very thin layers are easily visible. The abrupt borderline is visible, which even properly transfers imperfections of the mask openings to the deposited layer structure (lower right picture in figure 2).

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Furthermore no parasitic deposition can be observed all over the sample area. Please note that the thickness of the used amorphous layers is three orders of magnitude thicker than used in a-Si:H/c-Si structures.

In figure 3 first a ~10µm thick full area amorphous silicon layer was deposited on a glass. Afterwards plasma etching was applied through openings of the identical flexible mask used above. Once more one can see the abrupt borderline which perfectly transfers the imperfections of the mask openings to the etched layer structure (lower right picture in figure 2). No parasitic etching is observed all over the sample area.

The width of the deposited and etched test structures are ~250µm and ~450µm with a pitch of 1mm. These dimensions are more than adequate for IBC solar cells.

To have an idea of the steepness of the edges at the borderline of the prepared structures two 3D scans were prepared with a confocal microscope. As shown in figure 4 (left) the shape of the plasma etched step is perfectly perpendicular with no any rounding of the edge neither under etching of the mask. Furthermore the deposited *a*-Si:H layer (right) shows a well defined structure with slightly rounded edges.

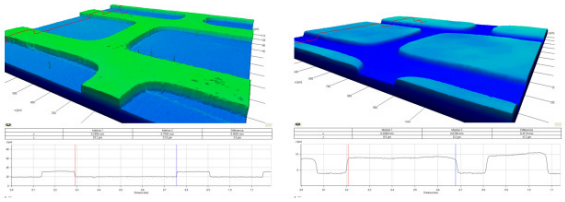

Figure 4: Topographies of the structured deposited *a*-Si:H layers shown in figure 1 (right) and etched *a*-Si:H layer after plasma etching from figure 2 (left) prepared by a confocal microscope.

2.2 TCO deposited via the mask

Usually the thin silicon layers of a-Si:H/c-Si HJ structures are covered with TCO to provide an anti reflection coating, and low ohmic contacts to the metallization, for light confinement, and to increase the lateral conductivity of the layer stack. In figure 4 80nm of indium tin oxide (standard used TCO) was deposited through the flexible mask onto a silicon wafer. Once more the shape of the mask is well defined and no any parasitic deposition occurs.

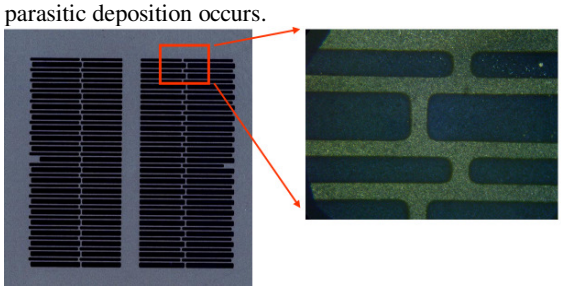

Figure 4: Photograph (left) and microscopic picture (right) of a ~80nm thick structured indium tin oxid (ITO) layer (dark/blue) deposited via a masking foil on a silicon wafer (grey).

2.3 Novel method using two stacked masks

By overlaying two masks the wafer can remain underneath the lower mask (blue mask in figure 5), which provides all the openings used in the two different upper masks (grey and brown in figure 5). During the complete process flow the upper masks are exchanged while the lower mask stays unmoved. In this example (figure 5) a BEHIND-like process flow is used in which two upper masks, for producing the BSF layer and the TCO, are involved. This technique allows processing the different structures without the need to touch the wafer after each step and consequently provides an extreme save wafer handling during all IBC-HJ specific process steps, what is highly recommended for very thin substrates of future technologies. Please note, that with the BEHIND process 695mV and high parallel resistances were archived.

2.4 Cell precursor with dielectric rear side

One sample prepared with this technology but with a different process flow to figure 5 is shown in figure 6. An oxidized (100nm) wafer was covered by two stacked masks, then local areas were opened and the first HJ layer stack was deposited (e.g. the emitter). Afterwards the upper mask was exchanged and the second HJ layer stack

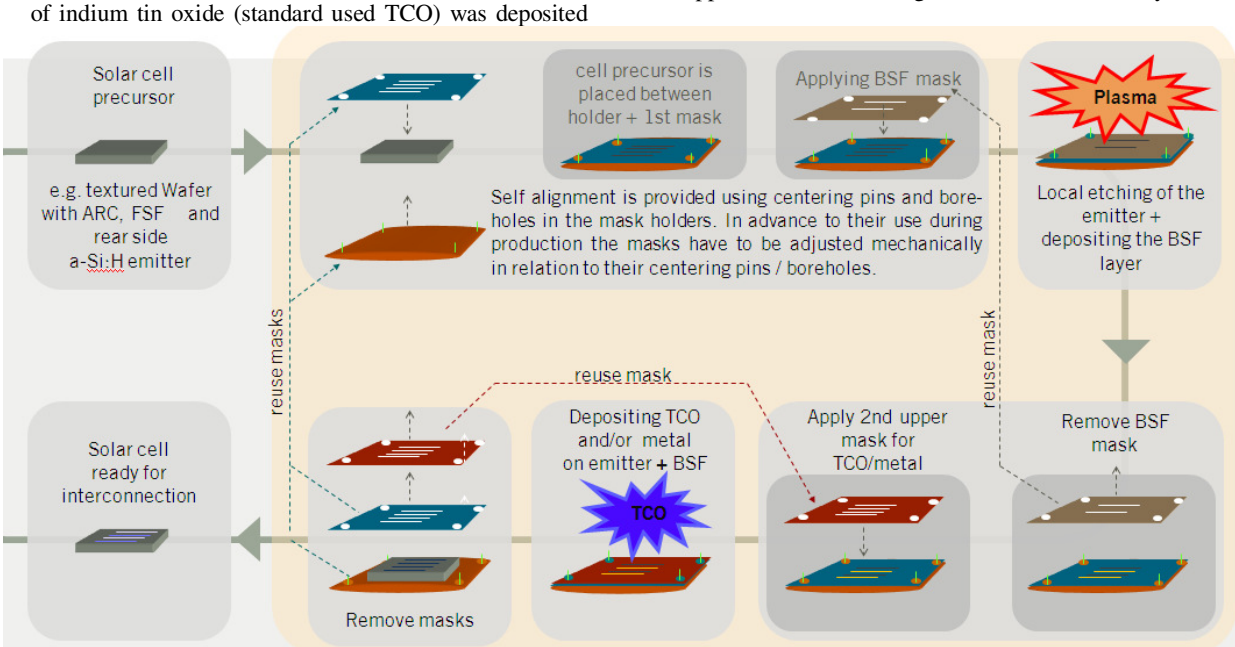

Figure 5: Example of one possible process flow using a BEHIND-like [5] procedure to prepare the structured *a*-Si:H layers.

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(e.g. the BSF) was deposited into the prior plasma etched openings. A well defined IBC structure is produced, which congruence is sufficient for this kind of cell type anyway.

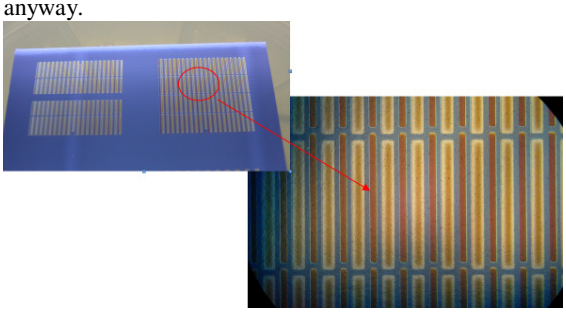

Figure 6: Photograph (left) and microscopic picture (right) of an oxidized silicon wafer after separate plasma etching the oxide and subsequent depositing of amorphous layers. Two stacked masks were used.

2.5 Self alignments of stacked masks

The processing procedure can be provided with a self aligning of the mask-stacks in mass production. Thus during the process flow the lower mask keeps it position relatively to the sample, only the position of the upper mask relative to the lower mask have to be adjusted.

This adjustment can be applied mechanically by using centering pins and boreholes in the mask holders (frame which holds the flexible mask). In advance to their use during the production process the masks have to be adjusted mechanically in relation to their centering pins and boreholes, respectively. In the production process the masks are adjusted automatically when they are put on the centering pins. This procedure provides sufficient accuracy.

3 Process cost estimation

The cost estimation for the specific process steps of the novel method is based on a multiple 100MW mass production for 6" wafers and a depreciation time for equipment of 5 years as well as for building and infrastructure etc. of 10 years.

The costs are calculated by using a Cost of Ownership (CoO) tool which has been developed at Q-Cells and is originally used for comparing process equipment of different suppliers for the same process step. It is a Windows-Excel based calculation which considers not only the equipment investment but also all aspects of a later date usage. Labor and maintenance costs are involved as well as operation materials and consumables. One result of the calculation is the overall equipment efficiency since the tool determines the net capacity of the equipment. This net capacity has a relevant influence on the wafer costs. As result the specific costs per wafer for a certain process step and equipment are obtained.

The exemplary CoO estimation is based on the process flow of figure 6 and starts with n-type silicon cell precursor with optical and electrical optimized front side (e.g. front surface field, front side silicon surface passivation, anti reflective coating). The deposition of the amorphous silicon emitter on the back side including an adequate wet chemical cleaning step previous to the layer depositions is calculated to 10,6 ct per 6" wafer (wa). The structured plasma etching followed by the HJ-BSF deposition is 14,4 ct/wa (figure 8) and the final TCO and/or metal deposition (in sum ~75nm) is estimated to 10,9 ct/wa. All this costs are distributed like presented in figure 9. The cost drivers are the estimated invest and the estimated reduced throughput due to prolonged vacuum pump down. In sum the process cost for the complete procedure excluding cost for preparing the precursor is 36,3 ct/wafer. As the cells bear of highly conductive metallisation the current collection should be shifted to the cell interconnection level e.g. like described in Patent DE 102008043833 A1.

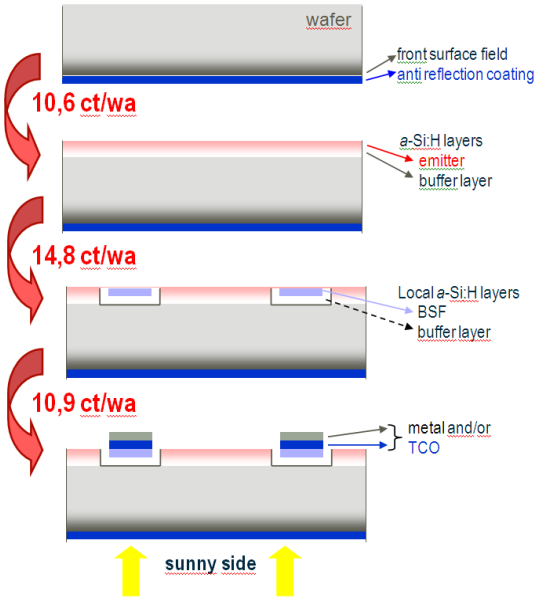

Figure 8: Estimated cost per wafer for IBC-HJ solar cells produced according to the flow of figure 5.

The CoO is based on equipment cost of 2009, is calculated for a first pilot production line and excludes further cost reduction potentials. Furthermore the net capacity can be improved. Due to this the expected process cost will be significantly lower.

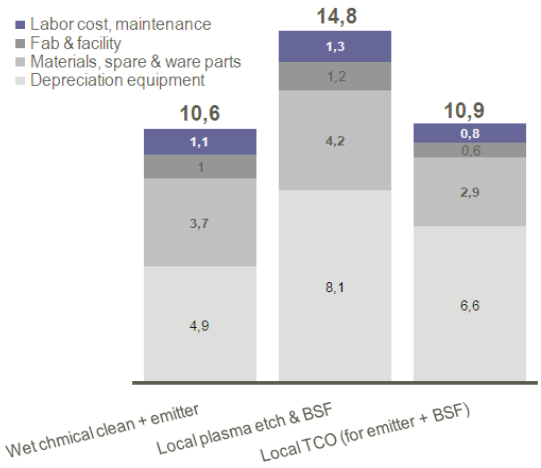

Figure 9: Cost distribution for the process flow of figure 5 excluding cost for preparing the cell precursor.

4 Conclusion

A new technique for preparing IBC-HJ solar cells is presented. Instead of lithographical processes it works with reusable masks or stacks of masks. These are softly

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attached to the sample surface in an exceptional way, which guarantees a dense proximity over large areas. By using stacks of masks an extreme save wafer handling for very thin wafers without touching the samples after each step is guaranteed and easy mechanical self aligning can be provided. The cell process cost are estimated to 36,3 ct/wa for the specific processes.
This technology is subject of the international patent family [10]. Q-Cells offer non-exclusive licenses to potentially interested companies. For more information please contact:
r.paugstadt@q-cells.com (licening),
m.scherff@q-cells.com (tecnical information)

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