

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

RUNERGY USA INC. AND RUNERGY ALABAMA INC.

Petitioners,¹

v.

TRINA SOLAR CO., LTD.

Patent Owner.

Patent No. 9,722,104

Issued: August 1, 2017

Filed: November 27, 2015

Inventor: Jungmin Ha, *et al.*

Title: Solar Cell and Method for Manufacturing the Same

Inter Partes Review No. IPR2025-00007

**SUPPLEMENTAL DECLARATION OF SANJAY BANERJEE
REGARDING U.S. PATENT NO. 9,722,104**

¹ Mundra Solar PV Ltd. and Adani Solar USA Inc. were joined as petitioners in this proceeding based on a petition and motion for joinder filed in IPR2025-00186, which was granted.

I, Sanjay Banerjee, do hereby declare and state, that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.



Executed on: October 20, 2025

Sanjay Banerjee

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Appendix A – Materials Relied On

I. INTRODUCTION

1. I have been retained by counsel for Petitioners Runergy USA Inc. and Runergy Alabama Inc. as an expert witness in the above-captioned proceeding. I have been asked to provide my opinion about the state of the art of the technology described in U.S. Patent No. 9,722,104 (“the 104 Patent”) and on the patentability of claims 1-11 of the 104 Patent, particularly in light of the Board’s Institution Decision (Paper 11), the Patent Owner’s Response to Petition for Inter Parties Review (Paper 16), and the Declaration of Dr. Martin Peckerar (EX2001). The following is my written testimony on these topics, which supplements my previous testimony I understand has been submitted in this proceeding as EX1003.

2. My background, qualifications, and compensation are set forth in my first declaration and CV. *See* EX1003 and EX1004.

II. FORMING A POLYSILICON BSF ON TOP OF A TUNNEL OXIDE DOES NOT OBVIATE THE NEED FOR ISOLATION

3. Throughout his declaration, Dr. Peckerar contends that there is no need for Jin’s gap T in both the combination with Chang and the combination with Feldmann. Dr. Peckerar’s arguments take two forms. First, he contends there is no need to physically separate the polysilicon BSF of Feldmann from the edge of the substrate with Jin’s gap T because “there is now a tunnel oxide layer located between and physically separating the two layers.” EX2001, ¶131. Second, he observes that in Jin, the gap is needed because Jin “forms both its emitter layer 120

and back surface field layer 150 by doping the front and backside of the same substrate,” whereas my opening declaration “points to tunnel oxide and polysilicon layers that are deposited on top of the substrate’s back surface.” *Id.*, ¶¶289, 291 (emphasis in original). For both combinations, I understand Dr. Peckarar’s point to be that when the polysilicon BSF is deposited on top of the substrate, the type of shorting in Jin no longer occurs, because that is the argument he makes with respect to the Jin/Feldmann combination. *Id.*, ¶149 (“Feldmann’s backside layers are not doped into Feldmann’s substrate. Thus, the type of shorting discussed in Jin can no longer occur.”). Dr. Peckarar is wrong on both points.

4. The purpose of Jin’s gap T is not merely to physically separate the BSF from the emitter diffused down the lateral sides of the substrate. Rather, the purpose is to electrically isolate the BSF from the emitter that has diffused down the lateral sides. For example, in describing Fig. 3, Jin states that “if the back surface electric field layer 150 is formed *separated from the edge* of the substrate 110, the back surface field layer 150 and the emitter layer 120 may be *kept from being shorted*.” EX1009-Jin, ¶58. Jin further states that when the gap T is smaller than 2 microns, “the back surface field layer 150 and the emitter layer 120 may be shorted due to diffusion of impurities.” *Id.*, ¶60. “Shorting” occurs when the BSF and emitter are close enough that electrical current may pass between them, thus reducing the current output of the cell. When shorting between the BSF and

emitter occurs, it “may be a cause for degrading the efficiency of the solar cell 100.” *Id.*, ¶60. Accordingly, Jin’s reason for separating the BSF from the edge of the substrate by a gap T is not merely to keep the emitter and BSF from physically touching, but to ensure that no shorting occurs between the two.

5. Inserting a tunnel oxide between the BSF and the substrate does not obviate the need to separate the BSF from the edge of the substrate to prevent shorting because tunnel oxides would not prevent *electrical* contact between the BSF and the emitter. Tunnel oxides are thin layers of oxide, usually silicon oxide. For example, Feldmann discloses that its tunnel oxide is only about 14 angstroms (or 1.4 nanometers). EX1012-Feldmann, 271. Although silicon oxide is generally considered an insulator that does not conduct electrical current, because of the thinness of the tunnel oxide, electrons and other charge carriers are able to pass directly through the tunnel oxide through a quantum mechanical process known as “tunneling”—that is the very reason it is called a *tunnel* oxide—even though such charge carriers cannot be electrically conducted through the tunnel oxide in a classical sense. See, e.g., EX1030-Streetman at 174 (“Although electrons with energy less than this barrier cannot go through the oxide classically, it was discussed in Chapter 2 that quantum mechanically electrons can tunnel through a barrier, especially if the barrier thickness is sufficiently small.”). For this reason, the tunnel oxide in Feldmann’s TOPCon structure “does not hinder majority charge

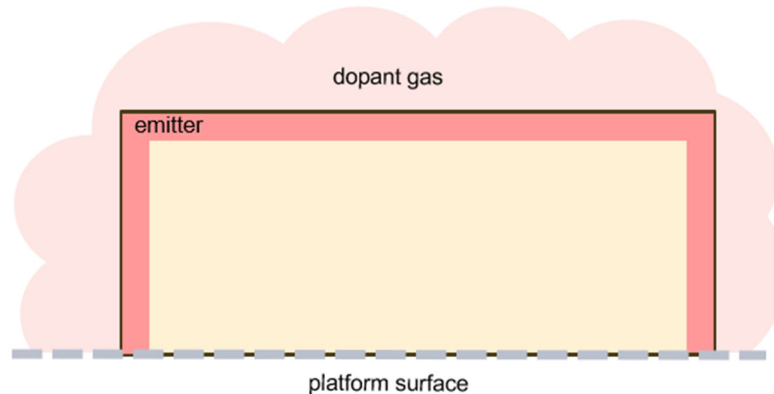
carrier transports across its barrier.” EX1012-Feldmann, 272. In fact, Feldmann’s TOPCon solar cell would not work at all if electrical current could not pass through the tunnel oxide, because the tunnel oxide would block *any* current generated in the solar cell from propagating to the back polysilicon and metal contact to power a load. This would result in an open circuit.

6. Moreover, Jin cautions that if the gap between the emitter and BSF is less than 2 *microns*, shorting may occur. *Id.*, ¶60 (“If the gap (or distance) T between the back surface field layer 150 and the edge of the rear surface of the substrate 110 is shorter than 2 μm , the back surface field layer 150 and the emitter layer 120 may be shorted due to diffusion of impurities, which may be a cause for degrading the efficiency of the solar cell 100.”). Two microns is 20,000 angstroms. Because tunnel oxides are orders of magnitude thinner than 2 microns, the gap between the emitter and the BSF from a tunnel oxide *alone* is substantially less, leading to shorting. *See, e.g.*, EX1012-Feldmann at 271 (~14 angstroms).

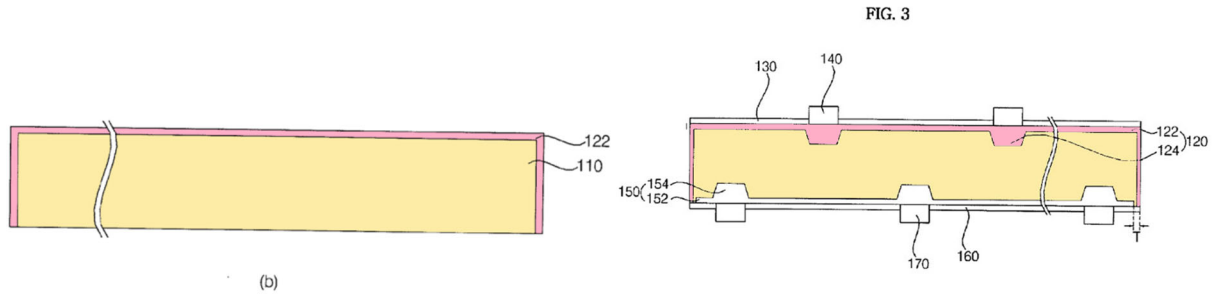
7. Accordingly, the insertion of a tunnel oxide between a polysilicon BSF and an emitter diffused down the side of the substrate by thermal diffusion (like that depicted in Jin) would neither block electrical current from flowing nor provide sufficient physical separation to prevent shorting between the emitter and BSF. A separation, like the gap T described in Jin, would remain necessary even with the tunnel oxide. Moreover, nothing about my analysis of the shorting

problem described by Jin above hinges on the BSF being diffused into the substrate versus a polysilicon layer being formed on top of the substrate.

8. In Chang's Fig. 8, for instance, the emitter may be formed by thermal diffusion, just like in Jin. EX1013-Chang, ¶98. As I explained in my opening declaration (at ¶¶69, 230), thermal diffusion exposes the substrate to a dopant vapor, which causes dopants to diffuse into not only the front but also the lateral sides of Chang's substrate.



In other words, the emitter wraps around the front surface of the substrate and down the lateral sides, as depicted in Figs. 3 and 7(b) of Jin, for example. That process occurs regardless of whether the BSF is also diffused into the substrate, or formed by depositing doped polysilicon on top of the back surface of the substrate. In either case, the end result is that the emitter and BSF are close enough to cause shorting unless they are physically separated and electrically isolated.



9. Nor does the tunnel oxide in the Chang/Jin or Jin/Feldmann combinations “act as a diffusion barrier,” as Dr. Peckerar contends. EX2001, ¶132, 139. According to Dr. Peckerar, “silicon dioxide is a well-known diffusion barrier.” EX2001, ¶132. However, the silicon oxide has to be thick enough to block diffusion, particularly when dopants are exposed to high temperatures during the manufacturing process. A tunnel oxide is too thin to block diffusion of dopants from the polysilicon BSF into the substrate.

10. For example, as early as 1985, Yablonovitch commented on the diffusion blocking ability of silicon oxide layers of varying thicknesses. His paper reported on the performance of crystalline solar cells having n-type “SIPOS” emitters. EX1039-Yablonovitch, abstract. “SIPOS” stands for “semi-insulating polycrystalline silicon,” which is a “mixture of microcrystalline silicon and silicon dioxide (SiO_x).” EX1039, 1211. As part of Yablonovitch’s fabrication method, before forming the SIPOS emitter on the test wafer, Yablonovitch thermally oxidized the silicon wafer with O_2 , which resulted in a thin layer of silicon oxide (SiO_2) on the surface of the wafers. EX1039-Yablonovitch, 1212, Table II (steps 5-

6), Fig. 3. The thin layer of silicon oxide and the SIPOS emitter (shown as micro-crystalline grains of silicon) are seen in Fig. 3 of Yablonovitch below.

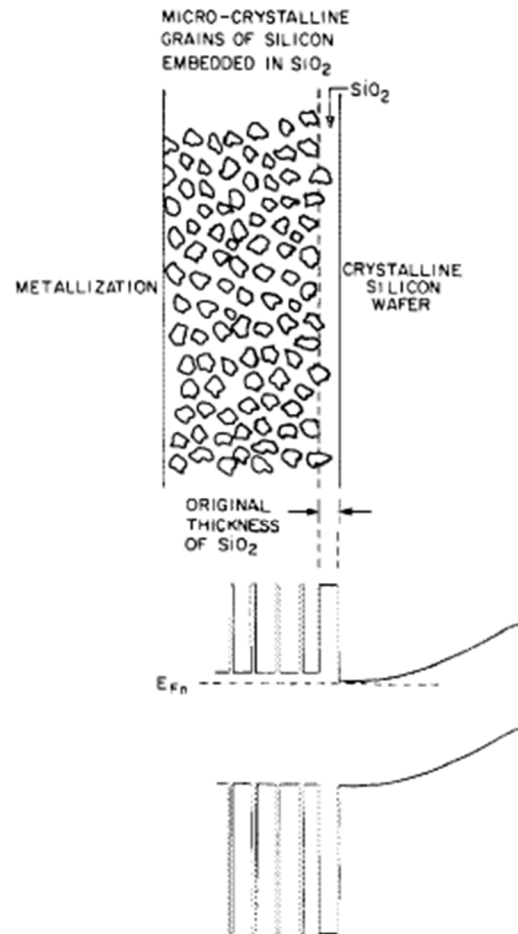


FIG. 3. Model for the metallurgical configuration of the SIPOS-Si heterojunction. Electron conduction is thought to proceed via the microcrystalline grains which protrude into the thin oxide layer.

11. After depositing the SIPOS emitter, Yablonovitch thermally annealed the test device at 900°C for fifteen minutes to crystallize the SIPOS and activate the dopants. EX1039-Yablonovitch, 1212, Table II (steps 7-9). Despite the presence of the silicon oxide layer between the SIPOS emitter and the silicon wafer, Yablonovitch reports that “phosphorus [dopants] diffuse[d] about 20-50 Å

into the silicon wafer as measured by secondary ion mass spectrometry.” EX1039-Yablonovitch, 1212. The diffusion occurred even though the oxide thickness was in the range of 25-40 Å (2.5-4.0 nm), thicker than the 14-20Å thick tunnel oxide disclosed in Feldmann and the 5-20Å thick tunnel oxide disclosed in Chang as preferred. EX1039-Yablonovitch, 1212 (“Oxide thickness between 25 and 40 Å was found to be equally favorable with respect to the ‘emitter Gummel number.’”); EX1012-Feldmann, 271 (“Then an ultra-thin wet chemical oxide layer was grown with a thickness determined to be about 14 Å by spectroscopic ellipsometry. It should be noted, that 20 Å is the maximum tolerable oxide thickness... at which tunneling becomes inefficient and, thus, results in a lowered FF.”); EX1013-Chang, ¶59 (“In order to further improve the tunneling effect, the thickness of the second tunneling layer 44 may be 0.5 nm to 4 nm, more specifically, 0.5 nm to 2 nm.”).

12. In a similar paper published in 1984, Kwark also reported on the use of chemical oxide “chemox” layers in solar cells having either SIPOS emitters or polysilicon (no oxygen) emitters. EX1024, 742-743. Kwark studied and presented data on the emitter saturation current J_{oe} for test devices having either a SIPOS emitter or a polysilicon (“POLY”) emitter, both with and without the intentionally added chemox layer. EX1024, 743, Figs. 4-6. For the POLY emitters, one of the devices Kwark studied was a so-called “emitter C” with a chemox layer, “which

relied solely on outdiffusion from the doped POLY to form the base-emitter junction” at annealing temperatures between 850 and 1000°C. EX1024, 743. In other words, the substrate/polysilicon emitter junction of the solar cell with emitter C was formed via diffusion of dopants from the polysilicon into the substrate, *through the chemox*. Based on Kwark’s collected data, Kwark deduced that the concentration of dopants outdiffused from the emitter into the substrate increased as the annealing temperature rose:

“Prediffused” emitter B displays a baseline J_{oe} of 5×10^{-14} A/cm² due to recombination in the bulk of the emitter. *To this is added a component due to outdiffusion from the heavily doped POLY which becomes increasingly significant* for annealing temperatures above 900°C. This is apparent if one notes that the increase in J_{oe} for emitter B can be accounted for by the J_{oe} of emitter C at the same temperature. At 1000°C, this *outdiffusion is severe enough to dominate* the J_{oe} which accounted for the lack of difference between emitters B and C. [EX1024, at 743 (emphasis added).]

As Kwark’s study demonstrates, a thin oxide layer such as chemox would not block diffusion of dopants from a polysilicon layer into a substrate, and in particular it would not block diffusion of dopants around 850-900°C, which is around the same annealing temperature regime where Feldmann’s TOPCon structure saw its best results in terms of surface passivation. See, EX1012-Feldmann, Fig. 1.

13. As for Kwark’s SIPOS emitters, Kwark observed that there was “little difference in J_{oe} between the SIPOS contacted emitters with and without the

chemox,” which “would indicate that the interface between SIPOS and monocrystalline silicon is similar in both cases.” EX1024-Kwark at 743. Kwark thus postulated that “a thin tunnelable interfacial oxide [formed] as a consequence of the high temperature annealing step,” which simply adds thickness to the existing chemox layer in the SIPOS devices that have one. EX1024-Kwark at 743 (“The smaller increase in J_{oc} for the SIPOS device with chemox can be explained by assuming that the chemox simply adds an additional thickness to the oxide layer resulting from the anneal step.”). In other words, for the SIPOS emitters, the oxide layer was *even thicker* than for the POLY emitters (like Feldmann’s and Chang’s), because the oxygen in the SIPOS added “an additional thickness” to the chemox layer during annealing. Despite this fact, Kwark studied a SIPOS “outdiffused emitter C” that relied on diffusion from the doped SIPOS into the substrate. EX1024-Kwark at Fig. 6. The thicker chemox-plus-interfacial oxide still did not block the diffusion of dopants into the substrate, though it “acted as a more robust diffusion barrier.” EX1024-Kwark at 743.

14. Chang also discloses that during the manufacture of Chang’s solar cell, dopants (second portion 30b) diffuse through tunneling layer 44 into the substrate during “thermal treatment” (annealing) of the polysilicon BSF:

Then, as shown in FIG. 16C, the second conductive type dopant in the first portion 20 a is diffused into the semiconductor substrate 10 by thermal treatment to form the second portion 20 b of the emitter area 20, and **the first conductive type dopant in the first portion 30 a is**

diffused into the semiconductor substrate 10 to form the second portion 30 b of the back surface field area 30. As such, in the embodiment of the invention, the first portions 20 a and 30 a serve as doping sources, **thereby forming the second portions 20 b and 30 b through diffusion using thermal treatment without using an additional doping method such as ion implantation.** As a result, the manufacturing process can be simplified. [EX1013-Chang, ¶149, Fig. 16C (emphasis added).]

FIG. 16C



15. In his declaration, Dr. Peckerar cites a patent, EX2003, in support of his contention that silicon dioxide is a well-known diffusion barrier, but that patent does not alter my opinions. EX2001, ¶132. While the oxide layer in that patent is described as 1-20Å thick, it is not exposed to the temperatures necessary to make the solar cells described in Feldmann, Jin, or Chang (e.g., in the range of 800-900°C). In fact, the patent’s abstract warns that the oxide must be formed by an aqueous bath “at a relatively low temperature such that diffusion of dopants in the semiconductor substrate is not induced.” EX2003, abstract; *see also id.*, 2:38-39 (“The aqueous bath preferably has a temperature in a range from about 0° C to about 200° C.”). Moreover, as the patent explains, the “temperatures to which structure 10 is exposed *are sufficiently low so as not to induce a diffusion of*

dopants from the doped active regions into the undoped regions of the semiconductor substrate.” EX2003, 4:28-32. But as I explained above, solar cell devices like those in Jin, Chang, and Feldmann experience annealing temperatures hundreds of degrees Celsius higher than that. See, e.g., EX1012-Feldmann at 271, Fig. 1 (“Afterwards, the samples’ passivation was activated in a tube furnace process with plateau temperatures in the range of $600\text{ }^{\circ}\text{C} < T_{\text{anneal}} < 1000\text{ }^{\circ}\text{C}$.”). As Chang, Kwark, and Yablonovitch show, at such temperatures, dopants would still diffuse through substantially thicker oxide layers. In sum, as Yablonovitch, Kwark, and Chang show, ultrathin oxide layers like the tunnel oxides in Feldmann and Chang would not block diffusion of dopants from the polysilicon emitter into the substrate in the proposed combinations, and they certainly would not render superfluous the use of Jin’s isolation gap T.

16. In paragraphs 149-151 of Dr. Peckerar’s declaration, he contends that the mechanism of charge transport through tunnel oxides like Feldmann’s “is both complicated and subject to significant debate,” citing what appear to be quotes or paraphrases of passages along with a figure purportedly from a textbook, “Electronic Materials: Science and Technology.” I understand Patent Owner did not submit this textbook as evidence in this proceeding, and I therefore do not have the ability to analyze and consider what the textbook actually says. Even if I assume that the bulleted paragraphs are accurately-reproduced quotes from the

textbook, it does not appear to me that these passages are describing tunnel oxides. For one thing, no thickness dimensions are given, nor does the term “tunnel oxide” appear (and the discussion of oxide trap charges refers to charges “deep in the oxide bulk,” which is inconsistent with a description of a tunnel oxide that is on the order of 14 angstroms thick). For another thing, the passages all purport to describe various types of impurities that may act as fixed or semi-fixed charges embedded in an oxide. But the issue with shorting through the tunnel oxide occurs because electrons or holes (which are not discussed in the “passages” referenced by Dr. Peckerar at all) quantum mechanically tunnel *through* the tunnel oxide, regardless of whether there are any “fixed charges” or the like in the tunnel oxide. Simply put, Dr. Peckerar has not provided the evidence he supposedly relies on, and even at face value, it appears to be entirely irrelevant to the issue of Jin’s shorting through a *tunnel* oxide.

17. Dr. Peckerar’s argument is also at odds with the 104 Patent itself, which describes the “unwanted[] short-circuit[ing] in the side of or the edge of the back surface of the semiconductor substrate 100” caused by “the impurities of the second conductive type [that] may be diffused into the side of or the edge of the back surface of the semiconductor substrate 100” during formation of the emitter (i.e., the “second conductive type region 120”). EX1001, 13:24-35. The 104 Patent notes that short-circuiting is an issue even though the first conductive type

semiconductor region 170 (BSF) is formed on, not in, the substrate 100. EX1001, 7:42-48, 8:65-9:7.

18. My opinion regarding the shorting that occurs through the tunnel oxide is further borne out by Chang, which explicitly discloses an isolation region despite having a tunnel oxide separating a polysilicon BSF and substrate/emitter, indicating that Skilled Artisans prior to the 104 Patent were aware that shorting such as that described by Jin can occur even when there is a tunnel oxide separating the BSF and the substrate. EX1013-Chang, ¶56, 61 (“In the embodiment of the invention, the back surface field area 30 includes a first portion 30 a formed on the second tunneling layer 44. The first portion 30 a of the back surface field area 30 formed on the second tunneling layer 44 may include a polycrystalline, amorphous or microcrystalline semiconductor....”)

III. RESPONSES TO DR. PECKERAR’S STATEMENTS REGARDING THE COMBINATION OF CHANG AND JIN

A. Paragraph 76 of Chang Does Not “Eliminate” Chang’s Need for Isolation

19. Ignoring the four paragraphs in which Chang describes the formation of an isolation region, ¶¶45, 51, 56, 62, Dr. Peckerar focuses on a single paragraph of Chang, ¶76, and interprets this paragraph as “eliminating” the need for an isolation region at all in Chang. I disagree with Dr. Peckerar’s interpretation of ¶76.

20. Paragraph 76 of Chang says in its entirety:

In this instance, the emitter area 20 and the back surface field area 30 may be disposed at different sides of the semiconductor substrate 10 to form a double-surface light-receiving type structure. As a result, light is incident upon the back surface of the semiconductor substrate 10 as well as the front surface of the semiconductor substrate 10, thereby increasing an amount of incident light and improving efficiency of the solar cell 100. **Because the emitter area 20 and the back surface field area 30 are not adjacent to each other, the necessity of performing an isolation process when the emitter area 20 and the back surface field area 30 are formed to be adjacent to each other is eliminated.** In addition, because the emitter area 20 and the back surface field area 30 are **entirely formed**, thus requiring no **additional patterning** and alignment processes. As a result, manufacturing process is simplified and cost is thus reduced.

21. Dr. Peckerar interprets this paragraph as indicating that Chang “eliminates” *all* need for isolation in any form. Dr. Peckerar misinterprets ¶76.

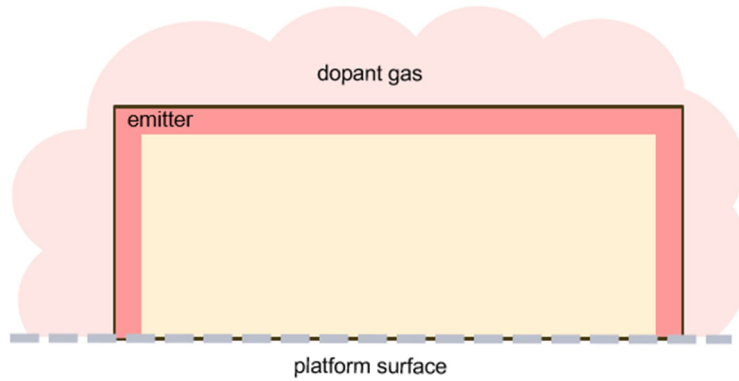
22. First, Dr. Peckerar’s interpretation directly conflicts with the four other paragraphs of Chang (¶¶45, 51, 56, 62) that describe the formation of an isolation region. Dr. Peckerar makes no effort to reconcile this manufactured inconsistency in Chang, and instead just ignores it. In my opinion, the proper interpretation of Chang ¶76 would not result in any inconsistency with the other passages of Chang that describe the formation of an isolation region.

23. In my opinion, ¶76 is describing a particular embodiment of Chang’s device in which the emitter is not diffused down the side of the substrate (and is therefore not “adjacent” to the BSF), rather than all embodiments of Chang. This is apparent initially from Chang’s use of the phrase “In this instance” to begin the

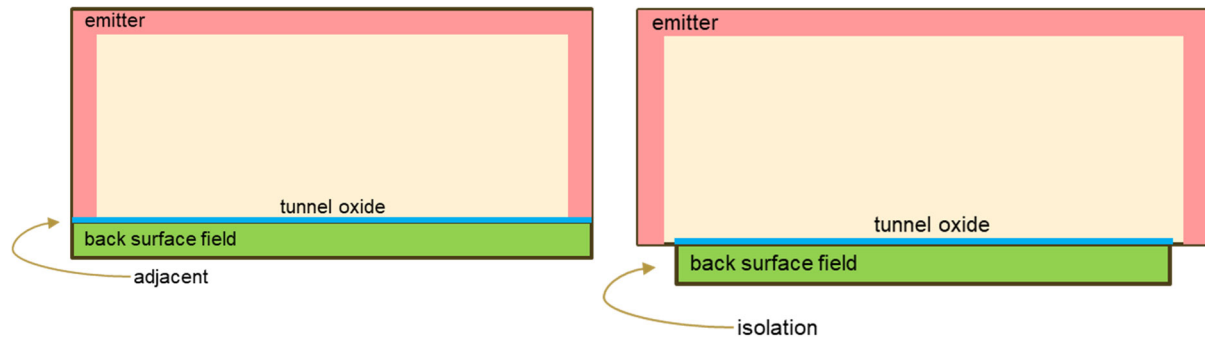
paragraph, which suggests ¶76 is addressing a specific case, and that what is discussed here does not apply to other “instances” of Chang’s device. Likewise, Chang states in ¶76 that “the emitter area 20 and the back surface field area 30 may be disposed at different sides” so that they are not adjacent, but the word “may” indicates that this description is optional and does not reflect every embodiment.

24. Chang’s teachings elsewhere further confirm my understanding. In particular, Chang expressly identifies two different techniques for forming the emitter region: thermal diffusion and ion implantation. EX1013-Chang ¶98 (“The emitter area 20 may be formed by a variety of doping methods (for example, thermal diffusion, ion implantation or the like).”).

25. As I have explained in my opening declaration and above, in a thermal diffusion process, the substrate is exposed to a dopant vapor that causes dopants to diffuse into the sides of the substrate. See EX1001, ¶¶71 & 247, and ¶8 above. So in the context of Chang, when Chang’s frontside emitter is formed via thermal diffusion, the front and lateral sides of Chang’s substrate become diffused with dopants, such that the emitter runs across the front of the substrate and down the lateral sides, like in the illustration below.



In this embodiment, if there is no isolation region, then the BSF and emitter are directly adjacent to each other, as shown in the left figure below.



26. Paragraph 76 of Chang, however, is discussing an embodiment in which the “the emitter area 20 and the back surface field area 30 are not adjacent to each other.” EX1013-Chang, ¶76. In other words, Chang ¶76 is not describing embodiments in which the emitter is formed by thermal diffusion. Accordingly, the need to perform an isolation step when the emitter is formed by thermal diffusion is not eliminated.

27. Ion implantation, on the other hand, works differently than thermal diffusion. In ion implantation, a concentrated beam of ions is directed onto the location where dopants are to be embedded, as depicted in the figure below from

the Quirk and Serda textbook. EX1030-Streetman, 159; EX1021-Quirk, 482, Fig. 17.5. The beam is then scanned across the area where the doped region is to be formed, such as an emitter region. *Id.* By controlling the scanning speed, beam energy, and dopant concentration, the density and depth of dopants can be controlled. *Id.* As shown below, dopants are only embedded where the beam is directed. As a result, by using ion implantation, the step of separately using a laser or other technique to form edge isolation is no longer necessary. See, e.g., EX1038-Rohatgi, 5:18-21 (“Selective emitters formed by ion implantation allow for more uniform incorporation of dopant, do not involve the formation of phosphosilicate glass, and eliminate the need for edge isolation.”).

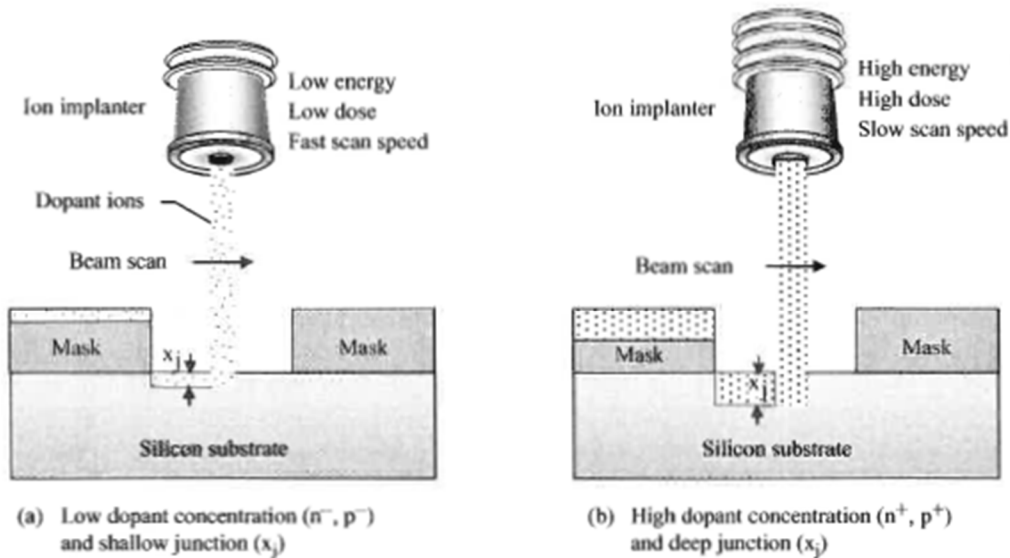
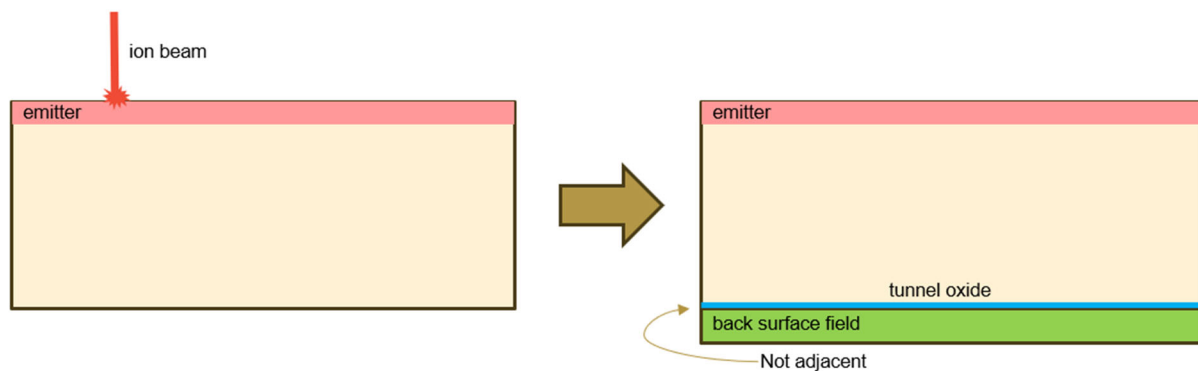


FIGURE 17.5 Controlling Dopant Concentration and Depth

28. Because dopants only become embedded in the substrate at the locations where the ion implant beam is aimed, forming Chang’s emitter layer

using ion implantation would only result in dopants forming the emitter region along the front surface of the solar cell, as illustrated below—the lateral sides of the substrate would remain undoped. In this situation, the emitter and BSF are “disposed at different sides of the semiconductor substrate” and “[b]ecause the emitter area 20 and the back surface field area 30 are not adjacent to each other, the necessity of performing an isolation process when the emitter area 20 and the back surface field area 30 are formed to be adjacent to each other is eliminated.”

EX1013-Chang, ¶76. In my opinion, it is the embodiments of Chang in which the emitter is formed via ion implantation that are being discussed in ¶76.

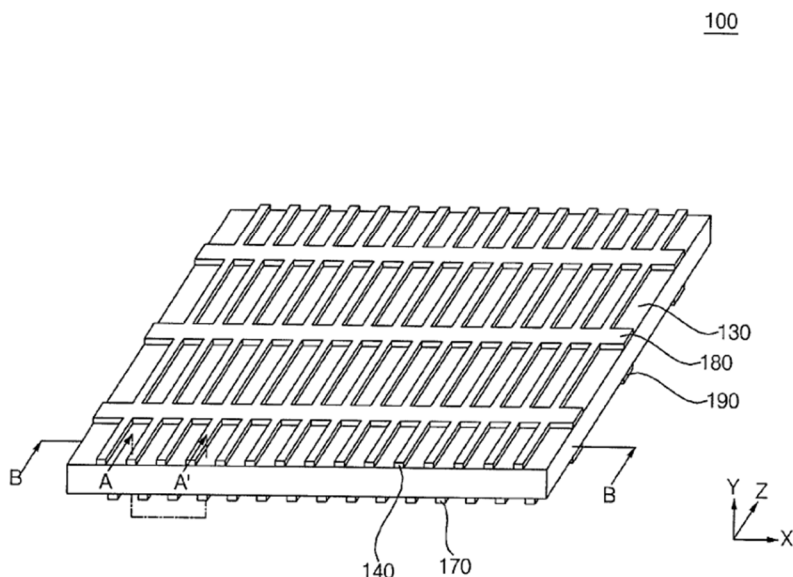


29. Moreover, Dr. Peckerar overstates the significance of the fact that Figs. 1 and 8 of Chang do not depict the isolation regions. For one thing, as noted above, Chang *discloses* forming a peripheral isolation region on the back surface of the substrate, whether or not it is depicted in the figures. The Skilled Artisan would understand that figures, such as those in patents, are not intended to reflect every detail of a device, but are high-level, stylized schematics intended to

facilitate comprehension and supplement what the specification describes. Chang explains in ¶¶30-31 that its “embodiments may be modified into various forms,” and that parts of the solar cell “are not illustrated for clear and brief description”.

30. Jin is a perfect example. Figures 2 and 3 of Jin both show parallel cross sections of the solar cell depicted in Figure 1, with Figure 2 extending along the line A-A’ and Figure 3 extending along the line B-B’. EX1009-Jin, ¶25.

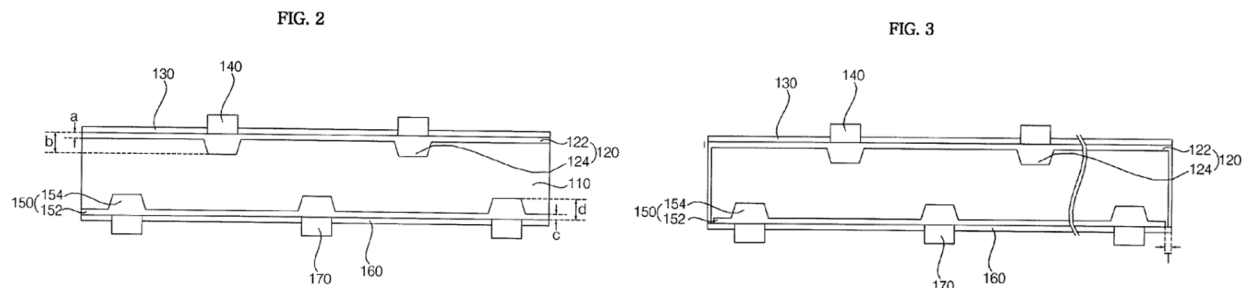
FIG. 1



31. Figure 2 therefore does not depict the isolation gap T or the emitter extending down the side of the substrate seen in Figure 3, because Figure 2 does not depict the very lateral sides of the substrate. Notably, Figure 2 only shows two finger contacts on the front of the cell, and three on the back. This is a substantially smaller number of fingers than are normally included on a solar cell

like Jin's (Figure 1 of Jin above depicts at least 16 finger electrodes, for example, though even that number is somewhat fewer than one would expect in an actual solar cell), which itself indicates that Figure 2 is depicting only a portion of the solar cell. Figure 3, on the other hand, includes a curvy break line, indicating that portions of the middle of the solar cell are not depicted, so that the lateral side of the solar cell depicting the isolation gap T and emitter down the sides can be depicted. In fact, every figure in Jin that illustrates a cross section of a solar cell with the isolation gap T and emitter on the sides *also* includes a break line; conversely, not a single figure in Jin shows the gap T/side emitter without a break line, or vice versa. In my experience, it is a common practice in figures in articles, textbooks, and patents to depict only relevant portions or details of a device, allowing the author to focus the reader's attention on the more important features under discussion, rather than bogging down the reader by drawing every possible feature.²

² The 104 Patent is itself an example of this practice, because the figures of the 104 Patent do not show the emitter layer extending down the sides of the substrate, the very detail Dr. Peckerar criticizes Chang for not showing, even though the 104 Patent's specification describes this detail. See EX1001 at 13:24-31. Figure 2 of



32. Chang's figures are no different. Tellingly, Figures 1 and 8 of Chang depict only two finger electrodes per side. But as Figure 2 of Chang clearly shows, there are *dozens* of finger electrodes in Chang's solar cell. Figures 1 and 8, therefore, like Jin's Figure 2, are clearly not intended to literally represent a cross section of the entire width of a solar cell. Moreover, there is nothing in Figures 1 and 8 such as a break line indicating that the sides of the figures are intended to show the true lateral side of the solar cell in Figure 2. In my opinion, the figures are instead intended only to highlight the vertical arrangement of the various layers that make up Chang's different solar cell embodiments.

the 104 Patent also includes a break line to signify that the interior of the solar cell is not shown, so that the sides can be displayed.

Figure 1 is a schematic diagram of a substrate 24(34). The substrate is a large rectangle with rounded corners, divided into a grid of vertical and horizontal lines. A circular inset provides a magnified view of the intersection of a vertical line 24b(34b) and a horizontal line 24a(34a). The inset shows the lines intersecting at a point, with dimensions W2 and P1 indicated.

B. Dr. Peckearar's Other Assertions Regarding Chang

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isolation region or the like” as an example of a pre-designated or inevitably formed region: “excluding pre-designated or inevitably formed regions such as periphery region, isolation region or the like.” EX1013-Chang ¶¶45, 51, 56, 62.

35. Dr. Pekcerar also suggests there are no pre-designated or inevitably formed regions in Chang’s Figure 1 or Figure 8. As already discussed above, the Skilled Artisan would understand that figures, such as those in patents, are not intended to reflect every detail of a device, but are high-level, stylized schematics intended to facilitate comprehension and supplement what the specification describes. Chang even makes that point in ¶¶30-31, noting that “embodiments may be modified into various forms,” and that parts of the solar cell “are not illustrated for clear and brief description”.

36. Either way, I understand that it does not matter whether a prior art reference *requires* the feature in question, only whether the prior art *discloses* the feature, even if the prior art calls the feature optional.

37. Dr. Peckerar makes a similar argument that Chang does not “preclude” forming the isolation region inward from the edge of the rear surface of the substrate, i.e., in the “edge portion”. Again, the question is not whether Chang *requires* forming the isolation region at the edge, the question is whether Chang *discloses* an isolation region there—Chang does. Chang teaches an isolation region, such as in the “periphery region.” As I noted in my opening declaration,

“periphery” means at the “perimeter” or “outer limits” of an area. EX1003, ¶227. The Skilled Artisan would therefore understand that Chang discloses an isolation region at the perimeter, or outer limits, of the back surface of the substrate.

38. Dr. Peckerar also argues that, under my understanding of Chang, there are isolation regions on both the front and backside of the substrate, so the isolation region on the backside does not “*prevent a contact*” between the frontside emitter and BSF. EX2001, ¶284-286. But that is not the embodiment of Chang I relied on in my opening declaration. E.g., EX1003, ¶196 (showing rear isolation only). Chang clearly discloses that there “may” be isolation in the front emitter, but there need not be: “In the embodiment of the invention, the first portion 20 a of the emitter area 20 *may* be entirely formed over the first tunneling layer 42.” EX1013-Chang, ¶51. Dr. Peckerar’s suggestion that *if* there is peripheral isolation on the rear side of Chang then there *must also* be isolation on the front side of Chang, does not follow and is not based on any actual disclosure in Chang. And of course, when there is a peripheral isolation region on the back of Chang’s device, as is the case in the combination presented in my opening declaration, it “*prevents a contact*” between Chang’s BSF and the emitter, for the reasons I discussed in my opening declaration. EX1003, ¶¶224-226, 230-231.

39. Dr. Peckerar next argues that a Skilled Artisan combining Jin’s gap T with Chang’s device would *not* apply the gap T to the tunnel oxide. Once again,

Dr. Peckerar ignores that Chang explicitly discloses that the isolation region also applies to the tunnel oxide, because the tunnel oxide is “entirely formed” over the substrate. EX1013-Chang, ¶56 (“Meanwhile, a second tunneling layer 44 is entirely formed over another surface (for example, back surface, hereinafter, referred to as a “back surface”) of the semiconductor substrate 10. As used herein, the expression “entirely formed” means that an element such as a layer is formed over an entire surface without an empty area or a non-coverage area, or is formed in an entire area excluding pre-designated or inevitably formed regions such as periphery region, isolation region or the like.”).

IV. RESPONSES TO DR. PECKERAR’S STATEMENTS REGARDING THE COMBINATION OF JIN AND FELDMANN

A. The Combination of Jin and Feldmann Would Be Subject to Shorting Without Jin’s Isolation Gap T

40. Dr. Peckerar disputes that there would be a shorting problem between the BSF and frontside emitter in the Jin/Feldmann combination, because the BSF in the combination is formed on top of the substrate, rather than in it. As I discussed above in ¶¶3-8, forming the BSF on top of the substrate does not obviate the problem of shorting discussed by Jin. This is shown by the fact that Chang also discloses an isolation region, despite disclosing a polysilicon BSF formed on top of the substrate. For the same reasons, the issue of shorting between the polysilicon BSF and the emitter in the Jin/Feldmann combination would remain a problem

because both Jin and Feldmann used thermal diffusion to form the front emitter, which would cause the emitter to extend down the lateral sides of the substrate close to the BSF. See, e.g., EX1009-Jin ¶78 (“Forming the second area 122 may be carried out by doping the substrate 110 with the first impurity of the second conductive type according to a *heat diffusion method*....”); EX1012-Feldmann, 270 (TOPCon “offers a simple processing scheme, which is *compatible with high-temperature processes such as diffusion*”), 271-272 (TOPCon “was implemented at the rear side of n-type silicon solar cells with a *diffused* boron-doped *emitter* (140 Ω/sq) *at the front side*”).

B. Response to Dr. Peckerar’s Shadow Mask Comments

41. In ¶178 of his declaration, Dr. Peckerar asserts that Jin only uses a mask to facilitate ion implantation. This is wrong. Jin actually discloses that the mask may be used during a heat diffusion, laser doping method, or an ion implantation method, or “[o]ther methods.” EX1009-Jin, ¶¶78, 84.

42. In paragraphs 185-191, Dr. Peckerar assumes that the tunnel oxide in the combination of Jin and Feldmann is thermally grown, and then proceeds to posit why Jin’s mask technique, and the shadow masking techniques described in my opening declaration, would not work using thermally grown oxide. In my opening declaration, I observed that there are a variety of different ways a skilled artisan would know to form a thin tunnel oxide like Feldmann’s, including plasma-

enhanced chemical vapor deposition, atomic layer deposition, and others. E.g., EX1003 ¶117; EX1031-Scherff §2.1; EX1013-Chang ¶146. A skilled artisan would not be confined to just using the thermal growth process as Dr. Peckerar assumes. His paragraphs 185-191 are thus irrelevant to my opinion that a metal shadow mask can be used in the combined teachings of Jin and Feldmann.

43. Dr. Peckerar contends that using these other methods to form the tunnel oxide in the combination of Jin and Feldmann would be “technologically infeasible” (¶193) but I disagree.

44. Forming a thin tunnel oxide using the shadow mask techniques I described in my opening declaration is technologically feasible, for example, using low temperature chemical vapor deposition. As I mentioned in my opening declaration, “[t]he Skilled Artisan would be aware that deposition techniques such as plasma enhanced chemical vapor deposition (PECVD)³ or atomic layer

³ PECVD is a form of low temperature CVD. EX1022-Luque, 284 (“Plasma-Enhanced Chemical Vapor Deposition (PECVD) is preferred to other CVD technologies (atmospheric pressure CVD or low pressure CVD) because it is a low temperature process ($T < 500^{\circ}\text{C}$), and this means reducing complexity and preventing lifetime degradation.”); *see also* EX1022-Luque, 28-29 (explaining that films “are typically deposited between 150 to 300°C” when using PECVD).

deposition (ALD) could be used to deposit the tunnel oxide and the polysilicon layer in the area not covered by the metal mask.” EX1003, ¶¶120, 221. Chang explicitly discloses this, stating: (“the first and second tunneling layers 42 and 44 may be formed, for example, by a method such as thermal growth *or deposition (for example, plasma-enhanced chemical vapor deposition chemical (PECVD), atomic layer deposition (ALD))* or the like”). EX1013-Chang, ¶14. And unlike the two processes Dr. Peckerar focuses on in his declaration—the “wet chemical process of Fetterman” (sic) and “thermally grown” oxide (EX2001, ¶188)—low temperature CVD does not have the same problem of oxygen collecting or forming underneath the entirety of the mask. In fact, Dr. Peckerar admits that a mask could be used to pattern an oxide formed by CVD, he just (mistakenly) assumes that the tunnel oxide here was not formed that way: “*Because the tunnel oxide layer is not deposited via either chemical vapor deposition* or sputtering—instead it is grown from the silicon substrate surface—*a metal shadow mask will have minimal impact* on the shape of the tunnel oxide.” EX2001, ¶187. But that is exactly what I described in my opening declaration, and Dr. Peckerar provides no justification nor cites any support for just assuming that “the tunnel oxide layer is not deposited [by] chemical vapor deposition.”

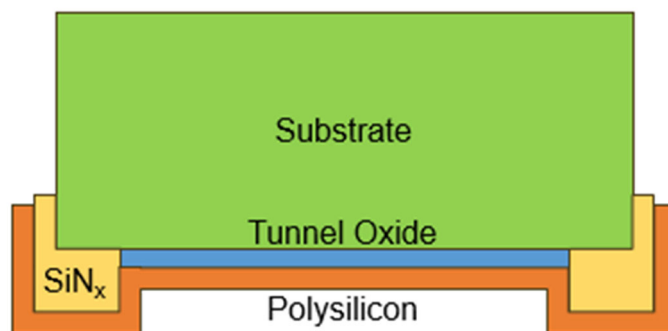
45. Moreover, much of Dr. Peckerar’s arguments reduce to complaints that he believes such a process would be *commercially* infeasible. E.g., EX2001,

¶¶183 (contending “masking not *routinely* used when the ’104 patent was filed”), 196 (pointing to potentially “significant layer variation around the mask edges”), 197 (citing evidence purporting to show “known TOPCon cell manufacturing processes”). But I understand that commercial feasibility is not needed to show a reasonable expectation of success. Moreover, the evidence Dr. Peckerar cites purporting to show that masks usage to form polysilicon via PECVD in TOPCon cells was only in the “idea” phase, Krieg (EX2007), actually cites a prior article, *PECVD Shadow Mask Deposition Of Amorphous Silicon – A Shortcut To Local Passivation Contacts* to M. Stöhr, which “successfully demonstrate[d] the deposition of well-defined a-Si fingers ... using a lab-type nickel shadow mask.” EX1040-Stöhr. Using masks in TOPCon or solar cells generally is not simply some infeasible hypothetical “idea,” as Dr. Peckerar contends.

46. In any event, I also provided four other examples in my opening declaration regarding how a Skilled Artisan could use, for example, a silicon nitride mask to form the tunnel oxide using Feldmann’s wet chemical process. EX1003, ¶¶118-121. A skilled artisan could then form the polysilicon BSF on top of the tunnel oxide using a silicon nitride mask, a metal mask, etc. *Id.*

47. Dr. Peckerar raises various criticisms of these four examples that I address below.

48. First, for the second example in my opening declaration (EX1003, ¶118), I explained how after forming a silicon nitride mask, a skilled artisan could deposit the polysilicon BSF over the silicon nitride mask, etch out the silicon nitride, and mechanically remove the overhanging polysilicon. Dr. Peckerar contends that this process is impossible without first selectively removing the polysilicon to expose the silicon nitride mask (EX2001, ¶¶224-227), but this is wrong. As Dr. Peckerar notes, when the polysilicon layer is formed, it will have a conformal structure around the sides of the substrate. *Id.*, ¶226. The silicon nitride used for the mask would also form a conformal structure around the sides of the substrate. I have indicated this by conceptually correcting the figure in ¶226 from Dr. Peckerar's declaration below, to show that the silicon nitride (yellow) also wraps around the edge of the back surface of the substrate (green). Because of this, portions of the silicon nitride mask remain exposed, allowing it to be wet etched out from beneath the polysilicon without the need to selectively remove any polysilicon, as Dr. Peckerar posits. Once that is completed, the now free-hanging polysilicon is mechanically removed, as I stated in my opening declaration. EX1003, ¶118.



49. Regarding the third example in my declaration (EX1003, ¶119)—using a silicon nitride mask for the tunnel oxide and a metal mask for the polysilicon—Dr. Peckerar’s only complaint is that the process is “complicated” and “expensive,” or would result in “reduced efficiency” so a skilled artisan would not use this process. But that does not speak to the expectation that the process would be successful in forming Jin’s isolation gap T in the combination with Feldmann. Dr. Peckerar also contends that the overspray problem would “likely” result in polysilicon extending past the tunnel oxide and contacting the substrate. But a Skilled Artisan would have been well aware of the overspray effect, and thus would understand the need to adjust basic manufacturing parameters—such as the width of the shadow mask or the deposition pressure—to ensure that the overspray of polysilicon does not result in the very shorting issue the isolation gap T is intended to prevent.

C. **Response to Dr. Peckerar's Negative Fixed Charges Comments**

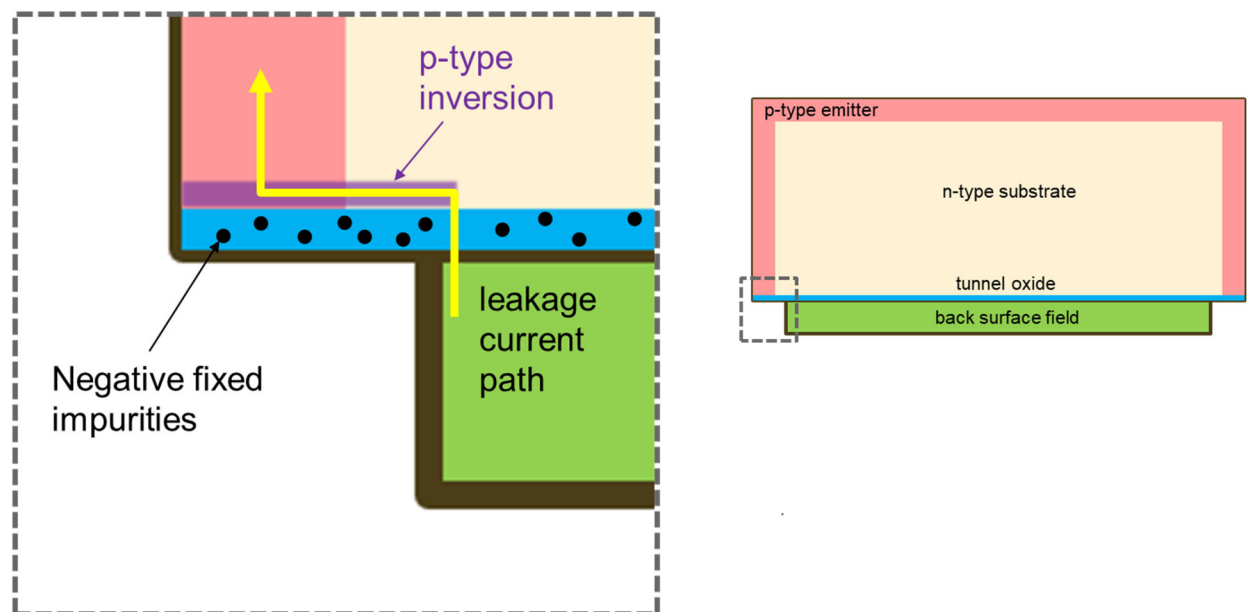
50. Dr. Peckerar contends that the tunnel oxide can extend to the edge without providing a leakage path to the emitter because the oxide is only 1.4 nm thick, which is “too thin to allow lateral conduction.” EX2001, ¶158. Dr. Peckerar’s argument misses the point. It is not lateral conduction through the tunnel oxide that would result in leakage and therefore shorting. Rather, during the formation of the tunnel oxide itself, fixed charges resulting from impurities are trapped in the silicon oxide.

51. A text book published by Ghandi in 1994, for example, explained that “silicon oxides can be grown with good control over interface traps and fixed charge,” indicating that both interface traps and fixed charges are issues with silicon oxide layers. EX1043-Ghandi, 451; *see also id.*, 472 (“fixed charge density in [oxides made by HCl oxidation] is lower than that obtained by growth involving a single chlorine-free low-temperature step”). Ghandi further explains that charge states in silicon dioxide is based on the formation of the oxide itself, and the “interaction between the oxide and the silicon surface.” *Id.*, 476.

52. Depending on the process used to form the tunnel oxide, the trapped fixed charges can be either positive or negative. *Id.*, 478. For example, while thermal growth results in positive fixed charges near the silicon-silicon oxide interface, deposition using, e.g., PECVD results in net negative fixed charges. *Id.*,

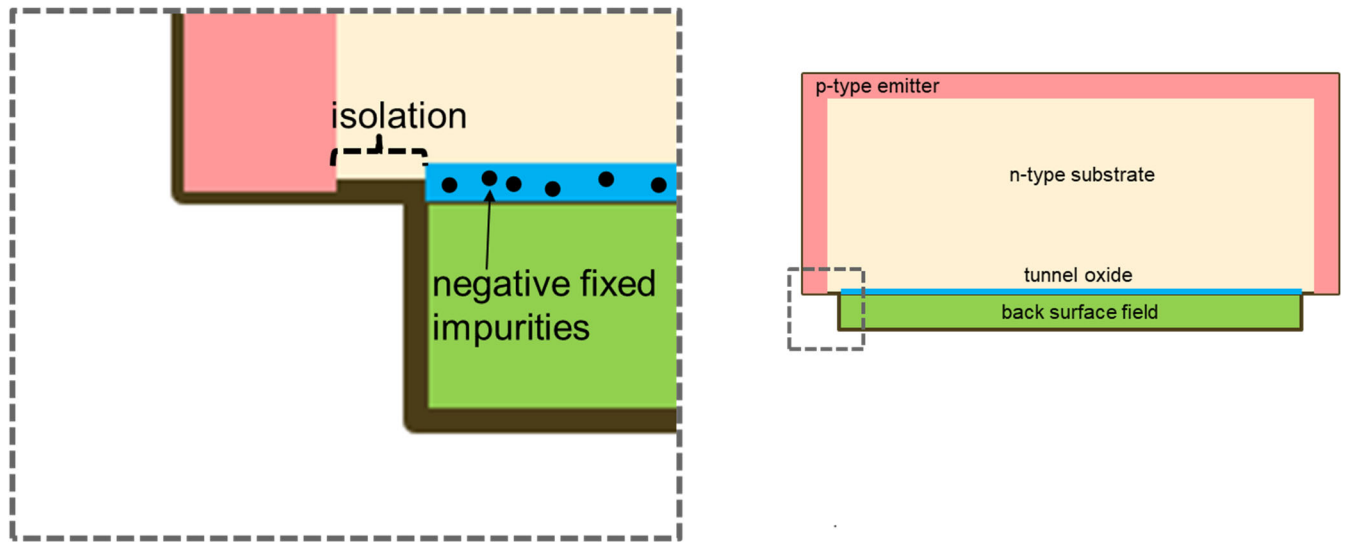
(“In thermally oxidized silicon, the first 100 Å of surface layer represents a silicon-rich transition between the silicon and the oxide. Consequently, there is a net fixed positive charge associated with this layer.”); EX1042-Boogaard, Abstract (silicon oxide formed by PECVD exhibits net negative oxide charge). It was well known that “high quality SiO₂ films can be produced by plasma-enhanced chemical vapor deposition (PECVD) at a temperature around 300° C.” EX1044-Ip, 123.

53. As I explained in my opening declaration, negative fixed charges in the silicon oxide layer could then create a p-type inversion in the n-type substrate. This would provide a leakage path to the p-type emitter on the front of the solar cell, as depicted below. EX1003, ¶113. It is this p-type inversion in the n-type substrate that provides the leakage path to the p-type emitter—not the tunnel oxide itself.



On the other hand, when the isolation region like those taught in Jin and Chang are

applied to the tunnel oxide, the leakage path is broken, and leakage current is reduced or eliminated.



54. Dr. Peckerar interpreted my explanation to be “arguing that incorporation of impurities into the oxide will produce a MOSFET-like structure” and explains that there is no such MOSFET structure in the Jin/Feldmann solar cell because “the tunnel oxide layer is located between an n-type polysilicon layer and p-type frontside emitter layer” rather than between “the source and drain areas” of a MOSFET, which are of the same type. EX2001, ¶159. Again, Dr. Peckerar misses the point. Nowhere in my discussion of trapped impurities and fixed oxide charges did I say that a MOSFET structure with source and drain of the same type is created. See EX1003, ¶113. Rather, I explained that the fixed negative charges in the tunnel oxide creates the p-type inversion in the n-type substrate. *Id.* While inversion layers are used in MOSFET transistors and MOSFET capacitors, in such

a MOSFET device, the inversion layer is created by the gate-to-source voltage. Here, the inversion layer is created by the presence of the fixed negative charges, and provides a leakage path to the emitter.

55. Dr. Peckerar further argues in ¶¶160-161 of his declaration that Feldmann’s “thermally grown oxide” would have “a positive fixed charge” and therefore would not have leakage. First, Feldmann’s tunnel oxide is not “thermally grown,” it is formed using a “wet chemical” process, so Dr. Peckerar’s observations about “thermally grown” oxides having positive fixed charge density are irrelevant to Feldmann. EX1012-Feldmann, 271. Second, there are a variety of different ways a Skilled Artisan would know to form a thin tunnel oxide, including plasma-enhanced chemical vapor deposition, atomic layer deposition, and others. E.g., EX1003 ¶117; EX1031-Scherff §2.1; EX1013-Chang ¶146. And as discussed above, techniques such as PECVD would result in a net *negative* charge, consistent with the observation in my opening declaration. See, e.g., EX1042-Boogaard, Abstract (“In contrast to the well-accepted positive charge for thermally grown SiO₂, the net oxide charge [of silicon oxide deposited by plasma enhanced chemical vapor deposition] was negative and a function of the layer thickness.”); EX1044-Ip, (“In terms of bulk trapped charge, the PECVD SiO₂ film contains in general a higher concentration of negative trapped charge than the

thermal oxide.”). This fact was well known prior to the 104 Patent. EX1042, Boogaard (2011); EX1044, Ip (1991).⁴

56. Dr. Peckerar’s comments that thermally grown oxide results in positive fixed charges are therefore inapplicable and do not alter the opinion in my opening declaration that: “If the tunnel oxide layer were to extend to the edge, the exposed portions of the oxide could trap impurities and create negative fixed oxide charges, which could then create a p-type inversion in the n-type base substrate, leading to a leakage path to the p-type emitter on the front of the solar cell.” EX1003, ¶113.

⁴ Chang’s tunnel oxide is also deposited via CVD. EX1013-Chang, ¶146 (“In this instance, the first and second tunneling layers 42 and 44 may be formed, for example, by a method such as thermal growth or deposition (for example, plasma-enhanced chemical vapor deposition chemical (PECVD), atomic layer deposition (ALD)) or the like, but the embodiment of the invention is not limited thereto and the first and second tunneling layers 42 and 44 may be formed by a variety of methods.”). The fact that Chang also expressly states to exclude the tunnel oxide from Chang’s isolation region thus further confirms my opinion that a skilled artisan would understand to remove the tunnel oxide because it can detrimentally trap negative fixed oxide charges. EX1013-Chang, ¶56.

57. In ¶¶163-168, Dr. Peckerar argues that “Dr. Banerjee proposes removing one layer (the tunnel oxide) from a portion of the backside of Jin’s substrate only to replace it with another layer (the antireflection/passivation layer 160) that exhibits the same problems and gives rise to the same concern.” Dr. Peckerar’s argument in ¶¶163-168 is based on a false underlying assumption.

58. As Dr. Peckerar notes, his argument assumes and is premised on the passivation layer 160 being the same material—i.e., silicon oxide—as the tunnel oxide in the proposed combination of Jin and Feldmann. EX2001 ¶164 (“Jin explains that this layer 160 can be formed from, among other things, a ‘silicon oxide.’”), ¶165 (“[R]emoving the tunnel oxide would not eliminate the issue. Instead, it would be equally present in the Petition’s and Dr. Banerjee’s proposed combination as silicon oxide would still be present in the same area.”), ¶166 (“Removing the tunnel oxide from the gap (or distance T) and replacing it with passivation film made from silicon oxide would have no impact....”).

59. Although it is true that Jin’s antireflection film/passivation layer 160 *can* be silicon oxide, it can also be silicon nitride, amorphous silicon, MgF₂, ZnS, TiO₂, or CeO₂, for example. EX1009-Jin ¶50, EX1003 ¶139. Moreover, in my first declaration I never stated that the antireflection film/passivation layer 160 should be silicon dioxide, or any compound in particular. EX1003 ¶139. That is because the claims of the 104 Patent do not require the antireflection

film/passivation layer 160 in the combination of Jin/Feldmann to be any particular material. Instead, all the claims require is a “*first passivation film*” and Jin’s antireflection film/passivation layer 160 “performs the function of a passivation layer,” regardless of which material is used. Jin ¶50.

60. Moreover, the list of possible materials Jin recites for the antireflection film/passivation layer 160 substantially overlaps with the list of passivation layer materials recited in the 104 Patent. EX1009-Jin ¶50; EX1001 at 11:33-39. Both include silicon nitride, silicon oxynitride, MgF₂, ZnS, TiO₂ and CeO₂, for example.

61. Dr. Peckerar’s argument in ¶¶163-168 is based on a false premise—that my first declaration replaces the tunnel oxide missing from the gap T isolation region in the combination of Jin and Feldmann with the same material, silicon oxide—and thus is not relevant.

D. Response to Dr. Peckerar’s Comments that Feldmann Discourages the Combination with Jin

62. Dr. Peckerar attacks the combination of Jin and Feldmann on the purported basis that Feldmann suggests that full rear metallization is required in order to benefit from Feldmann’s TOPCon structure.

63. First, Dr. Peckerar focuses on Feldmann’s comments that Feldmann’s teachings are contrary to “point contact rear passivation schemes.” EX2002 ¶244.

But the embodiments in Jin that I relied on in my opening declaration do not have “point contacts,” so this comment by Feldmann is irrelevant.

64. Notably, in ¶244 of Dr. Peckerar’s declaration, he quotes Feldmann but omits language providing important context for Feldmann’s comment, which is that Feldmann is distinguishing TOPCon structures from “PERL” cells: “Contrary to point contact rear side passivation schemes like PERL...” EX1012-Feldmann, 274. “PERL” stands for “Passivated Emitter and Rear Locally diffused” cells. EX1022-Luque, 261, Fig. 7.2. The excerpted figure below from the Luque textbook depicts a PERL cell. *Id.* As shown, PERL cells have small point contacts in the rear side. These point contacts are formed through contact windows in the oxide layer, denoted “SiO_x” in the figure below, electrically connecting the substrate to the rear “Al electrode.”

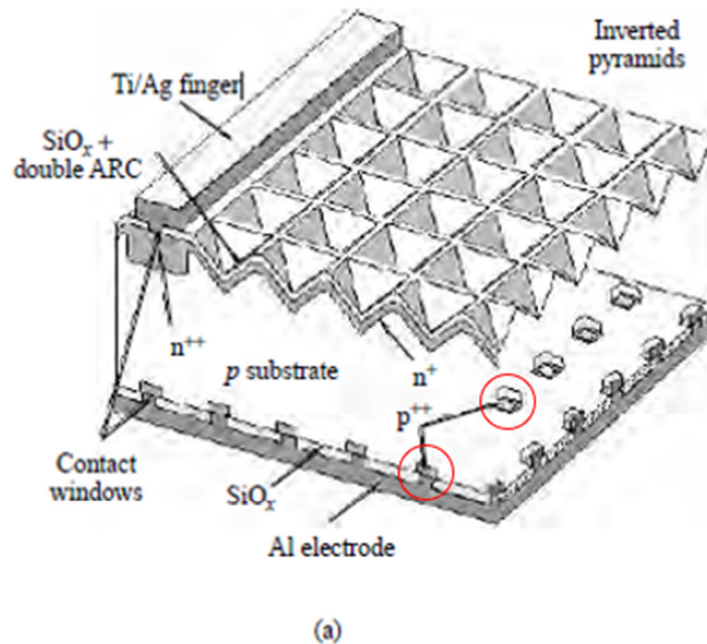


Figure 7.2 (a) Passivated emitter and rear locally diffused (PERL) cell; and (b) industrial cell with screen-printed contacts. (Not to scale)

65. These point contacts are necessary because in PERL cells, the SiO_x oxide layer (which is an insulator) is too thick to allow current to tunnel through; charge carriers are thus only able to pass through the oxide layer via the point contacts. For example, the 2008 article *High efficiency n-type Si solar cells on Al_2O_3 -passivated boron emitters* by Jan Benick and others describes PERL cells in which “[t]he rear surface exhibits a local P diffusion ($R_{\text{sheet}} \approx 20 \, \Omega/\text{sq}$) and is covered **with a 100 nm thick thermally grown SiO_2** .” EX1046-Benick, 3. It is the PERL cell in the Benick article (reference [22] in Feldmann) that Feldmann is citing and contrasting. EX1012-Feldmann, 272 (“Thus, the latter [TOPCon structure] allows for a one-dimensional carrier transport in the base, thereby leading to a FF which is more than 1% absolute higher than the FF of a PERL solar

cell featuring a similar front side [22].”). As Feldmann explains, “20 Å is the maximum tolerable oxide thickness... at which tunneling becomes inefficient and, thus, results in a lowered FF.” EX1022-Feldmann, 271. Accordingly, Benick’s 100nm-thick oxide layer (which is 1000 Å) is not a tunneling layer, which is why point contacts are needed in PERL cells.

66. Feldmann, on the other hand, uses a tunnel oxide layer that is only around 14 Å thick, which is thin enough that it “does not hinder majority charge carrier transport across its barrier.” EX1022-Feldmann, 272. For this reason, when a tunnel oxide layer like Feldmann’s is used, “point contacts” like those in PERL cells are not needed. The Jin/Feldmann combination (and Chang/Jin combination) discussed in my opening declaration has a tunnel oxide, like that taught by Feldmann, and thus neither has nor needs point contacts to operate. See EX1003, ¶¶128, 213. Feldmann’s criticism of “point contact rear side passivation schemes like PERL” is thus inapplicable to the proposed combinations, because they have tunnel oxides like Feldmann’s.

67. Moreover, instead of “point contacts,” Jin teaches the use of “finger” electrodes. A “finger” electrode is not a single point contact, but rather a long, thin contact that runs roughly the length of a solar cell, like those depicted in the figures from the Luque textbook below. See, e.g., Luque Figure 8.6 (shown below); see also EX1041-Swanson, 1:51-53 (“*Unlike the interdigitated contact cell having*

alternate p and n fingers, [in point contact cells,] the contact metal touches the silicon only *in an array of points* on the back surface.”) (emphasis added).

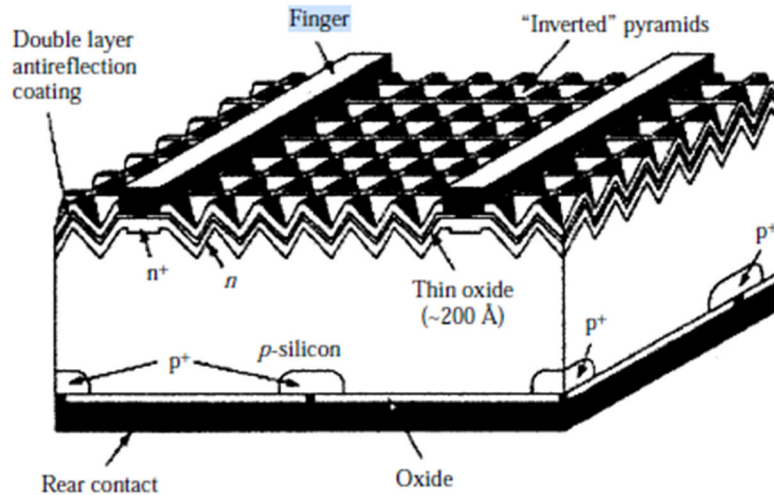
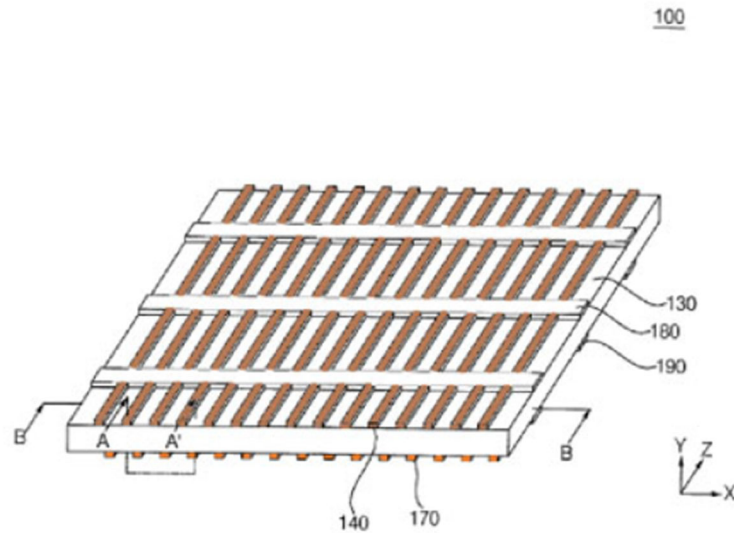


Figure 8.6 Structure of the test cells whose parameters are given in Table 8.1

68. Jin’s “finger” electrodes are no different than the finger electrodes in Luque and Swanson. Jin’s finger electrodes 140 are clearly shown in Fig. 1 (reproduced below) as a series of parallel lines that extend the length of the solar cell. EX1009-Jin ¶ 26; EX1003 ¶152.

FIG. 1



69. By contrast, unlike a finger contact, a “point contact” occupies a very small squarish area in the form of a “point,” rather than a long line. The figure from Luque below shows a PERL cell with the small, localized “point” contacts on the back of the cell, circled in red. The figure also shows a long finger electrode on the front of the cell, for comparison.

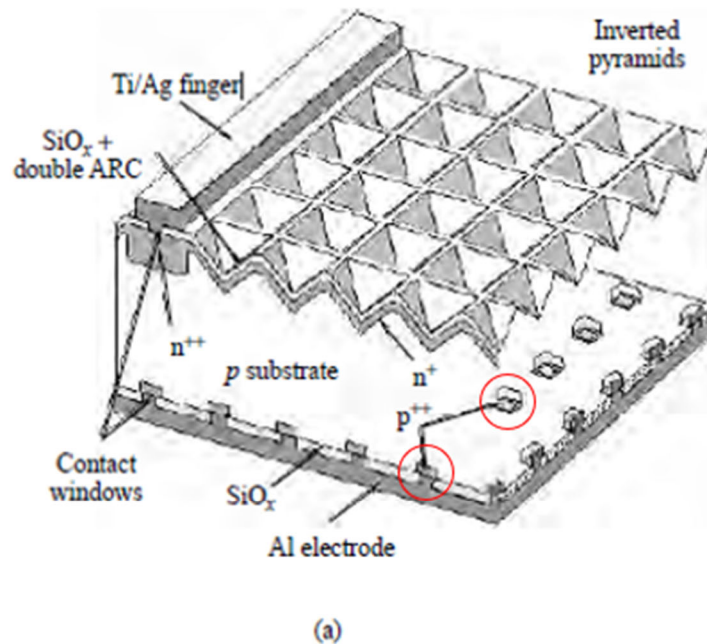


Figure 7.2 (a) Passivated emitter and rear locally diffused (PERL) cell; and (b) industrial cell with screen-printed contacts. (Not to scale)

70. Neither Jin, nor the proposed combination in my opening declaration, uses “point” contacts like those shown above, and Dr. Peckerar’s statement that “the proposed combination uses the very type of rear side contact Feldmann criticizes: a point contact” is simply wrong.

71. Dr. Peckerar also argues that the combined structure no longer significantly increases rear-side internal reflection. But Jin discloses a bifacial solar cell. E.g., EX1009-Jin ¶42; EX1003 ¶76. As I explained in my opening declaration: “Bifacial solar cells like that of Jin and Chang can receive light on both the front and back sides of the solar cell.” EX1003, ¶¶98, 112. Because bifacial solar cells can receive light through both surfaces, they are able to generate more power than a monofacial solar cell, that receives light through only one

surface. See, e.g., EX1022-Luque, 282 (“Bifacial cells are designed to collect light incident at both faces, which allows a boost in output power....”). Thus, the Skilled Artisan would know that the bifacial cells would boost power by absorbing external light from the rear that can more than make up for the incremental photon absorption by internal rear-reflection (which is limited to infrared light). This would not dissuade the Skilled Artisan from applying Feldmann’s TOPCon structure to a bifacial cell.

72. Dr. Peckerar tries to downplay this fact by asserting that removing the full rear metallization renders a cell less useful “on a non-reflective surface”—but this is an arbitrary observation about a particular scenario. The Skilled Artisan would understand, for example, that a bifacial solar cell like Jin’s is most useful in situations where light *is* expected to be reflected from behind the solar cell, and Dr. Peckerar has offered no reason the proposed combination would be limited to the situation where it is on a non-reflective surface. There is also no question that bifacial solar cells have been known to be extremely efficient outside of the highly specific scenario to which, without any justification, Dr. Peckerar constrains his analysis. See, e.g., Luque at 270 (“Bifacial structures in Figure 7.4 can, for the same reason, be very efficient at confining the light [66].”), 294 (“By encapsulation between two glass panes, bifacial modules offering increased power output per unit cell area can be produced without technology changes.”). Indeed,

as Luque explains, grids of finger electrodes like that used in Jin provide a favorable balance between decreasing series resistance⁵ (which generally improves as more of the surface area of a cell is covered with metal contacts) and increasing shadowing (which worsens as the amount of light that can enter the cell is blocked by metal contacts):

Even with this low-current advantage of multijunction cells, in adapting a cell from one sun to concentrator operation it may be well worth reducing series resistance. One of the most vital adaptations of a cell design for concentrator operation is the front-contact metallization. The series resistance of the cell depends on the density of front-contact grid fingers [30]; a grid design optimized for 1000 suns will have a much higher density of grid fingers than a one-sun grid. Grid-finger spacings of 200 μm or less are not unusual at 1000 suns. **Naturally, decreasing the grid-finger spacing increases the device shadowing and so decreases the current; thus, concentrator grid design involves careful trade-offs of the shadowing versus the series resistance.** Fortunately, with the sophisticated photolithography/evaporation/liftoff metallization processing used for high-efficiency devices, grid-finger widths on the order of 3 μm , with height/width aspect ratios of two or more, can be achieved. **Such finger dimensions allow a very dense packing of high-conductivity grids, while maintaining a reasonably low shadow loss.** [Luque at 378.]

73. For all of these reasons, I disagree with Dr. Peckerar's conclusion that combining Jin and Feldmann in the manner proposed results in a "less efficient" option, let alone an option so much less efficient than Dr. Peckerar's alternative combination that a Skilled Artisan would be dissuaded or discouraged from

⁵ Series resistance decreases the amount of current a solar cell can generate.

making the combination I proposed in my opening declaration given the affirmative reasons provided by both Jin and Feldmann for doing so. See EX1003, ¶¶106-114.

74. Lastly, Dr. Peckerar contends that the combination of Jin and Feldmann “eliminates [Jin’s] primary benefit: the use of increased doping density and thickness in the area of the electrodes.” EX2001, ¶248. In my opinion, Jin’s use of varied doping densities or thicknesses is not a “primary” efficiency benefit of Jin. Rather, it is just one of many mechanisms the Skilled Artisan would understand can affect efficiency. As I stated during my deposition, there are many knobs a Skilled Artisan would turn in attempt to increase efficiency in a solar cell. EX2002, 38:7-14. That is true of Jin’s teachings as well.

75. In fact, contrary to Dr. Peckerar’s “primary benefit” characterization, there are multiple express embodiments in Jin in which the BSF does *not* have varying thickness/doping densities. For example, Jin observes that the embodiment of Fig. 3 I relied on in the Jin/Feldmann combination “is not limited to” having a BSF varying doping densities/thicknesses:

In the above embodiment of FIGS. 1 to 3, the emitter layer includes the first area 124 and the second area 122 having different doping concentrations, and the back surface field layer 150 includes the third area 154 and the fourth area 152 having different doping concentrations. However, *the invention is not limited thereto*. [EX1009-Jin, ¶119.]

Accordingly, Jin states, the embodiment in Fig. 3 may also have the forms of Figs.

16 and 17, which do *not* have a BSF with varying dopant densities/thicknesses:

Thus, with reference to FIG. 15, an emitter layer 120 a may include only a second area 122 that is a shallow or lightly doping area. Also, *with reference to FIG. 16, a back surface field layer 150 a may include only a fourth area 152 that is a shallow doping area.* In addition, *with reference to FIG. 17, the emitter 120 a may include only a second area 122 that is the shallow doping area, and the back surface field layer 150 a may include only a fourth area 152 that is the shallow doping area,* simultaneously. [EX1009-Jin, ¶120.]

I have reproduced Jin Figs. 16 and 17 below.

FIG. 16

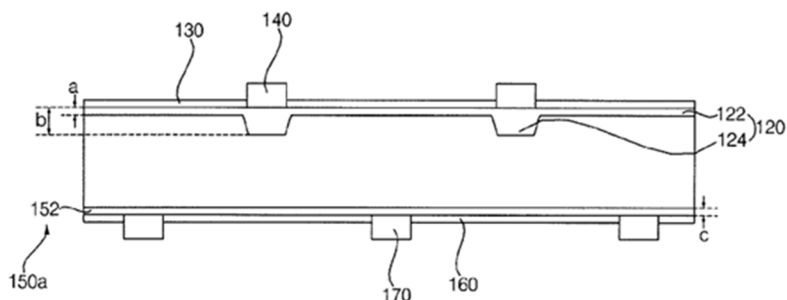
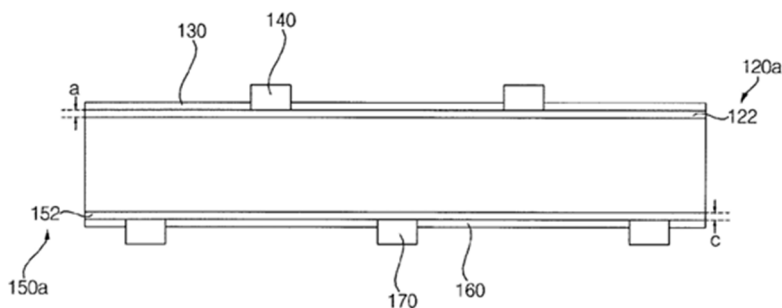


FIG. 17



76. Jin then reiterates that the embodiments of Fig. 3 “may be applied” to the embodiments of Figs. 16 and 17:

Also, the modified embodiments related to the embodiment of FIGS. 1 to 3 may be applied to the embodiments of FIGS. 15 to 17. [EX1009-Jin, ¶123.]

77. And importantly, Figs. 16 and 17 do not have the break line that is included in Fig. 3, indicating that Figs. 16 and 17 only show a small interior portion of the solar cell, and thus do not depict the edges where the isolation gap T is located. Instead, Figs. 16 and 17 show modifications to Fig. 2, which is only an excerpt of the embodiment in Fig. 3 that shows the gap T at the edges. In other words, the absence of gap T in Figs. 16 and 17 is not some special indication that those embodiments do not require or have isolation regions, as Dr. Peckerar has argued about Chang's figures.

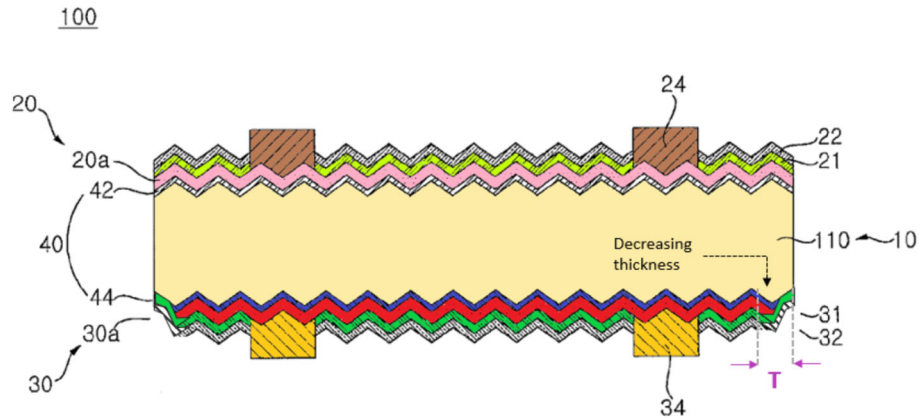
78. I pointed out during my deposition, before Dr. Peckerar signed his declaration, that Jin discusses embodiments that do not have a BSF where the doping density/thickness varies, yet he did not take into account Figures 16 and 17 at all in his declaration. EX2002, 39:5-13.

**V. THE COMBINATION OF CHANG AND JIN AND
THE COMBINATION OF JIN AND FELDMANN RENDER
OBVIOUS CLAIM 8**

79. Finally, I disagree with Dr. Peckerar's conclusions regarding claim 8. For both the Chang/Jin combination and Jin/Feldmann combination, Dr. Peckerar asserts that the combinations in my opening declaration do not satisfy claim 8's requirement that the polysilicon layer "*progressively decrease toward the isolation*

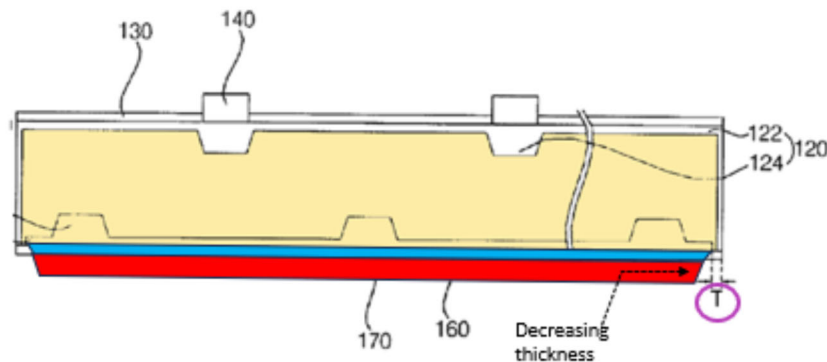
region” because the tapering of polysilicon material under the shadow mask means that small amounts of polysilicon are supposedly *in* the isolation region. See EX2001, ¶¶258-264, 300. I disagree.

80. Dr. Peckerar simply ignores that, even with the overspray of the polysilicon, there is still a gap between the edge of the substrate and the polysilicon/tunnel oxide in which there would be no polysilicon, and which would be an “*isolation portion*” as claimed. Dr. Peckerar also ignores that in my opening declaration, I specifically identified the areas not covered by polysilicon/tunnel oxide as the claimed “*isolation portions*.” For example, for the Chang/Jin combination, I explained in my analysis of claims 1 and 8 that “Chang discloses an ‘isolation region’... that excludes the ‘tunneling layer 44’ and ‘back surface field area 30’ (*first conductive type semiconductor region*)”, and that the “shadow mask approach would result in a taper in the back surface field area 30 (red) at the edges of the mask into the mask ‘shadow’ regions, ***towards the isolation region.***” EX1003, ¶¶223, 247 (emphasis added). Thus, my declaration is clear that the isolation region is the area at the edge of the back surface of the substrate that is not covered by either red polysilicon or blue tunnel oxide.



81. Likewise, in my analysis of claims 1 and 8 for the Jin/Feldmann combination, I explained that “[i]n the proposed combination of Jin and Feldmann, gap T is an ‘isolation portion’ as claimed,” and that using the “shadow mask approach in Jin/Feldmann would result in a taper in the polysilicon layer (red) at the edges of the mask into the mask ‘shadow’ regions, *towards the gap T isolation region*,” which is depicted as the area not covered by the blue polysilicon and red tunnel oxide. EX1003, ¶¶146, 163.

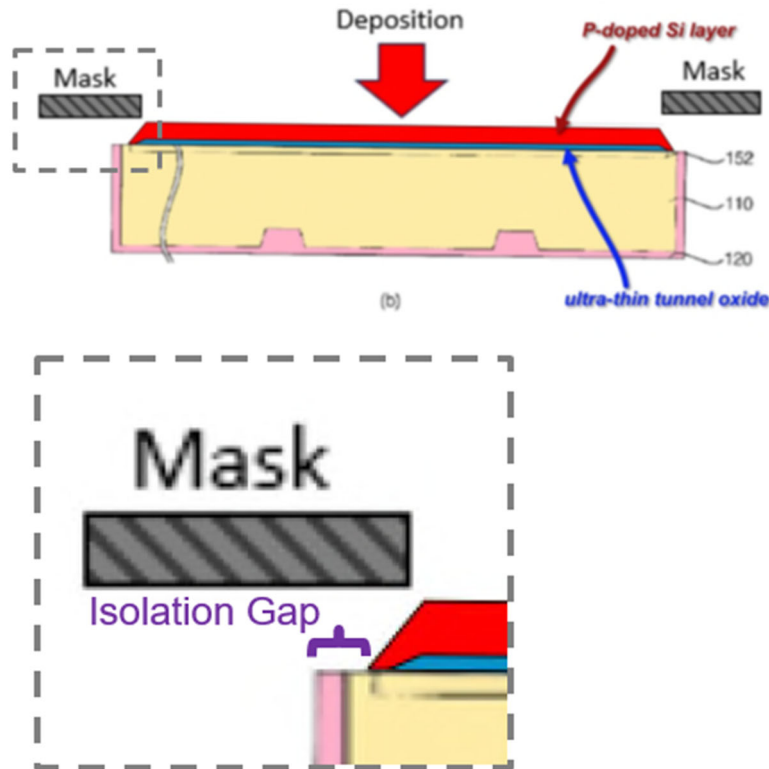
FIG. 3



82. Dr. Peckerar appears to be suggesting that the isolation region must have the same width as the thickness of the mask used to create the isolation region, but the claimed “*isolation portion*” is not defined by the thickness of the mask, if any, used to create it. Nor does the 104 Patent define or describe the “*isolation portion*” this way. Instead, consistent with how my opening declaration identifies the isolation region of the Chang/Jin and Jin/Feldmann combinations that corresponds to the claimed “*isolation region*,” the 104 Patent specification and claim 1 simply describe the isolation portion in the patent as the area at the edge of the back surface of the substrate not covered by either the polysilicon emitter layer or the tunnel oxide. *See* EX1001, FIG 2, 7:53 (defining “I” as “isolation portion I” in FIG. 2); 13:6-12 (defining “isolation portion I” as the region “in which the tunnel layer 160 and the first conductive type semiconductor region 170... are not formed”).

83. Finally, Dr. Peckerar even includes a figure in his declaration he contends represents the “more likely” way a Skilled Artisan would combine Jin and Feldmann, which I have reproduced below with an annotated inset. *See* EX2001, ¶218. Even in Dr. Peckerar’s “more likely” combination, there is still a gap between the edge of the substrate and the polysilicon where there is also no tunnel oxide, and where the pink colored emitter is separated from the red-colored

polysilicon BSF. Thus, the Skilled Artisan would understand that this gap is an “*isolation portion*” as claimed, toward which the red polysilicon layer is tapering.



VI. OPINIONS REGARDING EVIDENCE CITED IN HEREIN

84. I have been asked to offer opinions concerning some of the evidence I cite in my supplemental declaration: EX1039, EX1040, EX1042, EX1043, EX1044, and EX1046.

85. I am and have been throughout my career personally familiar with each of the journals identified in EX1039, EX1040, EX1042, EX1044, and EX1046. I have read many papers published in these journals during the course of my career, and have myself published papers in many of them. Each cited journal

is a well-known, reputable, reliable, and authoritative periodical which publishes compilations of scientific and technical publications and would be generally known to those in the field of solar cell design or manufacture.

86. Moreover, I have inspected each of the articles identified as EX1039, EX1040, EX1042, EX1044, and EX1046. In my opinion, and based on my experience with the journals identified in EX1040, EX1042, EX1044, and EX1046 and on the appearance, contents, substance, and distinctive characteristics of the exhibits, each listed exhibit is what it appears to be, *i.e.*, an article published in the journal with which it is associated in the exhibit. Indeed, I see nothing in any of those exhibits to suggest that the exhibit is not what it appears to be, or which raises any doubt as to the exhibit's authenticity or accuracy.

87. I am also personally familiar with the textbook identified as EX1043 (Ghandhi). I have used various versions of Ghandi's textbook, including the 1994 version submitted as EX1043, over at least the last 20 years. I have inspected the exhibit, and in my opinion, and based on my experience with the textbook identified in EX1043 and on the appearance, contents, substance, and distinctive characteristics of the exhibit, it is what it appears to be, *i.e.*, a digital copy of the 1994 version of the Ghandhi textbook. I see nothing in EX1043 to suggest that the

exhibit is not what it appears to be, or which raises any doubt as to the exhibit's authenticity or accuracy.⁶

88. Also, in my opinion, and based on my experience, the dates on the exhibits of EX1039, EX1040, EX1042, EX1043, EX1044, and EX1046 are reliable and trustworthy because journals and publishers of the type listed in these exhibits have a reputational incentive to accurately publish the submissions each such journal or textbook receives, including by attaching an accurate publication date on such documents. Any such journal or publisher that was known to publish inaccurate information, including publication dates, would likely soon not be read by those in the field. Indeed, if such journal or publisher were not reliable, they would quickly cease to operate because those working in the field would not author articles or books for them.

89. Moreover, it would be very difficult for such dates to be mistakenly or intentionally altered because the underlying document remains available to those working in the field, including the authors and the general public, from the journals in EX1039, EX1040, EX1042, EX1044, and EX1046 and the textbook in EX1043

⁶ Although there are some handwritten notes on the inside cover in EX1043 identifying a past owner of the textbook, I have not relied on these in forming any of my opinions.

themselves. Any question as to the date of a paper published in any of the journals or the textbook in these exhibits could therefore easily be verified and resolved.

90. It is also my opinion that the exhibits identified as EX1039, EX1040, EX1042, EX1043, EX1044, and EX1046 are the most probative and best source for both the content of the exhibit and the date of that content's publication because other ways of obtaining that information such as personally contacting the author(s) and publishers of the exhibits, would require an unreasonable amount of effort given the publicly available nature of the exhibits.

Appendix A:
Materials Relied On

Materials Relied On

The list of documents that I relied upon in forming my opinions is below.

Exhibit #	Reference Name
1001	U.S. Patent No. 9,722,104 (“104 Patent”)
1005	File History of U.S. Patent No. 9,722,104
1006	File History of U.S. Patent No. 10,014,419
1007	Korean Patent App. No. 10-2014-0168624 with certified translation
1008	Korean Patent App. No. 10-2015-0122846 with certified translation
1009	U.S. Patent App. Publication No. 2013/0056051 to Y. Jin, <i>et al.</i> (“Jin”)
1010	F.A. Lindholm, <i>et al.</i> , Heavily Doped Polysilicon-Contact Solar Cells, IEE Electron Device Letters, Vol. EDL-6, No. 7, (IEEE 1985) (“Lindholm”)
1011	Y.H. Kwark, <i>et al.</i> , N-Type SIPOS and Poly-Silicon Emitters, Solid-Stare Electronics, Vol. 30, No. 11, 1121-1 125 (1987) (“Kwark”)
1012	F. Feldmann, <i>et al.</i> , “Passivated rear contacts for high-efficiency n-type Si solar cells providing high interface passivation quality and excellent characteristics,” Solar Energy Materials & Solar Cells 120 (2014) 270-274 (2013 Elsevier B.V.) (“Feldmann”)
1013	U.S. Patent App. Publication No. 2014/0299187 to J. Chang, <i>et al.</i> (“Chang”)
1014	Japanese Patent App. Publication No. JP 2010-186862 to T. Watabe, <i>et al.</i> (“Watabe”) with certified translation
1015	U.S. Patent No. 8,647,914 to K. Seo, <i>et al.</i> (“Seo”)
1020	June 21, 2022 USPTO Director’s Memo
1021	M. Quirk, <i>et al.</i> , Semiconductor Manufacturing Technology (Prentice-Hall Inc. 2001)

Exhibit #	Reference Name
1022	A. Luque, <i>et al.</i> , Handbook of Photovoltaic Science and Engineering (John Wiley & Sons Ltd. 2003)
1023	Trina Solar n-type TOPCon Advanced technology steps onto the world stage, with efficiency reaching 26% in mass production and 700W+ in module power, <i>available at</i> https://www.trinasolar.com/us/trina-solar-n-type-vertex-to-reach-700gw (last visited August 19, 2024)
1024	Y. H. Kwark, <i>et al.</i> SIPOS Heterojunction contacts to silicon, 1984 International Electron Devices Meeting (1984): 742-745 (“Kwark II”)
1025	SY Lien, <i>et al.</i> , Tri-layer antireflection coatings (SiO ₂ /SiO ₂ —TiO ₂ /TiO ₂) for silicon solar cells using a sol-gel technique, Solar Energy Materials & Solar Cells 90, 2710-2719 (2006)
1026	D. Kray, <i>et al.</i> , Study on the edge isolation of industrial silicon solar cells with waterjet-guided laser, Solar Energy Materials & Solar Cells, 91, 1638–1644 (2007)
1027	Merriam-Webster’s Collegiate Dictionary, 10th Ed. (Merriam-Webster, Inc. 1998) (definition of “periphery”)
1028	S. Duttagupta, <i>et al.</i> , Progress in Surface Passivation of Heavily Doped n-Type and p-Type Silicon by Plasma-Deposited AlO _x /SiN _x Dielectric Stacks, IEEE Journal of Photovoltaics, Vol. 3, No. 4 (October 2013)
1029	Oxford College Dictionary, 2nd Ed. (Oxford University Press, Inc. 2002)
1030	B. Streetman and S. Banerjee, Solid State Electronic Devices, 6th Ed. (Prentice-Hall Inc. 2006)
1031	M. Scherff, Novel method for preparation of interdigitated back contacted a-Si:H/c-Si heterojunction solar cells, 26th European Photovoltaic Solar Energy Conference and Exhibition (2011)
1032	W. Decker, <i>et al.</i> , “Novel low pressure sputtering source and improved vacuum deposition of small patterned features using precision shadow

Exhibit #	Reference Name
	masks,” 59th Annual Technical Conference Proceedings (Society of Vacuum Coaters 2016)
1033	H. Okuyama, <i>et al.</i> , Position-selective growth of carbon nanotubes on Ni catalysts/Mo underlayers by thermal chemical vapor deposition, J. Mater. Res., Vol. 21, No. 11 (Materials Research Society 2006)
1034	T. Saga, Advances in crystalline silicon solar cell technology for industrial mass production, NPG Asia Materials, Volume 2, 96–102 (2010)
1036	U.S. Patent Pub. No. 2012/0003781 to Yun, <i>et al.</i> (“Yun”)
1038	U.S. Patent No. 9,153,728 to A. Rohatgi, <i>et al</i> (“Rohatgi”)
1039	E. Yablonovitch, <i>et al.</i> , A 720 mV open circuit voltage SiO _x :cSi:SiO _x double heterostructure solar cell, Applied Physics Letters 47, 1211 (1985)
1040	M. Stöhr, <i>et al.</i> , PECVD Shadow Mask Deposition of Amorphous Silicon – A Shortcut to Local Passivating Contacts,
1041	U.S. Patent No. 4,927,770 to R. Swanson, <i>et al.</i> (“Swanson”)
1042	A. Boogaard, Negative Charge in Plasma Oxidized SiO ₂ Layers, ECS Trans. 35 (4) 259-272 (2011)
1043	S. Ghandhi, VLSI Fabrication Principles – Silicon and Gallium Arsenide, John Wiley & Sons, Inc. (1994)
1044	B.K. Ip., <i>et al</i> , Charges and Defects In SiO ₂ Films Deposited By Plasma-Enhanced Chemical Vapor Deposition at Low Temperatures, Solid-State Electronics Vol. 34, No. 2, pp. 123-129 (1991)
1046	J. Benick, <i>et al.</i> , High efficiency n-type Si solar cells on Al ₂ O ₃ -passivated boron emitters, Applied Physics Letters 92, 253504 (2008)