

IPR2025-00006 and -00007

Runergy USA Inc. et al. v. Trina Solar Co. Ltd.

Petitioner Runergy's Demonstrative Exhibit

Hearing Date: January 29, 2026

Grounds

IPR2025-00006¹ – US10,230,009

Ground	Claims	35 U.S.C. §	Prior Art Combination
1	1-8, 11-13, 15, 17	103	Jin and Feldmann
2	16	103	Jing, Feldmann, and Chang
3	1-8, 11-13, 15-17	103	Chang and Jin
4	9-10	103	Jin, Feldmann, and Seo
5	9-10	103	Chang, Jin, and Seo
6	14	103	Jin, Feldmann, and Watabe
7	14	103	Chang, Jin, and Watabe

IPR2025-00007 – US9,722,104

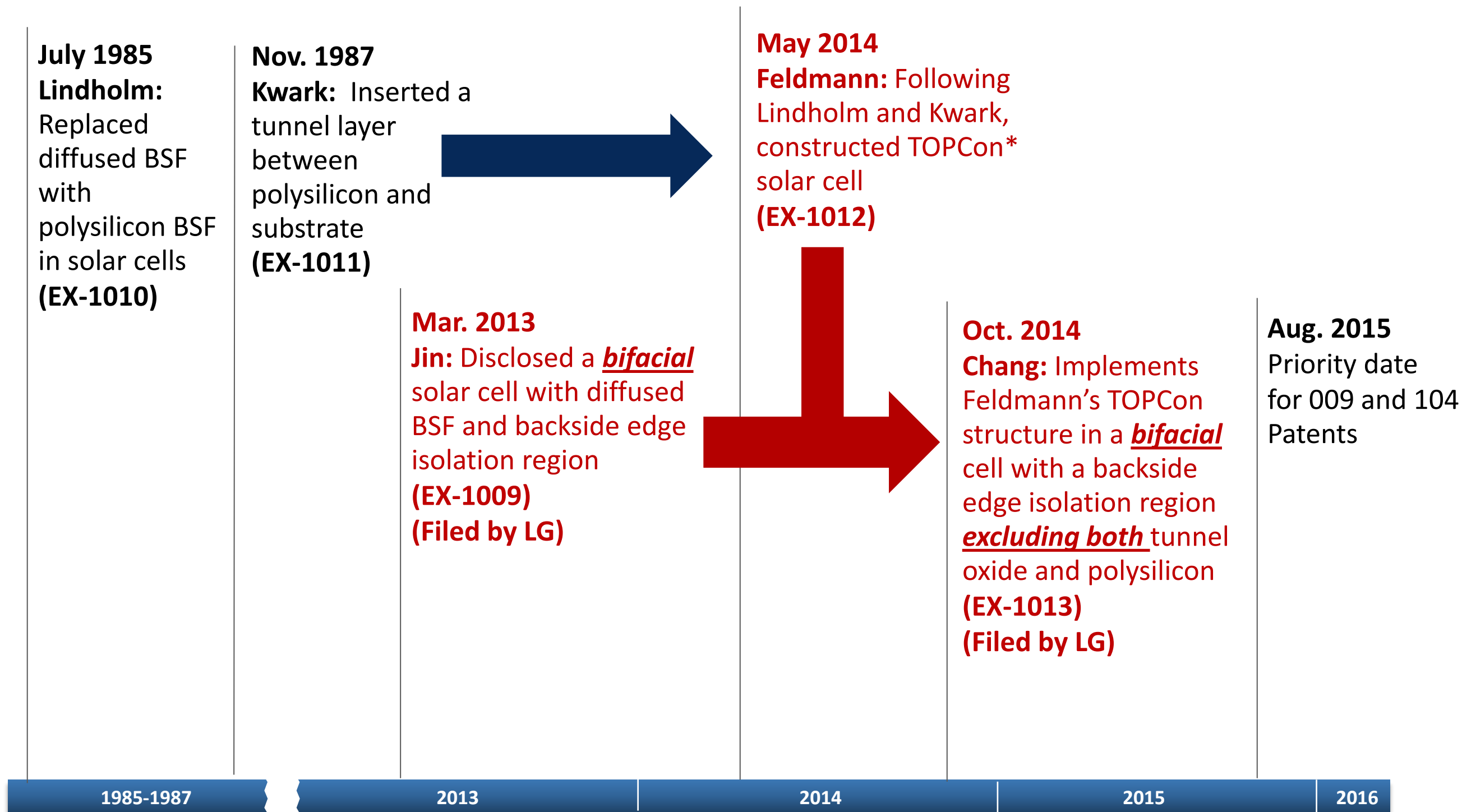
Ground	Claims	35 U.S.C. §	Prior Art Combination
1	1-6, 9-10	103	Jin and Feldmann
2	1-6, 9-10	103	Chang and Jin
3	7-8	103	Jin, Feldmann, and Seo
4	7-8	103	Chang, Jin, and Seo
5	11	103	Jin, Feldmann, and Watabe
6	11	103	Chang, Jin, and Watabe

1. All citations herein refer to the -006 IPR papers for simplicity.

Undisputed Issues

- TOPCon solar cells were known before the 009 and 104 patents
 - Effective filing date of 009/104 patents is August 31, 2015
- PO does not dispute satisfaction of the elements of the claims, except:
 - the claimed “*isolation portion*” limitation in claim 1;
 - “*opening formed in the first passivation film*” in claim 1 (by Jin/Feldman combination only)
 - the “*progressively decreases towards the isolation portion*” in dependent claims 8 (009 Patent) or 6 (104 Patent)
- Secondary considerations weigh in favor of obviousness
 - No commercial success and nexus
 - No unexpected results
 - No long felt and unresolved need
- The Seo or Watanabe references are appropriately combined with Petitioner’s other references

Timeline of Prior Art



Pet. at 14-23

EX1003-Banerjee, ¶¶75-77; 109-117

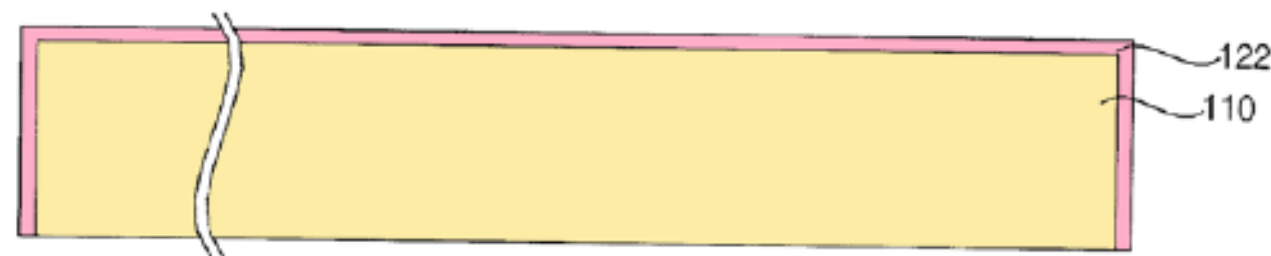
*TOPCon = tunnel oxide with polysilicon BSF for back surface passivation

Disputed Issues

- Jin/Feldmann combination: (Ground 1)
 - Motivation for isolation portion, tunnel oxide edge exclusion, and bifaciality
 - Whether a tunnel oxide layer is sufficient to prevent shorting
 - Including tunnel oxide at the edge vs. excluding tunnel oxide at the edge
 - Bifacial vs. monofacial (opening-in-passivation-layer issue)
 - Reasonable expectation of success of using shadow mask
- Chang/Jin combination: (Ground 3 (009) and Ground 2 (104))
 - Chang's disclosure of a backside isolation portion at the edge

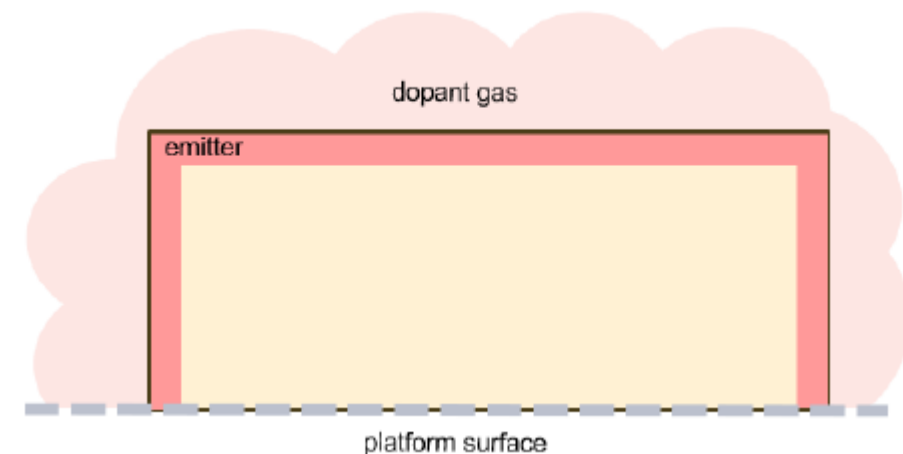
The Problem of Shorting: Front Dopants Diffusing Into Side Walls Also

Diffusion of dopants to form the front emitter layer *also* diffuses dopants into the lateral sides of the substrate



EX1009-Jin, FIG. 7(b)

(b)



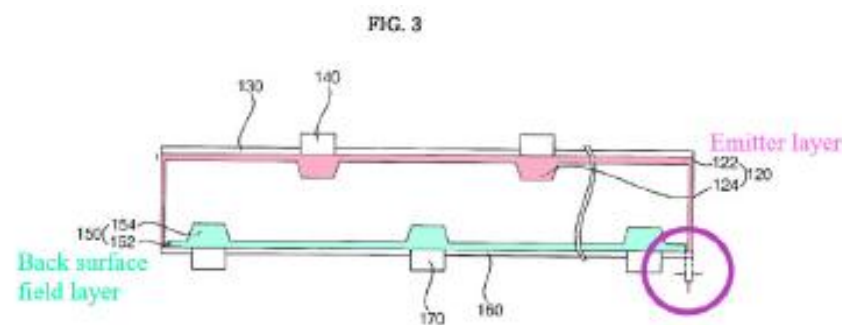
As a result, a flat-lying substrate exposed to dopant vapor during thermal diffusion will have dopants diffused into not only the top surface of the substrate, but also the exposed lateral side surfaces. This phenomenon is illustrated, for example, in Figure 7(b) of Jin below, in which the yellow n-type substrate 110 is diffused with p-type dopants to form the pink emitter layer 120 (“second area 122”), resulting in p-type doping along both the top and the lateral sides of the substrate. EX1009-

Jin, ¶78, Fig. 7(b).

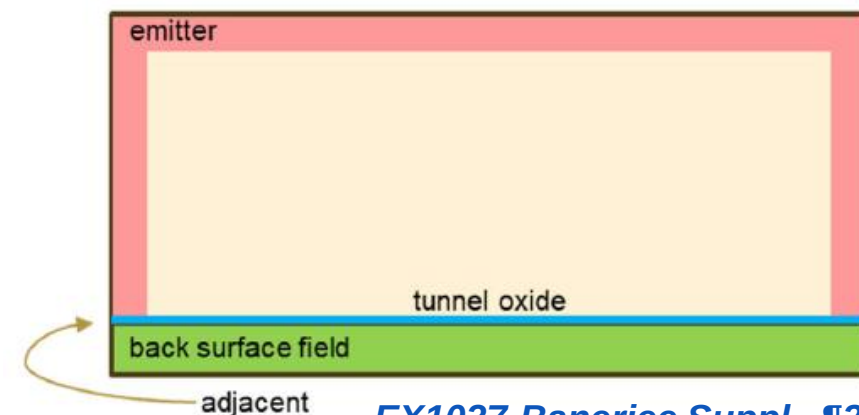
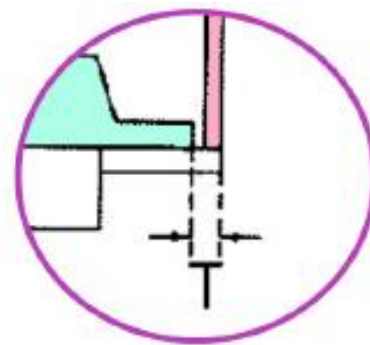
EX1003-Banerjee, ¶71
Pet. at 11-12; Reply at 6-7

The Problem of Shorting: Electrical Contact with the Sidewall Dopants

When the back surface field is applied, the two oppositely doped, adjacent regions come in electrical contact leading to shorting, absent an isolation region



EX1009-Jin, FIGs. 3 & 11



EX1037-Banerjee Suppl., ¶25

because of the dopants present on the side of the substrate, when the back surface field layer is subsequently formed on the back surface, the heavily doped p⁺ emitter and heavily doped n⁺ back surface field region may come in contact on the sides of the wafers. When this happens, the electrical pathway for the electrons and holes can become shorted between the emitter region and the back surface field along the side of the substrate, reducing the current output to the electrodes.

EX1003-Banerjee, ¶73
Pet. at 11-12; Reply at 6-7

Undisputed: Jin, Feldmann, Chang, and 009/104 Patents Disclose Diffusion to Form the Front Emitter Layer

5. The solar cell of claim 1, wherein the emitter region is formed by diffusing the impurities of the second conductive type into the second surface of the semiconductor substrate.

009 Patent, Claim 5

Jin's emitter layer 120 is formed via a "heat diffusion method" and when the substrate 110 is N-type, the emitter layer 120 is doped with a P-type impurity, e.g., Boron. EX1009-Jin, ¶¶47, 78. Feldmann likewise discloses a "diffused boron-doped emitter" on an "n-type silicon solar cell." EX1012-Feldmann, §1, Fig. 3; EX1003-Decl., ¶¶156-58.

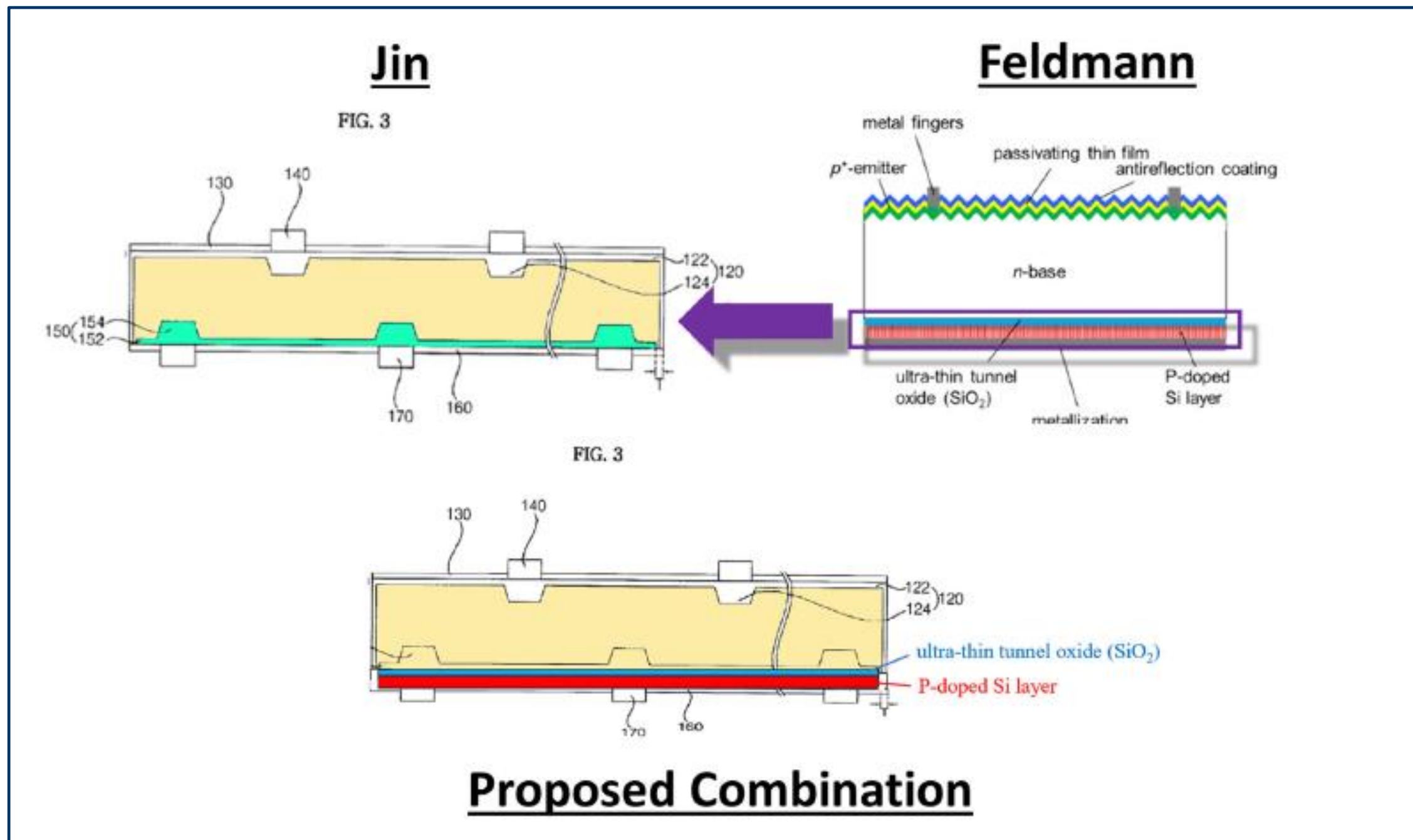
Pet. at 42

substrate." In Chang, the "emitter area 20" is formed "in the semiconductor substrate 10" front surface by "thermal diffusion" of a "dopant having a conductive type different from the semiconductor substrate." EX1013-Chang, ¶98. Thermal diffusion diffuses the dopant into the surface of the semiconductor substrate. EX1003-Decl., ¶259.

Pet. at 70

Maintaining the Isolation Portion in the Jin/Feldmann Combination Would Have Been Necessary and Obvious

- The proposed combination applies a known technique (Feldmann's TOPCon structure) to a similar device (Jin's bifacial solar cell with isolation region) to address a known problem (recombination and electrical shorting)



Patent Owner's Arguments

This is nothing more than an exercise in impermissible hindsight. Because it eliminated Jin's back surface field layer, Petitioner also eliminated the need to include Jin's gap (or distance) T in its current form. As the back side of the substrate is no longer doped via an ion implantation process, a POSITA would have formed the two new layers discussed in Feldmann differently. And when doing so, a

PO Response at 16

120. (See Ex. 2001, ¶¶ 118-131.) The tunnel oxide physically separates the two layers. Moreover, silicon dioxide—the material used to form the tunnel oxide layer—operates as a diffusion barrier. (See *id.*, ¶ 132; see also Ex. 2003, 2:41-46 (noting that an “oxide layer substantially prevents diffusion of dopants out of” one layer into another layer).) Thus, the presence of the tunnel oxide limits the ability of impurities in the polysilicon layer to diffuse into Jin's substrate. Put another way, because the back side of the substrate is no longer doped via ion implantation, the modified version of Jin proposed by Petitioner is no longer in need of the same type of gap (or distance) T shown in Jin's figures.

PO Response at 22

Dr. Banerjee: Tunnel Oxide Layer Does Not Prevent Shorting And Allows Current to Pass Through

5. Inserting a tunnel oxide between the BSF and the substrate does not obviate the need to separate the BSF from the edge of the substrate to prevent shorting because tunnel oxides would not prevent *electrical* contact between the BSF and the emitter.

considered an insulator that does not conduct electrical current, because of the thinness of the tunnel oxide, electrons and other charge carriers are able to pass directly through the tunnel oxide through a quantum mechanical process known as “tunneling”—that is the very reason it is called a *tunnel* oxide—even though such

EX1037-Banerjee Suppl., ¶15; Reply at 12, and 20

[0057] The second tunneling layer 44 passivates the surface of the semiconductor substrate 10 having many recombination sites and facilities transfer of carriers through a tunneling effect.

EX1013-Chang, ¶57; Reply at 12

Most importantly, the tunnel oxide layer needed for passivation does not hinder majority charge carrier transport across its barrier and thus allows for excellent FFs of above 82%. From SunsVoc

EX1012-Feldmann, 272; Reply at 20

Dr. Banerjee: Tunnel Oxide Layer Allows Diffusion of Dopants into Substrate, Particularly When Heated

barrier.” EX2001, ¶132. However, the silicon oxide has to be thick enough to block diffusion, particularly when dopants are exposed to high temperatures during the manufacturing process. A tunnel oxide is too thin to block diffusion of dopants from the polysilicon BSF into the substrate.

EX1037-Banerjee Suppl., ¶¶ 9-15; Reply at 13

[0149] Then, as shown in FIG. 16C, the second conductive type dopant in the first portion 20a is diffused into the semiconductor substrate 10 by thermal treatment to form the second portion 20b of the emitter area 20, and the first conductive type dopant in the first portion 30a is diffused into the semiconductor substrate 10 to form the second portion 30b of the back surface field area 30. As such, in the embodiment of the

EX1013-Chang, ¶149; Reply at 13

The annealing step (9) follows SIPOS deposition. This step is necessary to precipitate microcrystalline silicon grains within the material and to activate the phosphorus dopant. In addition during this step the phosphorus diffuses about 20–50 Å into the silicon wafer as measured by secondary ion mass spectrometry. This produces a very shallow n^+ accumulation layer which is transparent to minority carriers; i.e., the holes from the bulk “see” the Si-SiO₂ interface.

EX1039-Yablonovitch, 1212; Reply at 13
See also, EX1024-Kwark ¶742; Reply at 13

PO's Expert: Oxide Layer Has to Be “Considerably Thicker” than Tunnel Oxide to Block Diffusion

Q So you would agree that for SiO₂ to act as a diffusion barrier it would need to be significantly thicker than the thickness of a typical tunnel layer?

MR. De BLANK: Objection. Incomplete hypothetical, vague, outside the scope of the report.

A To be an effective diffusion barrier, it would have to be considerably thicker than a tunnel layer. Yeah.

EX1045-Peckarar Depo., 182:8-17; Reply at 13

Chang Implemented Feldmann's TOPCon Structure with An Isolation Portion at the Backside Edge

- Chang discloses excluding **both** the tunnel layer 44 and the back surface field 30 in the “periphery region, isolation region”

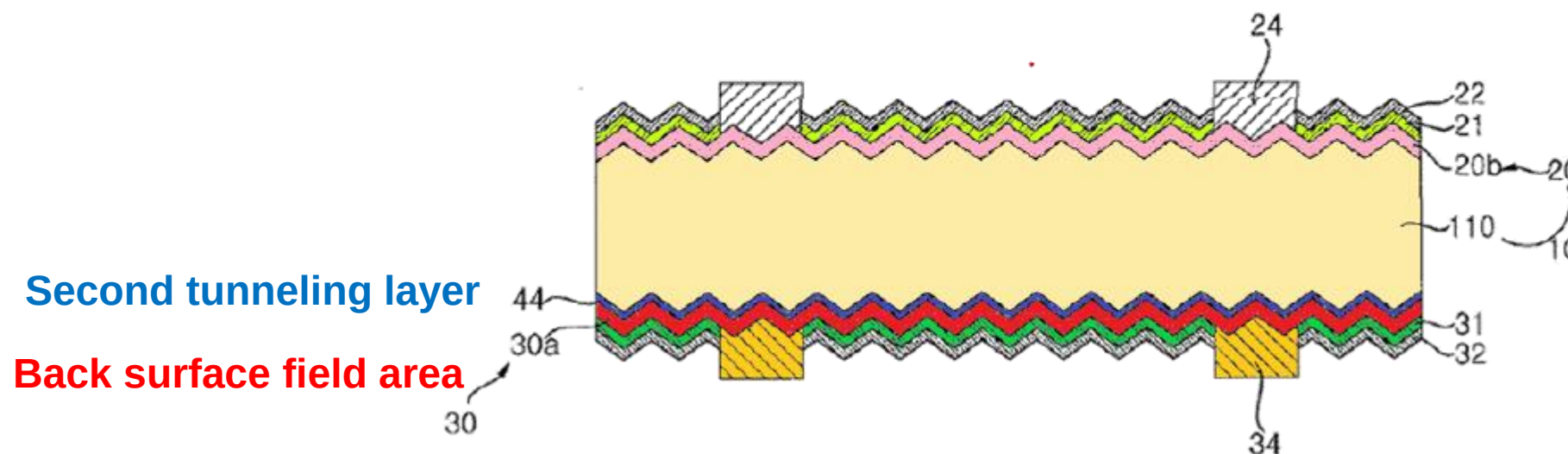
[0056] Meanwhile, a second tunneling layer 44 is entirely formed over another surface (for example, back surface, hereinafter, referred to as a “back surface”) of the semiconductor substrate 10. As used herein, the expression “entirely formed” means that an element such as a layer is formed over an entire surface without an empty area or a non-coverage area, or is formed in an entire area excluding pre-designated or inevitably formed regions such as periphery region, isolation region or the like.

EX1013-Chang, ¶56
Pet. at 26, 62-66

[0062] In the embodiment of the invention, the back surface field area 30 may be entirely formed over the second tunneling layer 44. As used herein, the expression “entirely formed” means that an element such as a layer is formed over an entire surface without an empty area or a non-coverage area, or is formed in an entire area excluding pre-designated or inevitably formed regions such as periphery region, isolation region or the like.

EX1013-Chang, ¶62
Pet. at 26, 62-66

FIG. 8



Disputed Issues

- Jin/Feldmann combination: (Ground 1)
 - Motivation for isolation portion, tunnel oxide edge exclusion, and bifaciality
 - Whether a tunnel oxide layer is sufficient to prevent shorting
 - Including tunnel oxide at the edge vs. excluding tunnel oxide at the edge
 - Bifacial vs. monofacial (opening-in-passivation-layer issue)
 - Reasonable expectation of success of using shadow mask
- Chang/Jin combination: (Ground 3 (009) and Ground 2 (104))
 - Chang's disclosure of a backside isolation portion at the edge

Dr. Banerjee Explains That POSA Would Have Understood Chang to Disclose an Edge Isolation Portion

241. Second, to a Skilled Artisan in this field, “isolation” means the introduction of a non-conductive separation, which can either be physical, electrical, or both, between two electrical or conductive components in order to prevent them from inadvertently cross-talking. For example, in a 2009 textbook I

EX1003-Banerjee, ¶241; Pet. at 63-65

243. In Chang’s solar cell, when the tunneling layer 44 and back surface field 30 are not formed in a certain portion or region of the back surface, i.e., the isolation region, it leaves a physical gap. And this physical gap prevents the conductive front emitter area 20 from contacting the conductive back surface field 30.

EX1003-Banerjee, ¶243; Pet. at 63-65

Dr. Banerjee Explains That POSA Would Have Understood Periphery to Refer to the Perimeter or Outer Limits

244. Third, Chang specifically refers to the “periphery region,” which denotes the location where the solar cell excludes the formation of the tunneling layer 44 and back surface field area 30, i.e., the location of the “isolation region.” EX1013-Chang, ¶¶56, 62. Webster Dictionary defines “periphery” as “the perimeter of a circle or other close curve, also: the perimeter of a polygon.” EX1027-Webster, 865. The Oxford College Dictionary defines “periphery” as “the outer limits or edge of an area or object.” EX1029-Oxford, 1020.

245. Accordingly, in my opinion the Skilled Artisan would understand that Chang’s “periphery region” refers to the solar cell/substrate’s perimeter or edge portion, as seen for example in peripheral white space of Figure 3 of the 009 Patent. Thus, the Skilled Artisan would understand that the electrically isolated

Ex1003-Banerjee, ¶244-245; Pet. at 64

Patent Owner's Expert Reads Chang *Not* Based On Chang's Express Definition of "Entirely Formed"

shows it. And "fully formed" -- there is a clear and present meaning to "fully formed," fully formed over the whole surface.

Q Do you mean "entirely formed"?

A Yes. I apologize.

Q So you're interpreting the term "entirely formed" in Chang according to its ordinary definition?

A Yeah. Yes.

*EX1045-Peckarar Depo., 161:8-162:3;
Reply at 3, n. 3*

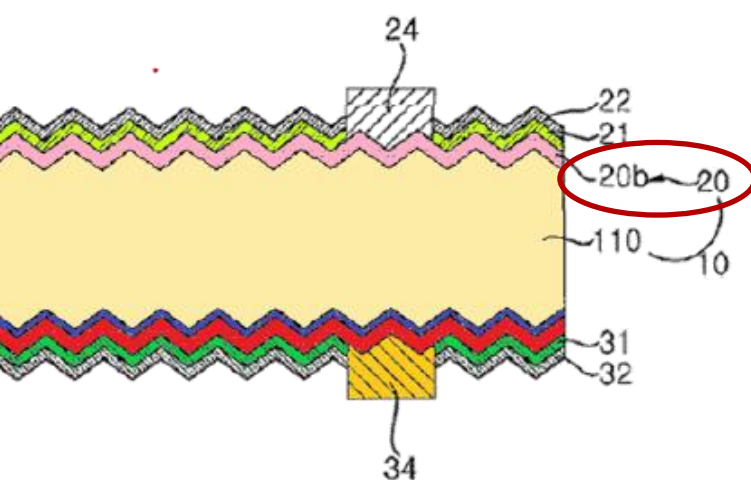
PO's Argument Based On Chang's Paragraph 76

[0076] In this instance, the emitter area 20 and the back surface field area 30 may be disposed at different sides of the semiconductor substrate 10 to form a double-surface light-receiving type structure. As a result, light is incident upon the back surface of the semiconductor substrate 10 as well as the front surface of the semiconductor substrate 10, thereby increasing an amount of incident light and improving efficiency of the solar cell 100. Because the emitter area 20 and the back surface field area 30 are not adjacent to each other, the necessity of performing an isolation process when the emitter area 20 and the back surface field area 30 are formed to be adjacent to each other is eliminated. In addition, because the emitter area 20 and the back surface field area 30 are entirely formed, thus requiring no additional patterning and alignment processes. As a result, manufacturing process is simplified and cost is thus reduced.

POR at 41-42

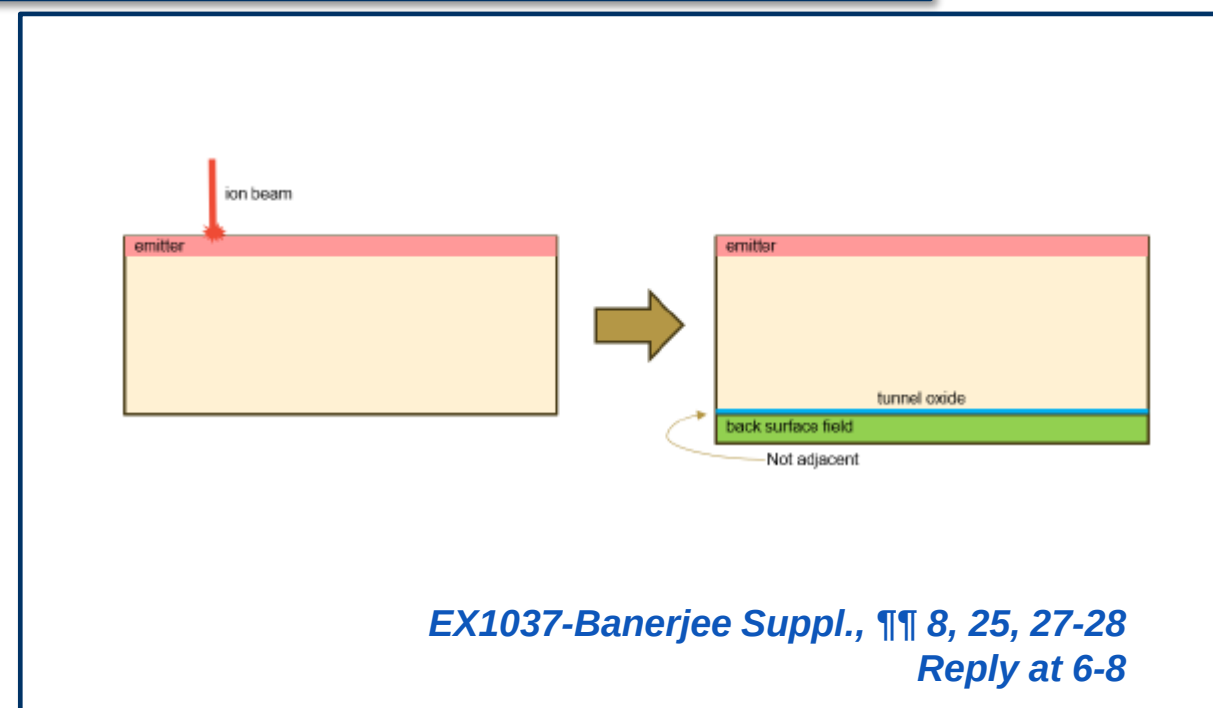
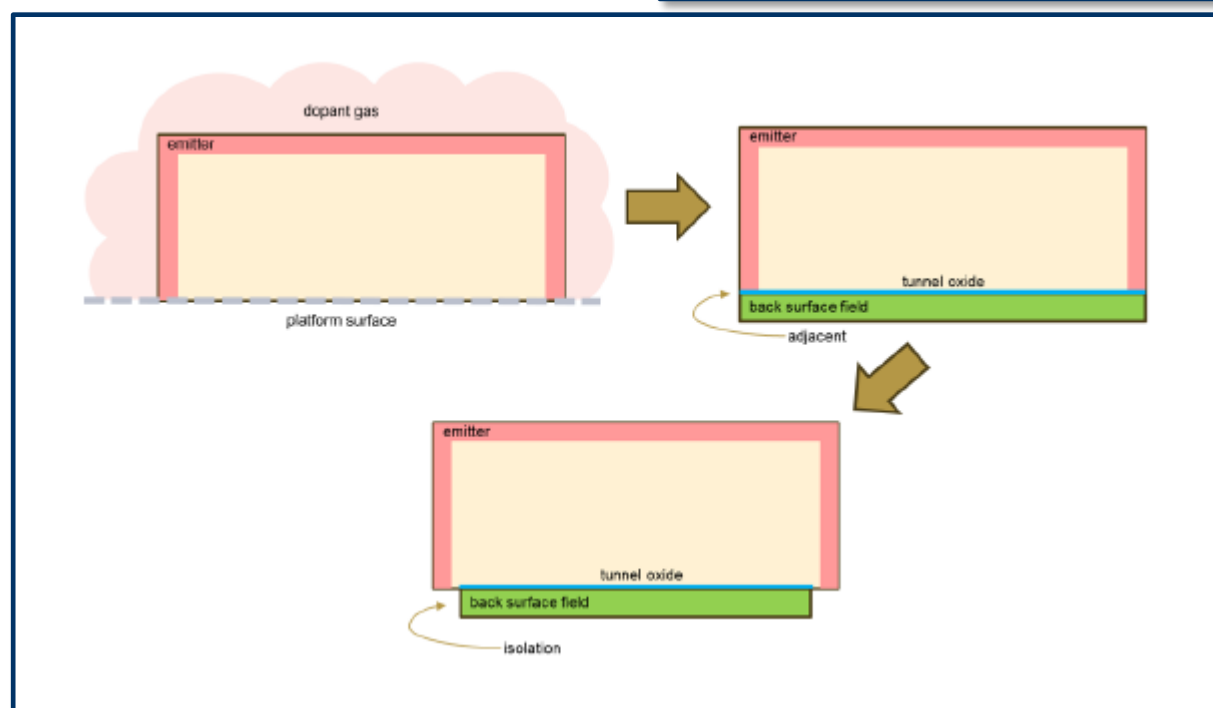
Chang's Thermal Diffusion and Ion Implantation Embodiments

FIG. 8



[0098] Referring to FIG. 8, in the solar cell according to the embodiment of the invention, the emitter area 20 includes a second portion 20b including a doping area formed in the semiconductor substrate 10. That is, the semiconductor substrate 10 may include the base area 110 as an undoped region and the second portion 20b of the emitter area 20 formed by doping the semiconductor substrate 10 with a dopant having a conductive type different from the semiconductor substrate 10. As a result, the second portion 20b may have the same crystalline structure as the base area 110. The emitter area 20 may be formed by a variety of doping methods (for example, thermal diffusion, ion implantation or the like).

*Ex.1013-Chang ¶98;
Reply at 6-8
Pet. at 70*



PO's Expert: Chang's Ion Implantation Does Not Dope the Substrate's Side Surfaces

Q In your opinion, Chang discloses a technique for preventing the emitter from diffusing to the sidewall?

A Right.

Q What technique is that?

A Well, ion implantation would be one. We said, as I recall, that is what he used but --

Q Chang uses ion implantation and that results in the sidewall not being contaminated with dopants?

MR. De BLANK: Objection. Vague. Compound. Document speaks for itself.

A I'm saying in answer to your question, yes, that's what he's disclosing.

*EX1045-Peckarar., 148:21-149:12;
see also, id., 146:20-149:12;
Reply at 8*

PO's Expert: Thermal Diffusion Will Dope the Substrate's Side Surfaces

Q So if Chang, instead of ion implantation used a gas diffusion process to diffuse its emitter layer, then it would need an isolation portion?

MR. De BLANK: Objection. Incomplete hypothetical.

A I'd have to -- it is true I'd have to look at the circumstance, how the processes were accomplished, but in general, if you use -- I will give you, if you use gaseous diffusion, you're going to contaminate the sidewall.

EX1045-Peckarar Depo., 150:10-20; Reply at 6

Institution Decision Recognized that Chang ¶76 Was For Some Non-Adjacent Embodiments, Not All Embodiments

We acknowledge Patent Owner’s argument that the combination fails because there is no need to isolate the emitter from the back surface field. Prelim. Resp. 26. In particular, Patent Owner directs our attention to a portion of Chang that states that “the emitter area 20 and the back surface field area may be disposed at different sides of the semiconductor substrate 10 to form a double-surface light-receiving type system,” and in that case, “[b]ecause the emitter area 20 and the back surface field area 30 are not adjacent to each other, the necessity of performing an isolation process when the emitter area 20 and the back surface field area 30 are formed to be adjacent to each other is eliminated.” *Id.* (citing Ex. 1013 ¶ 76). But, that paragraph in Chang begins with “[i]n *this* instance” and states that the components “*may* be disposed at different sides” of the substrate indicating multiple and differing embodiments are contemplated by Chang. Ex. 1013 ¶ 76 (emphasis added); *see also id.* ¶¶ 12–29 (describing the figures as including “an embodiment,” a “modified embodiment,” “another embodiment,” and “another modified embodiment.”)

Paper 11, Institution Decision at 27

Institution Decision: Chang's Diffusion, Like Jin's, of Front and Lateral Sides Necessitated Isolation Region

Furthermore, Patent Owner dismisses Chang's express statement that "entirely formed" excludes certain regions such as the periphery and isolation regions. "It is well settled that a prior art reference is relevant for all that it teaches to those of ordinary skill in the art." *In re Fritch*, 972 F.2d 1260, 1265 (Fed. Cir. 1992). And Petitioner, relying on the testimony of Dr. Banerjee, explains why the skilled artisan would have considered an isolation region advantageous. Pet. 65–66 (citing Ex. 1003 ¶¶ 247–248). In particular, Petitioner and its declarant explain that because the emitter layers of Jin and Chang are formed in the same manner (i.e., "heat diffusion" or "thermal diffusion") "dopants diffuse into the front and lateral side surfaces of the substrate" and Chang's isolation region, like Jin's "gap T" acts to isolate the emitter and back surface field to prevent electrical shorting. *Id.* (emphasis added) (citing Ex. 1003 ¶¶ 248).

Paper 11, Institution Decision at 28

Improper to Limit Chang's Teachings to Its Figures

Chang's figures. *Id.* But there is no requirement that a prior art feature be depicted in a figure—disclosure in the patent's specification is sufficient. *See, e.g., Krippelz v. Ford Motor Co.*, 667 F.3d 1261, 1268-69 (Fed. Cir. 2012) (error for court to rely on the absence of a “conical beam of light” in a prior art drawing when it was described by the written description). And, as Jin Fig. 2 demonstrates, illustrations of solar cells like Chang's often depict only an interior portion showing the cross-sectional layers, not necessarily including the edge portion. EX1037-SupplDecl., ¶¶29-33; EX1009-Jin, ¶25, Figs. 1-3.

Reply at 2

Dr. Banerjee Explains that Condensed Figures May Not Show the Sidewalls of the Solar Cell

facilitate comprehension and supplement what the specification describes. Chang explains in ¶¶30-31 that its “embodiments may be modified into various forms,” and that parts of the solar cell “are not illustrated for clear and brief description”.

30. Jin is a perfect example. Figures 2 and 3 of Jin both show parallel

FIG. 1

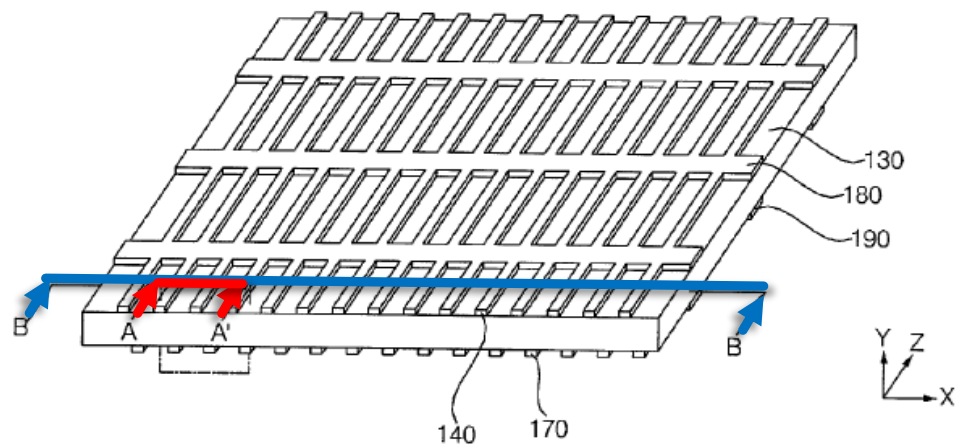
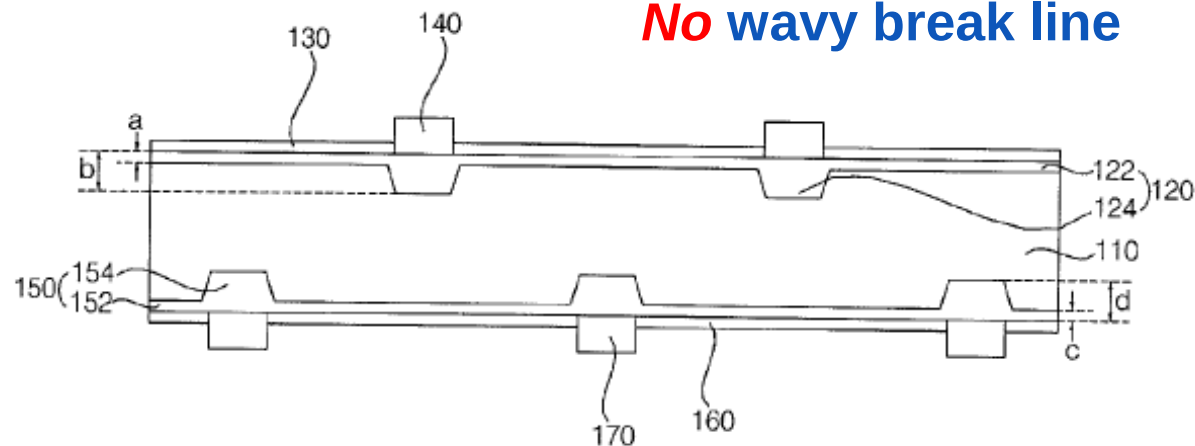


FIG. 2

No wavy break line

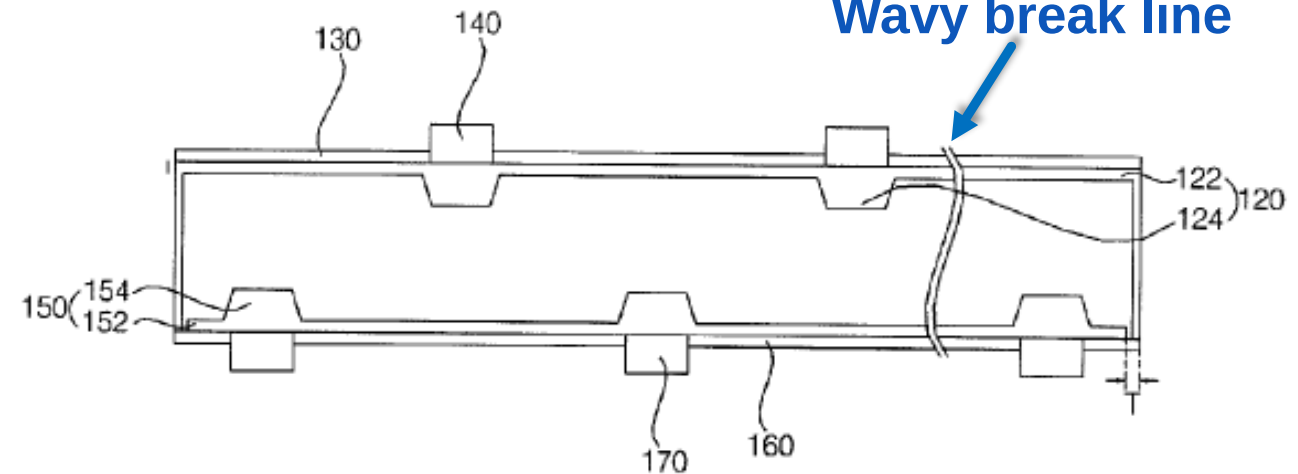


Along line A-A'

[0011] FIG. 1 is a perspective view of a solar cell according to one embodiment of the invention;
[0012] FIG. 2 is a cross-sectional view of the solar cell of FIG. 1 along line A-A';
[0013] FIG. 3 is a cross-sectional view of the solar cell of FIG. 1 along line B-B';

FIG. 3

Wavy break line



Along line B-B'

Ex. 1009-Jin, ¶¶11-13, FIGS.1-3; EX1037-SupDecl., ¶¶29-33; Reply at 2 and 26

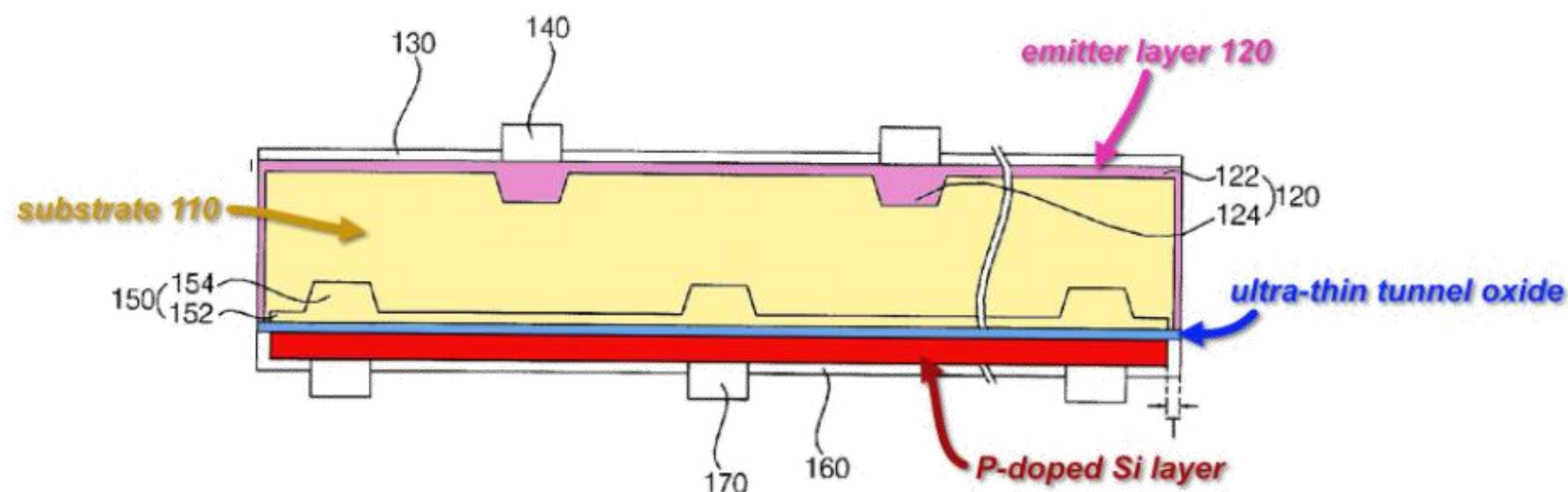
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Petitioner Runergy – Ex. 1048
IPR2025-00006 and 00007

Disputed Issues

- Jin/Feldmann combination: (Ground 1)
 - Motivation for isolation portion, tunnel oxide edge exclusion, and bifaciality
 - Whether a tunnel oxide layer is sufficient to prevent shorting
 - Including tunnel oxide at the edge vs. excluding tunnel oxide at the edge
 - Bifacial vs. monofacial (opening-in-passivation-layer issue)
 - Reasonable expectation of success of using shadow mask
- Chang/Jin combination: (Ground 3 (009) and Ground 2 (104))
 - Chang's disclosure of a backside isolation portion at the edge

Patent Owner's Argument

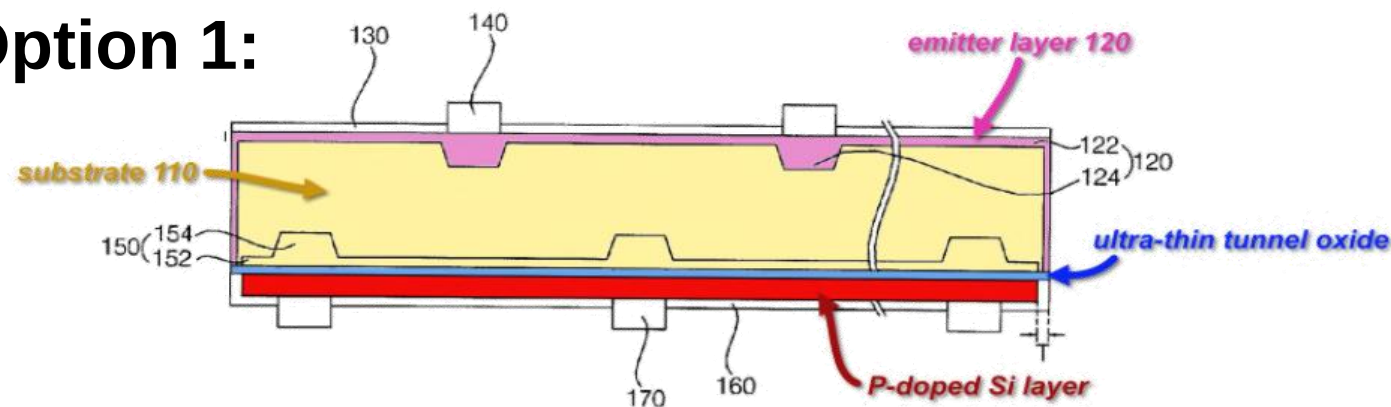


(*Id.*, ¶¶ 143-144.) This structure—which again is the most natural result of Jin and Feldmann’s teachings—does not satisfy the claims. The “oxide layer” is not “exclude[d]” from the “isolation portion” at the “edge” of the substrate.

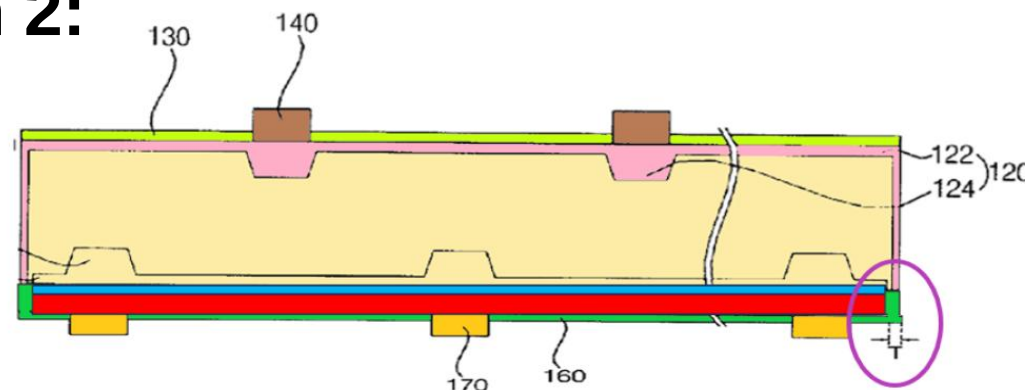
PO Response at 24

Obviousness Does Not Require the Best Option, Only a Suitable Option

Option 1:



Option 2:



Reply at 19-20

“It’s not necessary to show a combination is ‘the *best* option, only that it be a *suitable* option.’”

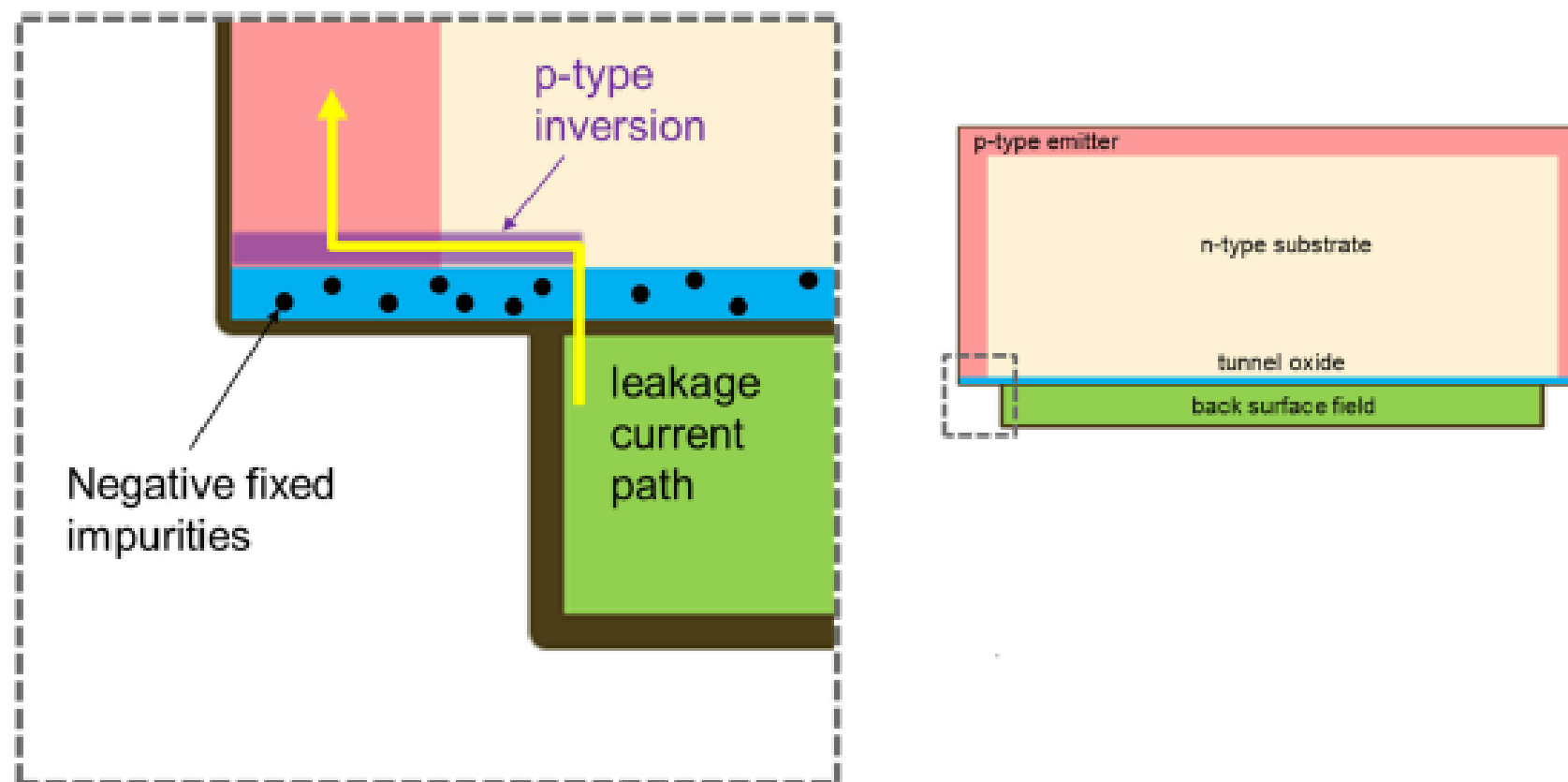
Intel Corp. v. Qualcomm, 21 F.4th 784, 800 (Fed. Cir. 2021)

“If there’s a known technique to address a known problem using ‘prior art elements according to their established functions,’ then there is a motivation to combine.”

Intel Corp. v. PACT, 61 F.4th 1373, 1380 (Fed. Cir. 2023)

Dr. Banerjee Explains A Reason for Not Extending the Tunnel Oxide Layer to the Edge

53. As I explained in my opening declaration, negative fixed charges in the silicon oxide layer could then create a p-type inversion in the n-type substrate. This would provide a leakage path to the p-type emitter on the front of the solar cell, as depicted below. EX1003, ¶116. It is this p-type inversion in the n-type substrate that provides the leakage path to the p-type emitter—not the tunnel oxide itself.



EX1037-Banerjee Suppl., ¶53; Reply at 21-22
See also, EX1003-Banerjee, 116; Pet. at 26

Disputed Issues

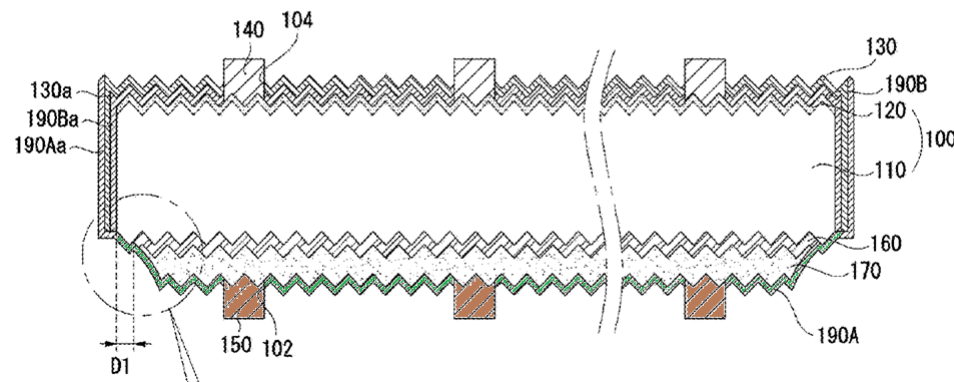
- Jin/Feldmann combination: (Ground 1)
 - Motivation for isolation portion, tunnel oxide edge exclusion, and bifaciality
 - Whether a tunnel oxide layer is sufficient to prevent shorting
 - Including tunnel oxide at the edge vs. excluding tunnel oxide at the edge
 - Bifacial vs. monofacial (opening-in-passivation-layer issue)
 - Reasonable expectation of success of using shadow mask
- Chang/Jin combination: (Ground 3 (009) and Ground 2 (104))
 - Chang's disclosure of a backside isolation portion at the edge

Monofacial and Bifacial Cells

009/104

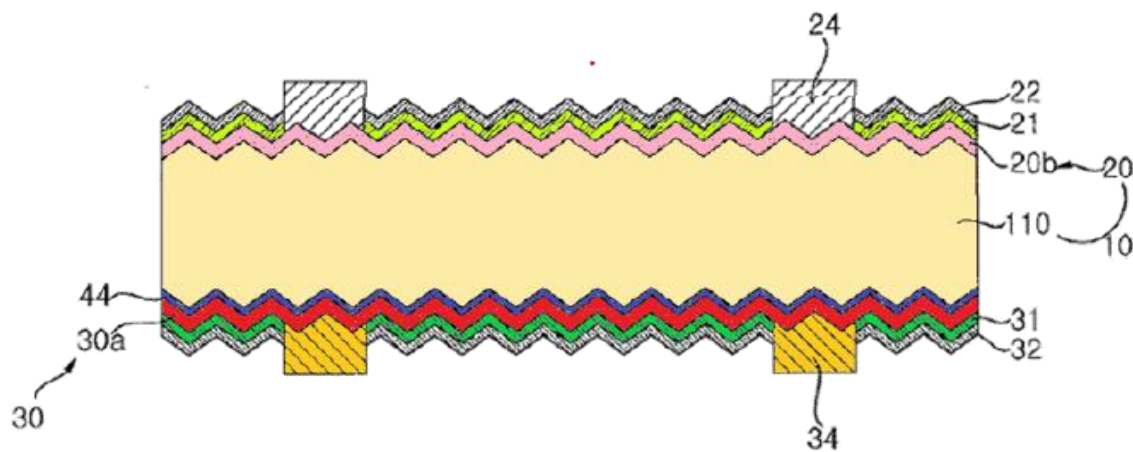
a first electrode connected to the polysilicon layer through an opening formed in the first passivation film;

FIG. 2

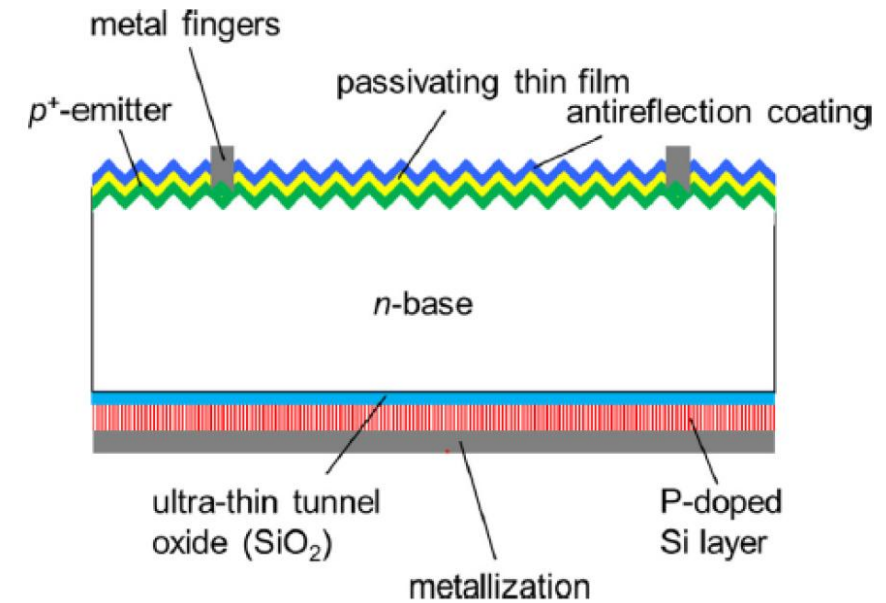


Chang

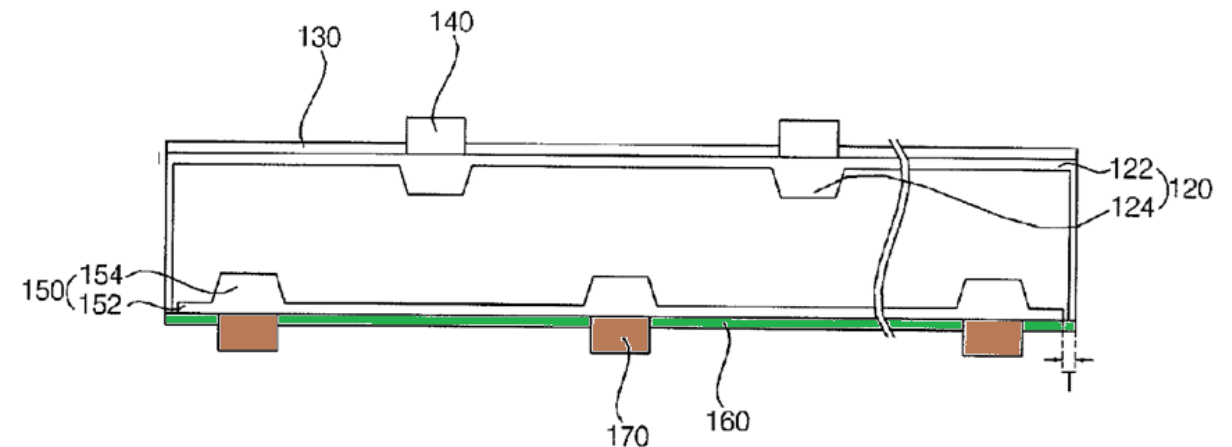
FIG. 8



Feldmann



Jin



EX1003-Banerjee Decl., ¶115; Pet. at 17, 26, 92; Reply at 27

PO's Reliance on Feldmann's "Criticism" of Point Contact or PERL Cells is Irrelevant

PERL Point-Contact Cells

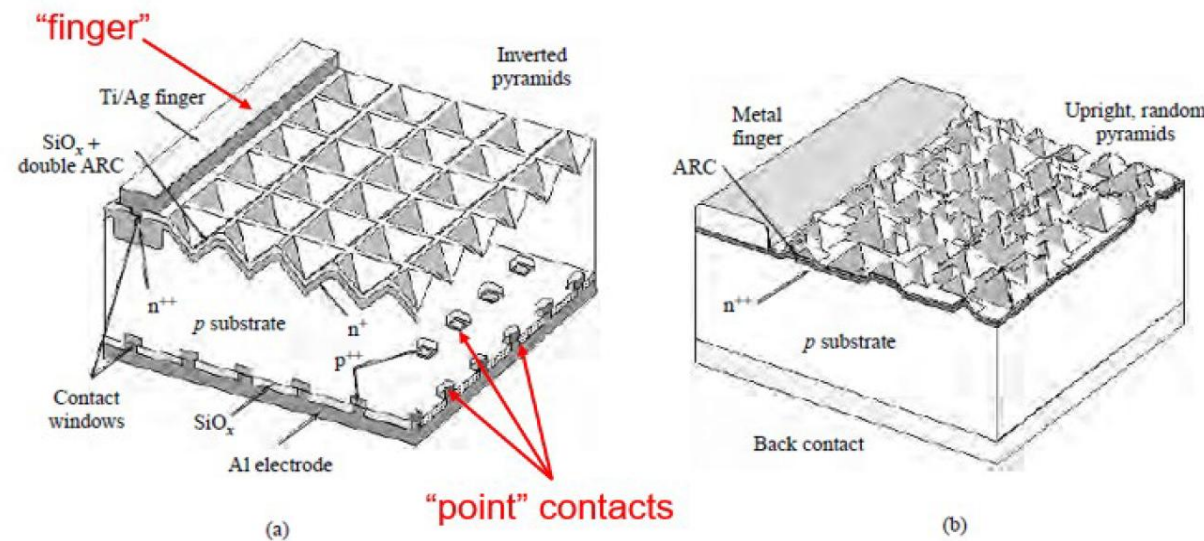
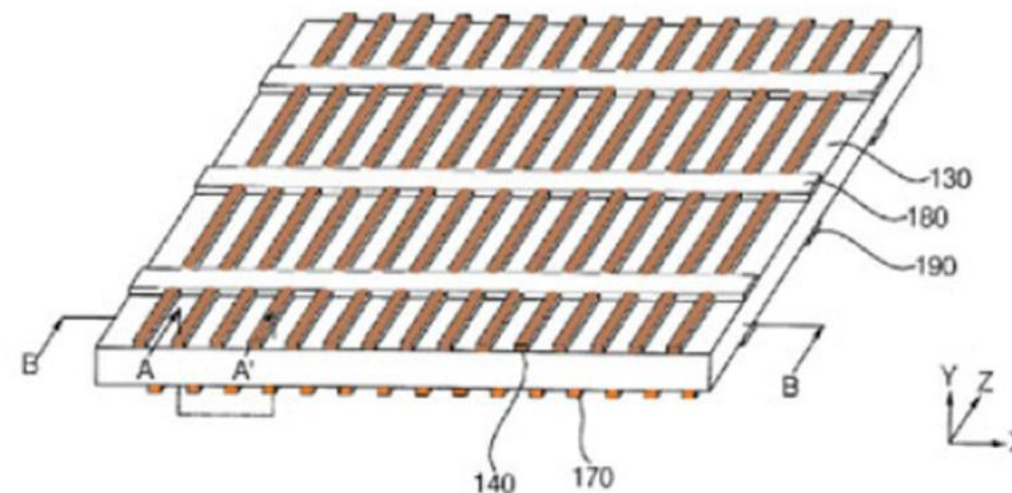


Figure 7.2 (a) Passivated emitter and rear locally diffused (PERL) cell; and (b) industrial cell with screen-printed contacts. (Not to scale)

Jin is not a point contact or PERL cell

Jin



EX1037-Banerjee-Suppl., ¶¶65-70; Reply at 27-29

Dr. Banerjee Explains That Bifacial Cells Absorb Light From Both Sides And Boost Power

declaration: “Bifacial solar cells like that of Jin and Chang can receive light on both the front and back sides of the solar cell.” EX1003, ¶¶104, 115. Because bifacial solar cells can receive light through both surfaces, they are able to generate more power than a monofacial solar cell, that receives light through only one surface. See, e.g., EX1022-Luque, 282 (“Bifacial cells are designed to collect light incident at both faces, which allows a boost in output power...”). Thus, the Skilled Artisan would know that the bifacial cells would boost power by absorbing external light from the rear that can more than make up for the incremental photon absorption by internal rear-reflection (which is limited to infrared light). This would not dissuade the Skilled Artisan from applying Feldmann’s TOPCon structure to a bifacial cell.

EX1037-Supp Banerjee, ¶71; Reply at 29

POSA Would Have Applied TOPCon To Bifacial Cells

115. Jin's solar cell is bifacial and can absorb sunlight from both the front and back surfaces. EX1009-Jin, ¶42. Feldmann's solar cell is monofacial and only absorbs sunlight from the front its front surface. EX1012-Feldmann, §2.2 ("the rear is fully metalized"). The Skilled Artisan, however, would not have been dissuaded from modifying Jin's back surface field layer 150 with Feldmann's TOPCon structure because, as discussed above, Feldmann, Lindholm, and Kwark all taught that adding the tunnel oxide layer between the substrate and BSF would increase efficiency by reducing recombination.

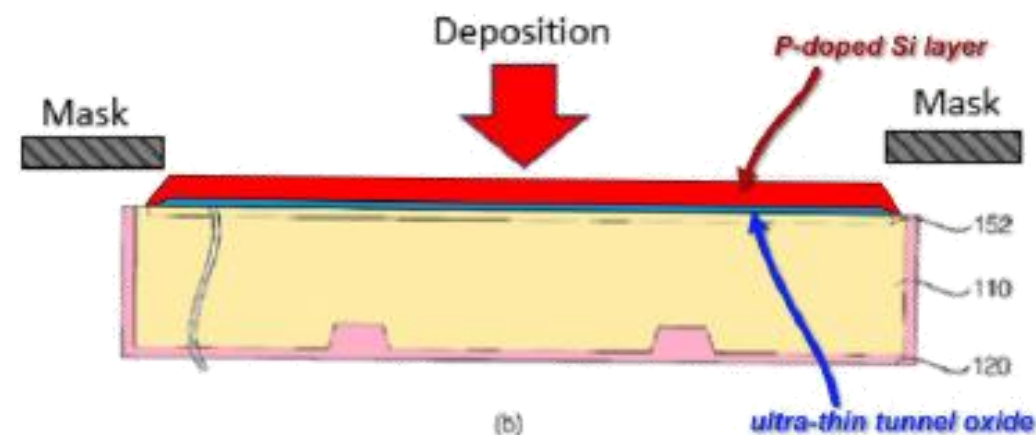
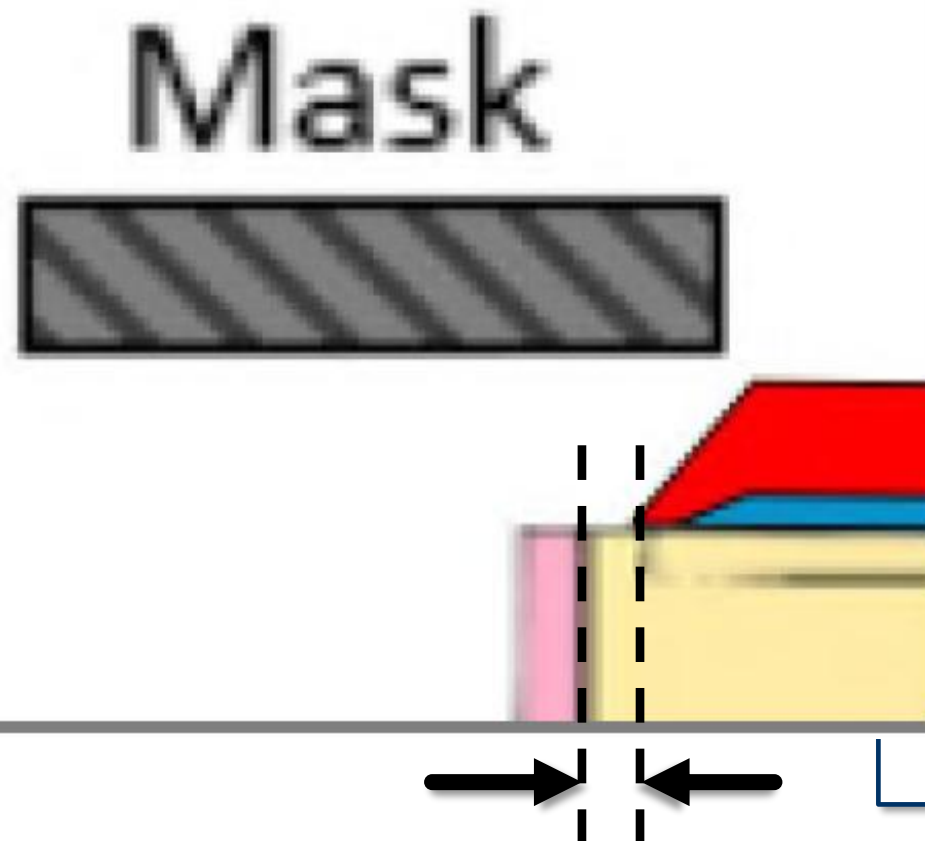
EX1003-Banerjee, ¶115; Pet. at 17, 26; Reply at 27

Disputed Issues

- Jin/Feldmann combination: (Ground 1)
 - Motivation for isolation portion, tunnel oxide edge exclusion, and bifaciality
 - Whether a tunnel oxide layer is sufficient to prevent shorting
 - Including tunnel oxide at the edge vs. excluding tunnel oxide at the edge
 - Bifacial vs. monofacial (opening-in-passivation-layer issue)
 - Reasonable expectation of success using shadow mask
- Chang/Jin combination: (Ground 3 (009) and Ground 2 (104))
 - Chang's disclosure of an backside isolation portion at the edge

Patent Owner Response Admits That Using Jin's Mask Results in the Claimed Isolation Portion

The polysilicon layer is much thicker (20 nm). (*See id.*) The ultra-thin tunnel oxide will fill only a portion of the mask's aperture. There will be little overspray due to the layer's thinness and shorter deposition time. The thicker polysilicon layer requires a longer deposition time and will fill the mask's aperture. This will result in more overspray. Thus, rather than producing the layered structure referenced in the Petition and by Dr. Banerjee, the following would be more likely result:



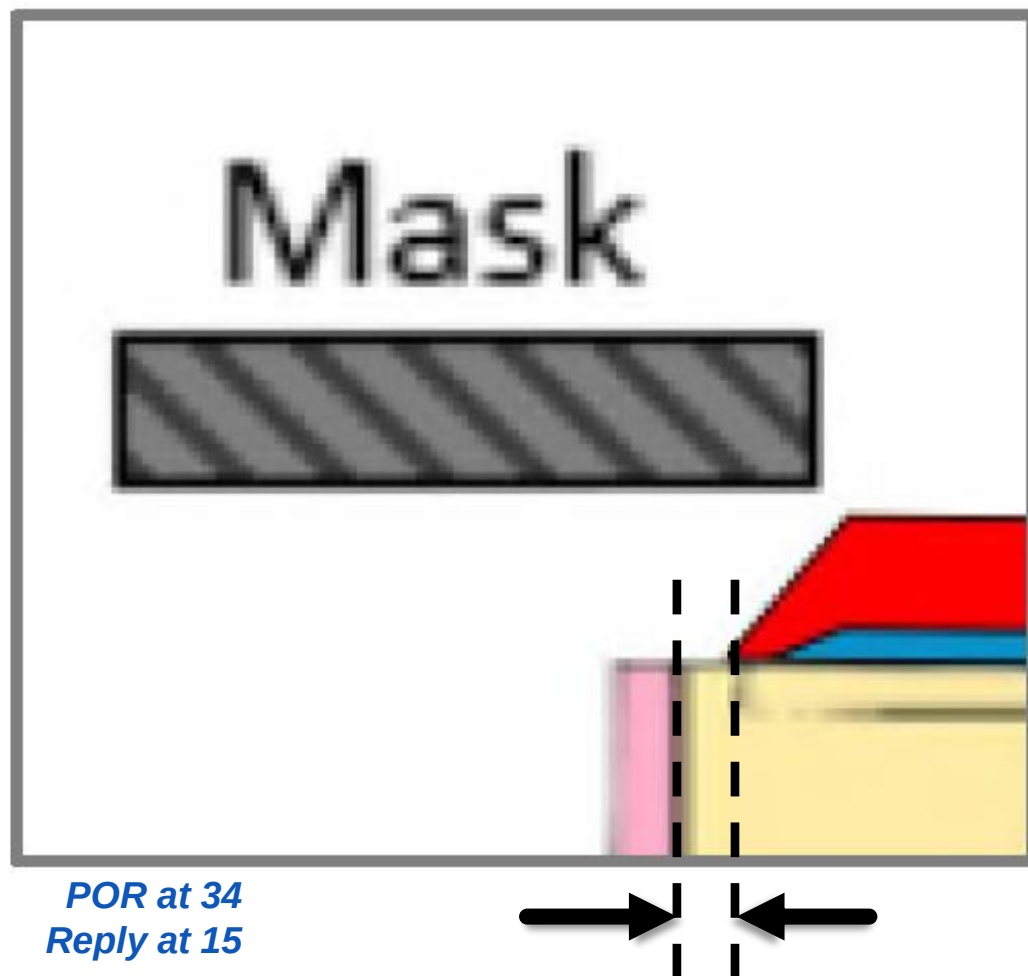
(Ex. 2001, ¶¶ 218-219.)

POR at 34

Gap T = isolation portion (excludes tunnel oxide and polysilicon)

Patent Owner's Response Also Admits Satisfaction of Claims 8 (009) and 6 (104)

No dispute that metal masks would lead to overspray and tapered ends



POR at 34
Reply at 15

8. The solar cell of claim 1, wherein a thickness of the edge portion in the polysilicon layer progressively decreases toward the isolation portion.

6. The solar cell of claim 1, wherein a thickness of an edge region in the first conductive type semiconductor region progressively decreases towards the isolation portion.

Gap T = isolation portion (excludes tunnel oxide and polysilicon)

Patent Owner Mischaracterizes Jin's Teaching of the Mask

“deposited” on top of the already grown oxide. (*Id.*) No mask is employed. While Jin does employ a metal mask, its mask is meant to facilitate “ion implantation” of an “impurity doped region” in a silicon substrate, not a CVD deposition process. (*E.g.*, Jin, [0009], [0079], [0083]-[0084]; see also Ex. 2001, ¶¶ 174-178.)

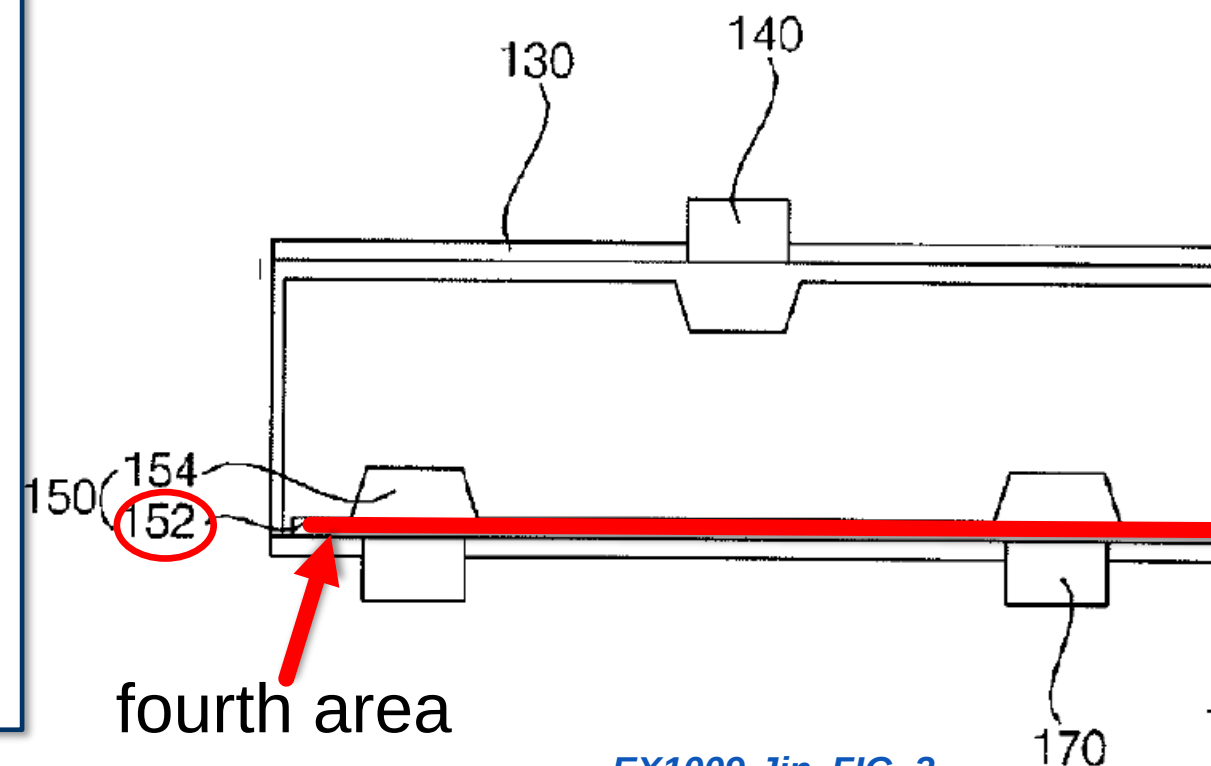
POR at 29

[0083] Next, as shown in FIG. 9, by using a second mask 410 having a part 412 to cover or overlap the edge part of the rear surface of the substrate 110, the fourth area 152 of the back surface field layer 150 is formed.

[0084] The fourth area 152 prevents or reduces recombination of electron-hole pairs separated from the rear surface of the substrate 110. The fourth area 152 may be formed by doping the substrate 110 with a second impurity of the same conductive type as the substrate 110 according to a heat diffusion method, a laser doping method, or an ion implantation method, as well as other methods. The fourth area 152 may have a doping density ranging from 5E18 to 1E20 and a doping depth of 0.3 μm to 1 μm .

EX1009-Jin, ¶¶ 83-84

FIG. 3



EX1009-Jin, FIG. 3

Dr. Banerjee Explains That POSA Would Know That Shadow Masks Have Been Used To Form Solar Cell Layers

119. As a first example, Jin discloses a mask in Figure 9 that would be used to cover the periphery or edge portion of the back surface of the substrate. Such masking technique, known as shadow masking was well known to the Skilled Artisan. The Skilled Artisan would know, for example, that reusable metal “shadow masks” have been used in the masking and forming of layers in solar cells. For example, Scherff discloses a reusable metal mask used for structuring the emitter and back surface field regions of an interdigitated back contact solar cell. EX1031-Scherff, Abstract. Scherff discloses that various layers can be deposited and plasma etched through openings in the mask. *Id.*, §2.

polysilicon layer. The Skilled Artisan would be aware that deposition techniques such as plasma enhanced chemical vapor deposition (PECVD) or atomic layer deposition (ALD) could be used to deposit the tunnel oxide and the polysilicon layer in the area not covered by the metal mask. EX1031-Scherff §2.1. For

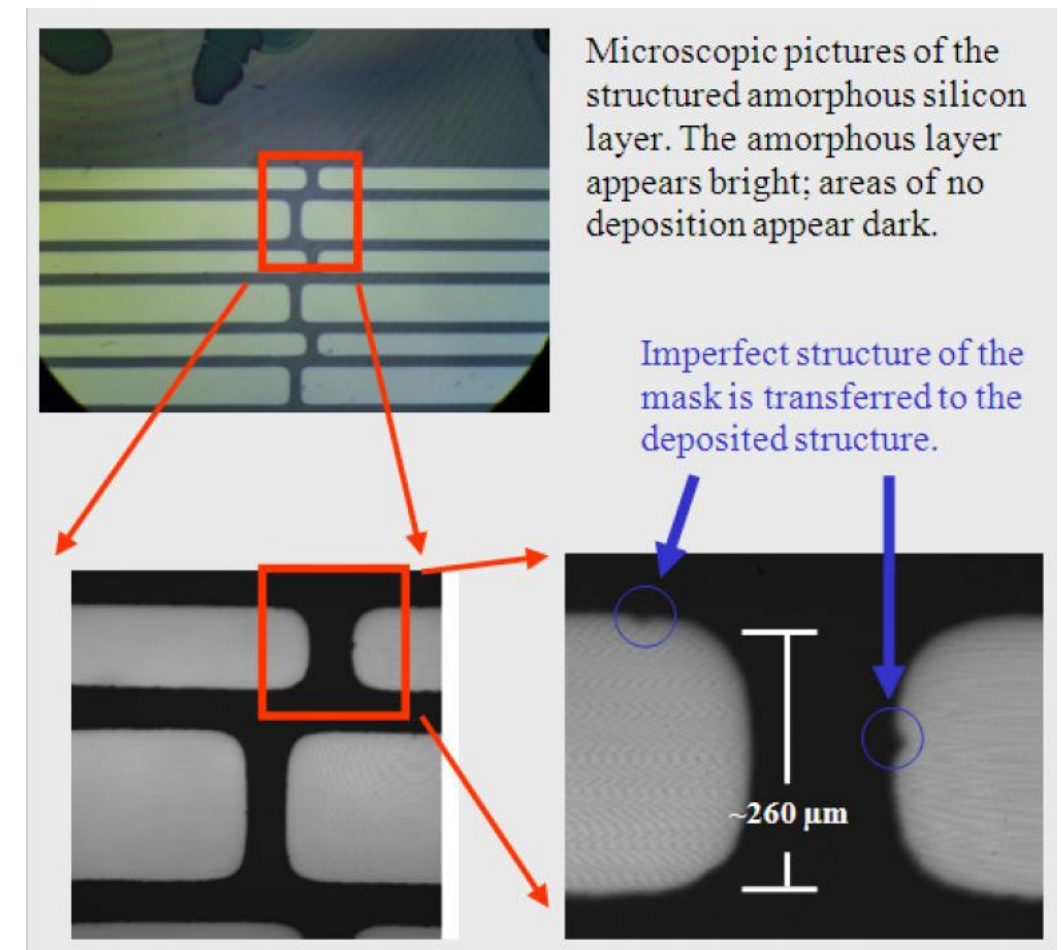
*EX1003-Banerjee, ¶¶119-120
Pet. at 27, 43; Reply at 24*

Prior Art Shows Use of CVD with Shadow Mask To Form Patterned Solar Cell Emitter/BSF Layers

ABSTRACT: We present a **novel method for structuring Emitter and BSF areas of interdigitated back contacted silicon heterojunction solar cells (IBC-HJ)**. The **method combines the benefits of in-line capability with vacuum processes only, reusable masks, self alignment** and furthermore an easy and **extreme safe wafer handling**. It is based on plasma etching of passivation layers and a following layer deposition procedure via openings in a **mechanical masking**. The exceptional way how the reusable masks are attached to the sample provides accurate masking over large area. By overlaying two masks the wafer can remain underneath the lower masking, which also

novel method (in figure 2). The *a*-Si:H was deposited in a standard parallel plate PECVD setup at an excitation frequency of 13.56MHz. Due to the absorption of the *a*-Si:H in the wavelength range up to 600nm the layer appears brown. Even very thin layers are easily visible.

*EX1031-Scherff, 2125-2126
Pet. at 27, 43; Reply at 24*



Those Skilled In the Art Have Successfully Demonstrated Shadow Mask for Use in TOPCon Solar Cells

For solar cells, a high-quality edge isolation, i.e. the separation of p and n regions, needs to be ensured. A parasitically deposited n doped poly-Si on the front side and on the wafer edges leads to a low shunt resistance due to direct the contact to the p⁺ emitter (Fig. 2). The removal of the poly-Si from the front side and of the edges is thus of utmost importance [1,5]. There are ideas to avoid the wrap-around completely by using physical vapor deposition (PVD) [6] or PECVD masks [7] and this would naturally reduce the required amount of TOPCon process steps [8]. The parasitical poly-Si can successfully be

7. M. Stöhr, B. Beier, J. Aprojanz, A. Vogt, N. Ambrosius, R. Brendel, T. Dullweber, PECVD shadow mask deposition of amorphous silicon – a shortcut to local passivation contacts, in *Proceedings of 37th European Photovoltaic Solar Energy Conference and Exhibition (EUPVSEC)*, online, 2020, pp. 521–524

EX2007-Krieg, 1

PECVD SHADOW MASK DEPOSITION OF AMORPHOUS SILICON – A SHORTCUT TO LOCAL PASSIVATING CONTACTS

M. Stöhr¹, B. Beier¹, J. Aprojanz¹, A. Vogt², N. Ambrosius², R. Brendel^{1,3}, T. Dullweber¹

¹Institute for Solar Energy Research Hamelin (ISFH), Am Ohrberg 1, 31860 Emmerthal, Germany

²LPKF Laser & Electronics AG, Osteriede 7, 30827 Garbsen, Germany

³Department of Solar Energy, Institute of Solid-State Physics, Leibniz Universität Hannover, Appelstraße 2, 30167 Hannover, Germany

Corresponding author: M. Stöhr, E-mail: stoehr@isfh.de, Tel.: +49 5151 999-314

ABSTRACT: We develop and investigate shadow masks for the local PECVD deposition of amorphous Si (a-Si) fingers to be applied as local poly-crystalline Si (poly-Si) passivating contacts in the industrial fabrication of novel solar cell concepts such as TOPCon, PERC+POLO and POLO-IBC. We first apply a nickel-based test mask with

5 CONCLUSION

We successfully demonstrate the deposition of well-defined a-Si fingers with finger widths down to 70 µm using a lab-type nickel shadow mask. The finger opening widths were found to limit the deposition rate through the shadow mask openings. Furthermore, a glass-based shadow mask enables the local deposition across a full M2-sized Si wafer with excellent position and finger width accuracy with respect to the glass mask layout. The offset

EX1040-Stohr, 524
EX1037-Banerjee Supp Decl, ¶45
Reply at 25, n. 5

Undisputed: POSA Would Know That Both Tunnel Oxide and Polysilicon Layers Could be Formed by CVD

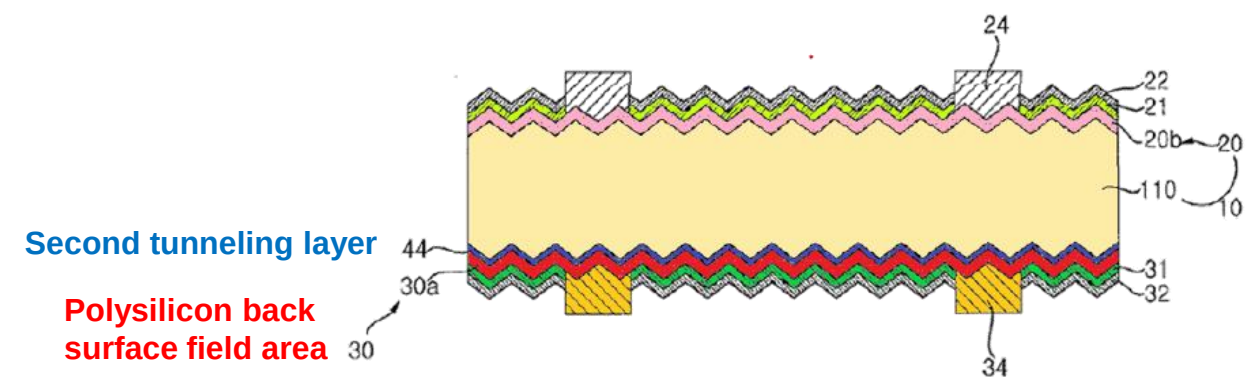
Patent Owner Response at 29

TOPCon solar cells. “TOPCon solar cells mainly employ[ed] ... PECVD oxidation, chemical oxidation, and ozone oxidation processes” to “deposit the thin layer of SiO_x ” that forms the tunneling layer. (Ex. 2004 at 4.) The “polysilicon layer” was deposited over the entire substrate via “low-pressure chemical vapor deposition (LPCVD) ... plasma-enhanced CVD (PECVD) ... inline atmospheric pressure CVD (APCVD) ... and sputtering....” (*Id.*; see also Ex. 2004 at 76 (similarly explaining

Chang

[0146] In this instance, the first and second tunneling layers 42 and 44 may be formed, for example, by a method such as thermal growth or deposition (for example, plasma-enhanced chemical vapor deposition chemical (PECVD), atomic layer deposition (ALD)) or the like, but the embodiment of the invention is not limited thereto and the first and second tunneling layers 42 and 44 may be formed by a variety of methods. In addition, first portions 20a and 30a of conductive type areas 20 and 30 may be formed of an amorphous, microcrystalline, or polycrystalline semiconductor. In this instance, the first portions 20a and 30a may be formed by a method, for example, thermal growth, deposition (for example, plasma-enhanced chemical vapor deposition chemical (PECVD)) or the like.

FIG. 8



Pet. at 27 - citing EX1003-Banerjee ¶120, citing Chang ¶ 146
Reply at 23 - citing EX1037-Banerjee Suppl. ¶44, citing Chang ¶ 146

Jin's Teachings Do Not Require the Differential Doped Regions in the BSF

[0119] In the above embodiment of FIGS. 1 to 3, the emitter layer includes the first area 124 and the second area 122 having different doping concentrations, and the back surface field layer 150 includes the third area 154 and the fourth area 152 having different doping concentrations. However, the invention is not limited thereto.

[0120] Thus, with reference to FIG. 15, an emitter layer 120a may include only a second area 122 that is a shallow or lightly doping area. Also, with reference to FIG. 16, a back surface field layer 150a may include only a fourth area 152 that is a shallow doping area. In addition, with reference to FIG. 17, the emitter 120a may include only a second area 122 that is the shallow doping area, and the back surface field layer 150a may include only a fourth area 152 that is the shallow doping area, simultaneously. In embodiments of the

FIG. 3

EX1010-Jin, ¶¶119-120
Reply at 15

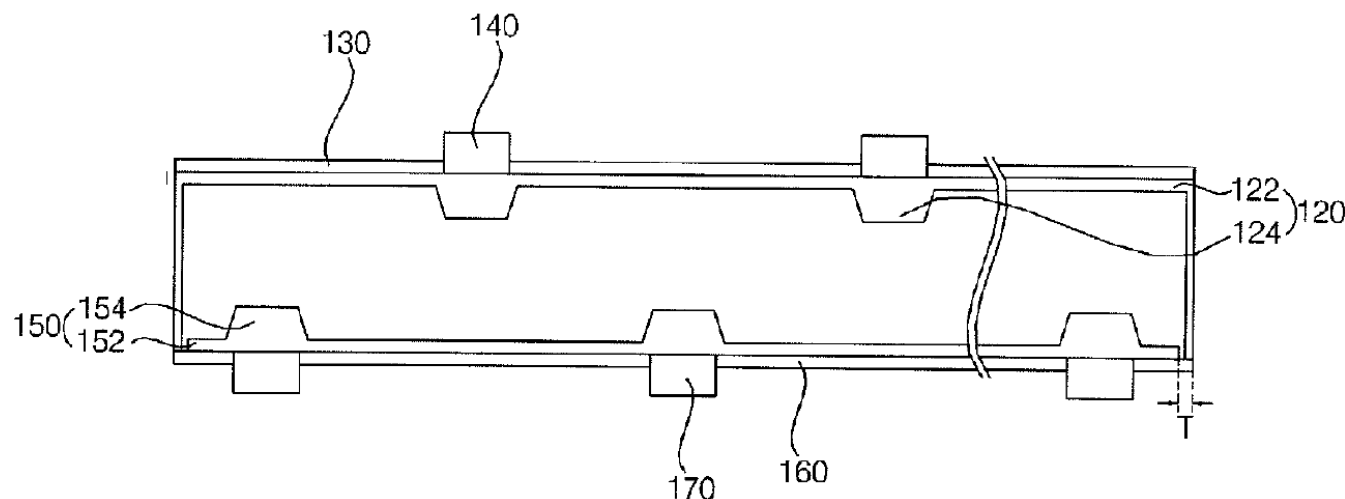


FIG. 16

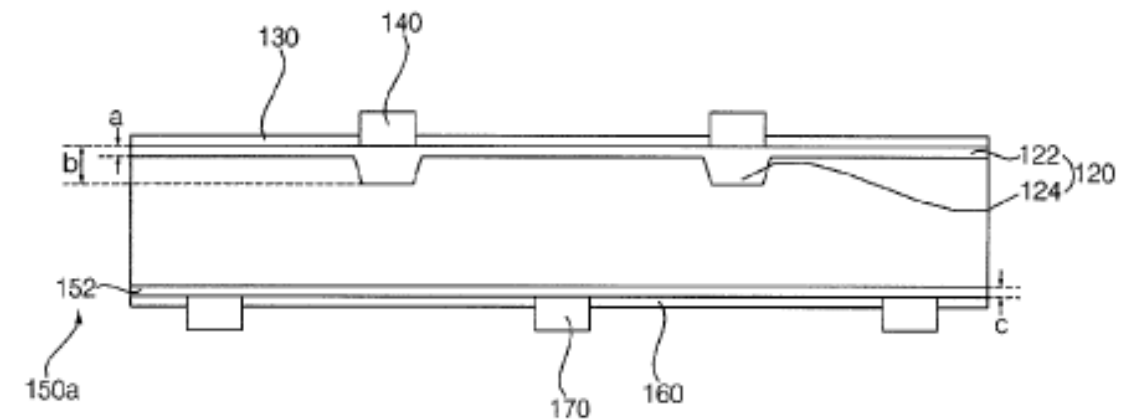
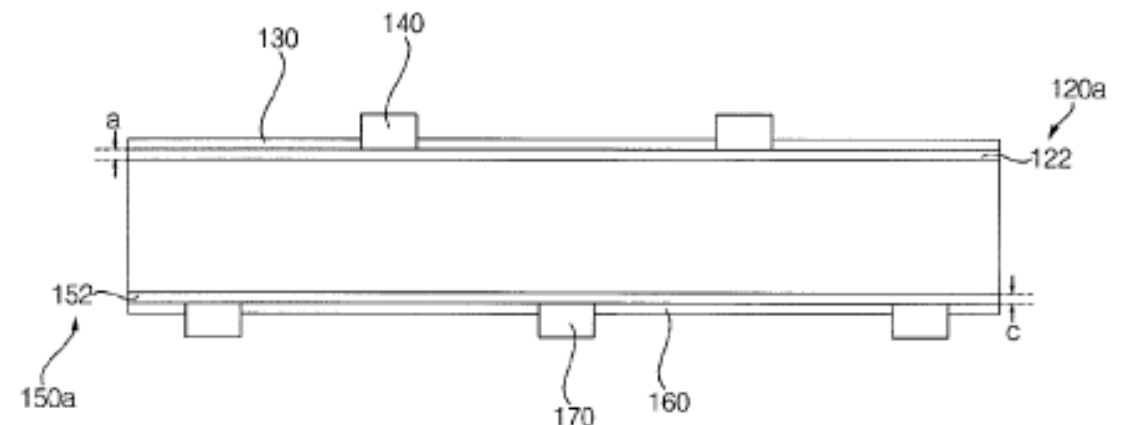


FIG. 17



Dr. Banerjee Explains Many Ways Known To POSA For Creating Gap-T/Isolation Portion

- Jin's shadow mask for both tunnel oxide and polysilicon layers
- Silicon nitride to mask edge/periphery for both tunnel oxide and polysilicon layers
- Combinations of silicon nitride mask and Jin's shadow mask
 - Selective etching of silicon nitride mask after tunnel oxide formation followed by Jin's shadow mask before polysilicon deposition
 - Selective etching of silicon nitride mask after tunnel oxide followed by polysilicon deposition and reverse mask etching of polysilicon
- Forming the tunnel oxide and polysilicon layers first and then reverse mask to protect center from etching of edge

*EX1003-Banerjee, ¶¶119-125
Pet. at 27; Reply at 23*

IPR2025-00006 and -00007

Runergy USA Inc. et al. v. Trina Solar Co. Ltd.

Petitioner Runergy's Demonstrative Exhibit

Hearing Date: January 29, 2026