

**UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD**

**RUNERGY USA INC., RUNERGY ALABAMA INC., MUNDRA SOLAR PV LTD.,
ADANI SOLAR USA INC., and CANADIAN SOLAR (USA) INC.,
Petitioners,**

v.

**TRINA SOLAR CO., LTD.,
Patent Owner.**

U.S. Patent No. 9,722,104

Case Nos. IPR2025-00007

**PATENT OWNER'S HEARING DEMONSTRATIVES
January 29, 2026**

The '104 Patent Relates Generally to TOPCon Solar Cells

A solar cell according to an example of the present invention includes a semiconductor substrate, a tunnel layer on the first surface of the semiconductor substrate, a first conductive type semiconductor region on the tunnel layer and configured to include impurities of a first conductive type, a second conductive type semiconductor region on a second surface which is the opposite surface of the semiconductor substrate and configured to include impurities of a second conductive type opposite the first conductive type,

*Ex. 1001, '104 Patent at 1:52-60
(see also Paper 16, Response at 5)*

TOPCon Solar Cells Provide Numerous Known Benefits

Such a tunnel layer 160 may generate a tunneling effect. More specifically, the tunnel layer 160 may function as a kind of barrier for electrons and holes.

That is, the tunnel layer 160 may not transmit minority carriers. After the minority carriers are accumulated in a portion neighboring the tunnel layer 160, only majority carriers having energy of a specific level or higher may pass through the tunnel layer 160. The majority carriers having energy of a specific level or higher may easily pass through the tunnel layer 160 by a tunneling effect.

Furthermore, the tunnel layer 160 may also function as a diffusion barrier for preventing the dopant of the first conductive type semiconductor region 170 from being diffused into the semiconductor substrate 100. The tunnel layer 160

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In particular, the tunnel layer 160 may be formed of a silicon oxide (SiO_x) layer including silicon oxide. The reason for this is that the silicon oxide layer has an excellent passivation characteristic and carriers can easily tunnel through the silicon oxide layer.

*Ex. 1001, '104 Patent at 7:60-8:15
(see also Paper 16, Response at 5-6)*

The '104 Patent Recognized a Problem With—and Improved Upon—Existing TOPCon Solar Cells

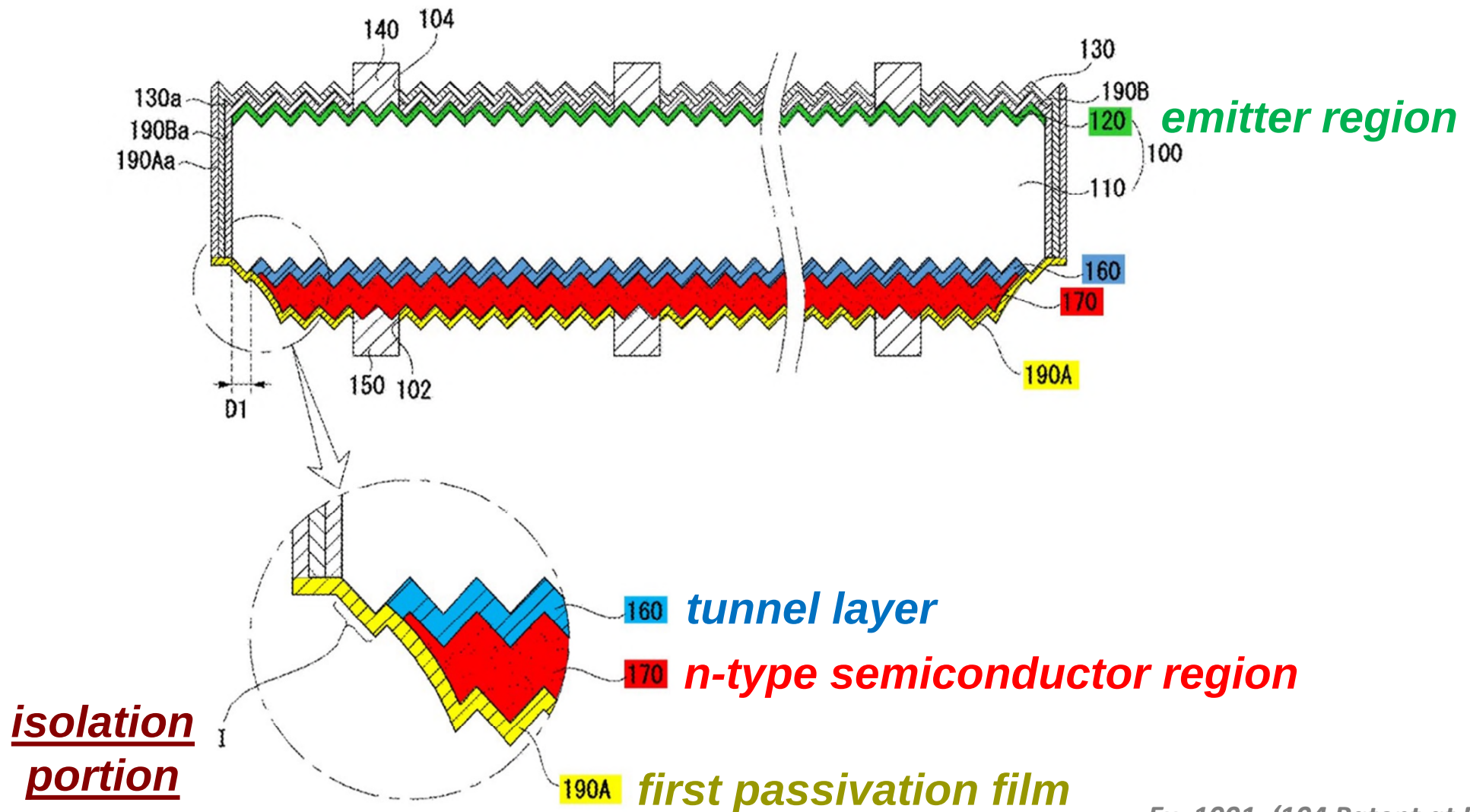
That is, when the second conductive type semiconductor region 120 is formed, the impurities of the second conductive type may be diffused into the side of or the edge of the back surface of the semiconductor substrate 100, and thus the first conductive type semiconductor region 170 and the second conductive type semiconductor region 120 may be unwantedly short-circuited in the side of or the edge of the back surface of the semiconductor substrate 100. In the present embodiment, such a problem can be fundamentally prevented by removing the first conductive type semiconductor region 170 from the edge of the back surface of the semiconductor substrate 100.

Such a tunnel layer 160 may be generally formed in portions other than an isolation portion I in the back surface of the semiconductor substrate 100. In this instance, “gen-

*Ex. 1001, '104 Patent at 13:24-35, 7:52-54
(see also Paper 16, Response at 8)*

The '104 Patent's Inventive TOPCon Solar Cell

FIG. 2



**Ex. 1001, '104 Patent at Fig. 2
(see also Paper 16, Response at 7-9)**

The '104 Patent Claims This Inventive Solar Cell

1. A solar cell, comprising:
a semiconductor substrate;
a tunnel layer on a first surface of the semiconductor substrate;
a first conductive type semiconductor region on the tunnel layer and containing impurities of a first conductive type;
a second conductive type semiconductor region on a second surface opposite to the first surface of the semiconductor substrate and containing impurities of a second conductive type opposite to the first conductive type;
a first passivation film on the first conductive type semiconductor region;
a first electrode formed on the first passivation film and connected to the first conductive type semiconductor region through an opening formed in the first passivation film;
a second passivation film on the second conductive type semiconductor region;
a second electrode formed on the second passivation film and connected to the second conductive type semiconductor region through an opening formed in the second passivation film; and
an isolation portion for preventing a contact between the first conductive type semiconductor region and the second conductive type semiconductor region,
wherein the isolation portion excludes the tunnel layer and the first conductive type semiconductor region, and is in an edge portion of the first surface of the semiconductor substrate, and
wherein the first passivation film covers the first surface of the semiconductor substrate and the isolation portion together.

Ex. 1001, '104 Patent at claim 1 (see also Paper 16, Response at 9)

The Petition Relies on Two Prior Art Combinations

Ground	Basis
<u>Ground 1</u>	Claims 1-6, 9-10 purportedly obvious over Jin and Feldmann
<u>Ground 2</u>	Claims 1-6, 9-10 purportedly obvious over Chang and Jin
Ground 3	Claims 7-8 purportedly obvious over Jin, Feldmann, and Seo
Ground 4	Claims 7-8 purportedly obvious over Chang, Jin, and Seo
Ground 5	Claim 11 purportedly obvious over Jin, Feldman, and Watabe
Ground 6	Claim 11 purportedly obvious over Chang, Jin, and Watabe

Paper 1, Petition at 3-4

Petitioner Did Not Carry Its Burden: The Prior Art Fails to Render the Claims Obvious

- ✗ The Petitioner *failed* to show why a POSITA would have combined Jin and Feldmann
- ✗ The Petitioner *failed* to show why a POSITA would have combined Chang and Jin
- ✗ The Petitioner *failed* to show why the art renders dependent claim 6 of the '104 patent obvious

Mere Separate Disclosure is Insufficient: an Evidence-Based Reason for Combining the Prior Art Is Required

“Obviousness concerns whether a skilled artisan not only could have made but would have been motivated to make the combinations or modifications of prior art to arrive at the claimed inventions.”

Belden Inc. v. Berk-Tek LLC, 805 F.3d 1064, 1073 (Fed. Cir. 2015) (emphasis added)

“It does not suffice to simply be known. A reason for combining must exist.”

Virtek Vision Int’l ULC v. Assembly Guidance Sys., Inc., 97 F.4th 882, 888 (Fed. Cir. 2024) (emphasis added)

(see also Paper 25, Sur-Reply at 11)

Petitioner's Improper Approach to Obviousness

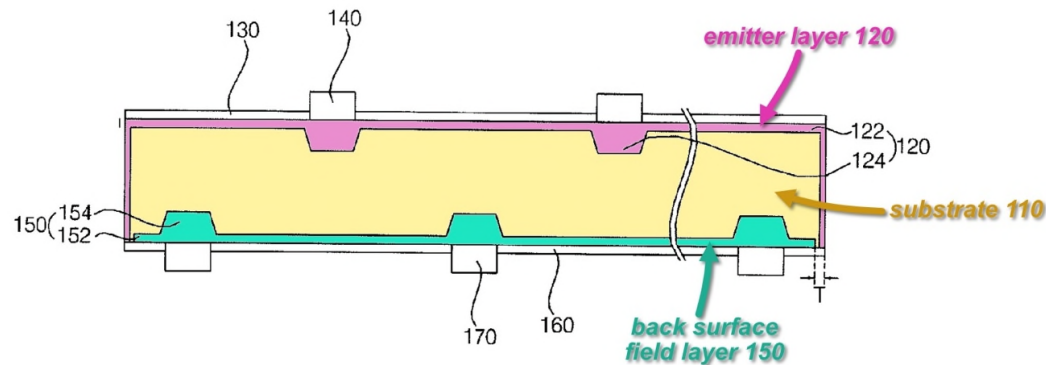
- Ignores that Jin and Feldmann teach **completely different** types of solar cells
- Requires POSITA to make a series of **atypical and inexplicable technical choices**
- **Eliminates** virtually all the improvements and benefits identified in both Jin and Feldmann
- **Improperly relies** on the '104 patent itself as purported evidence of obviousness

*Paper 16, Response at 16-18;
Paper 25, Sur-Reply at 2-13*

Jin and Feldmann Teach Fundamentally Different Types of Solar Cells

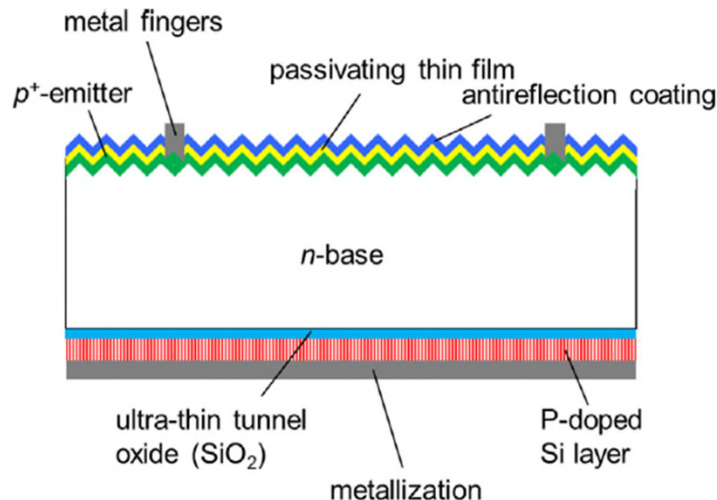
Jin:

FIG. 3



- Layers 120 / 150 doped **into** substrate
- **No** tunnel oxide
- **No** rear-side metallization
- **Includes** rear-side passivation layer

Feldmann:



- Rear-side layers applied **on top** of substrate
- **Includes** tunnel oxide
- **Includes** full rear-side metallization
- **No** rear-side passivation layer

*Ex. 1012, Feldmann at 272
(see also Paper 16, Response at 13, 19-22)*

Petitioner and its Expert Rely on the Use of an Atypical Tunnel Oxide Layer Formation Method

As an example, the Skilled Artisan could have placed a metal shadow mask, in the shape of Jin's Fig. 9 mask, on the substrate to cover the periphery before forming the tunnel oxide and phosphorous-doped polysilicon layers using PECVD.

EX1003-Decl., ¶117. The metal mask could then be lifted off the substrate, leaving the oxide and polysilicon layers only in the areas not covered by the mask—the entire surface of the substrate with the exception of the gap-T isolation region. *Id.* (Dr. Banerjee's declaration provides other well-known techniques as well. EX1003-Decl., ¶¶118-121.)

Paper 1, Petition at 26

Tunnel Oxides Were Typically Formed by Oxidizing the Silicon Substrate Surface Without a Mask

2. Fabrication of TOPCon solar cells

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boron diffusion is removed. After cleaning with chemicals, a tunneling SiO_x is thermally developed and a pure poly silicon layer (minimum partially poly-crystalline) is accumulated in a LPCVD system. The pure poly-silicon is doped in a phosphoryl

Ex. 2004 at 76

over the tunnel oxide. The n-TOPCon structure of these first cells was realized by growing a thin interfacial oxide in HNO_3 , depositing a phosphorus-doped Si-rich SiC_x layer by plasma-enhanced chemical vapor deposition (PECVD), thermal annealing at 800–900°C, and a hydrogen passivation step. The thermal annealing leads to a diffusion

Ex. 2006 at 3

(see also Paper 16, Response at 29-31 ; Paper 25, Sur-Reply at 4)

Feldmann Employs This Type of Typical Oxidation Process

procedure [11]. Then an ultra-thin wet chemical oxide layer was grown with a thickness determined to be about 14 Å by spectroscopic ellipsometry. It should be noted, that 20 Å is the maximum tolerable oxide thickness for the related metal–insulator–semiconductor (MIS) solar cells at which tunneling becomes inefficient and, thus, results in a lowered *FF* [12]. Subsequently, a 20 nm thick phosphorus-doped

Ex. 1012, Feldmann at 271

(see also Paper 16, Response at 29-30; Paper 25, Sur-Reply at 4)

Patent Owner's Unrebutted Expert Testimony: Typical Prior Art Methods Would Be Used During Tunnel Oxide Formation

199. Rather than employing the convoluted process Petitioner proposes, in my opinion, a POSITA would have instead manufactured the combined TOPCon cell of Jin and Feldmann using the processes actually taught in the art.

200. First, a tunnel oxide would be formed over the entire backside of the substrate in a separate, maskless processing step (such as thermal oxidation). This process would be carefully controlled to ensure uniformity and proper layer thickness. This process would be carefully controlled to ensure uniformity and proper layer thickness and optimized to minimize defects and impurities in the layer thus provided.

*Ex. 2001, Peckerar Decl., ¶¶ 199-200
(see also Paper 16, Response at 31-32; Paper 25, Sur-Reply at 4)*

The Petition *Did Not Explain* Why the Tunnel Oxide Would be Excluded from the Isolation Portion

passivation.” EX1012-Feldmann, Abstract. And because Feldmann’s emitter, like Jin’s, is formed by diffusion, it is susceptible to shorting and would benefit from Jin’s gap-T isolation region. EX1003-Decl., ¶113. Indeed, following Feldmann, Chang disclosed a bifacial solar cell with Feldmann’s TOPCon structure and Jin’s isolation region. *Id.*

*Paper 1, Petition at 25-26
(see also Paper 16, Response at 25)*

Petitioner's Expert Opinion is Conclusory and Devoid of Evidentiary Support

would benefit from Jin's gap-T isolation region to prevent shorting. In addition, the Skilled Artisan would have been motivated to have both the polysilicon layer and the tunnel oxide layer be separated from the edge of the substrate with Jin's gap-T isolation region. If the tunnel oxide layer were to extend to the edge, the exposed portions of the oxide could trap impurities and create negative fixed oxide charges, which could then create a p-type inversion in the n-type base substrate, leading to a leakage path to the p-type emitter on the front of the solar cell. And, as discussed in §V.D above, following Feldmann, Chang disclosed a bifacial solar cell with Feldmann's TOPCon structure and Jin's isolation region, in which both the polysilicon layer and the tunnel oxide layer are separated from the edge of the substrate by an isolation region.

*Ex. 1003, Banerjee Decl., ¶ 113
(see also Paper 16, Response at 27)*

Use of Typical Thermally Grown Tunnel Oxides Admittedly Eliminates the Need to Form the Claimed Isolation Portion

Q. Now, if you thermally grew a tunnel oxide, it would not result in the type of p-type inversion that you show in your figures in paragraph 53.

Correct?

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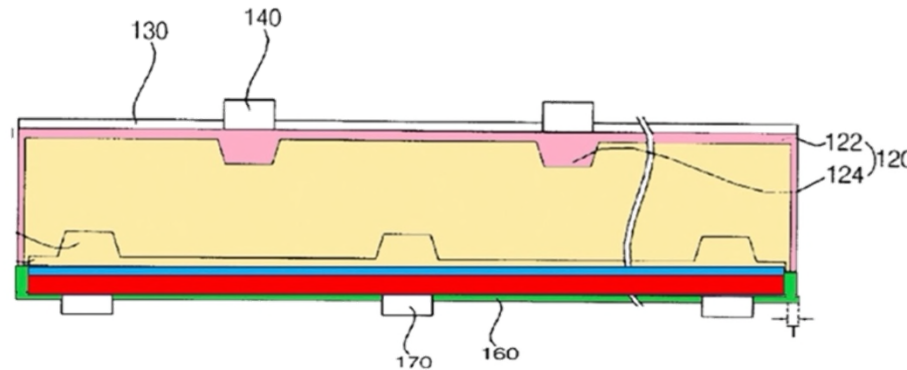
A. If you had a thermally grown oxide with positive charges, and the base, the semiconductor solar cell base was n-type, then it would not lead in a p-type inversion layer.

*Ex. 2010, Banerjee Depo., 26:12-21
(see also Paper 25, Sur-Reply at 7)*

Petitioner's Combination Places Silicon Oxide Back Into the Very Location Where the Tunnel Oxide Was Removed

163. Next, in Dr. Banerjee's combination, the backside of the combined Jin / Feldmann structure is coated with a passivation film 160. The passivation film (shown in green in Dr. Banerjee's demonstrative below) is located between the doped polysilicon layer (shown in red) and frontside emitter 120 (shown in pink):

Combination of Jin and Feldmann



(Ex. 1003, ¶ 138.)

164. Jin explains that this layer 160 can be formed from, among other things, a “silicon oxide.” (Jin, [0050].)

*Ex. 2001, Peckerar Decl, ¶¶ 163-164
(see also Paper 16, Response at 27-28)*

Patent Owner's Unrebutted Expert Testimony: Masks Were Not (and Could Not Be) Used to Form a Tunnel Oxide Layer

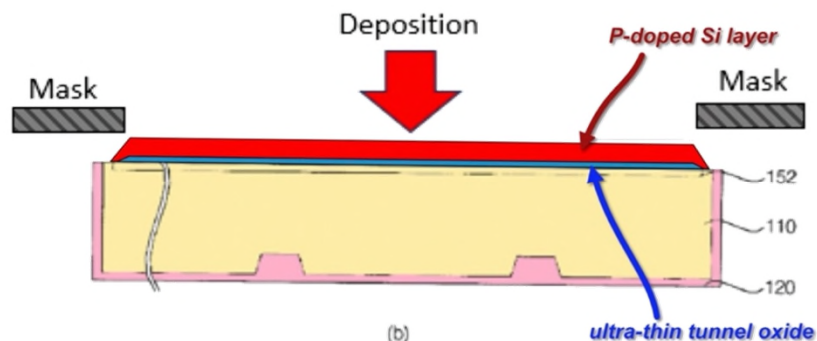
196. A POSITA would have recognized that use of a shadow mask when forming the tunnel oxide layer would likely result in significant layer variation around the mask edges, caused by variation in the thickness of the separation between the mask and the work-piece. This would worsen device uniformity and performance. A shadow mask would not provide the requisite degree of control and repeatability, especially given the dimension of the isolation portion, which could be as little as 1 nm. (*E.g.*, Ex. 1001, 2:31-32.) It simply would not have been possible to control the layer's physical extent in the manner proposed by Petitioner and Dr. Banerjee.

197. Showing this, no TOPCon cell manufacturer or researcher had—or even could have—employed a masking process that even remotely resembles that proposed by Petitioner and Dr. Banerjee. This is reflected by the various exhibits I discuss above summarizing known TOPCon cell manufacturing processes. (*See* Exs. 2004, 2006, 2008.)

*Ex. 2001, Peckerar Decl., ¶¶ 196-197
(see also Paper 16, Response at 30-31)*

Patent Owner's Unrebutted Expert Testimony: Use a Mask Results in the Very Problem Petitioner Attempts to Avoid

218. Thus (and once again if this type of process were even possible, which it is not), rather than producing the layered structure referenced in the Petition and by Dr. Banerjee, the following would be more likely result:

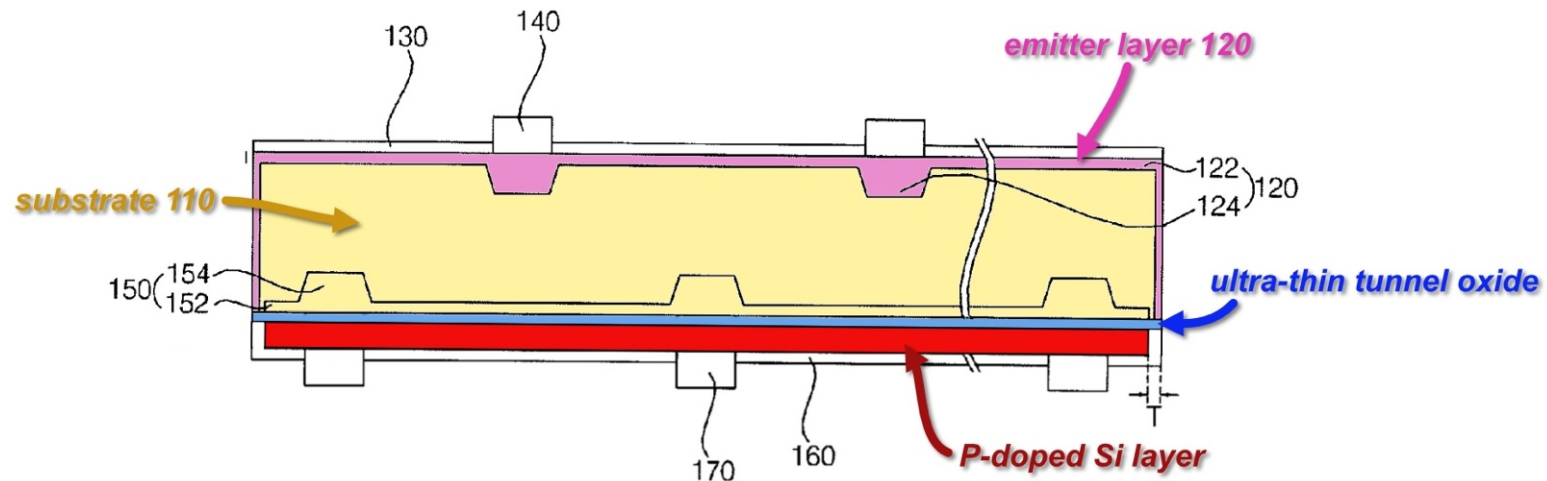


219. As shown, the thicker polysilicon layer with increased overspray results in the very thing the Petition seeks to avoid: polysilicon on the substrate in close proximity to Jin's emitter layer 120.

*Ex. 2001, Peckerar Decl., ¶¶ 218-219
(see also Paper 16, Response at 34-35)*

Even If Jin and Feldmann Were Combined, a POSITA Would Have Done So in a Way that Does Not Satisfy the Claims

FIG. 3



- ✓ Employs known and typical manufacturing methods
- ✓ Better ensures that there is no polysilicon / emitter contact
- ✓ Ensures that there is no dopant diffusion into substrate
- ✓ Improves efficiency and passivation
- ✓ Would use Feldmann's rear side metallization (rather than Jin's special doping to accommodate finger electrodes)

*Ex. 2001, Peckerar Decl., ¶¶ 138-144
(see also Paper 16, Response at 23-24)*

Petitioner's Proposed Combination Eliminates All the Efficiency Improving Features of Both Jin and Feldmann

Jin:

- Substrate “doping density” and “doping thickness” tailored to “reduce surface resistance” with “finger lines”

Ex. 1009, Jin at [0032]

Feldmann:

- “Vital” to include tunnel oxide across entire rear surface to achieve “excellent passivation”
- Employs full “rear metallization” and no “point contacts”
- Increases “rear side reflection”
- Does not employ rear “insulating dielectric layer” which “contradict[s]” TOPCon structure

Ex. 1012, Feldmann at 270, 272-274

(see also Paper 16, Response at 35-38; Paper 25, Sur-reply at 9-10)

Petitioner Repeatedly (and Improperly) Cites the '104 Patent Itself as Evidence of Obviousness

¶50; EX1037-SuppDecl., ¶¶59-60; EX1001, 11:33-39. The POR does not contend that materials other than oxides would trap detrimental impurities, and provides no unexpected results by the 104 Patent's removal of the tunnel oxide at the edge portion and then coating with the same list of antireflection film materials as Jin. The lack of unexpected results supports the finding that the claimed invention was obvious. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007) (“[W]hen a

E.g., Paper 20, Reply at 23

Petitioner Did Not Carry Its Burden: The Prior Art Fails to Render the Claims Obvious

- ✗ The Petitioner *failed* to show why a POSITA would have combined Jin and Feldmann
- ✗ The Petitioner *failed* to show why a POSITA would have combined Chang and Jin
- ✗ The Petitioner *failed* to show why the art renders dependent claim 6 of the '104 patent obvious

Petitioner's Improper Approach to Obviousness

- Ignores that Chang teaches that its cell is designed to **eliminate the need for isolation**
- Requires use of a **specific** manufacturing method (once again without any motivation for doing so)
- **Does not explain** why a POSITA would have been motivated to locate Chang's "isolation region" where the claims require
- Picks and chooses from Chang's various embodiments **without any explanation why**

*Paper 16, Response at 40-46;
Paper 25, Sur-Reply at 13-19*

None of Chang's Embodiments Include the Claimed "Isolation Portion"

FIG. 1

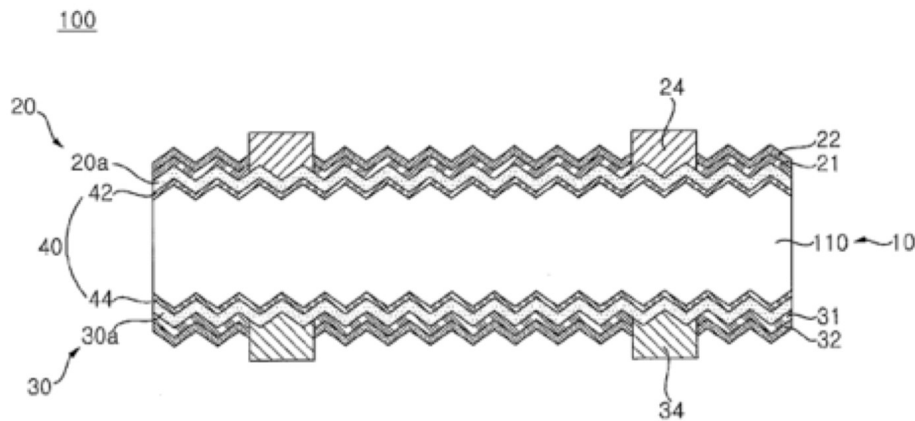
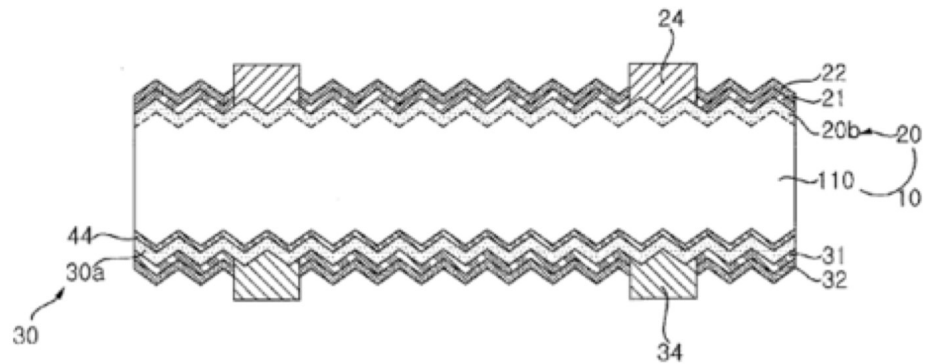


FIG. 8



*Ex. 1013, Chang at Figs. 1, 8
(see also Paper 16, Response at 41)*

Chang Explains that its Cell Is Specifically Designed to Avoid the Need to Perform Isolation

[0076] In this instance, the emitter area 20 and the back surface field area 30 may be disposed at different sides of the semiconductor substrate 10 to form a double-surface light-receiving type structure. As a result, light is incident upon the back surface of the semiconductor substrate 10 as well as the front surface of the semiconductor substrate 10, thereby increasing an amount of incident light and improving efficiency of the solar cell 100. Because the emitter area 20 and the back surface field area 30 are not adjacent to each other, the necessity of performing an isolation process when the emitter area 20 and the back surface field area 30 are formed to be adjacent to each other is eliminated. In addition, because the emitter area 20 and the back surface field area 30 are entirely formed, thus requiring no additional patterning and alignment processes. As a result, manufacturing process is simplified and cost is thus reduced.

*Ex. 1013, Chang at [0076]
(see also Paper 16, Response at 42-43)*

Petitioner Once Again Relies on the Use of a Specific Manufacturing Method (Without Any Motivation)

isolation region, PO simply asks the Board to ignore it. PO repeats its preliminary response argument, pointing to a single paragraph in Chang (¶76) it interprets as “eliminating” the need for any isolation at all. POR, 42-45. PO’s argument fails to address the fact that paragraph 76 of Chang addresses a specific embodiment different than the one relied on by the Petition.

In particular, Chang discloses that the front emitter area 20 may be formed by thermal diffusion *or* ion implantation. EX1013-Chang, ¶98. As discussed above in §II.A, thermal diffusion results in dopants diffused down the lateral sides of the substrate. As shown below, when the tunnel oxide layer and BSF are

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In contrast, ion implantation can advantageously “eliminate the need for edge isolation.” EX1038-Rohatgi, 5:18-21. This is because ion implantation accelerates a beam of dopants at the surface of the substrate, where they penetrate and settle an average distance into the substrate. EX1030-Streetman, 159; EX1037-SuppDecl., ¶27. Thus, doping occurs only where the beam is directed, such as the front of the substrate, *without* doping the lateral sides, and no edge isolation is needed. EX1037-SuppDecl., ¶¶27-28.

*Paper 20, Reply at 6-7
(see also Paper 15, Sur-Reply Response at 14-15)*

Even Petitioner's Chosen Thermal Diffusion Method Does Not Require the Claimed "Isolation Portion"

Q. So one other question about this.

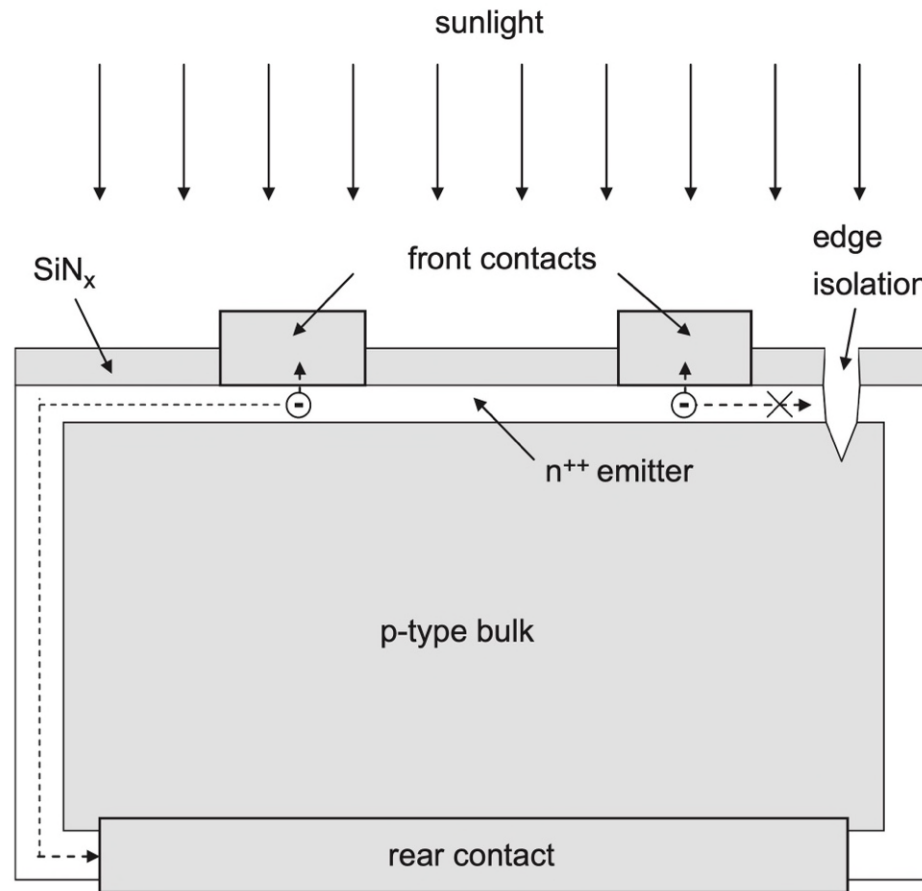
Can you perform thermal diffusion in a way that would not result in doping in the sides of a solar cell substrate?

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A. That scenario is not discussed in my report or in these prior art. But in general, yes, it is possible. You can always block thermal diffusion or dopants, if you had a sufficiently thick diffusion mask. And what I

*Ex. 2010, Banerjee Depo., 14:23-15:9
(see also Paper 25, Sur-Reply at 15)*

Chang's "Isolation Region or the Like" Can Be in Locations Other than the Cell Edge



*Ex. 1026 at 1639
(see also Paper 16, Response at 44)*

Petitioner Improperly Picks and Chooses (Without Explanation) From Chang's Different Design Options

Petitioner:

- “[E]xclud[es]” only backside polysilicon and tunnel oxide from “periphery region, isolation region or the like”
Paper 20, Reply at 10
- Employs thermal diffusion to form frontside layers
Paper 20, Reply at 6-7
- Forms passivation film over entire backside
Paper 20, Reply at 4
- Employs CVD to form tunnel oxide
Paper 20, Reply at 22

(see also Paper 25, Sur-Reply at 14-18)

Chang:

- Frontside layers have same physical extent as backside layers
Ex. 1013, Chang, [0045], [0051], [0056], [0062]
- Ion implantation can be used also be used
Ex. 1013, Chang, [0098]
- Passivation film meant to be coextensive with other backside layers
Ex. 1013, Chang, [0063]
- Thermal growth can also be employed
Ex. 1013, Chang, [0146]

Petitioner Did Not Carry Its Burden: The Prior Art Fails to Render the Claims Obvious

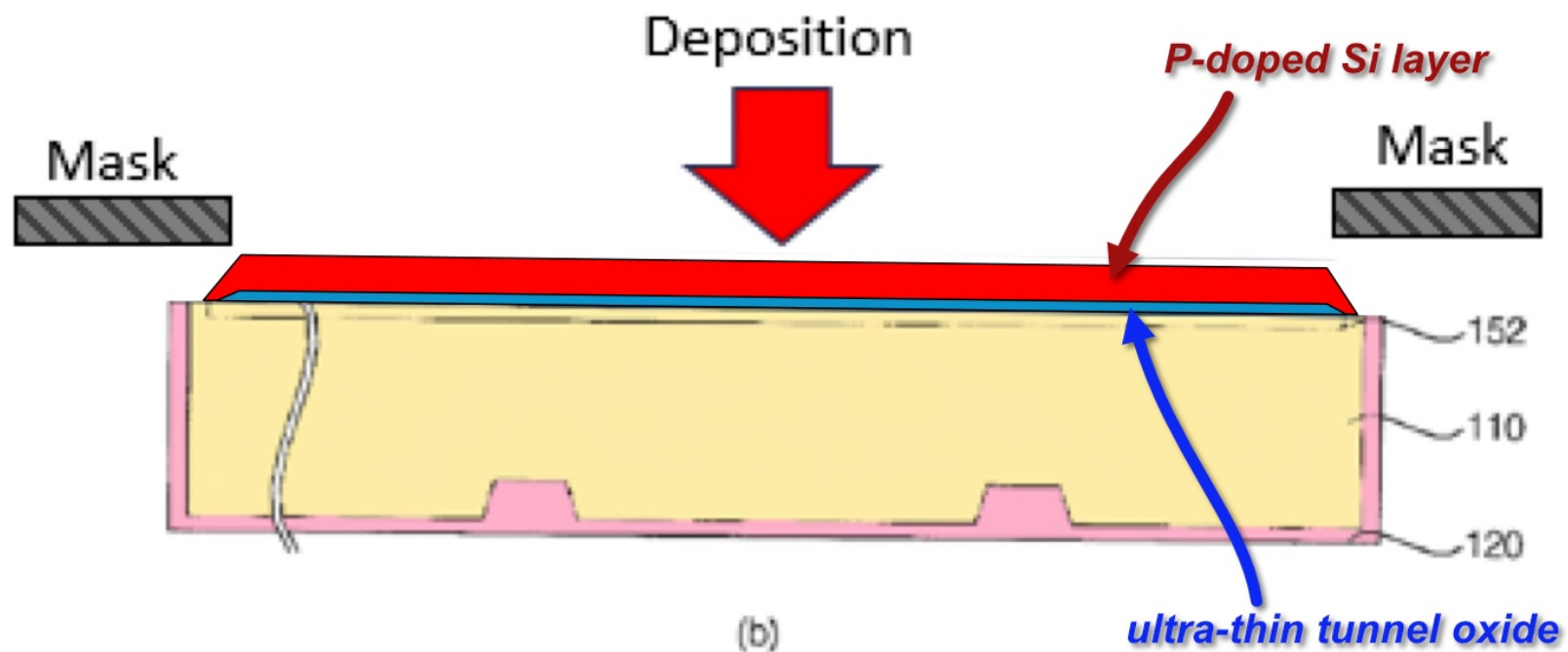
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- ✗ The Petitioner *failed* to show why a POSITA would have combined Chang and Jin
- ✗ The Petitioner *failed* to show why the art renders dependent claim 6 of the '104 patent obvious

'104 Patent Claim 6

6. The solar cell of claim 1, wherein a thickness of an edge region in the first conductive type semiconductor region progressively decreases towards the isolation portion.

*Ex. 1001, '104 Patent, Claim 6
(see also Paper 16, Response at 40)*

Petitioner Does Not Contest that There Will Be Polysilicon In What It Identified as the “Isolation Portion”



Paper 16, Response at 35, 40

Instead, Petitioner Changed Position and Introduced an Entirely New (and Unsupported) Argument in Reply

polysilicon thickness decreases. EX1001, FIG. 2. Nor is the “*isolation portion*” defined by the width of the mask used to create the isolation gap. PO’s own illustration of the “more likely result” of the polysilicon overspray using Jin’s mask admittedly shows that even when the polysilicon tapers, there is still a gap/isolation region where ***both the polysilicon and the tunnel oxide are absent***. POR, 35.

*Paper 20, Reply at 14-15
(see also Paper 25, Sur-Reply at 20)*

There Are No Relevant Differences Between the Claims of the '104 and '009 Patents

'104 Patent	'009 Patent
[1pre] A solar cell, comprising:	[1pre] A solar cell, comprising:
[1a] a semiconductor substrate;	[1a] a silicon semiconductor substrate <i>having a first conductive type</i> ;
[1b] a tunnel layer on a first surface of the semiconductor substrate;	[1b] an oxide layer on a first surface of the silicon semiconductor substrate;
[1c] a first conductive type semiconductor region on the tunnel layer and containing impurities of a first conductive type;	[1c] a polysilicon layer on the oxide layer and having <i>the first conductive type</i> ;
[1d] a second conductive type semiconductor region on a second surface opposite to the first surface of the semiconductor substrate and containing impurities of a second conductive type opposite to the first conductive type;	[1d] an emitter region at a second surface of the silicon semiconductor substrate opposite to the first surface and having a second conductive type opposite to the first conductive type;
[1e] a first passivation film on the first conductive type semiconductor region;	[1e] a first passivation film on the polysilicon layer ;
[1f] a first electrode formed on the first passivation film and connected to the first conductive type semiconductor region through an opening formed in the first passivation film;	[1f] a first electrode connected to the polysilicon layer through an opening formed in the first passivation film;
[1g] a second passivation film on the second conductive type semiconductor region;	[1g] a second passivation film on the emitter region;
[1h] a second electrode formed on the second passivation film and connected to the second conductive type semiconductor region through an opening formed in the second passivation film; and	[1h] a second electrode connected to the emitter region through an opening formed in the second passivation film; and
[1i] an isolation portion for preventing a contact between the first conductive type semiconductor region and the second conductive type semiconductor region,	[1i] an isolation portion for preventing a contact between the polysilicon layer and the emitter region,
[1j] wherein the isolation portion excludes the tunnel layer and the first conductive type semiconductor region, and is in an edge portion of the first surface of the semiconductor substrate, and	[1j] wherein the isolation portion excludes the oxide layer and the polysilicon layer , and is in an edge portion of the first surface of the silicon semiconductor substrate, and
[1k] wherein the first passivation film covers the first surface of the semiconductor substrate and the isolation portion together.	[1k] the first passivation film covers the first surface of the silicon semiconductor substrate and the isolation portion together.
[6] The solar cell of claim 1, wherein a thickness of an edge region in the first conductive type semiconductor region progressively decreases towards the isolation portion.	[8] The solar cell of claim 1, wherein a thickness of the edge portion in the polysilicon layer progressively decreases toward the isolation portion.