

Enhancement-Mode GaN MIS-HEMTs for Power Supplies

T. Imada, M. Kanamura and T. Kikkawa

FUJITSU LABORATORIES LTD., 10-1 Morinosato-Wakamiya, Atsugi City, 243-0197
TEL: +81-46-250-8243, FAX: +81-46-250-8168, E-mail: imada.tadahiro@jp.fujitsu.com

Abstract—In this paper, we present the current status of GaN-high electron mobility transistor (HEMT) for power-supply-applications. Advantages of GaN HEMT are summarized with discussing required characteristics applying for power supplies.

Then, we introduce our Enhancement-mode (E-mode) GaN MIS-HEMT technology. We focused on realizing both normally-off operation and high current density with high breakdown voltage. Detailed results are discussed in this paper. In particular, we developed a unique device structure called triple layer cap structure. High current density with normally-off mode was successfully achieved, which is preferable for power-supply application. We also demonstrated high speed performance with low on-resistance.

Index Terms— GaN, MIS-HEMT, ALD, Enhancement-mode

I. INTRODUCTION

The GaN high electron mobility transistors (HEMTs) have a high breakdown voltage with a high cutoff frequency. Currently GaN HEMTs for transmitter power amplifiers (PAs) of wireless base stations have been commercialized [1]. The GaN HEMT is also well recognized to be a good candidate for the next generation power-conversion devices (Table 1). The application of GaN HEMT is, for example, power factor corrector (PFC) or power supply unit (PSU) for servers (Fig. 1). Enhancement-mode (E-mode) operation is necessary for these applications. However, conventional GaN HEMTs is unsuitable for Enhancement-mode operation due to its strong piezo-electric effect.

TABLE I
CHARACTERISTICS OF SEMICONDUCTOR

Material	Band Gap (eV)	Breakdown Electric Field (V/m)	Thermal Conductivity (W/cm/K)	Electron Density (/cm ²)	Electron Mobility (cm ² /V/s)	Saturation Velocity (cm ² /V/s)	Dielectric Constant	Baliga FOM
Si	1.1	0.3	1.5	$\sim 10^{12}$	1300	1.0	11.8	414
GaAs	1.4	0.4	0.5	$\sim 10^{12}$	3000	1.3	12.8	2460
SiC	3.2	3.0	4.9	$\sim 10^{12}$	600	2.0	10.0	162000
GaN (HEMT)	3.4	3.0	1.5	$\sim 10^{13}$	1500	2.7	9.5	385000

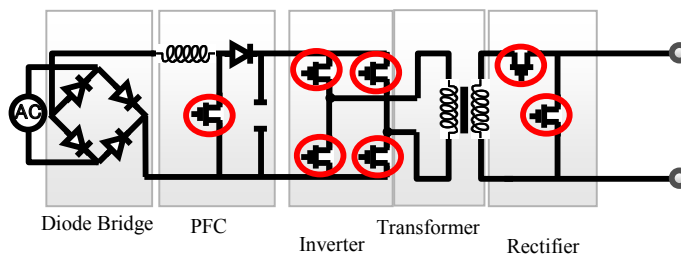


Fig. 1 PSU Circuit

As shown in Table 2, There are several approaches to realize Enhancement-mode operation for GaN HEMTs such as a gate recess structure[2],[3], F-treatment [4],[5], an introduction of InGaN cap layer [6] , adding p-GaN cap layer [7], using a piezo neutralization layer [8], and MOS-FET structure[9],[10]. Previous works reports applied these E-mode devices to circuits [4],[5],[7],[11]-[13]. But it is difficult to fabricate a GaN-HEMT with a high maximum drain current density and a threshold voltage over 2V.

We have developed recessed E-mode AlGaIn/GaN metal-insulator-semiconductor (MIS) HEMTs with novel n-GaN/AlN/n-GaN triple cap layers and an atomically deposited Al₂O₃ gate dielectric layer [14]. This was the first GaN-HEMT exhibiting normally-off characteristics and high current density with high breakdown voltage.

II. DEVICE STRUCTURE

The AlGaIn/GaN MIS-HEMTs in this study consists of n-AlGaIn/i-GaN HEMT structure on S.I.-SiC substrate with n-GaN/AlN/n-GaN triple cap layers as shown in Fig. 2. All layers were grown on a 3-inch SiC substrate by MOCVD [15]. The thickness of n-GaN/AlN/n-GaN thin triple-layers was 2/2/2 nm. The thickness of the AlGaIn electron supply layer is around 20 to 25 nm.

TABLE II
APPROACH TO REALIZE ENHANCEMENT MODE GAN DEVICE

Method	Gate recess	"F" treatment	InGaN cap p-GaN cap cap	Piezo Neutralization Layer	MOS Structure
Advantage	Small current collapse Epitaxial growth (no p-GaN, InGaN)	Current density Epitaxial growth	Controllability of V_{th} Forward breakdown voltage	Controllability of V_{th} Epitaxial growth	Low leak current High breakdown voltage
Disadvantage or unclear point	Controllability Damage Roughness	Controllability Damage Reliability	Epitaxial growth Reliability	Low V_{th} value	Epitaxial growth Reliability Low I_{max}

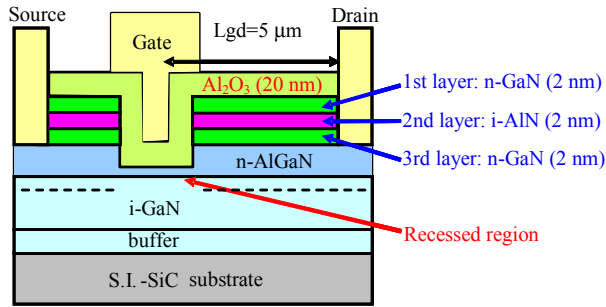
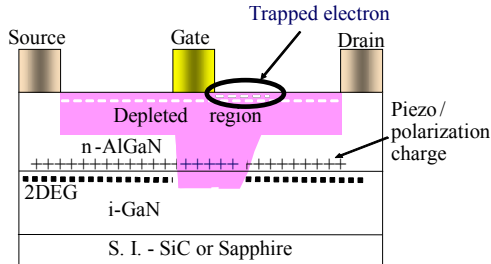


Fig. 2 Cross-sectional view of AlGaIn/GaN MIS-HEMT structure used in this work.

1. Pinched off state, $V_{ds} > 50$ V



2. On state after pinched off state V_{ds}

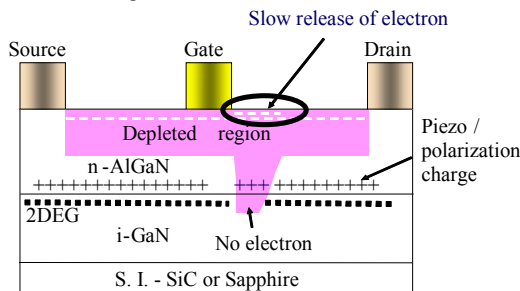


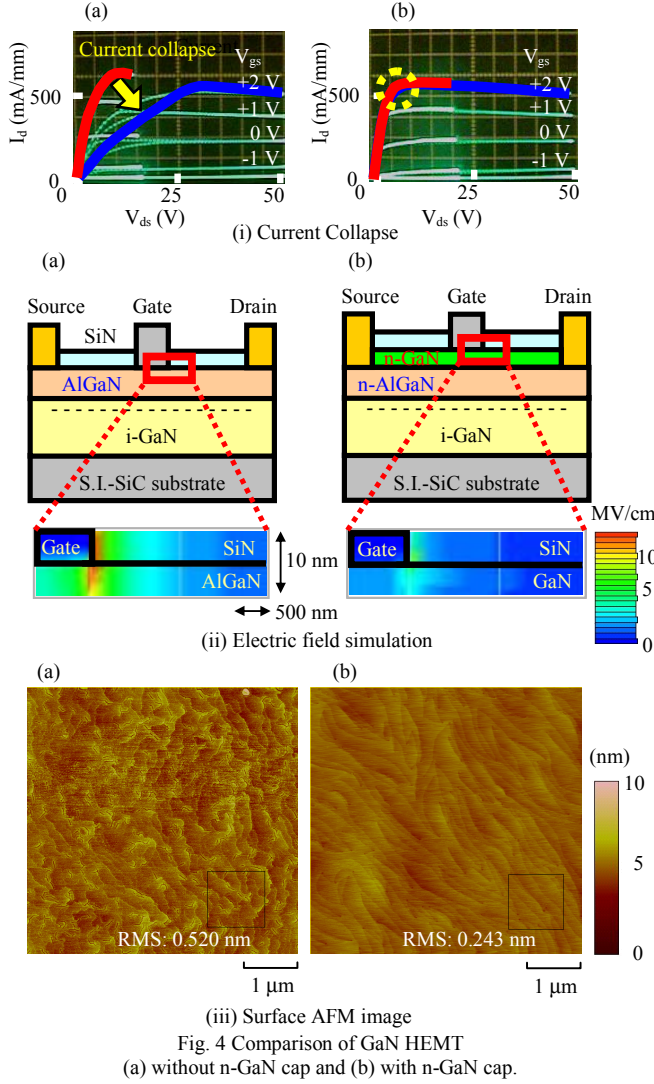
Fig. 3 Schematic of GaN HEMT current collapse.

For PAs of base station application, we have developed n-GaN cap structure, called a surface-charge-controlled structure [16]. By using an n-GaN cap layer, instead of an AlGaIn layer, surface oxidation and frequency-dispersion-related surface instability could be prevented. For example, n-GaN cap structure suppresses current collapse, which is a key issue for the GaN based devices. Current collapse is the phenomena that on resistance changes when the transistor turns on [17]. It is considered mainly because of traps on the surface of GaN device [18]-[20]. Hypothesis of current collapse mechanism is shown in Fig. 3. In off state, high electric field will occur at the drain side edge of gate if high voltage is applied between source and drain. In this case, electrons are trapped on the surface of this area. These trapped electrons cannot be released easily even if gate voltage becomes turned-on, which results in the increase of on resistance.

Figure 4 shows the measured current collapse, electric field simulation and surface roughness. The results of n-GaN cap layer structure were compared with conventional AlGaIn cap layer structure. By embedding this n-GaN cap layer on the top layer, current collapse could be suppressed. This is attributed to the reduced the concentration of electric field at the gate edge and smooth surface.

The second 2-nm AlN layer inserted in n-GaN cap causes conduction band bending to the downside because a polarization-induced electric field at the interface between AlN and GaN is strongly induced. Figure 5 shows the schematic energy band diagram of our fabricated HEMT structure. This conduction band bending increases the two-dimensional electron gas (2DEG) density. As a result, sheet resistance (R_{sh}) of Al-GaN/GaN HEMT with the piezoelectric-induced triple-layer cap structure was 27% lower than that of our conventional single n-GaN cap structure [21] remaining high breakdown voltage. On the other hand, a second

2DEG might be generated in the n-GaN cap layer on the bottom side when forward gate bias is applied. This second 2DEG can be the origin of the gate leakage path. Penetration of recess through triple cap (Fig. 2) makes this device able to suppress the increasing gate-drain leakage current.



The 2-nm GaN layer on the surface side is formed to keep a smooth surface morphology on the strained AlN layer. Figure 6 shows the surface morphology of the epitaxial layer with the triple-layer cap structure, compared with the AlN/GaN double layer cap structure without the surface-side GaN cap. An atomic force microscope (AFM) was used to measure the surface just after epitaxial growth. A lot of cracks were observed in the surface of the structure with AlN/GaN double layer cap which was terminated with AlN. On the other hand, the structure with the triple-layer cap had a substantially smoother surface. Root-mean-square (RMS) values for surface morphology were improved drastically from 0.56 nm to 0.14 nm.

The third GaN layer on the bottom side is inserted to compensate strain of AlN to obtain good morphology for high reliability.

Under gate electrode, there is a 20 to 25 nm-depth gate recessed region with the 20-50 nm Al_2O_3 gate dielectric layer. Al_2O_3 was deposited by atomic layer deposition (ALD) technique. Al_2O_3 has high band discontinuity to GaN, which is essential for E-mode operation. The dielectric constant of Al_2O_3 is also high (~ 8.0) so that carrier was well-controlled by the gate bias although thickness of the dielectrics is enough thick to suppress gate leak current.

III. DEVICE FABRICATION

Recessed ohmic technology [22] was used to reduce the ohmic contact resistance by removing the triple-layer cap structure at first. For ohmic recess formation, reactive ion etching (RIE) was used with Cl_2 gas. After removing the cap structure, ohmic metal was evaporated. Ohmic electrodes were annealed at a relatively low temperature of 550°C for 30 sec in N_2 ambient to keep the metal surface smooth. Next, the gate recess was formed by RIE with Cl_2 gas. In order to improve controllability of the etching depth and to keep a smooth surface morphology, the etching rate was reduced. The etching depth was about 20-25 nm and controlled by timing. Etching depth was measured by AFM in the nm-order. Thus, the key features to enhance controllability in this study are thin cap layer, slow etching rate, and precise AFM measurement.

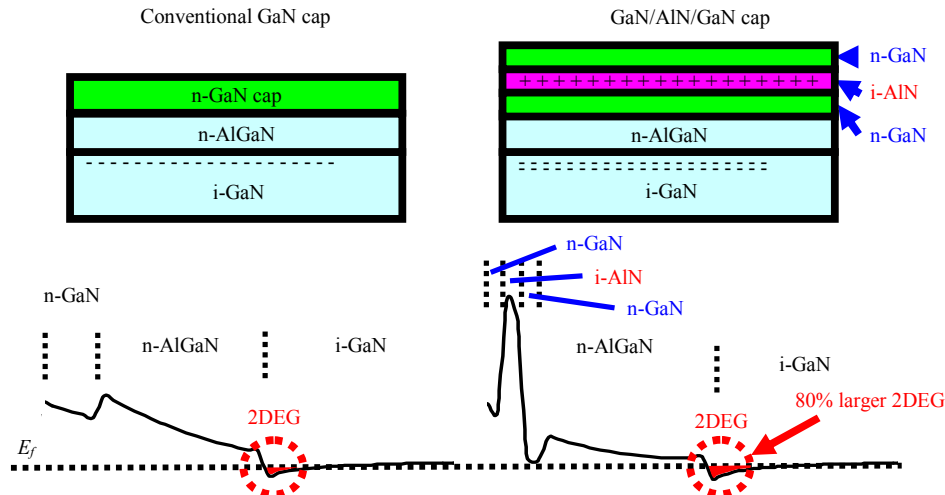


Fig. 5 Effect of 2nd i-AlN Layer

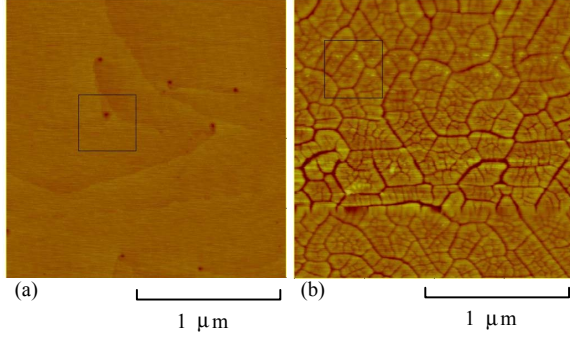


Figure 6 AFM photographs of GaN HEMT (a) with and (b) without surface GaN-cap on AlN layer.

Prior to gate metal deposition, we carried out gate recess etching by Cl-based RIE and deposition of 20-50 nm Al_2O_3 gate dielectrics by plasma-enhanced ALD at 350°C . In the case of designing thin dielectric structure, the ALD method is superior to CVD method in terms of controlling the surface roughness and film thickness. Trimethylaluminum (TMA) and O_2 plasma were used as the metal precursor and an oxidant, respectively. After deposition, we annealed the film at 650°C for 1 min. In this work, we did not carry out intentional surface treatment before deposition. Finally, a Ni/Au gate electrode was formed using an evaporation and lift-off technique. The typical gate length (L_g) was $0.8\text{ }\mu\text{m}$.

IV. DEVICE CHARACTERISTICS

Figure 7 shows the V_{th} dependence of gate recess etching depth. As recess etching depth increases, V_{th} changes linearly. V_{th} showed Enhancement-mode when a recess etching depth became deeper than 15 nm.

I_{ds} - V_{gs} characteristics for the recessed and non-recessed devices are shown in Fig. 8. The gate recessed structure dramatically changed the V_{th} from -5.8 V to $+3\text{ V}$ without any degradation of maximum drain current. The recessed GaN MIS-HEMT clearly showed the Enhancement-mode operation with a high maximum drain current of 860 mA/mm at $V_{gs} = 10\text{ V}$. The drain current at $V_{gs} = 0\text{ V}$ was $9\text{ }\mu\text{A/mm}$. The maximum transconductance was 155 mS/mm . The gate recess etching depth was around

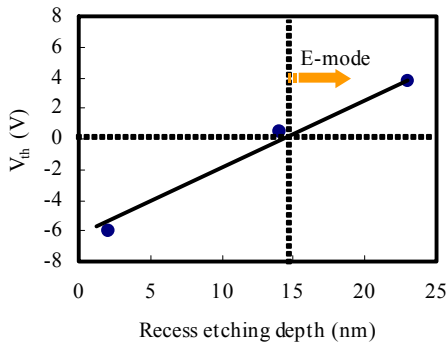


Fig. 7. V_{th} dependence of gate recess etching depth for AlGaIn/GaN MIS-HEMT.

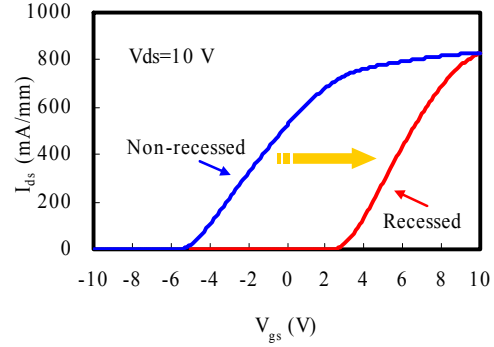


Fig. 8. Drain current and transconductance as a function of gate voltage.

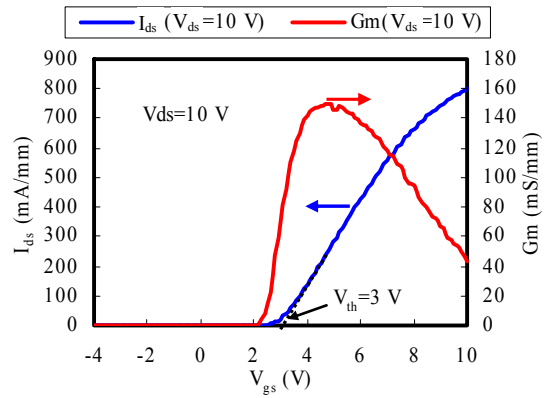


Fig. 9. I_{ds} - V_{gs} and G_m - V_{gs} profile for the E-mode AlGaIn/GaN MIS-HEMT.

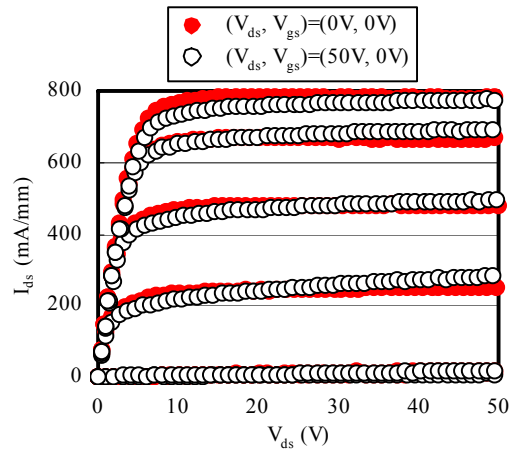


Fig. 10. Pulsed I-V characteristics under two bias conditions. Pulse width was $1\text{ }\mu\text{s}$ and pulse separation was 1 ms . Initial bias point were $(V_{ds}, V_{gs}) = (0\text{ V}, 0\text{ V})$ and $(50\text{ V}, 0\text{ V})$.

V. SWITCHING CHARACTERISTICS

Switching waveform of our developed GaN HEMT with triple cap layers is shown in Fig. 11. Gate width was 144 mm; and chip size is $3.5 \times 5.15 \text{ mm}^2$ (Fig. 12). In this measurement, V_{dd} was 50 V and load resistance was 5 ohm. Switching time was around 10 ns and this value is very small compared with Si MOSFET. R_{on} of this device was $105 \text{ m}\Omega$, and breakdown voltage was 420 V (Fig. 13, Fig. 14). Small total gate charge (Q_g) and capacitance result in this fast switching. Fig. 15 shows the result of Q_g measurement. In this measurement, V_{dd} was set at 10 V, and load resistance was 100 ohm. The gate to source charge (Q_{gs}), the gate to drain charge (Q_{gd}) and Q_g were 3.20 nC, 4.64 nC and 13.8 nC respectively. Fig. 16 shows V_{ds} dependence of capacitance values, such as input capacitance (C_{iss}), output capacitance (C_{oss}) and reverse transfer capacitance (C_{rss}). These capacitance values were very small compared with the Si MOSFET with same current and break down capacity.

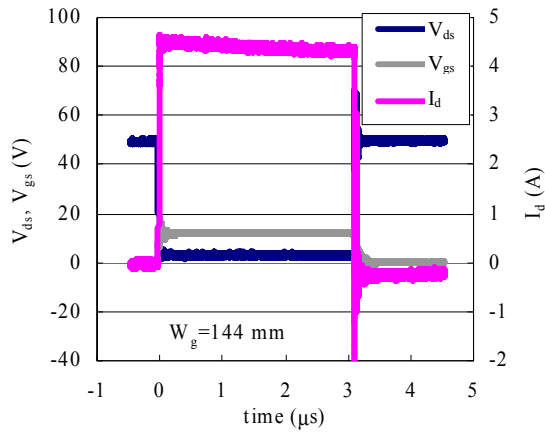


Fig. 11 Switching Waveform of the E-mode AlGaIn/GaN MIS-HEMT.

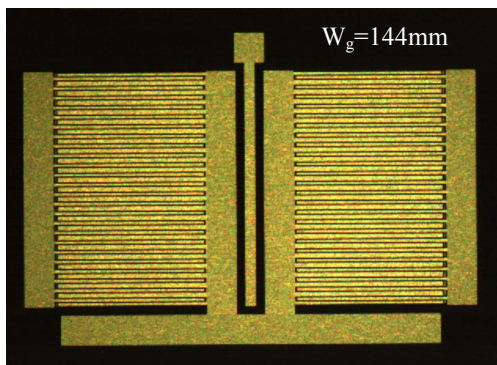


Fig. 12 Photograph of fabricated chip

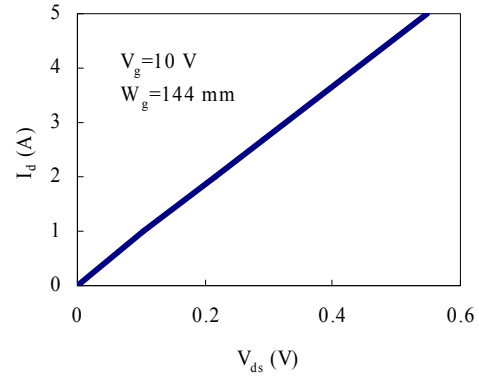


Fig. 13 I_d characteristics of AlGaIn/GaN MIS-HEMT with triple cap.

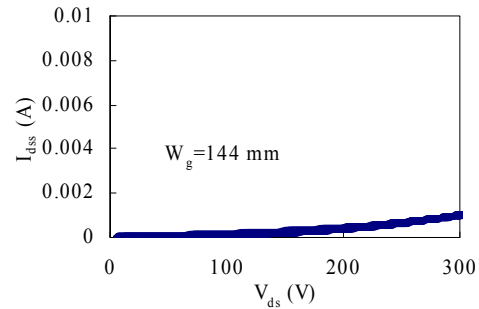


Fig. 14 I_{dss} of the E-mode AlGaIn/GaN MIS-HEMT.

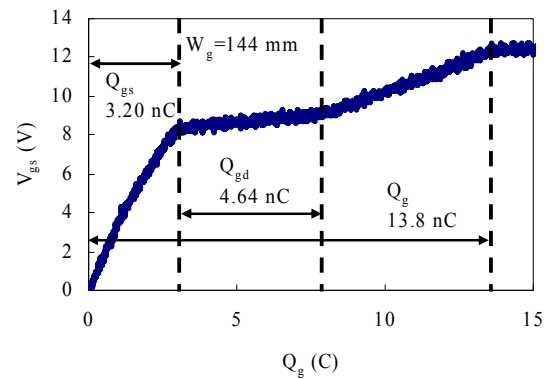


Fig. 15 Result of Q_g measurement

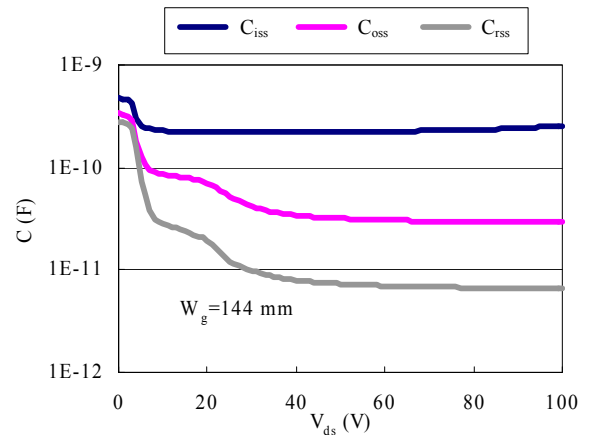


Fig. 16 Dependence of capacitance on V_{ds} ($V_{gs}=0 \text{ V}$)

VI. SUMMARY

We demonstrated AlGaIn/GaN E-mode MIS-HEMTs that exhibited a high maximum drain current density ($I_{\max}$) of 860 mA/mm with a threshold voltage of 3 V by introducing a piezoelectric-induced cap and a recessed ALD-MIS-gate structure. Switching characteristics of this HEMT are also fast compared with Si MOSFET. Figure 17 is the benchmarking of the specific on-resistance ($R_{\text{on}}A$) and the breakdown voltage for E-mode GaN FETs from earlier work [3]-[5],[7],[8],[23]-[27]. The developed GaN device achieved the combination of low on-resistance and high breakdown voltage. Figure 18 shows the benchmark of $I_{\max}$ and V_{th} for the published enhancement-mode GaN FETs which have high three-terminal breakdown voltages over 100 V [2],[5],[7],[8],[23],[25]-[32]. Our developed devices demonstrated a high $I_{\max}$ with sufficiently enough E-mode operation.

These results suggest that the recessed AlGaIn/GaN MIS-HEMT with the triple cap layers could be a promising device structure for power supply electronics.

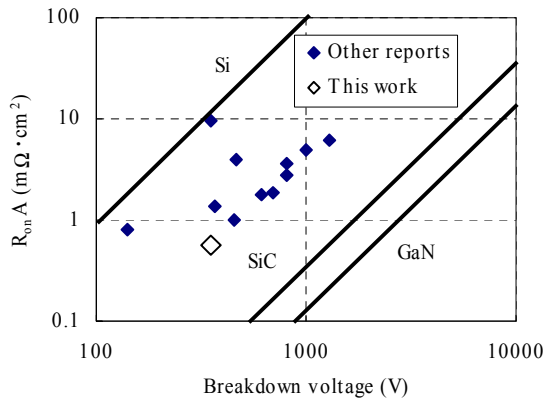


Fig. 17 Benchmarking of breakdown voltage and $R_{\text{on}}A$ for GaN E-mode transistors.

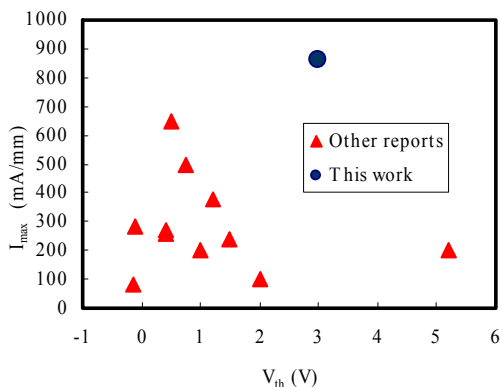


Fig. 18 Benchmarking of threshold voltage and $I_{\max}$ for GaN E-mode transistors.

REFERENCES

- [1] T. Kikkawa, K. Makiyama, T. Ohki, M. Kanamura, K. Imanishi, N. Hara, and K. Joshin, "High performance and high reliability AlGaIn/GaN HEMTs," *Phys. Status. Solidi (a)*, Vol. 206, No.6 (2009), pp.1135-1144.
- [2] T. Oka and T. Nozawa, "AlGaIn/GaN Recessed MIS-Gate HFET with High-Threshold-Voltage Normally-Off Operation for Power Electronics Applications," *Electron Device Lett*, VOL. 29, NO. 7(2008), pp. 668-670.
- [3] N. Kaneko, O. Machida, M. Yanagihara, S. Iwakami, R. Baba, H. Goto and A. Iwabuchi, "Normally-off AlGaIn/GaN HFETs using NiO_x Gate with Recess," *International Symposium on Power Semiconductor Devices & IC's*, 2009, pp. 25-28.
- [4] W. Chen, K.-Y. Wong and K. J. Chen, "Single-Chip Boost Converter Using Monolithically Integrated AlGaIn/GaN Lateral Field-Effect Rectifier and Normally Off HEMT," *Electron Device Lett*, Vol. 30, NO. 5 (2009), pp. 430-432.
- [5] K.S. Boutros, S. Burnham, D. Wong, K. Shinohara, B. Hughes, D. Zehnder and C. McGuire, "Normally-off 5A/1100V GaN-on-Silicon Device for High Voltage Applications," *Proc. International Electron Device Meeting*, 2009, pp. 161-163.
- [6] T. Mizutani, M. Ito, S. Kishimoto, and F. Nakamura, "AlGaIn/GaN HEMTs With Thin InGaIn Cap Layer for Normally Off Operation," *IEEE Electron Device Letters*, vol. 28, no. 7, pp. 549-551, Jul. 2007.
- [7] Y. Uemoto, T. Morita, A. Ikoshi, H. Umeda, H. Matsuo, J. Shimizu, M. Hikita, M. Yanagihara, T. Ueda, T. Tanaka and D. Ueda, "GaN Monolithic Inverter IC Using Normally-off Gate Injection Transistors with Planar Isolation on Si Substrate," *Proc. International Electron Device Meeting*, 2009, pp. 165-168.
- [8] K. Ota, K. Endo, Y. Okamoto, Y. Ando, H. Miyamoto and H. Shimawaki, "A Normally-off GaN FET with High Threshold Voltage Uniformity Using A Novel Piezo Neutralization Technique," *Proc. International Electron Device Meeting*, 2009, pp. 165-168.
- [9] Y. Niiyama, S. Ootomo, H. Kambayashi, N. Ikeda, T. Nomura and S. Kato, "Normally-Off Operation GaN Based MOSFETs for Power Electronics," *Compound Semiconductor Integrated Circuit Symposium*, 2009, pp. 1-4.
- [10] W. Huang, T. P. Chow, Y. Niiyama, T. Nomura and S. Yoshida, "730V, 34mΩ·cm² Lateral Epilayer RESURF GaN MOSFET," *Proc. Int. Symp. Power. Semicond. Devices ICs*, pp.265-268, 2007.
- [11] T. Nomura, M. Masuda, N. Ikeda and S. Yoshida, "Switching Characteristics of GaN HFETs in a Half Bridge Package for High Temperature Applications," *IEEE Trans. on Power Electronics*, Vol. 23, No. 2, pp. 692-697, 2008.
- [12] S. Iwakami, O. Machida, Y. Izawa, R. Baba, M. Yanagihara, T. Ehara, N. Kaneko, H. Goto and A. Iwabuchi, "Evaluation of AlGaIn/GaN Heterostructure Field-Effect Transistors on Si Substrate in Power Factor Correction Circuit," *Jpn. J. Appl. Phys.*, Vol. 46, No. 29, 2007, pp. L721-L723.
- [13] W. Saito, T. Nitta, Y. Kakiuchi, Y. Saito, K. Tsuda, I. Omura and M. Yamaguchi, "A 120-W Boost Converter Operation Using a High-Voltage GaN-HEMT," *IEEE Electron Device Letters*, Vol. 29, NO. 1, pp. 8-10, Jan. 2008.
- [14] M. Kanamura, T. Ohki, T. Kikkawa, K. Imanishi, T. Imada, A. Yamada and N. Hara, "Enhancement-Mode GaN MIS-HEMTs With n-GaN/i-AlN/n-GaN Triple Cap Layer and High-k Gate Dielectrics," *IEEE Electron Device Letters*, vol. 31, no. 3, pp. 189-191, Mar. 2010.

- [15] T. Ohki, T. Kikkawa, M. Kanamura, K. Imanishi, K. Makiyama, N. Okamoto, K. Joshin, and N. Hara, "An over 100 W AlGaIn/GaN enhancement-mode HEMT power amplifier with piezoelectric-induced cap structure," *Phys. Status. Solidi C* 6, no. 6, pp. 1365-1368, 2009.
- [16] T. Kikkawa, M. Nagahara, N. Okamoto, Y. Tatenno, Y. Yamaguchi, N. Hara, K. Joshin, and P. M. Asbeck, "Surface-Charge Controlled AlGaIn/GaN-Power HFET without Current Collapse and Gm Dispersion," *IEEE IEDM Tech. Digest*, pp. 585-588 (2001).
- [17] G. Simin, A. Koudymov, A. Tarakji, X. Hu, J. Yang, M. Asif Khan, M. S. Shur, and R. Gaska, "Induced strain mechanism of current collapse in AlGaIn/GaN heterostructure field-effect transistors," *Appl. Phys. Lett.*, vol. 79, pp. 2651-2653, 2001.
- [18] M. A. Khan, M. S. Shur, Q. C. Chen, and J. N. Kuznia, "Current/voltage characteristic collapse in AlGaIn/GaN heterostructure insulated gate field effect transistors at high drain bias," *Electron. Lett.*, vol. 30, pp. 2175-2176, 1994.
- [19] Steven C. Binari, Kiki Ikossi, Jason A. Roussos, Walter Kruppa, Doewon Park, Harry B. Dietrich, Daniel D. Koleske, Alma E. Wickenden, and Richard L. Henry, "Trapping effects and microwave power performance in AlGaIn/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 48, pp. 465-471, 2001.
- [20] Jin-Ping Ao, Yuya Yamaoka, Masaya Okada, Cheng-Yu Hu, and Yasuo Ohno, "Investigation on current collapse of AlGaIn/GaN HFET by gate bias stress," *IEICE Trans. Electron.*, vol. E91-C, pp. 1004-1008, 2008.
- [21] T. Kikkawa, K. Imanishi, M. Kanamura, and K. Joshin, "Recent Progress of Highly Reliable GaN-HEMT for Mass Production," *Int. Conf. Compound Semiconductor MANTECH Tech. Digest*, pp. 171-174 (2006).
- [22] M. Kanamura, T. Kikkawa, N. Adachi, T. Kimura, S. Yokogawa, M. Nagahara, N. Hara, and K. Joshin, "AlGaIn/GaN power HEMTs using surface-charge-controlled structure with recessed ohmic technique," *Extended Abstracts of Int. Conf. Solid State Devices and Materials*, 2003, pp. 916-917.
- [23] Y. Uemoto et al., "Gate Injection Transistor (GIT)—A Normally-Off AlGaIn/GaN Power Transistor Using Conductivity Modulation," *IEEE Trans. Electron Devices*, Vol. 54, No. 12, 3393, 2007.
- [24] N. Ikeda, J. Li, and S. Yoshida, "Normally-off operation power AlGaIn/GaN HFET," in *Proc. Int. Symp. Power Semicond. Devices ICs*, 2004, pp. 369-372.
- [25] W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, and I. Omura, "Recessed gate structure approach toward normally off highvoltage AlGaIn/GaN HEMT for power electronics applications," *IEEE Trans. Electron Devices*, Vol. 53, No. 2, pp. 356-362, Feb. 2006.
- [26] Y. Ohmaki, M. Tanimoto, S. Akamatsu and T. Mukai, "Enhancement-Mode AlGaIn/AlN/GaN High Electron Mobility Transistor with Low On-State Resistance and High Breakdown Voltage", *Jpn. J. Appl. Phys.*, Vol. 45, No. 44 (2006)
- [27] J. Derluyn, M. Van Hove, D. Visalli, A. Lorenz, D. Marcon, P. Srivastava, K. Geens, B. Sijmus, J. Viaene, X. Kang, J. Das, F. Medjdoub, K. Cheng, S. Degroote, M. Leys, G. Borghs and M. Germain, "Low Leakage High Breakdown E-Mode GaN DHFET on Si by Selective Removal of In-Situ Grown Si₃N₄," *Proc. International Electron Device Meeting*, 2009, pp. 157-160.
- [28] C. S. Suh, Y. Dora, N. Fichtenbaum, L. McCarthy, S. Keller, and U. K. Mishra, "High-breakdown enhancement-mode AlGaIn/GaN HEMTs with integrated slant field-plate," in *IEDM Tech. Dig.*, Dec. 2006, pp. 911-913.
- [29] W. Huang, T. P. Chow, Y. Niiyama, T. Nomura, and S. Yoshida, "Lateral implanted RESURF GaN MOSFETs with BV up to 2.5 kV," in *Proc. Int. Symp. Power Semicond. Devices IC's*, May 2008, pp. 291-294.
- [30] T. Adachi, T. Deguchi, A. Nakagawa, Y. Terada, and T. Egawa, "Highperformance E-mode AlGaIn/GaN HEMTs with LT-GaN cap layer using gate recess techniques," in *Proc. Device Res. Conf.*, 2008, pp. 129-130.
- [31] R. Chu, Z. Chen, S. P. DenBaars, and U. K. Mishra, "V-gate GaN HEMTs with engineered buffer for normally off operation," *IEEE Electron Device Lett.*, vol. 29, no. 11, pp. 1184-1186, Nov. 2008.
- [32] D. Song, J. Liu, Z. Cheng, W. C. W. Tang, K. M. Lau, and K. J. Chen, "Normally off AlGaIn/GaN low-density drain HEMT (LDD-HEMT) with enhanced breakdown voltage and reduced current collapse," *IEEE Electron Device Lett.*, vol. 28, no. 3, pp. 189-191, Mar. 2007.