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in [2.379]. The polarization-doped devices with a gate length of $0.7\text{ }\mu\text{m}$ yield $f_T = 19\text{ GHz}$ and $f_{\text{max}} = 46\text{ GHz}$.

2.5.4 Metal Insulator Semiconductor Field-Effect Transistors (MISFETs)

Nitride MISFETs are very attractive candidates for improved performance of the gate diodes relative to nitride MESFETs and HEMTs with metal/semiconductor Schottky-gates. At the same time MISFETs require the mastery of the insulator/semiconductor interface. This interface affects threshold voltages and other device properties to a great extent. GaN-based MOSFETs (Metal Oxide Semiconductor FETs) have been demonstrated, e.g., in [2.191]. The comparison of the $\text{SiO}_2/\text{AlGaIn}/\text{GaN}$ MOSFETs with regular Schottky-gate HEMTs yields similar drain current densities, while the gate current density is reduced by six orders of magnitude for the MOSFET. The threshold voltage is shifted by -3 V for the MOSFET relative to the HEMT. A quarter micron $\text{SiN}/\text{AlGaIn}/\text{GaN}$ MISFET was developed as reported in [2.1]. Again the threshold voltage V_{thr} is shifted to negative values of -7 V . This MISFET further yields a high power density of 6 W mm^{-1} up to 26 GHz . The DC- and small-signal parameters of the MISFET are very similar to those of the HEMT. An overview of III-N insulating gate FETs is further provided in [2.193]. The low-leakage currents of the MISFETs found at RT are also reduced at temperatures of 300°C . Further, the MISFET concept is applied to double heterojunction $\text{AlGaIn}/\text{InGaIn}/\text{GaN}$ structures, which reduce the current collapse to a high extent [2.192, 2.426].

Power Performance of MISFETs

Several demonstrations of the power performance of III-N MISFETs are available [2.69, 2.74]. Reduced gate-leakage of MIS gate devices relative to MESFETs and consequently improved linearity at 4 GHz are demonstrated in [2.69]. The third-order intermodulation ratio of 30 dBc is reached with a power density of 1.8 W mm^{-1} and an associated PAE = 40% at 2 GHz . SiO_2 is used as the gate dielectric. The microwave performance of undoped AlGaIn/GaN MISFETs on sapphire substrates is given in [2.74]. A power density of 4.2 W mm^{-1} at 4 GHz is obtained at $V_{\text{DS}} = 28\text{ V}$, again with a very negative threshold voltage $V_{\text{thr}} = -10\text{ V}$. The extrinsic transconductance is 100 mS mm^{-1} . $\text{SiO}_2/\text{AlGaIn}/\text{InGaIn}/\text{GaN}$ MOS double heterostructure FETs (MOSDHFETs) are demonstrated in [2.192, 2.426] with the introduction of the new channel material InGaIn . The importance of the additional carrier confinement is to reduce the spillover into trapping states. A Cat-CVD Insulated AlN/GaN MISHFET is given in [2.142]. Very thin AlN layers with a thickness of 2.5 nm are used as barrier layers. On top of this barrier a 3 nm SiN layer is deposited by Cat-CVD. This layer combination allows a very small gate-to-channel separation, which is used combination with gate length

of 60 nm to achieve a cut-off frequency $f_T = 107$ GHz. The application of GaN MISFETs for low-loss switching is discussed in [2.217]. A 1 mm wide AlGaIn/GaN MOSHFET yields switching powers of 43 W with 40 dB of isolation and 0.27 dB insertion loss at 100 MHz. The SiO₂ thickness is 7 nm in this case. The very negative threshold $V_{\text{thr}} = -9$ V is achieved for the device, which yields a maximum saturated pulsed-drain current of 2 A mm^{-1} .

2.5.5 High-Electron Mobility Transistors (HEMTs)

GaN HEMTs or heterojunction FETs (HFETs) are currently the most widespread and most advanced electronic nitride devices. They make full use of heterostructures and the advantageous breakdown and transport properties of undoped GaN. A huge number of compilations of GaN HEMT data is available, e.g., in [2.39, 2.96, 2.301, 2.302, 2.463]. Initial overviews are given in [2.40, 2.312, 2.422]. Initial microwave results of AlGaIn/GaN HEMTs have been given in [2.40, 2.190, 2.506]. An overview of AlGaIn/GaN HEMT technology is provided by Keller et al. and Mishra et al. from UCSB in [2.188, 2.301]. P_{sat} An overview of the application of GaN-based HFETs for advanced wireless communication is provided in [2.341]. Recent developments and trends in GaN HFETs in Europe are given in [2.455, 2.476]; overviews of the US activities are given, e.g., in [2.361, 2.401]. This section provides a systemized data collection which is presented with emphasis on the frequency aspect and the achievements relative to the theoretical predictions. To systemize device performance, Fig. 2.16 gives a compilation of the product cut-off frequency $f_T \times l_g$ as a function of gate length l_g . A product of $12 \text{ GHz}\mu\text{m}$ is found for $l_g \geq 300 \text{ nm}$ for GaN HFETs. A GaAs reference value of $15 \text{ GHz}\mu\text{m}$ is assumed. For gate lengths smaller than 300 nm, the short-channel effects become visible for GaN HFETs. Fig. 2.17 gives a compilation of the output power per unit gate width as a function of frequency. A distinction is made between pulsed- and cw-output power. The maximum power densities reach 12 W mm^{-1} without additional measures at the gate, while output power densities $\geq 40 \text{ W mm}^{-1}$ have been reported using field plates [2.511]; however, reliability concerns prevail. Significant improvements of the output power up to 101 GHz have been reported as compared to all other semiconductor technologies [2.291, 2.378]. Similar to Fig. 2.17, Fig. 2.18 gives the absolute cw- and pulsed-output power as a function of frequency. The power levels on the transistor level reach 370 W under cw-operation conditions [2.488] at 2 GHz. Under pulsed-operation with low duty cycles, even higher output power values of up to 1 kW have been reported [2.268, 2.304, 2.503]. For low-noise operation, Fig. 2.19 gives the minimum noise figure $N_{F,\text{min}}$ as a function of frequency for both a single-recess GaAs PHEMT and a planar GaN HFET. The comparison yields promising minimum noise figure for the GaN HFET, which is slightly increased relative to the GaAs PHEMT [2.153, 2.262]. The next paragraphs systematically discuss the various frequency bands with respect to power and noise performance.

Regrown Ohmic Contacts

Apart from planar and implanted contacts, more complicated contact concepts and processes have been developed to address specific issues. Epitaxially regrown contacts can solve specific device issues, while they have the great disadvantage of loosing the natural sequence of epitaxial and subsequent technological process steps. Regrown contacts have particular advantages for the definition and protection of p-type contacts. A study to improve the current gain of AlGaIn/GaN HBTs using a regrown emitter contact is given in [4.284]. The emitter contact is selectively regrown on the base layer, which is patterned by a dielectric mask. This technique is used to overcome the Mg-memory effect during MOCVD growth, which normally causes a displacement of the base-emitter junction. The technique is further useful to avoid etch damage of the base layer during processing. The etch damage is otherwise prohibitive, especially for the thin base layers necessary to increase the current gain in AlGaIn/GaN HBTs [4.284]. A specific analysis of the p-n diodes in a comparison of regrown and conventional contacts is given in [4.282]. N-doped AlGaIn layers are selectively regrown on the p-doped GaN surfaces. A Pd/Au metal sequence is deposited on the p-type GaN. Improved ideality factors and reverse leakage currents are obtained for the pn-diodes when growth pressure, growth temperature, and the semiconductor diode layer sequence are optimized compared to the as-grown p-type GaN. Regrown n-type contacts can also be used in FETs to reduce the access resistance. Self-aligned AlGaIn/GaN HFETs with extrinsic transconductance values as high as 400 mS mm^{-1} are reported in [4.33]. They are based on a regrown ohmic contact concept for a gate length of $1.2 \mu\text{m}$. Source and drain GaN layers are grown selectively by MOCVD. A 170 nm thick Si-doped GaN layer doped at $1 \times 10^{18} \text{ cm}^{-3}$ is grown on the etched surfaces. A layer sequence of Ti (20 nm)/Al (200 nm)/Ni (40 nm)/Au (40 nm) is deposited and annealed at 830°C for 30 s . The resulting source resistances are $0.95 \Omega \text{ mm}$. AlN/GaN insulated gate heterostructure FETs with regrown n+ GaN ohmic contacts are reported in [4.122]. Four nanometer thick AlN is used as a gate insulator in this case. After selectively removing the AlN insulator, both source- and drain-contact n-type GaN layers are regrown on the GaN channel with a thickness of 150 nm . Ti/Al/Au contacts are deposited and annealed at 900°C at 30 s in N_2 atmosphere. The contact resistance achieved with the regrowth method is as low as $0.22 \Omega \text{ mm}$.

4.3.2 Schottky Contacts

Metal-semiconductor Schottky contacts are the most critical elements in all those FETs that do not have a metal-oxide contact. Schottky-contact properties define charge control [4.238] and the hot spots of the electric fields in the gate region, as depicted in Fig. 4.7. This figure gives the simulated distribution of the electric field under the gate contact in an AlGaIn/GaN HEMT, in this case with a gate length $l_g = 600 \text{ nm}$. It can be seen that the field gradients

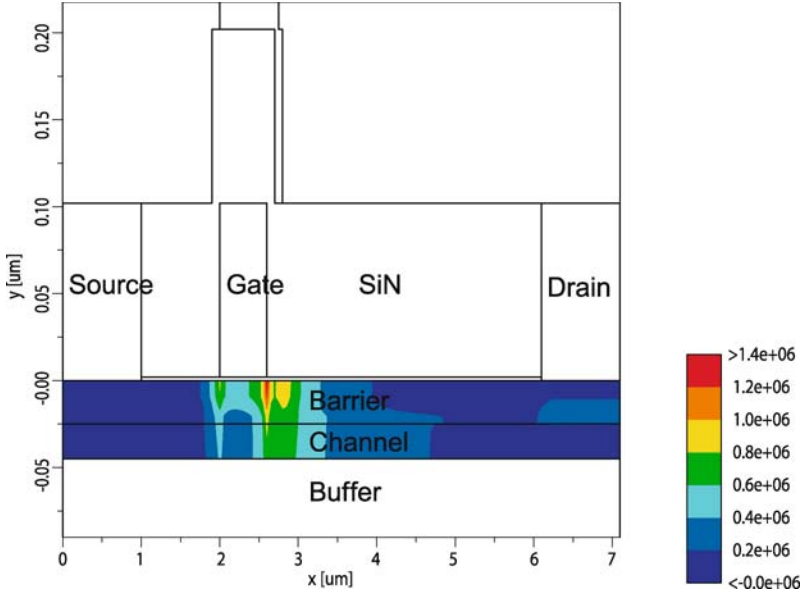


Fig. 4.7. Simulated field distribution in V/cm in an AlGaIn/GaN HFET at $V_{DS} = 60$ V

are located at the drain side end of the gate, and so a very precise gate definition is fundamental for FETs. Direct measurement of gate depletion regions has been reported. High breakdown voltages of up to 405 V in AlGaIn/GaN HFETs with simple Schottky contacts have been measured, as reported, e.g., in [4.261]. A fourth terminal is applied to the device that can be individually monitored. From this analysis the distribution of the depletion zone can be directly measured. It is found that the extension of depletion zone strongly varies with the voltage, which mitigates field peaking. It can be deduced from this analysis and from Fig. 4.7 that the impact of the surface is critical to the analysis. In a Schottky contact the forward current through a diode is considered ideal when $n = 1$, as given in (4.1) [4.78]. Nearly ideal Schottky contacts with low ideality factors n , as defined in (4.1), avoid early gain compression in FET power devices. The gate current is modeled:

$$I_G = I_0 \cdot \exp\left(\frac{q \cdot (V - I \cdot R_S)}{n \cdot k_B \cdot T_L}\right). \quad (4.1)$$

R_S denotes the series resistance of the diode and n the (non)-ideality. GaN FETs initially suffer from relatively high ideality factors n [4.114] due to various issues:

- High surface roughness affecting the morphology of the semiconductor–metal interface

- Isolation problems along the top semiconductor-passivation interface without the application of a gate or ohmic recess
- High drain-current levels through high (polarization and impurity) doping
- Nonohmic behavior of the access regions during the Schottky diode measurement

These issues are partly independent of the actual Schottky contact metal layer design and will be discussed further. The technological issues of the contact formation, however, include the following:

- The reduction of leakage currents at high-voltage operation of up to 300 V
- Stability with respect to high operation temperatures [4.110]
- The effects due to the formation of a Schottky gate on a polar semiconductor (Ga-face, N-face polarity) [4.219]
- Trapping behavior and dipole formation near the interface [4.219]
- Adhesion issues of the gate contacts on relatively rough interfaces
- The mechanical stability of the gates, e.g., with respect to the backside treatment of very hard substrate materials

Typically, the currents in a diode are modeled by a thermionic emission model:

$$I_G = A \cdot T_L^2 \cdot \exp\left(\frac{-q \cdot \phi_B}{k_B \cdot T_L}\right) \exp\left(\frac{qV}{n \cdot k_B \cdot T_L}\right). \quad (4.2)$$

Tunneling introduces an additional mechanism, as described in various publications, e.g., in [4.83]. The tunneling probability $T(E)$ is modeled in one dimension according to

$$T(E_x) = \exp\left[-2 \frac{\sqrt{2m^*}}{\hbar} \int_{x_1}^{x_2} \sqrt{\phi(x) - E_x} dx\right]. \quad (4.3)$$

Detailed leakage mechanisms at GaN- and AlGaN-Schottky interfaces are described in [4.83]. Temperature-dependent measurements between 200 and 300 K allow a separation of tunneling and thermionic effects in (4.2) and (4.3). Effective barrier thinning through unintentional surface-defect donors is found to enhance the Schottky-barrier tunneling in AlGaN/GaN HFETs and leads to increased leakage currents. The origins of leaky characteristics of Schottky diodes on p-doped GaN are discussed in [4.291]. The Mg concentration amounts to $5 \times 10^{19} \text{ cm}^{-3}$ near the interface. Au/Ni is used as metal stack. The defective surface region is considered critical for the formation of either Schottky or ohmic contacts for the same metal system. The physical background of the tunneling is the trap distribution near the interface, which enhances or suppresses the tunneling component. The influence of rapid thermal annealing on Ni/Pt/Au Schottky gates on n-doped AlGaN is described in [4.183]. Pt diffusion after annealing at the temperature of 600°C leads to improved Schottky barrier height.

Ti/Ni/Pt/Au gates do not show any significant change after a similar annealing treatment, since interfacial Ti serves as a diffusion barrier. Ni is found to be crucial for the formation of a stable Schottky interface. Similarly, the impact of thermal annealing on AlGa_N/Ni (3 nm)/Pt (30 nm)/Au (300 nm) Schottky diodes is investigated in [4.193]. The leakage current is significantly reduced after RTA. Two reasons are considered. One explanation is the Pt diffusion to the AlGa_N layer, the second explanation is the reaction of Ni with the AlGa_N surface, which reduces the surface trap density.

Very high operating temperatures are considered when Ir Schottky contacts are annealed at 500°C in O₂ ambient for 24 h [4.110]. The devices are found to be stable with respect to this temperature treatment. Thermal oxidation of diffused Ga is considered to improve the Schottky barrier ϕ_B in this case. A very high degradation temperature of 700°C is found for W and WSiN refractory contacts to n-GaN in [4.228]. Nb contacts degrade at a temperature of 300°C. However, in general, the refractory gates to GaN are found to be more leaky than those to GaAs. Surface roughness of the semiconductor layers remains an issue, especially with regard to small-gate-length devices with a gate length below 300 nm. Roughness is a serious reliability issue as reported in [4.70]. An increase of the medium scale roughness is based on the cracking of the degraded AlGa_N films. The local strain of AlGa_N relaxes. Gate adhesion is further a major issue for the realization of the gates [4.9, 4.75]. No adhesion problems have been found for both Ni/Au- and Cu-gates, as reported in [4.9]. Pure Pt gates are considered to suffer from adhesion problems on GaN and AlGa_N [4.75]. Other noble metals such as Au present similar problems [4.12].

The exposure of the gates to mechanical stress is another important issue. Additional metals on top of the gate heads introduces additional stress. Such nonuniform mechanical stress is evaluated by simulation in [4.25]. The III-N nitrides are found to be stiff, and the highest impact of stressed gate heads occurs for strongly strain-relaxed AlGa_N. Further, during backside processing [4.255], the FETs devices are subject to the stress induced by substrate thinning and thermal exposure due to viahole etching adjacent to the gates. Experimental investigations regarding the mechanical stability are currently rare.

Metal Stacks for Schottky Contacts

Various metal systems have been proposed for use in Schottky contacts on III-N semiconductors. The pretreatment of the semiconductor is discussed below. Overview articles on metal stacks are found, e.g., in [4.163]. Table 4.2 compiles the most important characteristics of a large number of metals and metal systems. The Schottky barrier ϕ_B , the doping of the semiconductor, and the extracted ideality factors n are given. Out of the selection in Table 4.2, several options have been eliminated for state-of-the-art technologies. Ni/Au

Table 4.2. Schottky barriers and ideality factors on various semiconductor materials

Material	Schottky barrier $q \cdot \phi_B$ (eV)	Doping (cm^{-3})	Ideality (–)	Ref.
Au	1.32	$4 \times 10^{17}/\text{n-GaN}$	1.24	[4.269]
Au	0.84–0.94	n-GaN	1.03	[4.78]
Cu	1.15	n-GaN	1.04	[4.9]
Ir	0.9–1.1	n-GaN	–	[4.110, 4.111, 4.113]
Mo	0.81–1.02	n-GaN	1.04–1.29	[4.208]
Nb	0.63	n-GaN	1.5	[4.228]
Ni	1.26	n- $\text{Al}_{0.15}\text{Ga}_{0.85}\text{N}$	–	[4.292]
Ni	0.71	n- $\text{Al}_{0.21}\text{Ga}_{0.79}\text{N}$	–	[4.113]
Ni/Au	0.97	n-GaN	1.05	[4.9]
Ni/Pt/Au	0.82	n-GaN	2.1	[4.193]
Pd	1.13	$\text{Al}_{0.21}\text{Ga}_{0.79}\text{N}$	–	[4.113]
Pt	1.1	$2 \times 10^{17}/\text{n-GaN}$	–	[4.238]
Pt/Ti/Au	–	n-GaN	–	[4.166]
Re	0.82	$1.5 \times 10^{17}/\text{n-GaN}$	1.1	[4.258]
Ru	1.1	–	–	[4.111]
Ti	0.58	$4 \times 10^{17}/\text{n-GaN}$	–	[4.18]
Ti	1	n- $\text{Al}_{0.15}\text{Ga}_{0.85}\text{N}$	–	[4.292]
W	0.63	n- $\text{Al}_{0.21}\text{Ga}_{0.79}\text{N}$	–	[4.113, 4.228]
WSi	0.58	n- $\text{Al}_{0.21}\text{Ga}_{0.79}\text{N}$	–	[4.113]
WSiN	Leaky	$1 \times 10^{17}/\text{n-GaN}$	–	[4.228]
Ni	2.0	p-GaN	–	[4.163]
Nb	Leaky	p-GaN	–	[4.228]
WSiN	0.8	p-GaN	–	[4.228]

is a favorite system in use. As a general trend, the Schottky barriers on AlGaN are higher than those on GaN. Nitronex reported the use of Ni/Au in [4.114]. Cree has also mentioned the use of Ni/Au in [4.275, 4.277]. Fujitsu/Eudyna and NEC [4.8] have reported on the use of Ni/Au in [4.118] for both HEMTs and MIS-HEMTs. RFMD also reported the use of Ni/Au in [4.221, 4.222]. Triquint reported the use of Pt/Au for high-power e-beam defined field-plate gates in [4.53, 4.153]. Other gate-stack options, such as Ir or W may be useful especially for high-temperature operation.

Cleaning and Pretreatment of the Gated Surface

Surface cleaning prior to metal deposition plays an important role for the yield and the homogeneity of the process, e.g., [4.114]. After opening the protecting SiN passivation layers [4.114] or resist layers prior to gate deposition, the

remainders on the semiconductor surface have to be fully removed to increase process robustness. At the same time, etch-damage has to be avoided. Opening the SiN dielectric involves plasma dry etching, as proposed, e.g., in [4.245]. This procedure has to be optimized for low-semiconductor damage, as performed in [4.114]. ICP-RIE is used for this procedure, as plasma density and ion energy can be effectively decoupled and damage can be reduced. Thus, sufficient etch rates can be achieved without the use of high DC-substrate bias.

Resist and oxide removal is another critical step before gate formation. A wet NH_4OH treatment in 1:10 volume is applied in [4.183] to remove native oxides. A similar oxygen plasma followed by a 1:10 $\text{NH}_4\text{OH}/\text{H}_2\text{O}$ treatment for 15 s is suggested in [4.238]. An O_2 -plasma-ashing in combination with diluted $\text{HCl}:\text{H}_2\text{O}$ (ratio 1:1) treatment is used in [4.9] for the same purpose. The same HCl treatment is mentioned in [4.258]. Surface oxide removal by aqua regia ($\text{HNO}_3:\text{HCl}=1:3$) is suggested in [4.208]. The impact of a short HCl dip prior to gate–metal deposition is studied in [4.141]. A trade-off is found achieving either low-leakage and stronger current collapse or increased leakage and negligible current collapse. The trade-off is attributed to the existence of a thin interfacial oxide layer under the gate, which is partly or fully removed by the HCl etch. Residual oxide leads to reduced leakage but increased dispersion in the general trade-off between leakage and dispersion. The design of the gate head is discussed in the following section.

Device Annealing

Rapid thermal annealing is a crucial procedure for the formation of ohmic contacts, as has already been reported. Further, annealing can be instrumental in removing the etch damage, e.g., [4.204]. In addition, annealing can be effectively used to stabilize devices during or after processing with respect to long-term reliability [4.99]. A study of the post-annealing effects on the $\text{AlGaIn}/\text{GaIn}$ HEMT performance after gate formation is given in [4.130]. The annealing is performed at 400°C for 10 min in N_2 atmosphere. The annealing is reported to reduce the number of surface defects with a time constant of $\leq 10\ \mu\text{s}$, resulting in a reduction of low-frequency dispersion observed by pulsed-DC-measurements with different time constants. Further annealing leads to the creation of traps with a time constant of $\geq 10\ \mu\text{s}$. Furthermore, the annealing of gate contacts has a large impact on the threshold voltage, as reported, e.g., in [4.59]. A device annealing is performed at 500°C and leads to a substantial change of the barrier height and the leakage currents. Similarly, gate annealing procedures have been developed to stabilize the gate process. Gate annealing in nitrogen atmosphere at 600°C for 5 min is reported in [4.193].

Gas Sensitivity

Any metal–semiconductor contact has a sensitivity to gases present at the metal–semiconductor interfaces. This sensitivity is based on the adsorption of

the gases and the resulting modification of the space charge zone under the gate. This can possibly be exploited at extremely high operating temperatures $\geq 300^\circ\text{C}$ due to the WBG properties of III-N semiconductors.

The hydrogen response of Pt-GaN Schottky diodes is investigated in [4.219] and in [4.132]. Hydrogen is found to dissociate on the Pt surface forming atomic hydrogen, which modifies the effective barrier height. Similar investigations of the hydrogen sensitivity of Pd/GaN diodes are reported in [4.271] and in [4.132]. The forward and reverse currents are significantly changed by the Schottky barrier reduction in the presence of hydrogen. The devices can be operated up to temperatures of 473 K. The changes of the effective Schottky barrier height in an atmosphere with 10% H_2 are typically in the order of 50 meV. Hydrogen-induced reversible changes in the drain current of $\text{Sc}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ MOS-HEMTs are discussed in [4.119]. The gas-induced effect is based on the dissociation of the molecular hydrogen at the Pt contact, followed by the diffusion of the atomic hydrogen to the oxide/semiconductor ($\text{Sc}_2\text{O}_3/\text{AlGaIn}$) interfaces, where the channel charge is modified, as already mentioned above.

4.4 Lithography

Lithography is a fundamental processing step for any semiconductor device. Optical lithography has been reported on for the formation of ohmic and gate contacts and further layers of III-N devices in [4.98, 4.166, 4.223]. Electron-beam gate lithography [4.263] has been used in the III-N material system for the gate formation of GaN FETs with gate lengths $\leq 300\text{ nm}$. Minimum physical gate lengths $l_g = 30\text{ nm}$ have been reported [4.93]. Even direct contact lithography is still used, mainly for contact definition, especially for 2-in. substrate diameter technologies, e.g., in combination with electron lithography [4.16, 4.126].

4.4.1 Optical Lithography

Optical stepper lithography provides parallel illumination of the wafer and thus provides a fast and thus cost effective lithography for mass production [4.61]. With the development in the silicon VLSI industry, optical gates down to physical lengths of 25 nm are being realized with UV [4.106, 4.187] and potentially with EUV optical stepper technology [4.232]. In the III-V semiconductor industry, the optical steppers used are typically i-line type and are based on 248 nm wavelength technology [4.61, 4.114]. Gate lengths down to at least 250 nm are typically realized, and the gate length can be decreased even to 150 nm, when phase shift masks are applied, e.g., [4.164]. The gate definition of GaAs and GaN FETs can be subdivided into the fundamental steps [4.61, 4.114]:

tures of 100K than at RT, and the pulsed-DC-measurements provide similar characteristics. The paper further suggests the existence of a hole contribution to the gate current at low temperatures. We can deduce from these findings that trapping is persistent at both surface and in the bulk and that their impact on the three-terminal characteristics of AlGaIn/GaN HFETs is consistent with findings in GaAs devices. However, the relative impact is more pronounced than is known in the GaAs world.

The Impact of the Initial State of the Device

When freshly processed devices are analyzed, the initial measurements often differ from a stable device status, if such status exists at all. A burn-in behavior is observed, which is partly, but not exclusively, attributed to the trapping effects, related current collapse, and reliability issues. Output characteristics, e.g., in [4.285], show a degradation when the device is measured repeatedly. As burn-in effect have also been observed for several other devices, e.g., InP HEMTs [4.35], the variation of the device properties is found to stop after a burn-in procedure [4.227] for optimized devices.

4.6.4 Technological Measures: Surface Preparation and Dielectrics

A minimum of surface treatment before and during passivation is necessary and unavoidable in any device processing. As a general finding, SiN- or other material-passivation greatly enhance the power performance of AlGaIn/GaN devices, e.g., in [4.17, 4.20, 4.72, 4.117, 4.241, 4.246]. The effect on leakage current and dispersion, however, has to be treated in detail, e.g., [4.242].

Surface Preparation

During device fabrication, surface treatment, and cleaning conditions are very important and at the same time unavoidable, as discussed, e.g., in [4.57, 4.171]. Because of the polar nature of the III-N semiconductor materials, the status of the epitaxial surface is critical when the wafers are removed from the growth reactor. The wafer is thus exposed to air prior to further processing and device passivation. The exposure typically leads to an initial oxidation. Early passivation techniques within the process flow have been considered relevant in [4.114, 4.117], since the exposure of the semiconductor surface to air and any kind of processing medium is found to be critical, as also known from GaAs processes [4.61, 4.262]. Typical related process steps in the context of device passivation are ohmic contact formation, annealing, device isolation, and gate recess definition. As an alternative to early SiN ex-situ passivation, in-situ passivation in the growth reactor has also been suggested in [4.104] in order to avoid surface contamination by ambients. This agrees with findings in [4.10] that both the GaN and AlGaIn surfaces are found to be highly corrosive when exposed to air or other ambients. This corrosion potentially requires the application of cleaning techniques.

Cleaning Procedures and Pretreatment

Given the sensitivity to any exposure, surface and interface cleaning procedures are vital for the reduction of surface states and dispersion, e.g., [4.178]. An improved fabrication process for obtaining high-power density AlGaIn/GaN HEMTs has been suggested in [4.244]. The exposure of the critical ungated surface through harmful plasmas and chemical treatments is completely avoided. For other process variants various surface cleaning procedures have been proposed for the reduction or compensation of surface states, e.g., in [4.72, 4.178]. Before PECVD deposition, the surface in [4.72] is cleaned (in this order) by acetone, methanol, isopropanol, and water. The surface is then dipped in 30:1 buffered oxide-etch for 30 s. No significant changes in device characteristics are seen after these wet cleaning and etch steps. Several other treatments are reported. The surface treatment by a combined HCl:HF:H₂O (1:1:2) and subsequent HF-buffered oxide-etch (14%) for 10 s in [4.49] is found to exert little influence on the carrier distribution and mobility. This and similar findings point to the existence of stable surface oxides, which can only be removed or modified by very aggressive techniques. The passivation in [4.49] is SiO₂. The effect of the pretreatment on pulsed-measurements is not reported. Subsequent deposition of the passivation, however, leads to a strong increase in channel-carrier concentration and reduced mobility. NH₃ low-power plasma pretreatment prior to SiN PECVD-based passivation is described in [4.57]. The NH₃ pretreatment is performed with the substrate held at 250°C. The gate-lag ratio observed during pulsed-operation and the output power degradation for long-term RF-operation can be significantly reduced. The increased device reliability is attributed to both the strengthening of the bonds at the interface and the incorporation of hydrogen, which passivates defects. A similar NH₃ treatment is reported in [4.117]. Dry plasma pretreatments are discussed in [4.178]. Plasmas based on SF₆, O₂, N₂O, NH₃, and N₂ are applied. Contrary to wet pretreatment NH₃-, N₂-, and combined NH₃/N₂-pretreatment delivers very strong changes and mitigates the drain-lag. The X-ray photoelectron spectroscopy (XPS) measurements reveal a correlation of the reduction of the carbon concentration on the AlGaIn surface with the degree of the mitigation of the drain-lag. Carbon contamination of the surface in AlGaIn/GaN HFETs can be mitigated by an air plasma descum and subsequent HCl dip prior to SiN deposition [4.14]. Auger spectroscopy reveals a correlation of the current collapse with the residual carbon contamination. The sensitivity of the breakdown voltage and related gate leakage and surface carrier concentrations to plasma damage in the AlGaIn barrier is discussed in [4.216]. A surface-charge defect model is applied. Simulations show that a significant reduction of the surface charge to levels of $1 \times 10^{12} \text{ cm}^{-2}$ is necessary in order to reach suitable gate currents at voltages >100 V, even when a field-plate concept is applied.

Surface treatment of III-N semiconductors is especially important for p-type material. Hydrogen is typically incorporated strongly into the material

during MOCVD growth, thus the layers are specifically sensitive to surface treatment. Hydrogen plasma treatment of p-type GaN is investigated using both hydrogen and deuterium to enable secondary ion mass spectroscopy (SIMS) investigations of the hydrogen effect [4.206]. Hydrogen plasma treatment leads to a strong hydrogen passivation of carriers in the p-type GaN. This is further confirmed by the analysis of the traps at 0.3 and 0.6 eV. Capacitance vs. frequency $C(f)$ -measurements confirm the impact of the plasma treatment on the p-type doping-activation and the suppression of the trapping. At the same time, additional trapping at 0.4 eV is created. Based on these results, the deposition of dielectric material is now analyzed.

The Deposition of Dielectrics: Passivation

The deposition of dielectrics at the semiconductor/vacuum interface yields a large number of possibilities. With the application of optimized interface passivation, the interface neutralizes the net surface charge, as given in Fig. 4.16, in both static and dynamic sense. The net surface charge arises from a polarized GaN cap or AlGaIn barrier and from the residual surface states resulting from dangling bonds, absorbed ions, or charge surface residual materials (e.g., oxides [4.10]).

Silicon Nitrides (Si_3N_4)

Silicon nitride is the most popular dielectric for the III-N material system, e.g., [4.17, 4.68, 4.114, 4.128, 4.139, 4.151, 4.246]. Typical effects of the passivation by SiN on III-N devices include the increase of the output power [4.246], reduction of frequency dispersive effects [4.72], and the modification of leakage currents [4.17, 4.242], often leading to a reduction of the breakdown voltages. Further long-term device reliability is positively affected [4.151]. Various methods and recipes exist for the deposition of SiN in its various modifications, e.g.,

- Plasma-enhanced chemical vapor deposition (PECVD) [4.57, 4.68, 4.241, 4.242, 4.246] for low damage deposition with low hydrogen content, including:
 - ECR-PECVD
 - ICP-PECVD [4.57]
- Catalytic chemical vapor deposition (CAT-CVD) [4.89, 4.90, 4.151]
- Others, such as epitaxial in-situ deposition [4.207].

The variations of PECVD deposition typically include the silane and ammonia flows [4.72], the deposition temperature [4.242], deposition pressure, deposition RF-power, and thickness [4.231]. The corresponding detailed engineering is discussed below.

Stress and Stress Engineering

Deposited SiN is an amorphous material that can be influenced in variety of ways. The actual deposition can be adjusted with respect to strain and stress on the underlying material. Stress ranges of the SiN_x on the semiconductor amount to 100–2,000 MPa, as reported, e.g., in [4.79, 4.293]. For SiN deposited by PECVD on AlGaIn/GaN HEMTs, several growth conditions are analyzed in [4.246]. The deposition temperature range amounts to 150–300°C. The SiN, grown under NH_3 -rich and higher temperatures conditions, gives the best power performance of the devices. The SiN is further characterized by the etch rate in buffered oxide etch. Nitrides with the lowest etch rate provide the best power densities in the III-N HFETs. A specific stress analysis of the SiN deposited by PECVD is reported in [4.241]. Dual frequency plasma deposition is used. Initial data suggests a strong impact of the induced stress. However, it is found that the surface damage through N-ion bombardment has a very strong influence on the surface, the carrier concentration, and the mobility. When this damage is avoided by a He precursor treatment and thus separated in the analysis, it is found that a uniform compressive stress on the surface has only a minimum impact on the polarization charges. The stress range amounts to –100 to 40 MPa meaning that the nitride is nearly stress-free. The mitigation of both leakage currents and current collapse by low-stress SiN_x with high refractive index is suggested in [4.116]. The in-situ CVD deposition of SiN in an MOCVD reactor is described in [4.39, 4.207]. The deposition occurs at 980°C using disilane and ammonia at a growth rate of 0.1 Å s^{-1} . The thickness of the deposited SiN amounts to 4 nm. Stress data is not provided although a very high strain of the initial SiN layers can be expected.

Temperature and Thickness of the Deposition

The SiN layer can be either composed of one or of several layers. The thickness of the initial and the subsequent passivation layers critically affects the stress and the permeability for ambients on the semiconductor layers. A PECVD-passivation of 350 nm thickness is reported in [4.72] based on silane (SiH_4) and ammonia (NH_3). The deposition is performed at 300°C after a dip in 30:1 buffered oxide etch for 30 s. The deposition leads to a significant increase in the RF-device output power. A more complete study of the various Si_3N_4 -deposition parameters is given in [4.246]. Deposition SiN-thickness, RF-deposition power, and temperatures are investigated with respect to their impact on breakdown and RF-power. The thickness of the first SiN varies between 47 and 275 nm. An optimum for the RF-output power of the AlGaIn/GaN HFET is achieved for a SiN thickness of 155 nm and a high deposition temperature of 300 °C, while the breakdown voltage is not critically affected by the SiN parameter variation. The increase in RF-output power is due to the increase in drain current.

The thickness of the PECVD-SiN determined by ellipsometry is 74–80 nm [4.57] deposited at a base plate temperature of 250°C. A $\text{SiH}_4:\text{NH}_3:\text{N}_2$ plasma recipe is used, which yields a refractive index of 2.03–2.09. The ICP RF-power is 35 W at 13.56 MHz. The crucial parameter is this investigation is not power performance but output power degradation and pulsed-DC-data after aging. The impact of hydrogen for the passivation of defects is discussed to lead to better stability.

The industrial process in [4.114] uses a 90 nm-thick SiN layer deposited by PECVD at 300°C and a pressure of 900 mTorr. After early passivation, this SiN layer is opened by an inductively coupled plasma (ICP)-etch for further processing. In combination with a low-damage ICP etch a very good device efficiency of 65% and output power density of 11 W mm^{-1} at 2 GHz are achieved. Further the thickness uniformity is of the order of 0.6%.

GaN HEMTs with SiN passivation deposited by catalytic chemical vapor deposition (Cat-CVD) are given in [4.89, 4.117, 4.151]. For the Cat-CVD deposited SiN in [4.151] the thickness is 50 nm after NH_3 pretreatment. The process was similarly developed for GaAs PHEMTs [4.86]. The Cat-CVD procedure with a NH_3 pretreatment provides the elimination of deposition plasma damage and thus reduces defect density at the interface. The output power degradation is 0.4 dB after 200 h of operation. For a similar Cat-CVD process, the deposition temperature is 250–300°C for a SiN thickness of 30 nm [4.90].

Based on these examples on the critical parameters strain, deposition-temperature, and -thickness the reliability aspect of SiN deposition is now discussed in more detail.

High-Field Effects in SiN

Similar to the semiconductor materials, the passivation materials and their interfaces are subject to high-field peaking and subsequent degradation effects. Further, the field distribution in the semiconductor and along the interfaces are critically affected by the SiN deposition so that the impact on reliability is strong. The typical degradation of AlGaIn/GaN HEMTs with a degradation of I_{DSS} as a function of time can be compared to the degradation of the current in silicon CMOS devices, e.g., [4.34]. Shifts in the threshold voltage can be fully dominated by interface trap creation at increased bias. Thus, similar measures are required for the mitigation in III-N (H)FETs. The effect of the biasing to SiN-passivated AlGaIn/GaN HEMT stressed at $V_{\text{DS}} = 17 \text{ V}$ and I_{DS} at $V_{\text{GS}} = 0 \text{ V}$ for only 1 h is strong. The PECVD deposition is performed at 300°C. The aging leads to a significant decrease in the transconductance g_{m} , a reduction of the saturated drain current I_{DS} , and a positive shift of the threshold voltage by at least 0.5 V [4.215]. The $1/f$ -noise measurements after aging reveal a significant increase of the spectral noise density after aging. These results suggest both hot electron trapping and surface-state creation during device stress.

Possible effects of SiN passivation and high-electric field on short-term AlGaIn/GaN HFET degradation are discussed in [4.131]. For a hot pinch-off

stress ($V_{DS} = 20\text{ V}$, $V_{GS} = -8\text{ V}$) for 12 h, the unpassivated device shows a degradation of the saturated current of -37% . SiN passivation reduces the degradation; however, it cannot suppress it completely (-16%). The degradation is again attributed to hot electron trapping to surface states, which can be partially mitigated by the passivation. The modification of the gate lag before and after electric-field stress suggests a modification of the surface trap profiles. A similar investigation, again supported by optical response measurements, is reported in [4.184]. The current collapse can be suppressed by light illumination with energy smaller than the bandgap. The collapse is again attributed to the surface states localized in the gate-to-drain spacing rather than the gate-to-source spacing. In general, the deposition of the appropriate passivation is a key for the realization of reliable devices.

Oxide Passivation of the Ungated Interface

Oxide, e.g., SiO₂ passivation is suggested as an alternative to Si₃N₄ passivation for use in III-N HFETs. Various investigations exist to determine the different surface conditions modified by bias in MIS- and regular Schottky-gate structures, e.g., [4.10, 4.65, 4.85]. This paragraph concentrates on the passivation of the ungated regions while gate dielectrics are discussed below.

A comparison of SiO₂ and Si₃N₄ passivation on AlGaIn/GaN HEMTs on silicon substrates is given in [4.17]. Both passivation layers are deposited by PECVD at 150°C (for SiO₂) and 300°C (for Si₃N₄). A higher surface trap density is considered to be responsible for the reduced power performance of the HEMTs with SiO₂ passivation. CV-investigations in MIS structures are reported in [4.10] for nitrided Ga₂O₃/SiO₂ films. The SiO₂ passivation is formed by remote O₂/He-based plasma using SiH₄ at 0.3 Torr. The SiO₂ films are deposited by remote PECVD. These improved oxide films provide a reduced density of interface states on n-GaN compared to Si₃N₄ on n-GaN. Effects of annealing on GaN–SiO₂-insulator MIM-interfaces is described in [4.174]. The deposition of the dielectric on n-type GaN is performed by low-pressure CVD (LPCVD) at 900°C using disilane and ammonia. The n-GaN is cleaned with H₂SO₄:H₂O₂ at 70°C. A very low surface charge of $3 \times 10^{11}\text{ cm}^{-2}$ is found. This density increases after annealing at 1,100°C. The growth of MgO- and Sc-based oxides for their use in AlGaIn/GaN HEMTs is described in [4.67]. MgO is found to produce lower interface state densities than Sc₂O₃. However, as a passivation material MgO is found to be degrading stronger than Sc₂O₃ in the annealing steps, which follow the actual passivation procedure. The application of oxides as gate dielectrics in MOSFETs is further discussed below.

Unconventional Dielectric Materials

A great number of more unconventional materials have been investigated for the passivation of III-N devices. They include polyimide (e.g., in [4.79]), low-k Bencocyclobutene (BCB) material passivation (e.g., in [4.267]), and insulators

such as AlN [4.285]. A 4:1 polyimide-to-thinner mixture is spun on the surface of AlGaIn/GaN HEMTs and cured at 300°C [4.79]. The effect of polyimide on the surface is attributed to the reduction in surface states and to the low stress of the polyimide on the surface and the nonoccurrence of plasma damage during deposition. The stress considered is lower than 70 MPa. This is an order of magnitude lower than in typical SiN films. Low-k BCB passivation of AlGaIn/GaN HEMTs is described in [4.267]. The thickness of the BCB amounts to 400 nm and is compared to a relatively thick Si₃N₄ layer of 300 nm. The inherent advantage of the BCB material is the reduced dielectric constant, the simple deposition, and the lack of deposition damage. The pulsed-DC-characteristics and the RF-output-power-results of BCB-passivated devices are similar to those with Si₃N₄ passivation. The physical nature of the stabilization of the semiconductor surface is not investigated in detail; however, it is found that the degradation of the transconductance and the drain current at 85°C is smaller than that for Si₃N₄.

The use of insulating materials of the III-N system is another option for surface deposition and, consequently, passivation. The growth of insulating AlN layers for the passivation of AlGaIn/GaN HFETs by migration-enhanced epitaxy (MEE) is described in [4.104]. The growth temperature is 150°C with a growth rate of 800 Å h⁻¹. The total AlN thickness is 1,000 Å. AlN has the advantage of high thermal conductivity directly near the heat source. The physical nature of the AlN passivation is attributed to the hardness of the material, which reduces gate-bias-induced stress on the material, as explained in [4.230]. Surface passivation using AlN deposited by reactive magnetron sputtering on both MISFETs and HFETs is described in [4.285]. The thickness of the AlN passivation is 50 nm and it is deposited at a very high processing temperature of 880°C. The AlN passivation reduces both gate leakage and current collapse. Further, the repeatability of the DC measurements is improved for the AlN passivation.

The successful application of unconventional dielectric materials supports the idea that surface preparation prior to deposition has a similar impact on the device performance to that of the actual deposition of the dielectric.

4.6.5 Epitaxial Measures: Surface Preparation and Dielectrics

Being part of the growth process, epitaxial measures are very attractive for solving the issue of dispersion reproducibly already during the growth process. This is especially important for achieving reliability for high-voltage operation [4.127, 4.225]. Typical epitaxial measures involve the introduction of the following

- A highly or medium-n-doped cap [4.128] for high-power transistors without surface passivation [4.225]
- p-Capped GaN/AlGaIn/GaN HEMTs [4.47, 4.48]
- AlN as a passivation material [4.104, 4.285]