

700V Lateral DMOS with New Source Fingertip Design

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Abstract—For decades of years, the most advanced commercial LDMOS was made by double RESURF technique using p-type field shaping layer until dual current path LDMOS which has triple RESURF structure. The specific on resistance of LDMOS was reduced to about 60% comparing to conventional LDMOS by using buried p-type field shaping layer which make it possible to get triple RESURF structure for LDMOS. The crucial point to get low specific on resistance of LDMOS is also source fingertip design because large source radius to avoid electric field concentration causes poor specific on-resistance characteristics. This paper presents high voltage LDMOS with two types of RESURF structure which has different charge balances to get lower specific on-resistance and high sustaining voltage at the same time.

I. INTRODUCTION

700V lateral double-diffused MOS (LDMOS) is used for high voltage integrated circuit (HVIC) products such as power switch and RESURF (REduced SURface Field) structure is essential for LDMOS to get low specific on-resistance while maintaining high sustaining voltage [1]-[5]. This RESURF technique has been developed and the on resistance of LDMOS has been reduced by using buried field shaping layer with two current flow paths along drift region [6]. In addition, the LDMOS should have a high breakdown voltage to endure a high voltage and simultaneously have a low on-resistance such that the LDMOS can maintain high switching characteristics. In a high-voltage semiconductor device, the curvature radius of a source or drain region has a close relation with the breakdown voltage characteristic of a device. Particularly, in some LDMOS transistors, the electric field is typically high at the tip portion of a source region having a relatively small curvature radius, which can result in reduced breakdown voltage. Fig.1 shows simulated breakdown characteristics as curvature radius (r , r' and r'') of source fingertip radius in conventional power LDMOS. As such, as the radius of the source fingertip is reduced, the electric field concentration increases at the source fingertip. The results show that with larger fingertip radius, breakdown voltage increases. The electric field concentration rate of source fingertip depends on curvature radius of it in power LDMOS. Accordingly, to achieve high voltage, the LDMOS must have enough curvature radius of source fingertip to avoid electric field concentration there. As a result, it is difficult to scale down the overall size of the LDMOS, and so fingertip design

is very important to get high breakdown voltage in power LDMOS.

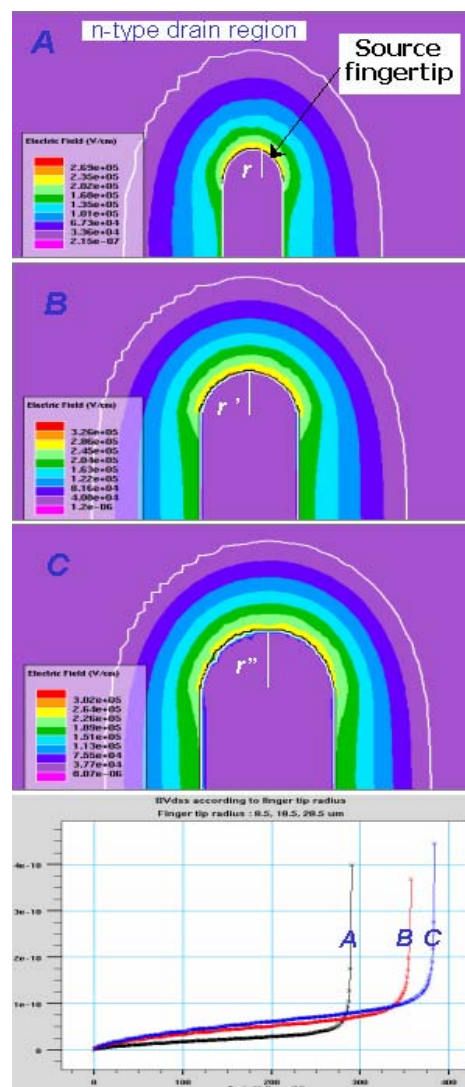


Fig.1 Simulation results according to curvature radius of source fingertip

In order to overcome this problem, the proposed LDMOS has adopted two different types of RESURF structure using buried field shaping layer at source fingertip and active area respectively. This new source fingertip design has small fingertip curvature radius, which results in LDMOS space saving and high breakdown voltage.

II. PROPOSED SOURCE FINGERTIP DESIGN AND SIMULATION

In the previous work, we proposed the structure as shown in Fig.2 in order to avoid concentration of electric field near the source fingertip [7]. Fig.2 shows schematic surface view and its cross-section at source fingertip, which not to be affected by the radius of source fingertip because n-type well is separated to each other and electrically connected by metal layout, so there is no n-type well to cause the electric field concentration around the source fingertip as seen the cut line of Fig.2. However, this structure cannot operate channel area at this area because there is no drain extension between the source and the drain by removing n-type drift region. The channel area does exist in the areas between the source and the drain where they are parallel to one another. As a result, about 7% channel area loss occurred at power LDMOS. Furthermore, this structure has disadvantage in reliability because of body-drain diode area reduction. The other work proposed small source fingertip structure that n-type drift region was removed partially [8]. The electric field concentration is reduced around the tip by eliminating the n-well layer near only source-drain fingertip.

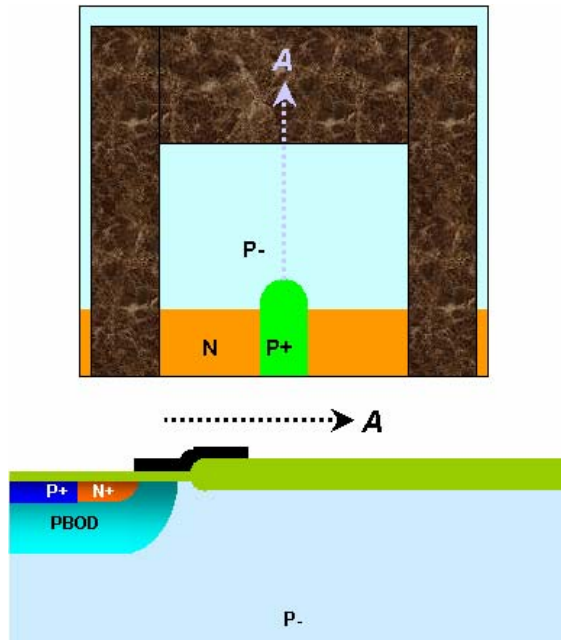


Fig.2 Schematic surface view and its cross-section of source fingertip of previous work

On the other hand, as explained earlier, we proposed small source fingertip design enabling high breakdown voltage without channel density reduction around the drain pad. Fig.3 shows schematic surface view of the proposed source fingertip region, its cross-section along A'-A and B'-B directions, respectively. As shown in these figures, In order to embody the high voltage LDMOS, the source fingertip was designed as fan-shaped pattern, which consists of slightly doped n-type well and buried p-type junctions without removing of n-type drift well around the drain pad, and buried p-type regions are arranged in the slightly doped n-type well to be spaced apart from one another along an outer circumferential surface of source fingertip. At this source fingertip region, electric field concentration is determined by the combination of slightly doped n-type well and buried p-type field shaping layers. N-type and p-type charges are well balanced in the parallel active channel area but at the source fingertip, p-type charges are more than n-type ones to enforce space charge depletion toward drain. As a result, the power LDMOS with small radius fingertip has smaller size than a comparable device with the same breakdown voltage characteristics.

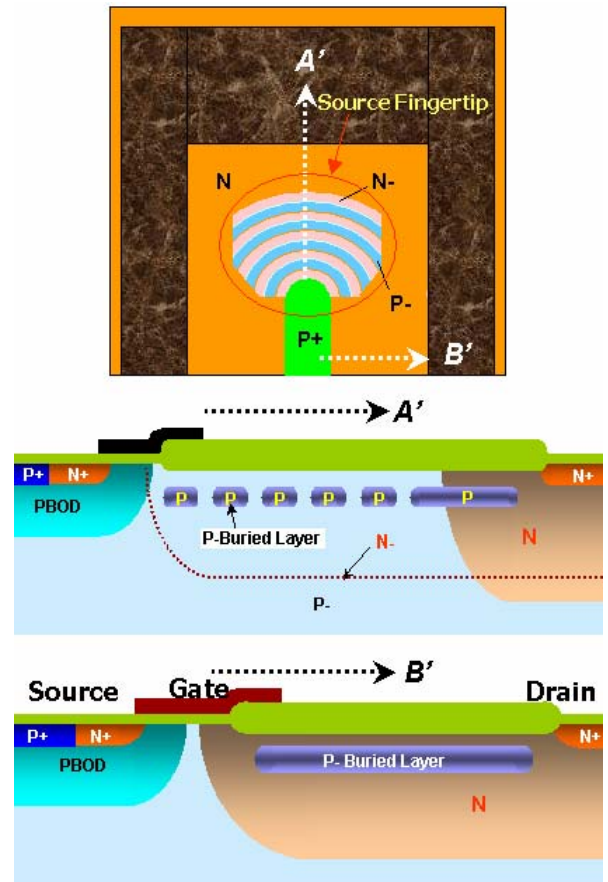


Fig.3 Schematic surface view and its cross-sections of the proposed source fingertip for this work

In the first place, we performed two-dimensional device simulations on the parallel channel area (fig.3 B'-direction) to optimize the critical process conditions and the device design

parameters in advance of the source fingertip design in the overall LDMOS structure. First of all, in order to achieve a breakdown voltage of over 700V, it is important to control doping concentrations and junction depths of etch layer such as p-type buried, n-type well and so on. Fig.4 shows various breakdown voltage values as a function of p-type buried implant dose according to change of n-type drift well dose at a proper design rules. As shown in fig.4, we could confirm to get a breakdown voltage of over 800V in a certain implant dose of p-type buried and n-type well. Fig.5 shows simulated depletion layer, potential contours and impact ionization rate when breakdown occurred at reverse bias of 811V. The potential contours are almost uniformly distributed between source and drain at the parallel channel area of LDMOS (fig.3 B'-direction). It results from that n-type and p-type charges are well balanced in the appropriate source to drain distance.

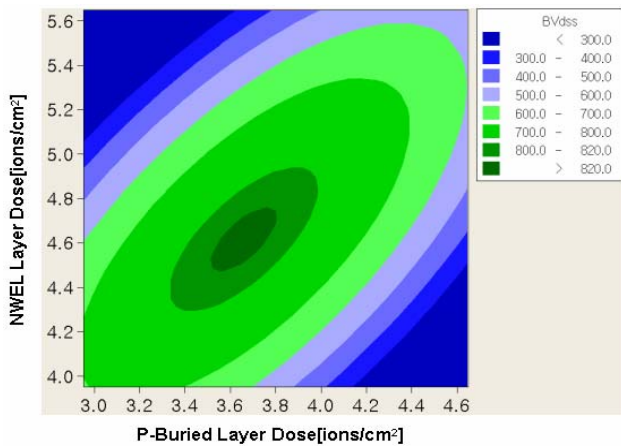


Fig.4 Simulated breakdown voltage of fig.3 B'-direction

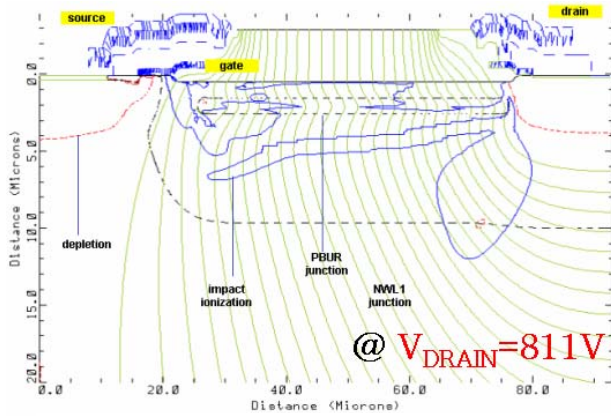


Fig.5 Simulated potential contour and impact ionization of fig.3 B'-direction

We performed also two-dimensional device simulation to optimize the proposed source fingertip from the results of simulation for the active channel region. Fig.6 shows depletion layer and potential contours of optimized source fingertip when breakdown occurred. We can see that the proposed fingertip is fully depleted and has uniform potential distribution, which reduces electric field concentration by the

balance of slightly doped n-type well and p-type buried regions with suitable space. This fingertip structure has higher breakdown voltage of 894V than breakdown voltage of active channel region, which avoids the breakdown at source fingertip of LDMOS.

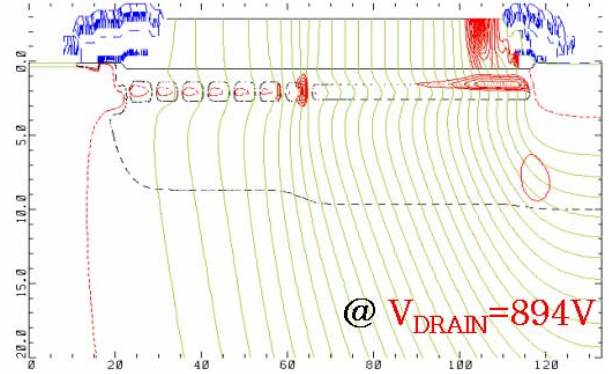


Fig.6 Simulated potential contour and impact ionization of fig.3 A'-direction for the proposed source fingertip

III. DEVICE FABRICATION

In order to fabricate the 700V LDMOS with the proposed source fingertip, we used high resistivity p-type substrate without EPI layer. As shown in simulation results above, the main processes are formation of slightly doped n-type well, n-type drift well and p-type buried that make source fingertip and drift region of the LDMOS. To begin with, slightly doped and n-type drift well are formed by implant and high temperature diffusion, followed p-type buried regions by high energy implant in the n-type wells after LOCOS process in order to define active areas. In the n-type well and p-type buried process steps, we performed implant of various dose to find optimal charge balance condition for the high breakdown and the low on-resistance. The other process steps follow conventional HVIC process including CMOS, bipolar and passive devices.

IV. EXPERIMENTAL RESULTS

Fig.7 shows fabricated actual top view of 700V LDMOS with the proposed source fingertip design for experimental evaluations. As expected, the experimental showed 700V LDMOS of best-in-class in electrical characteristics performance.

Fig.8 (a) and Fig.8 (b) show the variation of breakdown voltage and on-resistance values as a function of the p-type buried implant dose for four different n-type drift well dose conditions from experimental results on the test structure. As shown in fig.8 (a), for any given n-type drift well dose, we can see that the breakdown voltage has bell-shaped curve with a peak of over 750V breakdown voltage related to p-type buried dose variation. Furthermore, in variation of the on-resistance of fig.8 (b), as p-type buried dose decreases and n-type drift well increases, on-resistance decreases cause to drift resistance change between source and drain of the LDMOS. Therefore, we selected appropriate p-type buried and n-type drift dose to

embody high performance LDMOS by considering sensitivity of breakdown and on-resistance.

Finally, our buried p-type RESURF LDMOS with the new source fingertip guarantees breakdown voltage of more than 750V and specific on-resistance of 150 mohm.cm² which is about 60% of traditional LDMOS for HVIC products. Fig.9 (a) and (b) show breakdown and I-V curves of optimized LDMOS with the new source fingertip design to obtain breakdown voltage of over 750V. This LDMOS has hard breakdown characteristics without leakage current. Fig.10 shows measurement plot for dynamic on-resistance extraction.

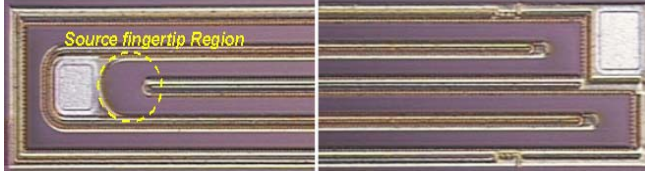
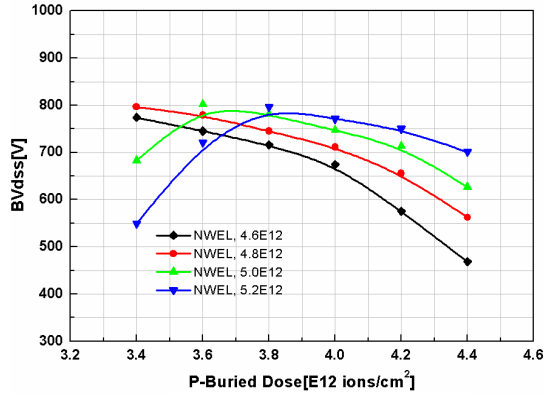
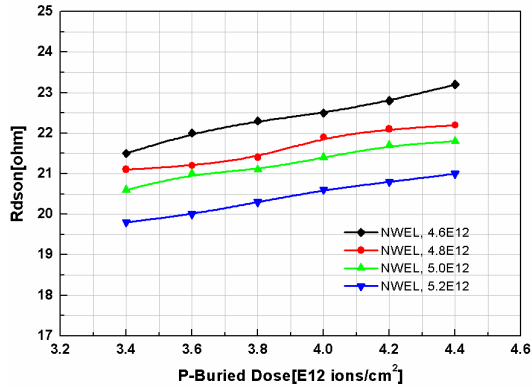


Fig.7 Actual LDMOS top view for experimental evaluations



(a) Breakdown voltage



(b) On-resistance

Fig.8 Measured breakdown voltage and on-resistance values as a function of the p-type buried implant dose for four different n-type drift dose conditions

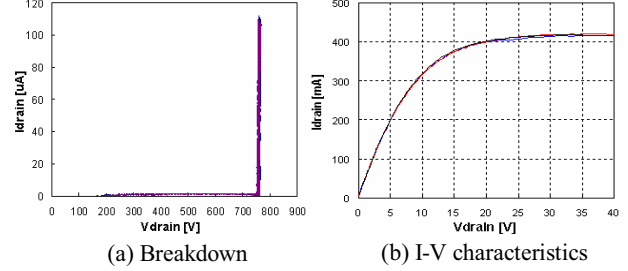


Fig.9 Measured breakdown and I-V curves

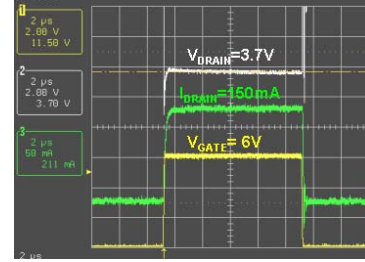


Fig.10 Measured dynamic on-resistance measurement plot

V. CONCLUSIONS

We proposed 700V buried p-type RESURF LDMOS with new source fingertip that has smaller in size than a comparable device with the same breakdown voltage characteristics. The proposed LDMOS has adopted two different types of RESURF structure at source fingertip and active channel area respectively. At this source fingertip region, electric field concentration is determined by the combination of slightly doped n-type well and buried p-type field shaping layers. Finally, the new designed LDMOS guarantees breakdown voltage of more than 750V and specific on-resistance of 150 mohm.cm² which is about 60% of traditional LDMOS for HVIC products such as switch mode power 1-chip IC's.

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