

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

The Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

Customer No.: 25700

This is a request for filing a

____ Continuation application XX Divisional application

under 37 CFR 1.53(b), of pending prior application Serial No. 13/941,335

filed on: 07/12/2013 for Applicant(s): Briere, et al.

entitled: "Transistor Having Elevated Drain Finger Termination"

XX 1. The filing fee is calculated below:

	(Col. 1)	(Col. 2)	SMALL ENTITY		OTHER THAN A SMALL ENTITY	
FOR:	No. Filed	No. Extra	RATE	FEE	RATE	FEE
BASIC FEE				\$140.00		\$280.00
SEARCH FEE				\$300.00		\$600.00
EXAMINATION FEE				\$360.00		\$720.00
APPLICATION SIZE FEE (Total Number of Sheets)	(45 -100)/50=	0	x \$200.00=	\$	x \$400.00=	\$
TOTAL CLAIMS	11 -20 =	0	x \$40.00=	\$	x \$80.00=	\$
INDEPENDENT CLAIMS	1 -3 =	0	x \$210.00=	\$	x \$420.00 =	\$
MULTIPLE DEPENDENT CLAIMS PRESENTED			+ \$390.00=	\$	+ \$780.00 =	\$
If the difference in Col. 1 is less than zero, enter "0" in Col. 2			TOTAL	\$		\$1,600.00

XX 2. Enclosed is a payment in the amount of \$1,600.00 by credit card(authorization provided with this electronic submission).

____ 3. Check No. ____ in the amount of \$ ____ is enclosed as a petition fee for a three month extension of time pursuant to Rule 1.17.

XX 4. Please cancel in this application original claims 1-9 and 16-20 of the prior application before calculating the filing fee.

5. A verified statement to establish small entity status under 37 CFR 1.9 and 1.27 was filed in the pending prior application and such status is still proper and desired.

XX 6. The prior application is assigned of record to: International Rectifier Corporation.

XX 7. The Power of Attorney in the prior application is to:

Customer No.: 25700

FARJAMI & FARJAMI LLP
26522 La Alameda Ave., Suite 360
Mission Viejo, California 92691
(949) 282-1000

XX (a) The Power appears in the original papers of the prior application.

 (b) Since the Power does not appear in the original papers, a copy of the Power in the prior application is enclosed.

XX (c) Recognize as associate attorney and address all future communications to:

Michael Farjami, Esq.
FARJAMI & FARJAMI LLP
26522 La Alameda Ave., Suite 360
Mission Viejo, California 92691
(949) 282-1000

XX 8. A preliminary amendment is enclosed.

XX 9. It is hereby requested that any request for a convention priority made in the prior application be transferred to this Rule 1.53(b) application.

 10. Applicant hereby petitions for an extension of time pursuant to Rule 1.136, if one is needed, for the above-noted prior application. A duplicate copy of this sheet is enclosed for filing in the proper application file.

XX 11. Enclosed is a copy of the latest inventor-signed application, including a copy of the oath or declaration as originally filed. I hereby verify that the papers are a true copy of the latest signed application Serial No. 13/941,335, as filed on 07/12/2013. No amendments referred to in the oath or declaration filed to complete the latest signed application, or the continuation and/or division thereof, introduced new matter therein.

XX 12. The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment, to Deposit Account Number 50-0731.

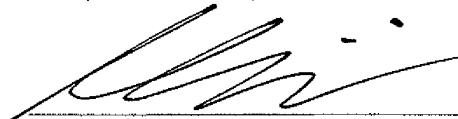
XX 13. Application Data Sheet (PTO/AIA/14) is enclosed.

 14. Request for Non-Publication (Form PTO/SB/35) is enclosed.

The undersigned declares further, that all statements made herein of his own knowledge are true, and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

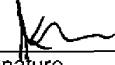
Respectfully submitted,
FARJAMI & FARJAMI LLP

Date: June 25, 2015


Michael Farjami
Reg. No. 38,135

Michael Farjami, Esq.
FARJAMI & FARJAMI LLP
26522 La Alameda Ave., Suite 360
Mission Viejo, California 92691
Tel: (949) 282-1000
Fax: (949) 282-1002

___ Inventor(s)
___ Assignee of Complete Interest
XX Attorney of Record in prior application.

<u>CERTIFICATE OF ELECTRONIC FILING</u>	
I hereby certify that this correspondence is being submitted electronically to the United States Patent and Trademark Office through the EFS Filing System, on <u>6/25/15</u> .	
<u>Kate Marlow</u> Name	<u></u> Signature

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	0400726D1
		Application Number	
Title of Invention	Transistor with Elevated Drain Termination		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2

☐	Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)
--------------------------	---

Inventor Information:

Inventor 1						Remove	
Legal Name							
Prefix	Given Name	Middle Name	Family Name	Suffix			
	Michael	A.	Briere				
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service							
City	Scottsdale	State/Province	AZ	Country of Residence	US		
Mailing Address of Inventor:							
Address 1		6902 E calle de las Estrellas					
Address 2							
City	Scottsdale	State/Province	AZ				
Postal Code	85266	Country	US				
Inventor 2						Remove	
Legal Name							
Prefix	Given Name	Middle Name	Family Name	Suffix			
	Reenu		Garg				
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service							
City	Torrance	State/Province	CA	Country of Residence	US		
Mailing Address of Inventor:							
Address 1		3553 Emerald Street, Apt #319					
Address 2							
City	Torrance	State/Province	CA				
Postal Code	90503	Country	US				
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button.							

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).
--

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	0400726D1
		Application Number	
Title of Invention	Transistor with Elevated Drain Termination		

☐ An Address is being provided for the correspondence information of this application.

Customer Number	25700		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	Transistor with Elevated Drain Termination		
Attorney Docket Number	0400726D1	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	6	Suggested Figure for Publication (if any)	

Publication Information:
☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	25700		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

When referring to the current application, please leave the application number blank.

Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Division of	13941335	2013-07-12
Prior Application Status	Expired	Remove	

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	0400726D1
		Application Number	
Title of Invention	Transistor with Elevated Drain Termination		

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
13941335	Claims benefit of provisional	61674553	2012-07-23
Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
13941335	Continuation in part of	13749477	2013-01-24
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
13749477	Claims benefit of provisional	61600469	2012-02-17

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)¹ the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

[Remove](#)

Application Number	Country ¹	Filing Date (YYYY-MM-DD)	Access Code ¹ (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

- ☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
- NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	0400726D1
		Application Number	
Title of Invention	Transistor with Elevated Drain Termination		

Authorization to Permit Access:

☒ Authorization to Permit Access to the Instant Application by the Participating Offices
If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application. In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application. In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.		
Applicant 1		
If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.		
Clear		
☒ Assignee	☐ Legal Representative under 35 U.S.C. 117	☐ Joint Inventor
☐ Person to whom the inventor is obligated to assign.		☐ Person who shows sufficient proprietary interest
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:		
Name of the Deceased or Legally Incapacitated Inventor :		
If the Applicant is an Organization check here. ☒		
Organization Name	International Rectifier Corporation	

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	0400726D1
		Application Number	
Title of Invention	Transistor with Elevated Drain Termination		

Mailing Address Information For Applicant:			
Address 1		Tony Bramian, Executive Director of IP	
Address 2		101 N. Sepulveda Blvd.	
City	El Segundo	State/Province	CA
Country	US	Postal Code	90245
Phone Number		Fax Number	
Email Address			
Additional Applicant Data may be generated within this form by selecting the Add button.			

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

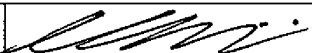
Assignee 1				
Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.				
If the Assignee or Non-Applicant Assignee is an Organization check here. ☐				
Prefix	Given Name	Middle Name	Family Name	Suffix
Mailing Address Information For Assignee including Non-Applicant Assignee:				
Address 1				
Address 2				
City		State/Province		
Country		Postal Code		
Phone Number		Fax Number		
Email Address				
Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.				

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	0400726D1
		Application Number	
Title of Invention	Transistor with Elevated Drain Termination		

Signature:

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Signature			Date (YYYY-MM-DD)	2015-06-25	
First Name	Michael	Last Name	Farjami	Registration Number	38135
Additional Signature may be generated within this form by selecting the Add button.					

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **Briere, et al.**

Serial No.:

Filed:

For: **Transistor with Elevated Drain Termination**

Examiner:

Group Art Unit:

This is a Rule 1.53(b) division of parent
U.S. Application entitled "Transistor Having
Elevated Drain Finger Termination," 13/941,335,
Filed 07/12/2013

PRELIMINARY AMENDMENT TO DIVISIONAL APPLICATION

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This amendment is directed to the accompanying 37 CFR §1.53(b) divisional application. Please enter the following amendments in the present Rule 1.53(b) divisional application.

In the Title:

Please amend the title as follows:

Transistor ~~Having~~ with Elevated Drain ~~Finger~~ Termination

In the Specification:

After the title, please insert the paragraph:

-- This is a divisional of application Serial No. 13/941,335 filed Jul. 12, 2013, which itself claims priority to U.S. provisional application Ser. No. 61/674,553, filed Jul. 23, 2012, and is a continuation in part of application Serial No. 13/749,477, filed Jan. 24, 2013, which itself claims priority to U.S. provisional application Ser. No. 61/600,469, filed Feb. 17, 2012. The disclosures in the above-referenced patent applications are hereby incorporated fully by reference into the present application.--

In the Claims:

Claims 1-9 (canceled)

Claim 10 (original): A transistor comprising:

drain finger electrodes and source finger electrodes situated on a semiconductor substrate;

said drain finger electrodes interdigitated with source finger electrodes;

a gate region configured to control current conduction in said semiconductor substrate between said drain finger electrodes and said source finger electrodes;

at least one of said drain finger electrodes having a drain finger electrode main body and a drain finger electrode end having an increased elevation relative to said drain finger electrode main body.

Claim 11 (original): The transistor of claim 10, wherein a dielectric material provides said increased elevation of said drain finger electrode end relative to said drain finger electrode main body.

Claim 12 (original): The transistor of claim 10, wherein said drain finger electrode end has an increased radius of curvature.

Claim 13 (original): The transistor of claim 10, wherein at least one of said source finger electrodes has a source finger electrode main body coupled to a source pad, said drain finger electrode end extending beyond said source finger electrode main body.

Claim 14 (original): The transistor of claim 10, wherein said drain finger electrodes are longer than said source finger electrodes.

Claim 15 (original): The transistor of claim 10, wherein said drain finger electrode end has an increased width relative to a width of said drain finger electrode main body.

Claims 16-20 (canceled)

Claim 21 (new): The transistor of claim 10, wherein said drain finger electrode main body is situated on said semiconductor substrate.

Claim 22 (new): The transistor of claim 10, wherein said transistor is a high-electron-mobility transistor (HEMT).

Claim 23 (new): The transistor of claim 10, wherein said transistor comprises a group III-V transistor.

Claim 24 (new): The transistor of claim 10, wherein said drain finger electrode end is substantially an ellipsoid.

Claim 25 (new): The transistor of claim 10, wherein said drain finger electrode is a tapered drain finger electrode.

REMARKS

This is a divisional application of the pending parent application Serial No. 13/941,335 filed 07/12/2013. This divisional application is filed during the pendency of the parent application. By this preliminary amendment, applicant has canceled claims 1-9 and 16-20, and has added new claims 21-25. Thus, claims 10-15 and 21-25 remain in the present divisional application. Applicant respectfully requests an early examination and/or allowance of claims 10-15 and 21-25 pending in the present application.

A true and correct copy of the parent application, including the specification, drawings and claims, as originally filed, is enclosed. Also enclosed is a true and correct copy of the declaration as filed in the parent application. Please direct all correspondence and communications to the undersigned attorneys of record.

Respectfully submitted,
FARJAMI & FARJAMI LLP

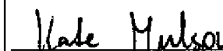
Date: June 25, 2015


Michael Farjami
Reg. No. 38,135

Michael Farjami, Esq.
FARJAMI & FARJAMI LLP
26522 La Alameda Ave., Suite 360
Mission Viejo, California 92691
Tel: (949) 282-1000
Fax: (949) 282-1002

CERTIFICATE OF ELECTRONIC FILING

I hereby certify that this correspondence is being submitted electronically to the United States Patent and Trademark Office through the EFS Filing System, on 6/25/15.


Name


Signature

Attorney Docket No.: 0400726

**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION
USING AN
APPLICATION DATA SHEET (37 CFR 1.76)**

Title of
Invention

Transistor Having Elevated Drain Finger Termination

As the below named inventor, I declare that:

This declaration is directed to:

- ☒ The attached application, or
☐ United States application or PCT International application number _____
filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application. I acknowledge the duty to disclose information, which is material to patentability of this application as defined in Section 1.56 of Title 37, Code of Federal Regulations (see the last page attached hereto).

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

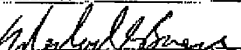
WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Michael A. Briere

Date: 7/12/13

Signature: 

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

37 C.F.R. Section 1.56 - Duty to disclose information material to patentability.

A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by Sections 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

Prior art cited in search reports of a foreign patent office in a counterpart application, and

The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

It refutes, or is inconsistent with, a position the applicant takes in:

Opposing an argument of unpatentability relied on by the Office, or

Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

Each inventor named in the application;

Each attorney or agent who prepares or prosecutes the application; and

Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

Attorney Docket No.: 0400726

**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN
APPLICATION DATA SHEET (37 CFR 1.76)**Title of
Invention**Transistor Having Elevated Drain Finger Termination**

As the below named inventor, I declare that:

This declaration is directed to:

- ☒ The attached application, or
☐ United States application or PCT international application number _____
filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application. I acknowledge the duty to disclose information, which is material to patentability of this application as defined in Section 1.56 of Title 37, Code of Federal Regulations (see the last page attached hereto).

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

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LEGAL NAME OF INVENTORInventor: Reenu GargDate: 10th July 2013Signature: Reenu Garg

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Attorney Docket No.: 0400726

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UNITED STATES PATENT APPLICATION
FOR
TRANSISTOR HAVING ELEVATED DRAIN
FINGER TERMINATION

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STATEMENT OF GOVERNMENT INTEREST

This invention was made with Government support under Contract No. DE-AR0000016 awarded by Advanced Research Projects Agency-Energy (ARPA-E). The Government has certain rights in this invention.

5

BACKGROUND

The present application claims the benefit of and priority to U.S. Provisional Patent Application Ser. No. 61/674,553, filed on July 23, 2012 and entitled "Elevated Drain Finger Termination," and is a continuation-in-part of U.S. Patent Application Ser. No. 13/749,477, filed on January 24, 2013 and entitled "Transistor Having Increased Breakdown Voltage," which itself claims the benefit of and priority to U.S. Provisional Patent Application Ser. No. 61/600,469, filed on February 17, 2012 and entitled "Drain Termination for Transistor with Improved Breakdown Voltage." The disclosures of the above applications are hereby incorporated fully by reference into the present application.

I. DEFINITIONS

15

As used herein, the phrase "group III-V" refers to a compound semiconductor including at least one group III element and at least one group V element. By way of example, a group III-V semiconductor may take the form of a III-Nitride semiconductor. "III-Nitride", or "III-N", refers to a compound semiconductor that includes nitrogen and at least one group III element such as aluminum (Al), gallium (Ga), indium (In), and boron (B), and including but not limited to any of its alloys, such as aluminum gallium nitride ($\text{Al}_x\text{Ga}_{(1-x)}\text{N}$), indium gallium nitride ($\text{In}_y\text{Ga}_{(1-y)}\text{N}$), aluminum indium gallium nitride ($\text{Al}_x\text{In}_y\text{Ga}_{(1-x-y)}\text{N}$), gallium arsenide phosphide nitride ($\text{GaAs}_a\text{P}_b\text{N}_{(1-a-b)}$).

20

a-b)), aluminum indium gallium arsenide phosphide nitride ($\text{Al}_x\text{In}_y\text{Ga}_{(1-x-y)}\text{As}_a\text{P}_b\text{N}_{(1-a-b)}$), for example. III-Nitride also refers generally to any polarity including but not limited to Ga-polar, N-polar, semi-polar, or non-polar crystal orientations. A III-Nitride material may also include either the Wurtzitic, Zincblende, or mixed polytypes, and may include single-crystal, monocrystalline, polycrystalline, or amorphous structures. Gallium nitride or GaN, as used herein, refers to a III-Nitride compound semiconductor wherein the group III element or elements include some or a substantial amount of gallium, but may also include other group III elements in addition to gallium. A group III-V or a GaN transistor may also refer to a composite high voltage enhancement mode transistor that is formed by connecting the group III-V or the GaN transistor in cascode with a lower voltage group IV transistor.

In addition, as used herein, the phrase “group IV” refers to a semiconductor that includes at least one group IV element such as silicon (Si), germanium (Ge), and carbon (C), and may also include compound semiconductors such as silicon germanium (SiGe) and silicon carbide (SiC), for example. Group IV also refers to semiconductor materials which include more than one layer of group IV elements, or doping of group IV elements to produce strained group IV materials, and may also include group IV based composite substrates such as silicon on insulator (SOI), separation by implantation of oxygen (SIMOX) process substrates, and silicon on sapphire (SOS), for example.

II. BACKGROUND ART

Group III-V heterostructure field-effect transistors (group III-V HFETs), such as group III-V high electron mobility transistors (group III-V HEMTs), are often utilized in

high power switching applications. For example, III-Nitride HEMTs may be utilized to provide switching and/or amplification functions.

Group III-V HFETs advantageously allow for power transistors using a lateral conduction topology in which drain, source, and gate electrodes are formed on one side of a semiconductor wafer or die. In a typical lateral transistor layout, for example, drain and source finger electrodes coupled to respective drain and source pads may be interdigitated with a gate region located between the source and drain. As the power requirement for such transistors continues to increase, the transistors are fabricated with a higher unit cell density. However, due to high termination electric fields typically present at the drain finger electrode ends, the gate-to-drain spacing at the drain finger electrode ends of higher density power transistors may be insufficient to reliably sustain a high breakdown voltage.

SUMMARY

A transistor having elevated drain finger termination such that at least a portion thereof is non-coplanar with the drain finger electrode main body, substantially as shown in and/or described in connection with at least one of the figures, and as set forth more
5 completely in the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 presents a top plan view of a transistor.

Figure 2 presents a top plan view of an exemplary transistor having a drain termination enabling increased breakdown voltage, in accordance with an implementation
5 of the present disclosure.

Figure 3A presents a top plan view of an exemplary drain termination enabling increased breakdown voltage, corresponding in general to the implementation shown in Figure 2.

Figure 3B presents a top plan view of an exemplary drain termination enabling
10 increased breakdown voltage, corresponding in general to the implementation shown in Figure 2.

Figure 4 presents a top plan view of an exemplary drain termination enabling increased breakdown voltage, corresponding in general to the implementation shown in Figure 2.

15 Figure 5 presents a top plan view of an exemplary drain termination including a tapered drain finger electrode enabling increased breakdown voltage, in accordance with an implementation of the present disclosure.

Figure 6A presents a top plan view of an exemplary transistor having a drain termination enabling increased breakdown voltage, in accordance with an implementation
20 of the present disclosure.

Figure 6B presents a cross-sectional view of an exemplary transistor, in accordance with an implementation of the present disclosure.

Figure 6C presents a cross-sectional view of an exemplary transistor having a drain finger electrode main body which is non-coplanar with the drain finger termination, in accordance with an implementation of the present disclosure.

DETAILED DESCRIPTION

The following description contains specific information pertaining to implementations in the present disclosure. The drawings in the present application and their accompanying detailed description are directed to merely exemplary

5 implementations. Unless noted otherwise, like or corresponding elements among the figures may be indicated by like or corresponding reference numerals. Moreover, the drawings and illustrations in the present application are generally not to scale, and are not intended to correspond to actual relative dimensions.

Figure 1 presents a top plan view of a transistor. Transistor 100 has active surface
10 102 including source pad 104, drain pad 106, and gate pad 108. Transistor 100 also includes gate region 109 adjoining gate pad 108, source finger electrodes 111, drain finger electrodes 121, and field dielectric 107 isolating source finger electrodes 111 and drain finger electrodes 121 from gate region 109. Source finger electrodes 111 are electrically coupled to source pad 104, and drain finger electrodes 121 are electrically
15 coupled to drain pad 106. It is noted that drain finger electrodes 121 are terminated adjacent source pad 104 by being simply rounded off to form semicircular drain finger electrode ends 125. It is further noted that the electrical coupling of source finger electrodes 111 and drain finger electrodes 121 to respective source pad 104 and drain pad 106 is shown by dashed lines because those connections may be formed using one or
20 more additional metal layers not shown in Figure 1.

Source finger electrodes 111 and drain finger electrodes 121 are situated in gate region 109 and are implemented in an interdigitated pattern such that gate region 109

surrounds source finger electrodes 111 and drain finger electrodes 121, and is disposed between the interdigitated source finger electrodes 111 and drain finger electrodes 121. As further shown in Figure 1, transistor 100 has source-to-drain half-pitch 135, i.e., the distance separating center line 131 of source finger electrode 111 from center line 132 of drain finger electrode 121.

Transistor 100 has an interdigitated layout commonly utilized to implement lateral power transistors. As shown in Figure 1, source-to-drain half-pitch 135 is substantially constant along the entirety of drain finger electrodes 121. However, due to the high termination electric fields, which may develop under high voltage operation, particularly at semicircular drain finger electrode ends 125, the robustness of transistor 100 may be compromised. As a result, transistor 100 may break down, become unstable, and/or fail catastrophically under high voltage operation. In accordance with an implementation of the present disclosure, various approaches are described, which can be utilized alone or in any combination to ease the high termination electric fields, amongst other advantages.

Figure 2 presents a top plan view of an exemplary transistor having a drain termination enabling increased breakdown voltage, in accordance with an implementation of the present disclosure. Figure 2 shows transistor 200 fabricated in active surface 202 of semiconductor body 201. Transistor 200 includes drain finger electrodes 220 interdigitated with source finger electrodes 210. Transistor 200 may be a high voltage transistor.

It is noted that as used herein, the feature referred to as a “transistor” may correspond more generally to a variety of specific transistor or other semiconductor

device implementations. In one implementation, for example, transistor 200 may take the form of a field-effect transistor (FET). For instance, transistor 200 may be an insulated-gate FET (IGFET) or a heterostructure FET (HFET). In one implementation, transistor 200 may take the form of a metal-insulator-semiconductor FET (MISFET), such as a metal-oxide-semiconductor FET (MOSFET). In other implementations, transistor 200 may take the form of a schottky gated transistor, or a P-N junction gated transistor or (JFET). When implemented as an HFET, transistor 200 may be a high-electron-mobility transistor (HEMT) incorporating a two-dimensional electron gas (2DEG). In yet another implementation, transistor 200 may take the form of a Schottky diode (not shown in Figure 2), for example through replacement of drain finger electrodes 220 with anode electrodes, replacement of the source finger electrodes 210 with cathode electrodes, and without the controlling gate electrode of Figure 2.

Referring to the exemplary implementation shown by Figure 2, semiconductor body 201 of transistor 200 may be configured to provide a group III-V HFET, such as a III-Nitride HEMT. III-Nitride materials include gallium nitride (GaN) and/or its alloys, such as aluminum gallium nitride (AlGaN), indium gallium nitride (InGaN), and aluminum indium gallium nitride (AlInGaN). These materials are semiconductor compounds that have a relatively wide, direct bandgap and strong piezoelectric polarizations, and can enable high breakdown fields, and the creation of 2DEGs. As a result, III-Nitride materials such as GaN are used in many microelectronic applications in which high power density and high efficiency switching are required.

Active surface 202 of transistor 200 includes source pad 204, drain pad 206, and

gate pad 208. In addition to drain finger electrodes 220 and source finger electrodes 210, transistor 200 also includes gate region 209, and field dielectric 207. Source finger electrodes 210 are electrically coupled to source pad 204, drain finger electrodes 220 are electrically coupled to drain pad 206, and gate region 209 is electrically coupled to gate pad 208. It is noted that the electrical coupling of source finger electrodes 210 to source pad 204 and that of gate region 209 to gate pad 208 is shown by dashed lines because those connections may be formed using one or more additional metal layers not shown in Figure 2.

It is noted that in some implementations, either or both of source pad 204 and drain pad 206 may be on the same plane as source finger electrodes 210 and drain finger electrodes 220. However, in other implementations, source pad 204 and/or drain pad 206 may be on a different plane than that occupied by source finger electrodes 210 and/or drain finger electrode 220. For example, source pad 204 and/or drain pad 206 may be formed on a backside of the device or substrate and electrically connected to their respectively corresponding finger electrodes using electrical through-substrate vias. Such transistor designs with ohmic pad (source and/or drain) construction on other planes are described in U.S. Patent Number 7,233,028, entitled "Gallium Nitride Material Devices and Methods of Forming the Same," and issued on June 19, 2007; and in U.S. Patent Number 7,915,645, entitled "Monolithic Vertically Integrated Composite Group III-V and Group IV Semiconductor Device and Method for Fabricating Same," and issued on March 29, 2011. The entire disclosures of U.S. Patent Number 7,233,028 and U.S. Patent Number 7,915,645 are hereby incorporated fully by reference into the present application.

As shown in Figure 2, source finger electrodes 210 and drain finger electrodes 220 may be implemented in an interdigitated pattern such that gate region 209 surrounds source finger electrodes 210 and is between interdigitated source finger electrodes 210 and drain finger electrodes 220. Source finger electrodes 210 have length 212, and drain finger electrodes 220 have length 222. Also shown in Figure 2 is source-to-drain half-pitch 235 of transistor 200, i.e., the distance separating center line 231 of source finger electrode 210 from center line 232 of drain finger electrode 220.

Source finger electrodes 210 have source finger electrode main bodies 214 coupled to source pad 204, and source finger electrode ends 216 adjacent drain pad 206. Drain finger electrodes 220 have drain finger electrode main bodies 224 coupled to drain pad 206, and curved drain finger electrode ends or tips 226 adjacent source pad 204. As shown in Figure 2, source-to-drain half-pitch 235 of transistor 200 is substantially constant from source finger electrode main bodies 214 to source finger electrode ends 216. As further shown in Figure 2, curved drain finger electrode ends 226 are modified in order to reduce the electric field at the tips of drain finger electrodes 220.

In at least one exemplary implementation, curved drain finger electrode ends 226 have an increased radius of curvature, such as $(r1)$ 236, for example, resulting in increased width 246 of curved drain finger electrode ends 226 relative to width 254 of drain finger electrode 220. It is noted that as used herein, width 254 is defined as the width of drain finger electrode 220 just before the transition to curved drain finger electrode end 226. As also shown in Figure 2, radius of curvature $(r2)$ 241 of gate region 209 surrounding curved drain finger electrode end 226 is also increased, which increases

the gate-to-drain spacing (d2) 257 in the vicinity of curved drain finger electrode ends 226 compared to the gate-to-drain spacing (d1) 267, further reducing the electric field at curved drain finger electrode ends 226. It is noted that for the purposes of the present application, when curved drain finger electrode ends 226 are described as having an
5 increased radius of curvature, that characterization can apply to either one, or both, of (r1) 236 and (r2) 241.

In some implementations, as shown in Figure 2, increased radius of curvature (r1) 236 of curved drain finger electrode ends 226 may cause curved drain finger electrode ends 226 to have a generally ellipsoidal shape as discussed in more detail in reference to
10 Figures 3A, 3B, and 4, below. One advantage of implementing curved drain finger electrode ends 226 as substantial ellipsoids is that such a shape can aid in reducing or relaxing the high termination electrical fields that can otherwise exist at semicircular drain finger electrode ends 125 of transistor 100, shown in Figure 1. As a result, increased radius of curvature (r1) 236 and/or increased radius of curvature (r2) 241, as
15 well as the subsequent increase in gate-to-drain spacing (d2) 257 at curved drain finger electrode ends 226, reduces the termination electric field at curved drain finger electrode ends 226 so as to achieve an increased breakdown voltage and reliability for transistor 200.

In some implementations, curved drain finger electrode ends 226 are extended
20 beyond source finger electrode main bodies 214 instead of or in addition to providing curved drain finger electrode ends 226 having an increased radius of curvature. As depicted in Figure 2, curved drain finger electrode ends 226 are situated closer to source

pad 204 than source finger electrode main bodies 214. In doing so, drain finger electrodes 220 may be longer than source finger electrodes 210, as shown. Extension of curved drain finger electrode ends 226 beyond source finger electrode main bodies 214 can advantageously achieve an increased breakdown voltage for transistor 200 without increasing source-to-drain half-pitch 235 along length 212 of source finger electrodes 210. Consequently, the exemplary transistor layout shown in Figure 2 can be implemented so as to allow for a tighter source-to-drain half-pitch while achieving increased breakdown voltage, thereby providing a low ON-resistance and improved robustness for transistor 200, concurrently.

10 It is noted that although the implementation shown in Figure 2 depicts drain finger electrodes 220 as having increased radius of curvature ($r1$) 236, increased radius of curvature ($r2$) 241, and increased width 246 at curved drain finger electrode ends 226, as well as having curved drain finger electrode ends 226 extending beyond source finger electrode main bodies 214, that representation is merely exemplary. In other implementations, drain finger electrodes 220 may not have all of those characteristics concurrently.

15 In one implementation, curved drain finger electrode ends 226 may extend beyond source finger electrode main bodies 214 but not have increased radius of curvature ($r1$) 236, increased radius of curvature ($r2$) 241, or increased width 246. Alternatively, according to another implementation, curved drain finger electrode ends 226 may have increased radius of curvature ($r1$) 236, increased width 246, and/or increased radius of curvature ($r2$) 241, but may not extend beyond source finger electrode main bodies 214.

Thus, according to a variety of possible implementations, drain finger electrodes 220 may have length 222 greater than length 212 of source finger electrodes 210, and/or may have curved drain finger electrode ends 226 extending beyond source finger electrode main bodies 214, and/or may have increased radius of curvature (r1) 236, increased width 246, and/or increased radius of curvature (r2) 241 at curved drain finger electrode ends 226.

Some of the features discussed in conjunction with Figure 2 will now be further described by reference to Figures 3A, 3B, and 4. Figures 3A, 3B, and 4 present respective top plan views of exemplary drain terminations having a decreased electric field at the ends or tips of the drain finger electrodes. As further described below, such a decreased electric field can result from increasing a radius of curvature of the gate-to-drain spacing between an edge of a curved drain finger electrode end and a boundary of a gate region surrounding the curved drain finger electrode end, thereby allowing for an increased breakdown voltage and a more robust and reliable transistor. It is noted that the exemplary implementations shown in Figures 3A, 3B, and 4 corresponding in general to the implementation shown in Figure 2.

Figure 3A presents a top plan view of an exemplary drain termination enabling increased breakdown voltage, corresponding in general to the implementation shown in Figure 2. Figure 3A shows a portion of gate region 309 surrounding drain finger electrode 320. Also shown in Figure 3A are source finger electrodes 310 with which drain finger electrode 320 is interdigitated, and field dielectric 307. Gate region 309, drain finger electrode 320, source finger electrodes 310, and field dielectric 307 correspond respectively to gate region 209, drain finger electrodes 220, source finger

electrodes 210, and field dielectric 207, in Figure 2.

Figure 3A shows the relative width of drain finger electrode 320 compared to source finger electrodes 310, as well as the smooth transitions at the curved end of drain finger electrode 320. It is noted that there are no sharp discontinuities in the curvature of the drain finger electrode end. In addition, and as further shown by Figure 3A, there are no sharp discontinuities at the boundary of field dielectric 307 with gate region 309, which also aids in reducing the electric fields at the end of drain finger electrode 320.

Continuing to Figure 3B, Figure 3B presents a top plan view of an exemplary drain termination enabling increased breakdown voltage, corresponding in general to the implementation shown in Figure 2. Figure 3B shows gate region 309 surrounding drain finger electrode 320. Drain finger electrode 320 has width 354, and also includes drain finger electrode main body 324 having width 334. In addition, Figure 3B shows curved drain finger electrode end 326 having increased radius of curvature (r_1) 336 relative to the radius of curvature of semicircular drain finger electrode ends 125 in transistor 100 of Figure 1. That is to say, in contrast to transistor 100 having semicircular drain finger ends 125, radius of curvature (r_1) 336 of curved drain finger end 326 is greater than a radius of curvature of a circle having a diameter equal to width 354.

Also shown in Figure 3B is radius of curvature (r_2) 341 of the gate electrode region surrounding the drain finger electrode end 326, radius of curvature (r_3) 371 of the smooth transition connecting curved drain finger electrode end 326 to drain finger electrode 320, and radius of curvature (r_4) 381 of the smooth transition connecting gate region 309 surrounding curved drain finger electrode end 326 to the gate region

surrounding drain finger electrode 320. Figure 3B further depicts gate-to-drain spacing (d1) 367, gate-to-drain spacing (d2) 357, and length 322 of drain finger electrode 320. Gate-to-drain spacing (d1) 367, gate-to-drain spacing (d2) 357, length 322, and width 354, correspond respectively to gate-to-drain spacing (d1) 267, gate-to-drain spacing (d2) 257, length 222, and width 254, in Figure 2. Moreover, curved drain finger electrode end 326, radius of curvature (r1) 336, and radius of curvature (r2) 341, in Figure 3B, correspond respectively to curved drain finger electrode ends 226, radius of curvature (r1) 236, and radius of curvature (r2) 241, in Figure 2.

In certain implementations, $r1 < r2 < r4$. Moreover, gate-to-drain spacing (d1) 367 is shown as being less than gate-to-drain spacing (d2) 357. By forming the gate-to-drain spacing such that $d1 < d2$, the reduced electric field at curved drain finger electrode end 326, in combination with the ellipsoidal shape of curved drain finger electrode end 326 and the smooth curvatures created by r1, r2, r3, and r4, allows for the formation of a more robust drain finger electrode termination. It is noted that for the purposes of the present application, when curved drain finger electrode end 326 is described as having an increased radius of curvature, that characterization can apply to any one of (r1) 336, (r2) 341, (r3) 371, or (r4) 381, as well as to any combination of (r1) 336, (r2) 341, (r3) 371, and (r4) 381.

Continuing to Figure 4, Figure 4 presents a top plan view of an exemplary drain termination enabling increased breakdown voltage, corresponding in general to the implementation shown in Figure 2. Figure 4 shows gate region 409 surrounding drain finger electrode 420. Drain finger electrode 420 has width 454 and includes drain finger

electrode main body 424 having width 434. In addition, drain finger electrode 420 has curved drain finger electrode end 426 with increased width 446 relative to width 454 of drain finger electrode 420. Also shown in figure 4 are field dielectric 407, radius of curvature (r1) 436, radius of curvature (r2) 441, radius of curvature (r3) 471, radius of curvature (r4) 481, gate-to-drain spacing (d1) 467, and gate-to-drain spacing (d2) 457, as well as minor axis 442 and major axis 443 of curved drain finger electrode end 426.

Gate region 409, field dielectric 407, and drain finger electrode 420 correspond respectively to gate region 309, field dielectric 307, and drain finger electrode 320, in Figures 3A and 3B. In addition, width 454, curved drain finger electrode end 426, and drain finger electrode main body 424 having width 434, correspond respectively to width 354, curved drain finger electrode end 326, and drain finger electrode main body 324 having width 334, in Figure 3B. Moreover, gate-to-drain spacings (d1) 467 and (d2) 457, and radii of curvature (r1) 436, (r2) 441, (r3) 471, and (r4) 481, in Figure 4, correspond respectively to gate-to-drain spacings (d1) 367 and (d2) 357, and radii of curvature (r1) 236, (r2) 241, (r3) 371, and (r4) 381, in Figure 3B. It is further noted that increased width 446 of curved drain finger electrode end 426, in Figure 4, corresponds to increased width 246 of curved drain finger electrode end 226, in Figure 2.

As shown in Figure 4, curved drain finger electrode end 426 has a shape described by major axis 443 and minor axis 442. Major axis 443 is longer than and substantially perpendicular to minor axis 442. As further shown in Figure 4, major axis 443 is substantially aligned with drain finger electrode 420, and minor axis 442 is substantially perpendicular to drain finger electrode 420.

In some implementations, for example, curved drain finger electrode end 426 may be substantially an ellipsoid having major axis 443 substantially aligned with drain finger electrode 420. Curved drain finger electrode end 426 taking the form of an ellipsoid with major axis 443 and minor axis 442 results from forming curved drain finger electrode end 5 426 and the surrounding gate region 409 with increased radii of curvature (r_1) 436, r_2 (441), r_3 (471), and r_4 (481) such that $r_1 < r_2 < r_4$. In addition, both r_3 and r_4 radii of curvature are optimized to have a smooth curvature with no sharp discontinuities where they meet drain finger electrode 420 and gate region 409 surrounding drain finger electrode 420, respectively.

10 Gate-to-drain spacing (d_1) 467 is shown as being less than gate-to-drain spacing (d_2) 457. As discussed above by reference to Figure 3B, by forming the gate-to-drain spacing such that $d_1 < d_2$, in combination with the ellipsoidal shape of curved drain finger electrode end 426, and the smooth curvatures created by radii of curvature r_1 , r_2 , r_3 , and r_4 , allows for the formation of a more robust drain finger electrode termination.

15 In some implementations, it may be advantageous for the ratio of increased width 446 to width 454 to be approximately equal to 2:1. In other implementations, it may be advantageous or desirable for the ratio of increased width 446 to width 454 to be greater than 2:1. An advantage of using an ellipsoidal shape for curved drain finger electrode end 426 is that such a shape can aid in minimizing the peak electric fields that can 20 otherwise be present at the transition from a main body to a rounded semicircular end termination region of a conventionally configured drain finger electrode, such as semicircular drain finger electrode ends 125, in Figure 1.

It is noted that width 454, increased width 446, and curved drain finger electrode end 426 are exaggerated in Figure 4, for conceptual clarity. Thus, drain finger electrode 420 is not drawn to scale. Nevertheless, drain finger electrode 420 corresponds to drain finger electrodes 220 in Figure 2, as well as to drain finger electrode 320 in Figures 3A and 3B, as noted above.

In some implementations, further improvements in high current carrying transistors can be realized with higher breakdown voltages and lower ON-resistance through use of tapered drain and source finger electrodes, which may be implemented in combination with a curved drain finger electrode end having an increased radius of curvature, corresponding to curved drain finger electrode ends 226/326/426 in respective Figures 2, 3B, and 4. Such tapered source and drain finger designs are described in U.S. Patent Number 7,417,257, entitled "III-Nitride Device with Improved Layout Geometry," and issued on August 26, 2008. The entire disclosure of U.S. Patent Number 7,417,257 is hereby incorporated fully by reference into the present application.

Figure 5 presents a top plan view of an exemplary drain termination including a tapered drain finger electrode enabling increased breakdown voltage, in accordance with an implementation of the present disclosure. Figure 5 shows gate region 509 surrounding tapered drain finger electrode 520. Tapered drain finger electrode 520 has width 554, and includes a tapered drain finger electrode main body 524 having width 534. In addition, tapered drain finger electrode 520 includes curved drain finger electrode end 526 with increased radius of curvature (r_1) 536 relative to the radius of curvature of semicircular drain finger electrode ends 125 in transistor 100 of Figure 1. That is to say, in contrast to

transistor 100 having semicircular drain finger ends 125, radius of curvature (r1) 536 of curved drain finger electrode end 526 is greater than a radius of curvature of a circle having a diameter equal to width 554.

As further shown in Figure 5, width 534 of tapered drain finger electrode main
5 body 524 is larger than width 554. In other words, in contrast to drain finger electrode 320/420 for which width 334/434 of drain finger electrode main bodies 324/424 may be substantially equal to width 354/454, tapered drain finger electrode 520 has a tapered drain finger electrode beginning width 534 that is greater than width 554.

A further approach to minimizing the termination peak electric fields is described
10 below with respect to Figures 6A, 6B, and 6C. Figure 6A presents a top plan view of an exemplary transistor having a drain termination enabling increased breakdown voltage, in accordance with an implementation of the present disclosure. The portion of transistor 600 shown in Figure 6A can correspond to the portion of transistor 200 labeled with bracket 6A in Figure 2. Figures 6B and 6C present cross-sectional views of exemplary
15 transistors, in accordance with an implementation of the present disclosure. The cross-sectional views in Figures 6B and 6C can correspond to cross-section 6-6 in Figure 6A in different implementations of the present disclosure.

Transistor 600 includes drain finger electrodes 620 and source finger electrode 610 corresponding respectively to drain finger electrodes 220 and source finger electrode 210
20 in Figure 2. Transistor 600 also includes gate region 609 corresponding to gate region 209 in Figure 2.

Similar to transistor 200, drain finger electrodes 620 are interdigitated with source

finger electrodes 610. Drain finger electrodes 620 and source finger electrodes 610 are situated in, on, or above (or a combination thereof, i.e., non-coplanar) semiconductor substrate 672. Semiconductor substrate 672 can be, for example, a III-Nitride material stack, such as a HEMT material stack, silicon, and/or other semiconductor material.

5 Current conduction paths, such as current conduction path 670, are in semiconductor substrate 672 between drain finger electrodes 620 and source finger electrodes 610. Gate region 609 is configured to control current conduction in semiconductor substrate 672 through the current conduction paths between drain finger electrodes 620 and source finger electrodes 610.

10 Also in transistor 600, drain finger electrodes 620 have drain finger electrode main bodies 624 and drain finger electrode ends 626 (e.g. curved drain finger electrode ends 626) corresponding respectively to drain finger electrode main bodies 224 and drain finger electrode ends 226 in Figure 2. Source finger electrodes 610 have source finger electrode main bodies 614 and source finger electrode ends (not shown in Figure 6A) corresponding respectively to source finger electrode main bodies 214 and source finger electrode ends 216 in Figure 2. In some implementations, drain finger electrode main bodies 624 are coplanar with drain finger electrode ends 626 as described by Figure 6B. In other implementations, drain finger electrode main body 624 is non-coplanar with at least a portion of drain finger electrode end 626 as described by Figure 6C.

20 Referring to Figure 6B, drain finger electrode 620a is shown having drain finger electrode main body 624a and drain finger electrode end 626a. Drain finger electrode 620a is situated on semiconductor substrate 672. In particular, drain finger electrode

main body 624a and drain finger electrode end 626a are both situated on semiconductor substrate 672 and are coplanar. Any or all of drain fingers electrodes 620 in transistor 600 can have a similar cross-section as shown in Figure 6B. However, by configuring any or all of drain fingers electrodes 620 in accordance with the implementation shown in
5 Figure 6C, termination electric fields, which may develop during operation, particularly at drain finger electrode ends 626, can be further eased.

Referring now to Figure 6C, drain finger electrode 620b is shown having drain finger electrode main body 624b and drain finger electrode end 626b. Drain finger electrode 620b is situated on semiconductor substrate 672. In particular, drain finger
10 electrode main body 624b is situated on semiconductor substrate 672. However, dielectric material 674 is situated between at least portion of drain finger electrode end 626b and semiconductor substrate 672. Drain finger electrode end 626b is formed over dielectric material 674 and over semiconductor substrate 672 such that at least a portion of drain finger electrode end 626b is non-coplanar with drain finger electrode main body
15 624b. Furthermore, dielectric material 674 insulates drain finger electrode end 626b from semiconductor substrate 672 thereby further easing termination electric fields, which may develop at drain finger electrode end 626b. Thus, transistor 600 can have an even higher breakdown voltage and a lower on-resistance when using the drain finger termination topology shown in Figure 6C.

20 Examples of dielectric material 674 include one or more dielectrics, such as any combination of silicon nitride, silicon oxide, oxynitride, or other insulating material. In certain implementations, dielectric material 674 includes tetraethyl orthosilicate (TEOS).

The dielectrics may be provided in layers, such as in a dielectric stack, or may be provided by a combination of similar or dissimilar materials.

In some implementations, dielectric material 674 is of a substantially uniform thickness. However, in the implementation shown in Figure 6C, dielectric material 674 is an increasing thickness dielectric material. By configuring the thickness of dielectric material 674, the easing of the termination electric fields can be controlled, for example, by gradually increasing the insulation thickness along the length of drain finger electrode end 626b between drain finger electrode end 626b and semiconductor substrate 672.

Dielectric material 674 may be situated at least partially in semiconductor substrate 672. For example, dielectric material 674 may be situated in a trench in semiconductor substrate 672. However, in the present implementation, dielectric material 674 is situated on and over semiconductor substrate 672. In doing so, drain finger electrode end 626b has increased elevation 676 and is non-coplanar relative to drain finger electrode main body 624b. Increased elevation 676 increases with the increasing thickness of dielectric material 674.

Thus, Figures 6A and 6B present another approach, which can be utilized to enhance performance of a semiconductor device, such as a transistor or a diode. As such, this approach may be applied to a device such as transistor 100 in Figure 1 without utilizing other approaches described herein. Alternatively, any the aforementioned approaches can be employed. For example, as shown in Figure 6A, any of drain finger electrodes ends 626 can have an increased radius of curvature. Furthermore, any of drain finger electrode ends 626 can extend beyond any of source finger electrode main bodies

614, as shown. Also, any of drain finger electrode ends 626 can be a tapered drain finger electrode (not shown in Figure 6A).

In accordance with various implementations disclosed by the present application, termination electric fields at drain finger electrode ends can be reduced. As a result,
 5 disclosed implementations achieve an increased breakdown voltage. The implementations disclosed herein can achieve the increased breakdown voltage while concurrently maintaining a low specific ON-resistance (on-resistance in the active area) through a shorter source-to-drain half pitch.

From the above description it is manifested that various techniques can be used for
 10 implementing the concepts described in the present application without departing from the scope of those concepts. Moreover, while the concepts have been described with specific reference to certain implementations, a person of ordinary skill in the art would recognize that changes can be made in form and detail without departing from the scope of those concepts. As such, the described implementations are to be considered in all
 15 respects as illustrative and not restrictive. It should also be understood that the present application is not limited to the particular implementations described above, but many rearrangements, modifications, and substitutions are possible without departing from the scope of the present disclosure.

CLAIMS

1. A transistor comprising:

drain finger electrodes interdigitated with source finger electrodes;

current conduction paths in a semiconductor substrate between said drain finger

5 electrodes and said source finger electrodes;

at least one of said drain finger electrodes having a drain finger electrode main

body and a drain finger electrode end, wherein at least a portion of said drain finger end is

non-coplanar with said drain finger electrode main body.

10 2. The transistor of claim 1, wherein a dielectric material is situated between
said drain finger electrode end and said semiconductor substrate.

3. The transistor of claim 2, wherein said dielectric material elevates said drain
15 finger electrode end over said semiconductor substrate.

4. The transistor of claim 1, wherein said drain finger electrode main body is
situated on said semiconductor substrate.

20 5. The transistor of claim 1, wherein said drain finger electrode end has an
increased radius of curvature.

6. The transistor of claim 1, wherein at least one of said source finger electrodes has a source finger electrode main body coupled to a source pad, said drain finger electrode end extending beyond said source finger electrode main body.

5 7. The transistor of claim 1, wherein said drain finger electrodes are longer than said source finger electrodes.

8. The transistor of claim 1, wherein said transistor is a high-electron-mobility transistor (HEMT).

10

9. The transistor of claim 1, wherein said transistor comprises a group III-V transistor.

10. A transistor comprising:

15 drain finger electrodes and source finger electrodes situated on a semiconductor substrate;

said drain finger electrodes interdigitated with source finger electrodes;

a gate region configured to control current conduction in said semiconductor substrate between said drain finger electrodes and said source finger electrodes;

20 at least one of said drain finger electrodes having a drain finger electrode main body and a drain finger electrode end having an increased elevation relative to said drain finger electrode main body.

11. The transistor of claim 10, wherein a dielectric material provides said increased elevation of said drain finger electrode end relative to said drain finger electrode main body.

5

12. The transistor of claim 10, wherein said drain finger electrode end has an increased radius of curvature.

13. The transistor of claim 10, wherein at least one of said source finger electrodes has a source finger electrode main body coupled to a source pad, said drain finger electrode end extending beyond said source finger electrode main body.

15

14. The transistor of claim 10, wherein said drain finger electrodes are longer than said source finger electrodes.

15. The transistor of claim 10, wherein said drain finger electrode end has an increased width relative to a width of said drain finger electrode main body.

16. A transistor comprising:
20 drain finger electrodes interdigitated with source finger electrodes;
a gate region configured to control current conduction in a semiconductor substrate between said drain finger electrodes and said source finger electrodes;

at least one of said drain finger electrodes having a drain finger electrode end and a drain finger electrode main body, wherein at least a portion of said drain finger end is non-coplanar with said drain finger electrode main body;

wherein an increasing thickness dielectric material is situated between at least said
5 portion of said drain finger electrode end and said semiconductor substrate.

17. The transistor of claim 16, wherein said increasing thickness dielectric material elevates said drain finger electrode end over said semiconductor substrate.

10 18. The transistor of claim 16, wherein said drain finger electrode end is substantially an ellipsoid.

19. The transistor of claim 16, wherein said drain finger electrode is a tapered drain finger electrode.

15

20. The transistor of claim 16, wherein said transistor is a high-electron-mobility transistor (HEMT).

ABSTRACT

According to an exemplary implementation, a transistor includes drain finger electrodes interdigitated with source finger electrodes. The transistor also includes a current conduction path in a semiconductor substrate between the drain finger electrodes and the source finger electrodes. At least one of the drain finger electrodes has a drain finger electrode end and a drain finger electrode main body, where the drain finger electrode main body is non-coplanar with at least a portion of the drain finger electrode end. The transistor may also include a dielectric material situated between at least a portion of the drain finger electrode end and the semiconductor substrate. The dielectric material can be an increasing thickness dielectric material. The dielectric material can thus elevate the drain finger electrode end over the semiconductor substrate. Further, the drain finger electrode end can have an increased radius of curvature.

FIG. 1

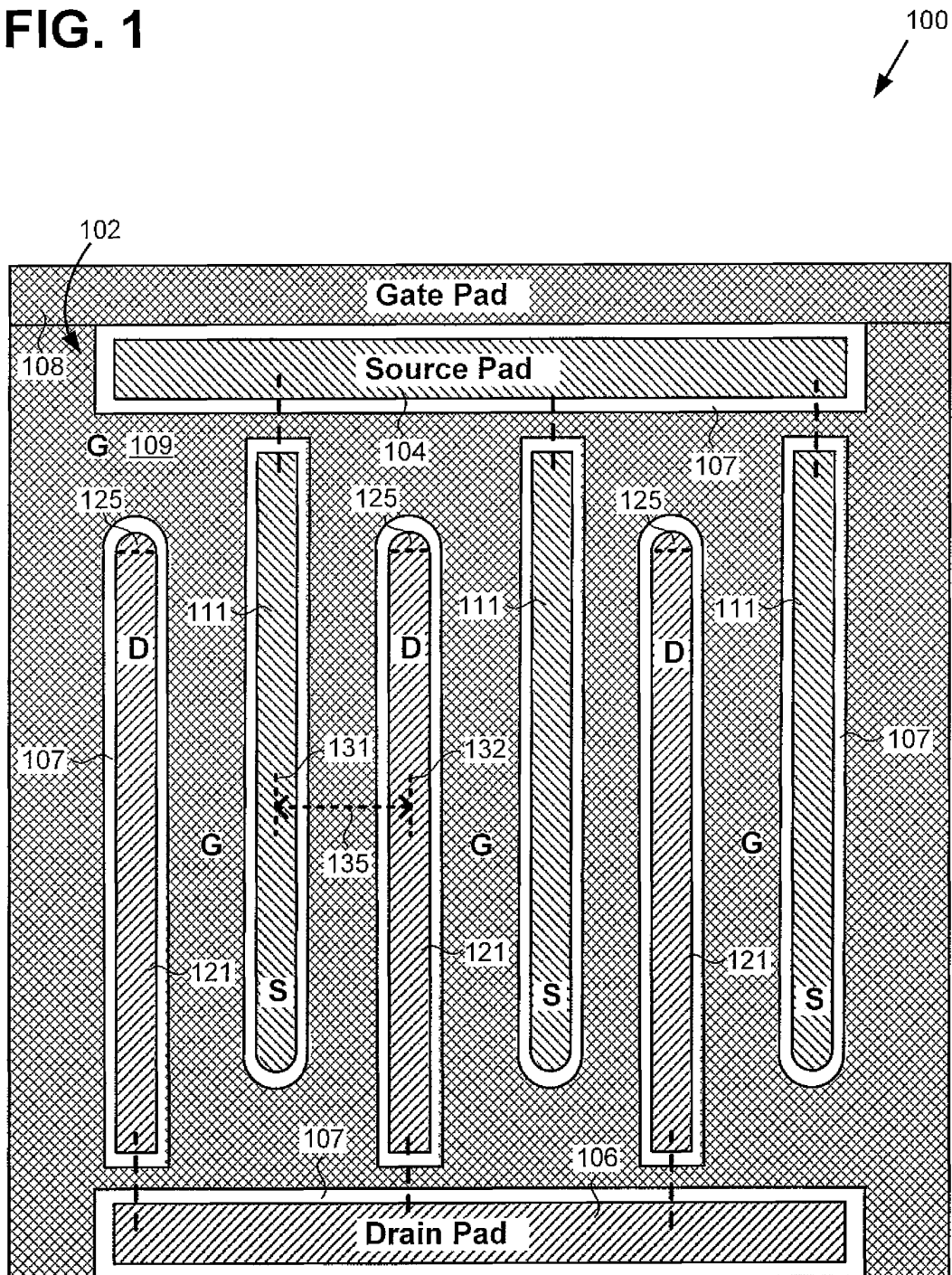


FIG. 2

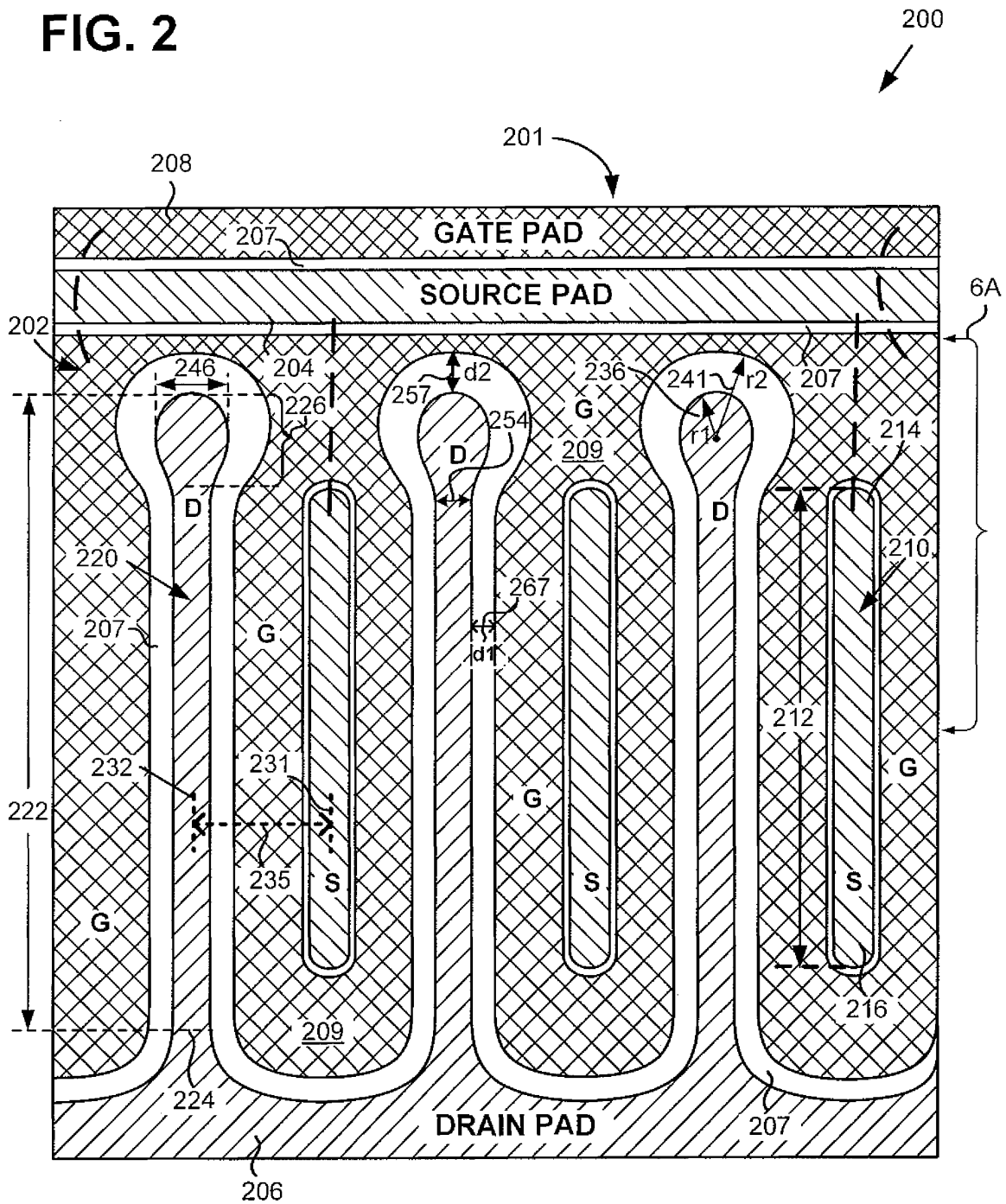


FIG. 3A

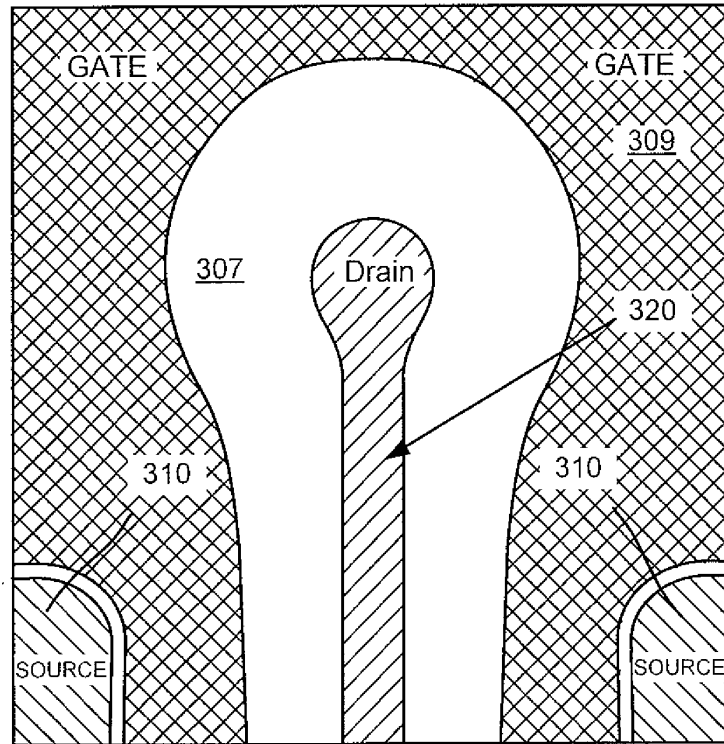


FIG. 3B

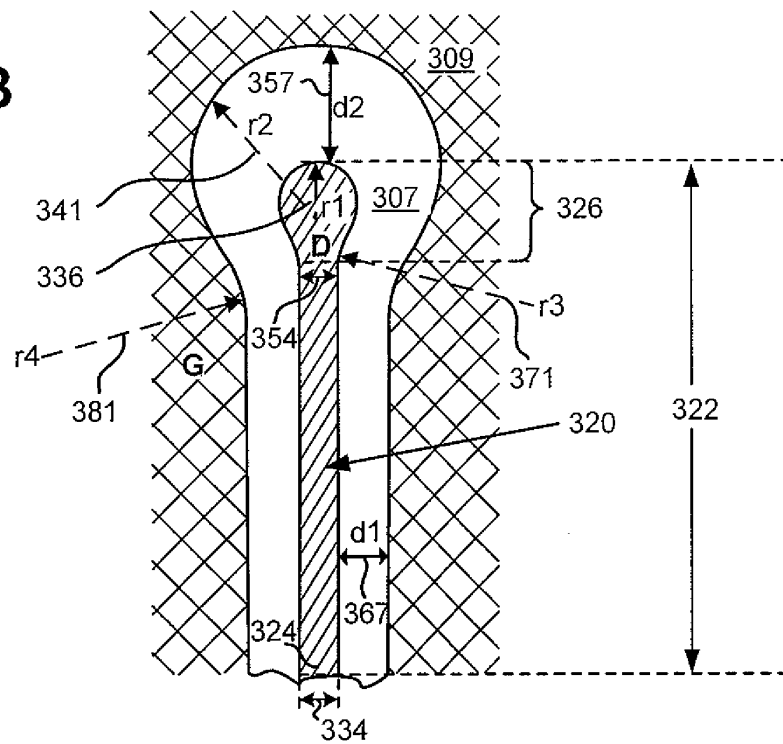


FIG. 4

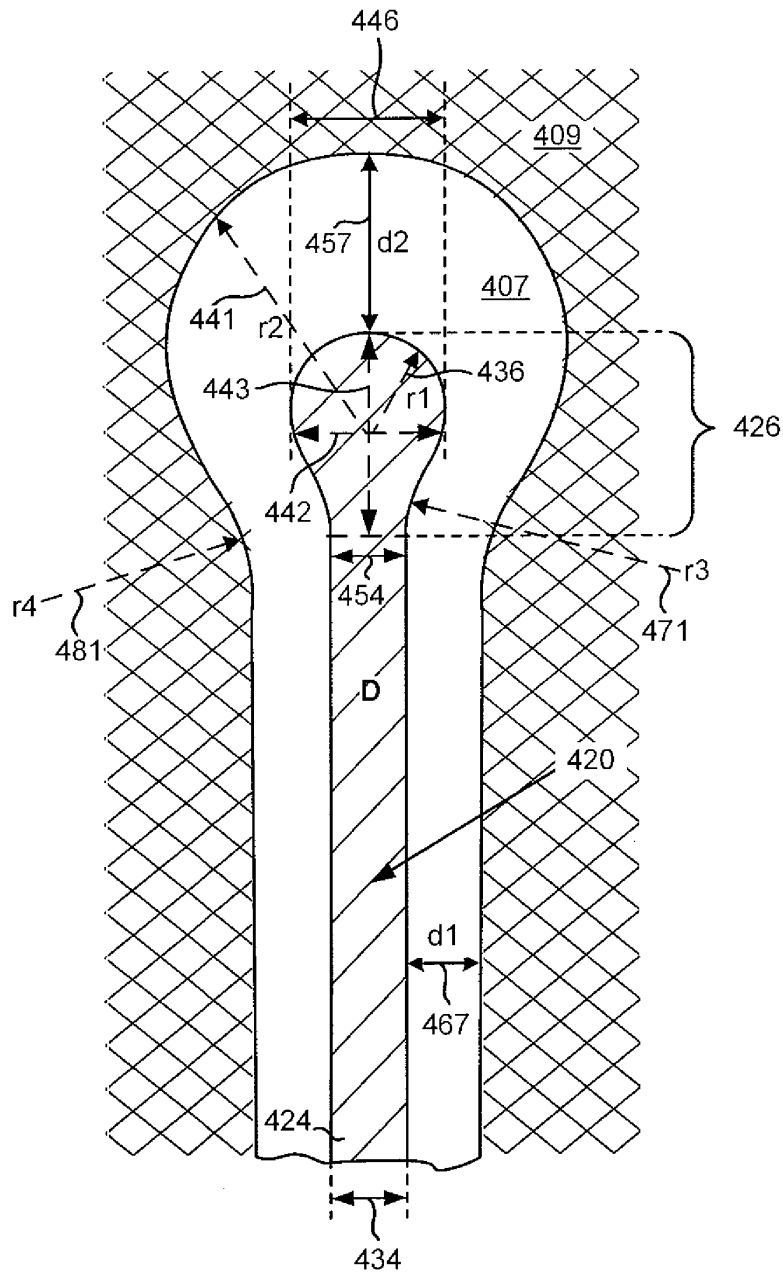


FIG. 5

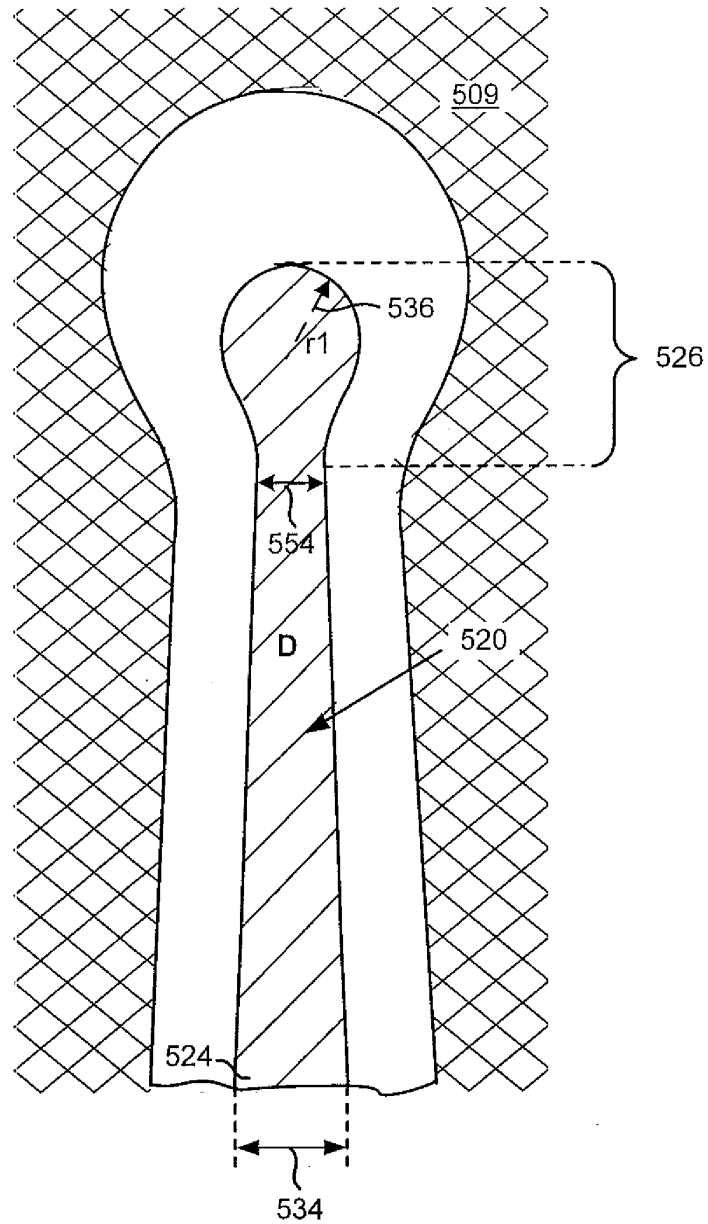


FIG. 6A

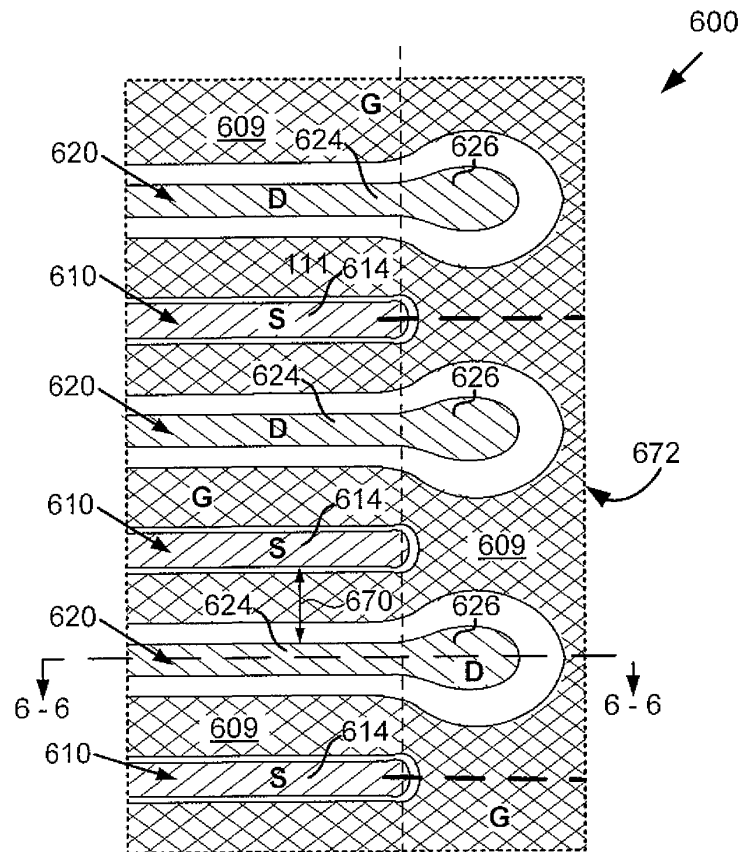


FIG. 6B

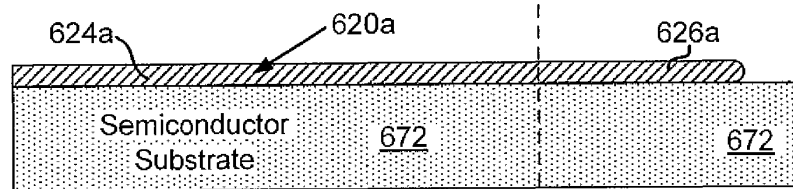
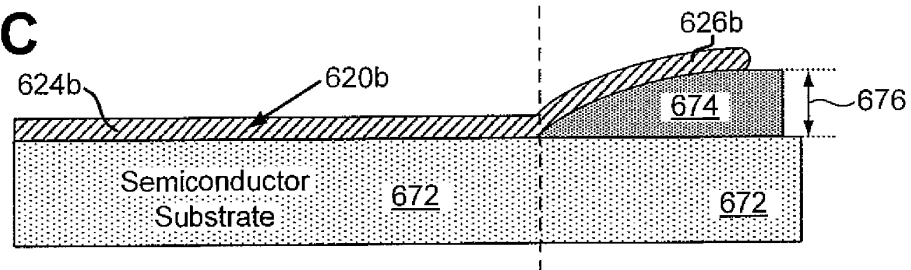


FIG. 6C



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Attorney Docket No.: 0400726D1

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: **Briere et al.**

Art Unit: 2897

Serial No.: 14/750,262

Examiner: Menz, Douglas M.

Filing Date: 06/25/2015

For: **Transistor with Elevated
Drain Termination**

AMENDMENT AND RESPONSE TO NON-FINAL OFFICE ACTION

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This is in response to the Non-Final Office Action dated October 5, 2015 in the above-referenced patent application. Please enter and consider the following amendments and remarks.

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.

Attorney Docket No.: 0400726D1

In the Claims:

Claims 1-9 (canceled)

Claim 10 (currently amended): A transistor comprising:

drain finger electrodes and source finger electrodes situated on a semiconductor substrate;

said drain finger electrodes interdigitated with source finger electrodes;

a gate region configured to control current conduction in said semiconductor substrate between said drain finger electrodes and said source finger electrodes;

at least one of said drain finger electrodes having a drain finger electrode main body and a drain finger electrode end having an increased elevation relative to said drain finger electrode main body;

wherein a dielectric material insulates said drain finger electrode end from said semiconductor substrate.

Claim 11 (currently amended): The transistor of claim 10, wherein said [[a]] dielectric material provides said increased elevation of said drain finger electrode end relative to said drain finger electrode main body.

Attorney Docket No.: 0400726D1

Claim 12 (original): The transistor of claim 10, wherein said drain finger electrode end has an increased radius of curvature.

Claim 13 (original): The transistor of claim 10, wherein at least one of said source finger electrodes has a source finger electrode main body coupled to a source pad, said drain finger electrode end extending beyond said source finger electrode main body.

Claim 14 (original): The transistor of claim 10, wherein said drain finger electrodes are longer than said source finger electrodes.

Claim 15 (original): The transistor of claim 10, wherein said drain finger electrode end has an increased width relative to a width of said drain finger electrode main body.

Claims 16-20 (canceled)

Claim 21 (previously presented): The transistor of claim 10, wherein said drain finger electrode main body is situated on said semiconductor substrate.

Claim 22 (previously presented): The transistor of claim 10, wherein said transistor is a high-electron-mobility transistor (HEMT).

Attorney Docket No.: 0400726D1

Claim 23 (previously presented): The transistor of claim 10, wherein said transistor comprises a group III-V transistor.

Claim 24 (previously presented): The transistor of claim 10, wherein said drain finger electrode end is substantially an ellipsoid.

Claim 25 (previously presented): The transistor of claim 10, wherein said drain finger electrode is a tapered drain finger electrode.

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REMARKS

Prior to the present amendment and response, claims 10-15 and 21-25 were pending in the present application. By the present response, Applicants have amended claims 10 and 11. Thus, claims 10-15 and 21-25 remain in the present application.

A. Rejection of Claims 10, 11, 13, 14, and 21 under 35 U.S.C. §102(b)

The Non-Final Office Action dated October 5, 2015 (hereinafter "Office Action") rejects claims 10, 11, 13, 14, and 21 under pre-AIA 35 U.S.C. §102(b) over U.S. Patent Application Publication Number 2006/0071304 by Jagannathan et al. (hereinafter "Jagannathan"). *See* pages 2-3 of the Office Action.

As stated in the original disclosure filed by Applicants, the present application is directed to transistors having reduced electric field terminations at drain finger electrode ends, thereby resulting in those transistors advantageously having an increased breakdown voltage. *See, e.g.*, page 25, lines 3-5 of the present application. Referring, for example, to figures 6A and 6C of the present application, such a transistor includes drain finger electrodes (e.g., drain finger electrodes 620) and source finger electrodes (e.g., source finger electrodes 610) situated on a semiconductor substrate (e.g., semiconductor substrate 672). *See id.* at page 22, lines 1-3. In addition, the transistor includes a gate region (e.g., gate region 609) configured to control current conduction in the semiconductor substrate between the drain finger electrodes and the source finger electrodes. *See id.* at lines 6-9.

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As taught by Applicants, at least one of the drain finger electrodes has a drain finger electrode main body (e.g., drain finger electrode main body 624b) and a drain finger electrode end having an increased elevation relative to the drain finger electrode main body (e.g., drain finger electrode end 626b having increased elevation 676 relative to the drain finger electrode main body 624b). *See id.* at page 24, lines 12-14. Moreover, and as further taught by Applicants, a dielectric material (e.g., dielectric material 674) is situated between the drain finger electrode end and the semiconductor substrate so as to insulate the drain finger electrode end from the semiconductor substrate. *See id.* at page 23, lines 12-17.

Independent claim 10 is currently amended to emphasize the features disclosed by Applicants and described above. *See* currently amended independent claim 10, above. Specifically, independent claim 10 is currently amended to recite, in part “wherein a dielectric material insulates said drain finger electrode end from said semiconductor substrate.” In addition, claim 11 is currently amended to harmonize its recitation with the changes introduced herein to independent claim 10. As noted above, support for the current amendments can be found at least at page 23, lines 12-17 of the present application.

In applying the present ground for rejection over Jagannathan, the Office Action asserts that Figure 5 of Jagannathan discloses a feature corresponding to the dielectric material disclosed and claimed by Applicants. *See* page 3 of the Office Action, referring to claim 11. However, it is noted that the Office Action fails to identify any specific

Attorney Docket No.: 0400726D1

feature shown in or described by reference to Figure 5 of Jagannathan as embodying such a disclosure of the dielectric material. Moreover, a review of Jagannathan reveals no support for the bare assertion in the Office Action that such a dielectric material is taught or even suggested by Jagannathan.

For example, the Office Action interprets the feature identified by reference number 318 (top portion) in Figure 5 of Jagannathan as corresponding to the drain finger electrode end disclosed and claimed by Applicants. *See* page 3, second paragraph of the Office Action. Referring to Jagannathan, according to the express teaching provided by that art reference, “drain contact 318 is connected to drain finger 306 with a metal contact 334.” *See* paragraph [0022] of Jagannathan. Jagannathan further states: “The drain fingers 306 and source fingers 308 include N⁺ wells, 330 and 328, respectively.” *Id.* However, highly conductive N type well 330, to which drain contact 318 is connected by metal contact 334, is formed in substrate 304. As a result, Applicants respectfully assert that Jagannathan cannot be reasonably interpreted to teach or suggest “wherein a dielectric material insulates said drain finger electrode end from said semiconductor substrate,” as affirmatively required by currently amended independent claim 10.

Thus, Applicants respectfully submit that currently amended independent claim 10 is patentably novel and inventive over Jagannathan. As such, claims 11, 13, 14, and 21 depending from and further limiting patentable independent claim 10 are also patentably novel and inventive over Jagannathan for at least the reasons discussed above.

Attorney Docket No.: 0400726D1

B. Rejection of Claims 22 and 23 under 35 U.S.C. §103(a)

The Office Action rejects claims 22 and 23 under pre-AIA 35 U.S.C. §103(a) over Jagannathan. *See* page 4 of the Office Action. However, as discussed above, Applicants respectfully assert that currently amended independent claim 10 is patentably novel and inventive over Jagannathan. As such, claims 22 and 23 depending from and further limiting patentable independent claim 10 are also patentably novel and inventive over Jagannathan for at least the reasons discussed above.

C. Rejection of Claims 12, 15, 24, and 25 under 35 U.S.C. §103(a)

The Office Action rejects claims 12, 15, 24, and 25 under pre-AIA 35 U.S.C. §103(a) over Jagannathan in view of U.S. Patent Application Publication Number 2004/0178443 by Hossain et al. (hereinafter "Hossain"). *See* page 5 of the Office Action. However, as discussed above, Applicants respectfully assert that currently amended independent claim 10 is patentably distinguishable over Jagannathan. As such, claims 12, 15, 24, and 25 depending from and further limiting patentable independent claim 10 are also patentably distinguishable over Jagannathan, as well as over Jagannathan in combination with any other cited reference, such as Hossain, for at least the reasons discussed above.

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D. Conclusion

Based on the foregoing reasons, Applicants respectfully submit that independent claim 10 and all claims depending therefrom, are patentably novel and inventive.

Moreover, Applicants assert that no new matter has been introduced herein. Accordingly,

Applicants respectfully request an early allowance of claims 10-15 and 21-25.

Attorney Docket No.: 0400726D1

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.

Respectfully Submitted,
FARJAMI & FARJAMI LLP

Date: Jan. 5, 2016



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Reg. No. 38,135

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Name of Person Performing Facsimile Transmission

Azin Bakhtiari 1/5/16
Signature Date



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FACSIMILE TRANSMISSION COVER SHEET

Date: January 5, 2016
To: United States Patent and Trademark Office
Examiner: Menz, Douglas M.; Art Unit: 2897
Fax: (571) 273-8300
Re: **Application Serial No.: 14/750,262**
Filing Date: 6/25/2015; First-Named Inventor: Briere
Attorney Docket No.: 0400726D1
From: Farjami & Farjami LLP

Number of pages including the cover sheet: 11

Message:

Enclosed please find the Amendment and Response to Non-Final Office Action dated October 5, 2015.

Authorization is hereby given to the Commissioner to charge any fees associated with this communication or credit any overpayment to Deposit Account **50-0731**.

Thank you.

The documents accompanying this facsimile contain PRIVILEGED AND CONFIDENTIAL information intended only for use of the individual or entity named above. If you are not the intended recipient, disclosure, copying, distribution or use of the contents of this facsimile information is prohibited. If you have received this facsimile in error, please immediately notify us by telephone and return the original facsimile to us at the above address via U.S. Postal Service. We will reimburse you for all expenses incurred.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/750,262	06/25/2015	Michael A. Briere	0400726D1	1059
25700 7590 03/28/2016 FARJAMI & FARJAMI LLP 26522 LA ALAMEDA AVENUE, SUITE 360 MISSION VIEJO, CA 92691			EXAMINER MENZ, DOUGLAS M	
			ART UNIT	PAPER NUMBER
			2897	
			NOTIFICATION DATE	DELIVERY MODE
			03/28/2016	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketing@farjami.com
farjamidocketing@yahoo.com
ffarjami@farjami.com

Office Action Summary	Application No. 14/750,262	Applicant(s) BRIERE ET AL.	
	Examiner DOUGLAS MENZ	Art Unit 2897	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 1/5/16.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) ☒ Claim(s) 10-15 and 21-25 is/are pending in the application.
5a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) ____ is/are allowed.
- 7) ☒ Claim(s) 10-15 and 21-25 is/are rejected.
- 8) ☐ Claim(s) ____ is/are objected to.
- 9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☒ The drawing(s) filed on 6/25/15 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some** c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) ☒ Notice of References Cited (PTO-892) | 3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date ____. | 4) ☐ Other: ____. |

DETAILED ACTION

The present application is being examined under the pre-AIA first to invent provisions.

Claim Rejections - 35 USC § 102

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 10, 11, 13, 14 and 21 are rejected under pre-AIA 35 U.S.C. 102b as being anticipated by Fujishima et al. (US 5523599).

Regarding claim 10, Fujishima discloses a transistor comprising:

drain finger electrodes (113, Fig. 6b) and source finger electrodes (112, Fig. 6b) situated on a semiconductor substrate;

said drain finger electrodes interdigitated with source finger electrodes (Figs. 6, 8 and Col. 15);

a gate region (111, Fig. 6b) configured to control current conduction in said semiconductor substrate between said drain finger electrodes and said source finger electrodes (Figs. 6, 8 and Col. 15);

at least one of said drain finger electrodes having a drain finger electrode main body (113 *portion directly on substrate*, Fig. 6a) and a drain finger electrode end having an increased elevation (113 *portion on dielectric 115*, Fig. 6a) relative to said drain finger electrode main body;

wherein a dielectric material (115, Fig. 6b) insulates said drain finger electrode end from the semiconductor substrate (Col. 8, line: 60 – Col. 9, line: 5).

Regarding claim 11, Fujishima further discloses wherein the dielectric material (115, Fig. 6b) provides said increased elevation of said drain finger electrode end (113 *portion on dielectric 115*, Fig. 6a) relative to said drain finger electrode main body (113 *portion directly on substrate*, Fig. 6a).

Regarding claim 13, Fujishima further discloses wherein at least one of said source finger electrodes (112, Fig. 6b) has a source finger electrode main body coupled to a source pad (Fig. 6b), said drain finger electrode end extending beyond said source finger electrode main body (Figs. 6b, 8).

Regarding claim 14, Fujishima further discloses wherein said drain finger electrodes are longer than said source finger electrodes (Fig. 8).

Regarding claim 21, Fujishima further discloses wherein said drain finger electrode main body is situated on said semiconductor substrate (Fig. 6b).

Claim Rejections - 35 USC § 103

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 22-23 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Fujishima et al. (US 5523599).

Regarding claims 22-23, Fujishima discloses the transistor of claim 10 as mentioned above. Fujishima does not explicitly disclose wherein the transistor is a high- electron-mobility transistor or a group III-V transistor. However, such transistor

classes are well known in the art and it would have been obvious to one of ordinary skill in the art to incorporate such into Fujishima's teachings.

Claims 12, 15 and 24-25 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Fujishima et al. (US 5523599) in view of Hossain et al. (US 2004/0178443).

Regarding claims 12, 15 and 24-25, Fujishima discloses the transistor of claim 10 as mentioned above. Fujishima does not explicitly disclose the drain finger electrode configurations of claims 12, 15 and 24-25. Hossain discloses interdigitated source/drain finger transistors with curved, taper, and other variations for the purpose of providing higher voltage breakdown of the transistor (Abstract, Figs. 2,4,5 and paragraphs 0004-0005, 0027-0047). It would have been obvious to one of ordinary skill in the art at the time of the invention to alter the shape of the drain finger terminations of Fujishima's device as taught by Hossain because Hossain explicitly discloses such shapes provide higher voltage breakdown of the transistor.

Response to Arguments

Applicant's arguments with respect to the claims have been considered but are moot because the arguments do not apply to any of the references being used in the current rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DOUGLAS MENZ whose telephone number is (571)272-1877. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fernando Toledo can be reached on 571-272-1867. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/DOUGLAS MENZ/
Primary Examiner, Art Unit 2897
3/18/16

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JUN 15 2016

Attorney Docket No.: 0400726D1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: **Briere et al.**

Art Unit: 2897

Serial No.: 14/750,262

Examiner: Menz, Douglas M.

Filing Date: 06/25/2015

For: **Transistor with Elevated
Drain Termination**

AMENDMENT AND RESPONSE TO FINAL OFFICE ACTION

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This is in response to the Final Office Action dated March 28, 2016 in the above-referenced patent application. Please enter and consider the following amendment and remarks.

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No.

50-0731.

Attorney Docket No.: 0400726D1

In the Claims:

Claims 1-9 (canceled)

Claim 10 (currently amended): A transistor comprising:

drain finger electrodes and source finger electrodes situated on a semiconductor substrate, said drain finger electrodes coupled to a drain pad, said source finger electrodes coupled to a source pad;

said drain finger electrodes interdigitated with said source finger electrodes, said drain finger electrodes extending beyond said source finger electrodes so as to be situated closer to said source pad than said source finger electrodes;

a gate region configured to control current conduction in said semiconductor substrate between said drain finger electrodes and said source finger electrodes;

at least one of said drain finger electrodes having a drain finger electrode main body and a drain finger electrode end having an increased elevation relative to said drain finger electrode main body;

wherein a dielectric material insulates said drain finger electrode end from said semiconductor substrate.

Attorney Docket No.: 0400726D1

Claim 11 (previously presented): The transistor of claim 10, wherein said dielectric material provides said increased elevation of said drain finger electrode end relative to said drain finger electrode main body.

Claim 12 (original): The transistor of claim 10, wherein said drain finger electrode end has an increased radius of curvature.

Claim 13 (original): The transistor of claim 10, wherein at least one of said source finger electrodes has a source finger electrode main body coupled to a source pad, said drain finger electrode end extending beyond said source finger electrode main body.

Claim 14 (original): The transistor of claim 10, wherein said drain finger electrodes are longer than said source finger electrodes.

Claim 15 (original): The transistor of claim 10, wherein said drain finger electrode end has an increased width relative to a width of said drain finger electrode main body.

Claims 16-20 (canceled)

Attorney Docket No.: 0400726D1

Claim 21 (previously presented): The transistor of claim 10, wherein said drain finger electrode main body is situated on said semiconductor substrate.

Claim 22 (previously presented): The transistor of claim 10, wherein said transistor is a high-electron-mobility transistor (HEMT).

Claim 23 (previously presented): The transistor of claim 10, wherein said transistor comprises a group III-V transistor.

Claim 24 (previously presented): The transistor of claim 10, wherein said drain finger electrode end is substantially an ellipsoid.

Claim 25 (previously presented): The transistor of claim 10, wherein said drain finger electrode is a tapered drain finger electrode.

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Attorney Docket No.: 0400726D1

JUN 15 2016

REMARKS

Prior to the present amendment and response, claims 10-15 and 21-25 were pending in the present application. By the present response, Applicants have amended independent claim 10. Thus, claims 10-15 and 21-25 remain in the present application. Applicants respectfully request reconsideration and allowance of pending claims 10-15 and 21-25 in view of the above amendment and the following remarks.

At the outset, it is noted that in the Office Action dated March 28, 2016, the Examiner has *finally rejected* claims 10-15 and 21-25 on the basis of newly cited art. *See* pages 2-5 of the Final Office Action dated March 28, 2016. Applicants respectfully request reconsideration and withdrawal of the finality of the rejection of the Office Action dated March 28, 2016.

A good and sufficient reason why the present response is necessary and was not earlier presented is that a new reference has been cited in the present final rejection dated March 28, 2016. That new reference is U.S. Patent Number 5,523,599 to Fujishima et al. (hereinafter "Fujishima"). Because Fujishima is a new reference upon which the Examiner has now relied, Applicants believe that it would be manifestly unfair for the Patent Office not to withdraw the finality of the present rejection and not to consider Applicants' arguments which are necessitated due to the newly cited reference Fujishima. Consequently, Applicants respectfully submit that a good and sufficient reason exists, as contemplated by 37 CFR §1.116(c), for withdrawing the finality of the present rejection.

Attorney Docket No.: 0400726D1

A. Rejection of Claims 10, 11, 13, 14, and 21 under 35 U.S.C. §102(b)

The Final Office Action dated March 28, 2016 (hereinafter “Final Rejection”) rejects claims 10, 11, 13, 14, and 21 under pre-AIA 35 U.S.C. §102(b) over Fujishima. See pages 2-4 of the Office Action. For the reasons discussed below, Applicants respectfully assert that currently amended independent claim 10 is patentably novel and inventive over Fujishima.

Applicants have previously explained that the present application is directed to transistors having reduced electric field terminations at drain finger electrode ends, thereby resulting in those transistors advantageously having an increased breakdown voltage. See, e.g., page 25, lines 3-5 of the present application. Referring, for example, to figures 6A and 6C of the present application, such a transistor includes drain finger electrodes (e.g., drain finger electrodes 620) and source finger electrodes (e.g., source finger electrodes 610) situated on a semiconductor substrate (e.g., semiconductor substrate 672). See *id.* at page 22, lines 1-3.

Referring to Figure 2 in combination with figures 6A and 6C, Applicants disclose that the drain finger electrodes are coupled to a drain pad (e.g., drain pad 206), and the source finger electrodes are coupled to a source pad (e.g., source pad 204). See *id.* at page 12, lines 8-11, and page 21, lines 18-21. Applicants further disclose that the drain finger electrodes extend beyond the source finger electrodes so as to be situated closer to the source pad than are the source finger electrodes. See *id.* at page 13, line 19 through page 14, line 1, and page 21, lines 18-21. In addition, the transistor includes a gate region

Attorney Docket No.: 0400726D1

(e.g., gate region 609) configured to control current conduction in the semiconductor substrate between the drain finger electrodes and the source finger electrodes. *See id.* at page 22, lines 6-9.

As taught by Applicants, at least one of the drain finger electrodes has a drain finger electrode main body (e.g., drain finger electrode main body 624b) and a drain finger electrode end having an increased elevation relative to the drain finger electrode main body (e.g., drain finger electrode end 626b having increased elevation 676 relative to the drain finger electrode main body 624b). *See id.* at page 24, lines 12-14. Moreover, and as further taught by Applicants, a dielectric material (e.g., dielectric material 674) is situated between the drain finger electrode end and the semiconductor substrate so as to insulate the drain finger electrode end from the semiconductor substrate. *See id.* at page 23, lines 12-17.

Independent claim 10 is currently amended to emphasize the features disclosed by Applicants and described above. *See* currently amended independent claim 10, above. Specifically, independent claim 10 is currently amended to recite, in part, “said drain finger electrodes extending beyond said source finger electrodes so as to be situated closer to said source pad than said source finger electrodes.” *Id.* As noted above, support for the current amendment of independent claim 10 can be found at least at page 13, line 19 through page 14, line 1, and page 21, lines 18-21 of the present application.

In rejecting independent claim 1 of the present application over Fujishima, the Final Rejection states:

Attorney Docket No.: 0400726D1

Regarding claim 10, Fujishima discloses a transistor comprising: drain finger electrodes (113, Fig. 6b) and source finger electrodes (112, Fig. 6b) situated on a semiconductor substrate; said drain finger electrodes interdigitated with source finger electrodes (Figs. 6, 8 and Col. 15); a gate region (111, Fig. 6b) configured to control current conduction in said semiconductor substrate between said drain finger electrodes and said source finger electrodes (Figs. 6, 8 and Col. 15); at least one of said drain finger electrodes having a drain finger electrode main body (113 *portion directly on substrate*, Fig. 6a) and a drain finger electrode end having an increased elevation (113 *portion on dielectric 115*, Fig. 6a) relative to said drain finger electrode main body; wherein a dielectric material (115, Fig. 6b) insulates said drain finger electrode end from said semiconductor substrate (Col. 8, line 60 – Col. 9, line 5). *See* pages 2-3 of the Final Rejection, *italics* reproduced from the Final Rejection.

However, a review of Fujishima reveals that the implementations disclosed in figures 6a, 6b, and 8 of Fujishima and relied upon in the Final Rejection fail to disclose or suggest drain finger electrodes that extend beyond source finger electrodes so as to be situated closer to a source pad than are the source finger electrodes. *See, e.g.*, figures 6a, 6b, and 8, and related text in Fujishima. Moreover, no other implementation disclosed by Fujishima discloses or suggests such features. *See* Fujishima. Consequently, Applicants respectfully assert that Fujishima fails to teach or suggest “said drain finger electrodes extending beyond said source finger electrodes so as to be situated closer to said source pad than said source finger electrodes,” as affirmatively required by currently amended independent 10.

Thus, Applicants respectfully submit that currently amended independent claim 10 is patentably novel and inventive over Fujishima. As such, claims 11, 13, 14, and 21

Attorney Docket No.: 0400726D1

depending from and further limiting patentable independent claim 10 are also patentably novel and inventive over Fujishima for at least the reasons discussed above, and also for the additional limitations contained in the dependent claims.

B. Rejection of Claims 22 and 23 under 35 U.S.C. §103(a)

In the Final Rejection, the Examiner has rejected claims 22 and 23 under pre-AIA 35 U.S.C. §103(a) over Fujishima. *See* pages 4-5 of the Office Action. However, as discussed above, Applicants respectfully assert that currently amended independent claim 10 is patentably novel and inventive over Fujishima. As such, claims 22 and 23 depending from and further limiting patentable independent claim 10 are also patentably novel and inventive over Fujishima for at least the reasons discussed above, and also for the additional limitations in dependent claims 22 and 23.

C. Rejection of Claims 12, 15, 24, and 25 under 35 U.S.C. §103(a)

In the Final Rejection, the Examiner has rejected claims 12, 15, 24, and 25 under pre-AIA 35 U.S.C. §103(a) over Fujishima in view of U.S. Patent Application Publication Number 2004/0178443 by Hossain et al. (hereinafter "Hossain"). *See* page 5 of the Office Action. However, as discussed above, Applicants respectfully assert that currently amended independent claim 10 is patentably distinguishable over Fujishima. As such, claims 12, 15, 24, and 25 depending from and further limiting patentable independent claim 10 are also patentably distinguishable over Fujishima, as well as over Fujishima in

Attorney Docket No.: 0400726D1

combination with any other cited reference, such as Hossain, for at least the reasons discussed above, and also for the additional limitations contained in the dependent claims.

D. Conclusion

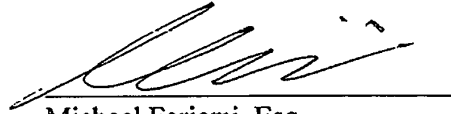
Based on the foregoing reasons, Applicants respectfully submit that independent claim 10 and all claims depending therefrom, are patentably novel and inventive. Moreover, Applicants assert that no new matter has been introduced herein. Accordingly, Applicants respectfully request an early allowance of claims 10-15 and 21-25.

Attorney Docket No.: 0400726D1

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.

Respectfully Submitted,
FARJAMI & FARJAMI LLP

Date: June 15, 2016


Michael Farjami, Esq.
Reg. No. 38,135

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CERTIFICATE OF FACSIMILE TRANSMISSION

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Azin Bakhtiarj
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FACSIMILE TRANSMISSION COVER SHEET

Date: June 15, 2016

To: United States Patent and Trademark Office
Examiner: Menz, Douglas M.; Art Unit: 2897

Fax: (571) 273-8300

Re: **Application Serial No.: 14/750,262**
Filing Date: 06/25/2015; First-Named Inventor: Briere
Attorney Docket No.: 0400726D1

From: Farjami & Farjami LLP

Number of pages including the cover sheet: 12

Message:

Enclosed please find the Amendment and Response to Final Office Action dated March 28, 2016.

Authorization is hereby given to the Commissioner to charge any fees associated with this communication or credit any overpayment to Deposit Account **50-0731**.

Thank you.

The documents accompanying this facsimile contain PRIVILEGED AND CONFIDENTIAL information intended only for use of the individual or entity named above. If you are not the intended recipient, disclosure, copying, distribution or use of the contents of this facsimile information is prohibited. If you have received this facsimile in error, please immediately notify us by telephone and return the original facsimile to us at the above address via U.S. Postal Service. We will reimburse you for all expenses incurred.

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PATENT APPLICATION FEE DETERMINATION RECORD				Application or Docket Number		Filing Date		☐ To be Mailed	
Substitute for Form PTO-875				14/750,262		06/25/2015			
ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO									
APPLICATION AS FILED – PART I									
(Column 1)		(Column 2)							
FOR	NUMBER FILED	NUMBER EXTRA		RATE (\$)		FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A					
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A					
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A					
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		X \$ =					
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		X \$ =					
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).								
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))									
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL					
APPLICATION AS AMENDED – PART II									
(Column 1)		(Column 2)		(Column 3)					
AMENDMENT	06/15/2016	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 11	Minus	** 20	= 0	X \$80 =		0	
	Independent (37 CFR 1.16(h))	* 1	Minus	***3	= 0	X \$420 =		0	
	☐ Application Size Fee (37 CFR 1.16(s))								
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
TOTAL ADD'L FEE						0			
(Column 1)		(Column 2)		(Column 3)					
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =			
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =			
	☐ Application Size Fee (37 CFR 1.16(s))								
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
TOTAL ADD'L FEE									
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.									

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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57579 7590 09/21/2016
MURPHY, BILAK & HOMILLER/INFINEON TECHNOLOGIES
1255 Crescent Green
Suite 200
CARY, NC 27518

EXAMINER

MENZ, DOUGLAS M

ART UNIT

PAPER NUMBER

2897

DATE MAILED: 09/21/2016

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/750,262	06/25/2015	Michael A. Briere	1012-1653 / 2012P80022 US	1059

TITLE OF INVENTION: Transistor with Elevated Drain Termination

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	12/21/2016

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**
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CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

57579 7590 09/21/2016

MURPHY, BILAK & HOMILLER/INFINEON TECHNOLOGIES
1255 Crescent Green
Suite 200
CARY, NC 27518

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/750,262	06/25/2015	Michael A. Briere	1012-1653 / 2012P80022 US	1059

TITLE OF INVENTION: Transistor with Elevated Drain Termination

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	12/21/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS
MENZ, DOUGLAS M	2897	257-192000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/750,262	06/25/2015	Michael A. Briere	1012-1653 / 2012P80022	1059
57579 7590 09/21/2016 MURPHY, BILAK & HOMILLER/INFINEON TECHNOLOGIES 1255 Crescent Green Suite 200 CARY, NC 27518			US EXAMINER MENZ, DOUGLAS M	
			ART UNIT 2897	PAPER NUMBER

DATE MAILED: 09/21/2016

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/750,262	Applicant(s) BRIERE ET AL.	
	Examiner DOUGLAS MENZ	Art Unit 2897	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 9/6/16.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are 10-15,21-25. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some *c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|--|
| 1. ☐ Notice of References Cited (PTO-892) | 5. ☐ Examiner's Amendment/Comment |
| 2. ☐ Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date _____ | 6. ☒ Examiner's Statement of Reasons for Allowance |
| 3. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 7. ☐ Other _____. |
| 4. ☐ Interview Summary (PTO-413),
Paper No./Mail Date _____. | |

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DETAILED ACTION

The present application is being examined under the pre-AIA first to invent provisions.

Allowable Subject Matter

Claims 10-15 and 21-25 are allowed.

The following is an examiner's statement of reasons for allowance:

There is no teaching or suggestion in the art of record disclosing a transistor comprising interdigitated source/drain finger electrodes configured in accordance with the limitations of claim 10, wherein the drain finger electrodes extend beyond the source finger electrodes so as to be situated closer to the source pad than the source finger electrodes and wherein at least one drain finger electrode has a drain finger electrode main body and a drain finger electrode end having an increased elevation relative to the drain finger electrode main body. Therefore, independent claim 10 is deemed allowable along with its dependent claims 11-15 and 21-25.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DOUGLAS MENZ whose telephone number is (571)272-1877. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fernando Toledo can be reached on 571-272-1867. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/DOUGLAS MENZ/
Primary Examiner, Art Unit 2897
9/16/16