

precipitate precipitate-to-band carrier transport takes place [4], [5]. They were able to explain the room-temperature nonideal B - E characteristics. Now, to model their temperature dependence, a qualitative analysis can be made based on the transport mechanisms taking place in the micro-Schottky precipitates. At very low temperatures, a field-effect tunneling transport takes place between bands and precipitate. For this temperature range [7]

$$J = J_S \exp \left(\frac{qV_F}{E_{00}} \right) \quad (4)$$

where E_{00} is a constant and J_S depends weakly on temperature. That is, the slope of $\ln J$ versus V is a constant, temperature independent. If a double tunneling process is taking place

$$J = A \exp(BT) \exp \left(\frac{qV_F}{E_{00}} \right) \quad (5)$$

where A and B are temperature- and voltage-independent factors.

As temperature rises, thermally assisted tunneling tends to dominate [7]

$$J = J'_S \exp \left(\frac{qV_F}{E_0} \right) \quad (6)$$

where

$$E_0 = E_{00} \coth(E_{00}/kT) \quad (7)$$

and

$$J'_S \propto \frac{T}{k \cosh(E_{00}/kT)} \quad (8)$$

We show now that our experimental results fit the functional dependences indicated above. For the constant in I_{BNIS} - V slope range, from Fig. 2, a good fitting is found for

$$nkT = 26 \text{ meV}, \quad T < 200 \text{ K} \quad (9)$$

that should correspond to the field-assisted tunneling carrier transport described by (5). Then

$$nkT = E_{00} = 18.5 \times 10^{-12} \left[\frac{N}{m_r \epsilon_r} \right]^{1/2} \quad (10)$$

allowing to estimate the semiconductor doping concentration level involved in the tunneling processes. A value of $N \approx 10^{19} \text{ cm}^{-3}$ is found, indicating metallic micro-Schottky barriers are near the surface, at the lateral regions. For this temperature range, $T < T_0 = 200 \text{ K}$, a linear plot of $\ln I_{BNIS}$ versus T is found (Fig. 3), in agreement with (5).

At temperatures greater than T_0 , data in Fig. 2 can be fitted by

$$n = 1.2 + 3(300 - T)10^{-3}, \quad T > 200 \text{ K} \quad (11)$$

that would correspond to the transport situation described in (6). For this temperature range, computing $\ln \{ [I_{BNIS} \cosh(E_{00}/kT)]/T \}$ versus $1/E_0$ from the data in Fig. 3, a straight line is obtained, as predicted by (6), and its slope allows us to obtain the Schottky-barrier height, $\phi_B \approx 1 \text{ eV}$. This large value can be understood as due to the fact that the B - E junction field distorts the energy bands and really imposes the metal-silicon barrier height, as shown by Lefferts [4].

An interesting result is that, for all temperatures, the saturation nonideal base current shown in Fig. 3 can be described by

$$I_{BNIS} = C_1 \exp \left(\frac{C_2}{n} \right) \quad (12)$$

Specific values for C_1 and C_2 depend on processing runs, but for a large set of our devices (both small and large) we have found $C_1 = 1.2 \times 10^{-37} \text{ A}$ and $C_2 = 60$.

A good agreement is then found between the temperature dependence of the nonideal base current component and the recombination mechanisms predicted by metallic precipitates behaving as micro-Schottky barriers.

CONCLUSIONS

At low temperatures, base current in n-p-n Si transistors shows ideality factors greater than 2 in the beta roll-off region. This fact reveals the presence of non-S-R-H recombination centers. Considering that it is well established that, B - E reverse bias characteristics can be explained by the presence of metallic microprecipitates at the junction, in this work it has been shown that the functional temperature dependence of the nonideal forward bias base current component can also be accounted by such a model.

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Noise Associated with Distributed Resistance of MOSFET Gate Structures in Integrated Circuits

R. P. JINDAL

Abstract—The effect of thermal voltage fluctuations in a resistive gate matrix perpendicular to the direction of channel current, in a MOSFET, are treated in detail. A general formula is derived to arrive at channel current fluctuations for an arbitrary gate matrix layout. This formulation is an extension of the analysis done by Thorner and is valid for frequencies at which the distributed RC time constants associated with the gate matrix are not important. The results of this analysis can be used to design low-noise resistive gate structures.

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INTRODUCTION

Noise associated with distributed gate resistance of large IGFET's can be comparable or larger than low field channel thermal noise. The usual case of interest is one in which the gate thermal noise voltage fluctuations are perpendicular to the channel current direction. An analysis for this case, when the two ends of the resistive gate are held at a fixed potential, has been done before [1]. This special situation is, however, true only for limited cases. In the present formulation the boundary conditions have been relaxed to accommodate finite fluctuations at the two end points. Further, an expression is derived to account for the noise arising from several of these mutually interacting gates connected by resistive paths which themselves contribute to noise. This allows one to compare the relative noise contributions due to the resistive gates and the resistive interconnects, and hence optimize the layout. It also provides a means of assessing, in a quantitative manner, the technological trade-offs involved in choosing the gate and interconnect materials for a specific low-noise application consistent with other circuit constraints. The analysis is restricted to frequencies of interest up to which the input signal is not attenuated due to the distributed RC time constants associated with the gate matrix.

PROBLEM DESCRIPTION

Consider a layout for the gate structure shown in Fig. 1. The layout can be split into two parts. One part consists of all gate material lying over thin oxide and hence contributing to transistor action (active portion), and the other part consists of gate material lying over thick oxide and hence not contributing to transistor action (passive portion). Now, although the passive portions of the gate material matrix are distributed resistances, for noise calculation purposes we can treat them as lumped resistors since they manifest themselves only through their end points. We shall refer to them as interconnect resistors. The active gate portions do exhibit their true distributed nature and hence have to be treated separately. We shall refer to them as gate resistors.

Thus we can think of the layout as a matrix of gate and interconnect resistors connected to a dc potential at one or more points.

Note that from topological considerations, we limit ourselves to the case where the gate resistance noise voltage fluctuations lie in a direction transverse to the source-drain current flow direction.

CALCULATION OF INTERCONNECT RESISTOR NOISE

Consider a gate matrix with n gate resistances and m interconnect resistances. Further, consider the i th gate of width w_i lying along the x axis as shown in Fig. 2(a). Let the device transconductance

$$g_{m_i} = \int_0^{w_i} g_{m_{0_i}}(x'') dx'' \quad (1)$$

Also, let the gate resistance

$$R_i = \int_0^{w_i} R_{0_i}(x'') dx'' \quad (2)$$

Let there be a voltage fluctuation δV_j across the terminals of the j th interconnect resistor R_j and let $\delta V_{g_i}(0)$ and $\delta V_{g_i}(w_i)$ be the corresponding gate voltage fluctuations at the two ends

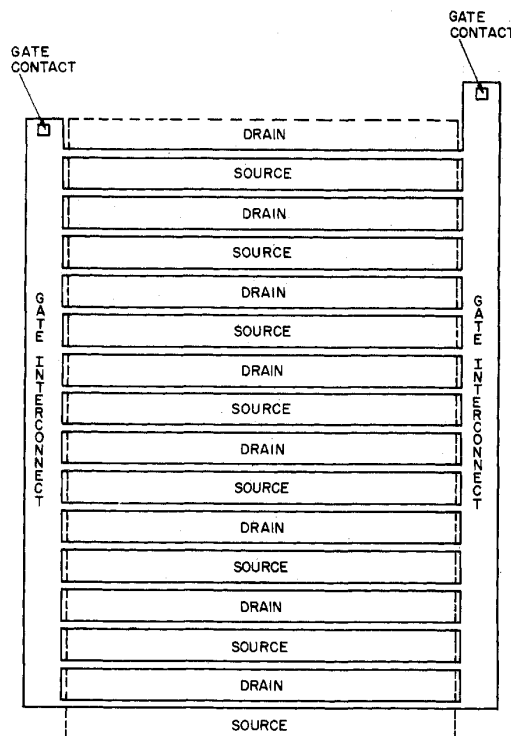


Fig. 1. A typical resistive gate matrix layout.

of the i th gate (see Fig. 2(b)). Then

$$\delta V_{g_i}(x) = [\delta V_{g_i}(w_i) - \delta V_{g_i}(0)] \frac{\int_0^x R_{0_i}(x'') dx''}{\int_0^{w_i} R_{0_i}(x'') dx''} + \delta V_{g_i}(0). \quad (3)$$

Also, from Nyquist's theorem [2] at low frequencies, we have

$$\overline{\delta V_j^2} = 4KTR_j\Delta f. \quad (4)$$

Then fluctuation in the i th channel current corresponding to δV_j is given by

$$\delta I_{dij} = \int_0^{w_i} g_{m_{0_i}}(x'') \delta V_{g_i}(x'') dx'' \quad (5)$$

$$= \overline{g_{m_{0_i}}} \cdot \overline{\delta V_{g_i}} \cdot w_i \quad (6)$$

where $\overline{}$ denotes a suitably defined average.

Defining $T_{V_{ij}}$, the transfer voltage fluctuation ratio, as

$$T_{V_{ij}} = \frac{\overline{\delta V_{g_i}}}{\delta V_j} \quad (7)$$

we have

$$\delta I_{dij} = w_i \cdot \overline{g_{m_{0_i}}} \cdot T_{V_{ij}} \cdot \delta V_j. \quad (8)$$

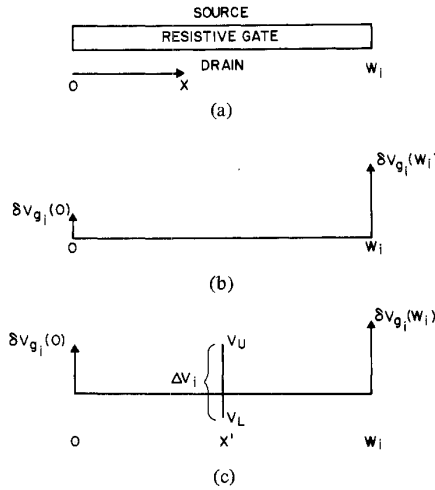


Fig. 2. (a) i th resistive gate; (b) fluctuations across the i th resistive gate due to noise fluctuations from other resistors, and (c) fluctuations across the i th resistor gate due to a noise fluctuation within itself.

Now, since δV_j produces correlated current fluctuation in all the n devices, we have

$$\delta I_{dj} = \sum_{i=1}^n (\bar{g}_{m0i} T_{Vij} w_i) \delta V_j \quad (9)$$

which gives from (4)

$$\overline{\delta I_{dj}^2} = \left\{ \sum_{i=1}^n (\bar{g}_{m0i} T_{Vij} w_i) \right\}^2 4KTR_j \Delta f. \quad (10)$$

Adding up the noise due to all the m interconnect resistors, we get

$$\overline{\delta I_d^2} = \sum_{j=1}^m \left\{ \sum_{i=1}^n (\bar{g}_{m0i} T_{Vij} w_i) \right\}^2 4KTR_j \Delta f. \quad (11)$$

SPECIAL CASES

For most cases of practical interest $g_{m0i}(x)$ is independent of x and

$$g_{m_i} = g_{m0i} w_i. \quad (12)$$

This implies a uniform device structure along the width of the transistor. Making this assumption, we have from (6)

$$\delta I_{dij} = g_{m_i} \overline{\delta V_{gi}} \quad (13)$$

where

$$\overline{\delta V_{gi}} = \frac{1}{w_i} \int_0^{w_i} \delta V_{gi}(x'') dx''. \quad (14)$$

Assuming $R_{0i}(x)$ to be independent of x (true for most cases of interest) we have from (3), (14), and (7)

$$T_{Vij} = \frac{\delta V_{gi}(0) + \delta V_{gi}(w_i)}{2\delta V_j} \equiv A_{Vij}. \quad (15)$$

This is the definition of A_{Vij} , a voltage fluctuation ratio. Then from (11) we get

$$\overline{\delta I_d^2} = \sum_{j=1}^m \left\{ \sum_{i=1}^n (g_{m_i} A_{Vij}) \right\}^2 4KTR_j \Delta f. \quad (16)$$

CALCULATION OF GATE RESISTOR NOISE

Consider again the gate strip in Fig. 2(a) and let there be a fluctuation ΔV_i at $x = x'$ (Fig. 2(c)) such that

$$V_U - V_L = \Delta V_i. \quad (17)$$

Let the corresponding fluctuation at the two ends of the gate be $\delta V_{gi}(0)$ and $\delta V_{gi}(w_i)$. Then

$$\begin{aligned} \delta V_{gi}(x, x') &= (V_L - \delta V_{gi}(0)) \frac{\int_0^x R_{0i}(x'') dx''}{\int_0^{x'} R_{0i}(x'') dx''} \\ &\quad + \delta V_{gi}(0), \quad 0 < x < x' \\ &= (\delta V_{gi}(w_i) - V_U) \frac{\int_{x'}^x R_{0i}(x'') dx''}{\int_{x'}^{w_i} R_{0i}(x'') dx''} \\ &\quad + V_U, \quad x' < x < w_i. \end{aligned} \quad (18)$$

Also, from current continuity

$$\frac{\delta V_{gi}(0) - V_L}{\int_0^{x'} R_{0i}(x'') dx''} = \frac{V_U - \delta V_{gi}(w_i)}{\int_{x'}^{w_i} R_{0i}(x'') dx''}. \quad (19)$$

The fluctuation in the channel current is given by

$$\Delta \delta I_{dii}(x') = \int_0^{w_i} g_{m0i}(x) \delta V_{gi}(x, x') dx \quad (20)$$

$$= \bar{g}_{m0i} \overline{\delta V_{gi}(x')} w_i \quad (21)$$

where $\bar{}$ denotes suitably defined averages. Defining as before

$$T_{Vii}(x') = \frac{\overline{\delta V_{gi}(x')}}{\Delta V_i} \quad (22)$$

we get

$$\Delta \delta I_{dii}(x') = w_i \bar{g}_{m0i} T_{Vii}(x') \Delta V_i. \quad (23)$$

Now, the fluctuation ΔV_i in the i th device produces correlated current fluctuations in all the other $n - 1$ devices. Hence, total current fluctuation

$$\Delta \delta I_{di} = \left[w_i \bar{g}_{m0i} T_{Vii}(x') + \sum_{j=1, j \neq i}^n w_j \bar{g}_{m0j} T_{Vji} \right] \Delta V_i. \quad (24)$$

Squaring and integrating this fluctuation over w_i , we get

$$\overline{\delta I_{di}^2} = \int_0^{w_i} \left[w_i \overline{g_{m0i}} T_{V_{ii}}(x') + \sum_{j=1, j \neq i}^n w_j \overline{g_{m0j}} T_{V_{ji}} \right]^2 \cdot 4KTR_{0i}(x') \Delta f dx' \quad (25)$$

where we have used the relation

$$\overline{\Delta V_i^2(x)} = 4KTR_{0i}(x) \Delta f dx. \quad (26)$$

Then summing up noise due to all gate resistors, we get

$$\overline{\delta I_d^2} = \sum_{i=1}^n \overline{\delta I_{di}^2} = \sum_{i=1}^n \int_0^{w_i} \left[w_i \overline{g_{m0i}} T_{V_{ii}}(x') + \sum_{j=1, j \neq i}^n w_j \overline{g_{m0j}} T_{V_{ji}} \right]^2 \cdot 4KTR_{0i}(x') \Delta f dx'. \quad (27)$$

SPECIAL CASES

For practical cases of interest assuming g_{m0i} to be independent of x , we have

$$g_{m_i} = g_{m0i} w_i$$

and

$$\overline{\delta V_{gi}(x')} = \frac{1}{w_i} \int_0^{w_i} \delta V_{gi}(x, x') dx. \quad (28)$$

Assuming $R_{0i}(x)$ to be independent of x , we get from (17)–(19) and (28)

$$\overline{\delta V_{gi}(x')} = \frac{1}{2} \left\{ \delta V_{gi}(0) + \delta V_{gi}(w_i) + \Delta V_i \left(1 - \frac{2x'}{w_i} \right) \right\}. \quad (29)$$

Then

$$T_{V_{ii}}(x') = \frac{\overline{\delta V_{gi}(x')}}{\Delta V_i} = \frac{1}{2} \left\{ \frac{\delta V_{gi}(0) + \delta V_{gi}(w_i)}{\Delta V_i} + 1 - \frac{2x'}{w_i} \right\}. \quad (30)$$

Using (15), we get

$$T_{V_{ii}}(x') = \frac{1}{2} \left\{ 2A_{V_{ii}} + 1 - \frac{2x'}{w_i} \right\}. \quad (31)$$

Then, from (25) (using $g_{m_i} = g_{m0i} w_i$) we get upon integration

$$\overline{\delta I_{di}^2} = 4KTR_i \Delta f \left[\frac{g_{m_i}^2}{12} + \left(\sum_{j=1}^n g_{m_j} A_{V_{ji}} \right)^2 \right]. \quad (32)$$

Summing up the noise contribution due to all the gate resistors, we get

$$\overline{\delta I_d^2} = \sum_{i=1}^n \left[\sum_{j=1}^n g_{m_j} A_{V_{ji}} \right]^2 4KTR_i \Delta f + \sum_{i=1}^n \frac{g_{m_i}^2}{12} 4KTR_i \Delta f. \quad (33)$$

Adding (16) and (33) we get

$$\overline{\delta I_{dT}^2} = \sum_{j=1}^{m+n} \left\{ \sum_{i=1}^n g_{m_i} A_{V_{ij}} \right\}^2 4KTR_j \Delta f + \sum_{i=1}^n \frac{g_{m_i}^2}{12} 4KTR_i \Delta f. \quad (34)$$

This is a closed-form expression for the total channel current fluctuations. It can be translated into an equivalent lumped gate noise resistance.

$$R_n = \frac{1}{g_{mT}^2} \left[\sum_{j=1}^{m+n} \left\{ \sum_{i=1}^n g_{m_i} A_{V_{ij}} \right\}^2 R_j + \sum_{i=1}^n \frac{g_{m_i}^2}{12} R_i \right] \quad (35)$$

where

$$g_{mT} = \sum_{i=1}^n g_{m_i}. \quad (36)$$

Since for all interconnect resistors, $g_m = 0$, we can extend the sum in (35) to obtain

$$R_n = \frac{1}{g_{mT}^2} \left[\sum_{j=1}^p \left\{ \sum_{i=1}^p g_{m_i} A_{V_{ij}} \right\}^2 R_j + \sum_{i=1}^p \frac{g_{m_i}^2}{12} R_i \right] \quad (37)$$

where p is the number of gate and interconnect resistors.

COMPARISON WITH LOW FIELD CHANNEL THERMAL NOISE

Based on previous analyses [3]–[6] one can write an expression for the channel current spectrum

$$S_I(f) = \gamma \cdot 4KTg_{do} \quad (38)$$

where g_{do} is drain conductance at zero drain bias and γ is a bias-dependent device parameter lying between 0 and 1.

Then the noise contribution due to finite resistance of the gate structure becomes equal to the channel thermal noise when

$$\gamma g_{do} = \sum_{j=1}^p \left\{ \sum_{i=1}^p g_{m_i} A_{V_{ij}} \right\}^2 R_j + \sum_{i=1}^p \frac{g_{m_i}^2}{12} R_i. \quad (39)$$

APPLICATION OF THE GENERAL EXPRESSION TO A SIMPLE LAYOUT

Consider the case of a single gate strip. Then $p = 1$ and we have

$$R_n = \frac{1}{g_{m1}^2} \left[(g_{m1} A_{V_{11}})^2 R_1 + \frac{g_{m1}^2}{12} R_1 \right]. \quad (40)$$

Now if the two ends of the gate are connected directly to a dc potential, $A_{V_{11}} = 0$. Then

$$R_n = \frac{R_1}{12}. \quad (41)$$

The factor (1/12) differs from (7/60) derived in [1]. This is due to an error in evaluating one of the integrals in the previous work.

Further, condition (39) gives

$$R_1 = 12 \cdot \gamma \cdot \frac{g_{do}}{g_{m1}^2}. \quad (42)$$

Assuming $g_{do} = g_{m1}$ and $\gamma = 2/3$ for a long-channel device with low conductivity substrate operating under saturation conditions, we have

$$R_1 = \frac{8}{g_{m1}}. \quad (43)$$

APPLICATION OF THE GENERAL EXPRESSION TO A COMPLEX LAYOUT

Consider the gate structure (Fig. 1) for the input device of a fiber optics preamplifier [7]. It consists of 15 gate resistances and 30 interconnect resistances. The equivalent diagram is

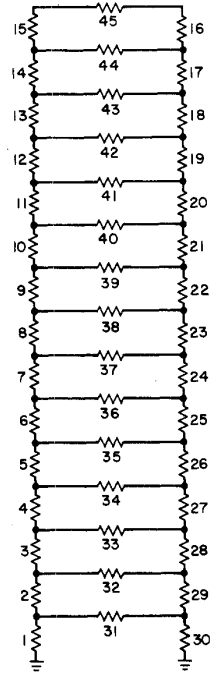


Fig. 3. Equivalent circuit for the resistive gate matrix of Fig. 1.

shown in Fig. 3. Then from (34) we have

$$\overline{\delta I_{dT}^2} = \sum_{j=1}^{45} \left\{ \sum_{i=31}^{45} g_{m_i} A_{V_{ij}} \right\}^2 4KTR_j \Delta f + \sum_{j=31}^{45} \frac{g_{m_j}^2}{12} 4KTR_j \Delta f \quad (44)$$

In the present case $g_{m_i} = g_m$, $R_i = R$ for $i = 31$ to 45 and $R_i = r$ for $i = 1$ to 30 . Therefore

$$\overline{\delta I_{dT}^2} = 5KTR \Delta f g_m^2 + 4KTr \Delta f g_m^2 \sum_{j=1}^{30} \left\{ \sum_{i=31}^{45} A_{V_{ij}} \right\}^2 + 4KTR \Delta f g_m^2 \sum_{j=31}^{45} \left\{ \sum_{i=31}^{45} A_{V_{ij}} \right\}^2 \quad (45)$$

Now, it turns out, from symmetry considerations, that one need not evaluate each $A_{V_{ij}}$. It is either zero or equal to $1/2$. We thus obtain

$$\overline{\delta I_{dT}^2} = 5KTR \Delta f g_m^2 + 2480KTr \Delta f g_m^2. \quad (46)$$

Total device transconductance is $15g_m$. Then

$$\overline{\delta I_{dT}^2} = 4KTR_n \Delta f (15g_m)^2 = 5KTR \Delta f g_m^2 + 2480KTr \Delta f g_m^2.$$

Therefore

$$R_n = \frac{R}{180} + 2.76r. \quad (47)$$

For polysilicon interconnect and gate material, we have $R = 1770 \Omega$, $r = 27 \Omega$. Therefore

$$R_n = 9.8 \Omega + 74.4 \Omega \approx 84 \Omega. \quad (48)$$

It is thus seen that the second term in the expression for R_n corresponding to the interconnect resistor noise dominates over the first term corresponding to the gate resistor noise. Therefore, considerable improvement in the noise performance can be achieved by reducing the interconnect resistance without switching to a lower resistivity gate material.

CONCLUSION

We have derived an expression governing the noise generated by an arbitrary resistive gate structure of an MOS integrated circuit. The results are expressed in terms of known parameters except for voltage fluctuation ratios. These ratios can be readily calculated by inspection for situations involving symmetry. For low-symmetry situations they can be either hand calculated or estimated using a circuit simulation program like ADVISE [8]. This approach can be used to assess the suitability of the gate and interconnect material, and hence design optimum gate structures, for specific low-noise applications.

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A Novel Scheme to Measure the Interface Trap Density Near Band Edges Using CCD's

SUDHIR K. MADAN AND BASABI BHAUMIK

Abstract—A new CCD-based technique to measure the interface trap density is proposed in this paper and the measured values agree with those obtained from the periodic pulse technique. The proposed technique has an operational advantage of measuring the interface state density near the band edge while operating the CCD at any convenient low frequency.

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