Noise Associated with Interdigitated Gate Structures in RF Submicron MOSFETs

Evangelos F. Tsakas and Alexios N. Birbas, *Member, IEEE*

***Abstract*—CMOS technologies have gained considerable attention and have raised expectations for employment in RF transceivers. The shrinkage of the MOSFET device dimensions along with the relatively wide gate electrode devices needed to accommodate RF applications lead to reconsideration of the noise properties of submicron MOSFETs. In this paper, we present the noise properties associated with interconnect resistors of an interdigitated structure and the resulting noise source (strong function of the number of fingers) is evaluated against the other noise sources present in the device such as channel thermal noise, induced gate noise, and resistive gate voltage noise. Short channel effects have been taken into account for the evaluation of these noise sources and two-port analysis performed in order to calculate minimum noise figure and optimum input resistance for noise matching.**

***Index Terms*—Distributed gate electrode, full CMOS transceivers, interdigitated structure, microwave integrated circuits, noise models.**

I. Introduction

DURING the last years CMOS technology, traditionally confined to the digital baseband part of radio frequency transceivers, makes useful inroads into the RF sections. Scaling of CMOS technologies toward deep submicron feature size made them very pervasive in today's analog circuit design especially for the implementation of frond-end RF transceivers.

Nevertheless, the dramatic improvement of MOSFET properties and performance points to a new era in RF integrated circuit design especially at the low GHz range where the dominant technology is currently silicon bipolar. Recent literature [1], [2] reports deep submicron MOSFETs (minimum gate length of 0.1 μm in some technologies) with unity cut-off frequency in the range of tens of GHz and minimum noise figure $(\mathrm{NF}_{\min})$ less than 1 dB. While MOSFET devices are dramatically scaled down, new materials are used extensively in the fabrication steps and new fabrication techniques are unavoidably employed in order to accommodate the ultra-small device dimensions. This progress leads us to reconsider some basic properties of the new miniaturized devices.

In Section II of this work we focus, in particular, on the noise properties of submicron MOSFETs. We show, based in the recent literature, how classical channel thermal noise and induced gate noise models are revised to take into consideration the short-channel effects [3], [4]. In Section III we focus on the noise analysis of MOSFET interdigitated (multifinger) structures. The extremely high values of transconductance, necessary to achieve the RF operating speeds, impose the necessity for wide gate electrodes (large W). This structure provides to the designer flexibility and in today's modern simulators is treated in the same way as a single finger transistor. The number of fingers is defined during layout and no physical effects imposed from this kind of structure are taken into account. However, Jindal [5] some time ago has shown that the effect of thermal voltage fluctuations in a resistive gate matrix perpendicular to the direction of the channel current in a MOSFET can become the dominant noise source in the device. His formulation, which was an extension of the analysis done by Thornber [6], is valid for frequencies at which the distributed RC time constants associated with the gate matrix are not important. In the current work, we investigate the noise originating from the interdigitated structure and the associated noise source is compared against other noise sources present. Moreover, this noise source is modeled appropriately to fit in circuit simulators.

The analysis of the RF noise properties would be incomplete if we did not treat the interdigitated MOSFET as a two-port device in order to calculate its noise figure (NF). In Section IV, we present the complete noise model and we prove that the $\mathrm{NF}_{\min}$ is dependent on the number of fingers n of the interdigitated structure. This section refers to [7] from where we draw experimental results to validate the analytical model.

II. Noise in Submicron MOSFETs

The noise contribution of the first stage of an amplification system influences dominantly the overall noise performance. CMOS inadequacies in device-level performance often have to be circumvented by innovations at the circuit architectural level. The circuit topology of the first stage of a CMOS implemented low noise amplifier (LNA) is usually a common source topology with inductive degeneration [8]–[10]. We present below the most significant noise sources associated with the input MOSFET of an LNA, which have been suitably modeled to accommodate the submicron characteristics. Since noise sources are described generically, the same equations apply for either the single-finger or the multifinger structure.

1) Channel thermal noise $(\overline{i_d^2})$ is the most important noise source. In order to calculate its value the channel must be separated longitudinally into two regions, one where the gradual channel approximation holds and another where carrier velocity saturation is present. The physical characteristics of the channel thermal noise as well as its origin

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E. F. Tsakas and A. N. Birbas are with the Department of Electrical and Computer Engineering, University of Patras, Patras 26500, Greece (e-mail: birbas@ee.upatras.gr).

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have been described in detail in [3]. We can use the classical expression

$$\frac{\overline{i_d^2}}{\Delta f} = 4k_B T \gamma g_{d0} \tag{1}$$

where k_B is the Boltzmann's constant, γ is a factor which is strongly dependent on bias, and g_{d0} is the zero-bias drain conductance. Gamma factor (γ) equals $2/3$ for the classical case but it deviates toward larger values for short channel devices. Especially in cases were the gate voltage is low, gamma factor can be greater then 3 [3].

2) Induced gate noise $(\overline{i_g^2})$ which is insignificant for large and relatively small device dimensions can become important as the device dimensions dramatically shrink and the frequency of operation is increased to tens of GHz. An expression of this noise has been given in [4] and the same quantitative results are obtained if someone uses a Green's function method approach [11]. According to [4]:

$$\frac{\overline{i_g^2}}{\Delta f} = \frac{\omega^2 W^2 C_{\text{ox}}^2 k_B T_o}{3\alpha^3 I_D^3} \times \left(\frac{P_{G1} \cosh^2(AL_s)}{2} + \frac{P_{G2} E_c}{A} \right) g_D^2 \tag{2}$$

where ω is the angular frequency, W is the channel width, C_{ox} is the gate oxide capacitance per unit area, $T_o = 300$ K, I_D is the drain bias current, α is a constant near unity used to parameterise the effect of the channel charge on the threshold voltage, E_c is the critical lateral electric field where velocity saturation occurs, L_S is the length of the velocity saturation region, $1/A$ is the characteristic length of this region, and P_{G1}, P_{G2} are the contributions of the two regions from the source to the drain, respectively. A cross correlation factor c can influence the overall gate noise current:

$$c = \frac{1}{j} \frac{\overline{i_{g1} i_{d1}^*} + \overline{i_{g2} i_{d2}^*}}{\left(\overline{i_g^2 i_d^2} \right)^{1/2}} \tag{3}$$

where the subscript 1 indicates the noise produced by the gradual channel region and the subscript 2 indicates the noise originating from the velocity saturation region. Typical values for c lie between 0.445 and -0.395 [12]. Calculations for short channel MOSFETs show that c can take a value less than -0.75 [4].

3) Gate resistance voltage noise $(\overline{v_g^2})$ accounts for the gate resistive material noise contribution. This noise source has been revised supposing a distributed gate electrode [13]–[15]. In this situation the drain-source capacitance shorts a part of the gate resistance and the total noise voltage is

$$\overline{v_g^2} = 4k_B T \frac{R_g}{3} \Delta f \tag{4}$$

where R_g is the total gate resistance. The addition of an extra gate bias point in an interdigitated structure can reduce this noise source by a factor of 12 [5], [6] and make it almost negligible.

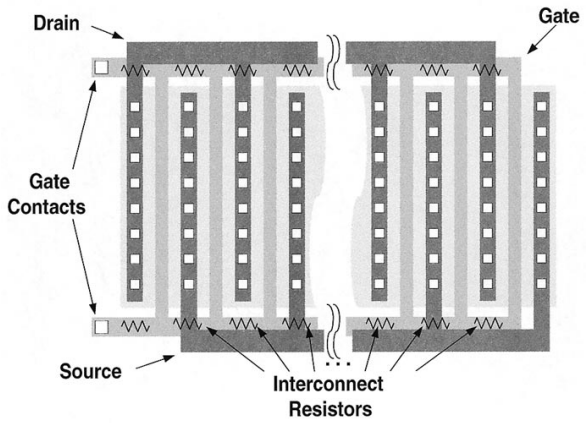

Fig. 1. Interdigitated (multifinger) structure suitable for the implementation of very wide transistors. The interconnect resistors are also drawn between two adjacent fingers. We investigate both the situations of two and one contact points for bias of the gate electrode.

4) Substrate resistance and series drain/source resistances also produce noise in a device. In most cases their contribution is considered to be very small and is neglected. While series drain/source resistances can be kept low by increasing doping the contribution of the back-gating effect of substrate resistance is still very important. There is strong evidence [8] that with careful substrate biasing the overall noise figure can be reduced by 0.3 dB.

III. Interdigitated Structure

All the aforementioned noise sources deteriorate the MOSFET performance in an RF circuit application affecting the noise figure of the device. Additionally, strict high gain specifications lead to the usage of very wide MOS transistors. The situation is very common in RF frond-end designs where the device transconductance lies in the range of tens of mS. Interdigitated (multifinger) structure is a very useful design technique, for the integrated circuit designers, to implement those transistors (Fig. 1). Even though interdigitated structures are extensively used, the associated properties have not been extensively studied in the literature. All the popular integrated circuit simulation packages treat this structure as a very wide MOSFET, no matter how many fingers are actually employed. To accommodate the physical properties associated with this different device shape, a new equivalent circuit that incorporates some additional elements must be employed. This equivalent circuit will lead us to a more accurate simulation model.

When the interdigitated structure is being used, there are no specific rules to decide the exact number of fingers to employ. This parameter is usually set to an appropriate value in order to reduce occupied area by suitably setting the shape of the device. Recently in the literature, the number of fingers was used to match the optimum noise impedance to the source impedance [7], [16]. The n parallel-finger transistors are treated as two-port networks and the known formula of the NF was recalculated. The NF_{min} was considered unchanged when we move from one finger to a multifinger scheme.

To calculate an accurate NF_{min} for an interdigitated MOSFET, in the context of the noise sources presented previ-

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ously, we take into account another noise source originating from the gate interconnect material of interdigitated structures. We consider these interconnects (small areas of polysilicon or silicide) as lumped resistors expressed in ohms per square. Apart from this noise source all other noise sources are treated as a single wide-gate transistor. Fig. 1 indicates that the distance between two adjacent gates scales down for lower feature size technologies, but the number of squares used for this connection is constant. Even if we increase the width of this resistor we cannot achieve a total length less than one or two squares. These interconnect resistors produce noise, which was first described by Jindal [5]. The main goal of that work was to compare the resistive gate noise and the resistive interconnect noise in order to lead the process technologies to the right choice of gate and interconnect materials. We expand this situation here for the submicron case.

To investigate the outcome derived in (10) we have to evaluate the transformation matrix M_{ij}, which represents the influence of the j-th interconnect resistance on the ith finger. We consider two cases, as follows.

a) There are two contact points at both edges of the interdigitated structure (Fig. 1). In this case we consider that the value of the interconnect resistances is negligible compared to the gate electrode resistance for each finger. As extracted from Fig. 2(b) the nominator of (9) is equal to $\overline{\delta V_j}$, since the voltage fluctuation of the interconnect resistance noise source is applied at the two ends of each finger, and thus M_{ij} is $1/2$ for $i \geq j$. For $1 < j$ both ends of the fingers are shorted to the ground. As a result, the interconnect resistors closer to the gate contact points are more significant, because their voltage fluctuation is transferred to the n-parallel channels through higher effective transconductance [Fig. 2(a)]. Then (10) becomes

$$\overline{\delta I_{\text{int}}^2} = 4k_BTR_{\text{int}}Bg_{m_i}^2 2\left[\left(\frac{n}{2}\right)^2 + \left(\frac{n-1}{2}\right)^2 + \left(\frac{n-2}{2}\right)^2 + K + \left(\frac{1}{2}\right)^2\right]. \tag{11}$$

The convergence of the series in (11) indicates that this noise source can be described completely by the following expression:

$$\overline{I_{\text{int}}^2} = 4k_BTR_{\text{int}}g_m^2B\frac{1}{2n^2}\sum_{k=1}^{n}k^2 = 4k_BTR_{\text{int}}g_m^2B\frac{(n+1)(2n+1)}{12n}. \tag{12}$$

The value of this noise source is a strong function of the number of fingers n. In many applications the number n approaches 100 [8] and then the interconnect resistance noise becomes significant and must be taken into account along with channel thermal noise calculations.

b) There is one contact point at the gate electrode. In this case we also consider that the interconnection resistances are negligible compared to the gate electrode resistance of each finger. For the voltage divider shown in Fig. 2(c), the voltage fluctuation at the two ends of each finger is noted as $\overline{\delta V_{\text{eff}_{j-1}}}$ and $\overline{\delta V_{\text{eff}_{n+1-j}}}$. Here subscripts $j-1$ and $n+1-j$ indicate the number of parallel fingers at the two parts of the voltage divider.

$$\overline{\delta V_{\text{eff}_{n+1-j}}} = \frac{j-1}{n}\overline{\delta V_j} \quad \text{for } i \geq j \tag{13}$$

$$\overline{\delta V_{\text{eff}_{j-1}}} = \frac{n+1-j}{n}\overline{\delta V_j} \quad \text{for } i < j. \tag{14}$$

From (9), (13) and (14) the resulting transformation matrixes are:

$$M_{ij} = \frac{\overline{\delta V_{\text{eff}_{n+1-j}}}}{2\overline{\delta V_j}} = \frac{j-1}{n} \quad \text{for } i \geq j \tag{15}$$

$$M_{ij} = \frac{\overline{\delta V_{\text{eff}_{j-1}}}}{2\overline{\delta V_j}} = \frac{n+1-j}{n} \quad \text{for } i < j. \tag{16}$$

The total channel current noise is then derived from (10), (15) and (16):

$$\overline{I_{\text{int}}^2} = 4k_BTBR_{\text{int}}g_m^2\frac{1}{n^2}2\sum_{j=1}^{n}\left(\sum_{i=1}^{n}\frac{1}{2}\right)^2 = 4k_BTBR_{\text{int}}\frac{g_m^2}{2}n. \tag{17}$$

In the case of one contact point, there is no shorted part of the interconnect resistance noise and thus an increase of the resulting channel noise is expected when compared to the previous case [(12)].

We now consider an interdigitated transistor with n fingers and $2n$ interconnect resistances [Fig. 2(a)]. The n parallel transistors are equal and the total transconductance of the device is the sum of the transconductances of all the fingers. The voltage noise that each interconnect resistance is contributing is given by

$$\overline{V_j^2} = 4k_BTR_{\text{int}}B \tag{5}$$

where R_{int} is the value of the interconnect resistance and B is the effective bandwidth. The channel current fluctuation caused by this resistance, as defined for one finger, is

$$\delta I_{\text{int}_{ij}} = g_{m_i}\overline{\delta V_{g_i(x)}} \tag{6}$$

where g_{m_i} is the transconductance of each finger and $\overline{\delta V_{gi(x)}}$ is the average voltage fluctuation along the particular finger caused by the ith interconnect resistance. This average can be defined as the mean value of the fluctuations at the two ends of the finger. Then the average channel current fluctuation for one finger is

$$\delta I_{\text{int}_{ij}} = g_{m_i}\frac{\delta V_{g_i(w)} + \delta V_{g_i(0)}}{2} \tag{7}$$

or

$$\overline{\delta I_{\text{int}_{ij}}^2} = g_{m_i}^2\left(\frac{\delta V_{g_i(w)} + \delta V_{g_i(0)}}{2\overline{\delta V_j}}\right)^2\overline{\delta V_j^2} = g_{m_i}^2\left(\frac{\delta V_{g_i(w)} + \delta V_{g_i(0)}}{2\overline{\delta V_j}}\right)^2 4k_BTR_{\text{int}}B = 4k_BTR_{\text{int}}BM_{ij}^2g_{m_i}^2 \tag{8}$$

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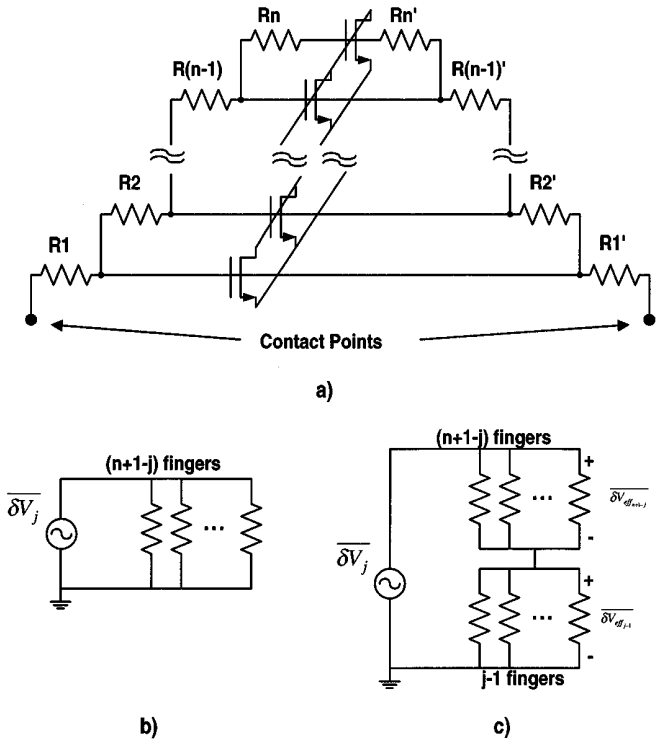

Fig. 2. (a) Equivalent circuit of the interdigitated structure. An uncorrelated voltage noise source is associated with each interconnect resistance. The equivalent circuit of the interdigitated structure is drawn for (b) two contact points and (c) one contact point, when one of the interconnect resistance voltage noise sources is considered.

where

$$M_{ij} = \frac{\delta V_{g_i(w)} + \delta V_{g_i(0)}}{2\overline{\delta V_j}}. \tag{9}$$

The total channel current noise can be derived if we add the contribution of all fingers due to all interconnect resistors

$$\overline{I_{\rm int}^2} = 4k_BTBR_{\rm int}\left(\frac{g_m}{n}\right)^2 2\sum_{j=1}^{n}\left(\sum_{i=1}^{n} M_{ij}\right)^2 \tag{10}$$

where $g_m = n \cdot g_{m_i}$ is the total device transconductance and the factor 2 accounts for the two rows of interconnect resistors (both edges of the fingers).

In Fig. 3 we present a comparison between the interconnect resistance noise source [(12)], the induced gate noise [4] and the channel thermal noise floor [3] as a function of the number of fingers. Interconnect resistance noise can be in the same order of magnitude to the channel thermal noise. These curves resulted for gate width $W = 100$ μm, gate length $L = 0.5$ μm, $V_{\rm gs} = 1.5$ V, $V_{\rm ds} = 3$ V, $R_{\rm int} = 4$ Ω, frequency $f = 1$ GHz and temperature $T = 300$ K. Parameters have been drawn for an HP 0.5 μm process available to us.

IV. Noisy Two-Port Description

With the addition of the interconnect resistance noise we have suitably described all the noise sources appearing in a submicron interdigitated MOSFET. Nevertheless, it is very useful to

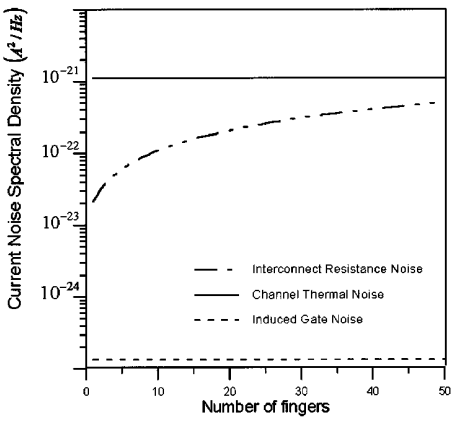

Fig. 3. Channel thermal noise, induced gate noise and interconnect resistance noise (calculated at both edges) versus the number of fingers n. The calculations have been made according to [3] and (2)–(4) for gate width $W = 100$ μm, gate length $L = 0.5$ μm, $V_{\rm gs} = 1.5$ V, $V_{\rm ds} = 3$ V, $R_{\rm int} = 4$ Ω, frequency $f = 1$ GHz and temperature $T = 300$ K.

calculate the RF noise properties of this device, such as noise figure (NF) and optimum noise resistance ($R_{\rm opt}$), in the context of all these noise sources. Fig. 4 shows the noise equivalent circuit of the interdigitated structure. The referred to the input correlated noise sources are

$$\upsilon_A = \upsilon_g - \frac{i_d + i_{\rm int}}{g_m} + (R_g + r_i)i_g - j\frac{f}{f_t}(R_g + r_i)(i_d + i_{\rm int}) \tag{18}$$

$$i_A = i_g - j\frac{f}{f_t}(i_d + i_{\rm int}) \tag{19}$$

where r_i is the channel charging resistance [7], i_d is the channel thermal noise, $i_{\rm int}$ is the interconnect resistance noise, i_g is the induced gate noise, υ_g is the gate voltage noise due to the resistive gate material perpendicular to the direction of channel current, and f_t is the unity current gain frequency which can be approached by the following expression:

$$f_t \approx \frac{g_m}{2\pi C_g}. \tag{20}$$

where $C_g = C_{\rm gs} + C_{\rm gd}$. Following a standard network analysis we can divide the voltage noise source to one uncorrelated and another correlated part aiming at the calculation of the minimum noise figure and the optimum input resistance for noise matching. We adopted the same formalism for the definitions of equivalent noise resistance and conductance as [17]. The noise conductance at the input (G_n), corresponding to the noise models detailed in Sections II and III, is

$$G_n = \left(\frac{f}{f_t}\right)^2 \gamma g_{do} C_1 \tag{21}$$

The resulting optimum noise resistance and minimum noise figure are given by

$$\mathrm{NF}_{\rm min} = 1 + 2\left(\frac{f}{f_t}\right)^2 \gamma g_{d0} C_2 (r_i + R_g) + \sqrt{\left(\frac{f}{f_t}\right)^2 C_3} \tag{22}$$

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$$R_{\rm opt} = \sqrt{\left(\frac{C_2}{C_1}\right)^2 (R_g + r_i)^2 + \left(\frac{f_t}{f}\right)^2 C_4}. \quad (23)$$

C_1–C_4 are suitably described parameters dependent strongly on the number of fingers n and are very complicated functions of frequency, unity current gain frequency (f_t) and all individual noise source's parameters (i.e. γ and R_g). These can be approached by numerical calculations based in [3] and (2)–(4). For this reason we can only have numerical evaluation of $\rm NF_{min}$ and $R_{\rm opt}$. For $n = 1$, parameter C_1 is less than one and if the induced gate noise is neglected, is equal to unity. Parameters C_2 and C_3 are also very close to unity for $n = 1$ but their values are increasing rapidly, to a few hundreds, for $n = 50$. The results of our calculations are shown in Fig. 5 where $\rm NF_{min}$ and $R_{\rm opt}$ are plotted versus $1/n$. The interconnect resistance noise was calculated for two edges contact points and the presented experimental measurement points were reprinted from [7]. It is apparent from this curve that as the number of fingers increases, the noise contribution of the interconnect resistances increases dramatically. For n equal to unity, or $R_{\rm int}$ equal to zero, (22) reverts to the classical expression of the noise figure plateau, which is independent of n. For the process parameters used in our calculations this noise floor lies somewhere below 2 dB.

Moreover, in order to provide a simplified circuit level model useful to circuit designers we adopt the analysis in [9] combined with the inductive degenerated common source topology. Since channel thermal noise and interconnect resistance noise are placed in parallel in the noise equivalent circuit of Fig. 3, we can extend the analysis and derive the following simplified equation for the total noise factor:

$$F = 1 + \frac{R_g}{R_s} + \frac{R_l}{R_s} + \left(\frac{\omega_t L_s}{g_m}\right)^2 \left(\gamma g_{d0} + R_i g_m^2 \frac{1}{2n^2} \sum_{k=1}^{n} k^2\right) \quad (24)$$

where n is the number of fingers, ω_t is the unity current gain angular frequency, and R_g and R_s are the parasitic resistors of the inductances L_g and L_s, respectively. In this formulation only the channel thermal noise is considered along with the interconnect resistance noise.

V. Discussion and Conclusions

According to the previous analysis and modeling, it is apparent that the noise performance of the interdigitated structure varies with the number of fingers. This is also supported by experimental evidence. The noise produced by the interconnect resistances is not only dependent on n but also can be of the order of channel thermal noise. When the interconnect resistances are higher than 10 Ω, there is strong dependence of the $\rm NF_{min}$ on the number of fingers. This situation can be eased if we employ alternative materials, i.e., silicided gate electrodes, which have an extremely lower sheet resistance. Nevertheless, even if we use such materials there is a tendency for large W/L ratios, which in turn leads to large number of fingers (approaching a hundred) and thus resulting in NF degradation.

The presented analytical modeling of these noise sources can replace the ad hoc hypothesis, made usually by circuit designers:

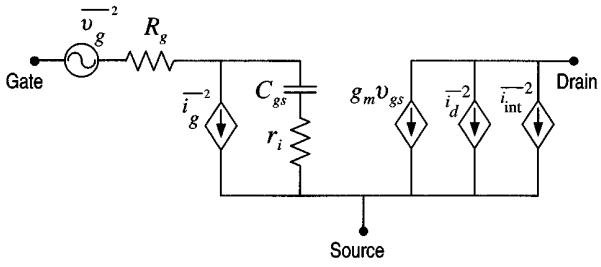

Fig. 4. Simplified noise model of the nth finger of an interdigitated MOSFET.

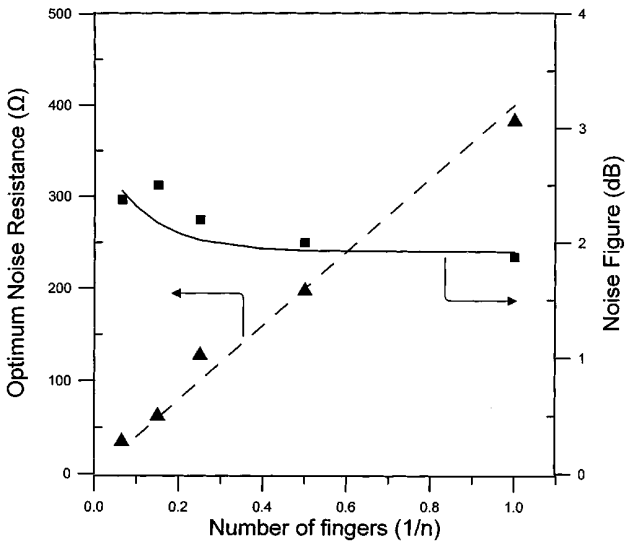

Fig. 5. Minimum noise figure and optimum noise resistance plotted as a function of the number of fingers following (22) and (23). The experimental points presented in this plot are reprinted from [7]. For a multi-finger transistor the deviation from the classical model was about 0.3 dB for $n = 15$.

"increment the expected overall noise figure by 0.5 dB to accommodate nonwell understood parasitics producing noise." An example for more accurate noise modeling is the erroneous assumption that the γ factor equals $2/3$, which is not the case since strong dependence of bias is analytically described in [3] and confirmed by measurements in [18].

Concerning $R_{\rm opt}$ there is no significant deviation from the classical expression, which assumes that it scales with $1/n$ [7]. The calculated value of $R_{\rm opt}$, as derived from (23), corresponds only to one finger. If we treat the n-fingers as two-port parallel networks the resulting optimum noise resistance for noise matching is not affected from the small valued interconnect resistances. The almost linear behavior of $R_{\rm opt}$ was validated from experimental results [7] and the actual dependence is drawn in Fig. 5.

The two cases where the gate resistive structure is contacted to either two or one points have been extensively discussed. These are the most common situations in integrated circuit design. Moreover, the case where the gate electrode is contacted at four points is very interesting (both ends at the two edges). If the value of the interconnect resistance is assumed negligible compared to the gate electrode resistance of one finger (which is true for most cases), then the noise contribution of the interconnect resistance's is zero.

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The main goal of this paper was to provide a complete noise analysis of interdigitated structures at the device level, compatible with the most recent advancements of MOS process technologies, by introducing an easy-to-use formulation of the interconnect resistance noise. Two-port noise properties were also treated providing new guidelines in design of RF frond-ends.

REFERENCES

[1] H. S. Momose *et al.*, "High frequency AC characteristics of 1.5 nm gate oxide MOSFET," in *IEDM Tech. Dig.*, Dec. 1996, pp. 105–108.

[2] T. Ohguro *et al.*, "0.18μ m low voltage/low power RF CMOS with zero Vth analog MOSFET's made by undoped epitaxial channel technique," in *IEDM Tech. Dig.*, Dec. 1997, pp. 837–840.

[3] D. P. Triantis, A. N. Birbas, and D. Kondis, "Thermal noise modeling for short channel MOS transistors," *IEEE Trans. Electron Devices*, vol. 43, pp. 1950–1955, 1996.

[4] D. P. Triantis, A. N. Birbas, and S. E. Plevridis, "Induced gate noise in MOSFET's revisited—The submicron case," *Solid-State Electron.*, vol. 41, pp. 1937–1941, 1997.

[5] R. P. Jindal, "Noise associated with distributed resistance of MOSFET gate structures in interdigitated circuits," *IEEE Trans. Electron Devices*, vol. ED-31, pp. 1505–1509, Oct. 1984.

[6] K. K. Thornber, "Resistive-gate-induced thermal noise in IGFET's," *IEEE J. Solid-State Circuits*, vol. SC-16, no. 4, pp. 414–415, 1981.

[7] T. Manku, "Microwave CMOS—Device physics and design," *IEEE J. Solid-State Circuits*, vol. 34, pp. 277–285, 1999.

[8] Q. Huang, P. Orsatti, and F. Piazza, "GSM transceiver frond-end circuits in 0.25-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 34, pp. 292–303, 1999.

[9] D. K. Shaeffer and T. H. Lee, "A 1.5-V, 1.5-GHz CMOS low noise amplifier," *IEEE J. Solid-State Circuits*, vol. 32, no. 5, pp. 745–759, 1997.

[10] Q. Huang, F. Piazza, P. Orsatti, and T. Ohguro, "The impact of scaling down to deep submicron on CMOS RF circuits," *IEEE J. Solid-State Circuits*, vol. 33, no. 7, pp. 1023–1036, 1999.

[11] T. Manku, M. Obrecht, and Y. Lin, "High-frequency dependence of channel noise in short-channel RF MOSFET's," *IEEE Electron Device Lett.*, vol. 20, pp. 481–483, Sept. 1999.

[12] A. van der Ziel, *Noise in Solid State Devices and Circuits*. New York: Wiley, 1986.

[13] E. Abou-Allam and T. Manku, "A small-signal MOSFET model for radio frequency applications," *IEEE Trans. Computer-Aided Design*, vol. 16, pp. 437–447, 1997.

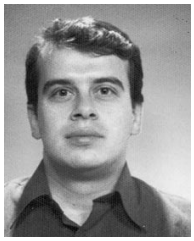
[14] S. F. Tin, A. A. Osman, and K. Mayaram, "Comments on "A small-signal MOSFET model for radio frequency applications"," *IEEE Trans. Computer-Aided Design*, vol. 17, pp. 372–374, 1998.

[15] B. Razavi, R. Yan, and K. Lee, "Impact of distributed gate resistance on the performance of MOS devices," *IEEE Trans. Circuits Syst. I*, vol. 41, pp. 750–754, 1994.

[16] T. Manku, "The impact of induced gate noise when simultaneously power and conjugate noise-matching MOS transistors," *IEEE Trans. Circuits Syst. II*, vol. 46, pp. 842–844, 1999.

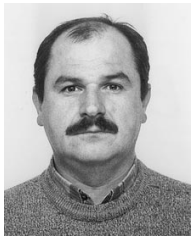
[17] G. D. Vendelin, A. M. Pavio, and U. L. Rohde, *Microwave Circuit Design Using Linear and Non-Linear Techniques*: Wiley, 1990.

[18] A. A. Abidi, "High frequency noise measurements on FET's with small dimensions," *IEEE Trans. Electron Devices*, vol. ED-33, pp. 1801–1805, Nov. 1986.



Evangelos F. Tsakas was born in Athens, Greece, in 1972. He received the B.S. degree in physics from University of Patras, Patras, Greece, where he is now a Ph.D. candidate in electrical engineering.

His research interests are in noise measurements and modeling of MOSFET, Si BJT, and SiGe HBT devices, and semiconductor device simulation. He is also involved in the design of low-noise, mixed analog-digital integrated circuits.



Alexios N. Birbas (S'83–M'92) received the Dipl. degree in electrical engineering from the University of Patras, Patras, Greece, in 1985, and the M.S.E.E. and Ph.D. degrees from the University of Minnesota, Minneapolis, in 1986 and 1988, respectively.

He was on the faculty of the University of Minnesota until 1989. He then worked in industry in the area of VLSI design. Since 1992, he has been with the faculty of Electrical and Computer Engineering Department, University of Patras, and is also an industry consultant. He has been leading an industry-sponsored team at the University of Patras, where he conducts research in the area of hardware-software co-design by exploring low-level and high-level design alternatives for the efficient development of complex systems on a chip. His research activities are in the area of microelectronics device modeling, device noise, and VLSI circuit design. He has published more than 50 technical papers in journals and conference proceedings.

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