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Paper No. __

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE AMERICA, INC.,
Petitioner,

v.

INFINEON TECHNOLOGIES AUSTRIA AG,
Patent Owner.

Case No. IPR2024-00975
Patent No. 9,899,481

PATENT OWNER'S PRELIMINARY RESPONSE

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LISTING OF EXHIBITS

Exhibit	Description
2001	Ohring, Milton, Reliability and Failure of Electronic Materials and Devices (Academic Press 1998)
2002	Murari, B., et al. (eds.), Smart Power ICs (Springer 2002)
2003	Baliga, Jayant, "Power Integrated Circuits-A Brief Overview," 33 IEEE Transactions on Electron Devices, 1936-39 (Dec. 1986)
2004	Pecht, Michael, et al. (eds.), Plastic-Encapsulated Microelectronics (John Wiley & Sons, Inc. 1995)
2005	Stueckler, F., CoolMOS™ C7 650V Switch in a Kelvin Source Configuration available at https://www.infineon.com/dgdl/Infineon-ApplicationNote_MOSFET_CoolMOS_C7_650V_in_TO-247_4pin-AN-v01_00-EN.pdf?fileId=db3a30433e5a5024013e6a9908a26410 (May 2013)
2006	Ruzyllo, Jerzy, Semiconductor Glossary as archived at http://web.archive.org/web/20160704112715/http://www.semi1source.com/glossary/default.asp?searchterm=lateral+transistor on July 4, 2016
2007	U.S. Patent Application Publication No. 2015/0214189 A1

I. INTRODUCTION

The ’481 Patent solves packaging problems for certain types of transistors formed from semiconductor compounds such as gallium nitride (GaN) rather than from silicon. A package protects a semiconductor device and provides connections from the semiconductor device to other components. By 2016, when the ’481 Patent was filed, compound semiconductor devices were attractive candidates for use in power supplies and power converters because they could carry large currents, support high voltages, and provide fast switching times. But the high voltages and fast switching times created packaging challenges.

All the challenged claims require a “lateral transistor” and a “die pad.” A lateral transistor is characterized by current flowing laterally (parallel to the semiconductor’s surface) between the transistor’s source and drain regions as opposed to flowing vertically (normal to the semiconductor’s surface) as in a “vertical transistor.” A “die pad … is part of a lead frame.”[1] Petition, 13. A leadframe is a metal structure with leads to provide connections from the semiconductor device to electrical components outside the package and may have a

[1] The ’481 Patent uses one word to refer to a leadframe (*e*.g., Ex. 1001, 1:9), while Nega and the Petition use two words (*e.g*., Petition, 13; Nega, ¶[0091]). This paper uses one word to be consistent with the ’481 Patent.

die pad to support the semiconductor device. Some leads may be integral with and connected to the die pad while others may be spaced a distance apart from the die pad and can be coupled to the semiconductor device by wire bonds or clips.

The ’481 Patent recognized that long conductors from an external source to the transistor’s source electrode had parasitic source inductance that could, particularly at fast switching times, negatively impact the transistor’s performance. The ’481 Patent counteracts that parasitic source inductance by using a technique called source sensing. All the challenged claims require source sensing functionality applied on a lead that is spaced apart from the die pad, as opposed to a lead that is integral with and connected to the die pad.

The Petition advances twelve grounds that it divides into two groups based on the primary reference. The grounds are characterized as the Nega Grounds (Grounds 1A-F) and the Liu Grounds (Grounds 2A-F). The grounds are fatally flawed and mischaracterize the way the prior art references work in material ways. Petitioner’s expert should have corrected these clear technical errors but did not because Petitioner’s expert simply rubber-stamped the Petition’s erroneous arguments and largely parrots the Petition verbatim.

A. The Nega Grounds Fail for at Least Three Independent Reasons

First, every challenged claim requires a lead that provides source sensing functionality and is spaced at a distance from the die pad. Petitioner attempted to

reconstruct the claims in hindsight by alleging that a POSA would have added Roberts' source sensing functionality to a lead that is spaced apart from Nega's alleged die pad. But Petitioner conflated the source and drain electrodes in Nega and proposed a Nega-Roberts Combination that connects ***source*** sensing functionality to Nega's ***drain*** electrode. It is undisputed that source sensing functionality is provided via a connection to the ***source*** electrode. A POSA simply never would have made Petitioner's Nega-Roberts Combination that connects source sensing functionality to the wrong (drain) electrode of Nega's transistor. The Nega Grounds fail for this reason alone.

Second, even if the Board were to overlook Petitioner's conflating of the source and drain electrodes in Nega's transistor and were to read the Petition as alleging that a POSA would have added source sensing functionality to the correct (source) electrode in the Nega transistor, the Nega Grounds still fail because Petitioner establishes no reason why a POSA would have used a lead ***spaced apart*** from the component Petitioner alleges "constitutes" Nega's die pad – its leadframe – to add an additional connection to Nega's ***source*** electrode. Because Petitioner conflated the source and drain electrodes in Nega's transistor, Petitioner used a lead spaced apart from Nega's leadframe to connect to the electrode that Petitioner alleged was the source electrode because a spaced apart lead is the type of lead Nega taught for connecting to ***that*** electrode. Following Petitioner's rationale

would have led to using a lead that was integral with and connected to the leadframe – not spaced apart from it – for connecting to Nega's actual source electrode because Nega only discloses connecting to the actual source electrode via a lead that is integral with and connected to the leadframe. Petitioner failed to even allege, let alone support with evidence, any reason why a POSA would have connected source sensing functionality to Nega's source electrode using a different type of lead (one spaced apart from a die pad) than the type of lead Nega taught for connecting to the source electrode. Petitioner thus failed to establish any reason why a POSA would have modified Nega in a manner that meets any challenged claim.

Third, the challenged claims were allowed after an amendment to require a lateral transistor. Despite that, Petitioner failed to establish that Nega discloses a lateral transistor as claimed. Petitioner cites no express disclosure in Nega of a lateral transistor because there is none. Petitioner alleges that Nega discloses a lateral transistor because its electrodes are arranged laterally on one side of the substrate. Petitioner is simply wrong because vertical transistors were known that also had all the electrodes arranged laterally on one side of the substrate. The only other "analysis" Petitioner offers is to annotate a Nega figure to allegedly show where current is alleged to flow. But Petitioner is demonstrably wrong about where the current path is in Nega's transistor because Petitioner draws its alleged

current path through an insulating film. It is beyond dispute that current does not (indeed cannot) flow through an insulating layer. Petitioner's analysis is facially flawed and failed to establish that Nega discloses a lateral transistor, as required by every challenged claim, either expressly or inherently.

B. The Liu Grounds Fail for at Least Three Independent Reasons

First, Petitioner alleges that Liu is prior art based on the filing date of a provisional application that Liu claims priority to, but the Petition fails to establish that Liu's provisional has the disclosure that the Liu Grounds rely on. Petitioner alleged in conclusory fashion that the disclosure in Liu's provisional is "identical or nearly identical" to the relied upon disclosure in Liu. But Petitioner and Petitioner's expert ignored that Liu discloses a semiconductor chip bonded to an ***electrically insulating*** die attach material whereas the Provisional discloses a chip bonded to an ***electrically conductive*** die attach material. Petitioner never even acknowledges this facial difference, let alone explain why it is somehow immaterial so that the disclosures are "identical or nearly identical" despite this difference. Thus, Petitioner failed to carry its burden to establish that the relied-upon disclosure from Liu is in Liu's provisional, which was required for Petitioner to prove that Liu is prior art to the challenged claims based on the filing date of Liu's provisional.

Second, Petitioner failed to establish that Liu discloses a lateral transistor. Petitioner cites no express disclosure in Liu of a lateral transistor—because Liu has no such disclosure. As it did in the Nega Grounds, Petitioner simply assumes that Liu discloses a lateral transistor because all its electrodes are on one side. But the prior art discloses vertical transistors with all the electrodes on one side. The Petition failed to establish that Liu discloses a lateral transistor either expressly or inherently.

Third, the Petition failed to establish that Liu discloses a die pad. "Die pad" is a term of art that means a portion of a leadframe on which a die[2] is attached. The Petition admits that a "die pad … is part of a lead frame." Petition, 13. But the Petition makes no allegation that the embodiment of Liu on which the Petition relies even has a leadframe. The Petition, therefore, failed to establish that Liu's device has a die pad because a die pad must be part of a leadframe and the Petition failed to establish that Liu's device has a leadframe.

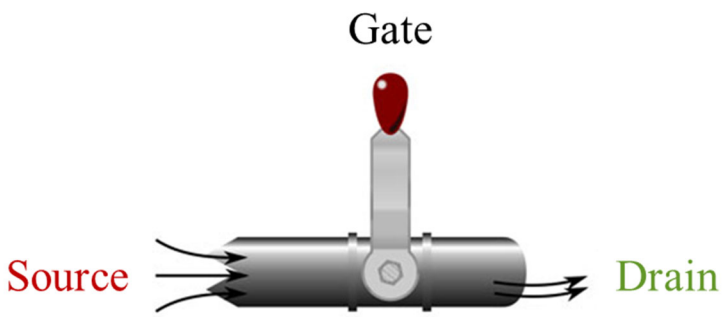
II. TECHNOLOGY BACKGROUND

A. Transistors

A transistor works like a gate valve. When the gate of a gate valve is open, fluid flows from a **source** to a **drain**. When the gate is closed, fluid flow stops.

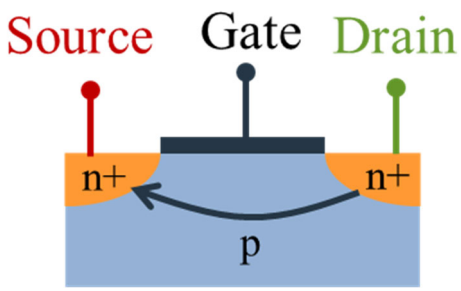
[2] A die is a portion of a semiconductor wafer ready to be packaged.

Gate Valve



A field effect transistor (FET)—the type of transistor at issue here—is a semiconductor device with an electrical gate to control the flow of current instead of a physical gate to control the flow of fluid in a gate valve. Semiconductor devices were traditionally made of silicon (Si), but other semiconductive materials made of compounds such as silicon carbide (SiC) and gallium nitride (GaN) were emerging when the application for the ’481 Patent was filed. Ex. 1001, 1:17-25. When a voltage exceeding a threshold is applied to the transistor’s gate, the gate opens or closes (depending on its design), thereby controlling the flow of electrical current between the source and drain. Ex. 2001 at 62-63.

Transistor



B. Lateral versus Vertical Transistors

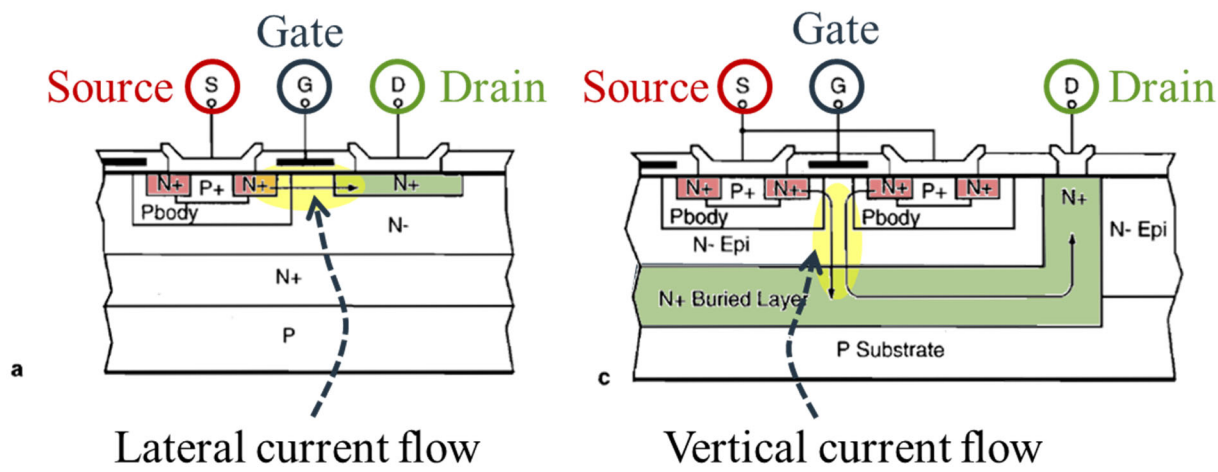
Transistors can be vertical or lateral transistors. This characterization is determined by the direction of current flow relative to the surface of the semiconductor device. A lateral transistor is a transistor in which current flows across "in the direction parallel to" the device surface. Ex. 1002, 33-34. Current "flows in the direction normal to" the device surface in a vertical transistor. *Id*.

The difference between lateral and vertical transistors is illustrated in the figures below which are annotated reproductions of Figures 1.7a and 1.7c from a textbook entitled "Smart Power ICs." Ex. 2002, 7-8 ("lateral structure" shown in "Fig. 1.7a," whereas "current flow is vertical in the power device structure" in "Fig. 1.7c"). In the annotated figures, the transistor's **source region** (an N+ region) is highlighted red and the **drain region** (also an N+ region) is highlighted green. The **source** and **drain** regions are connected to respective electrodes at the surface of the device. There is also a gate electrode. The source, drain, and gate electrodes are labeled S, D, and G, respectively. In the lateral transistor on the left, the current flows parallel to the device surface from the **source region** to the **drain region**. In the vertical transistor on the right, the **drain region** is formed by an "N+ ***Buried*** Layer"[3] that is buried below the **source region**. As a result, when a

[3] Emphasis is added throughout unless otherwise noted.

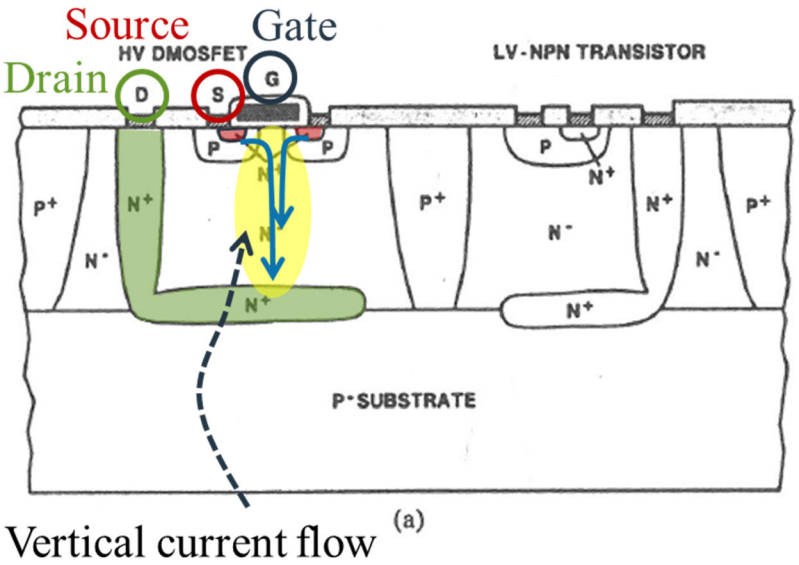
voltage is applied at the **gate**, the current flows vertically between the **source region** and the **drain region,** normal to the surface of the device.

Example of a Lateral Transistor **Example of a Vertical Transistor**



Another example of a vertical transistor is shown in the figure below which is an annotated reproduction of a figure from an IEEE article entitled "Power Integrated Circuits - A Brief Overview," published by IEEE in 1986. Ex. 2003, 1937 ("Fig. 3(a) … preserves a ***vertical*** high-voltage ***transistor structure***"), Fig. 3(a) (annotated below). The electrodes for the source and drain regions are labeled S and D, respectively, and the gate electrode is labeled G. Again, the **drain region** is formed by an N+ layer that is buried below the **source region**. The current flows vertically between the **source region** and the **drain region**, normal to the surface of the device.

Another Example of a Vertical Transistor



C. Parasitic Source Inductance

Transistors are typically housed in a package that provides electrical connections from the transistor, through bond wires or clips, to external contacts called leads that are used to connect the transistor to other electrical components, such as other components on a printed circuit board. Ex. 1001, 1:6-16. One such external component is a driver used to control the voltage applied to the transistor's gate to turn the transistor on and off. *Id.*, 5:46-53.

Long conductors (*e.g.*, leads and bond wires) attached to the transistor's source have unwanted parasitic inductance that can have an undesirable impact on the transistor's performance. *Id.*, 5:39-45. For example, when the gate driver for a normally-off transistor turns off the voltage applied to the gate, the expectation is that the transistor will turn off and no current from the source will flow through the

transistor. However, due to parasitic source inductance, a voltage difference between the source and gate may remain, which keeps the transistor turned on when it should be off and thereby results in unintended and undesired current flow from the source through the transistor when the transistor should be off. Ex. 2005, 4 ("the switching losses are significantly increased by the negative feedback caused by the parasitic inductance in the source lead of the power switch"). The continued current flow when the transistor should be off results in energy loss. Ex. 1001, 5:39-45. The higher the switching speeds, the worse the energy loss becomes. Ex. 2005, 4 ("With new generations of power switches becoming faster and faster, the effect of the parasitic elements of package and board limit more and more the overall system performance.").

As discussed below, the '481 Patent is directed to packages for GaN power transistors that exclude such "parasitic source inductance from the driver circuit" and overcome the problems that arise from parasitic source inductance. Ex. 1001, 5:43-53.

D. Leadframe, Die Pad, and Leads

A "***leadframe***" is a "mechanical support and the electrical and thermal interconnection" of a semiconductor chip. Ex. 2002, 500. A leadframe is typically constructed from a metal ribbon from which holes are punched or etched out to

form a die pad and various leads. Ex. 2002, 486, Fig. 13.2 (below, annotated). The center of the leadframe shown below is a die pad.

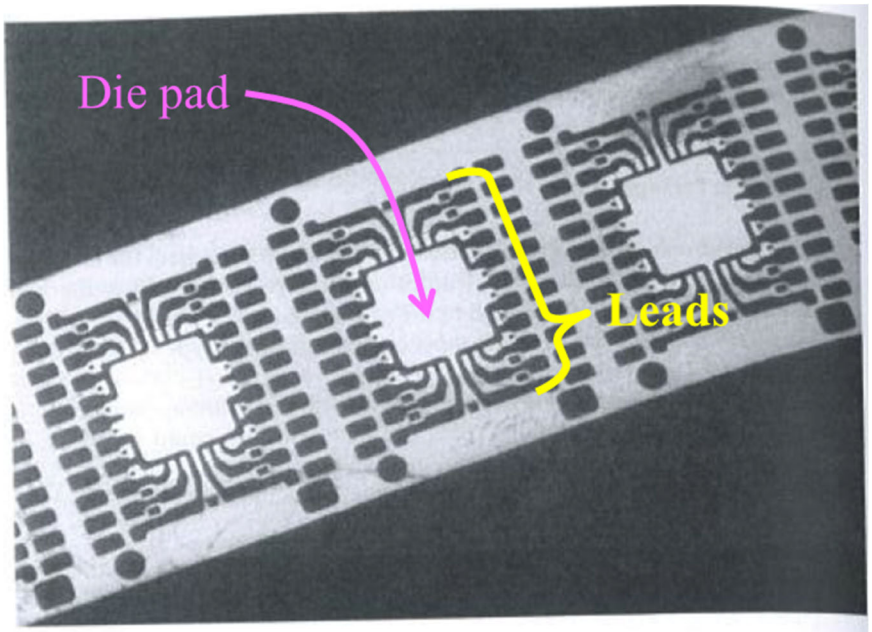
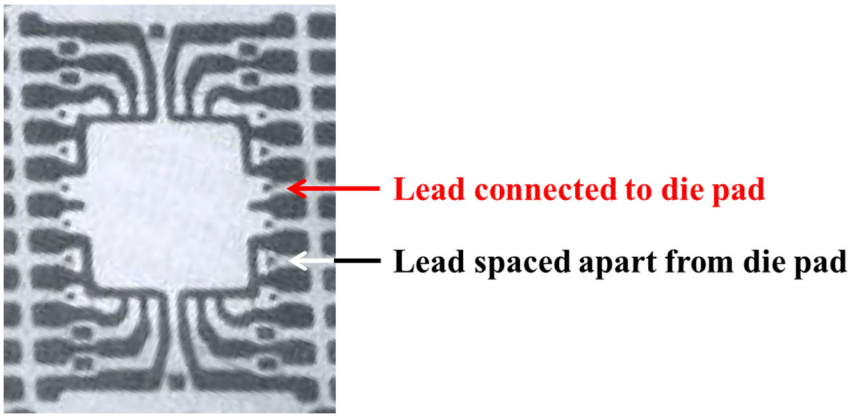


Fig. 13.2 Leadframe of medium power SOP, with heat transfer leads connected to die-pad

A ***die pad*** is the portion of the leadframe on which a die is attached. Ex. 2004, 117, 452. The leadframe also has ***leads***, which are used to connect the die to external electrical components. Ex. 2002, 486. Some of the leads are connected to the die pad and some are spaced a distance apart from the die pad. *Id.*, Fig. 13.2 (below, annotated).



III. INFINEON'S '481 PATENT

Patent Owner Infineon is a world-leading designer and manufacturer of semiconductors, including GaN power transistors, used in a variety of electronic and microelectronic applications and industries. Power transistors are used as a switch or rectifier in power supplies (or power converters). Power supplies convert electric voltage and/or current from a source to the correct voltage, current, and frequency to power a load (*i.e.*, a device or component). For many decades, power transistors and circuits were fabricated primarily using silicon as the semiconductor material. Ex. 1001, 1:17-19. But silicon-based power transistors have limitations that were increasingly tested given increasing power density, switching speed and efficiency requirements for devices, and stricter environmental pollution regulations. *Id.*, 1:25-29.

While semiconductor devices made from GaN and other compounds had emerged as attractive candidates for power applications to carry large currents, support high voltages, and provide fast switching times, "[t]he high voltages and

fast switching times of such devices result in additional challenges for package development." *Id.*, 1:25-29. For example, high switching speeds of a transistor device can result in "a voltage drop across a parasitic source inductance which is sufficiently high to counteract the driving voltage which may result in increased energy loss." *Id.*, 5:39-43.

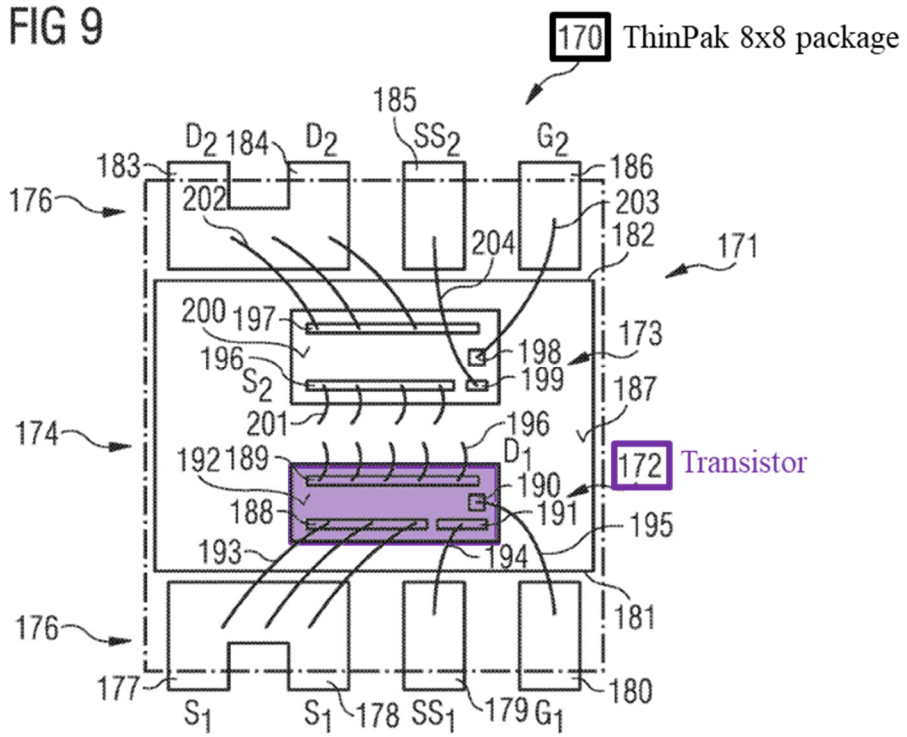
The technology disclosed and claimed in the '481 Patent solves the problem of packaging a GaN lateral transistor in a package having a leadframe by using a "separate connection to the source" – a connection "separate from the connection between the source pad [] and the die pad" – with "a source sense functionality … to exclude the parasitic source inductance from the driver circuit." *Id.*, 5:43-53. The '481 Patent discloses connecting source sensing functionality to a lead that is spaced apart from the die pad. *E.g.*, *id.*, 4:48-51, 63-66, Fig. 1A. The '481 Patent discloses a device that "may have a blocking voltage capability of at least 400V and a switching frequency capability of at least 100 kHz." *Id.*, 15:15-18.

A. Disclosed Embodiments

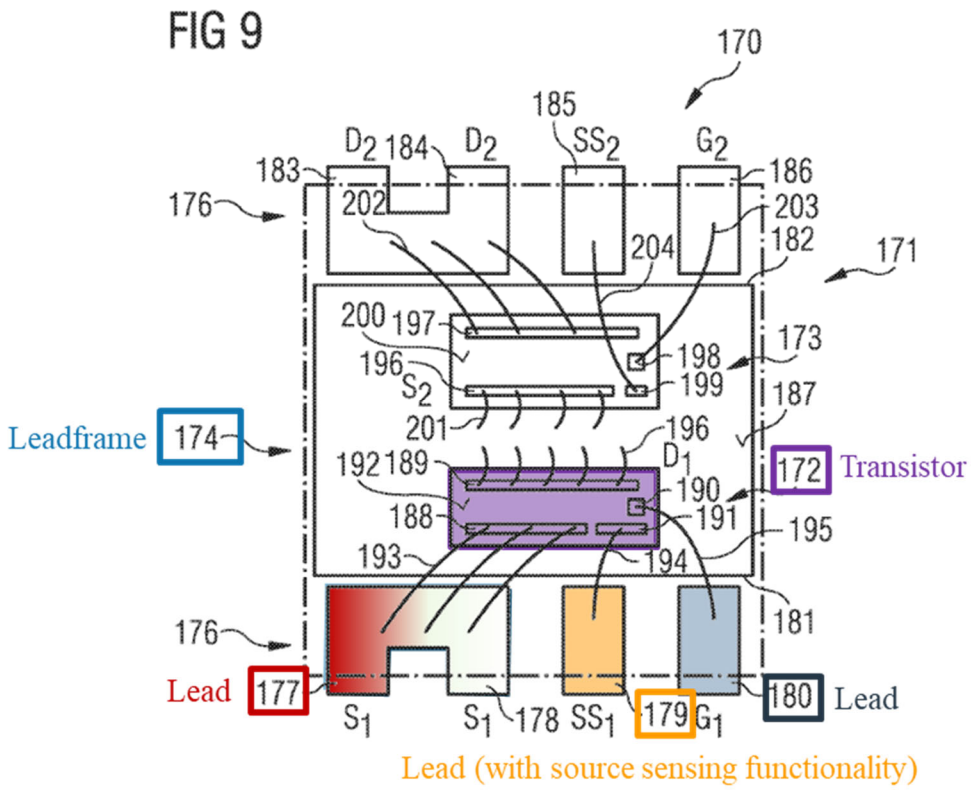
The '481 Patent discloses several embodiments having different package footprints. One is shown in Figure 9, reproduced below.

Figure 9 "illustrates a plan view of an electronic component 170 providing a switch circuit 171 including two **compound semiconductor transistor devices 172**, 173." *Id*, 12:39-41. "The footprint of the electronic component 170 may

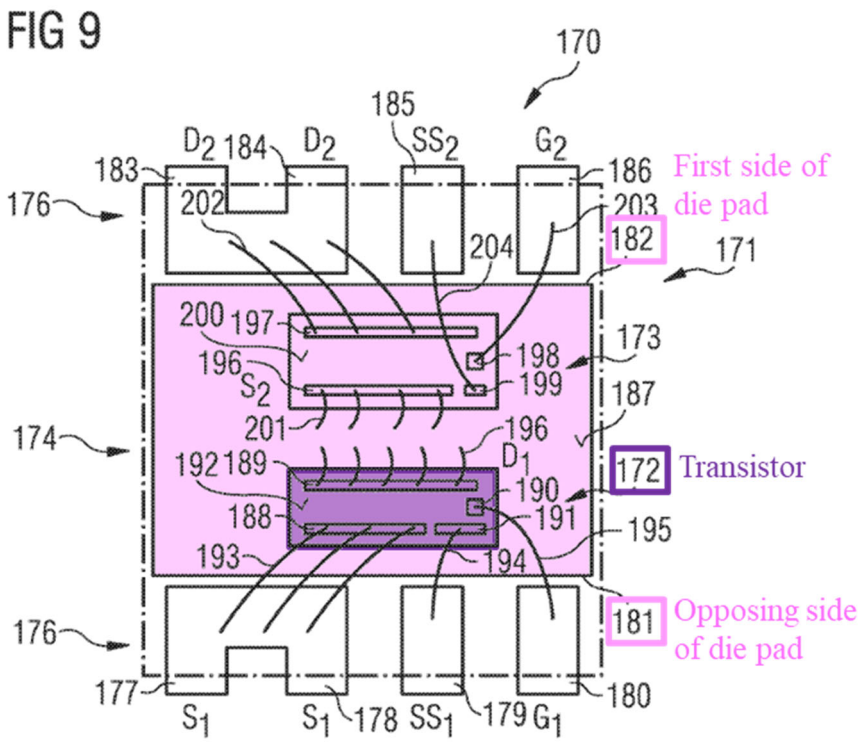
conform to a **ThinPak 8x8 package**." *Id*., 13:45-46. The disclosed transistor devices "may be Group III nitride based High Electron Mobility Transistors, for example." *Id*., 12:61-63.



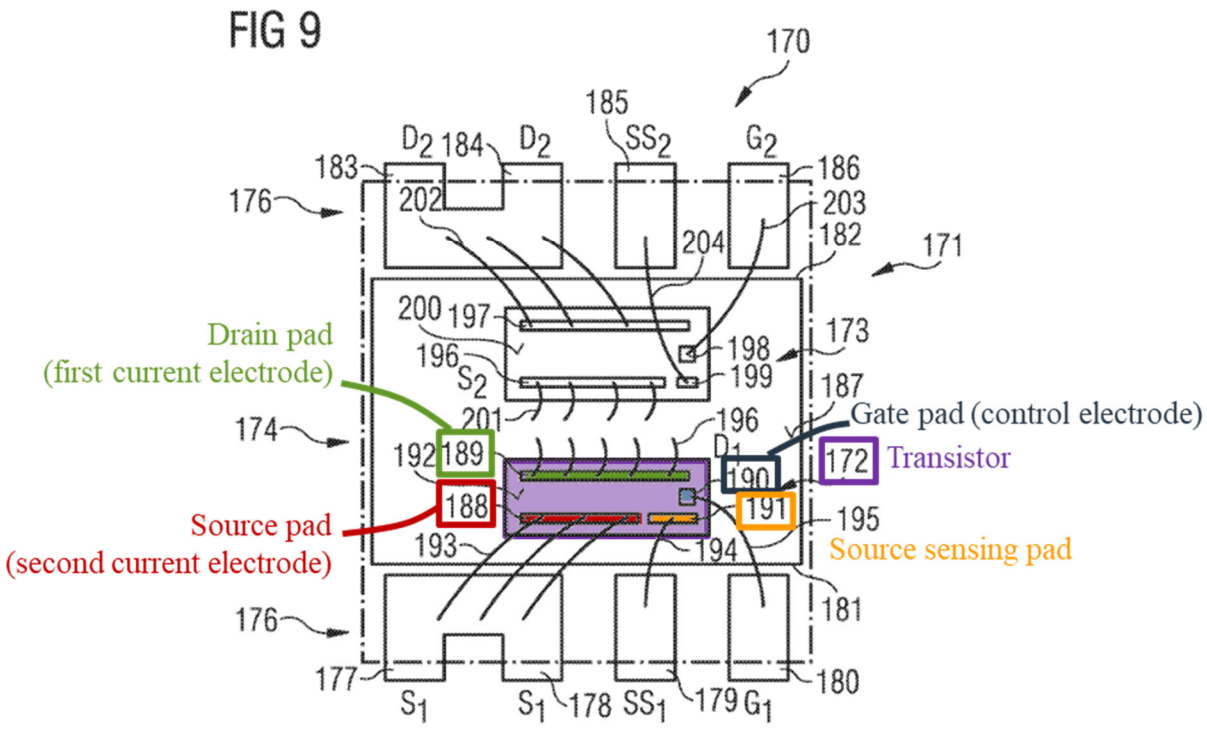
"The electronic component 170 provides a surface mount device (SMD)" with "**a source sense function 179**," "a **leadframe 174**," and nine contact surfaces provided by lower surfaces of the **leads 177**, 178, **179**, **180**, 183, 184, 185, and 186. *Id*., 12:43-55, 13:37-40.



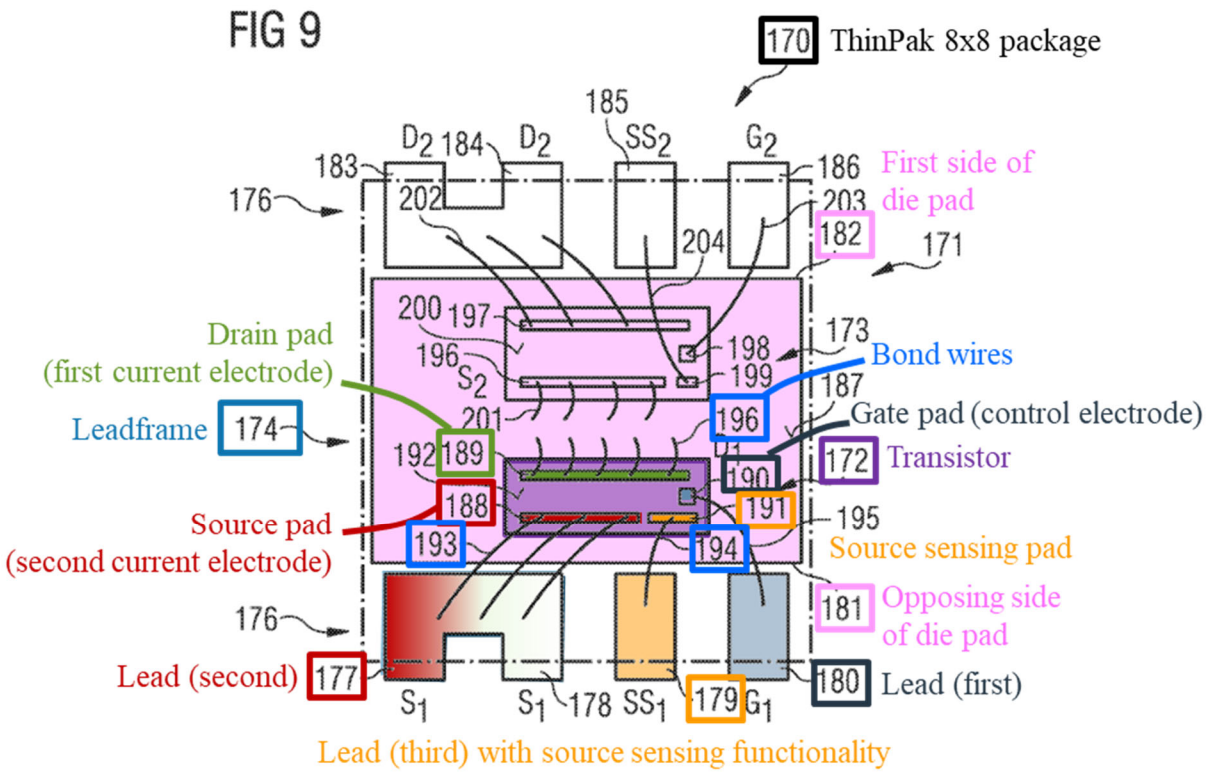
The electronic component also includes "a contact surface provided by the lower surface of the **die pad, which has a first side 181 and opposing side 182**." *Id*., 12:45-55. The "two **transistor devices 172**, 173 are mounted on an upper surface 187 of the **die pad**." *Id*., 12:57-58.



"**[T]ransistor device 172** includes a **source pad 188**, **a drain pad 189**, **a gate pad 190** and **a source sensing pad 191** arranged on its upper surface 192." *Id*., 12:64-66.

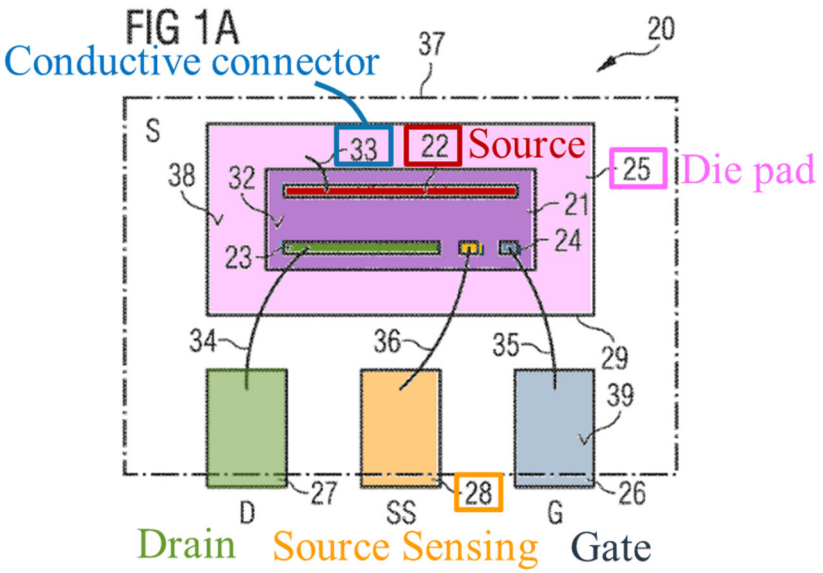


"The **source pad 188** is electrically coupled to the **leads 177**, 178 by one or more bond wires 193." *Id.*, 12:66-13:1. "The **source sensing pad 191** is electrically coupled to the **lead 179** by a bond wire 194 and the **gate pad 190** is electrically coupled to the **outermost lead [180]** on first side 181 of the die pad." *Id.*, 13:1-4. "The **drain pad 189** is electrically coupled to the **die pad** 175 by a plurality of **bond wires 196**." *Id.*, 13:4-6.



The second compound semiconductor transistor device 173 has a similar construction. *Id.*, 13:7-17.

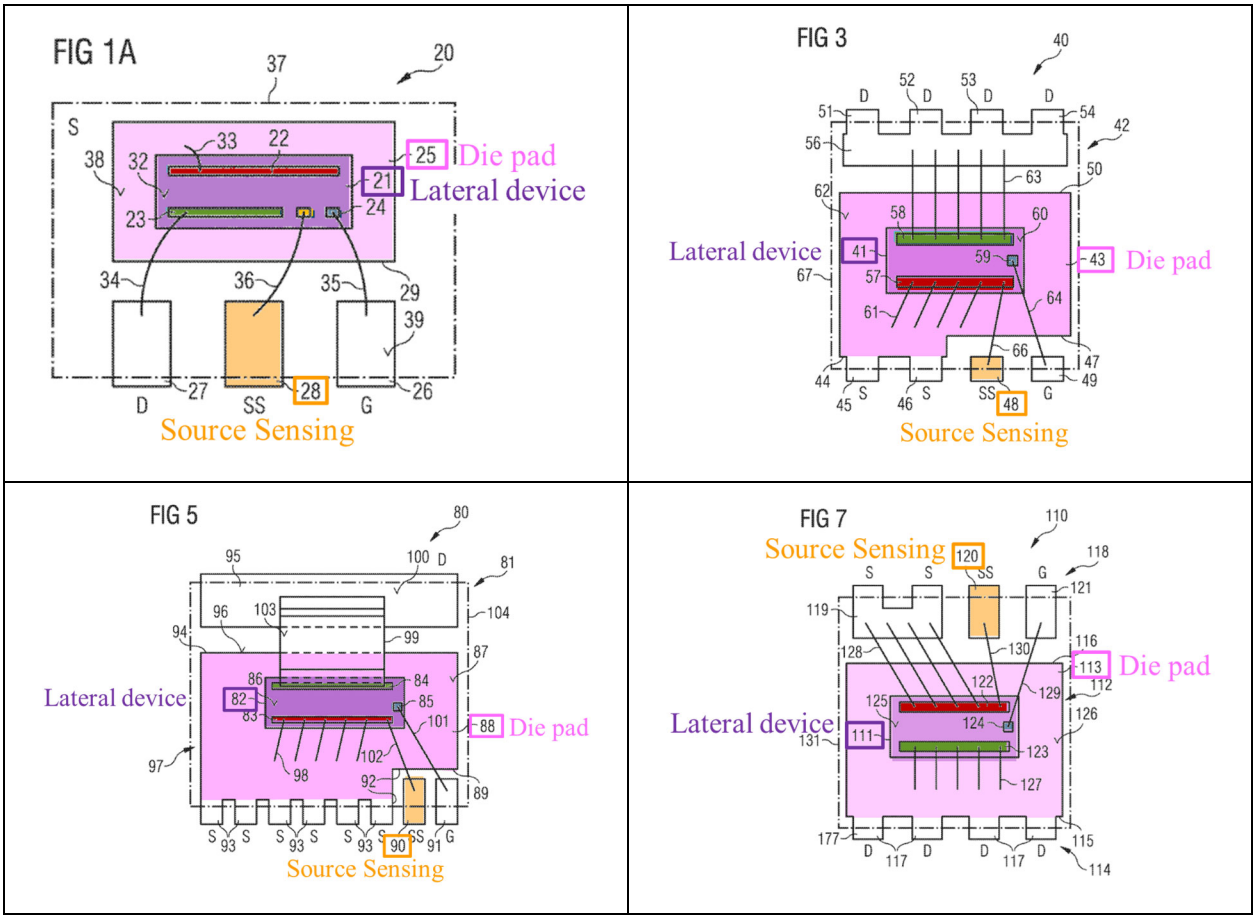
The ’481 Patent discloses another embodiment in Figures 1A-1B, similar to the embodiment disclosed in Figure 9, but with only a single transistor for a smaller package footprint. In the Figure 1A-1B embodiment, “the first current electrode 22 is the source electrode,” as opposed to the drain as in the embodiment of Figure 9, “and is electrically coupled to the die pad 25 by a conductive connector 33.” *Id.*, 4:48-51.



For the embodiment of Figures 1A-1B, "the die pad 25 is coupled to source so that the lower surface 30 of the die pad 25 provides a source contact for the electronic component 20." *Id.*, 4:53-56. The "third lead 28 is coupled to the compound semiconductor transistor device 21 and provides a source sense functionality" separate from the die pad. *Id.*, 4:45-47. The '481 Patent states that "[t]he compound semiconductor transistor device 21 is a lateral device." *Id.*, 4:37-38.

The above embodiments solve the problem of packaging a lateral GaN transistor by using a "separate connection to the source," "separate from the connection between the source pad [] and the die pad," with "a source sense functionality … to exclude the parasitic source inductance from the driver circuit." *Id.*, 5:43-53. In both embodiments illustrated above, source sensing functionality is provided via a lead (28 in Fig. 1A and 179 in Fig. 9) that is spaced apart from the die pad.

The ’481 Patent discloses embodiments that have (1) a lateral transistor (*id*., 4:37-38, 7:51-52, 9:2-5, 10:24-27, 14:44-47) mounted on a (2) die pad (*id*., 4:15-17, 7:34-37, 9:5-7, 10:11-16, 12:43-45, 13:52-57), and (3) a separate lead providing source sensing (“SS”) functionality that is spaced a distance apart from the die pad (*id*., 4:63-5:1, 8:6-10, 9:45-46, 11:58-61). *See also id*. Figs. 1A, 3, 5, 7, 9, 10A.



B. Prosecution History

The application leading to the ’481 Patent, application No. 14/997,914, was filed on January 18, 2016, with twenty claims. Ex. 1002, 151-155. The Examiner

rejected independent claim 1 as anticipated by U.S. Patent Publication No. 2009/0212284 ("Otremba '284") and independent claims 1, 12, and 19 as obvious over U.S. Patent Publication Nos. 2015/0115313 ("Otremba '313") and 2011/0049580 ("Lui '580"). *Id*., 50-54.

The Applicant amended independent claims 1, 12, and 19 to further require that the "first" (claims 1 and 12) or "Group III nitride-based" (claim 19) "transistor device is a ***lateral transistor device***." *Id*., 28-30. The Applicant argued that Otremba '284 and Otremba '313 disclosed vertical transistor devices, not a lateral transistor device, as required by the amended claims, and that the amended claims were not anticipated or obvious for that reason (among others). Ex. 1002, 31-34. The Applicant stated that it "is well-known in the semiconductor arts" that a lateral transistor device is a "transistor in which **current flows across the base** in the **direction <u>parallel to</u>**" the device surface in contrast to vertical transistor "in which current across the base flows in the direction normal to the surface." *Id*., 33 (emphasis original). The Applicant cited http://www.semi1source.com/glossary/default.asp?searchterm=lateral+transistor for the "definition of 'lateral transistor.'" *Id*., 34. Exhibit 2006 is a copy of that webpage as preserved by the Internet Archive in 2016.

The Examiner allowed the amended claims, stating in the Reasons for Allowance that "the prior art of record, either singularly or in combination, does

not disclose or suggest the combination of limitations [including] … wherein the compound semiconductor transistor device is a ***lateral transistor*** device." Ex. 1002, 12-13.

C. Challenged Claims

Petitioner challenges all the claims (claims 1-17) of the '481 Patent ("Challenged Claims"). Claims 1, 10, and 17 are independent. Claims 2-9 and 11-16 depend directly or indirectly from claims 1 and 10, respectively.

IV. THE NEGA GROUNDS FAIL TO DEMONSTRATE A REASONABLE LIKELIHOOD OF PROVING ANY CLAIM UNPATENTABLE

The Nega Grounds (Grounds 1A-F) fail to demonstrate a reasonable likelihood of proving any Challenged Claim unpatentable for at least three independent reasons.

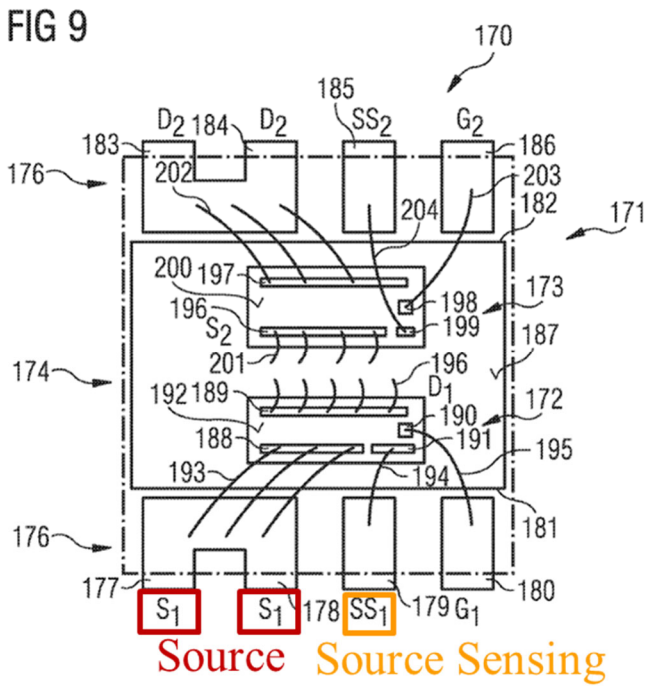
A. Reason #1: Petitioner Proposed a Combination a POSA Never Would Have Made Because Petitioner Conflated Nega's Source and Drain Electrodes

Every independent claim, and thus every Challenged Claim, requires a "third lead … [that] provides a source sensing functionality" (*see* Limitations [1e], [10a], and [17a]) and that the "third lead [is] ***spaced at a distance from the die pad***" (Limitations [1d], [10a], and [17c]). Thus, all Challenged Claims require a third lead that both provides source sensing functionality and is spaced at a distance from the die pad.

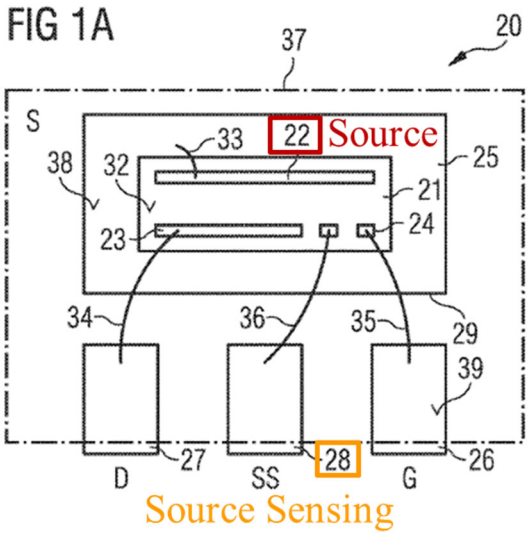
In its attempt to reconstruct the claims in hindsight, Petitioner alleges that a POSA would have added Roberts' source sensing to a lead spaced apart from Nega's leadframe, which Petitioner argues constitutes a die pad. But Petitioner conflated the source and drain electrodes in Nega's transistor and proposed a Nega-Roberts Combination that connects ***source*** sensing functionality to Nega's ***drain*** electrode. A POSA never would have made Petitioner's Nega-Roberts Combination.

1. The Specification Describes Locating Source Sensing Functionality on a Lead Spaced from the Die Pad

The inventors recognized that prior art devices had a problem with "a voltage drop across a parasitic source inductance," "which may result in increased energy loss." Ex. 1001, 5:39-43. The inventors solved this problem by using a "separate connection to the source," "separate from the connection between the source pad [] and the die pad," with "a source sense functionality … to exclude the parasitic source inductance from the driver circuit." *Id*., 5:43-53. The '481 Patent consistently discloses placing the source sensing functionality on a lead that is spaced apart from the die pad rather than on a lead that is connected to the die pad. For example, in the Fig. 9 embodiment, the source is connected to leads 177 and 178 (which are spaced apart from the die pad) and the source sensing functionality is provided to a separate lead that is also spaced apart from the die pad. *Id*., 12:66-13:6, Fig. 9 (below, annotated).



The source sensing functionality is placed on a lead spaced apart from the die pad even in embodiments when the source is connected to leads that are connected to the die pad as shown in the Fig. 1 embodiment below. *Id.*, 4:48-51, 63-66, Fig. 1A (below, annotated).



2. Petitioner Alleges that Nega's Leadframe "Constitutes" a Die Pad

Petitioner argues that Nega discloses a die pad "because it discloses lead frame LF1." Petition, 13-14 ("Nega's lead frame LF1 … ***constitutes*** a die pad."). Petitioner identifies no disclosure in Nega of a die pad. *Id*. Nega never uses the term "die pad." *See generally* Ex. 1005. While a die pad must be part of a leadframe (*see infra* §V.C.1), Petitioner fails to establish that the converse is true, *i.e.*, that ***every*** leadframe must have a die pad. Patent Owner does not concede that Nega discloses a die pad.

For purposes of denying institution, the Board need not resolve whether Nega necessarily discloses a die pad because it discloses a leadframe. That is because even if Petitioner were correct that Nega's leadframe "constitutes a die pad," Petitioner failed to show that a POSA would have added Roberts' source sensing functionality to a lead spaced apart from Nega's alleged die pad. Petition, 13-14. While the claims require a lead spaced apart from the die pad (*see* Limitations [1d], [10a], and [17c]), this paper explains why Petitioner failed to establish that a POSA would have added Roberts' source sensing functionality to a lead spaced apart from Nega's ***leadframe***, because Nega never refers to a ***die pad*** and Petitioner treats Nega's disclosure of a leadframe as disclosure of a die pad. Petition, 13-14.

3. Petitioner Connects Source Sensing Functionality to the Wrong (Drain) Electrode in Nega's HT1 Transistor Device

It is undisputed that source sensing functionality is implemented by providing a "connection to the source." Ex. 1001, 5:43-45; Petition, 18 (Roberts' Kelvin Source Sense connection "enable[s] an external driver device to more cleanly drive the intrinsic ***source***"), 21 ("a 'source-sensing lead may be connected to a ***source*** contact'") (quoting Otremba528).

In an attempt to reconstruct the claims through hindsight by alleging that a POSA would have added source sensing functionality to a lead spaced apart from the die pad, ***Petitioner mislabels the source and drain in Nega's HT1 device***. This is far from a harmless oversight because, as explained below, the lead for the actual source electrode in Nega's HT1 device (rather than the drain electrode Petitioner mislabeled as the source electrode) is connected to Nega's leadframe that Petitioner argues constitutes a die pad. Petitioner does not cite a single reference that describes providing source sensing on a spaced apart lead when the source is connected to the leadframe as Nega discloses.

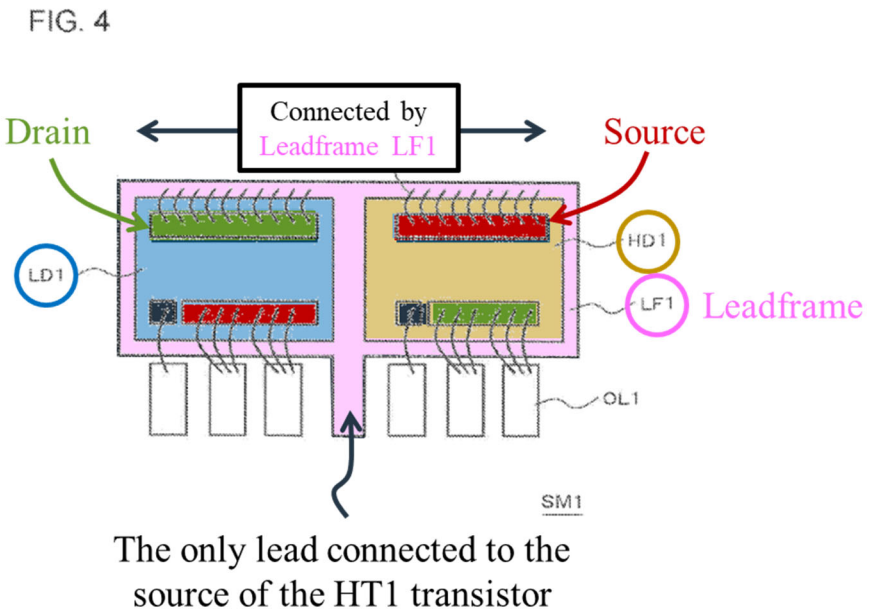
Petitioner alleges that a POSA would have added a lead that provides source sensing functionality to Nega's Fig. 4 embodiment. Petition, 23 ("modifying Nega, Fig. 4 to add Roberts's source sensing third lead"). Fig. 4 shows two side-by-side devices (a high side device and a low side device), each including a transistor. Fig. 4 labels the high side device on the right HD1 and Nega says it has

a transistor HT1. Nega, ¶¶[0090]-[0091]. Fig. 4 labels the low side device on the left LD1 and Nega says it has a transistor LT1. *Id*.

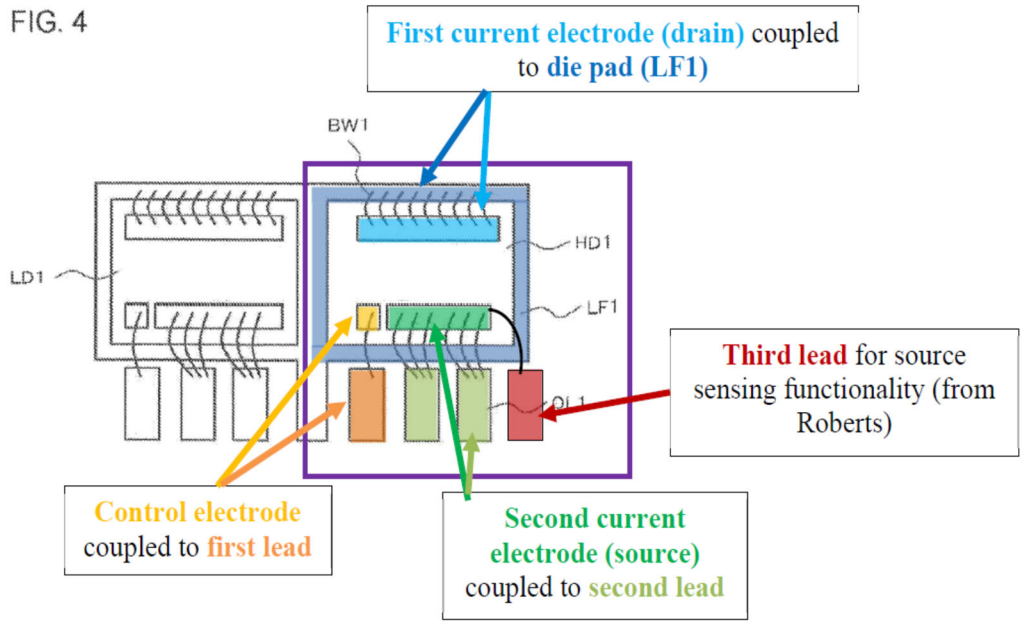
Petitioner calls the right-side transistor a "First transistor." Petitioner sometimes labels this transistor – rather than the entire device – HD1 (*see e.g.*, Petition, 5 and 39) and sometimes refers to this transistor using Nega's terminology by referring to this transistor as HT1 (*see e.g.*, *id*., 39). Petitioner calls the left-side transistor a "Second transistor." Petitioner sometimes labels this transistor – rather than the entire device – LD1 (*see e.g.*, Petition, 5 and 39) and sometimes refers to this transistor using Nega's terminology by referring to this transistor as LT1 (*see e.g.*, *id*., 39).

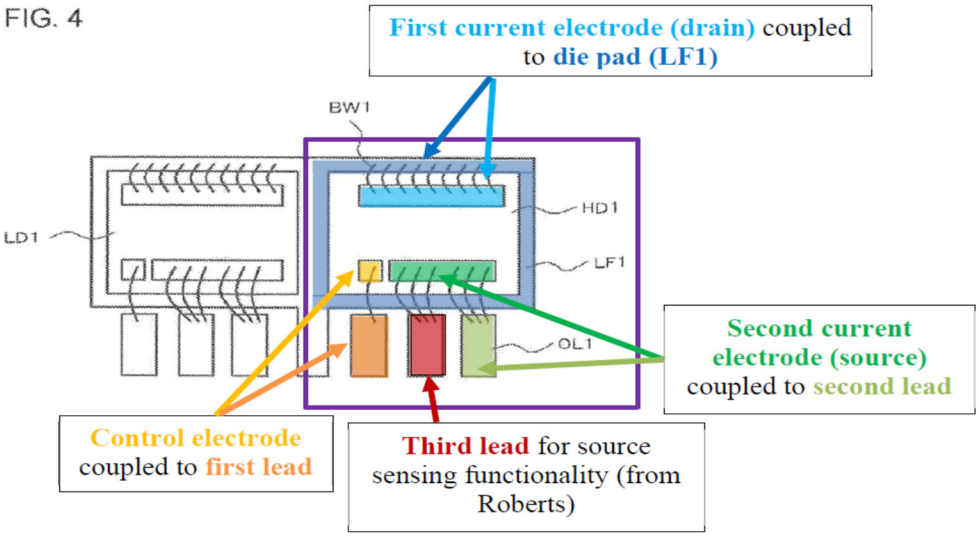
Only the transistor on the right (HT1) is a GaN transistor, thus meeting the claimed requirement of a "compound" or "Group III nitride-based" transistor device, so that is the transistor Petitioner seeks to modify in its combinations and map the claims onto. *See e.g.*, Petition, 4-5, 10-42.

In Nega's Fig. 4 arrangement, the drain of transistor LT1 is connected through the leadframe to the source of transistor HT1. Nega, ¶[0033]. Nega has a single lead for these two connected electrodes, and it is the center lead, highlighted in pink below. That lead is integral to the leadframe and not spaced apart from it like the other leads that are connected to the transistor's electrodes via wires.



As shown in Petitioner's annotated figures reproduced below from the Petition at 23-24, Petitioner alleges that a POSA would have connected source sensing functionality to the bottom right electrode highlighted green in Nega's HT1 transistor. Petitioner mislabels this electrode as the source electrode. But this is the ***drain electrode*** of transistor HT1. As explained below, the source electrode for HT1 is the top electrode that Petitioner highlights blue (and misidentifies as the drain electrode) and is connected to the center lead in Nega's device that is integral with the leadframe.



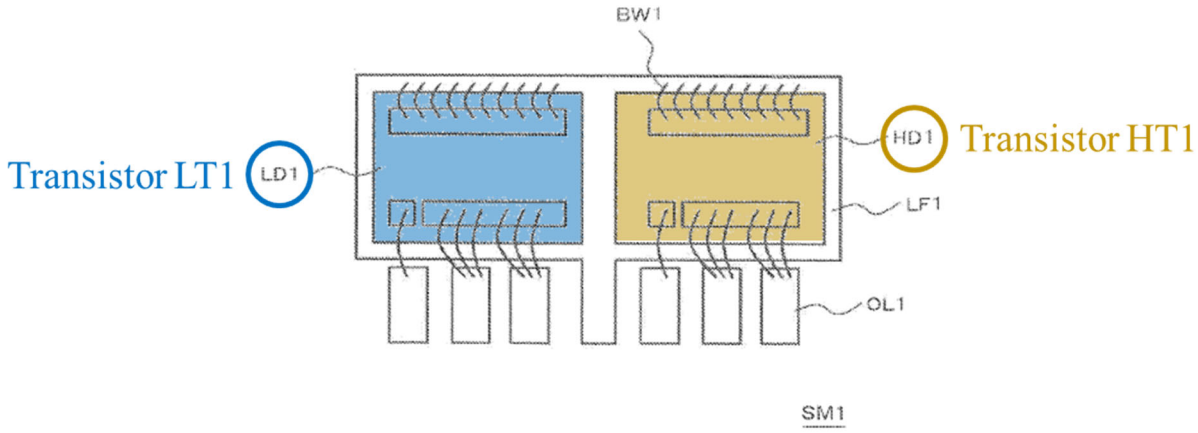


Nega, Fig. 4 (annotated).

Petitioner relies on Nega's first embodiment (described by Nega, ¶¶[0030]-[0107] and Figs. 1-4 and 6). Petition, 4-5, 10-42. Nega states that "FIG. 4 is a plan view illustrating an example of the semiconductor device SM1 according to the present [first] embodiment." Nega, ¶[0090]. In that figure, Nega depicts "a

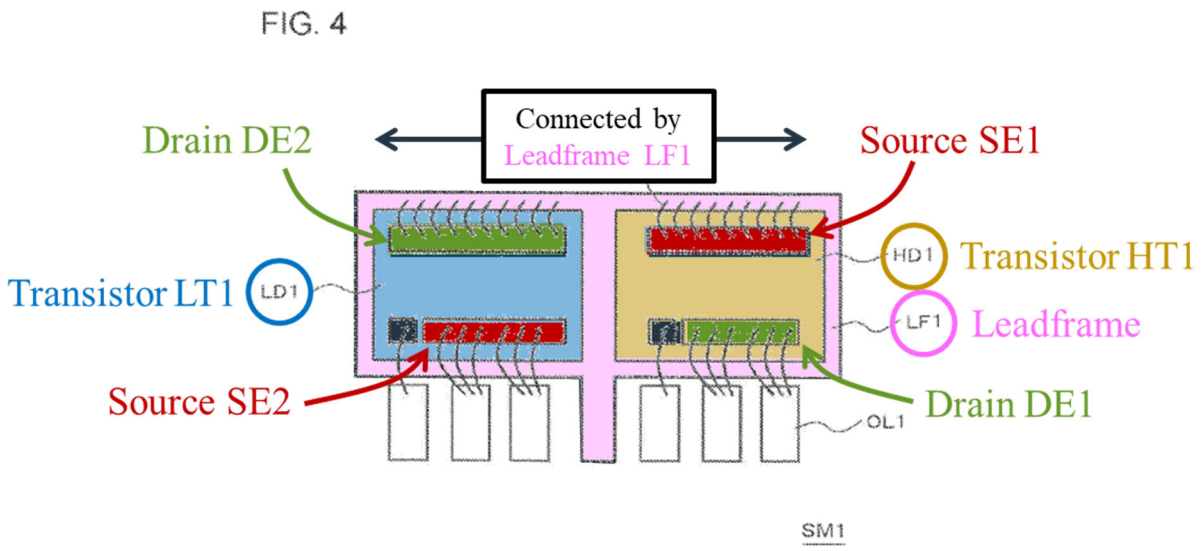
high-side switching device HD1 constituted by the ***transistor HT1*** and a low-side switching device LD1 constituted by the ***transistor LT1***." *Id.*, ¶[0091], Fig. 4 (below, annotated).

FIG. 4



"[A]ccording to the present [first] embodiment," "the transistor LT1 includes a drain electrode DE2 ***connected to the source electrode SE1 of the transistor HT1***, and a grounded source electrode SE2." Nega, ¶[0033]. The electrodes from transistor LT1 and HT1 that are "connected" in Fig. 4 are the top electrodes in both transistors, which are both coupled via wires to the leadframe. These top electrodes that are "connected" are the drain electrode DE2 of transistor LT1 and "***the source electrode SE1*** of transistor HT1." *Id.* Thus, Nega is clear that the ***top*** electrode of transistor HT1 is the source electrode SE1 of transistor HT1 – not the bottom right electrode as Petitioner erroneously alleges. Petition at 4-5, 17, 23-24.

In the figure below, Patent Owner annotates Nega Fig. 4 to ***correctly*** identify the transistor's electrodes consistent with Nega's disclosure.



4. The Board Should Hold Petitioner to its Failed Nega-Roberts Combination and Find that the Nega Grounds Fail

A POSA never would have made the Nega-Roberts device that Petitioner alleges because a POSA never would have added source sensing functionality to the electrode of Nega's transistor that Petitioner alleges because that is the transistor's ***drain*** electrode rather than its ***source*** electrode. *See supra* §IV.A.3. The Nega Grounds fail for this reason alone.

It is not the Board's role to fix problems with the Petition or address arguments Petitioner could have made but did not—the Board's role is to address the arguments the Petition did make. *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1356 (2018) (The Board does not "enjoy[] a license to depart from the petition and institute a different inter partes review of [its] own design.") (emphasis omitted); *In*

re Magnum Oil Tools Int'l, Ltd., 829 F.3d 1364, 1381 (Fed. Cir. 2016) (The Board must "base its decision on arguments that were advanced by a party" and has no power to "raise, address, and decide unpatentability theories never presented by the petitioner."); *Nautilus Hyosung v. Diebold*, IPR2016-00580, Paper 15, 7 (Jan. 31, 2017) ("[t]he Board must base its analysis on the arguments and evidence presented in the petition and not upon what the petitioner *could have* argued.") (emphasis original); *Samsung Elecs. Co. v. Elm 3DS Innovations, LLC*, 925 F.3d 1373, 1383 (Fed. Cir. 2019) ("We will not fault the Board for analyzing Petitioners' obviousness grounds in the way presented in the Petition.").

The Board should reject the Nega Grounds because they are based on a combination that a POSA never would have made.

B. Reason #2: Petitioner Failed to Show that a POSA Would Have Added Roberts' Source Sensing Functionality to a Lead Spaced Apart from a Die Pad as Claimed

Even if the Board were to overlook Petitioner's conflating of the source and drain electrodes in Nega's transistor, and even if the Board were to consider Petitioner to have alleged that a POSA would have added source sensing functionality to the correct (source) electrode in the Nega transistor, the Nega Grounds still fail because Petitioner establishes no reason why a POSA would have used a lead ***spaced apart*** from the leadframe for adding an additional connection to Nega's ***source*** electrode.

1. Petitioner Fails to Establish that a POSA Motivated by Roberts to Modify Nega According to Petitioner's Own Rationale Would Have Arrived at the Claimed Invention

As explained *supra* §IV.A.1, every Challenged Claim requires a third lead that both provides source sensing functionality and is spaced at a distance from the die pad. As explained below, even if a POSA would have been motivated to add Roberts' source sensing functionality to Nega, Petitioner failed to establish any reason why a POSA would have added Roberts' source sensing functionality to a lead spaced apart from Nega's leadframe (alleged die pad) rather than to a Nega lead that is connected to the leadframe. Petitioner thus failed to establish any reason why a POSA would have combined the teachings of Nega and Roberts ***in a manner that meets any Challenged Claim***. *TQ Delta, LLC v. CISCO Sys., Inc.*, 942 F.3d 1352, 1359 (Fed. Cir. 2019) (reversing the Board's obviousness determination; "a conclusory assertion with no explanation is inadequate to support a finding that there would have been a motivation to combine because 'this type of finding, without more, tracks the *ex post* reasoning *KSR* warned of and ***fails to identify any actual reason why a skilled artisan would have combined the elements in the manner claimed***.'") (internal citation omitted).

a. A POSA Would Have Attached Source Sensing Functionality to the Source Electrode of Nega's Transistor

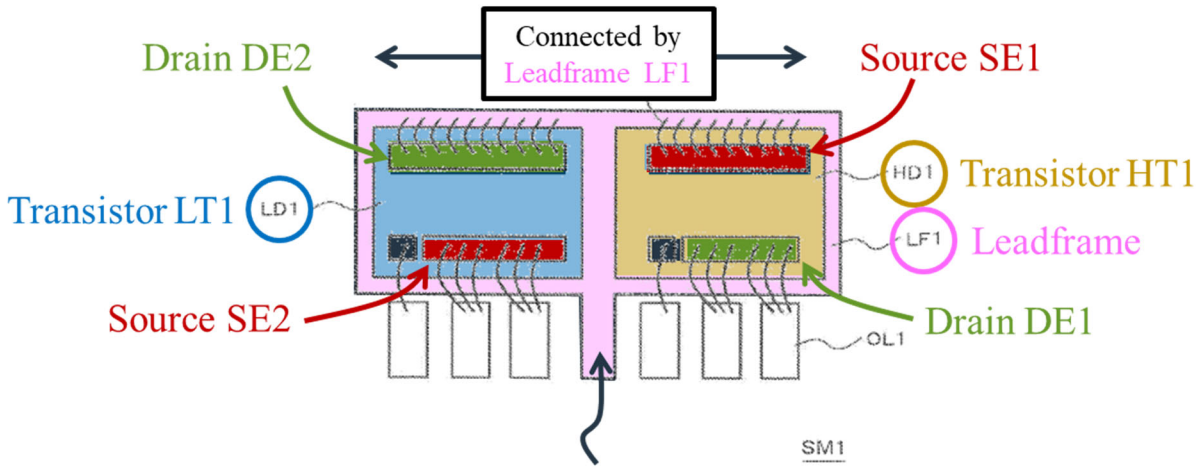
The Petition states that the purpose of Roberts' source sensing functionality was to "enable an external driver device to more cleanly drive the intrinsic ***source***, free of inductive L di/dt noise generated by the high current fluctuations of the ***source***." Petition, 18; *see also* Ex. 1001, 5:43-45 (source sensing functionality is implemented by providing a "connection to the ***source***"). Petitioner further states that Otremba529 achieves "the same purpose as Robert's [sic] Kelvin Source Sense connection" by using a source-sensing lead "connected to a ***source*** contact." Petition, 21. Petitioner illustrates a source sensing lead connected to what Petitioner alleges is the ***source*** electrode of Nega's transistor HT1 transistor. Petition, 23-24 (see annotated figures). Finally, Petitioner alleges a POSA would have modified a lead "***connected to the source electrode***" "to serve as a lead for source sensing functionality." Petition, 23.

Thus, a POSA motivated by Roberts in the manner Petitioner alleges would have connected source sensing functionality to a lead connected to the ***source*** electrode in the HT1 transistor that Petitioner alleges meets the claimed compound semiconductor device. Petition, 11.

b. Nega's Source Electrode Lead is Not Spaced Apart from the Leadframe

The only lead Nega discloses as being connected to the source electrode of the HT1 transistor is the center lead that is integral with and ***connected to the leadframe***. Nega, ¶[0033]; *supra* §IV.A.3. This is shown in Fig. 4 (annotated below) where the source SE1 electrode for transistor HT1 is connected by bond wires to the leadframe, and where the leadframe has a single center lead (highlighted pink) that is integral with the leadframe.

FIG. 4



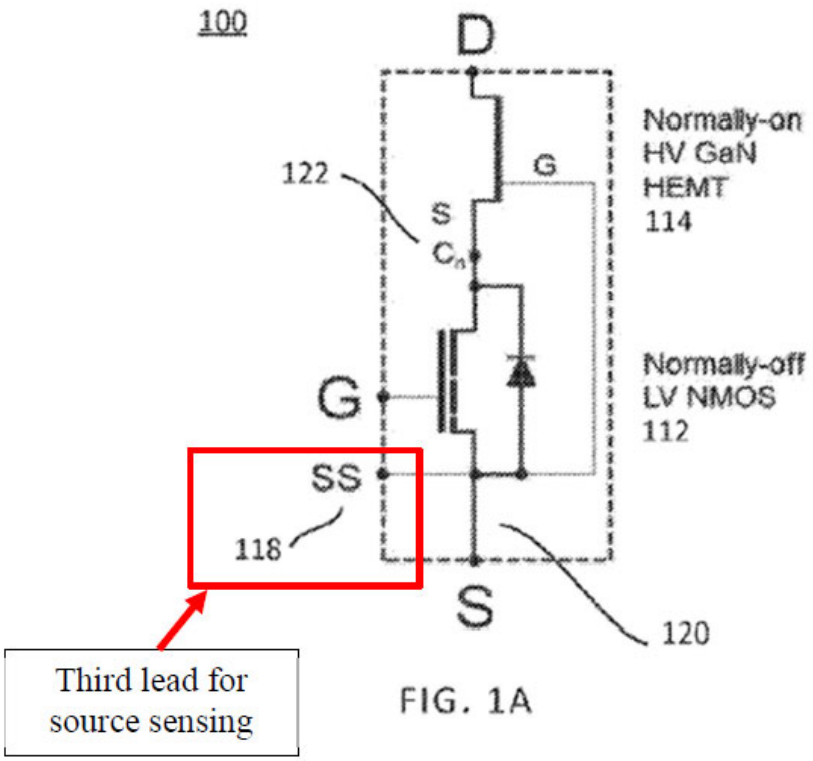
The only lead connected to the source of the HT1 transistor is not spaced a distance from the leadframe

c. Petitioner Failed to Establish Any Reason Why a POSA Would Have Used a Lead Spaced Apart from Nega's Leadframe for Source Sensing

Because it misidentified the source electrode in Nega's HT1 transistor (*see supra* §IV.A.3), the Petition failed to address the fact that Nega teaches connecting to the source electrode via a lead connected to the leadframe. Petitioner never

established any reason why a POSA would have used a spaced apart lead for a source sensing connection despite Nega only teaching a connection to the source electrode of transistor HT1 via a lead integral with the leadframe.

Petitioner alleges that a POSA would have been motivated by Roberts to add source sensing functionality to Nega and annotates Roberts' figure to illustrate a "Third lead for source sensing." Petition, 18-19. As shown by Petitioner's annotated figure (reproduced below), Roberts teaches applying source sensing to a lead that is connected directly to the transistor's source electrode (labeled S in the annotated Roberts figure). Petitioner never alleges, let alone establishes, any reason why a POSA would have used a lead spaced apart from Nega's leadframe to provide another connection to Nega's source electrode rather than using a lead that is integral with and connected to the leadframe for connecting to the source electrode as taught by Nega.



Id., Fig. 1A (annotated).

Petition, 19.

Petitioner implicitly alleged that a POSA would have used the same type of lead taught by Nega to make multiple connections to an electrode. In this respect, as shown by Nega's Fig. 4 that Petitioner annotates (Petition, 23-24), Nega teaches using leads that are spaced apart from the leadframe when connecting to the electrode to which Petitioner alleged a POSA would have added source sensing functionality. Petitioner annotated Nega's Fig. 4 to add source functionality via a "third lead" in two alternative ways, both of which use a lead that is spaced apart from the leadframe like the other leads used to connect to that same electrode. Petition, 23-24.

When Petitioner's rationale is applied for coupling to the ***actual source electrode*** in Nega—rather than the drain electrode Petitioner erroneously mislabeled (*see supra* §IV.A.3)—a POSA would have used a lead that is connected to Nega's leadframe to add source sensing functionality because Nega's existing lead to the source electrode of the HT1 transistor is connected to the leadframe. Following this rationale would have yielded a Nega-Roberts Combination that would not meet any Challenged Claim because it would not have a source sensing lead spaced a distance from the die pad (Petitioner argues Nega's leadframe constitutes a die pad) as required by every Challenged Claim.

It was insufficient for Petitioner to establish a reason to combine the prior art references in ***some*** way. To demonstrate any Challenged Claim obvious, Petitioner needed to establish some ***reason why*** a POSA "would have… combined [the] prior art elements" in a manner that "***yield[s] the claimed invention***." *Unigene Lab. v. Apotex*, 655 F.3d 1352, 1360 (Fed. Cir. 2011); *see also KSR Int'l v. Teleflex*, 550 U.S. 398, 418-20 (2007) (establishing obviousness requires establishing some ***reason*** to combine the prior art in the manner claimed); *TQ Delta*, 942 F.3d at 1359 ("a conclusory assertion with no explanation is inadequate… because [it]… ***fails to identify any actual reason why a skilled artisan would have combined the elements in the manner claimed***.'").

To prove the Challenged Claims obvious, Petitioner needed to establish some ***reason why*** a POSA would have not only added Roberts' source sensing functionality to Nega, but more specifically would have done so by adding source sensing functionality to a lead spaced apart from the die pad as Petitioner alleges (Petition, 23-24) rather than to a lead connected to the die pad. Petitioner ***did not even allege such a reason***, let alone substantiate any (unstated) reason with evidence.

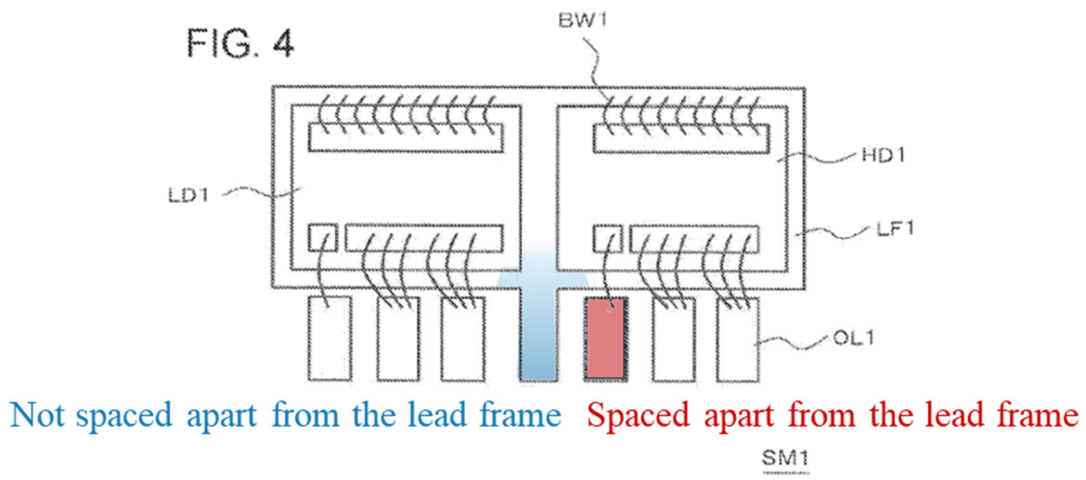
In arguing that a POSA had a reason to add Roberts' source sensing functionality to Nega, Petitioner simply alleged in conclusory fashion that a POSA would have added source sensing functionality to a "separate lead." Petition, 21-22. The Petition presents two versions of its Nega-Roberts Combination. In one version, Petitioner draws in a new "third lead" for source sensing functionality and that lead is spaced apart from Nega's leadframe like the other leads for that same electrode.[4] *Id*., 23. In the other version, Petitioner chooses one of Nega's existing

[4] Petitioner could not have proposed using a lead integral with the leadframe for connecting to the green highlighted electrode (misidentified as HT1's source electrode) because doing so would have created a short-circuit (via the leadframe) between the green and blue electrodes because Nega Fig. 4 shows that the blue electrode is wired to the leadframe.

leads that is spaced apart from its leadframe and "repurpose[s]" it by labeling it as a "third lead" to which Roberts' source sensing functionality is added. *Id*., 23-24. A POSA never would have made either combination because both purport to add source sensing functionality to transistor HT1's drain electrode rather than its source electrode. *See supra* §IV.A.3.

But even if the Board were to rewrite the Petition's Nega Grounds to allege that a POSA would have added source sensing functionality to the electrode that is the correct source electrode for Nega's HT1 transistor, the Nega Grounds still fail because Petitioner failed to provide any ***reason why*** a POSA would have added source sensing functionality by using a lead spaced apart from Nega's leadframe rather than by using a lead connected to the leadframe.

Nega's Fig. 4 embodiment that Petitioner relies on has a single lead (**blue** below) to the source electrode of the HT1 transistor and – unlike the leads (**red** below) to the drain electrode (that Petitioner misidentified as the source electrode), the single lead for the HT1 source electrode is connected to the leadframe, not spaced apart from it. Petitioner never alleged any reason why a POSA would have added Roberts' source sensing functionality to Nega's source electrode by using a different (spaced apart, **red**) lead rather than by using the type of lead (connected to the leadframe, **blue**) that Nega teaches for its connection to the source electrode of the HT1 transistor.



Given that Petitioner did not even allege a reason why a POSA would have added Roberts' source sensing functionality to Nega's source electrode by using a different (spaced apart) lead rather than the type of lead (connected) that Nega teaches for connecting to the source electrode, Petitioner manifestly failed to substantiate any (unstated) reason with ***evidence***.

Petitioner's failure to establish some evidence-based reason why a POSA would have added Roberts' source sensing functionality to Nega using a lead ***spaced apart*** from the leadframe is fatal to all the Nega Grounds (Grounds 1A-1F). *Unigene Lab.*, 655 F.3d at 1360 (Petitioners needed to establish some ***reason why*** a POSA "would have… combined [the] prior art elements" in a manner that "***yield[s] the claimed invention***."); *KSR*, 550 U.S. at 398 (establishing obviousness requires establishing some ***reason*** to combine the prior art in the manner claimed); *TQ Delta*, 942 F.3d at 1359 (same).

2. No Credible Evidence Supports Petitioner's Arguments

Petitioner makes conclusory statements such as "Nega-Roberts teaches the following configuration" (Petition, 22) and shows adding a source sensing lead spaced a distance apart from Nega's leadframe (*id*., 23-24). But as explained above, Petitioner did not establish any reason why a POSA would have combined the teachings of Nega and Roberts in that way. The Petition cites five paragraphs of the Lebby declaration. But the Lebby declaration cannot save the Nega Grounds because nothing in the Lebby declaration can be incorporated by reference into the Petition. *Instrumentation Lab'y v. Hemosonics*, IPR2017-00855, Paper 55, 20 (Feb. 13, 2019)) ("[a]rguments and information that are not presented and developed in the Petition, but instead are incorporated by reference, are not entitled to consideration, as it is improper to incorporate by reference arguments from one document into another document." (citing 37 C.F.R. § 42.6(a)(3)); 37 C.F.R. § 42.104(b)(5) (the ***Petition*** "must" identify "the ***relevance*** of the evidence to the challenge raised, including ***identifying specific portions of the*** evidence that support the challenge.").

Regardless, the cited portions of the Lebby declaration do nothing more than parrot the Petition nearly verbatim so the testimony shares the same above-discussed shortcomings that the Petition has. *Compare* Petition, 22-24 *with* Lebby ¶¶[0110] and [0112]-[0115]. This type of unsupported conclusory testimony that

simply parrots the Petition warrants no weight under the Board's precedential *Xerox* decision. *Xerox Corp. v. Bytemark, Inc*., IPR2022-00624, Paper 9 at 15 (PTAB Aug. 24, 2022) (precedential) ("the cited declaration testimony is conclusory and unsupported, adds little to the conclusory assertion for which it is offered to support, and is entitled to little weight. *See* 37 C.F.R. § 42.65(a) ('Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.')").

The Board routinely denies institution where the petition is supported by little more than experts who merely repeat conclusory assertions articulated in the petition. *See e.g. Tesla v. Nikola*, IPR2019-01646, Paper 7, 19 (PTAB Mar. 27, 2020) (denying institution, holding "Mr. Baker's testimony simply repeats the conclusions articulated in the Petition" which "is entitled to little or no weight.") (quoting 37 C.F.R. § 42.65(a)); *One World Techs. v. Chervon*, IPR2020-00885, Paper 21, 29 (PTAB Nov. 6, 2020) (similar); *Fitbit v. Koninklijke Philips*, IPR2020-00774, Paper 13, 25 (PTAB Oct. 16, 2020) (similar); *Micro-Tech (Nanjing) v. Bos. Sci. Scimed.*, IPR2020-00185, Paper 11, 19-20 (PTAB May 4, 2020) (similar); *Initiative for Med., Access & Knowledge (I-Mak) v. Gilead Pharmasset*, IPR2018-00122, Paper 10, 21 (PTAB May 21, 2018) (similar).

Dr. Lebby's testimony cannot save the Petition from its above-identified failing to establish some reason why a POSA would have combined the teachings

of Nega and Roberts in a manner that meets the Challenged Claims by using a lead spaced a distance apart from Nega's leadframe to provide source sensing functionality.

C. Reason #3: Petitioner Failed to Show that Nega Discloses a Lateral Transistor as Claimed

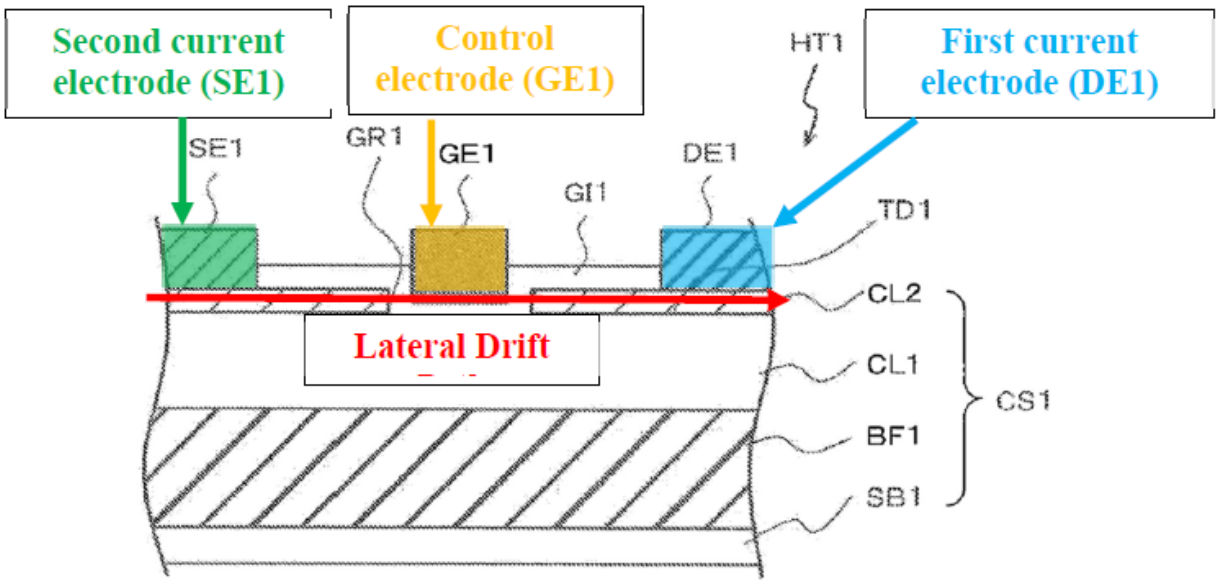
Despite the fact that the claims were amended to recite a ***lateral*** transistor to distinguish over the prior art, and the Examiner cited that in the reasons for allowance (*supra* III.B; Ex. 1002, 12-13), Petitioner failed to establish that Nega discloses a lateral transistor.

Petitioner cites no express disclosure in Nega of a lateral transistor. Petition, 24-25. Petitioner also fails to establish that Nega inherently discloses a lateral transistor and Nega manifestly does not do so. The Nega Grounds fail because Petitioner failed to show that Nega discloses a lateral transistor as required by every Challenged Claim.

1. Petitioner Relies on the Location of the Electrodes for Nega's Transistor

Petitioner argues that Nega discloses a lateral transistor "because [Nega's transistor] HT1 is arranged laterally—gate, source, and drain side by side on the same lateral plane in a lateral drift path—and either of its source or drain is coupled to the lead frame LF1 (die pad)." Petition, 24-25 (using the annotated figure reproduced below).

FIG. 2



Nega, Fig. 2 (annotated).

Petitioner misapprehends what characterizes a transistor as a lateral transistor and conflates the location of the transistor's electrodes with the direction that current flows within the transistor. Petitioner highlights the location of the electrodes. But all the ***electrodes*** being "arranged laterally" on one side of the substrate does not—as Petitioner alleged (*id.*)—mean a transistor is a lateral transistor. Indeed, vertical transistors were known in which all the electrodes were "arranged laterally" on one side of the substrate (*infra* §IV.C.2).

Moreover, Petitioner draws a red arrow that purports to show where the "lateral drift" is in Nega's transistor, but Petitioner is demonstrably wrong. The area through which Petitioner drew a red arrow to identify where "lateral drift"

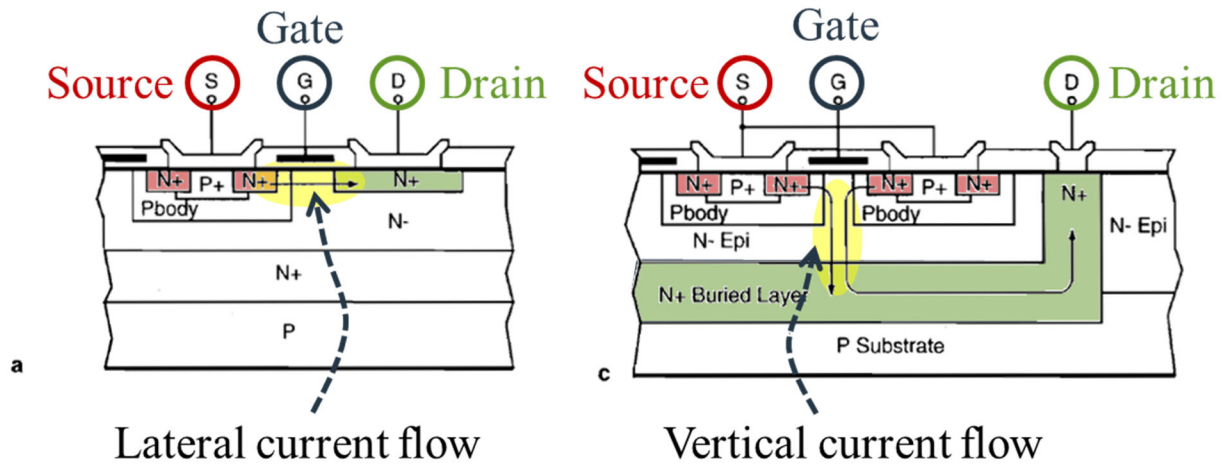
allegedly occurs in Nega's transistor is a "gate ***insulating*** film GI1." Nega, ¶[0069]. It is beyond dispute that current does not pass through an "insulating film." Ex. 2001, 52 ("Insulators are used to isolate conducting regions at different electric potentials so that no current flows between them."). Petitioner's characterization of Nega's transistor is manifestly wrong and cannot carry Petitioner's burden to prove that Nega's transistor is a lateral transistor.

Petitioner failed to establish that Nega teaches, either expressly or inherently, that its transistor is a lateral transistor as required to meet the Challenged Claims.

2. A Lateral Transistor Cannot Be Identified by the Placement of the Transistor's Electrodes

As explained in Section II.A above, a ***lateral transistor*** is a "transistor in which current flows "in the direction **parallel to**" the device's surface. Ex. 1002, 33-34 (emphasis original). In contrast, in a ***vertical transistor***, current "flows in the direction **normal to the surface**." *Id*. The difference is illustrated below.

Example of a Lateral Transistor **Example of a Vertical Transistor**



Ex. 2002, 7-8 ("lateral structure" shown in "Fig. 1.7a," and "current flow is vertical in the power device structure" in "Fig. 1.7c"), Fig. 1.7a-c (annotated); *see also* Ex. 2003, 1937 ("Fig. 3(a) … preserves a vertical high-voltage transistor structure"), Fig. 3(a).

The electrodes in ***both*** the lateral and vertical transistors shown above are "arranged laterally" on the top of the substrate.

3. Nega's Electrodes Being "Arranged Laterally" on Top of the Substrate Does Not Expressly or Inherently Disclose a Lateral Transistor

By statute, the Petition must state its grounds "with particularity." 35 USC § 312(a)(3). The Board has promulgated two rules specifying "Content" the petition "must have" to meet this particularity requirement. Those rules require that the Petition identify and explain the prior art evidence that supports the challenge. 37 C.F.R. § 42.22 (the petition "must" include a "***detailed explanation***

of the significance of the evidence"); 37 C.F.R. § 42.104(b)(4) ("[t]he petition must specify ***where each element of the claim is found in the prior art*** patents or printed publications relied upon").

Petitioner alleges that "Nega's source, drain, and gate are spread laterally in a lateral drift path, instead of vertically stacked." Petition, 24-25. But the ***only evidence*** Petitioner cites to allegedly support this assertion is Nega's Fig. 2. *Id*. Petitioner's argument that Nega's Fig. 2 transistor has a "lateral drift path" is based on the false assumption that the transistor's ***electrodes*** being arranged laterally means the transistor's "drift path" is lateral so the transistor is a lateral transistor.[5] *Id*. ("HT1 is arranged laterally—gate, source, and drain side by side on the same lateral plane"). But as shown *supra* §IV.C.2, immediately above, both lateral and vertical transistors can have their ***electrodes*** "arranged laterally" on the top of the substrate.

The only other "analysis" Petitioner provides is to draw a red arrow purporting to show where the "lateral drift" is in Nega's transistor. Petitioner erroneously assumes that Nega works like the lateral transistor illustrated below

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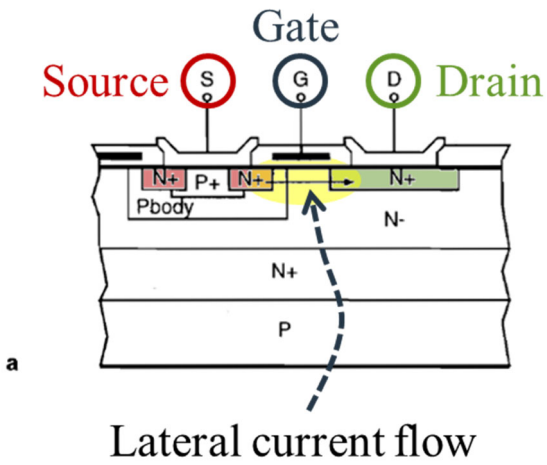
[5] Petitioner makes the same erroneous assertion in connection with the Liu Grounds in alleging that Liu's transistor is a lateral transistor based solely on the location of the transistor's electrodes. *See infra* § V.B.

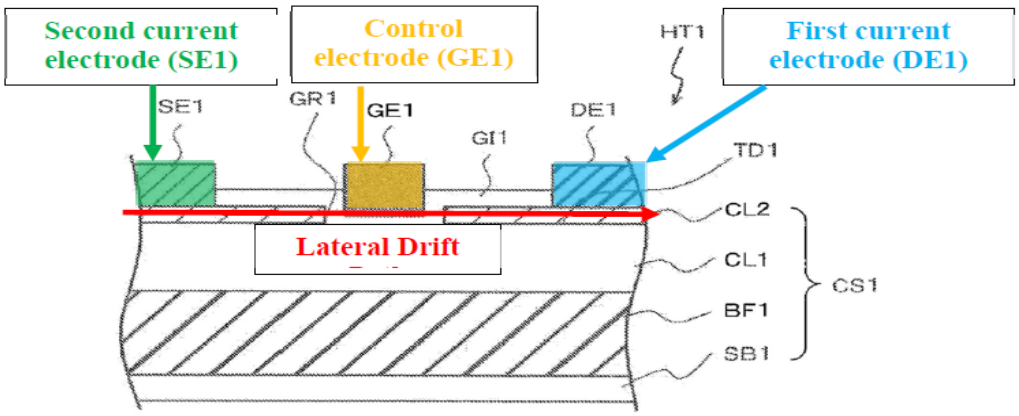
left where the current flows laterally between the source and drain regions. But that is manifestly untrue.



Ex. 2002, 7-8, Ex. 2003, 1937.

As shown below, the area between what Petitioner alleges are the source and drain regions in Nega's transistor, and through which Petitioner draws its alleged "Lateral Drift," is labeled GI1. *See* Petition, 25. But GI1 is a "gate ***insulating*** film GI1." Nega, ¶[0069]. Current cannot pass through an "insulating film." Ex. 2001, 52 ("Insulators are used to isolate conducting regions at different electric potentials so that no current flows between them."). Nega's transistor simply does not work in the manner that Petitioner assumed because Petitioner's characterization of Nega's transistor is manifestly wrong.

FIG. 2



Nega, Fig. 2 (annotated).

For the "element" in Limitation [1f] that requires a "lateral transistor," Petitioner only alleges that it is found in the prior art in Nega. Petitioner does not rely on any teaching in Roberts to meet Limitation [1f] and does not allege that a POSA would have modified Nega's Fig. 2 transistor in any way to meet Limitation [1f]. Thus, Petitioner's showing depends entirely on Nega either expressly or inherently disclosing that its Fig. 2 transistor is a lateral transistor. But Petitioner fails to establish that either is true.

No express disclosure: In terms of "where" the lateral transistor element is allegedly "found in the prior art" (37 C.F.R. § 42.104(b)(4)), the Petition cites no disclosure in Nega other than Fig. 2. Petition, 24-25. But Nega's Fig. 2 plainly does not disclose where the transistor's "drift path" is and does not disclose that the transistor is a lateral transistor. The arrangement of the ***electrodes*** laterally, as relied on by the Petition, fails to expressly disclose a lateral transistor because

vertical transistors can also have their electrodes "arranged laterally" on top of the substrate. *Supra* §IV.C.2. And Nega's Fig. 2 does not disclose that its "Lateral Drift" path is where Petitioner alleges because current will not flow through Nega's insulating film GI1. Nega, ¶[0069]. Petitioner cannot carry its burden to prove that Nega expressly discloses that its transistor is a lateral transistor by citing only to Nega's figure and then erroneously alleging that it discloses a "drift path" through an insulating layer. Petitioner fails to prove that Nega expressly discloses that its transistor is a lateral transistor as required by Limitation [1f].

No inherent disclosure: Given that Nega does not expressly disclose that its transistor is a lateral transistor, the Petition could only substantiate its assertion that "Nega discloses" this (Petition, 24-25) if Nega inherently disclosed a lateral transistor. *LBT IP I LLC v. Apple Inc*., 2023 WL 3914920, at *3 (Fed. Cir. June 9, 2023) ("It is undisputed that [the prior art reference] does not expressly disclose" a claim limitation so petitioner's "argument regarding [the prior art reference]'s disclosure is substantively one of inherency"). But Petitioner does not even allege that Nega inherently discloses a lateral transistor, let alone meet the high burden required to establish inherency.

Establishing inherency would have required Petitioner to demonstrate that Nega's Fig. 2 transistor is "necessarily" a lateral transistor because it cannot be a vertical transistor. *Guangdong Alison Hi-Tech Co. v. Int'l Trade Comm'n*, 936

F.3d 1353, 1364 (Fed. Cir. 2019) ("An element may be inherently disclosed only if it is ***necessarily*** present, not merely probably or possibly present, in the prior art.") (internal quotation marks and citations omitted). Petitioner does not carry that burden. Petitioner fails to even allege, let alone prove, that Nega's Fig. 2 transistor cannot be a vertical transistor. *See supra* §IV.C.2. Petitioner does not remotely establish that Nega inherently discloses that its Fig. 2 transistor is a lateral transistor.

4. Petitioner's Expert Does Not Credibly Support Petitioner's Assertion that Nega Discloses a Lateral Transistor

In connection with Limitation 1[f], Petitioner cites Lebby, [0116]-[0118], without any explanation of the content or relevance of those three paragraphs. Petition, 25. The Lebby declaration does not and cannot support Petitioner's arguments for two reasons.

First, "[a]rguments and information that are not presented and developed in the Petition, but instead are incorporated by reference, are not entitled to consideration." *Instrumentation Lab'y*, IPR2017-00855, Paper 55 at 20; *see also* §IV.B.2 (citing other authority). The three paragraphs of the Lebby declaration string-cited by the Petition without any explanation should not even be considered.

Second, Lebby paragraphs [0116]-[0118] merely parrot the Petition's Limitation [1f] analysis verbatim without citing any documentary evidence to support the conclusory assertion that Nega discloses a lateral transistor. *Compare*

Petition, 24-25 *with* Ex. 1003 ¶¶[0116]-[0118]. This testimony warrants no weight under the Board's precedential decision in *Xerox*, IPR2022-00624, Paper 9, at 14-16 ("[T]he cited declaration testimony is conclusory and unsupported, adds little to the conclusory assertion for which it is offered to support, and is entitled to little weight.") (citing 37 C.F.R. § 42.65(a) ("Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight")). Because Dr. Lebby merely parrots the Petition verbatim, Dr. Lebby's analysis is unsupported and facially deficient for the same reasons the Petition's arguments are.

5. Conclusion: The Petition Failed to Establish that the Nega-Roberts Device Has a Lateral Transistor as Claimed

The Petition failed to establish that Nega expressly or inherently discloses a lateral transistor. Ground 1A fails for claim 1 for this independent reason.

D. The Remaining Claims in Ground 1A and the Remaining Nega Grounds Inherit the Petition's Flawed Analysis of Claim 1 in Ground 1A

Like claim 1, claims 10 and 17 also require a spaced apart lead used for source sensing. *See* Limitations [10a], [17a], and [17c]. Petitioner's analysis of those limitations in Grounds 1A, 1B, 1C, and 1D merely cross-references the Petition's analysis for claim 1. Petition, 36 (Limitation [10a]), 50-51 (Limitations [17a] and [17c] in Ground 1B), 62-63 (Limitations [17a] and [17c] in Ground 1C and 1D). Because Petitioner did not meet its burden to establish the Nega-Roberts

Combination has a spaced apart lead used for source sensing in its claim 1 analysis (*see supra* §IV.A-B), it failed to meet its burden to establish the same for claims 10 and 17 as well.

And like claim 1, claims 10 and 17 also require a lateral transistor. *See* Limitations [10d] and [17e]. Petitioner's analysis of those limitations in Grounds 1A, 1B, 1C, and 1D merely cross-reference the Petition's analysis for claim 1. *Id.*, 40 (Limitation [10d] in Ground 1B), 51 (Limitation [17e] in Ground 1B), 63 (Limitation [17e] in Grounds 1C and 1D). Because Petitioner did not meet its burden to establish the Nega-Roberts Combination discloses a lateral transistor in its claim 1 analysis (*see supra* §IV.C), it failed to meet its burden to establish the same for claims 10 and 17 as well.

And the challenges to the dependent claims in all of Grounds 1A-1F inherit the failings for their independent claims so the above failings in Ground 1A for claim 1 are fatal to all the Nega-based Grounds 1A-1F for every Challenged Claim.

V. THE LIU GROUNDS FAIL TO DEMONSTRATE A REASONABLE LIKELIHOOD OF PROVING ANY CLAIM UNPATENTABLE

The Liu Grounds (Grounds 2A-F) fail to demonstrate a reasonable likelihood of proving any Challenged Claim unpatentable for multiple independent reasons detailed below.

A. Reason #1: Petitioner Failed to Prove that Liu Qualifies as Prior Art Because Petitioner Failed to Show that Liu's Cited Disclosures Are in Liu's Provisional Application

Liu (Ex. 1010) is a patent that issued from a divisional of Application No. 15/202,917 that was filed on July 6, 2016—after the '481 Patent was filed on January 18, 2016. The Petition notes that Liu claims priority to U.S. Provisional Application No. 62/196,629 ("Provisional") filed July 24, 2015, and Petitioner relies on the filing date of the Provisional to purportedly establish that Liu is prior art. Petition, 71.

Petitioner admits that for Liu to be prior art to the '481 Patent, the Provisional must have provided a written description of "the subject matter of Liu Petitioner relies on." Petition, 71 (citing *Penumbra, Inc. v. RapidPulse, Inc.*, IPR2021-01466, Paper 34, 29-35 (Mar. 10, 2023) (precedential)); *see also* Petition, 72 (alleging that "all Liu's cited disclosures are ***identical or nearly identical*** to its Provisional"). Petitioner bears the burden of production and the burden of persuasion to demonstrate that all the Liu disclosure it relied upon is in Liu's Provisional. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378-80 (Fed. Cir. 2015) ("The burden of production was on [petitioner] to prove that, under § 119(e)(1), [the prior art patent] was entitled to the benefit of the filing date of its provisional application, and it failed to do that."). Petitioner failed to carry that burden.

As demonstrated below, Petitioner failed to establish that the portions of Liu that Petitioner cites had written description support in Liu's Provisional. Given that, Petitioner failed to show that Liu is accorded the earlier filing date of the Provisional under 35 U.S.C. § 102(d)(2) and thus failed to show that Liu is prior art to the '481 Patent.

1. The Cited Portions of Liu Disclose a Different Device than the Provisional

Petitioner cites Liu, 8:11-26 several times to purportedly establish the Liu discloses the following limitations:

Limitation **[1a]** (Petition, 83-84, citing Liu, 8:16-25);

Limitation **[1b]** (Petition, 85-86, citing Liu, 8:11-16); and

Limitations **[1c]**, **[1d]** and **[1e]** (Petition, 87, citing Liu, 8:16-25).

Petitioner alleges that the disclosure in 8:11-26 is found in the Provisional at [00042]. Petitioner's "analysis" is that "all Liu's cited disclosures are ***identical or nearly identical*** to its Provisional." Petition, 72. Petitioner purports to support its assertion of "identical or nearly identical" disclosure by using a table that places disclosure in Liu and the Provisional side-by-side. Petition, 72-73. The table below reproduces some of the disclosure in Liu and the Provisional that the Petition presents side-by-side. As the Board can see, this demonstrates that Liu and the Provisional describe ***different*** devices.

Relied-Upon Liu Subject Matter (Liu, 8:11-26)	Alleged Provisional Support [00042]
A semiconductor chip 40B is bonded to surface 138A of device receiving area 138 using a die attach material 421, wherein **die attach material 421 is an electrically insulating die attach material**. Thus, surface 44 is bonded to surface 138A of device receiving area 138 **through an electrically insulating die attach material 421**….	A semiconductor chip 40B is bonded to surface 138A of device receiving area 138 using a die attach material 42, wherein **die attach material 42 is an electrically and thermally conductive die attach material**. Thus, surface 44 is bonded to surface 138A of device receiving area 138 **through an electrically and thermally conductive die attach material 42**….

Petitioner relies on Liu's disclosure of a semiconductor chip 40B bonded to surface 138A of device receiving area 138 using an **electrically insulating** die attach material 421. But the Provisional discloses the opposite, a semiconductor chip 40B bonded to surface 138A of device receiving area 138 using an **electrically** and thermally **conductive** die attach material 42. This difference is ignored by Petitioner and Dr. Lebby.

2. Petitioner Failed to Explain the Facial Difference Between the Cited Portions of Liu and the Corresponding Disclosure in the Provisional

Petitioner never even acknowledges the facial difference between the cited portions of Liu and the Provisional, let alone explain why it is somehow immaterial. Petitioner cites Lebby, [0226]-[0227], but Petitioner never explains the content or significance of those two paragraphs, and those paragraphs from the Lebby declaration cannot be incorporated by reference into the Petition. *Supra*

§IV.B.2 (citing authority). Moreover, that testimony, even if it were considered, merely parrots the Petition's conclusory assertion that the disclosures are "nearly identical" without even acknowledging, let alone analyzing, the differences in the disclosures. *Compare* Petition, 72 *with* Ex. 1003, ¶[0226]. This testimony warrants no weight under the Board's precedential decision in *Xerox*, IPR2022-00624, Paper 9, at 14-16 ("[T]he cited declaration testimony is conclusory and unsupported, adds little to the conclusory assertion for which it is offered to support, and is entitled to little weight.") (citing 37 C.F.R. § 42.65(a) ("Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight")).

Neither Petitioner nor Dr. Lebby even acknowledges that the Provisional describes a different device than Liu and neither explains how or why the device in Liu's Provisional is "nearly identical" to the device in Liu despite having an "electrically conductive" die attachment material rather than an "electrically … insulating" die attachment material. Without such explanation, the Petition is facially deficient and cannot establish that Liu is entitled to the Provisional's earlier filing date. *Penumbra*, IPR2021-01466, Paper 34 at 29-35; *Dynamic Drinkware,* 800 F.3d at 1378. Petitioner thus failed to establish Liu is prior art over the '481 Patent.

B. Reason #2: Petitioner Failed to Establish that Liu Discloses a Lateral Transistor

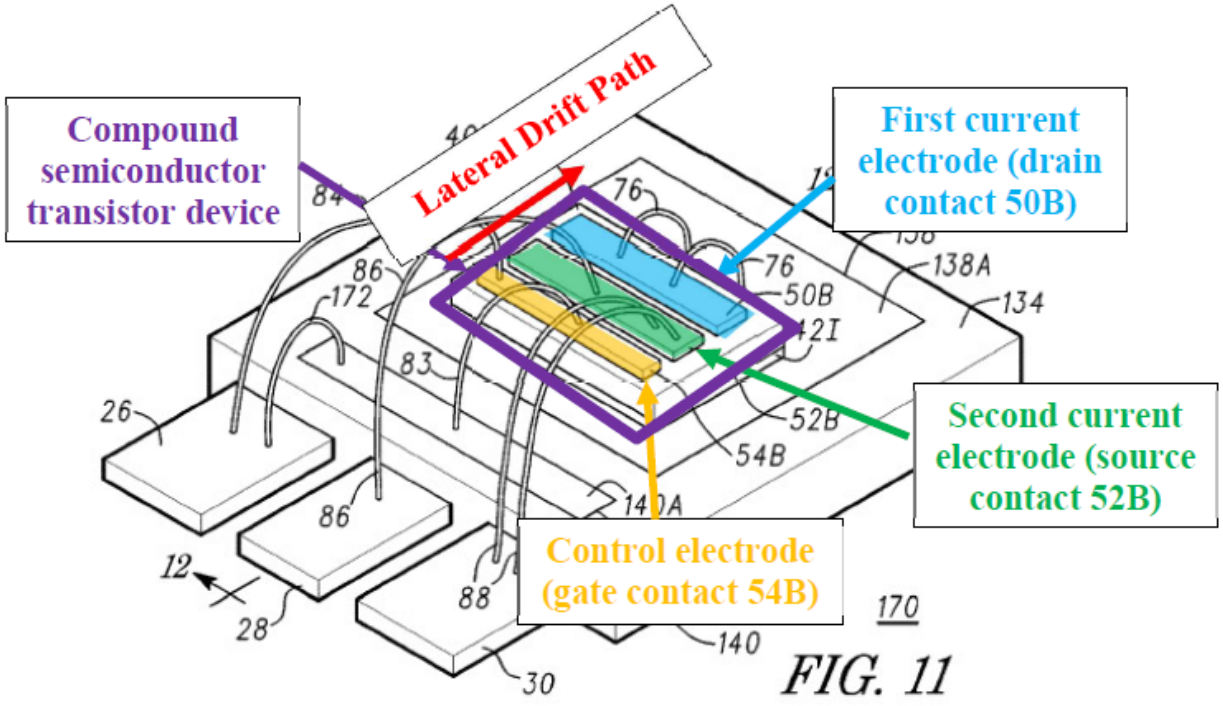
Petitioner failed to establish that Liu discloses a lateral transistor as required by Limitations [1f], [10d], and [17e] and thus by every Challenged Claim. As explained *supra* §II.B, a lateral transistor device is one "in which ***current flows*** … in the **direction parallel to**" the device's surface." Ex. 1002, 33-34 (emphasis original).

Petitioner does not rely on any reference other than Liu and does not allege any modification to Liu to meet the claimed lateral transistor. Instead, Petitioner alleges that Liu discloses a lateral transistor. Petition, 91-93. But Petitioner failed to show that Liu discloses a lateral transistor either expressly or inherently.

1. Petitioner Failed to Establish that Liu Inherently Discloses a Lateral Transistor

Petitioner states "Liu's semiconductor component 170 is arranged laterally" because "Liu's source, drain, and gate are spread laterally across the semiconductor material creating a lateral drift path, as opposed to a vertical configuration." Petition, 91-93 (annotating Figs. 11-12 as shown below). The ***only evidence*** the Petition cites to allegedly support the assertion that Liu's transistor has a lateral drift path is Liu's Figs. 11-12. Petition, 92-93. The transistor in Liu's Figs. 11-12 is a "field effect semiconductor device" that is "include[d]" in the "semiconductor chip 40B." Liu, 8:11-25. As shown in Petitioner's annotated

version of Fig. 11 reproduced below, Petitioner drew a line through semiconductor chip 40B purporting to show a "Lateral Drift Path" for the transistor inside the chip. But the Liu figures that Petitioner relies on do not show anything about the structure of the transistor inside chip 40B. Petitioner's assertion about the direction of the "Drift Path" of the transistor inside the chip is entirely unsupported.



Liu, Fig. 11 (annotated); Provisional, Fig. 11.

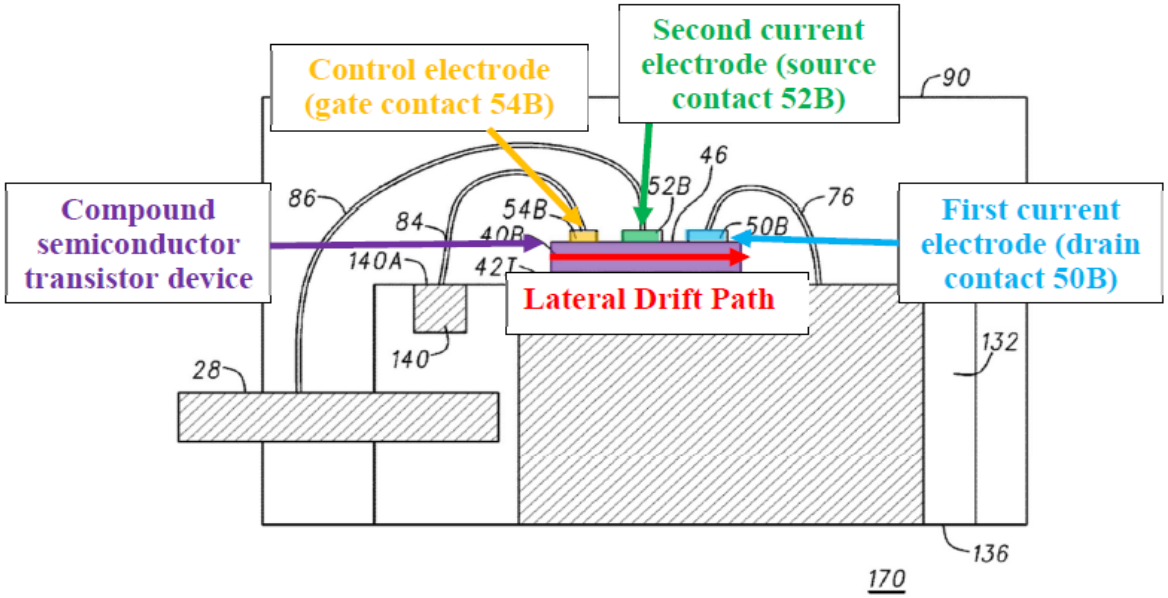


FIG. 12

Liu, Fig. 12 (annotated); Provisional, Fig. 12.

Petitioner's annotations to Figs. 11-12 purport to highlight the direction of the current flow within the transistor relative to the device's surface, but nothing in Liu supports that Fig. 11-12's transistor's drift path is lateral. Petitioner's argument that the transistor in Liu's Figs. 11-12 has a "lateral drift path" is based entirely on the false assumption that because the transistor's ***electrodes*** are arranged laterally, the transistor's "drift path" is lateral so the transistor is a lateral transistor. *Id.*, 91-93. But as explained *supra* §IV.C.2, both lateral and vertical transistors can have their electrodes "arranged laterally" on the top of the substrate.

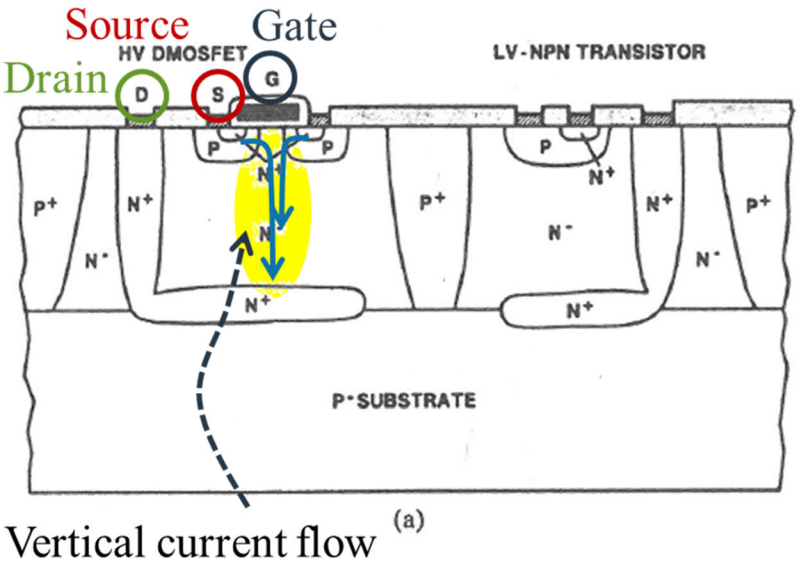
Given that Liu does not expressly disclose that its transistor is a lateral transistor and given that Liu does not expressly disclose the direction of its "drift path," Petitioner could only substantiate its assertion that "Liu discloses" a lateral

transistor (Petition, 91) if Liu inherently disclosed a lateral transistor. *LBT IP I*, 2023 WL 3914920 at *3 (because it was "undisputed that [the reference] does not expressly disclose" a limitation, petitioner's "argument regarding [the reference]'s disclosure is substantively one of inherency"). But Petitioner does not even allege that Liu inherently discloses a lateral transistor, let alone meet its burden to establish inherency.

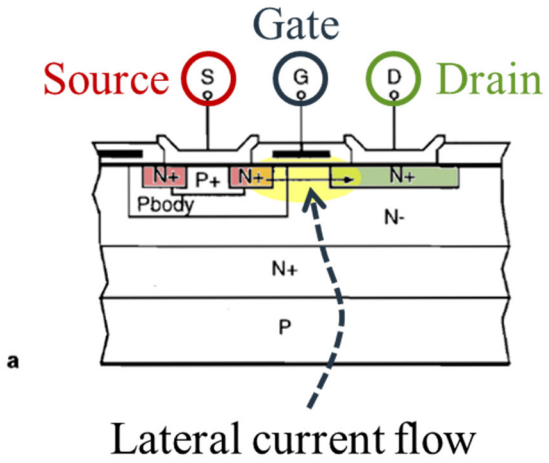
Establishing inherency is a high bar that would require Petitioner to demonstrate that Liu's Figs. 11-12 transistor is "necessarily" a lateral transistor because it cannot be a vertical transistor. *Guangdong Alison Hi-Tech*, 936 F.3d at 1364 ("An element may be inherently disclosed only if it is ***necessarily*** present, not merely probably or possibly present, in the prior art.") (internal quotation marks and citations omitted). Petitioner does not carry that burden. The arrangement of the electrodes laterally on the same side of the substrate in Liu's Figs. 11-12 does not mean that the transistor must necessarily be a lateral transistor because the transistor could be a vertical transistor. *See supra* §IV.C.2.

Petitioner does not even allege, let alone submit evidence to establish, that Liu's transistor could not be a vertical transistor with electrodes on the top as was known in the art. Ex. 2002, 7-8 ("current flow is vertical in the power device structure" in "Fig. 1.7c"), Fig. 1.7c; Ex. 2003, 1937 ("Fig. 3(a) … preserves a vertical high-voltage transistor structure"), Fig. 3(a) (below, annotated).

Prior Art Vertical Transistor with Drain-Source-Gate Electrode Arrangement

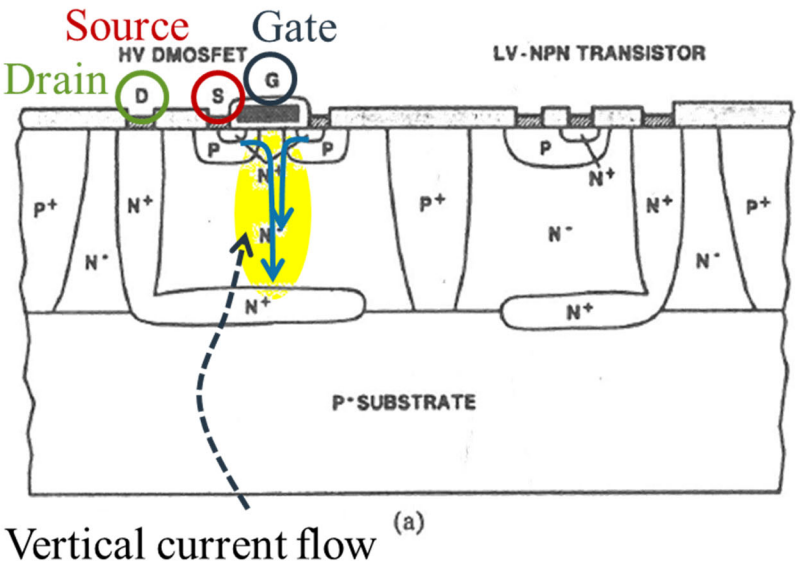


Indeed, it is significant that Liu's electrodes are not arranged with the gate electrode between the source and drain electrodes. In a lateral transistor, a voltage at the gate induces a lateral channel between the source and drain regions as shown below. Petitioner never explains how, according to its theory, Liu could create such a lateral channel between the source and drain regions when its gate electrode is not between the source and drain electrodes.

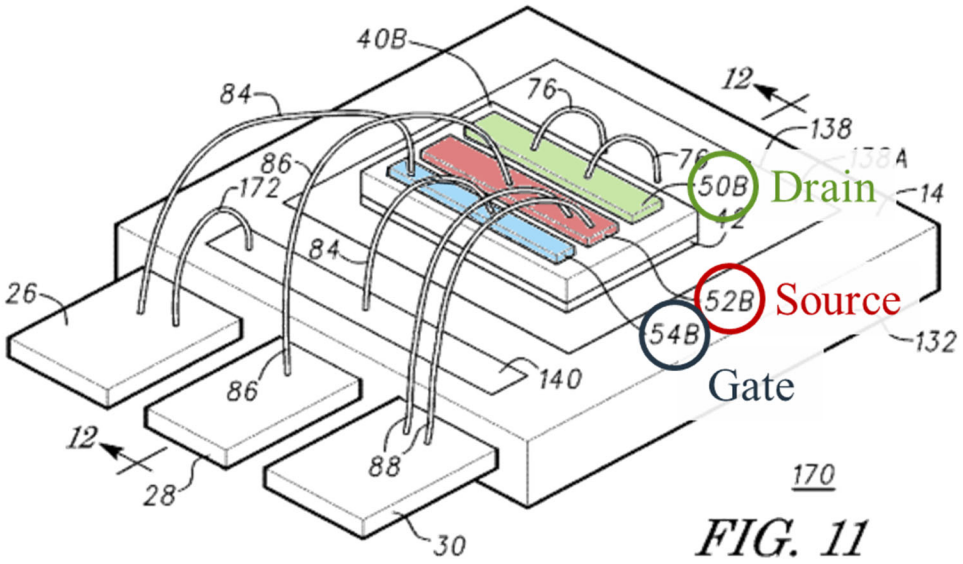


Indeed, Liu's arrangement of electrodes, where the gate electrode is not between the source and drain electrodes, is consistent with the prior art vertical transistor shown below. Ex. 2003, 1937 ("Fig. 3(a) … preserves a vertical high-voltage transistor structure"), Fig. 3(a) (below, annotated).

<u>Prior Art Vertical Transistor with Drain-Source-Gate Electrode Arrangement</u>



Liu's Device with Drain-Source-Gate Electrode Arrangement



As demonstrated above, the arrangement of electrodes on the top surface of Liu's device does not ***necessarily*** mean that the transistor is a lateral transistor device and is entirely consistent with a vertical transistor device. Petitioner failed to establish that Liu inherently discloses a lateral transistor.

2. Petitioner Failed to Establish that Liu Expressly Discloses a Lateral Transistor

To the extent Petitioner is relying on express disclosure in Liu and not inherency, Petitioner equally failed to establish that Liu expressly discloses a lateral transistor. Petitioner cites no portion of Liu that expressly discloses Liu's device as being a lateral transistor, or that expressly discloses the direction of current flow in Liu's transistor. Petition, 91-94. Liu has no such disclosure. *See generally* Ex. 1010. Again, Liu's transistor is in a "chip 40B." Liu, 8:11-25. The

structure of the transistor is not shown anywhere in the Liu figures Petitioner relies upon and Petitioner cites no other disclosure in Liu that would support Petitioner's assertion that the transistor is a lateral transistor.

Petitioner erroneously assumed that Liu's figures showing the electrodes positioned on the same side of the substrate was determinative of the transistor being a lateral transistor – it is not. *See Supra* §IV.C.2 (vertical transistors can have their electrodes arranged this way). Thus, Petitioner failed to establish that Liu expressly discloses a lateral transistor.

3. Petitioner's Expert Does Not Credibly Support Petitioner's Assertion that Liu Discloses a Lateral Transistor

In connection with Limitation 1[f], Petitioner block cites four paragraphs from the Lebby declaration (¶¶[0243]-[0246]). Petition, 93. But the Lebby declaration cannot cure the Petition's shortcomings for two reasons.

First, "[a]rguments and information that are not presented and developed in the Petition, but instead are incorporated by reference, are not entitled to consideration, as it is improper to incorporate by reference arguments from one document into another document." *Instrumentation Lab'y*, IPR2017-00855, Paper 55 at 20; *see also supra* §IV.B.2 (citing other authority). The citation to four paragraphs of the Lebby declaration without any explanation in the Petition is not a sufficient substitute for an explanation of the relevance of the evidence relied upon

and should not be considered. 37 C.F.R. § 42.22 (the "***petition*** … must include … a detailed explanation of the significance of the evidence").

Second, if the Board were to wade into the Lebby declaration, the Board would find that the declaration largely verbatim parrots the Petition's Limitation [1f] analysis without citing any documentary evidence to support the conclusory assertion that Liu discloses a lateral transistor. *Compare* Petition, 91-93 *with* Ex. 1003 ¶¶[0243]-[0246]. This testimony warrants no weight under the Board's precedential *Xerox* decision. *Xerox*, IPR2022-00624, Paper 9 at 14-16 ("[T]he cited declaration testimony is conclusory and unsupported, adds little to the conclusory assertion for which it is offered to support, and is entitled to little weight.") (citing 37 C.F.R. § 42.65(a) ("Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight")). Because Dr. Lebby merely parrots the Petition verbatim, Dr. Lebby's analysis is unsupported and facially deficient for the same reasons Petitioner's argument fails.

4. Conclusion: The Petition Failed to Establish that Liu Discloses a Lateral Transistor as Claimed

Petitioner erroneously assumed that a transistor with laterally-spaced electrodes is necessarily a lateral transistor. That is manifestly wrong. As a result, Petitioner failed to establish that Liu expressly or inherently discloses a lateral transistor. Ground 2A fails for this independent reason.

C. Reason #3: Petitioner Failed to Establish that Liu Discloses a Die Pad as Claimed

The Liu Grounds also fail because Petitioner failed to establish that Liu has a die pad as required by every Challenged Claim (*see* Limitations [1b], [10a], [17a]). As explained below, "die pad" is a term of art that means a portion of a leadframe on which a die is attached. Petitioner admits a "die pad … is part of a lead frame." Petition, 13. But Petitioner never even alleges, let alone establishes, that the Liu embodiment on which Petitioner relies has a leadframe. Petition, 87-91. Petitioner, therefore, failed to establish that Liu's device has a die pad (which is part of a leadframe) as required by every Challenged Claim.

1. Die Pad Is a Portion of a Leadframe

"Die pad" is a term of art that means a portion of a leadframe on which a die is attached. For example, one 1995 textbook defines "DIE PAD" in its glossary as the "***portion of the leadframe on which the IC die is mounted***." Ex. 2004, 452; *see also id*., 117 ("The integrated circuit diced from the wafer is attached to ***the center of the leadframe, called the die-attach pad***…..."). Variations of this definition are used throughout the art. *E.g*. Ex. 2007, ¶[0027] ("the device carrier may comprise multiple metal plates such as, *e.g*., ***die pads*** and/or terminal pads of, *e.g*., ***a leadframe***.").

A leadframe is typically constructed from a metal ribbon from which holes are punched out to form the die pad and various leads. Ex. 2002, 486, Fig. 13.2 (reproduced below).

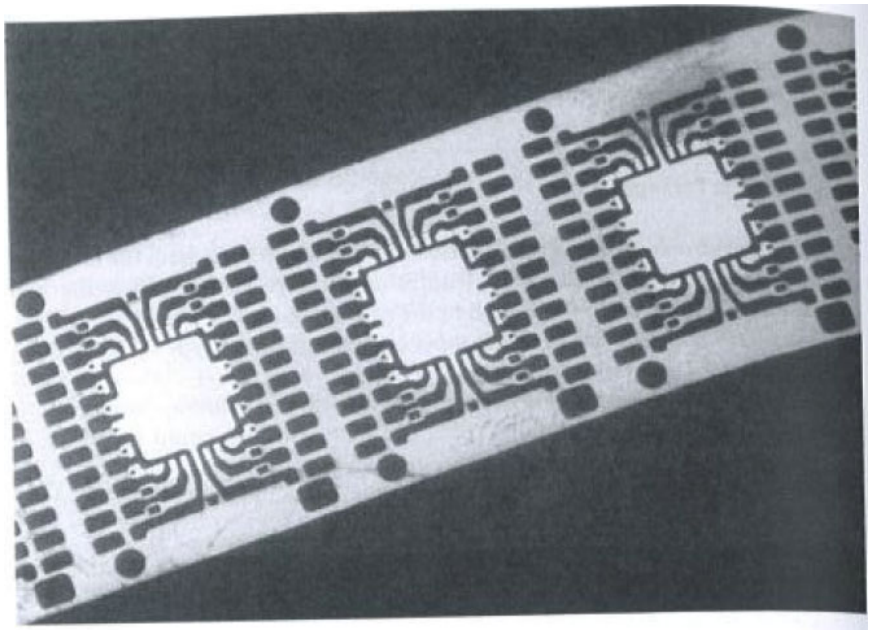


Fig. 13.2 Leadframe of medium power SOP, with heat transfer leads connected to die-pad

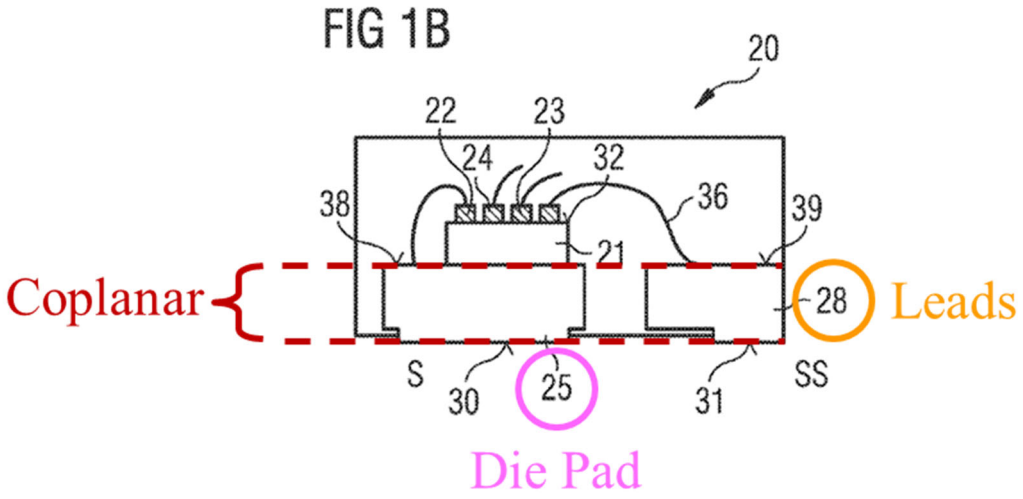
A die pad, thus, typically has the same thickness as the surrounding leads. *Id.*

2. The '481 Patent Uses "Die Pad" Consistently with Its Meaning in the Art

The '481 Patent has no express definition of a "die pad," but uses that term consistently with its meaning in the art as the portion of a leadframe on which a die is attached. For example, the '481 Patent states that, "[t]he leads 90, 91, 95 and ***die pad*** 88 ***form part of a leadframe*** 97 of the electronic component 80." Ex. 1001, 9:20-21, 10:11-16 ("The electronic component 110 includes a compound semiconductor device 111 and a ***leadframe*** 112 ***including a die pad*** 113 and a

plurality of leads 114 arranged on two opposing sides 115, 116 of the die pad 113."), 12:43-45 ("The electronic component 170 includes a ***leadframe*** 174 ***including a die pad*** 175 and a plurality of leads 176 arranged 45 on two opposing sides of the die pad 175."), 13:52-57 (similar).

The '481 Patent consistently describes its leads and die pad as having substantially the same thickness, consistent with how leadframes are typically made from one ribbon of metal. For example, the '481 Patent states that "[a]s can be seen in the cross-sectional view of FIG. lb, die pad 25 has lower surface 30 which is substantially coplanar with the lower surfaces 31 of the leads 26, 27, 28." Ex. 1001, 4:27-29, Fig. 1B (below, annotated). The '481 Patent further states that "[t]he upper surface 38 of the die pad 25 and the upper surfaces 39 of the leads 26, 27, 28 are substantially coplanar." *Id*., 4:33-35, Fig. 1b.



The ’481 Patent discloses that the top and bottom surfaces of the die pad and leads are coplanar because, as explained in Section V.C.1, *supra*, the leadframe (including the die pad and leads) is typically made from a single ribbon of metal. *E.g*. Ex. 1001, 4:35-36 (“The die pad 25, first lead 25, second lead 27 and third lead 39 may include a metal such as copper.”), 9:22-25 (“The leadframe 97 may include a metal such as copper. The leads 90, 91, 95 and die pad 88 may have substantially the same thickness so that the upper surfaces and lower surfaces are substantially coplanar.”), 10:44-48 (similar).

In sum, the ’481 Patent uses the term “die pad” consistent with its meaning in the art as a portion of a leadframe on which a die is attached.

3. Petitioner Failed to Establish that Liu Discloses a Die Pad Under Petitioner’s Own Construction

Petitioner and Petitioner’s expert construed a “die pad” as part of a leadframe. Petition, 13 (“die pad … is part of a lead frame”); Ex. 1003 ¶[098] (“A die pad … is part of a lead frame.”). The Petition “must” demonstrate “[h]ow the ***construed*** claim is unpatentable.” 37 C.F.R. § 42.104(b)(4). To meet this requirement (“must”) the Petition had to show that the device used in each of the Liu Grounds has a die pad that “is part of a lead frame.” But the Petition failed to establish that Liu’s “device receiving area 138”—which the Petition argued is a die pad (Petition, 85-87)—is part of a leadframe as would be required to meet the “construed claim” for two reasons.

First, Petitioner cites Liu as disclosing that the ***leads*** are part of a leadframe, but nowhere cites any part of Liu that says the ***device receiving area 138***, which Petitioner alleges is a die pad, is part of the leadframe. Petition, 85-87. With respect to the embodiment of Liu on which Petitioner relies (Figs. 11-12), Liu teaches that "leads 26, 28, and 30" are "leadframe leads" (Ex. 1010, 8:8), but never teaches that "device receiving area 138" is part of the leadframe.

Second, Liu's depiction of device receiving area 138 is inconsistent with it being part of the leadframe. For example, the top and bottom surfaces of the leads, which Liu discloses are part of a "leadframe" (*e.g.*, Liu, 8:27-40), are not coplanar with the top and bottom surfaces of device receiving area 138. Liu, Fig. 12 (annotated below). Indeed, device receiving area 138 is shown as being far thicker than the leads (*e.g.*, lead 28). Liu never says that device receiving area 138 is stamped out of the same piece of metal as the leads (*e.g.*, lead 28). Nothing in Liu suggests that device receiving area 138 is part of the leadframe.

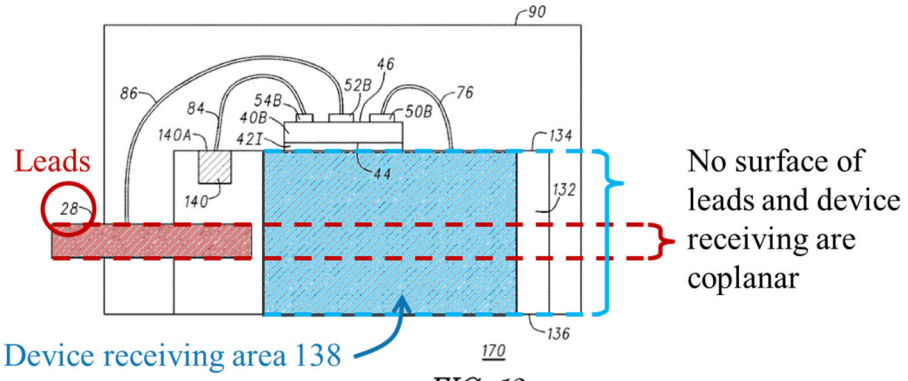


FIG. 12

While patent figures are not necessarily drawn to scale, Liu provides disclosure that makes clear that when Liu discloses components that are coplanar Liu describes them as such and shows this relationship in the figures. For the different embodiment in Figs. 1-2, bond pads 22 ***are*** described and shown in the figures are being coplanar with device receiving area 18 at their top surfaces. *Id*., 3:9-12. Similarly, for the embodiment in Figs. 6-7, bond pads 140 are described and shown in the figures as being coplanar with device receiving area 138 at their top surfaces. *Id*., 5:45-46. That Liu depicts these components in the figures as being coplanar (see below) supports that Liu not describing the device receiving area 138 as being coplanar with the leads (*e.g*., lead 28) in Figs. 11-12 supports that they are not in fact coplanar.

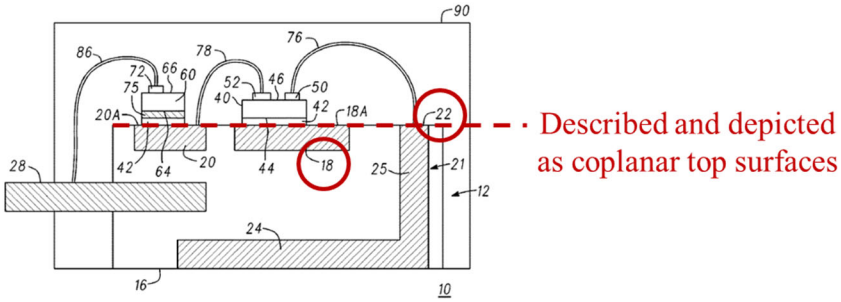


FIG. 2

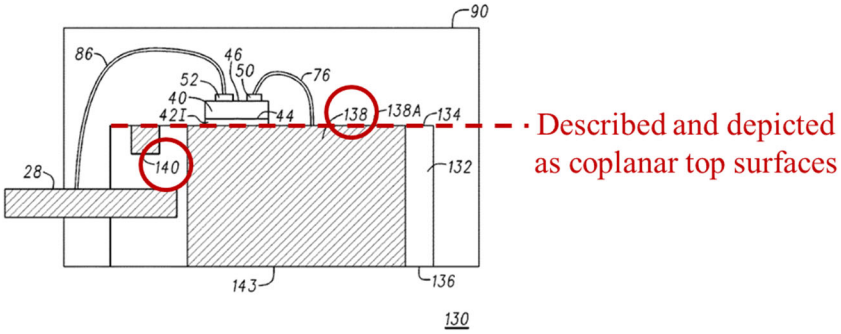


FIG. 7

Again, for the embodiment in Figs. 11-12 that Petitioner relies on, Liu never discloses that any surface of the leads and the device receiving area are coplanar and depicts them as not being coplanar as shown below. Liu also discloses the device receiving area 138 as being far thicker than the lead 28, indicating that they were not stamped out of the same piece of metal the way a leadframe is. Ex. 2002, 486, Fig. 13.2.

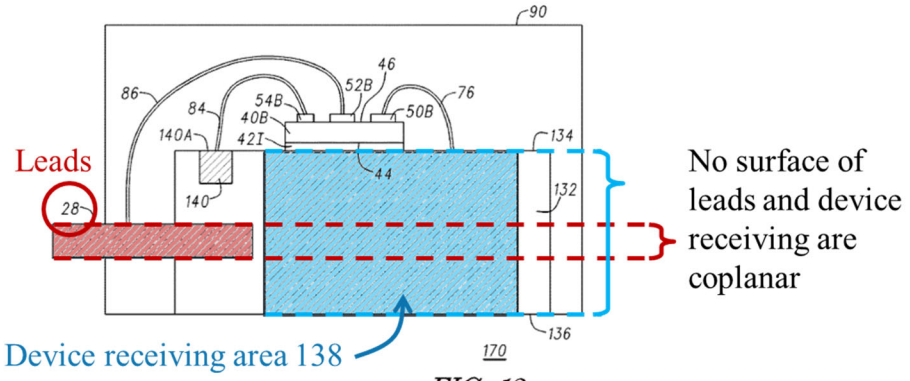


FIG. 12

It is not Patent Owner's burden to show that Liu's device receiving area 138 is not part of Liu's leadframe. It was Petitioner's burden to prove that device receiving area is part of Liu's leadframe. Yet, Petitioner cites no evidence establishing that Liu's device receiving area 138 is part of a leadframe, as would be required for it to be a die pad under the ***Petition's own construction***.

4. Petitioner Proposed No Alternate Construction of "Die Pad" that Would Encompass Liu's Device Receiving Area

To the extent the Petition can be read as implicitly suggesting that a "die pad" need not be "part of a lead frame" that would fail for at least two reasons.

First, the Petition was required ("must") to identify "[h]ow the challenged claim is to be construed" as well as "[h]ow the construed claim is unpatentable." 37 C.F.R. § 42.104(b)(3)-(4). Petitioner never identifies any construction of the term "die pad" other than that it "is part of a lead frame." Petition, 13.

Second, to the extent the Petition is read as implicitly suggesting that Liu's device receiving area falls within the scope of the claimed die pad for some

unstated reason, Petitioner cannot meet its burden by implication. *Garmin v. LoganTree*, 825 F. App'x 894, 898-99 (Fed. Cir. 2020) (affirming the Board's finding that a petition failed because it failed to explain how a claim limitation was met – "a petitioner in an inter partes review has the burden of demonstrating unpatentability by a preponderance of the evidence; bare assertion through implication that a reference discloses a claim limitation, without more, is not enough to meet this burden").

Because Petitioner construed "die pad" to be "part of a lead frame" and offered no contrary construction, Petitioner must demonstrate how that "construed claim" is unpatentable. 37 C.F.R. § 42.104(b)(3)-(4). Because Petitioner failed to establish that Liu's device receiving area 138 is part of a leadframe, Petitioner failed to establish that Liu's device receiving area 138 is a die pad under Petitioner's own construction.

D. Petitioner's Showing for the Remaining Claims in Ground 2A and the Other Liu Grounds Inherit Petitioner's Flawed Analysis of Claim 1 in Ground 2A

The Liu Grounds do not challenge independent claim 10 so the only other challenged independent claim is claim 17 in Grounds 2B and 2F.

Like claim 1, claim 17 also requires a lateral transistor. *See* Limitation [17e]. Petitioner's analysis of a lateral transistor for claim 17 in Grounds 2B and 2F merely cross-references the Petition's analysis for claim 1. Petition, 101

(Ground 2B), 111 (Ground 2F). Because Petitioner did not meet its burden to establish Liu discloses a lateral transistor in its claim 1 analysis (*see supra* §V.B), it failed to meet its burden to establish Liu discloses a lateral transistor for claim 17 as well.

And like claim 1, claim 17 also requires a die pad. *See* Limitation [17a]. Petitioner's analysis of a die pad for claim 17 in Grounds 2B and 2F merely cross-reference Petitioner's analysis for claim 1. I*d*., 100 (Ground 2B), 109 (Ground 2F). Because Petitioner did not meet its burden to establish Liu discloses a die pad in its claim 1 analysis (*see supra* §V.C), it failed to meet its burden to establish Liu discloses a die pad for claim 17 as well.

And the challenges to the dependent claims in all of Grounds 2A-2F inherit the failings for their independent claims so the above failing in Ground 2A for claim 1 is fatal to all the Liu-based Grounds 2A-2F for every Challenged Claim.

VI. CONCLUSION

Institution should be denied because the Petition failed to establish a reasonable likelihood that any Challenged Claim is unpatentable.

Respectfully submitted,
Infineon Technologies Austria AG

Date: September 20, 2024

/Richard Giunta/

Richard F. Giunta, Reg. No. 36,149
WOLF, GREENFIELD & SACKS, P.C.

CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24, the undersigned certifies that the foregoing **PATENT OWNER'S PRELIMINARY RESPONSE** contains 13,693 words excluding; a table of contents, a table of authorities, a certificate of service or word count, or appendix of exhibits or claim listing. Patent Owner has relied on the word count feature of the word processing system used to create this paper in making this certification.

Date: September 20, 2024

/Dara Del Rosario/
Dara Del Rosario
Paralegal
WOLF, GREENFIELD & SACKS, P.C.

CERTIFICATE OF SERVICE UNDER 37 C.F.R. § 42.6 (e)(4)

I certify that on September 20, 2024, I will cause a copy of the foregoing document, including any exhibits filed therewith, to be served via electronic mail, as previously consented to by Petitioner, upon the following:

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