

Recent Progress of E-mode Gallium Nitride Metal–Insulator–Semiconductor -High Electron Mobility Transistors with Hybrid Ferroelectric Charge Trap Gate (FEG-HEMT) for Power Switching Applications

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Aluminum gallium nitride/gallium nitride (AlGa_N/Ga_N) heterostructure devices have proven to be highly effective for high-frequency power amplifiers and power switching applications with improved performance compared to those made with traditional silicon technology and other advanced semiconductor technologies. The development of enhancement-mode (E-mode) AlGa_N/Ga_N high electron mobility transistors (HEMTs) and metal–insulator–semiconductor HEMTs (MIS-HEMTs) has been a focus in recent years due to their potential applications. Arising from the concept of a flash-memory-like hybrid ferroelectric charge storage structure, the high-performance hybrid ferroelectric charge storage gate (FEG) Ga_N HEMT has gradually gained a great deal of attention due to the concept being a useful and versatile tool to realize E-mode operations. This article attempts to review the latest progresses in this technology, including alternative improvements and device characteristics. Future challenges for the E-mode FEG-HEMT are also discussed.

1. Introduction

As energy consumption throughout the world increases and the need for green energy grows, energy efficiency is a top priority for the progress of next-generation power-switching devices applications.^[1–3] With the continuous demand for high-power density, small size, and low-cost devices for future power electronics applications, conventional Si-based devices are reaching their physical limits. Much effort has been devoted to implementing renewable resources for electrical power conversion systems with high efficiencies. The renovation of traditional power

systems by using wide bandgap semiconductors has become a challenging and popular topic.^[4,5]

Gallium nitride (Ga_N) and related wide bandgap semiconducting alloys have been regarded as leading candidate materials for the next generation of high-power and high-frequency electronic devices.^[6,7] Wide bandgap Ga_N-based materials are, especially with heterostructures such as AlGa_N/Ga_N, attractive for high-frequency power amplifiers and power switches applications, owing to their superior material properties. Ga_N HEMT or Ga_N high electron mobility transistor offers tremendous potential for power switching and high frequency (RF) applications. Compared with Si counterparts, the higher breakdown field and higher drift velocity of the Ga_N-based devices produce lower losses

at high voltage and high-temperature operations.^[8,9] Due to the spontaneous polarization and piezoelectric polarization, the 2DEG forms at the heterointerface creating a high sheet carrier density at the AlGa_N/Ga_N hetero-interface. The high carrier concentration together with high electron mobility, caused by the material's unique polarization-induced electric field, contribute to very low resistances and high output power for the power devices; however, the conventional epi structure and device architecture are usually depletion mode devices, to achieve enhancement-mode (E-mode) operation which is strongly desired for safe operations of power switching systems. For power electronic applications (E-mode), devices play a crucial role in the view of simplifying the circuit design, lower standby power dissipation, and fail-safe considerations.

In the past, various approaches have been proposed for the realization of normally-OFF Ga_N HEMTs. These include the use of recessed gates,^[10,11] p-type Ga_N,^[12,13] fluorine implantation,^[14,15] and oxide charge engineering.^[16] While p-type E-mode Ga_N devices have been successfully commercialized, they require additional protection circuit design due to their low threshold voltage and low gate breakdown. Even though fluorine implantation and oxide charge engineering demonstrate a higher V_{th} , these approaches still lack enough thermal stability and also need PBTI results to verify the V_{th} stability. Among

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the E-mode GaN fabrication techniques, the gate-recessed structure is widely used due to its simple fabrication process.^[17] Combining the recess-gate technique with high-quality gate dielectric has been demonstrated to have outstanding device performance with high V_{th} and good V_{th} stability, but the current density and the ON-resistance are still poorer than the state-of-art normally-ON device.^[18] To avoid process variation and severe degradation of electron mobility, the etching process for fabricating the gate-recessed structure needs to be cautiously controlled. Furthermore, in general, the threshold voltage for the power device should be around $\approx +3$ V to avoid fault turn-on. Thus, a novel normally-OFF GaN technology is still needed for GaN power device applications.

Over the years, simulation studies and experimental results demonstrated that the charge trapping/storage stacked structure was a compelling candidate for achieving E-mode operation of AlGaN/GaN metal-insulator-semiconductor (MIS)-HEMTs. GaN metal-insulator-semiconductor MIS-HEMT using charge storage structure can shift the V_{th} of the device to achieve normally-OFF operation without current degradation. Hasegawa et al.^[19] have demonstrated through simulation that by using a floating gate or an oxide layer to compensate for the two-dimensional electron gas (2DEG) in a GaN HEMT structure, the normally-OFF operation can be achieved for the device. This concept has been experimentally demonstrated by Lee et al.^[20] using a charge storage structure with a TaN floating gate and a HfO_2 charge storage layer. Recently, the NYCU group in Taiwan has shown that implementing an additional ferroelectric layer (such as $Hf_xZr_{1-x}O_2$) on top of the charge storage layer demonstrates exceptional electrical characteristics and shows great potential for future power switching applications. Doped-hafnium-oxide-based ferroelectric thin films have already proved themselves as promising materials for ferroelectric memory technologies.^[21–23] These materials provide superior properties over traditional ferroelectrics with the perovskite structure such as scalability, the possibility to grow these materials by atomic layer deposition (ALD), and full CMOS process compatibility.

With the benefit of the lower crystallization temperature of HZO and the feasibility of ALD deposition, the ferroelectric-charge-trapping gate stack has attracted a great deal of attention due to the concept of realizing E-mode operation for GaN-based HEMTs. Wu et al.^[24,25] realized a high V_{th} normally-OFF GaN

HEMT with high drain current density by the implementation of a hybrid ferroelectric charge trap gate stack (FEG-HEMT), with a laminated $Hf_{0.5}Zr_{0.5}O_2$ ferroelectric layer stacked on top of a charge trapping layer (CTL). The FEG-HEMT exhibits a higher positive V_{th} shift after charge injection, higher V_{th} stability, and reliable gate oxide with higher breakdown. Furthermore, Feng et al.^[26] also demonstrated an E-mode with β - Ga_2O_3 power MOSFET with the ferroelectric charge storage gate stack structure with excellent electrical characteristics, showing the versatility of the ferroelectric charge trap gate stack.

Owing to the ferroelectric charge trap gate being a novel concept, more intensive research and development may be needed. This paper aims at giving the readers a wider comprehensive understanding of the performances and operations of the GaN FEG-HEMT. In Section 2, we review the fabrication process and electrical performances of the GaN FEG-HEMT. The benefits of a HZO ferroelectric layer will also be discussed. In Section 3 and 4, we present technologies for improving the ferroelectric charge trap gate stack behavior, including stability of the charge trapping and enhanced ferroelectric behavior. In Section 5, we present a source-connected field plate (SCFP) structure for the FEG-HEMT to redistribute and hence to reduce the high electric field under a high drain bias.

2. The E-mode GaN MIS-HEMTs using Hybrid Ferroelectric Charge Trap Gate Stack (FEG-HEMT) Technology

2.1. Fabrication of the E-mode GaN FEG-HEMT

Figure 1a,b shows the fabrication process flow and the typical structure of our device, respectively. The device fabrication starts with ohmic contact formation. In situ nitrogen plasma treatment was employed before the deposition of a SiNx passivation layer using PECVD.^[27] After passivation, the gate was fabricated. A nitride etching and gate recess procedure were performed using a low-power ICP system. The sample was then loaded into the ALD machine promptly. The gate stack growth by ALD consisted of a ferroelectric laminated structure (28 nm Al_2O_3 – $Hf_{0.5}Zr_{0.5}O_2$ – Al_2O_3)/CTL (6 nm)/tunneling oxide layer (10 nm Al_2O_3). The $HfZrO_4$ mixed oxide was deposited with a cycle ratio of Hf: Zr = 1:1. The ferroelectric laminated

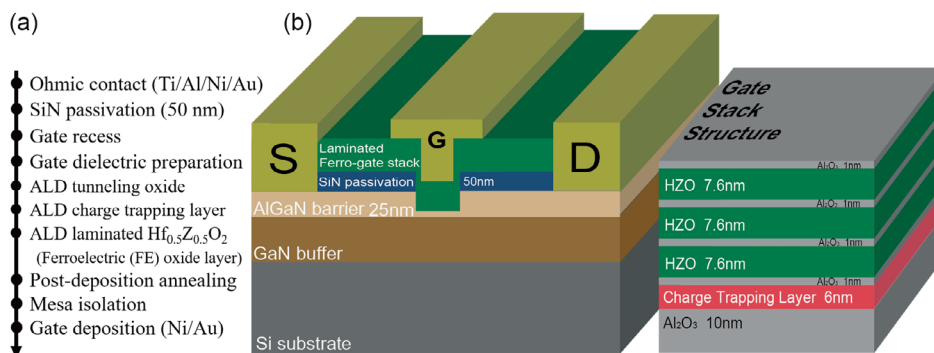


Figure 1. a) Process flow and b) typical structure of the E-mode GaN FEG-HEMT. Reproduced under terms of the CC-BY license.^[32] Copyright 2022, The Authors. Published by IEEE.

structure $\text{Al}_2\text{O}_3\text{-Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2\text{-Al}_2\text{O}_3$ was designed to help prevent non-FE phase formation and to reduce the leakage current.^[25] Post-deposition annealing of the gate stack was then performed at 400 °C. After the gate stack deposition, ion implantation was used for mesa isolation. Finally, the gate metal was then deposited by electron beam evaporation.

2.2. E-mode FEG-HEMT Operations

Before conducting E-mode operations, the FEG-HEMT device requires an initialization to shift the V_{th} of the device to a more positive value. **Figure 2** illustrates the mechanism behind the formation of a high V_{th} for the FEG-HEMTs. After the device fabrication, a high voltage bias was applied to the gate electrode as the initialization process. The gate voltage used for the initialization process was determined by the safety margin based on the gate leakage current characteristics of the device at different temperature regimes. During the initialization process, two events would occur, that is, 1) a strong polarization in the ferroelectric stack; and 2) 2DEG electrons tunneling into the CTL and captured. The initialization process with 1 ms is enough to cause a strong polarization in the $\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$ film; however, different initialization time durations should be considered depending on the applications. After the initialization process, the large electron concentration in the CTL with a combination of the remnant polarization in the ferroelectric layer makes the V_{th} of the device higher and more stable. Normally, GaN-HEMTs with a partial recess gate (still maintains a thin barrier layer) could preserve high channel mobility, but on the other hand, the threshold voltage is not positive enough to achieve practical E-mode operation. With the help of the ferroelectric charge trap gate stack, the V_{th} of the partial gate recess could be enhanced. Furthermore, since the polarization of the AlGaIn/GaN heterostructure is not affected by the initialization charging process, the device shows both a high threshold voltage and a high current density at the same time.

2.3. E-mode FEG-HEMT Performances

In ref. [25], the FEG-HEMT device performances were compared to the device without the laminated ferroelectric layer, namely the non-FE device as shown in Figure 2. The device only differs from the gate stack, and the gate stack of a non-FE device consisted of a

tunnel oxide layer/charge-trapping layer/HfO₂ laminated structure. First, to ensure that the device is in E-mode operation, the initialization process was conducted before subsequent electrical measurements. Devices showed a V_{th} of +0.42 and +2.71 V after initialization for the non-FE device and the FE device, respectively. It was suggested that the FE device possesses a higher density of trapped electron concentration and low density of unfilled trapped states in the HfON charge-trapping layer than the non-FE device, as explained later. The FE device exhibited small V_{th} hysteresis (0.14 V) during the up-and-down sweeping. On the contrary, the non-FE device showed a large V_{th} hysteresis (0.29 V). There are two possible reasons for these results. One is that the non-FE device with poor polarization possesses a high density of unfilled shallow trapping states. Assuming that the number of trapping states is fixed and the number is the same for both gate stacks, the FE device with strong FE polarization can greatly reduce the number of unfilled trapped states in the HfON CTL compared to the non-FE device with poor polarization. The other one is that a severe electron trapping behavior was observed in the non-FE device during the up-and-down sweeping process. After the initialization process, the non-FE device possessed more unfilled trapped states than the FE device and the charge trapping still existed during the forward and reverse V_{GS} sweepings.

Furthermore, Wu et al.^[25] also demonstrated the gate leakage characteristics of the FE devices. The FE devices exhibited an increment in their drain current-gate voltage ($I_{\text{GS}}\text{-}V_{\text{GS}}$) characteristics between 11 and 14 V, which was attributed to the resistive switch effect in the ferroelectric hafnium zirconium oxide ($\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$) film. The non-FE devices had low gate leakage current and no F-N tunneling behavior, which was attributed to strong electron trapping in the gate stack of the non-FE devices. The FE devices also showed better positive bias temperature instability (PBTI) performance than the non-FE devices, with lower threshold voltage shifts at both 25 and 125 °C. This was attributed to the internal electric field caused by the ferroelectric polarization, resulting in the slower electron trapping rate in the $\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$ film. In addition, it was also suggested that the number of unfilled trapping states was much less in the FE device after the initialization process, causing less V_{th} instability when exceeding a longer stress time. The FE devices also had higher maximum drain current ($I_{\text{DS, MAX}}$) and lower on-resistance (R_{ON}) than those of the non-FE devices.

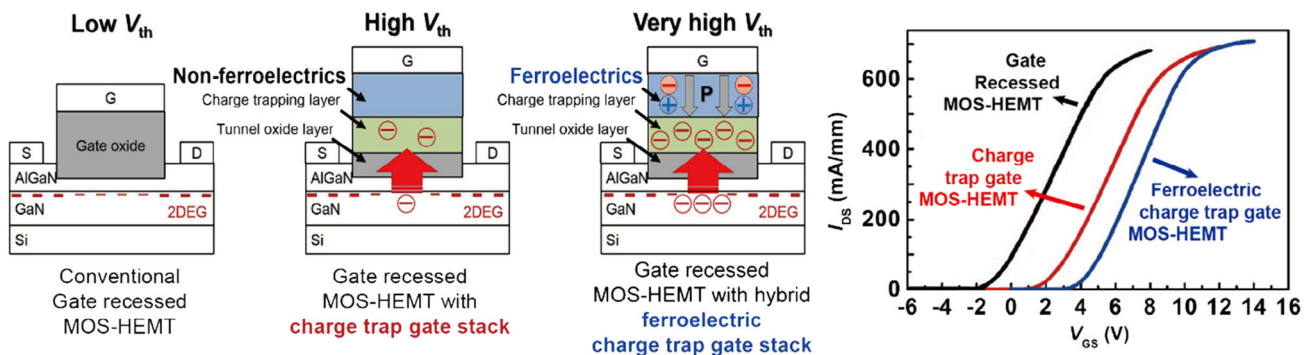


Figure 2. The main concept of the E-mode hybrid ferroelectric charge storage gate (FEG) GaN HEMT for obtaining a high V_{th} , low R_{ON} , and high output current. In addition, a transfer characteristics comparison is illustrated to demonstrate the V_{th} difference of the fabricated device.

The fabricated FEG-HEMT demonstrated an $I_{DS, MAX}$ of 820 mA mm^{-1} at a gate voltage (V_{GS}) of 14 V and an R_{ON} of $11.1 \Omega \text{ mm}$. The FE devices also exhibited a high breakdown voltage of 820 V with a drain current of $10 \mu\text{A mm}^{-1}$ at $V_{GS} = 0 \text{ V}$ (E-mode operation). In addition, large gate-width FEG-HEMTs with currents exceeding 40 A have also been demonstrated, showing the potential of these devices for high-power applications. Overall, these results demonstrate that the incorporation of a ferroelectric layer in the gate stack of GaN HEMTs can improve the electrical performance and suitability for these devices to be used in high-efficiency power switching applications.

3. Charge Trapping Layer Engineering

The trapping and retention abilities of the CTL affect strongly on the V_{th} behaviors of the E-mode FEG-HEMT devices. Hf-based and Zr-based oxides have been chosen to replace conventional Si_3N_4 as the CTL, mainly due to their better scalability, large numbers of trapping sites, larger conduction band offset, and relatively higher dielectric constant. Recently, nitrogen incorporation in high-k thin films has been intensively studied and has shown promising properties to further increase and stabilize the threshold voltage of E-mode FEG-HEMTs.^[28–30]

3.1. Nitrogen Incorporation in HfO_2 and ZrO_2

An important characteristic of the CTL is its capability to confine the electrons, which would directly lead to higher threshold voltages after initialization. It has been reported that the larger ΔE_C (conduction band offset) of oxynitrides from the Al_2O_3 layer directly contributes to the enhancement of the direct tunneling during the initialization due to the reduced barrier height induced by nitrogen incorporation (Figure 3). The largest ΔE_C of the HfON from the Al_2O_3 with the deeper energy state of the charge trapping center for the HfON would result in the largest V_{th} shift and the best electron confinement, which is a key factor for E-mode performance and V_{th} stability.^[31]

To prove the concept mentioned earlier, six FEG-HEMT samples were fabricated with different CTLs for comparison, namely (a) ZrO , (b) ZrN , (c) ZrON , (d) HfO , (e) HfN , and (f) HfON . In ref. [32], Wu et al. first investigated the effect of various CTL materials on the threshold voltage shifts of the E-mode FEG-HEMTs after the initialization process. The authors also characterized the gate leakage and performance under positive and negative bias threshold voltage instability (PBTI and NBTI) conditions.

The results showed that the CTLs with oxynitrides (HfON and ZrON) had higher threshold voltage shifts than those of the CTL with oxides (HfO_2 and ZrO_2). The largest threshold voltage shift was observed in the device with HfON suggesting the highest charge trapping capability of the HfON CTL, as well as the partial crystallization of HfO_2 due to nitrogen incorporation.^[29] However, nitride CTLs, HfN and ZrN, showed the lowest threshold voltage shifts and even resulted in D-mode operations after initialization. The authors speculate that this may be because transition metal nitrides are metallic and are usually used as electrodes rather than for charge storage.

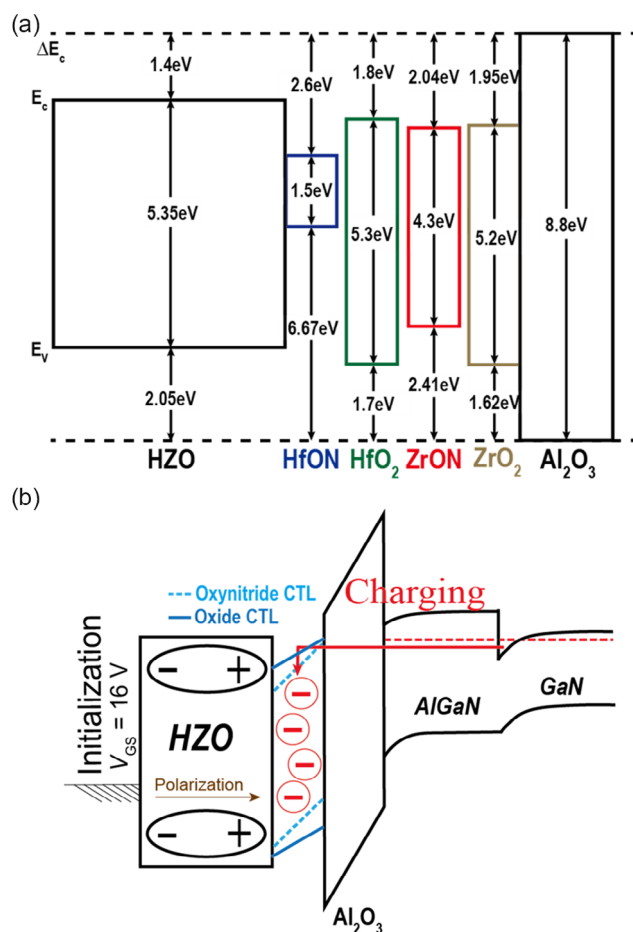


Figure 3. a) The band alignment of the Hf-based and Zr-based oxide and oxynitride charge trapping layers with respect to Al_2O_3 and b) schematic band diagram of polarizing the ferroelectric gate stack during initialization, illustrating a charge storage process of a FEG-HEMT with oxide or oxynitride CTL. Reproduced under terms of the CC-BY license.^[32] Copyright 2022, The Authors. Published by IEEE.

In terms of gate leakage, the devices with HfON and ZrON CTLs showed the lowest leakage current after initialization (Figure 4). To point out, the reason why the HfON sample showed the most reduced gate leakage current may be due to the elimination of V_O -related gap states. Nitrogen incorporation has been found to effectively deactivate these gap states by changing the charge states of V_O from neutral (V_O^0) to positive (V_O^{2+}), which has been demonstrated in previous studies.^[33] It is worth noting that the presence of V_O -related gap states in dielectric materials could have a negative impact on the device performance, as they could lead to increased leakage current. By deactivating these gap states through nitrogen incorporation, the HfON sample may have achieved improved performance and reduced leakage current. The low leakage current of the HfON CTL suppresses the incomplete charging at the initialization process, as shown in Figure 5. The more complete charging of the HfON CTL sample also demonstrated smaller V_{th} hysteresis than the ZrON CTL sample (Figure 6), which this phenomenon was also mentioned in Section 2.3. The low leakage current

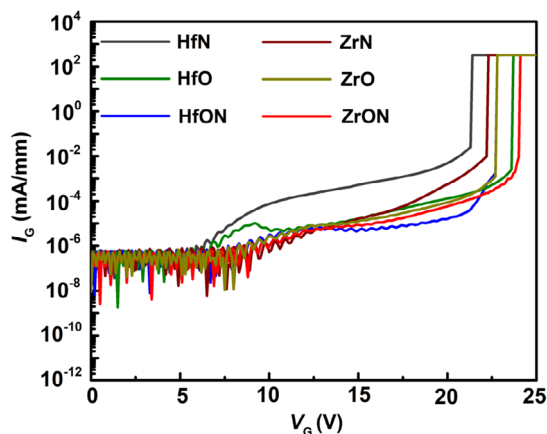


Figure 4. Gate leakage and gate breakdown I_G - V_G characteristics of FEG-HEMTs with Hf-based and Zr-based charge trapping layers. Reproduced under terms of the CC-BY license.^[32] Copyright 2022, The Authors. Published by IEEE.

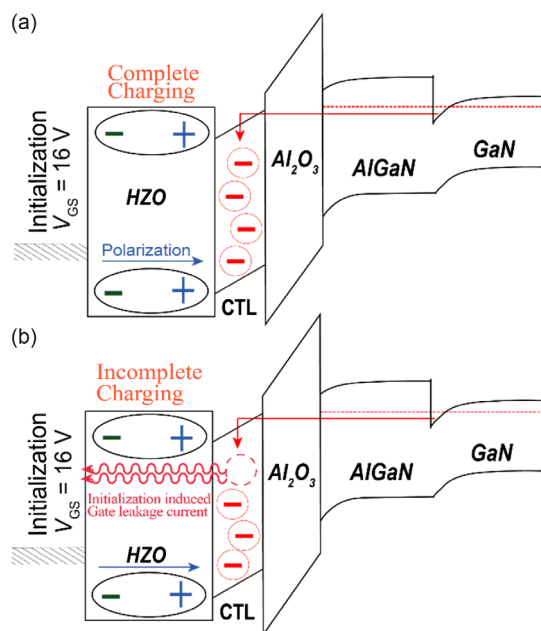


Figure 5. Schematic band diagram of a) complete charging and b) incomplete charging during the initialization process. Reproduced under terms of the CC-BY license.^[32] Copyright 2022, The Authors. Published by IEEE.

also resulted in better reliability under the PBTI (positive bias threshold voltage instability) and NBTI (negative bias threshold voltage instability) tests.^[32]

4. Ferroelectric Engineering Dedicated to FEG-HEMTs

Trivalent dopants, particularly those from the lanthanoid series, have been shown to be effective in inducing the ferroelectric

phase in HfO_2 films. These dopants are able to disrupt the local symmetry of the crystal lattice and promote the development of spontaneous polarization, which is a key characteristic of ferroelectric materials.^[29,34–39] Furthermore, the use of trivalent dopants has been found to improve the stability and reproducibility of the ferroelectric phase, making them particularly attractive for use in ferroelectric-based devices. Not only that, doping in HZO films with an acceptor center can rearrange the Fermi level of the HZO to the midgap position, which can significantly reduce the leakage current. With the unique advantage exhibited by lanthanum doping, both enhancing ferroelectricity and reducing leakage current, lanthanum is a suitable dopant, especially for the ferroelectric layer in E-mode FEG-HEMT devices.^[40–42] In this section, the study of the best ferroelectric stack for the E-mode FEG-HEMT is presented.

4.1. Lanthanum-Doped $\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$ with Plasma-Enhanced Atomic Layer Deposition-Grown Seeding Layer Ferroelectric Engineering Technique

In ref. [43], Wu et al. investigated the use of a 0.4 mol% La-doped $\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$ (HZLO) with a plasma-enhanced atomic layer deposition (PEALD) grown seed layer (SL) in FEG-HEMTs. First, MFMs (metal/ferroelectric thin film/metal) were analyzed. In the experimental results,^[43] the HZLO MFMs exhibit increased ferroelectricity, wake-up-free behavior (little transition from a nonferroelectric phase to a ferroelectric phase), and reduced leakage current when post deposition annealed (PMA) at higher temperatures (700 °C) took place. These characteristics show promising results for the ferroelectric engineering of the FEG-HEMT. However, on the downside, La acts as an amorphizer in hafnium oxide.^[44,45] Consequently, there always seems to be a trade-off between the appropriate crystalline structure and the thermal budget of the doped HfO_2 -based ferroelectrics. The requirement for high annealing temperatures in order to attain a high remanent polarization and reduced leakage current was not practical for device processing. Lowering the thermal budget while maintaining the benefits of La doping is a challenge to overcome.

A seeding layer method was implemented to tackle the thermal budget challenges. ref. [43] introduced the incorporation of a PEALD-grown ZrO_2 SL prior to the growth of the HZLO film, which enhanced the nucleation and significantly reduced the required post-deposition annealing temperature. Literature and studies have shown that a deposition of a ZrO_2 seeding layer before HZO thin film growth could promote the vertical growth of a noncentrosymmetric α -phase in the HZO during the crystallization annealing process.^[46,47] Two MFM structures were analyzed: (a) TiN/HZLO (10 nm)/TiN and (b) TiN/HZLO (9 nm)/SL (1 nm)/TiN. When added the seeding layer, the $2P_r$ of the HZLO film (PMA (post metal anneal) at 400 °C) increased from 12 to 18 $\mu\text{C cm}^{-2}$. Furthermore, the HZLO with seeding layer MFM also exhibits wake-up-free behavior at a low PMA of 400 °C, whereas this behavior is only observed at a higher PMA (700 °C) when the seeding layer was not implemented. This demonstrated a more stable ferroelectric behavior which aided the V_{th} stability of the FEG-HEMT. Furthermore, the leakage current of the HZLO/SL MFM exhibited a significantly mitigated soft

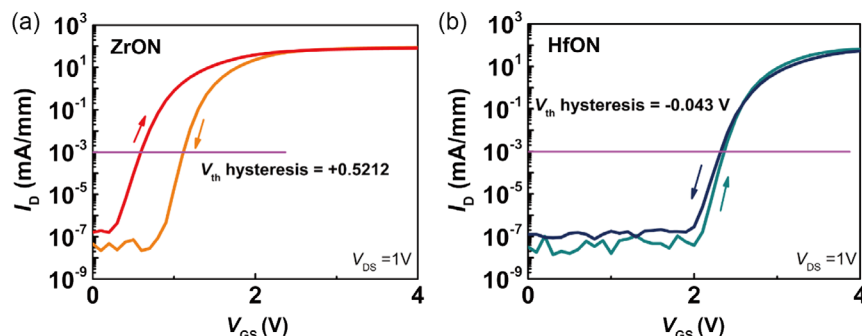


Figure 6. I_D - V_G hysteresis of FEG-HEMTs with a) ZrON and b) HfON as charge trapping layers. Reproduced under terms of the CC-BY license.^[32] Copyright 2022, The Authors. Published by IEEE.

breakdown and hard breakdown, compared to the HZLO MFM. The use of PEALD-grown ZrO_2 as a SL has been shown to promote the formation of the α -phase, improve crystallinity, and reduce the thermal budget (annealing temperature). The SL layer incorporation before the HZLO deposition could effectively decrease the needed annealing temperature to achieve the characteristics benefiting the FEG-HEMT. These superior characteristics displayed by the HZLO/SL MFM provide insight into potential ways to improve the ferroelectric gate stack in the E-mode FEG-HEMT devices.

4.2. High-Performance FEG-HEMT with HZLO/SL Laminated Ferroelectric Stack

The E-mode GaN FEG-HEMT exhibited a positive threshold voltage of 3.7 V (defined at a drain current density of $1 \mu\text{A mm}^{-1}$) after initialization and a small threshold voltage hysteresis of 0.12 V. The output characteristics showed a maximum drain current density of 560 mA mm^{-1} and an on-resistance of $9.8 \Omega \text{ mm}$. Due to the suppression of soft breakdown effects and the reduction of leakage currents through La-doping in HZO, the device displayed a high off-state breakdown voltage of 917 V at a V_{GS} of 0 V. The dynamic on-resistance to static on-resistance ratio exhibits a low value of 1.37 with a switching time of approximately 150 μs (Figure 7).

4.3. Aiming for Large Gate Breakdown, High TDDDB Lifetime, and Long Threshold Voltage Retention Time

Despite the attractive features of a larger gate swing and reduced gate leakage, the commercialization of the recessed-gate E-mode GaN MIS-HEMTs has been delayed compared with that of the p-GaN power transistors due to concerns regarding to the threshold voltage stability and gate dielectric reliability. For the commercialization of the FEG-HEMTs, the stability of the gate stack and V_{th} retention have to be confirmed. Ferroelectric engineering of the FEG-HEMT with lanthanum doping and seeding layer incorporation has shown excellent improvement in gate leakage reduction and ferroelectric behavior stability. Providing sufficient stability and reliability for the commercialization of the FEG-HEMT have been demonstrated.

The gate leakage characteristics of the FEG-HEMT in ref. [43] showed similar improvements in the HZLO/SL MFM as reported before. The use of an enhanced nucleation seeding layer and the crystallization of La_2O_3 resulted in the absence of soft breakdown until a V_{GS} of 25 V, while a high hard breakdown voltage occurred at 26.6 V. The improved gate breakdown leads to a larger off-state breakdown voltage, more complete charging of the CTL, and a higher gate swing.

Time-dependent dielectric breakdown (TDDDB) has been extensively studied in various technologies such as Si-based and III-V devices and can be used to evaluate the reliability and stability of

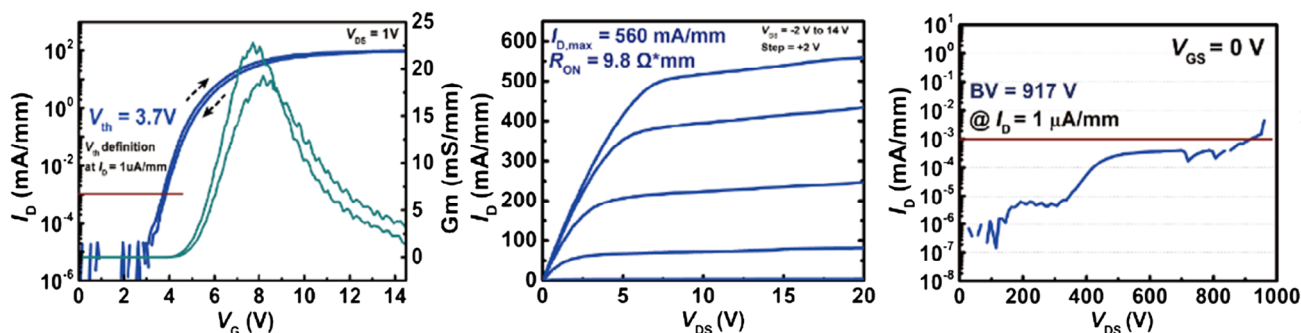


Figure 7. Transfer, output, and BV characteristics of the FEG-HEMT with HZLO/SL laminated ferroelectric gate stack. Reproduced with permission.^[43] Copyright 2022, IEEE.

transistors.^[48,49] TDDDB experiments typically involve applying a constant current stress (CCS) or constant voltage stress (CVS) to a group of transistors while monitoring changes in current with respect to time. When the gate is biased at a high voltage, the strong electric field causes a gradual degradation of the oxide, leading to an increase in its leakage current after a certain period of time. As stressed for a longer time, more random traps will be generated and a percolation path will be formed. Under these conditions, electrons can flow through this conduction path, resulting in a sudden increase in current and ultimately leading to oxide breakdown.^[48] The electric-field-accelerated TDDDB test was also performed on the FEG-HEMT with the HZLO/SL laminated ferroelectric-gate stack (**Figure 8**). The mitigated soft breakdown and delayed hard breakdown results indicated that the ferroelectric engineering could inhibit the percolation path formation. The Weibull distribution of the time-to-breakdown (t_{BD}) exhibited a slope $\beta > 3$, indicating a small variability and tight distribution in the breakdown behavior, making it reliable for E-mode power applications.^[49] Using a V_G power-law model to analyze trap generation and gate leakage mechanisms, the lifetime of the ferroelectric charge trapping gate stack is determined to be 13.76 V at a failure rate of 63.2% and 13.38 V at a failure rate of 0.01%. Literature suggests that the reported lifetime of p-GaN devices with a failure rate of 63.2% and a duration of 10 years is less than 6.5 V. In comparison, the FEG-HEMT displayed not only exceptional electrical characteristics but also a high TDDDB lifetime, indicating a larger gate voltage headroom for long-term, high-performance E-mode power operation.

Besides the gate leakage improvement, the V_{th} stability of the ferroelectric engineered FEG-HEMT is also addressed. The incorporation of an SL enhanced ferroelectricity and exhibited wake-up-free behavior, leading to a more stable ferroelectric behavior in the laminated ferroelectric stack. The V_{th} retention time was measured by an initialization process at first and then an $I_D V_G$ sweep after given time intervals of resting, meaning that the device was not biased during the V_{th} retention test period. The E-mode FEG-HEMT exhibited a threshold voltage of 3.1 V after a 30 000-second V_{th} retention test ($V_{GS} = 0$ V, $V_{DS} = 0$ V). In addition, the threshold voltage values after 1000 s of retention testing showed a stable trend. Therefore, the threshold voltage values at 1, 10, 20, and 30 k seconds were extracted and fitted using a power law. An estimated threshold voltage of 2.9 V was determined for a retention time of 10 years.

5. Field Plate Engineering for E-mode GaN FEG-HEMT: A Source-Connected Field Plate Technology

In Section 3 and 4, we reviewed electrical characteristic enhancement technologies regarding the engineering of the ferroelectric charge trap gate stack. In this section, a field plate scheme demonstrated by ref. [50] is discussed. A proposed SCFP structure by Wu et al.^[50] was fabricated to stabilize the V_{th} of the FEG-HEMT under high drain biases.

As previously mentioned, it is important to fully consider the charging and discharging of electrons in the CTL of FEG-HEMTs as they can lead to device failures. In GaN HEMTs, the OFF-state breakdown often occurs due to an avalanche process at the drain side of the gate edge, which experiences a high electric field in the OFF state (high drain voltage and low gate voltage).^[51] This high electric field causes electrons to escape from the CTL at a rapid rate, resulting in a negative V_{th} shift to the pristine D-mode regime and causing device false turn on (**Figure 9**). Furthermore, one of the benefits of GaN devices is the high breakdown field due to the material properties. In order to fully demonstrate the potential of E-mode FEG-HEMTs for future power applications, the V_{th} stability under high drain bias must be fully addressed, which is the emphasis of this study.

To further mitigate the threshold voltage instability under high-voltage switching operations, field plate engineering is adopted.^[52–54] Lately, there has been another way to further improve field plate structure. Mao et al.^[55] proposed a novel T-shaped source field plate, showing the structure of a T-shaped source field plate with a trench metal that penetrates the passivation layer. The T-shaped source field plate HEMT can modulate the electric field profile more effectively and have better performance thanks to the trench metal, which is closer to the 2DEG channel and further extends the depletion region.^[56]

Reference [50] introduced a SCFP approach that illustrates a new concept to isolate the high electric profile at the drain-side gate edge. The SCFP approach was to fabricate an inner field plate next to the gate metal and connect it to the source. This novel SCFP approach aimed to create a secondary D-mode MISHEMT structure by incorporating a cascode-like configuration, which consists of an E-mode GaN FEG-HEMT and a secondary D-mode MISHEMT structure in the same device. The secondary D-mode MISHEMT structure had a lower

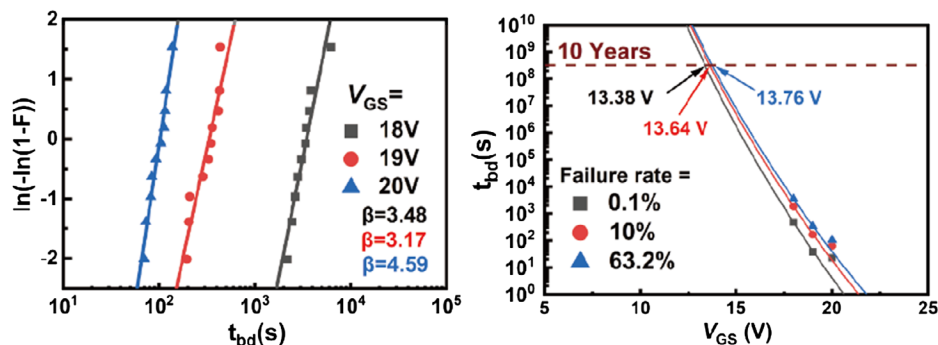


Figure 8. Weibull plot and lifetime prediction of the FEG-HEMT with La-doped HZO/PEALD ZrO_2 seed layer laminated ferro-gate. Reproduced with permission.^[43] Copyright 2022, IEEE.

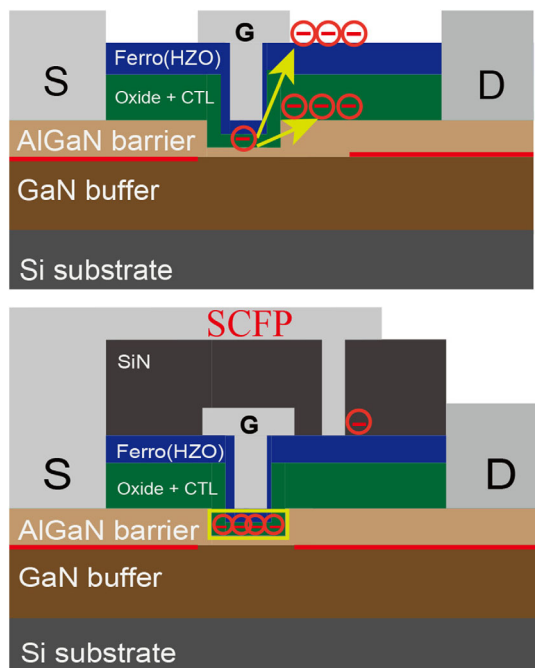


Figure 9. Schematic illustrations of the charge leakage mechanism under a high drain bias in FEG-HEMTs with and without a field plate structure.

on-resistance and a smaller junction capacitance.^[56] Furthermore, the high electric profile that was originally located at the drain-side gate edge was successfully relocated.

5.1. The Source-Connected Field Plate FEG-HEMT Performance

Three samples were compared for DC characteristics, dynamic R_{ON} , ON-state current degradation, and OFF-state V_{th} retention in ref. [50] One was a normal AlGaIn/GaN HEMT without a field plate (NFP FEG-HEMT), another was an AlGaIn/GaN HEMT with a top field plate (TFP FEG-HEMT), and the other was an AlGaIn/GaN HEMT with both a top field plate and a SCFP (SCFP FEG-HEMT). **Figure 10** shows the schematic structures of the three samples. The SCFP FEG-HEMT device showed a V_{th} value of 2.81 V, a maximum drain current of 757.2 mA mm^{-1} , and a breakdown voltage of 866.3 V (**Figure 11**). Overall, the SCFP sample exhibited a higher breakdown field compared to the TFP sample. The additional 2nd MISHEMT, created by the inner field plate, can further increase the breakdown voltage compared with the TFP HEMT. Due to the closer distance of the inner field plate to the 2DEG, the device with SCFP can modulate the electric field profile more effectively and achieve a higher breakdown.

Furthermore, the SCFP sample showed a 25% lowered dynamic R_{ON} when operated at $V_{DSQ} = 400 \text{ V}$. The D-mode MISHEMT was able to redistribute the high electric field profile

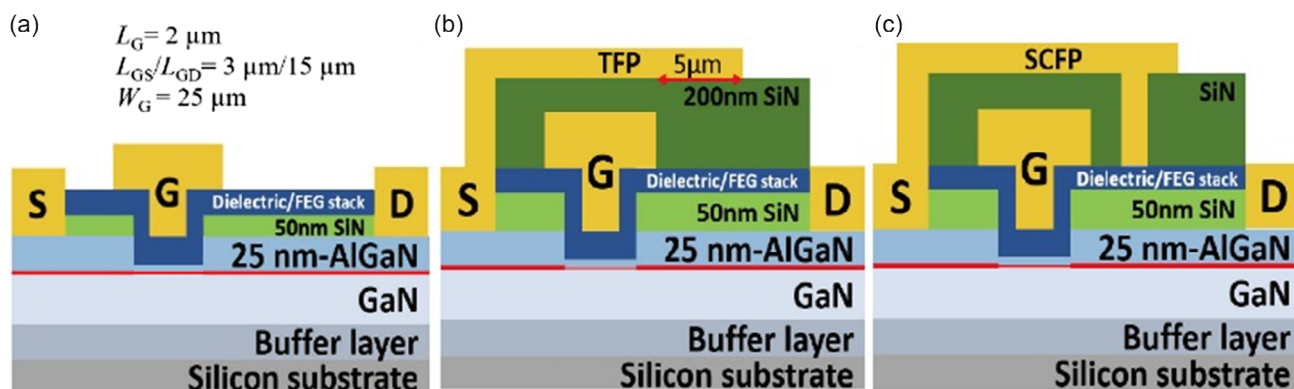


Figure 10. Schematic structures of FEG-HEMTs (dielectric/FEG stack: $\text{Al}_2\text{O}_3\text{-HfZrO}_4\text{-Al}_2\text{O}_3\text{/HfON/Al}_2\text{O}_3$) for a) NFP, b) TFP, and c) SCFP samples.

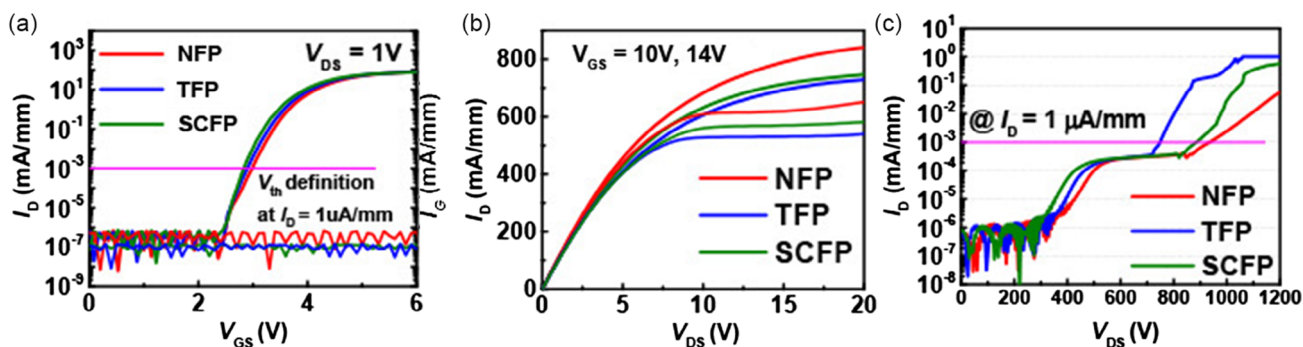


Figure 11. a) Transfer characteristics, b) output characteristics, and c) OFF-state breakdown characteristics of the NFP, TFP and SCFP HEMTs. Reproduced with permission.^[50] Copyright 2021, IEEE.

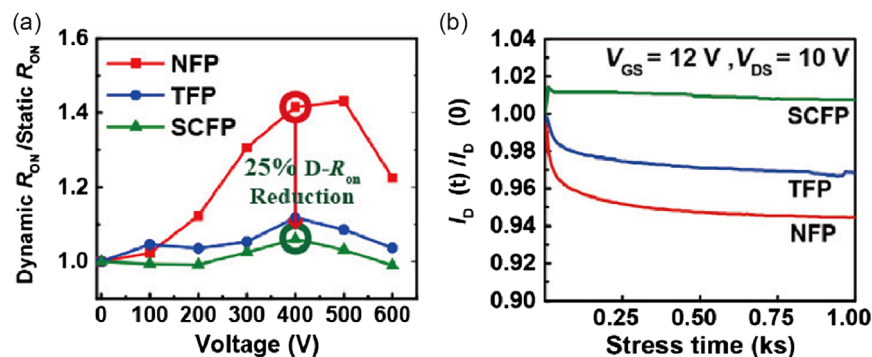


Figure 12. a) Dynamic R_{ON} ratio comparison and b) ON-state stress test result comparison of the GaN FEG-HEMTs with field plate. Reproduced with permission.^[50] Copyright 2021, IEEE.

Table 1. Summarization of the GaN FEG-HEMT device performance.

	V_{th}	$I_{DS,max}$	Max rating (V_{Gmax})	Breakdown voltage
E-mode GaN MIS-HEMTs with hybrid ferroelectric charge trap gate (FEG-HEMT)	2.5–5 V (depending on the V_{th} before initialization)	>700 mA mm	23 V	>800 V

from the original gate edge to minimize trappings near the drain-side gate edge. Furthermore, the reversed polarization effect could help to avoid trapping under high drain biases. This could be beneficial in maintaining the stability and reliability of the device under highly drain biased conditions. Additionally, the tight distribution of dynamic R_{ON} suggests that the D-mode MISHEMT could effectively control the flow of current through the device, which can contribute to the improved performance. To further investigate the trapping effects and to address virtual effects in FEG-HEMTs, an ON-state stress test was also illustrated. Besides the least dynamic R_{ON} increment, the SCFP structure also showed the least current degradation under high biased conditions. One possible reason implied for the reduced current degradation during the on-state was the creation of the nonrecessed D-mode MISHEMT by the cascode-like structure, which is likely to have a lower R_{ON} and better interface quality (Figure 12).

The V_{th} stability was addressed through a multicycle OFF-state V_{th} retention test. The SCFP structure was found to significantly reduce the negative shift percentage in threshold voltage (V_{th}) under high drain stress conditions. This was concluded due to the isolation of the CTL in the FEG-HEMT from the high drain stress by the secondary D-mode MISHEMT. The D-mode MISHEMT effectively absorbs the majority of the high electric field distribution, thereby protecting the CTL from the adverse effects of the high OFF-state stress. This resulted in a more stable V_{th} behavior and improved performance of the FEG-HEMT. Table 1 summarizes the performance of E-mode GaN MIS-HEMTs with hybrid ferroelectric charge trap gate (FEG-HEMT) in this review.

6. Conclusion

Driven by the demands for power devices with enhanced performance that meets the power system requirements, E-mode

AlGaIn/GaN devices with high V_{th} are the must. The novel hybrid ferroelectric charge trap gate stack scheme has given a brand new perspective on how to achieve E-mode operation in GaN MIS-HEMTs to meet the system requirements, such as EV and solar panels. We have made efforts to further improve the performance of the FEG-HEMT for future power applications. In this review article, we focus on various concepts and methods to improve the FEG-HEMT performance including nitrogen incorporation in the oxide-based CTL and lanthanum doping with seeding layer ferroelectric engineering. Along with the enhanced ferroelectric charge trap gate stack, an initial demonstration of a SCFP is also discussed. With all these progress in technology, the E-mode GaN FEG-HEMT technology is expected to play an important role in future GaN power electronics.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

AlGaIn/GaN, enhancement mode, ferroelectric charge trap gate stack, GaN, metal-insulator semiconductor (MIS)-HEMT, threshold voltage stability

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