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GaN Power HEMT > 650 V: A Parametric Analysis and Comparison to SiC MOSFET

🕒 June 23, 2022 [Sonu Daryanani](#)*This article focuses on the detailed parametric analysis and comparison between GaN Power HEMT > 650 V and SiC MOSFET.*

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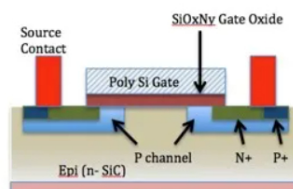
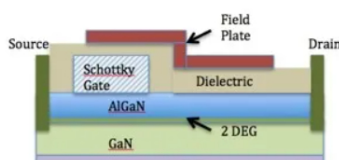
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Over the last few years, SiC MOSFETs have enjoyed a dominant role in high voltage (>600V) and high power applications. The advantages in thermal conductivity, high critical fields, much-improved switching efficiency, and the ability to form silicon dioxide on its surface have allowed key process, design and reliability improvements allowing its large-scale usage in some high-growth applications such as in EV's for board chargers, traction inverters and DC to DC converters, PV inverters, motor control, transport systems and the power grid.

Back in the 1990s, most research on GaN was focused on the creation of blue and eventually white, LEDs and lasers. The direct bandgap of ~ 3.4 eV, the ability to form quaternary layers with Al, In, P and quantum confinement through hetero-junction layers created through Metal-Organic CVD (MOCVD) laid the foundation for this. This work was then leveraged to take advantage of the high electron mobility and saturation velocity achieved in High Electron Mobility Transistors (HEMT) to create RF devices far superior to their Si counterparts. It is in this area of RF MMICs that the GaN PowerHEMT process and design technologies were significantly improved, and today, these form the backbone of some of the essential Communication, Radar and Electronic Warfare equipment, some with frequency ratings exceeding or at the RF X-Band spectrum (8.5 to 11 GHz).

The voltage range for these RF devices was typically in the <200V range. The lateral HEMT device has natural disadvantages over the Vertical V-DMOS typically used in SiC MOSFETs for HV device creation (see Figures 1 (a) and 1(b) for representative device cross-sections). High surface electrical fields in the lateral drift region between the gate and drain typically would limit the high voltage limits, and several advances in field plate technologies that shape/lower the electrical field would allow improvements in this rating.

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In the dynamic field of electronics, there is a

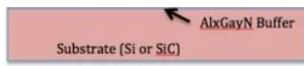


Figure 1 (a)

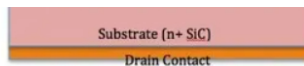


Figure 1(b)

Figure 1 (a) GaN Power HEMT device structure and Figure 1 (b) SiC VDMOS device structure

Table 1 lists some of the key material properties of SiC and GaN.

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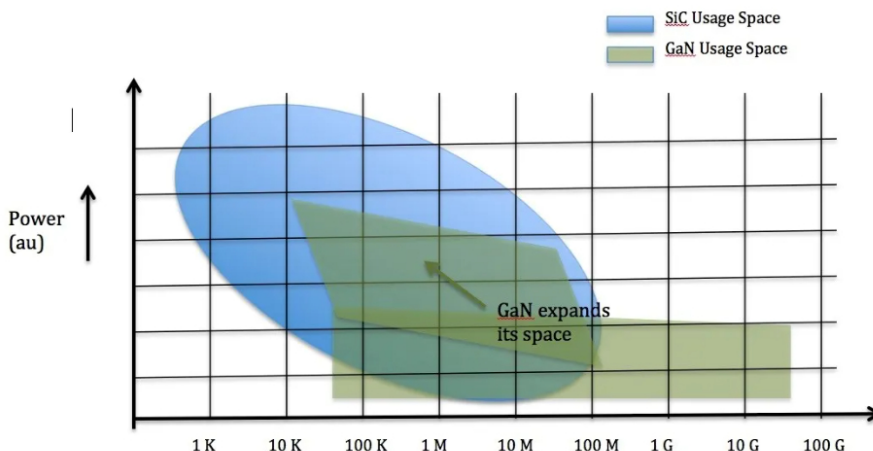
	4H-SiC MOSFET	GaN HEMT
Bandgap eV	3.26	3.39
Ecrit MV/cm	2.2	3.3
Electron Mobility in Device cm ² /V-s	<100	1500-3000
Vsat cm/s (x 1x10 ⁷)	2	3
BFOM (relative to Si)	500	2700
λ W/cm-K	4-5	1.3-1.7/4*
		* GaN on SiC substrates

Table 1: Some Key Material Properties of SiC MOSFET and GaN Power HEMT. The BFOM is the Baliga Figure of Merit

It should be noted that though the bulk SiC mobility as quoted in the literature is much higher (~ 700 to 1000 cm²/V-s), the mobility obtained in the MOSFET is much lower, though to be due to trapping sites at the SiC/SiO₂ interface. The mobility listed for the GaN Power HEMT is observed and reported on the 2 Dimensional Electron Gas (2-DEG) formed at the AlGaIn/GaN interface, which forms the conduction channel of the device.

From this initial focus on RF devices, tremendous progress has been made on GaN transistors to deliver devices in the HV power FET range. Several companies such as Transphorm, ST Microelectronics, GaN Systems, Cambridge, Innoscience, GaN Power International, and Texas Instruments, to name just a few, offer devices at a 650V rating or higher. From a voltage perspective, this hits the sweet spot for several EV applications such as Level 2 On-Board Chargers (OBCs) and other applications long considered to be in the SiC domain. GaN offers lower terminal capacitances and improved mobility allowing device scaling and faster, more efficient switching. The lack of a p-n junction also allows for no reverse recovery loss from switching. Heat transfer and packaging then become key constraints, and a lot of research is now focused on improving this.

Figure 2 and Figure 3 below illustrate the expanding space of GaN in these applications.



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Figure 2: The growing space of GaN in the SiC power FET space

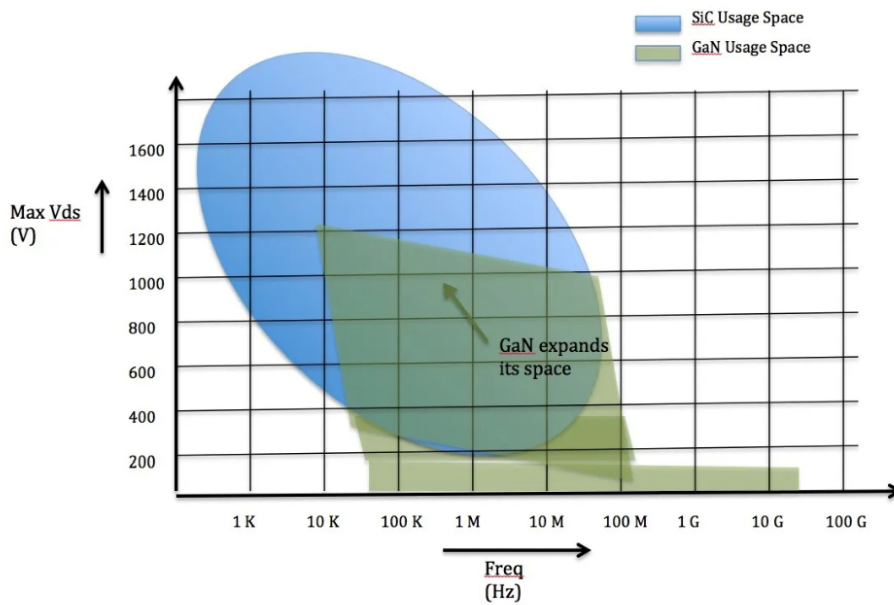


Figure 3: Voltage vs Freq space usage of GaN Power HEMT

The growth of GaN is typically done either on SiC or Si substrates. Buffer layers help relieve the stress from the lattice mismatch. RF GaN manufacturers have typically opted for the GaN on SiC approach to leverage SiC's superior thermal capability for the high power density amplifiers. The Power FET industry has opted for the GaN on Si approach. The Si substrate offers a much cheaper approach and also offers an easier path for 200 mm wafer manufacturing. Innoscience has demonstrated this with their 8-inch GaN on Si Fabs in China.

The GaN Power HEMT device is naturally a depletion mode device (or d-mode: normally on, would need a negative V_{gs} to turn off). For most Power FET applications, an enhancement mode (or e-mode: normally off, 0V should turn the device off) behaviour is essential. To this end, two different approaches have been used. On the one hand, barrier height modifications can be done using a p-type GaN or AlGaIn gate, creating a depleted region underneath this layer that would create a normally-off device. This approach has been favoured by many to produce e-mode HEMT devices. Another approach has been to cascode an LV Si-MOSFET in series with the GaN device, as shown in Figure 4.

Tradeoffs exist between the two approaches. While the single e-mode device is simpler to use, makes paralleling devices less complex and offers superior capacitance and reverse recovery characteristics, the problem is that it is hard to achieve a threshold voltage much above 1.5V due to characteristics of the p-AlxGayN layer. This leaves the gate subject to switching noise and spurious device behaviour.

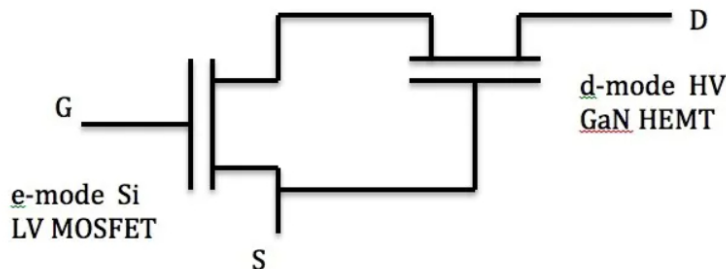


Figure 4: GaN d-mode HEMT in a cascode arrangement

A much more robust gate is obtained with the cascode scheme, with $V_{t's}$ in the favoured $\geq 2.5V$ range. The higher gate margin can enable a more straightforward gate driver.

To compare the device behaviour and the pros and cons of each approach, a parametric analysis is presented in Table 2 below. In this analysis, four devices are selected, two SiC MOSFETs and two GaN Power

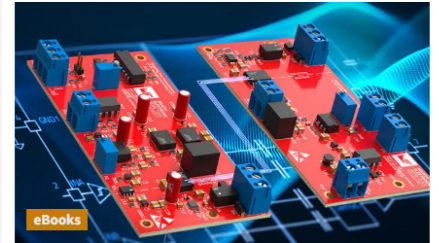
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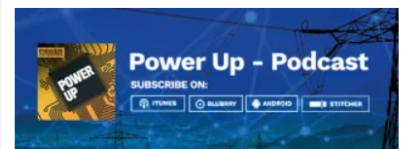
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July 25, 2024 [Maurizio Di Paolo Emilio](#)

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HEMTs. All four have a maximum Vds operation voltage of around 650V and a 25C Rdson rating of around 20 mOhms. The two GaN devices are labelled G1 and G2, while the SiC devices are S1 and S2. Devices S2 and G2, in addition, use the same package, so package-caused differences in some of the AC characteristics can be discounted in this case.

Company	S1	G1	S2	G2
Device	SiC MOSFET	GaN HEMT	SiC MOSFET	GaN HEMT + Si LV FET
Comment	Trench V-DMOS	non cascode e-mode	Planar VDMOS	cascode d-mode HEMT
Vds rating	650 V	650V	700 V	650 V
Rdson typ (25C)	18 mΩ @50 A, 18 V Vgs	25 mΩ @10 A, 6 V Vgs	15 mΩ @40 A, 20 V Vgs	15 mΩ @60 A, 10 V Vgs
Rdson (hot)	27 mΩ, 175°C, 18 V Vgs	65 mΩ @150°C	19 mΩ, 175°C, 20V Vgs	31 mΩ, 150°C, 10V Vgs
Vgs rating	-5 V to 18 V (recommended)	-10 V to 7 V	-10 V to 23 V	-20 V to 20 V
Vth (V)	3.2 V @ 1mA Ids, Vgs= Vds	1.7 V @ 14mA Ids, Vgs=Vds	2.4 V @ 4mA Ids, Vgs = Vds	4.0V @ 2mA Ids, Vgs = Vds
Vplat	5.5 V	4.0 V	5.5 V	6.5 V
Vgs margin	12.5 V	3.0 V	17.5 V	13.5 V
Id (cont) 25C	116 A	60 A	140 A	93 A
IDM pulse (A) (with SOA)	220 A	120 A	350 A	600 A
Tjmax	175 °C	150 °C	175 °C	150 °C
Qg nC/condition	157 nC (400V Vds, 50A)	14.2 nC (400V Vds, Vgs 6V)	215 nC (470V Vds, 40A)	74 nC (400V Vds, 60A)
Qoss nC	117	134	357	123
Pd max (25C)	484 W	460 W	455 W	266 W
Vsd (V) /condition	2.5 V @ 30A	3.4 V @ 50A	3.4 V @ 40A	1.6 V @ 60A
Qrr	308 nC (50A, 400V Vds, 4000 A/μs)	0 nC	495 nC (40A, 470V Vds, 1200 A/μs)	430 nC (60 A, 400 V Vds, 1000 A/μs)
Rthjc	0.31 °C/W	0.27 °C/W	0.22 °C/W	0.47 °C/W
Igss 25C	< 100 nA over Vgs	320 uA, Vgs 6V	< 100 nA over Vgs	< 400 nA over Vgs
Idss 25C	< 10 μA over Vds	4 μA over Vds	< 100 μA over Vds	7 μA over Vds

Table 2: Parametric Comparison of 2 SiC devices S1, S2 with 2 GaN Power HEMT devices G1, G2

Parameters of concern are highlighted in yellow and favourable ones in green. It is immediately obvious that G1, with its single e-mode device, offers a key advantage of GaN, namely no reverse recovery charge Qrr. The poor gate margin, though, is also highlighted by the much higher I_{gss} gate leakage. G2 on the other hand, has good gate margins, much like SiC, but with a corresponding increase in Qrr.

Generally, the lower gate charge Qg is highlighted in both GaN Power HEMTs. This can create a significant improvement in hard switching applications.

One clear disadvantage of GaN highlighted in Table 2 is the poor temperature coefficient of Rdson, with ≥ a doubling of the 25oC Rdson at 150C. It could also be argued that if the goal is to meet a certain 150oC Rdson, the GaN device would effectively have to be built with excess margin at 25oC, with a corresponding increase in die size and gate/output capacitance. The Rdson increase makes a more parallel device approach more critical. Paralleling GaN devices can present challenges due to the diverse parasitic components, especially in the cascoded arrangement. Integrated gate drivers with adaptive control can be a possible solution.

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Sonu Daryanani received his Ph.D. in Electronics Engineering in 1993 from the University of Bradford, England while doing research at AT&T Bell Labs, NJ on GaAs optoelectronics. Over the last 25 years he was a Device/Process Integration Engineer at Microchip Technology, AZ working on microcontroller and discrete devices. He is now a consultant and writer for PowerElectronics News. He can be reached at sldaryanani@gmail.com

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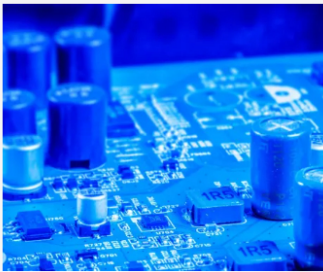
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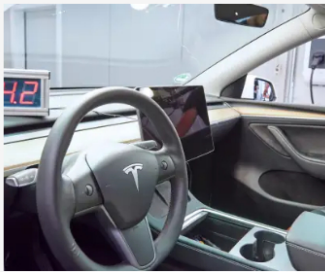
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