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Review

Circuit Models of Power MOSFETs Leading the Way of GaN HEMT Modelling—A Review

Enrico Bottaro, Santi Agatino Rizzo * and Nunzio Salerno

Department of Electrical Electronic and Computer Engineering, University of Catania, 95125 Catania, Italy; enrico.bottaro@unict.it (E.B.); nunzio.salerno@unict.it (N.S.)
* Correspondence: santi.rizzo@unict.it

Abstract: Gallium nitride high-electron-mobility transistor (GaN HEMT) is a key enabling technology for obtaining high-efficient and compact power electronic systems. At the design stage of a power converter, the proper modelling of the GaN HEMT is essential to benefit from their good features and to account for the limits of the current technology. Circuit models of power MOSFETs have been deeply investigated by academia and industry for a long time. These models are able to emulate the datasheet information, and they are usually provided by device manufacturers as netlists that can be simulated in any kind of SPICE-like software. This paper firstly highlights the similarities and differences between MOSFETs and GaN HEMTs at the datasheet level. According to this analysis, the features of MOSFET circuit models that can be adopted for GaN HEMT modelling are discussed. This task has been accomplished by overviewing the literature on MOSFETs circuit models as well as analysing manufacturers netlists, thus highlighting the models MOSFETs valid or adaptable to GaN HEMTs. The study has revealed show that some models can be adapted for the GaN HEMT devices to emulate static characteristics at room temperature while the MOSFET models of dynamic characteristics can be used for GaN HEMT devices. This study enables the devices modellers to speed up the GaN HEMT modelling thanks to the use of some well-established MOSFET models. In this perspective, some suggestions to develop accurate GaN HEMT models are also provided.

Keywords: silicon MOSFET; silicon carbide (SiC); SiC MOSFET; gallium nitride (GaN); GaN HEMT; wide-bandgap semiconductor; circuit model; behavioural model; power electronics; SPICE

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1. Introduction

The worldwide growth of environmental awareness has pushed toward the diffusion of green power sources and high-efficiency power components and systems [1–3]. In such a contest, the devices based on wide-bandgap (WBG) materials, in particular, silicon carbide (SiC) [4,5] and gallium nitride (GaN) [6,7], have a key role in developing high-efficiency converters. GaN high-electron-mobility transistors (HEMTs) also enable the design of highly compact power converters [8], which are very attractive in many industrial and commercial sectors [9]. More specifically, the encumbrance and weight lowering are achieved thanks to the reduction in the device size in comparison with previous technologies and, above all, thanks to the reduction in the size of passive components which is due to the ability at operating at a higher switching frequency [10,11]. Figure 1 shows the application areas of the three different device technologies. SiC devices are a candidate in substituting Si IGBT devices in applications such as traction inverters and industrial manufacturing sectors [12], while GaN devices are better than Si MOSFETs for the on-board converters and switch-mode power supply used in data centres and IoT applications [13].

The design stage of converters including GaN HEMTs is very critical due to the combination of their fast switching with the parasitic inductances of the packaging and board [14–16] that, in turn, interact with the parasitic capacitances of the device as well [17].

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Overvoltages and oscillations are some of the main related phenomena that could lead to many issues, e.g., exceeding the device breakdown voltage, electromagnetic interference, multiple false device trigger and so on [18–20]. These issues can be partially faced by innovative driving techniques [21] provided that an optimal design of the converter is performed.

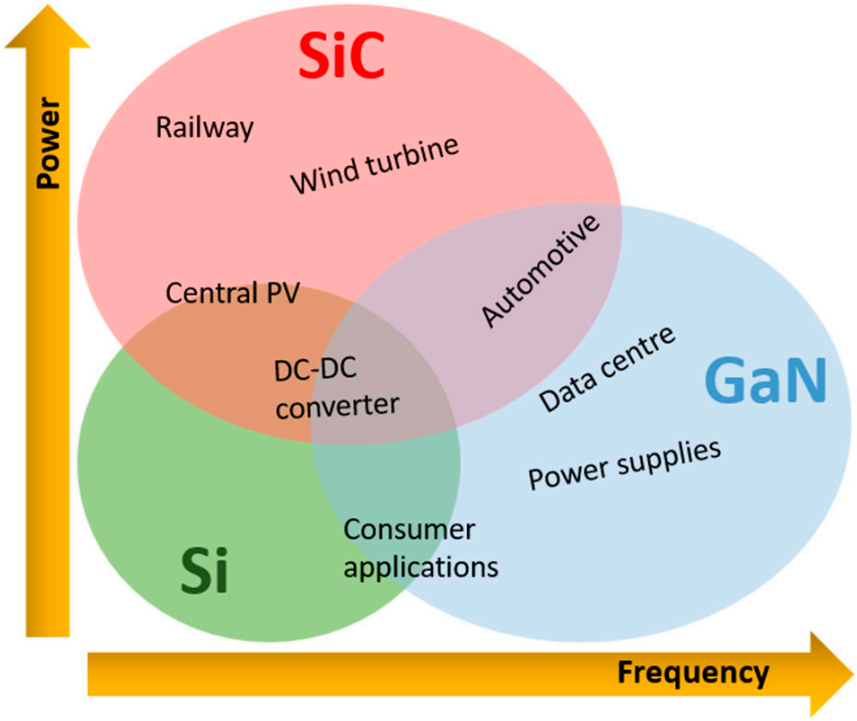


Figure 1. Main application fields of Si, SiC MOSFETs and GaN HEMT devices.

The computer-aided design (CAD) of a GaN-based power converter needs an accurate model of the device to foresee, by means of simulations, the efficiency and waveforms related to different design choices [22,23]. The use of enhanced models for the evaluation of efficiency is a common practice in many sectors [24,25].

The first modelling approaches date back to the 1970s with technology CAD (TCAD) software [26]. In this case, the model accounts for the device physics, and the modelling can support the device development, that is, the design of the device only (computer-aided manufacturing). On the other hand, these models can be useful at the converter design stage, since the knowledge of the physical relationships that govern the device, embedded into the converter, enable them to accurately foresee its behaviour [27]. However, when these device models are used for converter design, the simulation time could be unacceptable in the industrial sector [28]. Another problem is that device models themselves could require a great development effort and time. Moreover, they require information about the technology which is not available to the users. Hence, only the manufacturers can develop this kind of model. In this case, probably, the model is provided as a black box (since manufacturers usually do not want to provide technology information) developed for simulation in specific tools.

Behavioural models consist of a set of equations that do have not any relation to the device physics [29]. The parameters of the equations are set to emulate the device behaviour at the terminals, and they can be easily implemented in SPICE-like simulation tools, largely adopted both in industrial and academic contexts [30,31]. This black-box approach can be used also in the modelling of power converters [32]. The major issue of the behavioural model is the identification of the value of the parameters to obtain simulations results that fit with measurements [33]. To perform this task, the use of stochastic optimization algorithms is the best way to find the optimal value of the fitting parameters, that is, the

value involving a better approximation of the actual waveforms [34]. Finally, semi-physical models are behavioural models partially based on device physics. Semi-physical and behavioural models, referred to as "circuit models" in the following, are only considered in this paper.

The target of circuit modelling is fitting quantities and waveforms obtained by simulation with the datasheet and laboratory measurements. In other words, the model must emulate the device behaviour in static and dynamic conditions. In this perspective, the circuit model must be accurate to properly support the design stage. On the other hand, as said before, the time necessary for the development of the model and the computational effort the model requires during a simulation are important aspects to be considered. The development of models of new devices must consider these crucial aspects. Therefore, if a new device presents some features similar to those of another well-established device satisfying these conflicting targets, the new device can be modelled readapting the approach used in the (good) model of the latter to account for these features.

In this context, the main contribution of the paper is the analysis of the literature related to MOSFET models as well as the analysis of manufactures netlists that have been performed to highlight the features of MOSFET models that can be adopted for GaN HEMT modelling. The study has revealed that some models can be adapted for the GaN HEMT devices to emulate the static characteristics at room temperature, while the MOSFET models of dynamic characteristics can be used for GaN HEMT devices. This study enables the devices modellers to speed up the GaN HEMT modelling, thanks to the use of some well-established MOSFET models.

With this in mind, in Section 2, the main similarities and differences between power MOSFETs and GaN HEMT datasheets are analysed. The results of this comparison are combined, in Section 3, with an overview of power MOSFETs modelling approaches to highlight the ones that can be useful to develop circuit models of GaN HEMTs. Finally, the conclusion of the study has been reported.

2. Comparison between MOSFET and GaN HEMT

This section analyses the main similarities and differences between MOSFET (Si and SiC technologies) and GaN HEMT devices. The results of the comparison aim at highlighting the modelling approaches that can be transferred to GaN HEMTs. The comparison considers datasheet information and, more in general, the common data used to build circuit models of MOSFETs. More specifically the pieces of information usually considered for MOSFET modelling are:

- Output characteristic;
- Transfer characteristic;
- Threshold voltage;
- Conduction resistance;
- Third quadrant and reverse recovery current;
- Parasitic capacitances.

In the following, various datasheets of Si MOSFET, SiC and GaN HEMT devices from different manufacturers have been considered for each point in the previous list, since the curves for a given technology and analogous breakdown voltage are similar regardless of the product family or manufacturer.

The devices analysed have breakdown voltages of 600 V or 650 V. Most of the analyses focus on GaN HEMTs with 650 V breakdown, though many basic considerations apply to 100 V GaN HEMT characteristics as well.

The following sub-section shows some comparisons among the three technologies: Si MOSFETs, SiC MOSFETs and GaN HEMTs. For each comparison, different devices are chosen to confirm the similarity among the devices of the same technology.

Therefore, for all these devices, the same circuit modelling strategy can be adopted to emulate the characteristic (e.g., the same formula could be adopted).

2.1. Output Characteristic

The output characteristic is one of the most important features of any device. It reports the drain current (I_D) vs. the drain-source voltage (V_{DS}). Various curves at different gate-source voltages, at room temperature, are typically reported (see Figure 2a,c,e). The output characteristic is also evaluated at a different temperature above the room temperature. Typical values are 125 °C or 150 °C for Si MOSFETs and GaN HEMTs and 175 °C for SiC MOSFET only (see Figure 2b,d,f). The recommended range of gate-source voltage (V_{GS}) is usually between 4 V and 15 V for Si MOSFET, between 6 V and 20 V for SiC MOSFET, and between 2 V and 6 V for GaN HEMT.

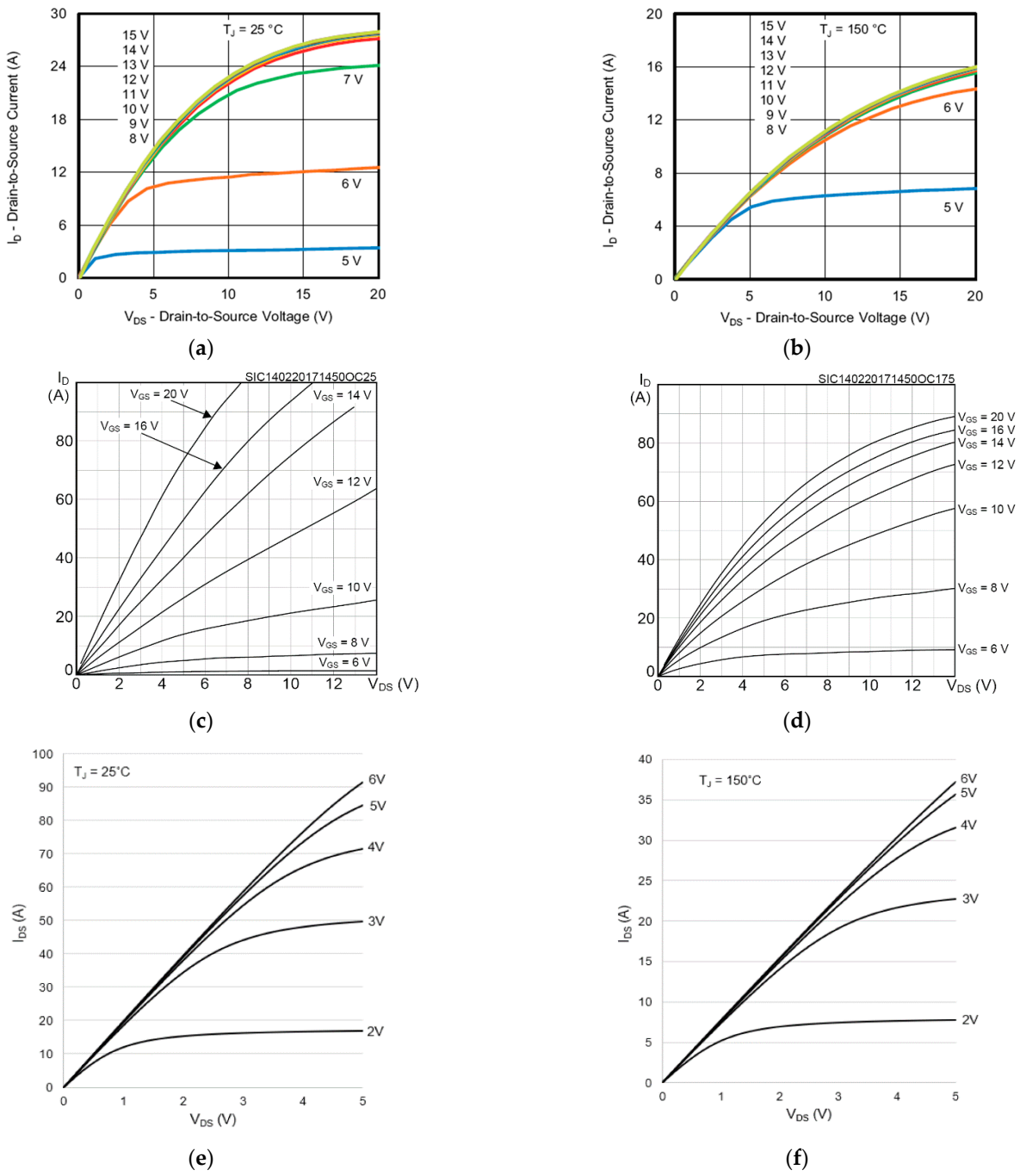


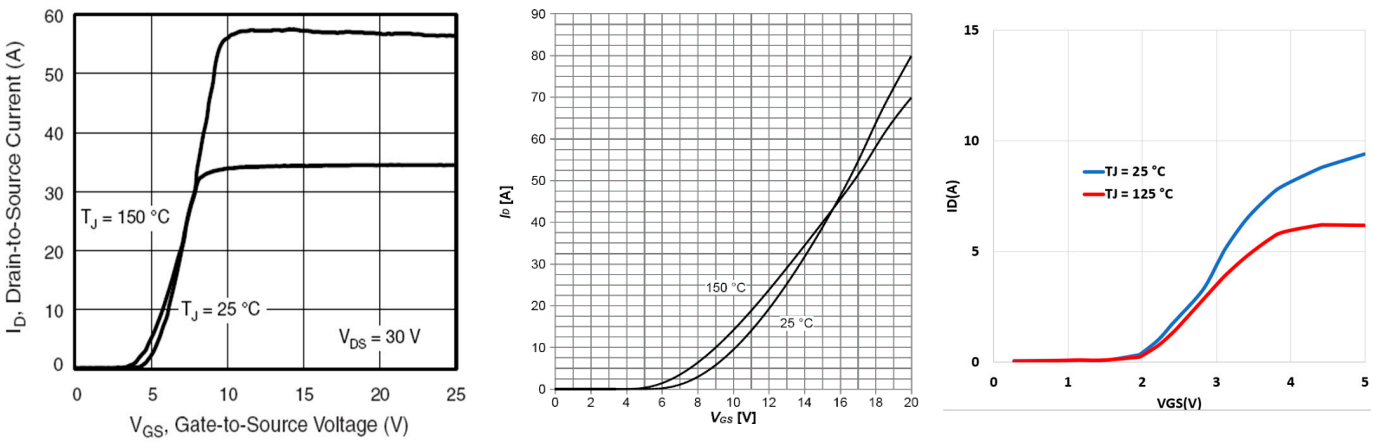
Figure 2. Output characteristics at 25 °C (**a**,**c**,**e**), 150 °C (**b**,**f**), and 175 °C (**d**). (**a**,**b**) Si MOSFET (Vishay SiHA15N80AEF) [35]; (**b**,**c**) SiC MOSFET (STMicroelectronics SCTL35N65G2V) [36]; (**e**,**f**) GaN HEMT (GaN System GS66508B) [37].

In the MOSFET characteristics, three different regions are identified: the cut-off, the linear-ohmic and the saturation region. The cut-off region is situated at the bottom of the output characteristic. In this region, devices are considered open switches. The linear-ohmic region concerns the low V_{DS} values with increasing current. The almost-flat zones are those where the MOSFET operates in the saturation region. The trend of the curves in the output characteristic of GaN HEMTs is similar to the MOSFET one. Figure 2 also highlights the dependence of the drain current on the temperature.

Considering Si and SiC MOSFET curves, when the temperature increases, the drain current increases for V_{GS} values up to approximately 6 V for Si MOSFETs (12 V for SiC MOSFETs), and it decreases for higher V_{GS} values. Instead, in GaN HEMT devices, as the temperature increases, the drain current decreases for any V_{GS}. The temperature behaviour just described is highlighted in Section 2.2.

2.2. Transfer Characteristic

The transfer characteristic relates the drain current to the gate-source voltage (V_{GS}). This characteristic is usually evaluated at different temperatures. The typical range of gate-source voltage (V_{GS}) is usually between 0 V and 20 ÷ 25 V for Si and SiC MOSFET, while it is between 0 V and 5 V for GaN HEMT. Figure 3 shows typical curves of the transfer characteristic.



(**a**) (**b**) (**c**)

Figure 3. Typical transfer characteristics at different temperatures: (**a**) Si MOSFET (Vishay SiHB22N65E) [38]; (**b**) SiC MOSFET (Infineon IMZA65R107M1H) [39]; (**c**) GaN HEMT (GaNPower GPI65008DF56) [40].

Figure 3 confirms the aforementioned variation of the drain current as the temperature increases at the various V_{GS} shown in Figure 2. More specifically, the intersection between the curves in Figure 3a (Si MOSFET) and Figure 3b (SiC MOSFET) confirms that, at low V_{GS}, the drain current increases as the temperature increases, while at high $V_{GS,}$ the drain current decrease as the temperature increases. The intersection point in Figure 3a,b is called zero temperature coefficient (ZTC). It corresponds to a gate voltage at which the device's DC electrical performance remains constant with temperature. The temperature coefficient defined as $\Delta I_D/\Delta T_J$ is positive below ZTC since the drain current increases as the temperature increases. While it is negative above ZTC, [41]. For V_{GS} values below the ZTC point, the device could suffer from thermal problems because the local hot spots lead to more current, and due to this phenomenon, local power dissipation rises that, in turn, increases the current, and a possible thermal runaway situation can occur. The lack of such an intersection in Figure 3c confirms that this phenomenon is absent in GaN HEMT devices, since the drain current always decreases as the temperature increases.

2.3. Threshold Voltage Characteristic

The threshold voltage (V_{TH} or $V_{GS,TH}$) is the minimum voltage to apply between the gate and source pin to create the conductive channel and start flowing current in the device [42]. The threshold voltage characteristic relates the V_{TH} to the temperature variation. This characteristic is very important because it affects the static characteristics (as output and transfer characteristics) when the device is simulated at a temperature different from the ambient one. The decrease in V_{TH} causes an early switch-on of the device. This behaviour can be seen at the bottom of Figure 3a,b because the current starts to flow at a lower voltage V_{GS} than the ambient temperature. The V_{TH} characteristic, for specified values of drain current and drain-source voltage, is commonly given in the datasheets, in the range from −50 °C to approximately 175 °C. For both Si and SiC MOSFETs, it decreases when the temperature increases; therefore, it has a negative temperature coefficient [43] (see Figure 4).

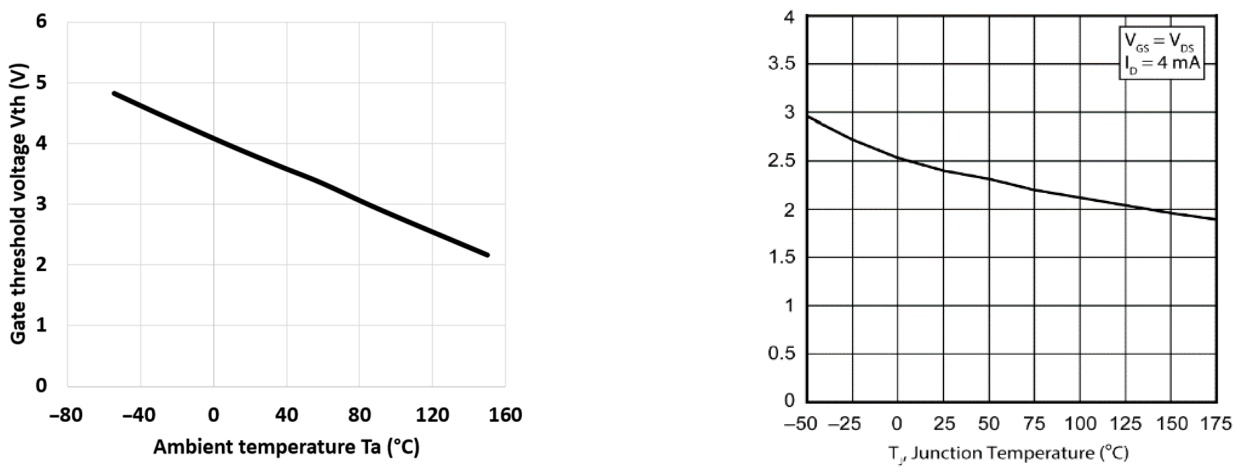


Figure 4. Threshold voltage: (**a**) Si MOSFET (Toshiba TK22V65X5) [44]; (**b**) SiC MOSFET (Microsemi MSC015SMA070B) [45].

Instead, in GaN HEMTs, since they have a different physical structure, the threshold voltage is almost temperature-independent, and usually, the V_{TH}-temperature curve is not shown in the device datasheets.

Figure 5 shows the threshold voltage vs. temperature in a GaN HEMT cascode device. In this case, the V_{TH} variation is due to the low-voltage Si MOSFET embedded in the cascode with a GaN depletion mode device.

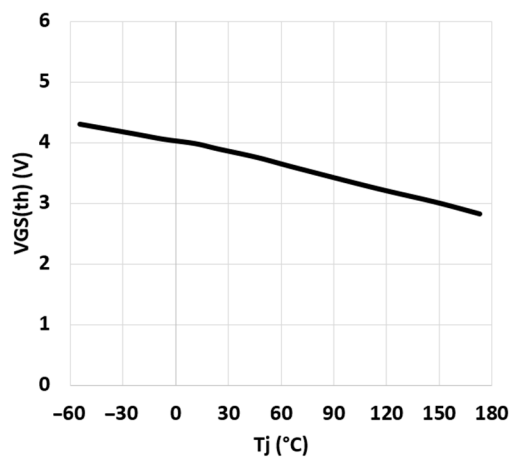
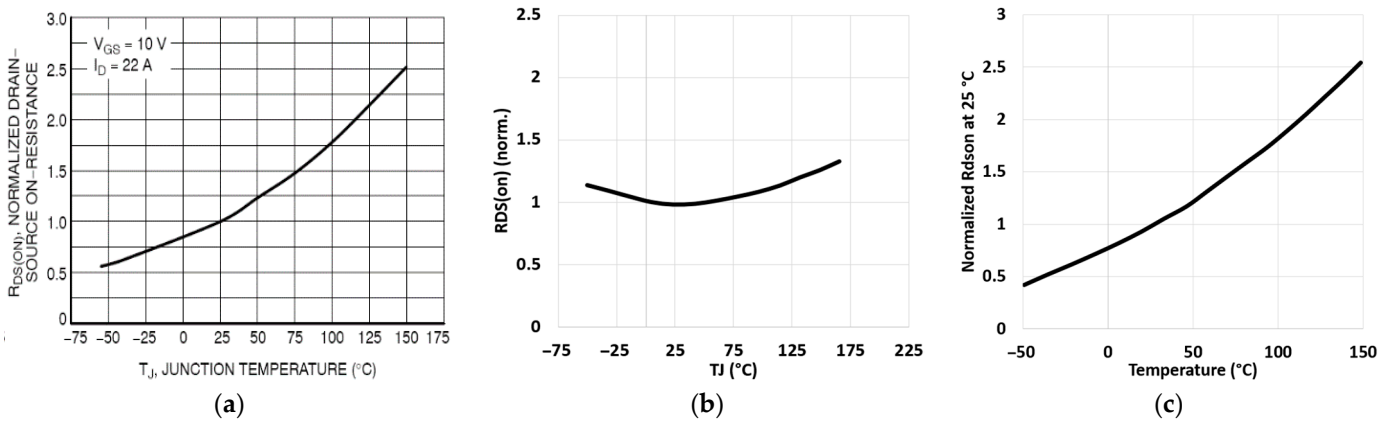


Figure 5. The threshold voltage of GaN HEMT cascode (NEXPERIA−GAN041650WSB) [46].

2.4. Static On-Resistance ($R_{DS,on}$) Characteristic

The static on-resistance, $R_{DS,on}$, is the drain-source resistance at a specified drain current and gate-source voltage in the linear-ohmic region of the output characteristic. The on-resistance characteristic is evaluated when temperature varies in the range approximately from −50 °C to 175 °C for Si and SiC MOSFETs, while between −50 °C and 150 °C for GaN HEMT. The on-resistance of the device is usually normalized to its value at 25 °C. This characteristic is useful to foresee the device conduction losses and is one of the most important in the evaluation of power efficiency. Figure 6 shows typical trends for Si, SiC MOSFET, and GaN HEMT Si MOSFET and GaN HEMT present an increasing on-resistance with increasing temperature (positive temperature coefficient), while in SiC MOSFET, $R_{DS,on}$ has a negative temperature coefficient (the on-resistance decreases as temperature increases) below 25 °C. On the other hand, above room temperature, the on-resistance increases, thus obtaining a typical U-shape characteristic. As shown in Figure 6, the trend of the 3 curves is similar to the room temperature.

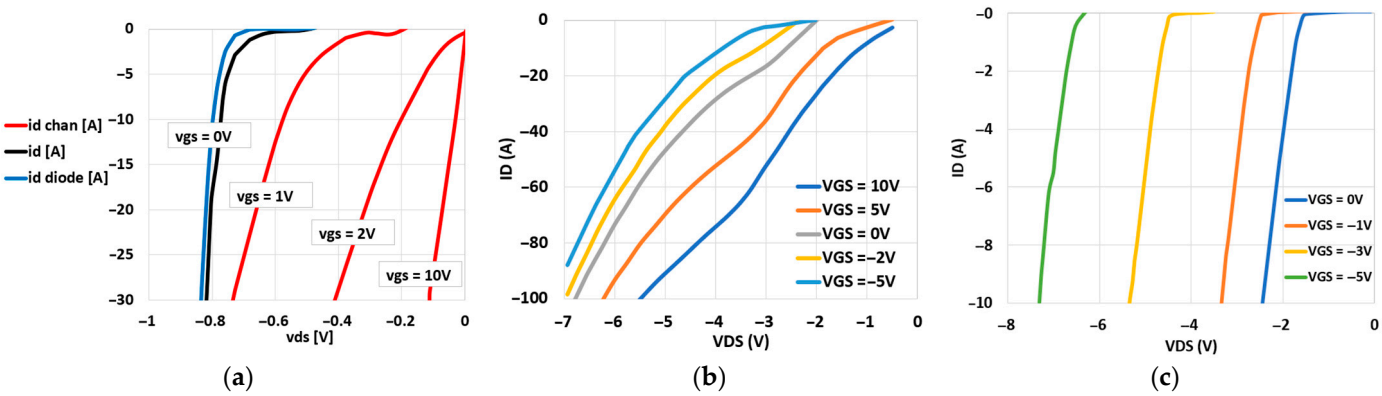


(**a**) (**b**) (**c**)

Figure 6. On-resistance versus temperature (**a**) Si MOSFET (ON Semiconductors NTBL070N65S3-D) [47]; (**b**) SiC MOSFET (STMicroelectronics SCTL35N65G2V) [36]; (**c**) GaN HEMT (GaNSystem GS−065−004−1−L) [48].

2.5. Third Quadrant and Reverse Recovery Current Characteristics

Third quadrant datasheets (Figure 7) refer to the device reverse conduction: negative drain current I_D vs. negative drain-source voltage V_{DS}. Curves for different gate-source voltage V_{GS} at T = 25 °C are given, in the typical range of drain-source voltage (V_{DS}) between −1 V and 0 V for Si MOSFET, and between −7 V and 0 V for SiC MOSFET and GaN HEMT. A MOSFET has an intrinsic body diode in its structure. This parasitic diode enables the third quadrant conduction, but it introduces the well-known problem of the reverse recovery current, which leads to much higher switching losses. Indeed, the value of V_{GS} also affects the third quadrant conduction, since it can reduce the voltage drop due to the current flowing into the channel. As shown in Figure 7a, at high V_{GS}, the current flows simultaneously in the MOSFET channel and the diode, but when the V_{GS} voltage becomes close to a negative value, the current starts to flow in the diode only [49]. As shown in Figure 7b, for a given current, the negative source-drain voltage drop increases as V_{GS} decreases. Finally, when V_{GS} becomes negative causes a change in the knee and the slope of curves (see Figure 7b).



(**a**) (**b**) (**c**)

Figure 7. Third quadrant conduction of (**a**) Si MOSFET: total drain current (black curves) is the sum of the body diode current (blue curve) and the channel current (red curves) [50]; (**b**) SiC MOSFET (STMicroelectronics SCTH35N65G2V7) [51]; (**c**) GaN HEMT (Infineon IGO60R070D1) [52].

GaN HEMT has not an intrinsic body diode. When it operates in third quadrant conduction the current flows into the 2DEG channel and it is affected by V_{GS} [53,54]. For high V_{GS} (higher than V_{TH}), the first and third quadrants have similar curves. When V_{GS} decreases, towards negative values, the current curve has the characteristic shape of a diode (see Figure 7c). The lack of a parasitic body diode avoids the presence of the reverse-recovery current phenomenon. On the other hand, in GaN HEMT cascode devices, the presence of the low-voltage Si MOSFET causes the reverse recovery current.

2.6. Capacitance Characteristic

The capacitance characteristic shows the relationship between the capacitances and the drain-source voltage across the device. These capacitances evaluated in the MOSFET and GaN HEMT devices are C_{ISS} (input small-signal capacitance), C_{RSS} (reverse small-signal capacitance) and C_{OSS} (output small-signal capacitance). The equations of parasitic capacitances are shown in the following:

$$\begin{aligned} C_{ISS} &= C_{GD} + C_{GS} \\ C_{RSS} &= C_{GD} \\ C_{OSS} &= C_{GD} + C_{DS} \end{aligned} \tag{1}$$

They are non-linear and "small signal" capacitances that influence the dynamic behaviour of a device. These capacitances are provided in the datasheet as curves depending on V_{DS} in the range $0 \div 500$ V (see Figure 8). The capacitances also depend on the size of the device, the capacitance values of the MOSFETs are about double those of the GaN HEMTs with the same V_{DS}. The Si MOSFET based on Super-Junction technology presents a constant C_{ISS} and a strong variation of C_{OSS} and C_{RSS}, at low V_{DS}. A similar trend occurs in SiC MOSFETs, although the capacitance values, as well as their sweep, are less than in Si MOSFETs. Analogous considerations can be applied, in turn, to GaN HEMT, even if it presents lower capacitance values and lower capacitance sweep. In conclusion, although the capacitance values are different among the three technologies, the trend is quite similar.

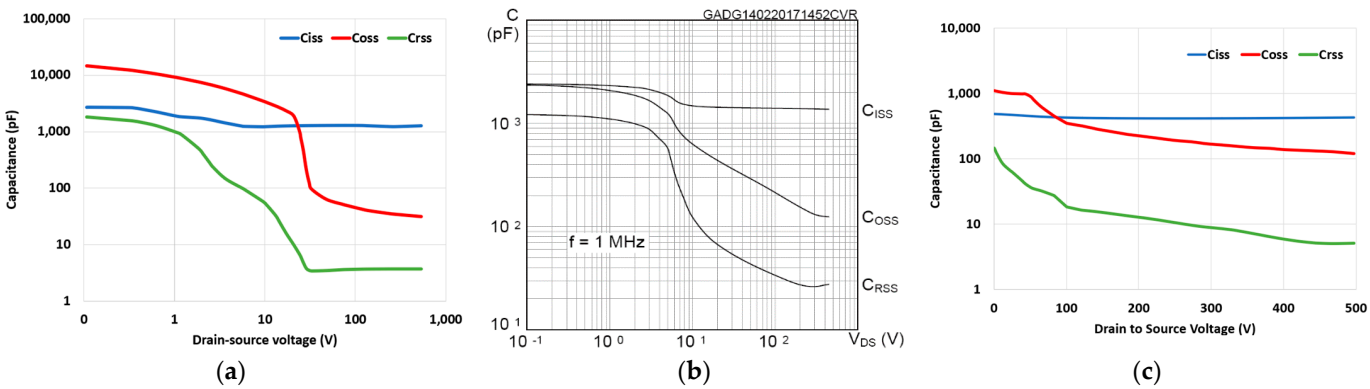


Figure 8. The Capacitance variations: (**a**) Si MOSFET (Toshiba TK14G65W) [55]; (**b**) SiC MOSFET (STMicroelectronics SCTL35N65G2V) [36]; (**c**) GaN HEMT (GaNPower GPI65060DFN) [56].

Figure 9 shows the capacitances of the GaN HEMT cascode device and shows that, compared to other GaN HEMT devices, they have higher values due to the embedded Si MOSFET.

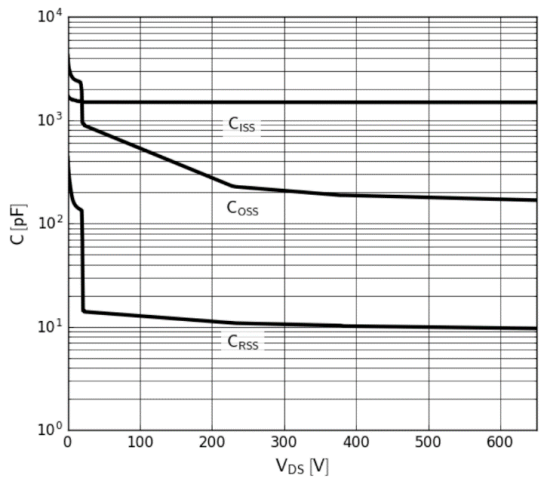


Figure 9. The capacitance of GaN HEMT cascode (Transphorm TP65H035WS) [57].

3. Circuit Model

Circuit models are widely used in academia and industry to design power converters and foresee their performance. The models use mathematical expressions to emulate the behaviour of the device. Some circuit models do not present any relation with the device physics (behavioural models), others include some device physical parameters in the mathematical expressions (semi-physics and physics models). Behavioural models use mathematical expressions whose fitting parameters (i.e., coefficients, exponents and so on) are appropriately set to emulate the datasheet quantities described in Section 2. Semi-physics models use physics quantities related to the device in combination with the aforesaid parameters. Finally, physics models adopt only equations and quantities strictly related to device physics. Behavioural and semi-physics models are quite accurate and enable fast simulations and development times. These two important features make them the most diffused ones. Therefore, only these kinds of the model are analysed in the following, and thus the considered circuit models are behavioural or semi-physics ones. Furthermore, in the semi-physical models of MOSFETs when they are adapted to GaN HEMTs, the semi-physical parameters become fitting parameters for GaN HEMTs. This is because the physical structure between MOSFET and GaN HEMT is different, so there is no correspondence for the semi-physical parameters. Any circuit model includes various blocks to emulate the static and dynamic behaviour of a device. Figure 10 shows

the different blocks usually present in the circuit models of MOSFETs (Figure 10a,b) and GaN HEMTs (Figure 10c,d).

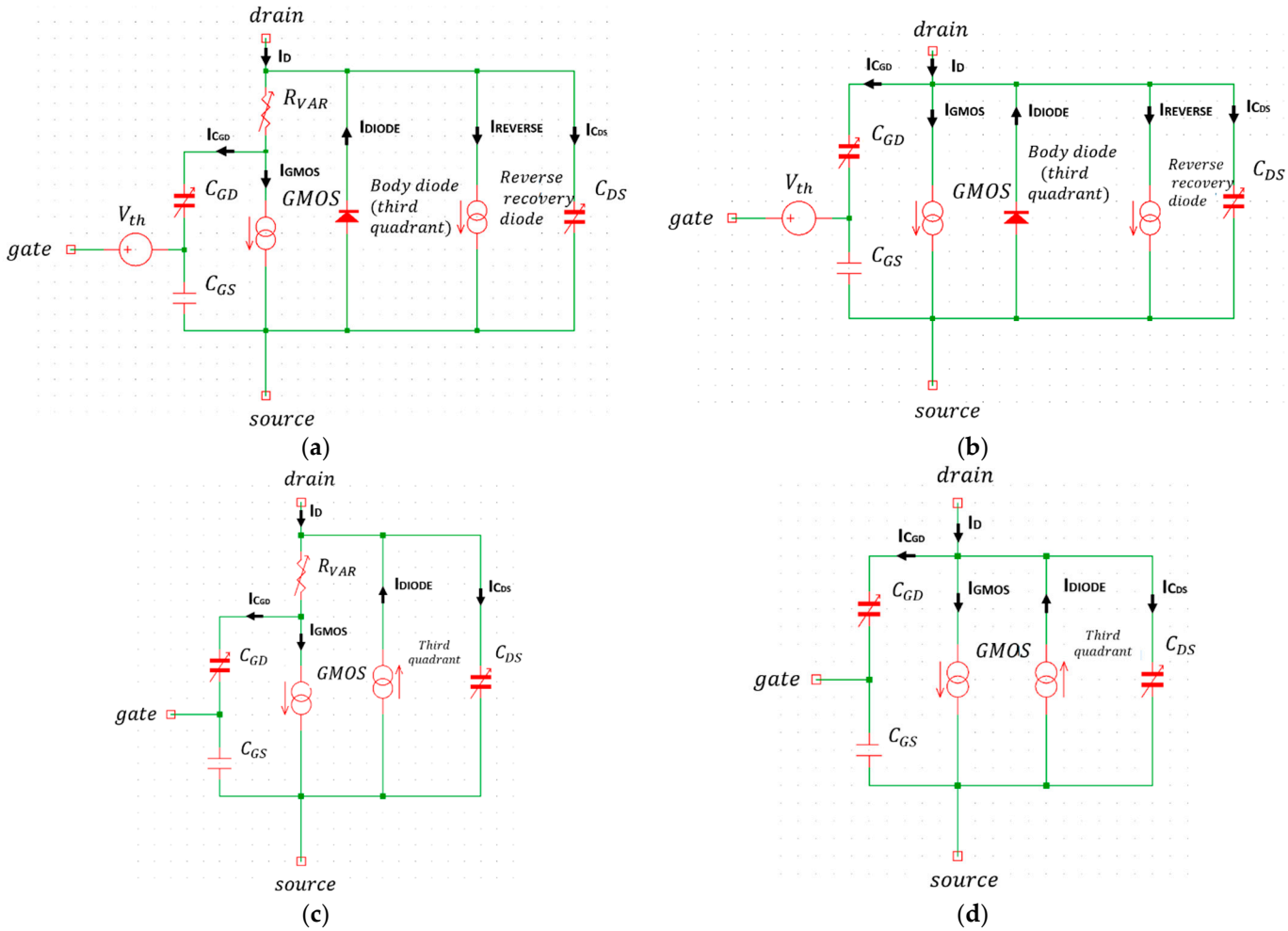


Figure 10. Generic behavioural models of power devices where, usually, the GMOS block mainly emulates the output and transfer characteristics; the Vth and the R_{VAR} block emulate the variation of, respectively, the threshold voltage and the conduction resistance with temperature; the third quadrant block emulates the reverse conduction; the reverse recovery diode block emulates the reverse recovery current; C_{GS}, C_{GD} and C_{DS} emulate the parasitic capacitances: (**a**) MOSFET with R_{VAR}; (**b**) MOSFET without R_{VAR}; (**c**) GaN HEMT with R_{VAR}; (**d**) GaN HEMT without R_{VAR}.

The GMOS block enables us to emulate the output and transfer characteristics that represent the static behaviour of the device. In the MOSFET model, block Vth emulates the dependence of the voltage threshold from the temperature, and it is used in combination with the GMOS block. When R_{VAR} is considered (Figure 10a,c), it usually emulates the variation of the conduction resistance with the temperature, and it also affects the static behaviour of the model. Another static characteristic, the third quadrant curves related to the parasitic diode conduction, is emulated by the body diode and GMOS blocks in MOSFET, and a similar block is employed in GaN HEMT. Moreover, in the MOSFET, the reverse recovery diode block emulates the reverse recovery current of this parasitic diode, thus affecting the dynamic behaviour of the device.

In the same way, the blocks C_{GD} (gate-drain capacitance), C_{DS} (drain-source capacitance) and C_{GS} (gate-source capacitance) model the capacitance characteristics both in MOSFET and GaN HEMT devices, thus enabling to account for the dynamic behaviour, such as the gate charge and the switching waveforms.

Finally, as mentioned in Section 2, the Vth and the reverse recovery diode blocks, existing only in the MOSFET model, must be considered in the cascade GaN HEMTs.

Many approaches can be used to implement each block. Therefore, in the following, these approaches are analysed to highlight those useful for the GaN HEMT modelling, taking into account the comparison reported in Section 2. For each block, the equations proposed in the literature (the papers have been collected by Scopus) and the ones developed by some semiconductor manufacturers are reported [58].

In the following equations, physical quantities are explained the first time they appear. Moreover, all quantities are listed in Abbreviation.

3.1. GMOS

The GMOS block is implemented through a controlled current source that sets the drain current of the device in the first-quadrant operation, by implementing non-linear equations that impose the shape of the drain current. These equations include some parameters whose value must be determined appropriately to fit the simulation curves that emulate the output and transfer characteristics.

As said in the introduction of this section, some models include physical quantities in the equations and are identified as semi-physics models. Among the best known for the GMOS block are the Shichman–Hodges model, the Enz–Krummenacher–Vittoz (EKV) model, the Angelov model and the Curtice–Etterberg model, which are discussed in the following.

In 1968, the Shichman–Hodges equation was developed [59,60]. This MOSFET model is usually known as MOSFET LEVEL 1 [61], which includes the channel length modulation:

$$\mathrm{I_{GMOS}} = K_n \frac{W}{L} \begin{cases} 0 & \mathrm{V_{DS}} < 0 \\ \left[[\mathrm{V_{GS}} - \mathrm{V_{TH}}]\mathrm{V_{DS}} - \frac{\mathrm{V_{DS}^2}}{2} \right] [1 + \lambda \mathrm{V_{DS}}] & 0 < \mathrm{V_{DS}} < \mathrm{V_{GS}} - \mathrm{V_{TH}} \\ \frac{[\mathrm{V_{GS}} - \mathrm{V_{TH}}]^2}{2} [1 + \lambda \mathrm{V_{DS}}] & \mathrm{V_{DS}} > \mathrm{V_{GS}} - \mathrm{V_{TH}} \end{cases} \quad (2)$$

where K_n is the transconductance coefficient, W is the channel width, L is the channel length, $\mathrm{V_{TH}}$ is the threshold voltage (see Section 3.2) and λ is the channel length modulation coefficient. The equation is implemented into a current source that emulates the three operational regions (cut-off, linear and saturation) by the three distinct equations that appear in Equation (2). In [61], Equation (2) is used for modelling the output characteristic of GaN HEMT.

MOSFET LEVEL 3 is a more complex model that describes the MOSFET behaviour more accurately than the standard MOSFET LEVEL 1 [62]:

$$\mathrm{I_{GMOS}} = \begin{cases} \frac{K_n}{1+\theta(\mathrm{V_{GS}}-\mathrm{V_{TH}})} \frac{W}{L} (\mathrm{V_{GS}} - \mathrm{V_{TH}})(\mathrm{V_{DS}} - Rs\, \mathrm{I}_{GMOS} - Rd\, \mathrm{I_{GMOS}}) - \left[1 + \frac{\gamma}{2\sqrt{\varphi}}\right] \frac{(\mathrm{V_{DS}} - Rs\, \mathrm{I_{GMOS}} - Rd\, \mathrm{I_{GMOS}})^2}{2} & \text{Triode region} \\ \frac{K_n}{1+\theta(\mathrm{V_{GS}}-\mathrm{V_{TH}})} \frac{W}{L} (\mathrm{V_{GS}} - \mathrm{V_{TH}})^2 \left[\frac{2\sqrt{\varphi}}{2(2\sqrt{\varphi}+\gamma)}\right] & \text{Saturation region} \end{cases} \quad (3)$$

where θ is the mobility modulation constant, Rs is the source resistance, Rd is the drain resistance, φ is the surface potential in strong inversion, γ is the body-effect parameter. Furthermore, these equations are adaptable to GaN HEMT device models as proved in the following. These equations have been used to emulate the behaviour of two GaN HEMTs devices developed by GaNSystem (GS66504B and GS66506T).

In Figure 11, the simulation results obtained by using the parameters values of the MOSFET LEVEL 3, in [62], are almost good. The comparison highlights a discrete ability of the MOSFET LEVEL 3 to be used for the behavioural models of GaN HEMT devices.

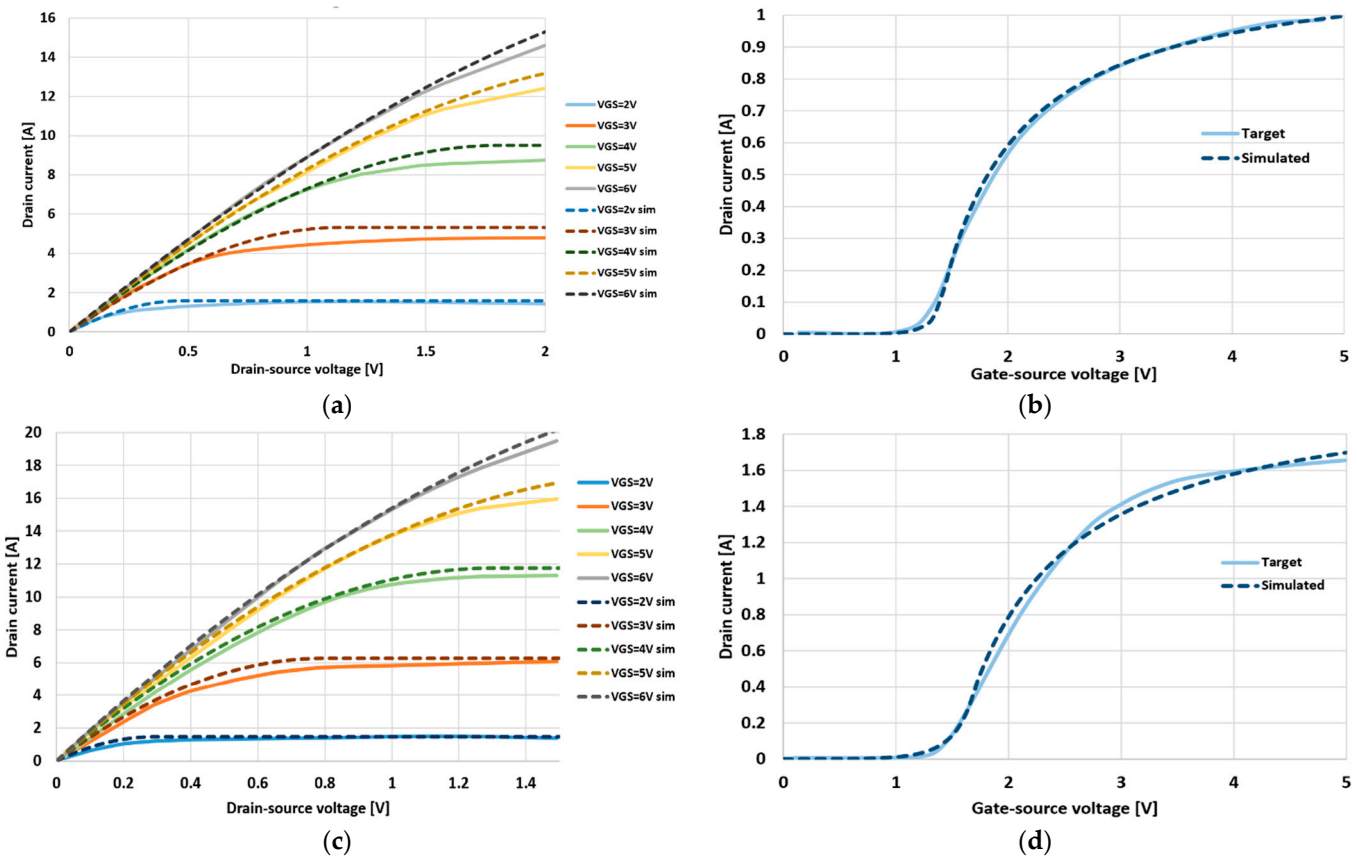


Figure 11. Comparison between target curves (solid lines) and simulated curves (dashed lines): (**a**) output characteristic of GS66504B [63]; (**b**) transfer characteristic of GS66504B [63]; (**c**) output characteristic of GS66506T [64]; (**d**) transfer characteristic of GS66506T [64].

Some quantities depend on the temperature, but such dependence is not accounted for in the previous models. For this reason, in [58], a new model that accounts for the dependence of the current I_D on the temperature variation has been proposed. Indeed, the model is based on MOSFET LEVEL 1:

$$I_{GMOS} = \begin{cases} \frac{W}{L} V_{DS}[1+\lambda V_{DS}]\left[V_{GS} - V_{TH} - \frac{V_{DS}}{2}\frac{V_{lin}}{KP_{sat}}\right]V_{lin} & V_{DS} < [V_{GS} - V_{TH}]\frac{KP_{sat}}{V_{lin}} \\ \frac{W}{L} V_{DS}[1+\lambda V_{DS}][V_{GS} - V_{TH}]^2 KP_{sat} & V_{DS} > [V_{GS} - V_{TH}]\frac{KP_{sat}}{V_{lin}} \end{cases} \quad (4)$$

where two temperature-dependent coefficients V_{lin} and KP_{sat} are added to improve Equation (2); V_{lin} values are tabled, while KP_{sat} is expressed as functions of the junction temperature T_j:

$$KP_{sat} = KP_{sat0}\left[\frac{T_j + 273}{300}\right]^{K_{sat}}$$

where KP_{sat0} and K_{sat} are fitting parameters.

At room temperature, the accuracy increases with increasing V_{GS}. High accuracy is achieved at high temperatures for all V_{GS} [65].

Another I_D-temperature dependence of Equation (2) (MOSFET LEVEL 1) has been created in [66]:

$$I_{GMOS} = K_n \frac{W}{L} \begin{cases} 0 & V_{DS} < 0 \\ \left[[V_{GS} - V_{TH}]V_{GMOS} - \frac{V_{GMOS}^2}{2}\right][1+\lambda V_{GMOS}] & 0 < V_{DS} < V_{GS} - V_{TH} \\ \frac{[V_{GS} - V_{TH}]^2}{2}[1+\lambda V_{GMOS}] & V_{DS} > V_{GS} - V_{TH} \end{cases} \quad (5)$$

where

$$V_{GMOS} = V_{DS} - R_{D1}\, I_{GMOS}$$

and

$$K_n = K_{n1} + K_{n2}[V_{GS} - 10]$$
$$K_{n1} = A\, T_j + B$$
$$K_{n2} = -C\, T_j + D$$
$$V_{TH} = -E\, T_j + F$$
$$R_{D1} = G\, T_j^2 + H\, T_j + I$$

where *A*-*I* are fitting parameters. In [66], *W* and *L* have been set equal to 1. When these fitting parameters are added, the model is not semi-physical but becomes behaviour. Excellent results are achieved both at room temperature and varying temperatures.

The need for temperature-dependent models is not the only necessity. Another request is to have a unique equation concerning the Shichman–Hodges model. In [67], the three operation regions can be described utilizing a single equation (based on the Shichman–Hodges equation):

$$I_{GMOS} = \frac{K_n}{2}|V_{TH}|^n \left[\frac{V_{GS}}{V_{TH}} - 1\right]^n \tanh\left(\frac{\alpha V_{DS}}{V_{GS} - V_{TH}}\right) \quad (6)$$

where n and α are fitting parameters, that modify the transition between the linear and saturation region. At low V_{DS} the hyperbolic tangent function looks like a linear function, thus emulating the linear-ohmic region. At high V_{DS}, the hyperbolic tangent tends to be one; thus, the drain current depends only on the first term.

As early as 1995, there was a need for models with a single equation dependent on temperature. Indeed, the EKV model is based on two logarithmic functions. The original EKV model [68] is reported in the following equation:

$$I_{GMOS} = 2K_n\phi_t^2 \left\{ \left[\ln\left(1 + e^{\frac{[V_{GS}-V_{TH}]}{2\phi_t}}\right)\right]^2 - \left[\ln\left(1 + e^{\frac{[V_{GS}-V_{TH}]}{2\phi_t}}\right)\right]^2 \right\} \quad (7)$$

where ϕ_t is the thermal voltage.

The aim of high accuracy has led to various models based on the EKV one. As in [69], the resulting model includes curve-fitting parameters to match the static characteristics and the effect of channel length modulation in the saturation region:

$$I_{GMOS} + I_{Diode} = 2K_n[V_{GS} - V_{TH}]\phi_t^2 k_S \left\{ \left[\ln\left(1 + e^{\frac{[V_{GS}-V_{TH}]}{2\phi_t k_S}}\right)\right]^k - \left[\ln\left(1 + e^{\frac{[V_{GS}-V_{TH}]-nV_{DS}^{\alpha}}{2\phi_t k_S}}\right)\right]^k \right\} [1 + \lambda V_{DS}] \quad (8)$$

where k_S is the sub-threshold slope, n and α are fitting parameters for the linear region. Equation (8) is valid for both first and third quadrant conduction currents and it is implemented with two opposite current sources in the GMOS block. The model accuracy increases when V_{GS} increases. In [69], simulations carried out at different temperatures are reported and they are very accurate.

The Angelov model and Curtice–Etterberg models were developed for GaAs HEMT devices between the 1980s and 1990s. Since then, these models have been used for MOSFET devices. The Angelov model proposed a hyperbolic tangent function for emulating the static behaviour of the device [70].

$$I_{GMOS} = K_n[1 + \tanh(\psi)][1 + \lambda V_{DS}]\tanh(\alpha V_{DS}) \quad (9)$$

where α is the saturation voltage parameter and the argument ψ is:

$$\psi = P_1\left[\mathrm{V_{GS}} - V_{pk}\right] + P_2\left[\mathrm{V_{GS}} - V_{pk}\right]^2 + P_3\left[\mathrm{V_{GS}} - V_{pk}\right]^3$$

where V_{pk} is the value of $\mathrm{V_{GS}}$ at which the transconductance reaches its maximum value. In [71,72], the Angelov model has been implemented in the MOSFET device. However, as this model does not emulate the temperature behaviour of the device, Equation (10) has been implemented to include temperature dependence.

$$X_T = X_{T25}\left[1 + X_{Tj}\left[T_j - T_{25}\right]\right] \tag{10}$$

where T_{25} is the room temperature, X_T is a generic parameter temperature-dependent. Moreover, to improve the accuracy of the model, some parameters vary with $\mathrm{V_{GS}}$: $\alpha(\mathrm{V_{GS}})$, $K_n(\mathrm{V_{GS}})$ and $\lambda(\mathrm{V_{GS}})$.

The demand for ever more accurate models has led to the creation of new complex equations, based on the Angelov model. The one, proposed in [73], aims at improving the model in the High Voltage High Current region:

$$\mathrm{I_{GMOS}} = 0.5\left[I_{dsp} - I_{dsn}\right] \tag{11}$$

where

$$I_{dsp} = A\ g_1\ [1 + f_1][1 + g_3 f_2 + B\ g_4]$$
$$I_{dsn} = A\ g_1\ [1 + f_1][1 + g_3 f_2 + B\ g_4]$$

and

$$g_1 = 1 + \tanh(0.5[\mathrm{e}^{g_2} - \mathrm{e}^{-g_2}])$$
$$g_2 = C_1\left[\mathrm{V_{GS}} - f_3 + C_2\ [\mathrm{V_{GS}} - f_3]^2 + C_3\ [\mathrm{V_{GS}} - f_3]^3\right]$$
$$g_3 = G_1 + G_2\ g_1$$
$$g_4 = \mathrm{e}^{J[\mathrm{V_{GS}} - K]}$$
$$f_1 = \tanh([E + F\ g_1]\mathrm{V_{DS}})$$
$$f_2 = \tanh([H_1\ \tanh(1 + H_2\ \mathrm{V_{GS}})]\mathrm{V_{DS}})$$
$$f_3 = D - L + L\ \tanh(F\ \mathrm{V_{DS}}) - M[\mathrm{V_{DG}} - K]^2$$

In the previous equations, A, B, C_1, C_2, C_3, D, E, F, G_1, G_2, H_1, H_2, J, K, L, and M are fitting parameters. The presence of many fitting parameters allows the high level of accuracy of the model, but the evaluation of their optimal value is complicated and time-consuming. Hence, the use of an automatic tool for the optimal setting of these parameters is recommended [34].

Instead, the equation of the original Curtice–Etterberg FET model [74] is reported in the following:

$$I_{DS} = \left[A_0 + A_1 V_1 + A_2 {V_1}^2 + A_3 {V_1}^3\right]\tanh(\gamma V_{out}(t)) \tag{12}$$

where

$$V_1 = V_{in}(t - \tau)\left[1 + \beta\left[V_{out}^0 - V_{out}(t)\right]\right]$$

where γ is a fitting parameter that allows the modify the output curves in the ohmic region, β is the fitting parameter for pinch-off, V_{out}^0 is the output voltage at which A_0, A_1, A_2 and A_3 are evaluated, and τ is the internal time delay of FET.

In [75], a model based on the Curtice one for SiC MOSFET:

$$\mathrm{I_{GMOS}} = b\left[1 + \lambda'\right]\tanh(a\mathrm{V_{DS}})\left[\left[1 + \lambda'\right]^{-1} + \left[1 - \left[1 + \lambda'\right]^{-1}\right]\left[1 - \mathrm{e}^{\left[-\frac{\mathrm{V_{DS}}}{\mathrm{V_T}}\right]}\right]\right] \tag{13}$$

where λ, λ', $\mathrm{V_T}$, a and b are fitting parameters.

Another model based on the Curtice–Etterberg FET model is reported in [76], where accurate characteristics are obtained over a wide temperature range by using the following new equation, depending on V_{DS} and V_{GS}:

$$I_{GMOS} = \frac{H_t V_{GS}^{2B_t}}{\left[V_{GS}^{2C} + e^{2C}\right]^{\frac{B_t}{C}}} \tanh\left(A_d V_{DS}^{k_d}\right)[1 + \lambda[V_{DS} - V_{DS,tr}]] \tag{14}$$

where

$$B_t = B_0 + \alpha_B\left[T_j - T_{25}\right]$$
$$H_t = H_0 + \alpha_H\left[T_j - T_{25}\right]$$
$$A_d = A_g\left[T_j\, V_{GS}^{k_g}\right]$$
$$A_g = A_{g0} + \alpha_{A1}\left[T_j - T_{25}\right] + \alpha_{A2}\left[T_j - T_{25}\right]^2$$
$$k_g = k_{g0} + \alpha_{k1}\left[T_j - T_{25}\right] + \alpha_{k2}\left[T_j - T_{25}\right]^2$$

In the previous equations, C, k_d, B_t, B_0, H_0, α_B, α_H, α_{A1}, α_{A2}, α_{k1}, α_{k2}, A_{g0} and k_{g0} are fitting parameters and $V_{DS,tr}$ is the V_{DS} voltage at which the transfer is measured in the datasheet. In Equation (14), a product of three terms appears. The first term is inspired by the model of the C3M device developed by Cree [58]. The second and third terms are based on the Curtice–Etterberg model. In the original Curtice–Etterberg model, the temperature dependence is not present, but this model includes temperature dependence using the two second-degree polynomial functions Ag and kg. In [76], the validation of the model has been carried out for different SiC MOSFETs from various manufacturers at different temperatures (25 °C and 150 °C), and the results are very accurate for all tested devices.

In [58], another temperature-dependent model based on the Curtice–Etterberg model is proposed. The GMOS equation proposed:

$$I_{GMOS} = \frac{k_{ah}\, V_{GS}{}^{k_{ae}+a}}{\left[V_{GS}^{2b} + e^{2c}\right]^{d}\left[V_{GS}^{2k_{af}} + e^{2k_{af}k_{ag}}\right]^{\frac{K_{ae}}{2K_{af}}}} \tanh(\gamma V_{DS})[1 + \lambda V_{DS}] \tag{15}$$

where γ, k_{ag}, a, b, c, d are fitting parameters, and k_{ah}, k_{ae}, k_{af} are temperature-dependent fitting parameters. The model accuracy improves with increasing V_{GS} [65].

Moreover, a new GMOS equation based on EKV and Curtice-Ettenberg model is proposed in [58].

$$I_{GMOS} = \frac{f_{GS}\left[1 + \left[B_1 + B_2 \tanh\left(\frac{f_{GS}}{C_1}\right)\right] \frac{e^{\frac{T_j - T_{25}}{-C_T}}}{10}\right] V_{DS}}{|V_{DS}| + \left[B_1 + B_2 \tanh\left(\frac{f_{GS}}{C_1}\right)\right] e^{\frac{T_j - T_{25}}{-C_T}}} \tag{16}$$

where

$$f_{GS} = G_1\, V_{GS}{}^{[g_t\, e^{[\frac{T_j - T_{25}}{g_1}]}\, e^{[\frac{T_j - T_{25}}{g_2}]}\, e^{[\frac{T_j - T_{25}}{g_3}]}]}$$

where B_1, B_2, C_1, C_T, G_1, g_t, g_1, g_2 and g_3 are fitting parameters. The results at 25 °C and 125 °C show that the model accuracy increases when the gate-source voltage decreases [65].

In more recent years, the need for behavioural models has arisen. This is in order not to have a dependence on the physical parameters of the device and for curves that can be modified in all their parts. The simplest behavioural models to emulate the output characteristic as in [77]:

$$I_{GMOS} = \left\{\frac{K_1}{1 + [bV_{DS}]^{C_0}} + K_2\right\}\left\{[V_{GS} - V_{TH}][bV_{DS}] - \frac{1}{2}[bV_{DS}]^2\right\} \tag{17}$$

where K_1, K_2, C_0 and b are parameters to be optimally set to emulate the characteristic accurately. This equation allows the simulation of the linear-ohmic and saturation regions. The results show an excellent accuracy of the output characteristic at low V_{DS} while the accuracy tends to decrease at high V_{DS} values.

Another behavioural temperature-independent model is proposed in [78]:

$$I_{GMOS} = AC\left[\frac{V_{GMOS}}{SS}V_{GS} + \tanh(B\,V_{GMOS})\right]\log\left(1 + C\,e^{D\,(V_{GS}-TH)}\right) \quad (18)$$

where AC, SS, B, C, D and TH are fitting parameters. Equation (18) is used for modelling GaN HEMT in [79]. In Figure 12, the output and transfer characteristics simulated with Equation (18) in a SiC MOSFET and a GaN HEMT are reported. Figure 12 highlights that Equation (18) can be valid for the GaN HEMT model with almost excellent results.

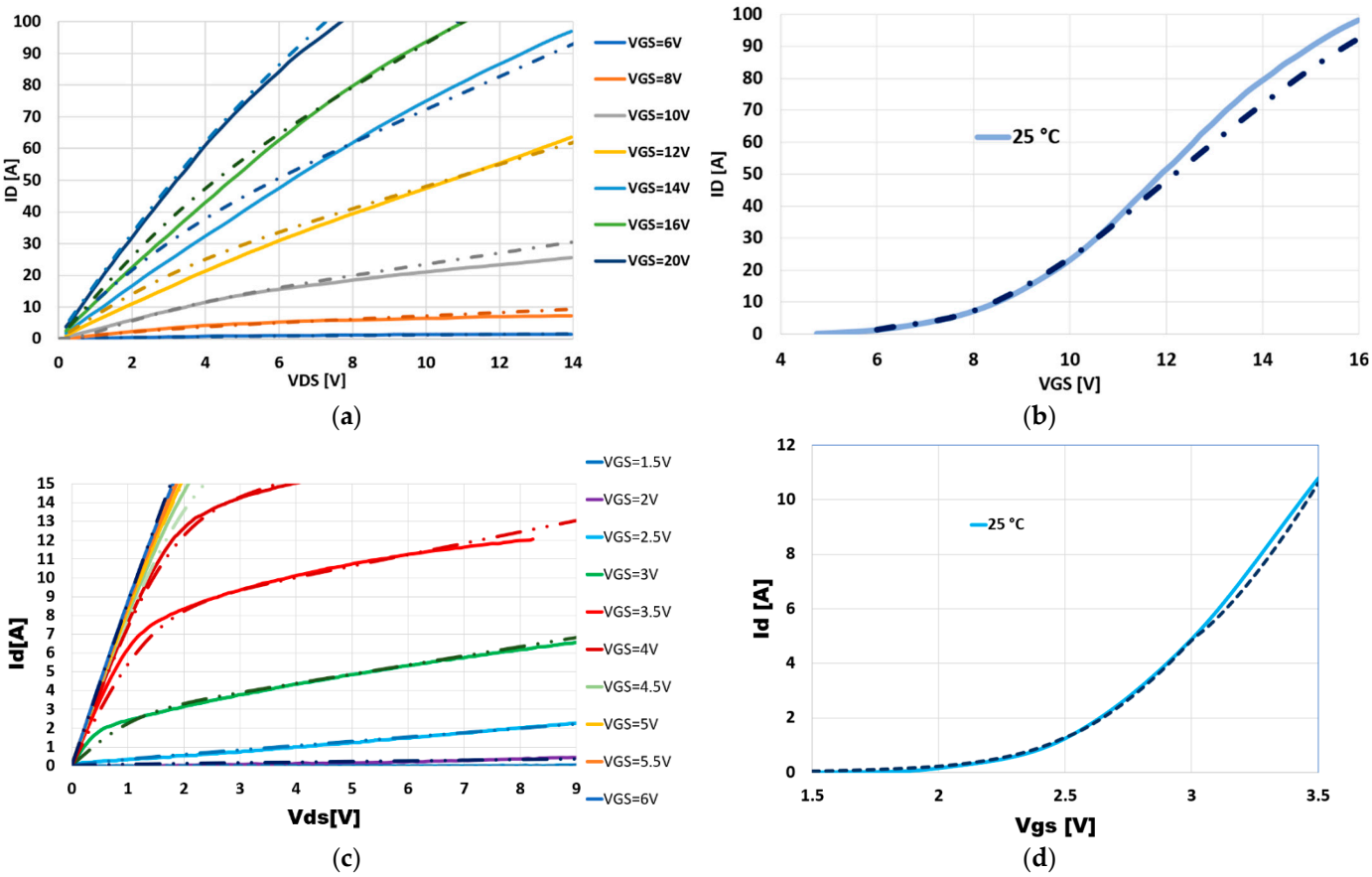


Figure 12. Comparison between target curves (solid lines) and simulated curves (dashed lines): (**a**) output characteristic of SiC MOSFET [78]; (**b**) transfer characteristic of SiC MOSFET [78]; (**c**) output characteristic of GaN HEMT [79]; (**d**) transfer characteristic of GaN HEMT [79].

The need for a temperature-dependent equation, earlier pointed out, is satisfied in [80]. The modelling approach considers the product of two mathematical equations. One equation account for the output characteristic while the other is for the transfer one. The final equation (Equation (19)) is implemented into the GMOS block:

$$I_{GMOS} = I_{GMOS,transfer}\,I_{GMOS,output} = k\left\{1 + \tanh\left[\begin{array}{c} a\,[f_{GS} + c] + \\ +b\,[f_{GS} + d^2] \end{array}\right]\right\}\frac{p\,f_{GS}\,f_{DS}}{1 + q\,f_{GS}\,f_{DS}} \quad (19)$$

where

$$f_{GS} = [m_{gs}\,\mathrm{V_{GS}} + n_{gs}]$$
$$f_{DS} = [m_{ds}\,\mathrm{V_{DS}} + n_{ds}]$$
$$m_{gs} = m_1[T_j - 25]^2 + m_2[T_j - 25] + 1$$
$$n_{gs} = n_1[T_j - 25]^2 + n_2[T_j - 25]$$
$$m_{ds} = m_3[T_j - 25]^2 + m_4[T_j - 25] + 1$$
$$n_{ds} = n_3[T_j - 25]^2 + n_4[T_j - 25]$$

The hyperbolic tangent function is used to fit the transfer characteristic. In the equation, k, a, b, c, and d are fitting parameters. While p and q are fitting parameters, but they are of the output characteristic function. $\mathrm{V_{GS}}$ and $\mathrm{V_{DS}}$ values are obtained using a quadratic function of temperature where T_j is the junction temperature, and m_1, m_2, m_3, m_4, n_1, n_2, n_3 and n_4 are the fitting parameters.

The temperature dependence can also be implemented by means of an auxiliary current source placed in parallel with a current source, that models the drain current at 25 °C. Then, the GMOS block of Figure 10 is made of two current sources in parallel [81], and the current vs. temperature dependence is emulated by the following equation:

$$\mathrm{I_{GMOS}} = \mathrm{I_{GMOS,25}} \left\{ \left[\frac{T_j + 273}{25 + 273} \right]^{TCI1} \left[1 - \left[\frac{T_j + 273}{25 + 273} \right]^{TCI2 - TCI1} \right] \right\} \tag{20}$$

where $\mathrm{I_{GMOS,25}}$ is the drain current at 25 °C emulated by the other current source, and $TCI1$ and $TCI12$ are fitting parameters. To emulate the behaviour of the SiC MOSFET current as the temperature increases, $TCI1$ must assume a positive value and $TCI2$ must be less than $TCI1$.

Another similar approach is proposed in [82]. In this case, the drain current at room temperature is multiplied by a different factor that depends on the temperature.

$$\mathrm{I_{GMOS}} = \mathrm{I_{GMOS,25}} \left[\frac{25}{T_j} \right]^K \tag{21}$$

where K is a negative fitting parameter.

Equations (20) and (21) can be used only when the models consider the range of $\mathrm{V_{GS}}$ below ZTC. Nevertheless, these equations can be used for GaN HEMT. In Equation (20), $TCI1$ must be set at a negative value and $TCI2 < TCI1$. Instead, in Equation (21), K must have a positive value.

In conclusion, the GMOS block mainly accounts for the output and transfer characteristics, and as mentioned above (Sections 2.1 and 2.2), the shape of these characteristics is quite similar for the three technologies. Therefore, the temperature-independent equations proposed for the GMOS in the circuit models of MOSFETs are valid also for GaN HEMTs by properly setting the parameters of the equation. The semi-physics models are suitable for GaN HEMT devices too. The same physical parameters used in the MOSFET model are used as fitting parameters in GaN HEMT [62]. However, when the temperature increases, the behaviour of the drain current in MOSFET and GaN HEMT is different. In GaN HEMT the drain current decreases with increasing temperature regardless of the value of $\mathrm{V_{GS}}$, while MOSFETs present this behaviour only at high $\mathrm{V_{GS}}$ values. Hence, the temperature-dependent equations used for the GMOS of the MOSFETs must be adapted for GaN HEMTs. Instead, in Equations (20) and (21), it is sufficient to change the coefficients to emulate the variation of the current as the temperature varies in the GaN HEMT. Despite that, it is possible to simplify the equations for GaN HEMT, since its temperature behaviour does not depend on $\mathrm{V_{GS}}$ values.

3.2. Vth-Threshold Voltage

This block implements the threshold voltage Vth variation with increasing temperature. The threshold voltage variation is very important because it affects the output and transfer characteristic: the term Vth is included in several equations of the GMOS block in Section 3.1.

In [82], the threshold voltage variation with temperature is modelled as a linear law:

$$\mathrm{V_{th}} = \left[\frac{T_j + 273}{25 + 273}\right]\alpha \tag{22}$$

where α is a fitting parameter. This simple implementation allows fast simulation but at the cost of inaccurate results.

Another linear equation is proposed in [83]:

$$\mathrm{V_{th}} = \mathrm{V_{TH,25}} - \rho_{TH}\left[T_j - T_{25}\right] \tag{23}$$

where $\mathrm{V_{TH,25}}$ is the threshold voltage at 25 °C, and ρ_{TH} is a fitting parameter. The results show that this equation provides a good fitting between the datasheet and target curves.

Better accuracy is achieved by implementing a third-degree polynomial function [81]:

$$\mathrm{V_{th}} = VT3\left[T_j - T_{25}\right]^3 + VT2\left[T_j - T_{25}\right]^2 + VT1\left[T_j - T_{25}\right]^1 \tag{24}$$

where $VT3$, $VT2$ and $VT1$ are fitting parameters.

Nevertheless, the threshold voltage of GaN HEMT devices is temperature independent, therefore the previous equations implemented for MOSFETs are useless for GaN HEMT devices. However, in the case of GaN HEMT cascode devices, the equations implemented in the MOSFET for modelling the $\mathrm{V_{TH}}$ variation with the temperature can be used.

3.3. R_{VAR}

This block allows emulating the $\mathrm{R_{DS,on}}$ (see Section 2.4) variation with the temperature. It is not always present in circuit models (see Figure 10). When it is used, it could interact with the GMOS block and, consequently, both of them could concur in emulating the output and transfer characteristics.

The $\mathrm{R_{VAR}}$ block of Figure 10 can be implemented either with a current-controlled voltage source (CCVS) or with a voltage-controlled current source (VCCS).

The typical trend of the $\mathrm{R_{DS,on}}$ vs. temperature curve, observed in SiC MOSFET between −50 °C and 175 °C (see Figure 6b), is called "U-shape".

This trend can be perfectly reproduced by a second-degree polynomial function as the following [81]:

$$\mathrm{R_{VAR}} = \mathrm{R_{VAR,25}}\left[1 + TC1\left[T_j - T_{25}\right] + TC2\left[T_j - T_{25}\right]^2\right] \tag{25}$$

where $\mathrm{R_{VAR,25}}$ is the typical $\mathrm{R_{DS,on}}$ value at 25 °C, and $TC1$ and $TC2$ are fitting parameters.

Another second-degree polynomial equation, in this case implemented in a VCCS, is analysed in [58]:

$$\mathrm{I_{RVAR}} = \frac{\mathrm{V_{RVAR}}}{\mathrm{R_{VAR}}} = \frac{V_{RVAR}}{A_1\, T_j^2 + A_2\, T_j + A_3 + 10^{-9}} \tag{26}$$

where A_1, A_2 and A_3 are fitting parameters.

Other implementations of the $\mathrm{R_{VAR}}$ block also include the dependence on electrical variables in addition to the temperature dependence. As in [47,83] with the following equation:

$$\mathrm{R_{VAR}} = R_{D0}\left[\frac{T_j}{T_{25}}\right]^{r_0} + R_{D1}\left[\frac{T_j}{T_{25}}\right]^{r_1}\frac{V_{RVAR}}{V_1 + V_{RVAR}}\left[\frac{V_{GS}}{V_2}\right]^{-r} \tag{27}$$

where R_{D0}, R_{D1}, V_1, V_2, r, r_0 and r_1 are fitting parameters.

Additionally, in [58], the following exponential equation, implemented in a CCVS, is analysed:

$$\mathrm{R_{VAR}} = D_1\, I_D\, \mathrm{e}^{\frac{T_j - T_{25}}{d_1}} \mathrm{e}^{\frac{T_j - T_{25}}{d_2}} + D_2\, I_D\, |I_D|^k\, \mathrm{e}^{\frac{T_j - T_{25}}{d_3}} \tag{28}$$

where D_1, D_2, d_1, d_2, d_3 and k are fitting parameters, while I_D is the drain current. Equations (24) and (25) allow us to achieve satisfactory results but with a higher mathematical complexity [65]. If only the operating temperature range between 25 °C and 175 °C is considered to model the $\mathrm{R_{VAR}}$ block for the SiC MOSFET, equations can be simplified, because in this temperature range, the trend of the curve is an increasing monotone function. For example, in [84], the following equation is proposed:

$$\mathrm{R_{VAR}} = \mathrm{R_{VAR,25}} \left[1 + \frac{k_r}{100}\right]^{T_j - T_{25}} \tag{29}$$

where k_r is a fitting parameter.

This approach is useful for modelling the same block for the GaN HEMTs since a monotonous increase in $\mathrm{R_{DS,on}}$ with increasing temperature is observed (see Figure 6c).

Some circuit models are able to account for $\mathrm{R_{DS,on}}$ temperature curve without using the $\mathrm{R_{VAR}}$ block (as in Figure 10b,d). In this case, the curve emulation is obtained through the GMOS equation [72]. The polynomial equations, developed for the GMOS block, consider the variation of on-state resistance with temperature.

In conclusion, the previous equations have been developed to reproduce the "U-shape" curve of SiC MOSFET in a temperature range between −50 °C and 175 °C. As highlighted in Section 2.4, the on-resistance curve above 25 °C is similar for the Si, SiC MOSFETs and GaN HEMT. Therefore, the $\mathrm{R_{VAR}}$ equations for SiC MOSFET can be used for Si MOSFET and GaN HEMT only in a temperature range between 25 °C and 175 °C. However, Equation (29) can be used for the GaN HEMT in the temperature range between −50 °C and 150 °C because it is an increasing monotone function.

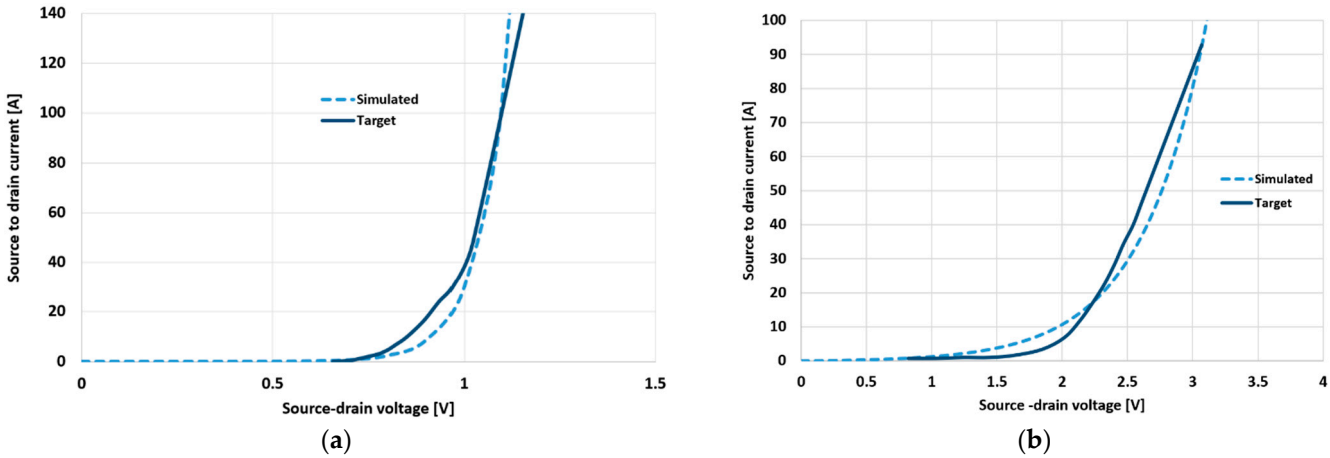
3.4. Third Quadrant Conduction

The third quadrant characteristic is enabled when the $\mathrm{V_{DS}}$, across the device, is negative. As explained in Section 2.5, the third quadrant current is simulated at negative and positive $\mathrm{V_{GS}}$. In several cases, the GMOS and body diode blocks cooperate to emulate the current in the third quadrant.

A first implementation of the body diode block in the MOSFET model could be achieved by means of the Shockley diode equation [85]:

$$\mathrm{I_{Diode}} = \begin{cases} 0 & \mathrm{V_{Diode}} < 0 \\ I_{sb}\left[\mathrm{e}^{k_{tb}\mathrm{V_{Diode}}} - 1\right] & \mathrm{V_{Diode}} > 0 \end{cases} \tag{30}$$

where $\mathrm{V_{Diode}}$ is the voltage across the diode, and I_{sb} and k_{tb} are fitting parameters. The previous equation has been tested for a MOSFET device and a GaN HEMT. The simulations are shown in Figure 13.



(**a**) (**b**)

Figure 13. Comparison of third quadrant behaviour between target curves (solid lines) and simulated curves (dashed lines): (**a**) Si MOSFET (Infineon IPP60R099C6) [86]; (**b**) GaN HEMT (EPC EPC2001) [87].

The results, shown in Figure 13, confirm that the models used for the MOSFET devices are adaptable to the GaN HEMT models with almost satisfying results.

However, the lack of dependence on the temperature is the main limit of this equation. To overcome this limitation a new equation has been proposed equation in [66]:

$$\mathrm{I_{Diode}} = \mathrm{I_{S,25}}\left[\mathrm{e}^{\frac{q\,\mathrm{V_{Diode}}}{kT_j}} - 1\right] \tag{31}$$

where $\mathrm{I_{S,25}}$ is the saturation current at 25 °C, q is the electron charge, k is the Boltzmann's constant. This equation is implemented in the body diode block, which is placed in parallel with the $\mathrm{C_{DS}}$ block, and they are in series with the diode resistance (see Figure 14a).

To improve the accuracy of the temperature-dependent models, in [80], the resistance of the diode is also modelled:

$$\mathrm{I_{Diode}} = \mathrm{I_S}\left[\mathrm{e}^{\frac{q[\mathrm{V_{Diode}} - \mathrm{I_{Diode}} R_{S,T}]}{NkT}} - 1\right] \tag{32}$$

where

$$\mathrm{I_S} = \mathrm{I_{S,25}}\,\mathrm{e}^{\left[\frac{\left[\frac{T_j}{T_{25}} - 1\right] V_{EG}\, q}{NkT_j}\right]} \left[\frac{T_j}{T_{25}}\right]^{\frac{X_{TI}}{N}}$$

$$\mathrm{R_{diode}} = \mathrm{R_{diode,25}}\left[1 + T_{RS1}\left[T_j - T_{25}\right] + T_{RS2}\left[T_j - T_{25}\right]^2\right]$$

and N is the emission coefficient, $\mathrm{I_s}$ the saturation current, $\mathrm{R_{diode}}$ is the parasitic resistance of the diode, $\mathrm{R_{diode,25}}$ is the parasitic resistance of the diode at 25 °C, V_{EG} is the bandgap voltage, X_{TI} is a fitting parameter temperature-dependent, T_{RS1} and T_{RS2} are fitting parameters temperature independent. The model provides accurate results at −40 °C, 25 °C and 150 °C.

In recent years, the need has arisen to have behavioural models of the body diode. These models are temperature dependent, and they include the resistance of the diode too. In the following, these models are reported in order of complexity of their equations.

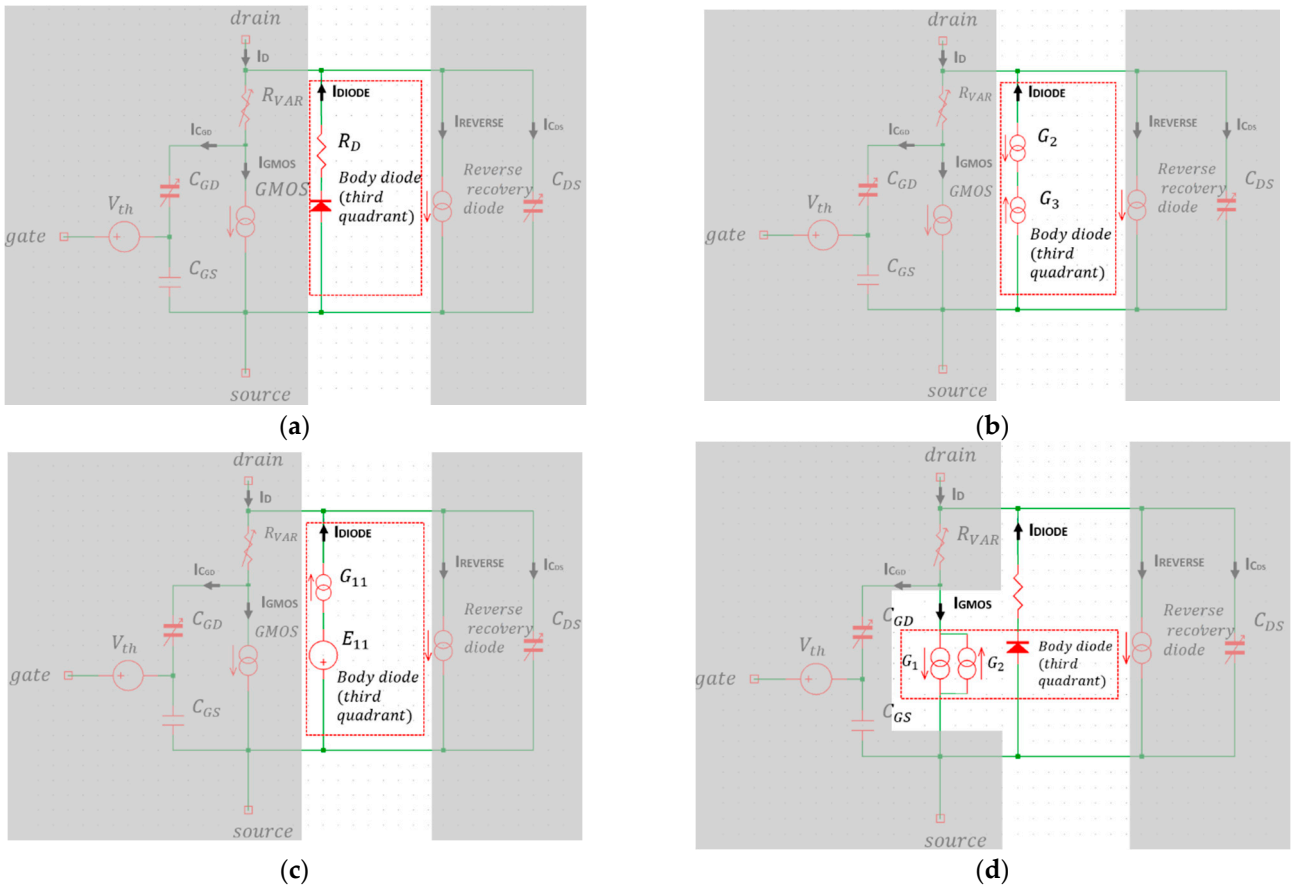


Figure 14. Various body diode and third quadrant implementations: (**a**) body diode; (**b**) STMicroelectronics and Cree "C3M" series; (**c**) ROHM; (**d**) Cree "C2M" series.

The body diode behavioural temperature-dependent model can be obtained also employing two voltage-controlled current sources (VCCS) that represent the diode resistance and diode current behaviours, as G2 and G3 in Figure 14b. In [58], the following equations are given for the two VCCSs (see Figure 14b):

$$\begin{cases} \mathrm{I_{G2}} = \mathrm{e}^{-15+\frac{\mathrm{V_{diode}}}{a_1-a_2\ 1\mathrm{e}^{-6}\ T_j}} - B1 \\ \mathrm{I_{G3}} = \frac{\mathrm{V_{diode,resistance}}}{\mathrm{R_{Diode}}} \end{cases} \tag{33}$$

where a_1, a_2 and $B1$ are fitting parameters and:

$$\mathrm{R_{diode}} = \left[-A - B2\ \left[T_j - 25\right]\right]\ \mathrm{V_{GS}} + \left[-C - D\ \left[T_j - 25\right]\right]$$

and A, $B2$, C and D are fitting parameters. The results show that the model is very accurate at negative $\mathrm{V_{GS}}$ [65], if used together with a model of the GMOS block that also includes the third quadrant static characteristic of the drain-source current.

Another behavioural model with the equation for both the resistance of the body diode and the body diode is the following reported in [58]:

$$\begin{cases} \mathrm{I_{G3}} = \frac{\mathrm{V_{diode,resistance}}}{\alpha\left[f_{gs}\right]^2 + b\ f_{hyp}(V_{GS}) + c} \\ \mathrm{I_{G2}} = f_{sd1}{}^{f_{kbb}}\ \mathrm{e}^{f_{kaa}} \end{cases} \tag{34}$$

where *a*–*c* are temperature-dependent fitting parameters and:

$$f_{gs} = \frac{V_{GS} + \sqrt{V_{GS}^2 + 4(1e^{-6})^2}}{2}$$
$$f_{sd1} = \frac{V_{SD1} + \sqrt{V_{SD1}^2 + 4(1e^{-6})^2}}{2}$$

and f_{kbb} and f_{kaa} are functions of the gate-source voltage and temperature. V_{SD} is the source-drain voltage. With this model, good results are achieved for all V_{GS} values [65].

The block of the body diode is always in parallel to the block of the C_{DS} capacitance (see Figure 10), for this reason, it might be more effective to have a single block for both the body diode and C_{DS} as in [58]:

$$I_{diode} = A_1 \left[e^{a_1 e^{\left[\frac{T_j - T_{25}}{-b_1}\right]}} - 1 \right] e^{\left[\frac{T_j - T_{25}}{-b_2} e^{\frac{T_j - T_{25}}{-b_3}}\right]} \left[1 + e^{\left[-V_{diode} - A_2 e^{\frac{\frac{T_j - T_{25}}{b_4}}{A_3}}\right]} \right] + \\ + \frac{dV_{diode}}{dt} \left[B_1 [V_{diode} - B_2] + B_3 \left[1 - c_1 \frac{\tanh\left(\frac{V_{diode}}{c_1}\right)}{c_2} \right]^{-C_3} \right] \quad (35)$$

where A_1, A_2, A_3, B_1, B_2, B_3, a_1, b_1, b_2, b_3, b_4, c_1, c_2 and c_3 are fitting parameters. The voltage derivative term in Equation (35) allows modelling the parasitic C_{DS} capacitance by including it into the body diode VCCS (G11 in Figure 14c). In this case, the resistance of the diode is modelled by a current-controlled voltage source (E11 in Figure 14c), whose equation is:

$$V_{diode,resistance} = A \sinh^{-1}\left(\frac{I_{diode,resistance}}{B}\right) + C\, I_{diode,resistance} \quad (36)$$

where *A*, *B* and *C* are fitting parameters.

In the semi-physics EKV model of the GMOS block defined by Equation (8) (see Section 3.1), the emulation of the third quadrant current for positive V_{GS} is included, through the combination of G1 and G2 (see Figure 14d). In this case, the body diode is modelled through a SPICE diode with custom parameters to match the SiC MOSFET device [69].

The behaviour in the third quadrant is similar for all three technologies. Therefore, all the previous models, regardless of whether they use the Shockley diode equation or its modifications, are useful for modelling the third quadrant operations of GaN HEMTs. Reverse recovery current is a feature only of MOSFET; thus, its modelling is not useful for GaN HEMT circuit models, except for GaN HEMT cascode devices where there is a Si MOSFET.

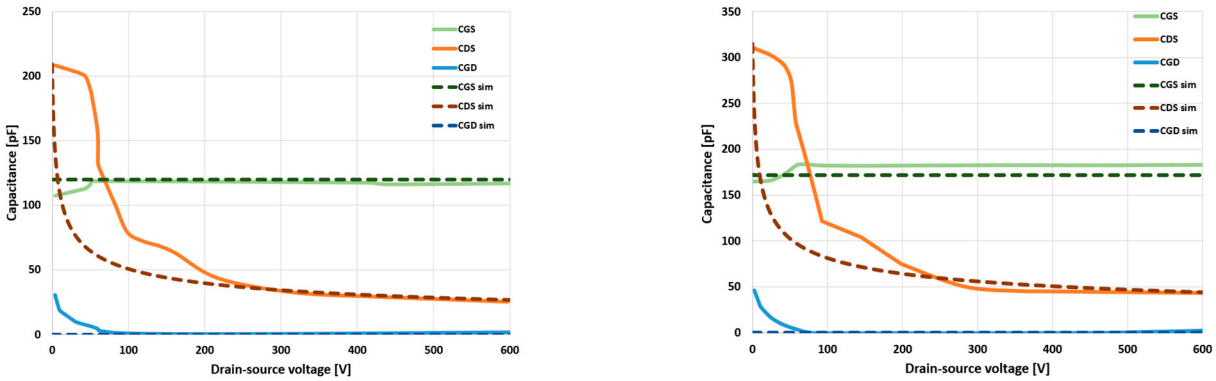
3.5. Parasitic Capacitances

As shown in Section 2.6, the capacitances of a device vary with the drain-source voltage variation. The values C_{GD}, C_{DS} strongly varies at varying this voltage, while the variation of C_{GS} is usually negligible. Hence, when the C_{GS} is not mentioned, it is implemented as a fixed capacitance. An accurate capacitance model is necessary to obtain proper dynamic simulations. More models propose a behavioural approach rather than the semi-physics or physical ones.

The standard approach for modelling the capacitance consists of the use of the junction capacitance equations. In [62,66,72,88] and [89], C_{DS} is described through Equation (37) as described in the MOSFET LEVEL 1 and LEVEL3 [60,62].

$$C_{DS} = C_{DS}(0) \left[1 + \frac{V_{DS}}{V_{bi}} \right]^{-M} \quad (37)$$

where $C_{DS}(0)$ is the zero-bias drain-source capacitance, V_{bi} is the built-in junction potential and M is the p-n gradient factor, and it can be used as a fitting parameter. The previous equation can be adapted to the GaN HEMT model. To demonstrate this, in paper [62], Equation (37) has been used to model the C_{DS} capacitance. As shown in Figure 15, the results are satisfactory at higher voltages. At low voltages, the model could be improved by adding a flat zone to simulate C_{DS}. This means that the LEVEL 1 MOSFET model does not perform well for GaN HEMTs without changes.



(**a**) (**b**)

Figure 15. Comparison between target curves (solid lines) and simulated curves (dashed lines): (**a**) capacitance characteristic of GS66504B; (**b**) capacitance characteristic of GS66504B.

Additionally, in [61], the capacitance behaviours of a GaN HEMT have been emulated through the MOSFET LEVEL 1. However, the MOSFET LEVEL 1 model does not present a satisfactory result for modelling GaN HEMTs.

To increase the accuracy of the model, other fitting parameters can be added as in [69]:

$$C_{DS} = C_{J0}\left[1 + \frac{V_{DS}}{V_{bi}}\right]^{-M} + C_{\infty} \tag{38}$$

In this case, C_{J0} and C_{∞} are fitting parameters.

The previous equation usually modelled the C_{DS} capacitance, but they can lead the way for modelling C_{GD}. Indeed, in [66], a function based on the junction equation is used to model the C_{GD} capacitance. The equation has been modified to increase its accuracy:

$$C_{GD} = \frac{C_{GD}(0)}{\left[1 + V_{DG}\left[1 + k_1 \frac{1+\tanh(k_2[V_{DG}-V_{TH}])}{2}\right]\right]^{M}} \tag{39}$$

where k_1, k_2 are fitting parameters and V_{GD} is the gate-drain voltage. The results have been evaluated by simulating the C_{ISS}, C_{OSS} and C_{RSS} capacitance and they show high accuracy results.

Another approach using the junction capacitance equations is reported in [90]. Equation (40) is the evolution of the equation of Equation (37). It arises from the need to improve the dynamic behaviour of an already known model (Shichman–Hodges or MOSFET LEVEL 1). For this reason, a modification of the Shichman–Hodges model is proposed:

$$\begin{aligned} C_{GS} &= \begin{cases} C_{GS}(0)\left[1 - \frac{V_{GS}}{PBCGS}\right]^{-MGS} & V_{GS} < F_{C1}\,PBCGS \\ C_{GS}(0)[1-F_{C1}]^{-[1+MGS]}\left[1 - F_{C1}[1+MGS] + MGS\,\frac{V_{GS}}{PBCGS}\right] & V_{GS} > F_{C1}\,PBCGS \end{cases} \\ C_{GD} &= \begin{cases} C_{GS}(0)\left[1 - \frac{V_{GD}}{PBCGS}\right]^{-MGD} & V_{GD} < F_{C1}\,PBCGD \\ C_{GS}(0)[1-F_{C2}]^{-[1+MGD]}\left[1 - F_{C2}[1+MGD] + MGD\,\frac{V_{GD}}{PBCGD}\right] & V_{GD} > F_{C1}\,PBCGD \end{cases} \end{aligned} \tag{40}$$

where F_{C1}, $PBCGS$, MGS, F_{C2}, $PBCGD$, MGD are a new set of model parameters. The improvement in the results achieved with the modification of the Shichman–Hodges model with respect to the original model is remarkable.

Differently from those above, the following models use a behavioural approach with physical parameters that have been devised to improve the accuracy of capacitance. These models are classified as semi-physics models.

An innovative equation that describes C_{GD} and C_{DS} variations is reported [91]:

$$\begin{aligned} C_{GD} &= [C_{GD}(0) - C_{GDMIN}]\left[1 + \tfrac{2}{\pi}\arctan\left(\tfrac{V_{GD}}{V^*_{GD}}\right)\right] \\ C_{DS} &= \frac{C_{DS}(0)\left[\frac{\pi}{2} + \arctan\left(-\frac{V_{DS}}{V^*_{DS}}\right)\right]}{\frac{\pi}{2}} + C_{DSMIN} \end{aligned} \tag{41}$$

where $C_{GD}(0)$ is the capacitance at $V_{GD} > 0$, for $V_{GD} < 0$ the C_{GD} decreases to a minimum value C_{GDMIN}. The equation for C_{DS} is valid for $V_{DS} > 0$, while for $V_{DS} < 0$ C_{DS} is constant. V^*_{GD} and V^*_{DS} are fitting parameters. The result reported in the dynamic test validation is good. To obtain more accurate models, other fitting parameters are added to Equation (41) [89]. The C_{GD} and C_{DS} equations are modelled with a hyperbolic tangent term and fitting parameters:

$$C_{GD} = C_{GD}(0)\left[1 + V_{GD}\left[1 + k_a \frac{1 + \tanh(k_b\, V_{DG} - k_c)}{2}\right]\right]^{-k_1} \tag{42}$$

where k_1, k_a, k_b, k_c are fitting parameters. The C_{GD} equation is implemented in a VCCS in series with a small resistance

In the previous models, the C_{GS} is almost always considered constant because it shows a small variation with the variation of the V_{DS} (see Section 2.6) and therefore it is modelled with a fixed capacitance. Instead, in [88], the small variation of C_{GS} is modelled with a hyperbolic-tangent-based function:

$$C_{GS} = 0.5\, C_{gsm}[1 - \tanh(V_{GS})] + C_{gsmin} \tag{43}$$

where C_{gsmin} is the gate-source capacitance when the gate drive is positive and C_{gsm} is the gate-source capacitance increment when the gate voltage is negative. Modelling C_{GS} with Equation (43) allows for achieving higher accuracies than considering it constant.

Finally, the behavioural models without any connection to the physics of the device are reported. They present an excellent alternative to the previously described models. These models can use already known mathematical equations such as the Sigmoid function or other equations built ad hoc to emulate the desired characteristics.

In [85] the C_{GD} and C_{DS} models described through the Sigmoid function are proposed:

$$\begin{aligned} C_{GD} &= \frac{a_1}{1 + e^{[-b_1[V_{GD} + c_1]]}} + d_1 \\ C_{DS} &= \frac{a_2}{1 + e^{[-b_2[V_{SD} + c_2]]}} + d_2 - \frac{a_1}{1 + e^{[-b_1[V_{GD} + c_1]]}} + d_1 \end{aligned} \tag{44}$$

where a_1, b_1, c_1, d_1, a_2, b_2, c_2, and d_2 are fitting parameters. This approach provides satisfactory results.

Instead, [89] proposes equations ad hoc by means of the tanh function to emulate the behaviour of C_{GD} and C_{DS} capacitances.

$$C_{GD} = 10^{-12}\left[[A + B]^{k_2}\, C\right] \tag{45}$$

where

$$\begin{aligned} A &= a_1[min(max(\mathrm{V_{GD}}, a_2), a_3) - a_2] \\ B &= b_1\left[1 - b_2 \tanh\left(\frac{min(\mathrm{V_{GD}}, a_2)}{b_3}\right)\right] \\ C &= c_1 \tanh([\mathrm{V_{GD}} + c_2]c_3) + c_4 \\ \mathrm{C_{DS}} &= 10^{-12}[D + E] \end{aligned} \tag{46}$$

where

$$D = d_1[max(\mathrm{V_{SD}}, d_2) - d_2]$$

$$E = e_1\left[1 - e_2 \tanh\left(\frac{min(\mathrm{V_{SD}}, e_3)}{b_4}\right)\right]^{-0.481}$$

where k_2, a_1–a_3, b_1–b_3, c_1–c_3, d_1, d_2, e_1–e_4 are fitting parameters. $\mathrm{C_{GS}}$ and $\mathrm{C_{DS}}$ equations are implemented in a VCCSs.

Another behavioural model for $\mathrm{C_{DS}}$ and $\mathrm{C_{GD}}$ is given in [92]. A composed function with the sum of a hyperbolic tangent term and an exponential one is proposed:

$$I_{Cds} = \frac{\mathrm{dV_{DS}}}{\mathrm{dt}} f_{\mathrm{C}} \tag{47}$$

where

$$f_{\mathrm{C}} = \sum\nolimits_i a_i \, \mathrm{e}^{b_i \, \mathrm{V_{DS}}} - \frac{c_i}{2}[\tanh(d_i[\mathrm{V_{DS}} - e_1\,]) - 1]$$

and a_i–e_i are fitting parameters. The comparison between simulated and target curves shows the high accuracy of this capacitance implementation.

Previous models can be implemented in current/voltage sources or variable capacitance. Instead, the following model can be implemented in current or voltage sources, but they depend on an external circuit for improving the model accuracy. In [80], $\mathrm{C_{GD}}$ is modelled by one voltage source and one reference capacitance (see Figure 16a).

$$i_{gd} = \frac{i_{ref}}{C_{ref}} = \frac{\mathrm{d}E_{gd}}{\mathrm{dV_{DG}}} \frac{\mathrm{dV_{GD}}}{\mathrm{dt}} = C_{gd} \frac{\mathrm{dV_{GD}}}{\mathrm{dt}} \tag{48}$$

where

$$E_{gd} = s_1 \, s_3 \, \ln\left(1 + \mathrm{e}^{\frac{\mathrm{V_{GD}} - s_2}{s_3}}\right) + s_4 \, s_6 \, \ln\left(1 + \mathrm{e}^{\frac{\mathrm{V_{GD}} - s_5}{s_6}}\right) + s_7 \, \mathrm{V_{GD}}$$

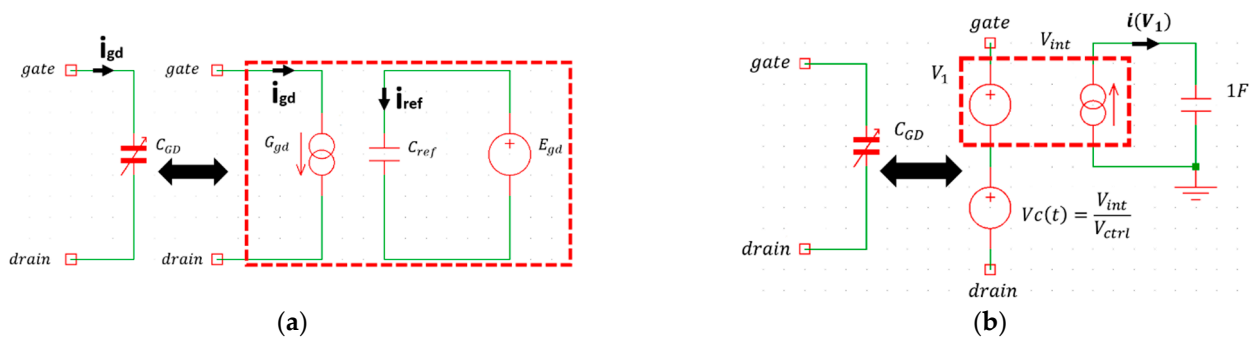


Figure 16. Parasitic capacitance implementations: (**a**) in [80]; (**b**) in [88].

Assume that:

$$\mathrm{C_{GD}} = s_1 \frac{1}{1 + \mathrm{e}^{\frac{s_2 - \mathrm{V_{GD}}}{s_3}}} + s_4 \frac{1}{1 + \mathrm{e}^{\frac{s_5 - \mathrm{V_{GD}}}{s_6}}} + s_7$$

where s_1 to s_7 are fitting parameters of the $\mathrm{C_{GD}}$-$\mathrm{V_{GD}}$ characteristic. $\mathrm{E_{GD}}$ is used to compute the derivative of the gate-drain voltage, which is equal to the current, I_{ref}, flowing through the 1F reference capacitance, C_{ref} is used to realize the $\mathrm{V_{GD}}$ derivative of $\mathrm{C_{GD}}$. The com-

parison between simulated and target curves has highlighted the good accuracy of this modelling approach.

A similar approach is proposed in [88] whose SPICE implementation is reported in Figure 16b. To diminish the risk of convergence problems in SPICE simulations, due to the presence of a non-linear equation, this model implements the C_{GD} capacitance starting from the well-known capacitor's branch equation written as:

$$C_{GD} = \frac{\int I_c(t)dt}{V_c(t)} = \frac{V_{int}}{V_{ctrl}} \tag{49}$$

where V_{int} is the voltage on the 1F capacitance (see Figure 16b), and V_{ctrl} is given by the following empirical formula:

$$V_{ctrl} = \begin{cases} A \tanh(aV_{GD}) + B & V_{GD} > 0 \\ C\ a \tanh(aV_{GD}) + D & V_{GD} < 0 \end{cases} \tag{50}$$

where a is a fitting parameter while A, B, C and D are constant parameters calculated depending on the C_{GD} min and C_{GD} max experimental values extracted by switching waveforms measured during a turn-on process in the half-bridge test circuit. The excellent result of C_{GS} fitting is achieved at drain-source voltages higher than 300 V.

A simpler and more accurate approach to modelling the behaviour of capacitances is that of look-up tables [58]. This approach provides excellent results because it implements a capacitance vs. V_{DS} correspondence extrapolated from the datasheet data. The C_{GD} and C_{DS} models consist of the following equation:

$$i_{GD} = C_{GD}(V_{DS}) \frac{dV_{GD}}{dt} \tag{51}$$

The derivative is implemented through an auxiliary circuit composed of one voltage source and one capacitance, and the approach is the same for the C_{GD} and C_{DS} capacitances. $C_{GD}(V_{DS})$ (or $C_{DS}(V_{DS})$) is implemented with the look-up table.

As can be seen from Section 2.6, the capacitance curves are similar for both MOSFETs and GaN HEMTs, the only difference is in the values of the capacitances. This means that the MOSFET models are valid for GaN HEMT devices too.

3.6. Summary Table

Most of the circuit models present in the literature have been analysed. Table 1 lists the MOSFET models described, specifying, for each of them, which blocks are suitable to be adapted for modelling GaN HEMTs. Table 1 provides an overview of the models previously reported and analysed. For each model of MOSFETs, it is indicated whether it is valid, adaptable, or useless to GaN HEMTs (when - appears in Table 1, it means that the paper does not model and has not reported that block). An equation used in the MOSFET model is "valid" for the GaN HEMT model when the equation can be also used in this model by setting only the values of the fitting parameters. While an equation used in the MOSFET model is "adaptable" when it needs some changes to be used for the GaN HEMT models, otherwise it is "useless". Most of the models that emulate the static characteristics (GMOS block) of the MOSFET device are valid or adaptable for modelling the GaN HEMT. The Vth block is never useful for GaN HEMT modelling, as highlighted in Section 3.2. R_{VAR} and third quadrant blocks are valid and adaptable to GaN HEMTs in very few cases. Instead, the proposed capacitance models for MOSFETs are all valid for GaN HEMTs. As can be seen from Table 1, no model proposed for MOSFET is useful for modelling the GaN HEMT in all its blocks.

Table 1. GaN modelling: usability of equations adopted in MOSFET models. Legend: ✓valid; • adaptable; x useless; - not reported.

Model	GMOS	V_{TH}	R_{VAR}	Third Quadrant	Capacitance
[58]	•	-	x	•	✓
[62]	✓	-	-	-	•
[66]	•	-	-	✓	•
[67]	✓	-	-	-	-
[69]	•	-	-	•	✓
[71]	✓	-	-	-	-
[72]	✓	-	•	-	•
[73]	✓	-	-	-	-
[75]	✓	-	-	-	-
[76]	•	-	-	-	-
[77]	✓	-	-	-	-
[78]	✓	-	-	-	-
[80]	•	-	-	•	-
[81]	✓	x	x	-	-
[82]	✓	x	-	-	-
[83]	-	x	x	-	-
[84]	-	-	✓	-	-
[85]	-	-	-	✓	✓
[88]	-	-	-	-	•
[89]	-	-	-	-	•
[90]	-	-	-	-	✓
[91]	-	-	-	-	✓
[92]	-	-	-	-	✓

4. Conclusions

In this paper, an overview of circuit models of the MOSFETs has been proposed. The comparison of each characteristic between the Si, SiC MOSFET and GaN HEMT datasheets has been carried out. This comparison has been fundamental to understanding if a MOSFET model is adaptable for the GaN HEMTs. The models have been commented to be used or adapted to develop the GaN HEMTs models. The comparison between the output and transfer characteristics of MOSFETs and GaN HEMT has highlighted that the behaviour of MOSFETs and GaN is similar (positive temperature coefficient) at low temperatures, while it is dissimilar (negative temperature coefficient for MOSFETs and positive temperature coefficient for GaN) at high temperature. Consequently, the equations that model this specific behaviour in the GMOS block of the MOSFETs are valid for GaN HEMT at room temperature only. The V_{TH} equations are useless for GaN HEMT modelling. R_{VAR} equations proposed for SiC SMOFET can be useful for the modelling of Si MOSFET and GaN HEMT only in the temperature range between 25 °C and 150 °C. The equations proposed for the body diode and third quadrant of MOSFET can be valid for GaN HEMT. Additionally, the trend of the capacitance characteristic is similar between MOSFET and GaN HEMT devices. For this reason, the equations, and implementations for the capacitances of MOSFETs are valid for GaN HEMTs although they present lower parasitic capacitances. The use of stochastic optimization algorithms to find the values of the fitting parameters is the best approach, since it enables us to reach a good result in an automatic manner. The effectiveness of this approach strongly increases as the equation complexity and the number of fitting parameters increase. The result of this paper provides a starting point for the modelling of GaN HEMT devices.

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Abbreviation

WGB	Wide bandgap
Si	Silicon
SiC	Silicon carbide
GaN	Gallium nitride
MOSFET	Metal oxide semiconductor field effect transistor
HEMT	High-electron-mobility transistor
CAD	Computer-aided design
TCAD	Technology computer-aided design
I_D	Drain current
V_{DS}	Drain-source voltage
V_{GS}	Gate-source voltage
V_{GD}	Gate-drain voltage
V_{SD}	Source-drain voltage
I_{GMOS}	GMOS current
$I_{GMOS,25}$	GMOS current at 25 °C
V_{GMOS}	GMOS voltage
I_{diode}	Diode current
V_{diode}	Diode voltage
R_{diode}	Parasitic resistance diode
$R_{diode,25}$	Parasitic resistance diode at 25 °C
$R_{VAR,25}$	Typical $R_{DS,on}$ value at 25 °C
V_{TH}	Threshold voltage
$V_{TH,25}$	Threshold voltage at 25 °C
T_{25}, T_j	Room, junction temperature
$I_{S,25}$	Saturation current
C_{DS}	Drain-source capacitance
C_{GS}	Gate-source capacitance
C_{DG}	Drain-gate capacitance
C_{ISS}	Input small signal capacitance
C_{OSS}	Output small signal capacitance
C_{RSS}	Reverse small signal capacitance
q	Electron charge
k	Boltzmann's constant
N	Emission coefficient
V_{EG}	Bandgap voltage
θ	Mobility modulation constant
W	Channel width
L	Channel length
Rs	Source resistance
Rd	Drain resistance

φ	Surface potential in strong inversion
γ	Body-effect parameter
λ	Channel modulation
K_s	Sub-threshold slope
K_n	Transconductance coefficient
ϕ_t	Thermal voltage
M	P-n gradient factor
V_{bi}	Built-in junction potential
$C_{GD}(0)$	Zero-bias gate-drain capacitance
$C_{DS}(0)$	Zero-bias drain-source capacitance

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