

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE AMERICA, INC.,
PETITIONER,

V.

INFINEON TECHNOLOGIES AUSTRIA AG,
PATENT OWNER.

IPR2025-00010
U.S. Patent 9,070,755

DECLARATION OF YUJI ZHAO, Ph.D.

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I. INTRODUCTION

1. I have been retained by Innoscience America, Inc. (“Petitioner”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office.

2. I am over 21 years of age and, if I am called upon to do so, I would be competent to testify as to the matters set forth herein.

3. I understand that this proceeding involves U.S. Patent No. 9,070,755 (“the ’755 patent,” Ex-1001).

4. I have been asked by Petitioner to provide my opinion on whether the claims of the ’755 patent would have been anticipated and/or obvious to a person of ordinary skill in the art at the time of the earliest possible priority date of the ’755 patent. In performing my analysis, I have been asked to assume that the priority date of the ’755 patent is July 23, 2012 and my opinions are set forth below. However, my opinions would not change if the ’755 patent was entitled to a priority date of February 17, 2012.

5. Throughout this declaration, I refer to specific pages, figures, and/or line numbers of various exhibits. These citations are illustrative and are not intended to suggest that they are the only support for the propositions for which they are cited.

II. SUMMARY OF OPINIONS

6. This declaration considers claims 1-14 of the '755 patent. Below, I set forth the opinions I have formed, the conclusions I have reached, and the bases for these opinions and conclusions. I believe the statements contained in this declaration to be true and correct to the best of my knowledge.

7. Based on my experience and knowledge of the art at the time of the applicable priority date, it is my opinion that claims 1-14 of the '755 patent would have been anticipated and/or obvious based on the asserted grounds discussed below.

8. I am being compensated for my time at my normal hourly rate. My compensation is in no way contingent upon the nature of my findings, the presentation of my findings in testimony, or the outcome of this proceeding.

III. QUALIFICATIONS AND BACKGROUND

9. I believe that I am well qualified to serve as a technical expert in this matter based upon my qualifications, discussed in detail below.

10. I am competent to write this declaration.

11. I am an independent consultant. All of my opinions stated in this declaration are based on my own personal knowledge and professional judgment. In forming my opinions, I have relied on my knowledge and experience in GaN materials science and electronics, and on the documents and information referenced

in this declaration. I am over 18 years of age and, if I am called upon to do so, I am competent to testify as to the matters set forth herein.

12. In formulating my opinions, I have relied upon my training, knowledge, and experience in the relevant art. Provided as Exhibit 1004 is a copy of my current curriculum vitae, which details my education and experience, and a list of all other cases in which, during the previous 8 years, I testified as an expert at trial or by deposition. The following provides a brief overview of some of my experience that is relevant to the matters set forth in this declaration.

13. I have a B.S. in Microelectronics from Fudan University, and an M.S. and Ph.D. in Electrical and Computer Engineering from University of California Santa Barbara (UCSB).

14. I have more than 10 years of experience in the area of GaN materials science and electronics, where I am widely recognized as a leader in the GaN electronics field. I have extensive, hands-on experience with GaN devices, including epitaxial growth, device fabrication, device wiring, and packaging. I have served as a Professor in Electrical and Computer Engineering, and I have taught many undergraduate and graduate classes on semiconductor electronics, including GaN devices fabrication and testing. In addition, I have given numerous invited lectures and seminars on GaN device technologies for many of the world's leading TSMC, MIT, Stanford University, and IEEE.

15. For my graduate studies, I worked with Prof. Shuji Nakamura at UCSB, who is recognized as the world's top scientist in the GaN research, who received the Nobel Prize in Physics in 2014 for his work on GaN materials and LEDs. I also worked with Prof. Umesh Mishra, who is a pioneer in the research of GaN high electron mobility transistors (HEMTs) and an elected member of U.S. National Academy of Engineering, which is considered to be among the highest recognitions in engineering-related fields. While at UCSB, I was a key researcher and a project leader in the Solid State Lighting and Energy Center (SSLEC), which is the world's leading research center for GaN materials and electronics research with an annual research budget of over \$5M. I have personally fabricated, tested, and packaged hundreds of GaN devices. My research work on GaN materials and devices led to the filing of several patent applications, over 100 media reports in six languages (including highlights in Science, Semiconductor Today, and Yahoo), and numerous papers and invited conference presentations, along with recognition from the SSLEC in years 2010 through 2012 with the "Outstanding Research Achievement Award."

16. After my Ph.D., I continued my research on GaN devices as an Assistant Professor at Arizona State University. I was the founder and Director of GaN Device Research Group at Arizona State University, which is funded by DoD, DOE, NASA, SFAz (Science Foundation of Arizona). The focus of the research group is on GaN devices including HEMTs. This research group engages over five

faculty members, and over twenty postdoctoral researchers and graduate students, and is one of the largest GaN research laboratories in the US, including state of the art equipment and methods to fabricate, analyze and test GaN HEMTs. In July 2021, I joined Rice University to lead the GaN research efforts, where I am currently a tenured Full Professor in the Department of Electrical and Computer Engineering.

17. I have served as PI or co-PIs for several large-scale US research programs on GaN power electronics. For example, I am the leading PI for the DOE ARPAe PNDIODES project, which is \$3M program for GaN power devices for electric vehicle applications. I am currently Co-PIs for two US national semiconductor centers, including the DOE ULTRA EFRC - a \$12 Million national research center focusing on power electronics, and the DARPA/SRC JUMP 2.0 CHIMES Center - a \$32.7 Million national center focusing on next generational 3D chips supported by Intel, TSMC, Samsung, and IBM. Both centers have extensive GaN electronics research efforts. Since August 2014, I have been awarded over \$50 million in collaborative research funding.

18. I am a member of two of the largest professional engineering societies: the Institute of Electrical and Electronics Engineers, Inc. ("IEEE") and the Materials Research Society ("MRS"). These professional societies address, among other things, GaN materials, devices, and packaging.

19. I have served on various conference committees (invited to participate) on leading semiconductor device conferences, including the Device Research Conference (DRC), the International Conference on Metal Organic Vapor Phase Epitaxy (ICMOVPE), and the Lester Eastman Conference on High Performance Devices (LEC). All of these conferences have large GaN devices sessions.

20. I have written five book chapters on GaN devices, two of which are directly related to GaN electronics and HEMTs. I have over 250 journal and conference publications on various subjects related to semiconductor devices, among which over 80 publications are directly on GaN electronics and HEMTs. A full list of my publications (articles and book chapters) on GaN electronics is included in my CV.

21. In 2010 through 2013, I received the UCSB Outstanding Research Achievement Award for contributions to fabrication high performance GaN devices. In 2015, I received the Bisgrove Scholar Faculty Award for research work in developing GaN electronics for communication and medical applications. In 2015, I received the NASA Early Career Faculty Award. In 2016, I received the DoD DTRA Young Investigator Award. In 2017, I received the Arizona State University Fulton Outstanding Assistant Professor Award for research work in GaN devices including HEMTs. In 2017, I was selected as an honorable Faculty Scientist to showcase NASA research to Congress at Capitol Hill, where I reported my research

to Rep. Lamar Smith, the Chairman of the Congress Committee on Science, Space, and Technology. In 2019, I received the MIT Technology Review Innovators Under 35 (TR 35) – China Award for my contributions in GaN research. In 2019, I received the Presidential Early Career Award in Science and Engineering (PECASE) from the White House, which is the highest honor given by the US government to early-career scientists and engineers. In 2023, I received TMS Frontiers of Materials Award for my contributions to GaN materials and electronics research.

22. Based on my education and experience, I believe that I have a detailed understanding of the state of the art during the relevant period.

IV. MATERIALS CONSIDERED

23. In forming my opinions, I have reviewed and considered the following documents and any other document cited in this declaration.

Exhibit	Description
Ex-1001	U.S. Patent No. 9,070,755 (“the ’755 patent”)
Ex-1005	U.S. Patent No. 5,523,599 to Fujishima et al. (“Fujishima”)
Ex-1006	U.S. Patent No. 5,910,670 to Ludikhuize (“Ludikhuize”)
Ex-1007	U.S. Patent Publication No. 2006/0091498 to Sriram et al. (“Sriram”)
Ex-1008	U.S. Patent No. 7,417,257 to Beach et al. (“Beach”)
Ex-1009	U.S. Patent Publication No. 2006/0255403 Asano et al. (“Asano”)

Exhibit	Description
Ex-1010	Kanamura et al., <i>High power and high gain AlGaIn/GaN MIS-HEMTs with high-k dielectric layer</i> , Phys. Stat. Sol., 5, No. 6, 2037–2040 (2008)
Ex-1011	Okino et al., <i>Drain Current DLTS of AlGaIn–GaN MIS-HEMTs</i> , IEEE Electron Device Letters, Vol. 25, No. 8 (2004)
Ex-1012	Imada et al., <i>Enhancement-Mode GaN MIS-HEMTs for Power Supplies</i> , The 2010 International Power Electronics Conference (2010)
Ex-1013	U.S. Patent Publication No. US2011/0073912 to Marui et al.
Ex-1014	U.S. Patent Publication No. US2010/0171150 to Smith et al.
Ex-1015	U.S. Patent Publication No. US2012/0146097 to Endo et al.
Ex-1016	U.S. Patent Publication No. US2009/0278236 to Sato et al.
Ex-1017	U.S. Patent Publication No. US2010/0193842 to Sato et al.
Ex-1018	Excerpts from Rudiger Quay, Gallium Nitride Electronics (2008)
Ex-1019	Mishra et al., <i>AlGaIn/GaN HEMTs—An Overview of Device Operation and Applications</i> , Proceedings of the IEEE, Vol. 90, No. 6 (2002)
Ex-1020	Wu et al., <i>Very-High Power Density AlGaIn/GaN HEMTs</i> , IEEE Transactions on Electronic Devices, Vol. 48, No. 3 (2001)
Ex-1021	S.H. Lee et al., <i>700V Lateral DMOS with New Source Fingertip Design</i> , Proceedings of the 20th International Symposium on Power Semiconductor Devices & IC's (2008)
Ex-1024	U.S. Patent Publication No. 2011/0121389 (“De Boet”)
Ex-1025	Excerpts from Umesh K. Mishra et al., Semiconductor Device Physics and Design (2008)
Ex-1027	Steven Leibson, <i>A Brief History of the MOS transistor, Part 1: Early Visionaries</i> , Electronic Engineering Journal (Apr. 3, 2023),

Exhibit	Description
	https://www.eejournal.com/article/a-brief-history-of-the-mos-transistor-part-1-early-visionaries/
Ex-1028	R. P. Jindal, <i>Noise Associated with Distributed Resistance of MOSFET Gate Structures in Integrated Circuits</i> , IEEE Transactions on Electron Devices, Vol. ED-31, No. 10 (October 1984)
Ex-1029	Evangelos F. Tsakas et al., <i>Noise Associated with Interdigitated Gate Structures in RF Submicron MOSFETs</i> , IEEE Transactions on Electron Devices, Vol. 47, No. 9 (September 2000)
EX-1032	Hiroshi Iwai et al., <i>The Transistor was Invented 75 Years Ago: A Big Milestone in Human History</i> , The Electrochemical Society Interface (Winter 2022)
EX-1033	Cassiano Ferro Moraes, <i>Understanding Transistors: What They Are and How They Work</i> , Wevolver (Nov. 6, 2023), https://www.wevolver.com/article/understanding-transistors-what-they-are-and-how-they-work
EX-1034	RS, <i>A Complete Guide to MOSFET Transistors</i> (Jan. 16, 2023), https://uk.rs-online.com/web/content/discovery/ideas-and-advice/mosfet-guide
EX-1035	A. Blicher et al., <i>Encyclopedia of Physical Science and Technology</i> , Vol. 5, p. 831-849 (Robert A. Meyers, 3d. ed. 2003)
EX-1036	D. W. Runton et al., <i>History of GaN</i> , IEEE Microwave Magazine (May 2013)
EX-1037	Qorvo, <i>What You Need to Know About GaN Technology</i> (Feb. 15, 2023), https://www.qorvo.com/design-hub/blog/what-you-need-to-know-about-gan-technology
EX-1038	W. F. Perina et al., <i>Effect of interface traps on the different conduction mechanisms of MISHEMT from 200 K to 450 K</i> , 2024 38th Symposium on Microelectronics Technology and Devices (SBMicro) (Sept. 2024)

Exhibit	Description
EX-1039	Jui-Sheng Wu et al., <i>Recent Progress of E-mode Gallium Nitride Metal–Insulator–Semiconductor -High Electron Mobility Transistors with Hybrid Ferroelectric Charge Trap Gate (FEG-HEMT) for Power Switching Applications</i> , Physica Status Solidi (a) - Applications and Materials Science, Vol. 220, No. 16 (Aug. 2023)
EX-1040	Sonu Daryanani, <i>GaN Power HEMT > 650 V: A Parametric Analysis and Comparison to SiC MOSFET</i> , Power Electronics News (Jun. 23, 2022), https://www.powerelectronicsnews.com/gan-power-hemt-650-v-a-parametric-analysis-and-comparison-to-sic-mosfet/
EX-1041	U.S. Patent Publication No. 2005/0127438 (“Hossain 438”)
EX-1042	Enrico Bottaro et al., <i>Circuit Models of Power MOSFETs Leading the Way of GaN HEMT Modelling—A Review</i> , Energies 2022, 15, 2415 (May 7, 2022)
EX-1043	Utkarsh Jadli, <i>Modeling Power GaN-HEMTs Using Standard MOSFET Equations and Parameters in SPICE</i> , Electronics 2021, 10, 130 (January 9, 2021)
EX-1044	Shreepad Karmalkar, <i>A New Equivalent MOSFET Representation of a HEMT to Analytically Model Non-Linear Charge Control for Simulation of HEMT Devices and Circuits</i> , IEEE Transactions on Electron Devices, Vol. 44, No. 5 (May 1997)

24. I have also relied on my education, experience, research, training, and knowledge in the relevant art, and my understanding of any applicable legal principles described in this declaration.

25. All the opinions contained in this declaration are based on the documents I reviewed and my knowledge and professional judgment. My opinions

have also been guided by my understanding of how a person of ordinary skill in the art would have understood the claims of the '755 patent at the time of the invention.

26. I reserve the right to supplement and amend any of my opinions in this declaration based on documents, testimony, and other information that becomes available to me after the date of this declaration.

V. LEGAL STANDARDS

27. I am not a lawyer. My understanding of the legal standards to apply in reaching the conclusions in this declaration is based on discussions with counsel for Petitioner, my experience applying similar standards in other patent-related matters, and my reading of the documents submitted in this proceeding. In preparing this declaration, I have tried to faithfully apply these legal standards to the challenged claims.

28. I have been informed that there are two ways in which prior art may render a patent claim unpatentable. First, I have been informed that the prior art can “anticipate” a claim. Second, I have been informed that the prior art can render a claim “obvious” to a person of ordinary skill in the art. I understand that a claim is patentable if it was not anticipated and would not have been obvious in view of the prior art as of the effective filing date of the patent.

29. I have been informed that a dependent claim is a patent claim that refers back to another patent claim. I have been informed that a dependent claim includes all the limitations of the claim to which it refers.

30. I have been asked to provide my opinions as to whether the cited prior art discloses or renders obvious claims 1-14 of the '755 patent from the perspective of a person of ordinary skill in the art at the '755 patent's earliest possible priority date in 2012, as described in more detail below.

31. I have been informed that in *inter partes* review proceedings, such as this one, the party challenging the patent bears the burden of proving unpatentability by a preponderance of the evidence. I understand that a preponderance of the evidence means "more likely than not."

32. For the purposes of this declaration, I have been asked to provide my opinions on issues regarding unpatentability. I have been informed of the following legal standards, which I have applied in forming my opinions.

A. Level of Ordinary Skill

33. I have been informed that a person of ordinary skill in the art is determined by considering several factors, including the (i) type of problems encountered in the art; (ii) prior art solutions to those problems; (iii) rapidity with which innovations are made; (iv) sophistication of the technology; and (v) educational level of active workers in the field.

34. I have been instructed to assume that a person of ordinary skill in the art is not a specific, real individual but rather a hypothetical individual having the qualities reflected by the factors discussed above.

B. Prior Art

35. I have been advised and understand that the information used to evaluate whether an invention was new and not obvious when made is generally referred to as “prior art.” I understand that prior art includes patents and printed publications that existed before the earliest priority date or the earliest filing date of the patent (which I have been informed is also called the “effective filing date”). I have been informed and understand that a patent or published patent application is prior art if it was filed before the effective filing date of the claimed invention and that a printed publication is prior art if it was publicly available before the effective filing date of the claimed invention.

C. Anticipation

36. I have been informed that, under 35 U.S.C. § 102, a patent claim is unpatentable for anticipation if the claimed subject matter was patented or described in a printed publication before the effective filing date of the claimed invention. I have been informed that this is referred to as unpatentability by anticipation. I have been informed that a patent claim is anticipated under § 102 if a single prior art reference discloses all limitations of the claim.

D. Obviousness

37. I have been informed that for obviousness under 35 U.S.C. § 103, a patent claim is unpatentable if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a person having ordinary skill in the art to which said subject matter pertains at the time the invention was made. I have been informed that this is referred to as unpatentability by obviousness.

38. I have been informed that an obviousness analysis includes the following considerations:

- a. Determining the scope and content of the prior art;
- b. Ascertaining the differences between the prior art and the claims at issue;
- c. Resolving the level of ordinary skill in the pertinent art; and
- d. Considering evidence of secondary indicia of nonobviousness (if available).

39. I have been informed that the relevant time for considering whether a claim would have been obvious to a person of ordinary skill in the art is the time of invention. For my obviousness analysis, counsel for Petitioner instructed me to assume that the date of invention for the challenged claims is July 23, 2012. My

opinions would not change if I assumed (i) a later date of invention or (ii) that the date of invention for the challenged claims is February 17, 2012.

40. I have been informed that a reference may be modified or combined with other references or with a person of ordinary skill in the art's own knowledge if the person would have found the modification or combination obvious. I have also been informed that a person of ordinary skill in the art is presumed to know all the relevant prior art, and the obviousness analysis may take into account the inferences and creative steps that a person of ordinary skill in the art would employ.

41. I have been informed that whether a prior art reference renders a patent claim obvious is determined from the perspective of a person of ordinary skill in the art. I have also been informed that there is no requirement that the prior art contain an express suggestion to combine known elements to achieve the claimed invention. I have also been informed that a suggestion to combine known elements to achieve the claimed invention may come from the prior art as a whole or individually and may consider the inferences and creative steps a person of ordinary skill in the art would employ, as filtered through the knowledge of one skilled in the art. However, I have also been informed that, while taking these previous statements into account, obviousness grounds cannot be sustained by mere conclusory statements and must include some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.

42. In determining whether a prior art reference could have been combined with another prior art reference or other information known to a person having ordinary skill in the art, I have been informed that the following principles may be considered:

- a. A combination of familiar elements according to known methods would have been obvious if it yielded predictable results;
- b. The substitution of one known element for another would have been obvious if it yielded predictable results;
- c. The use of a known technique to improve similar devices, systems, or methods in the same way would have been obvious if it yielded predictable results;
- d. The application of a known technique to a device, system, or method that is ready for improvement would have been obvious if it yielded predictable results;
- e. Any need or problem known in the field and/or addressed by a prior art reference can provide a reason for combining the elements in the manner claimed;
- f. A person of ordinary skill often will be able to fit the teachings of multiple references together like a puzzle; and

- g. The proper analysis of obviousness requires a determination of whether a person of ordinary skill in the art would have a “reasonable expectation of success”—but not “absolute predictability” of success—in achieving the claimed invention by combining prior art references.

43. I have been informed that, when a work is available in one field, design alternatives and other market forces can prompt variations of it, either in the same field or in another. I have been informed that if a person of ordinary skill in the art could have implemented a predictable variation and would have seen the benefit of doing so, that variation would have been obvious. I have been informed that, in many fields, there may be little discussion of obvious combinations, and in these fields, market demand—not scientific literature—may drive design trends. I have been informed that, when there was a design need or market pressure and there are a finite number of predictable solutions, a person of ordinary skill in the art would have had a good reason to pursue those known options.

44. I have been informed that the law permits the application of “common sense” in examining whether a claimed invention would have been obvious to a person skilled in the art. For example, I have been informed that combining familiar elements according to known methods and in a predictable way may suggest obviousness when such a combination would have yielded nothing more than

predictable results. I understand, however, that a claim is not obvious merely because every claim element is disclosed in the prior art, and that a party asserting obviousness must still provide a specific motivation to combine or modify the references as recited in the claims and explain why one skilled in the art would have reasonably expected to succeed in doing so.

45. I have been informed that there is no rigid rule that a reference or combination of references must contain a “teaching, suggestion, or motivation” to combine references. But I also understand that the “teaching, suggestion, or motivation” test can be a useful guide in establishing a rationale for combining elements of the prior art. I have been informed that this test poses the question as to whether there is an express or implied teaching, suggestion, or motivation to combine prior art elements in a way that realizes the claimed invention, and that it seeks to counter impermissible hindsight analysis.

46. I am not aware of any evidence of secondary considerations that would support a determination of nonobviousness of the claimed subject matter in the ’755 patent.

47. I have been informed that, in an obviousness analysis, prior art must be analogous to the patent being considered. I have been informed that a prior art reference is considered to be analogous, or in the same field of art, if the reference is either (1) in the same field of endeavor as the challenged patent, regardless of the

problems the challenged patent and the prior art address; or (2) reasonably pertinent to the particular problem being solved by the challenged patent.

VI. TECHNOLOGY OVERVIEW

A. History of Transistors

48. Field-Effect Transistors (FETs) were developed in the 1920s and are a key technology in modern electronics, used extensively in integrated circuits and various electronic devices. Ex-1027 (“By contrast, development of the metal-oxidesemiconductor (MOS) field-effect transistor (FET) took decades, from its conception in the 1920s to an initial working device at the very end of the 1950s, to working commercial products in the 1960s”). One type of FET was the MISFET, which provides an insulating layer between the gate and the semiconductor channel to improve device control, was first considered in the 1920s, and emerged in the 1960s. Ex-1032 (“the idea of ... MISFET (Metal Insulator Semiconductor FET)/MOSFET (Metal Oxide Semiconductor FET) in 1928 were filed as patents by Julius E. Lilienfel. ... Later, the ideas of MISFETs/MOSFETs were proposed by several people—Oskar Heil in 1934,¹⁸ Heinrich Welker in 1945,¹⁹ and even by W. Shockley in 1945¹³ and others. But none of them showed successful amplification results until 1960, because of immature semiconductor quality and poor understanding of and technology to control the semiconductor surface”). A major breakthrough occurred in FET technology with the invention of MOSFETs (Metal-

Oxide-Semiconductor FETs), which is a type of MISFET, and this device is still one of the dominant transistors in electronics today. Ex-1027 (“When Bell Labs announced the junction transistor in 1951, it quickly became the dominant transistor in the industry because it was superior in every way to the original point-contact device”); EX-1033 (“The next major innovation came in 1959 with the invention of the metal-oxide-semiconductor field-effect transistor (MOSFET), also known as the MOS transistor. The MOS transistor offered several advantages over the BJT, including lower power consumption and the ability to be miniaturized, making it ideal for integrated circuits. Today, MOS transistors are the most widely used type of transistor in the world.”). MOSFETs are considered MISFETs because they include an insulating layer (e.g., silicon dioxide layer). Ex-1034 (“All MOSFETs are MISFETs (Metal Insulator Semiconductor Field Effect Transistors) but not all MISFETs are MOSFETs”); Ex-1035, 839 (“The most important MISFET is the metal oxide semiconductor transistor (MOSFET).”).

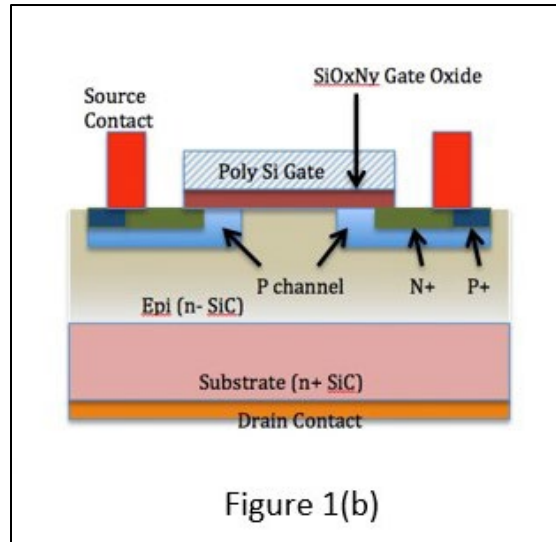
49. GaN HEMTs, another type of FETs, developed in the 1990s and commercialized in the 2000s, introduced higher-power and higher-frequency performance. Ex-1036, 82 (“In the early 1990s, gallium nitride (GaN) was deemed an excellent, next generation, semiconductor material for high power/high frequency transistors based on the material parameters of bandgap, electron mobility, and saturated electron velocity.”); Ex-1037 (“GaN's potential as a high-power and high-

frequency semiconductor transistor-based material was first recognized and explored in the early 1990s. By the mid to late 2000s, GaN had made its way into production applications for defense and aerospace and commercially in light-emitting diodes (LEDs) for solid-state lighting.”). GaN MIS-HEMTs are a type of MISFET as they use an insulating layer between the gate and the semiconductor channel to improve device control. Ex-1038, 1, 3 (“Combining the opposite behaviors of the threshold voltage curves of the MISFET and HEMT as a function of temperature, gives a possible explanation of the threshold voltage rebound effect observed in MISHEMT.”); Ex-1010 (Kanamura), 2037-38 (discussing introducing an insulator between the gate and semiconductor in a AlGa_N/Ga_N HEMT to create a AlGa_N/Ga_N MIS-HEMT); Ex-1011 (Okino). GaN MIS-HEMTs were developed and commercialized in the early 2000s and further advanced GaN-based technologies, making them vital in modern power and RF applications. Ex-1011 (2004 research paper on AlGa_N–Ga_N MIS-HEMTs); Ex-1010 (2007 research paper on AlGa_N/Ga_N MIS-HEMTs); Ex-1039, 1, 9 (explaining the viability and usefulness of MIS-HEMTs).

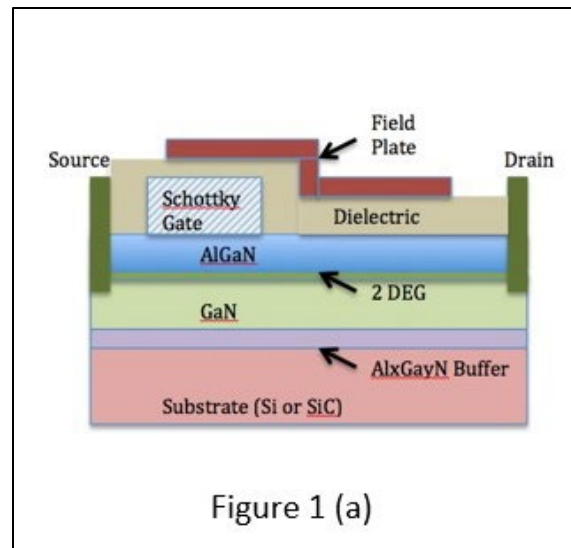
B. Electrode Structure Commonalities

50. As shown by the figures below, FETs, including MISFETs, MOSFETs, GaN HEMTs and GaN MIS-HEMTs, share a basic electrode structure that facilitates the control of current through the device, including (i) a source electrode where

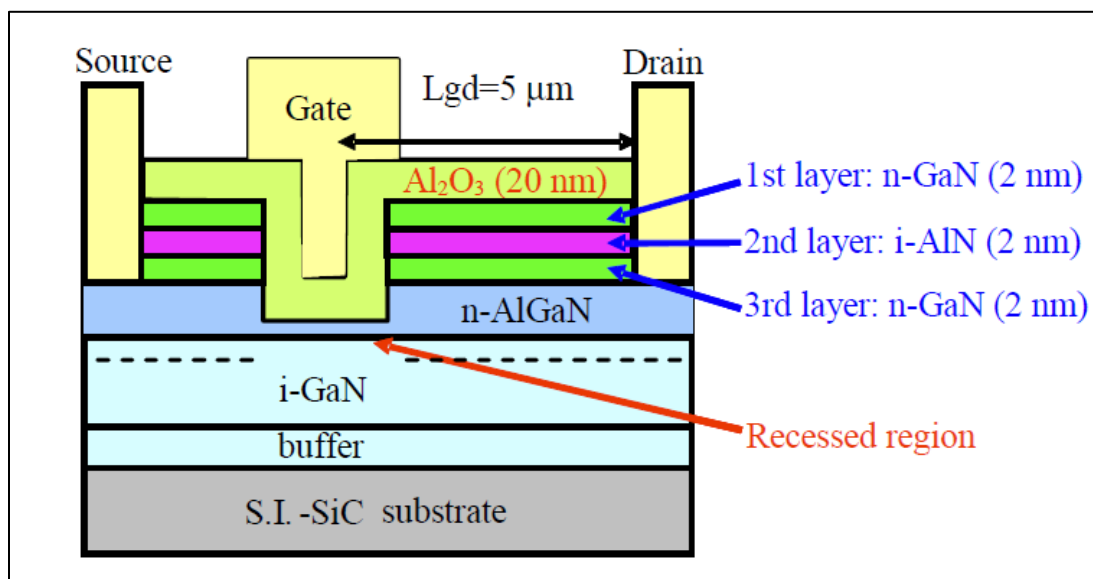
charge carriers originate, (ii) a drain electrode where the charge carriers exit after flowing from the source electrode, and (iii) a gate electrode that controls the flow of charge carriers between the source and drain. The '755 Patent confirms this as well, noting that “[i]n a typical lateral transistor layout, for example, drain and source finger electrodes coupled to respective drain and source pads may be interdigitated with a gate region located between the source and drain.” ’755 Pat., 2:8-21, 3:56-4:8.



Ex-1040 (showing an example of a structure a MOSFET, which is a type of MISFET as I explained above).



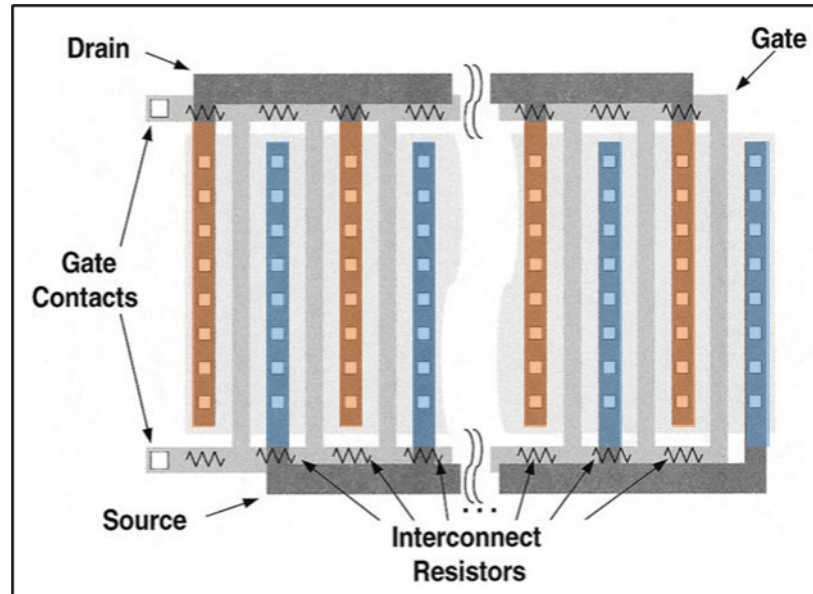
Ex-1040 (showing an example of a GaN HEMT structure).



Ex-1012 (Imada), Fig. 2 (showing a “cross-sectional view of AlGaN/GaN MIS-HEMT structure”).

51. MISFETs, MOSFETs, and GaN HEMTs can be designed with interdigitated structure, as shown below, which is a layout in which the **source** and **drain** electrodes are arranged in a repeating, finger-like pattern that maximizes the

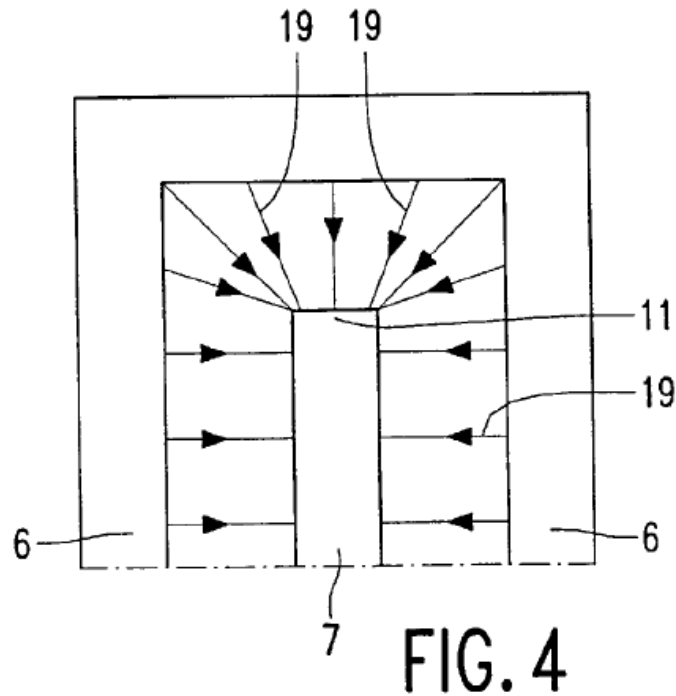
overlap and surface area between the active regions while minimizing the device footprint.



Ex-1029, 1746.

52. It was well known that current converges at the end portions of the drain finger electrode causing an increased electric field creating various device issues.

Ludikhuize, 4:4-26, Fig. 4.



Ludikhuize, Fig. 4 (showing concentration of the electric field at the end portions 11 of drain finger 7).

53. It was also well known to change the configuration or geometry of the finger-like portions of these electrodes to address this issue. For example, in 2007, a patent described tapered fingers for controlling high currents at the end portions. Beach, Fig. 3, Claim 1, Abstract, 5:57-6:11.

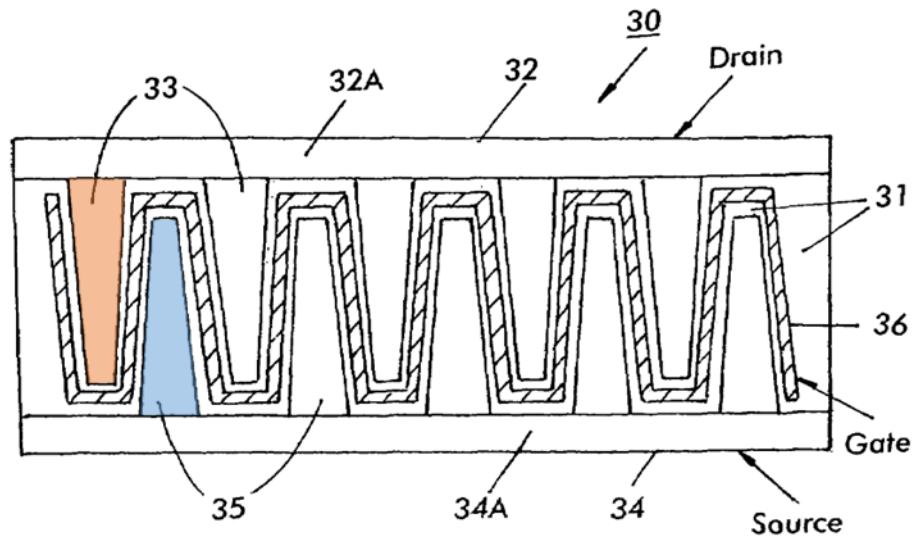


FIG. 3

Beach, Fig. 3 (showing **drain electrodes** and **source electrodes**), Claim 1, Abstract, 5:57-6:11.

54. In 2011, a patent publication disclosed a **drain electrode** with end portion with an increased curvature than the rest of its main body to reduce the electric field effect at the end portion. Ex-1024 ¶¶37-38, Fig. 4 (annotated).

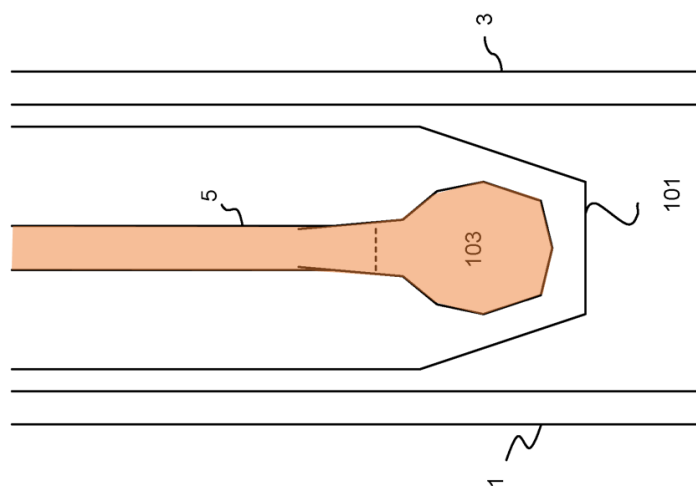
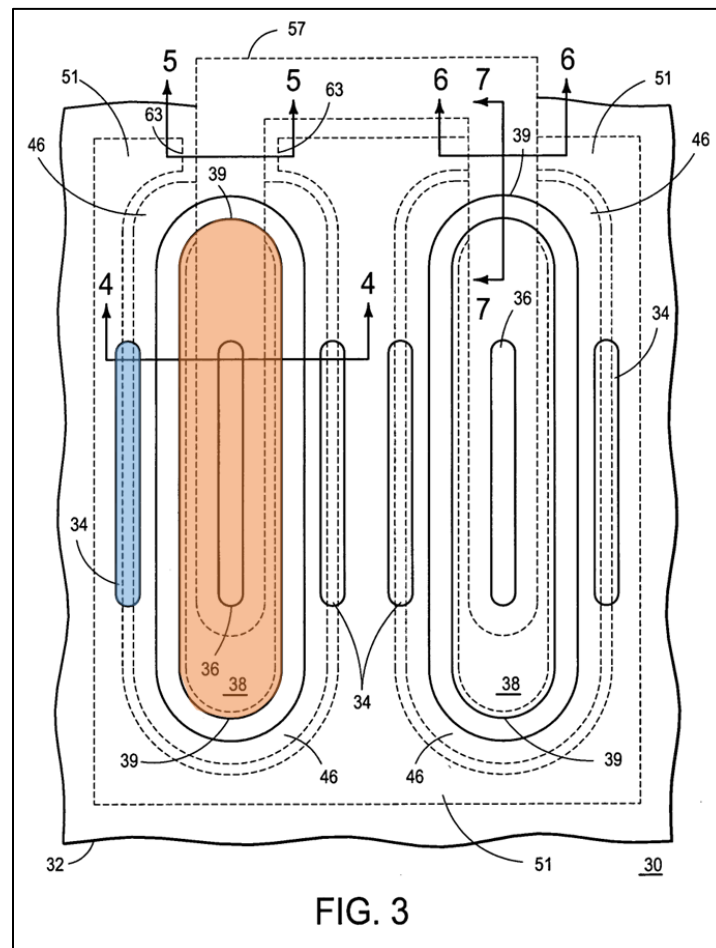


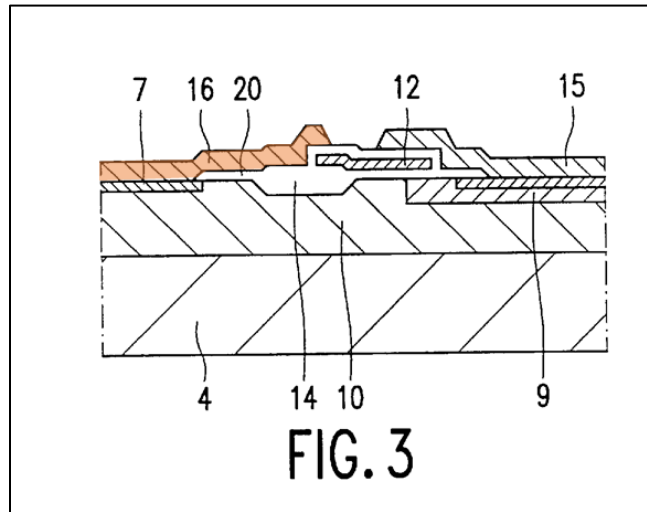
Fig. 4

55. A 2005 patent publication discloses **drain finger electrodes** longer than the **source finger electrodes**, such that the drain electrodes extend past the source electrodes on both sides. *See* Ex-1041 ¶20 (explaining that Fig. 3 shows drain fingers 39 and source regions 34); Fig. 3 (showing that drain fingers 39 are longer and extend past the source regions 34), ¶35 (noting that a “further advantage is that the drain finger design is flexible to include long drain fingers”), ¶¶16-17 (noting that the disclosed “structure according to the present invention eliminates electric field crowding issues associated with fingertip regions”); *see also id.*; ¶¶ 5, 8, 19.



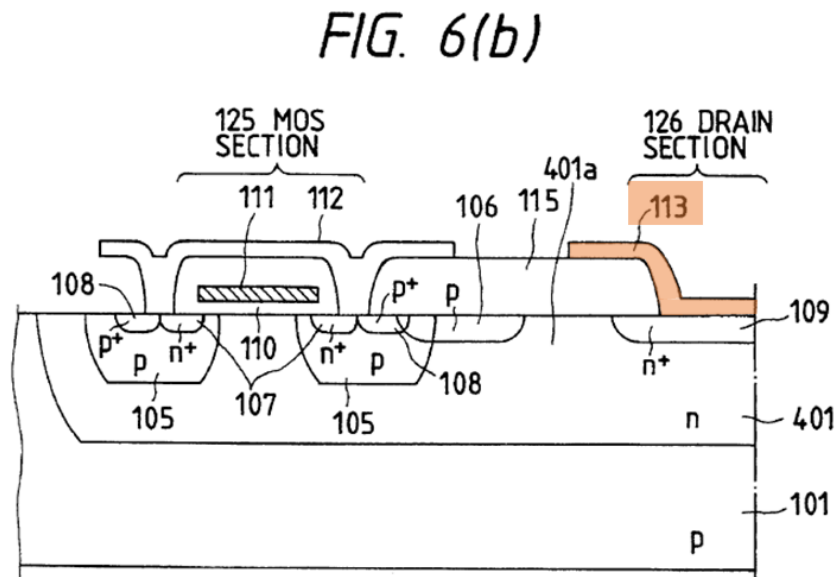
Ex-1041, Fig. 3 (annotated).

56. A 1999 patent, Ludikhuize, describes elevating the end portion of a drain finger electrode to reduce the electric field in the drift region of the device and raise the breakdown voltage of the device. Ludikhuize, Figs. 1, 3, 4:43-57.



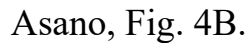
Ludikhuize, Fig. 3 (annotated). Specifically, Ludikhuize explains that the “drain electrode 16 extends over the drift region 10 at the area of the end face 11 of the drain. As a result, the electrode 16 acts as a field plate on the drain at high voltages, so that the electric field in the drift region is reduced, and thus the breakdown voltage is raised. To enhance this effect, the field oxide 14 at the end face 11 of the drain may be provided at some distance away from the drain zone 7, in a modified version of the device shown in FIG. 1. This is shown in FIG. 3, ... electrode 16 effectively acts as a field plate, thus reducing the concentration of equipotential lines.” Ludikhuize, 4:43-57.

57. A 1996 patent, Fujishima, also describes elevating the end portion of the **drain finger** to help alleviate the electric field effect. Fujishima, 8:59-9:2, 10:66-11:8, 12:27-32, Figs. 6(b).



Fujishima, Fig. 6(b) (annotated).

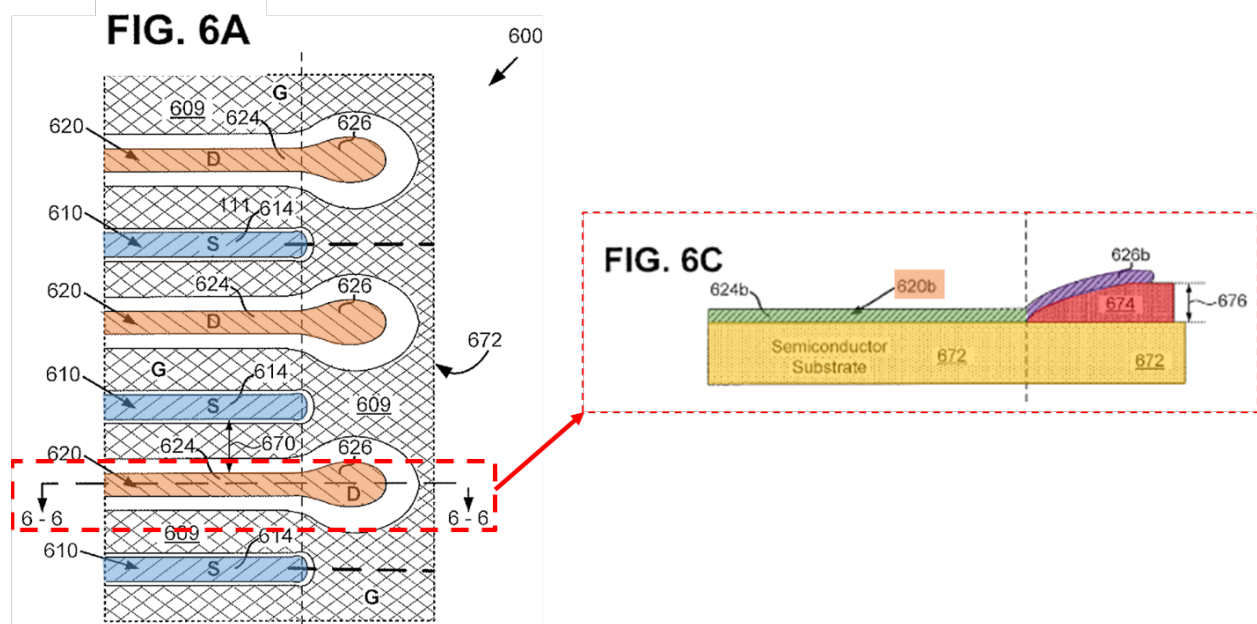
58. A 2006 publication, Asano, depicts a similar configuration, which a POSA would have understood to have the same effect—reducing the electric field at the end portion.



A. Overview

60. Figures 6A and 6C describe one electrode structure design. Figure 6A shows **drain finger electrodes 620** and **source finger electrodes 610** in an

interdigitated pattern and Figure 6C shows a cross sectional view of a **drain finger electrode** that shows a **main body portion 624b** and **end portion 626b**, which is elevated over a **substrate 672** using a **dielectric material 674**.



61. The '755 patent discloses additional electrode structure designs, including (i) the **end portion** of the **drain finger electrode** having an ellipsoid shape that has an increased radius of curvature ('755 Pat., 5:27-42), (ii) the **end portion** of the **drain finger electrode** extending past the main body of a **source finger electrode** (*id.*, 5:43-51), and (iii) **drain finger electrodes** that are longer than **source finger electrodes** (*id.*). The '755 patent also describes a tapered **drain finger electrode** but concedes that “tapered source and drain finger designs [were] described” in Beach in 2008—four years before the alleged time of invention. *Id.*, 8:43-55.

VIII. CLAIM CONSTRUCTION

62. I understand that the United States Patent and Trademark Office interprets claim terms in an *inter partes* review proceeding under the same claim construction standard that is used in a United States federal court. I understand that, under this standard, the meaning of claim terms is considered from the viewpoint of a person of ordinary skill in the art at the time of the alleged invention.

63. I have been informed that claim terms are generally given their ordinary and customary meaning as understood by one of ordinary skill in the art in light of the specification and the prosecution history pertaining to the patent. I understand, however, that claim terms are generally not limited by the embodiments described in the specification.

64. I understand that in addition to the claims, specification, and prosecution history, other evidence may be considered to ascertain the meaning of claim terms, including textbooks, encyclopedias, articles, and dictionaries. I have been informed that this other evidence is often less significant and less reliable than the claims, specification, and prosecution history.

65. I understand that a district court has yet to construe the claim terms of this patent. At this time, I do not see the need to construe any terms of the challenged claims for the purposes of this proceeding. Therefore, in preparing my analysis, I have applied the ordinary and customary meaning that each claim term would have

to a person of ordinary skill in the art in light of the '755 patent's specification and prosecution history. If any claim terms are differently construed, I reserve the right to reassess my opinions under said constructions.

IX. LEVEL OF ORDINARY SKILL IN THE ART

66. In rendering the opinions set forth in this declaration, I have been asked to consider the '755 patent's claims and the prior art through the eyes of a person of ordinary skill in the art (which I may also refer to as "one skilled in the art," "skilled artisan," "POSA," or similar variations). I have considered factors such as the educational level and years of experience of those working in the pertinent art, the types of problems encountered in the art, the teachings of the prior art, patents and publications of other persons or companies, and the sophistication of the technology.

67. Taking into consideration the factors described in Section V.A, it is my opinion that a POSA at the time of the purported invention would have possessed at least a four-year degree in electrical engineering or a closely related field, and at least two years of experience in semiconductor device design. Additional education could substitute for professional experience and vice versa.

68. I met the criteria for a POSA at the effective filing date of the '755 patent.

X. GROUNDS OF UNPATENTABILITY

69. Based on my review of the materials set forth above, including my application of the knowledge of a person of ordinary skill in the art (“POSA”), it is my opinion that claims 1-14 of the ’755 patent are anticipated or would have been obvious to a POSA. In particular, it is my opinion that claims 1-14 of the ’755 patent would have been anticipated and/or obvious to a POSA at the effective filing date of the ’755 patent, based on the grounds shown below:

Grounds		Challenged Claims	Basis	Prior Art
Fujishima Grounds	1A	1-5, 8-14	§102	Fujishima
	1B	1-14	§103	Fujishima
	1C	6-7	§103	Fujishima and Ludikhuize
	1D	8-9, 14	§103	Fujishima and Sriram
	1E	13	§103	Fujishima and Beach
Asano Grounds	2A	1-4, 8-9	§102	Asano
	2B	1-4, 8-9	§103	Asano

XI. FUJISHIMA GROUNDS 1A-1E ANTICIPATE OR RENDER OBVIOUS CLAIMS 1-14

A. Grounds 1A-1B: Fujishima Anticipates and/or Renders Obvious Claims 1-14

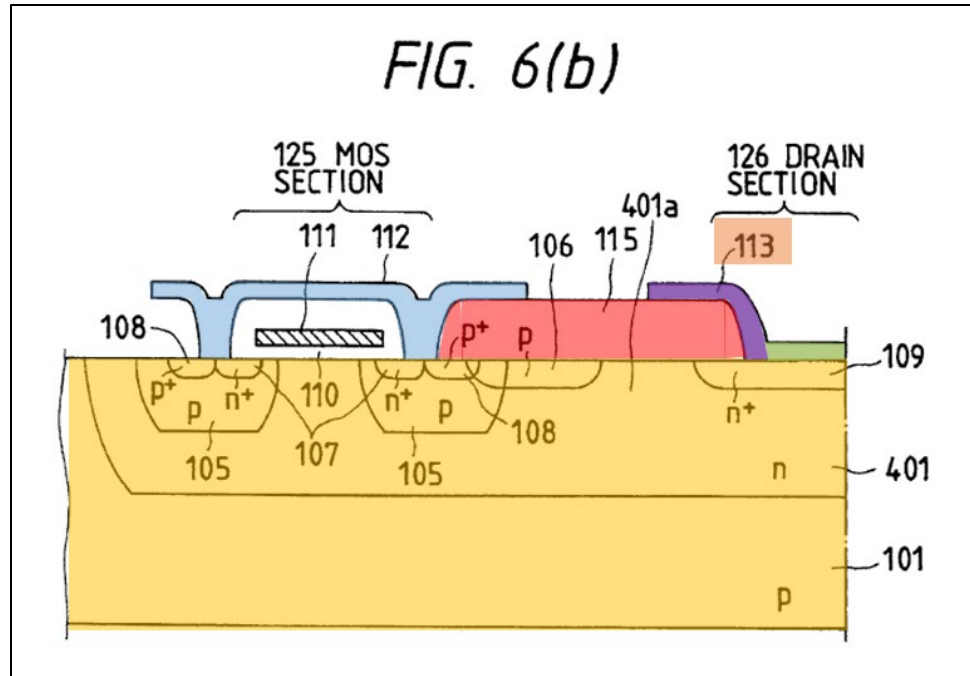
1. Fujishima

70. Fujishima discloses a configuration of transistors, specifically a configuration for high voltage “Metal Insulator Semiconductor” field effect

transistors—or MISFETs. Fujishima, 1:6-13; '755 Pat., 3:56-65. A POSA would have understood that, by February of 2012 (i.e., the earliest claimed time of the invention alleged in the '755 patent), one known type of MISFETs was Gallium Nitride High Electron Mobility Transistors (HEMT) MISFETs—GaN MIS-HEMT for short—which is a group III-V transistor. Ex-1010-1017; Ex-1018, 155; Ex-1025, 375-378, 393-94, 402-403; Ex-1019-20. As Figure 6(b) shows, for example, a POSA would have understood that Fujishima discloses a lateral transistor structure with both the drain and source on the same surface of the semiconductor substrate. Fujishima, 13:37-51, Fig. 6(b).

71. Fujishima further discloses configuring transistors to have a “high withstanding voltage” and minimize negative electric field effect, including at the ends of drain finger electrodes of the transistor. Fujishima, 2:65-3:34, 3:44-52, 6:13-33. A POSA would have understood that one of Fujishima’s disclosed configurations projects the end portion of a drain electrode over an insulating film to minimize the electric field at the end portion. *Id.*, 12:23-40, Fig. 6(b).

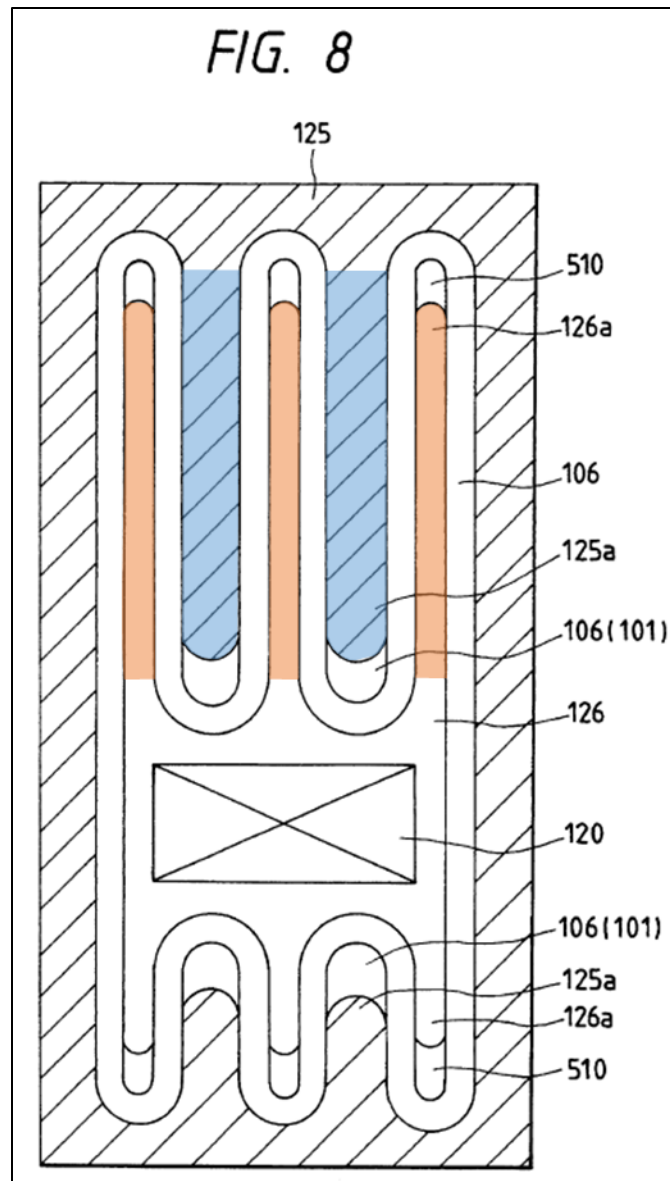
72. This is shown below in Fujishima’s Figure 6(b), which shows a cross-section of the MISFET configuration including **a drain electrode 113** with **a main body portion** and **an end portion**, **a source electrode 112**, **a substrate**, and **an insulating layer 115** that (i) has an increased thickness from the outer end to the center and (ii) elevates portions of both electrodes.



73.

Id., Fig. 6(b) (annotated). As the Figure above shows, the elevated parts of the **end portion** of the **drain electrode 113** are non-coplanar with the **main body portion**, which, as Fujishima explains, minimizes the negative electric field effect at the **end portion** of the drain electrode. *Id.*, 12:27-31, 10:66-11:4, 3:1-33, 3:44-52, 6:13-33.

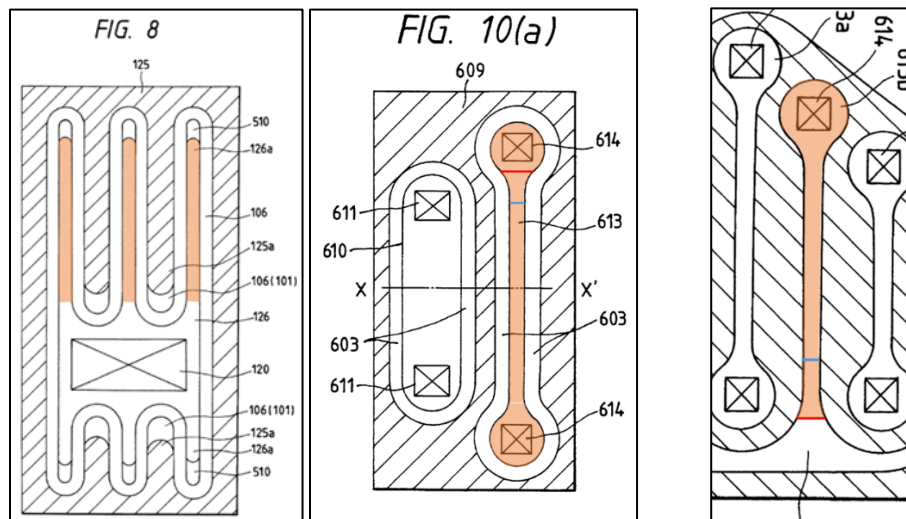
74. A POSA would have also understood that Fujishima's Figure 8 shows the top view of the same MISFET configuration in Figure 6(b). *Id.*, 13:37-51. As shown below, Figure 8 shows multiple **drain finger electrodes** extending from a base portion and multiple **source finger electrodes** with a similar finger configuration:



Id., Fig. 8 (annotated). Fujishima explains that the **source electrode fingers** and **drain electrodes fingers** “are juxtaposed in an interdigitated manner.” *Id.*, 13:37-51. A POSA would have further understood that the current flows from the **drain** to the **source**, as that is a core principle of transistors. Ex-1025, 356.

75. A POSA would have understood that Fujishima discloses multiple options for configuring a **drain finger electrode**. For example, in addition to Figure

8's configuration, Figure 10(a) shows the **drain finger electrode** having an **end portion** that tapers into an ellipsoid shape, which, as Fujishima explains, improves the device by increasing the device withstand voltage and reducing negative electric field effects. *Id.*, 5:14-22, 17:29-54. This is consistent with how a POSA would have understood the benefits of such a configuration, as sharp edges create negative electric field effect, whereas curved portions reduce or eliminate such an effect. Additionally, Fujishima discloses another configuration option as Figure 16 discloses a **drain electrode** with tapered fingers showing that the drain fingers have a width greater at one segment than another segment, as indicated by the red and blue lines below.



Id., Figs. 8, 10(a) (annotated), Fig. 16 (annotated and excerpted).

2. Independent Claim 1

a. [1pre]: A transistor comprising:

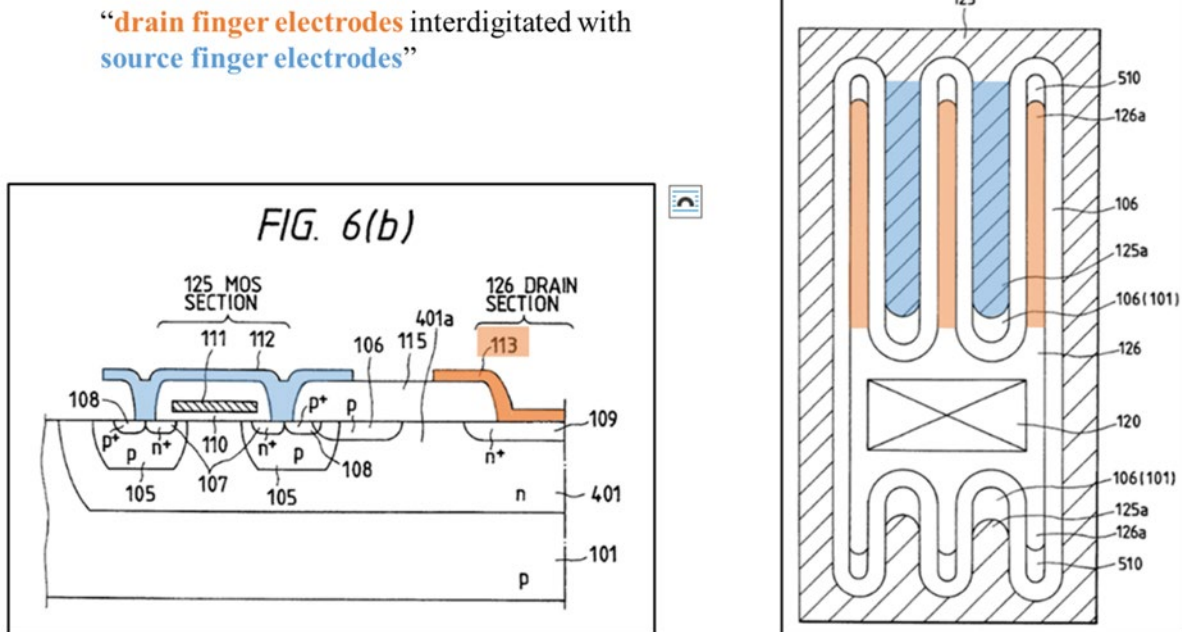
76. If the preamble is limiting, it is my opinion that Fujishima discloses or renders obvious [1pre] because it discloses a “high voltage MIS field effect *transistor*.” Fujishima, Abstract, 1:6-19, 13:37-40.

b. [1a]: drain finger electrodes interdigitated with source finger electrodes;

77. It is my opinion that Fujishima discloses [1a] because it discloses **drain finger electrodes** and **source finger electrodes** that “are juxtaposed in an interdigitated manner.” Fujishima, 15:9-24, Figs. 6(b), 8.

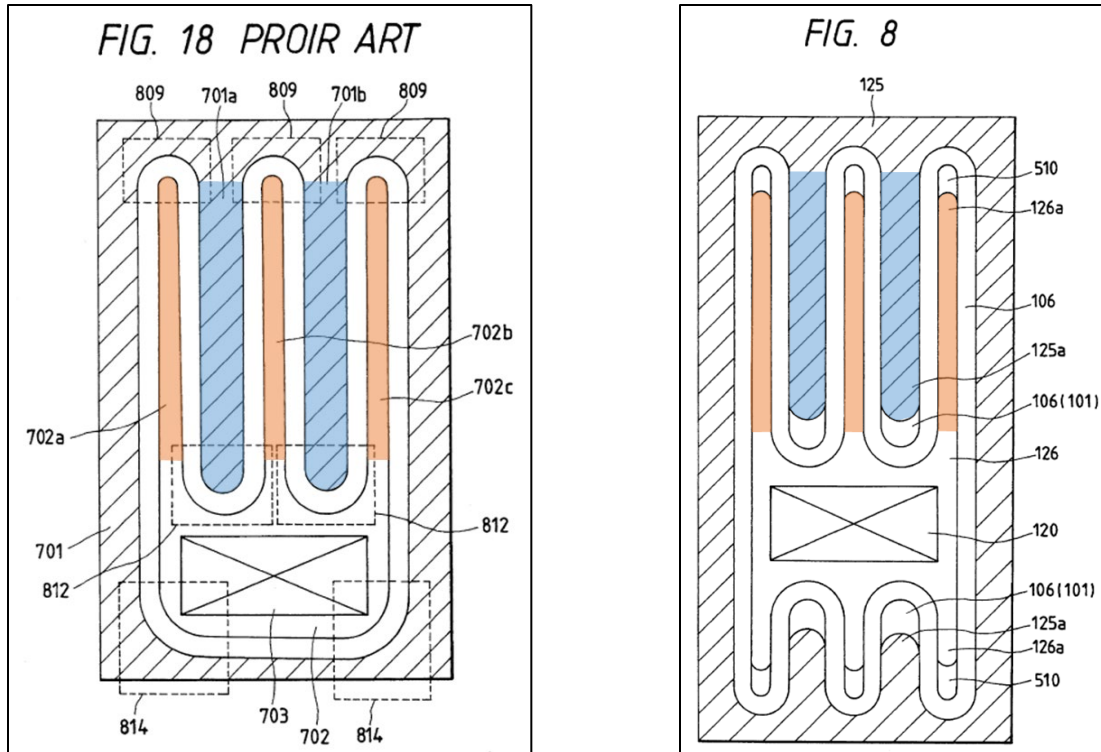
78. A POSA would have understood that Figure 6(b) shows a drain section 126 with **drain electrode 113** and a MIS section 125¹ with a **source electrode 112**. *Id.*, Fig. 6(b), 8:38-59, 1:19-22, 13:47-51, 15:9-16, 16:38-45; *see id.*, 10:66-11:4, Fig. 17. These disclosures explain that the drain section 126 is the output terminal region and the MIS section is the input terminal regions. Figure 8 shows the “overall planar structure” from a top view of the transistor that is partially shown in Figure 6(b), with Figure 8 showing **drain finger electrodes** and **source finger electrodes**. *Id.*, 13:41-44.

¹ Note, that Fujishima’s disclosures interchangeably use “MIS Section” and “MOS Section.”



Fujishima, Figs. 6(b), 8 (annotated). Fujishima explains that the MIS Section 125 (which includes **source electrode 112**) and drain section 126 (which includes **drain electrode 113**) “are juxtaposed in an interdigitated manner.” *Id.*, 15:9-24, Fig. 8; *see also* Ex-1028-1029 (describing and depicting interdigitated structures).

79. Fujishima provides additional context for Figure 8 in its description of a prior art shown in Figure 18. A POSA would have understood that Figures 8 and 18 disclose a similar structure such that the descriptions and explanations relating to Figure 18 are relevant and inform what is shown in Figure 8.



Fujishima, Figs. 18, 8 (annotated). Specifically, Fujishima explains that Figure 18 discloses that an input terminal region 701 and a drain output terminal region 702 “are formed in an interdigitated shape” with **three drain regions 702a to 702c** “formed between adjacent” input terminal regions **701a to 701b**. *Id.*, 1:30-44, Fig. 18, 3:23-34. A POSA would have understood **drain regions 702a to 702c** to be drain finger electrodes and regions **701a to 701b** to be source finger electrodes, especially given their structure shown in the Figures and described in Fujishima. *Id.* Moreover, this same structure is shown in Figure 8 and, thus, a POSA would have understood these disclosures further support that Figure 8 discloses drain finger electrodes interdigitated with source finger electrodes. *Id.*, Fig. 8. Figure 18 shows drain finger ends 809 in an active area of the transistor with high electric field concentrations,

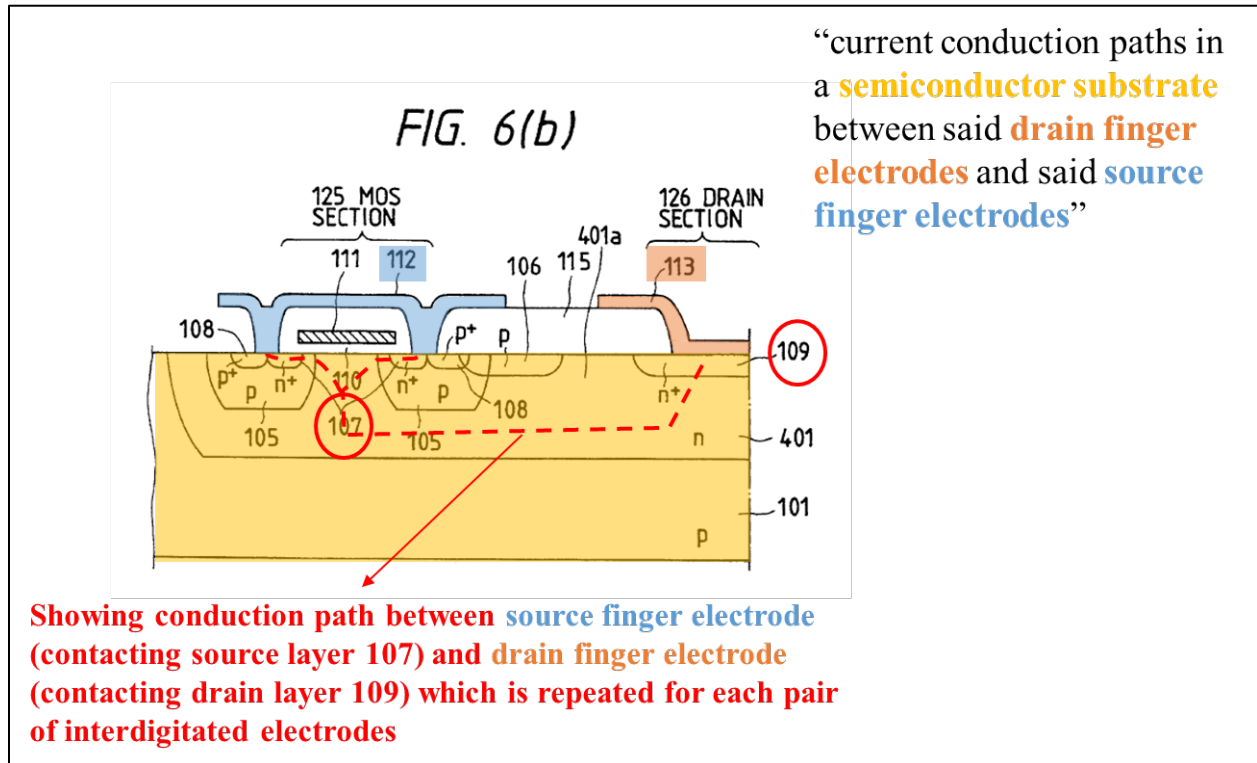
which is similarly shown in Figure 8, which shows a similar structure with drain finger ends in an active area of the transistor, which would also have high electric field concentrations for the same reasons such electric field effect exists in Figure 18.

c. [1b]: current conduction paths in a semiconductor substrate between said drain finger electrodes and said source finger electrodes;

80. It is my opinion that Fujishima discloses or renders obvious [1c] because it discloses current paths through the **substrate** between the **source finger electrodes** to the **drain finger electrodes**. Fujishima discloses a lateral MISFET and a POSA would have understood this MISFET includes current conduction paths between the **drain finger electrodes** and **source finger electrodes**.

81. Specifically, Fujishima discloses a “current path” for charge carriers such as electrons “from the MIS section [125] to the drain section [126].” Fujishima, 5:62-67. As previously discussed, Figure 6(b) shows that MIS section 125 with **source electrode 112** and drain section 126 with **drain electrode 113**, and a POSA would have understood that the electrons flow between these two electrodes on a conduction path. Moreover, Figure 6(b) shows a cross section showing one set of source and drain electrodes—however, Fujishima discloses multiple sets of interdigitated drain and source electrodes and a POSA would have understood that multiple conduction paths exist that have electrons flow on such paths between each

set of interdigitated drain and source fingers. *See* Fujishima, 5:46-48, 10:11-19, 10:43-52, Fig. 6(b).



Fujishima, Fig. 6(b) (annotated).

82. Additional disclosures in Fujishima further support this understanding. For example, Fujishima explains that in the disclosed MISFET, “electrons released from the source layer 107 flow through the surface portion of the **semiconductor substrate**” to the “drain layer 109.” Fujishima, 12:19-40, 10:49-53, 8:59-63, Fig. 6(b). A POSA would have understood that the source layer is the terminal connected to the source electrode (i.e., **source electrode 112** in Fujishima) where electron charge carriers enter the transistor device and the drain layer is the terminal connected to the drain electrode (i.e., **drain electrode 113** in Fujishima) where

electron charge carriers leave the transistor device. A POSA would have further understood that the drain and source layers are doped regions within the **semiconductor substrate** and these layers belong to the same physical substrate material but simply have altered electrical characteristics due to the presence of dopants.² See Fujishima, 2:29-37 (explaining that electron carriers flow horizontally from the source to the drain to be absorbed). A POSA would have further understood that current flow is the opposite direction of electron flow, so Fujishima's disclosure of electron flowing from the **source** to the **drain** also disclose a current conduction path flowing from the **drain** to the **source**. Thus, it is my opinion that a POSA would have understood that Fujishima discloses current conduction paths in the substrate between the **source finger electrodes** and **drain finger electrodes**. See Section XI.A.2.b. A POSA would further have understood that current conduction paths are provided in the substrate for all the interdigitated **drain finger electrodes** and **source finger electrodes**. *Id.*

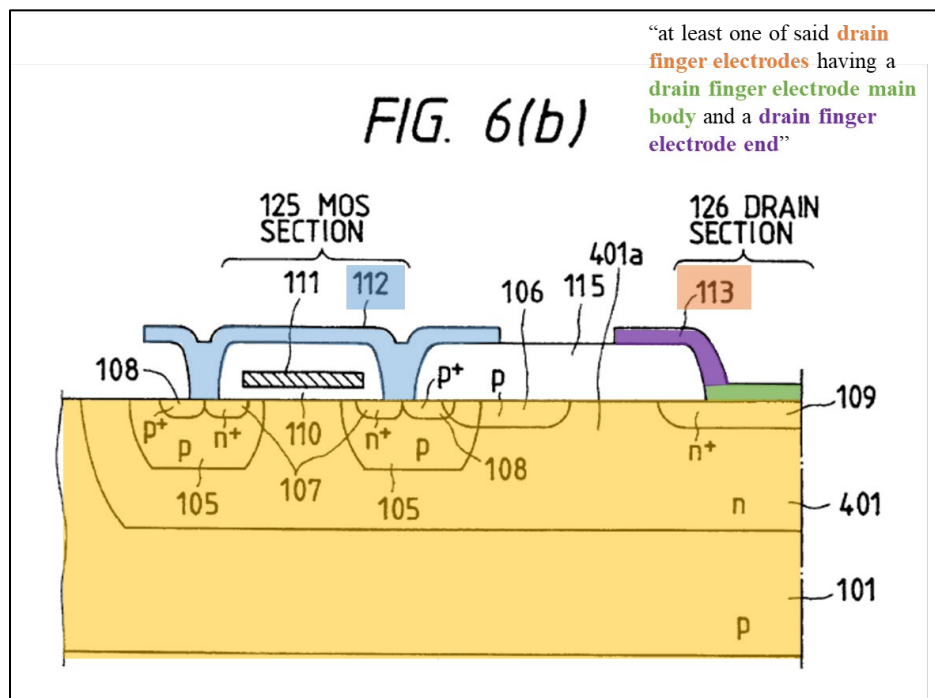
83. **For Ground 1B**, it is also my opinion that a POSA would have found it obvious that Fujishima's MISFETs operate to enable charge carriers to flow over

² The '755 patent explains that the "semiconductor substrate" can be "a III-Nitride material stack, such as a HEMT material stack, silicon, and/or other semiconductor material." '755 Pat., 9:34-37. Fujishima's semiconductor substrate includes semiconductor material with various doped regions, including p-type base layer 105, n⁺-type source layer 107, p⁺-type base contact layer 108, n⁻-type drain layer 109, and n-type well layer 401—all of which are formed in the substrate. Fujishima, Fig. 6(b), 8:41-46, 8:59-62.

current conduction paths in the **semiconductor substrate** between the **source finger electrodes** and **drain finger electrodes**. *See* Section XI.A.2.b. In addition to the suggestions above, a transistor's fundamental purpose is to control the flow of electrical current over a current conduction path between drain and source electrodes. *Id.* Specifically, a gate electrode controls the current flow between the source and drain electrodes based on an applied gate voltage. *Id.*; Ex-1025, 356 (“The [transistor] device consists of an active channel through which electrons (or holes) flow from the source to the drain. The source and drain contacts are ohmic contacts. The conductivity of the channel is modulated by a potential applied to the gate. This results in the modulation of the charge density flowing in the channel. It is important to isolate the gate from the channel so that no current flows into the gate.”). In Fujishima, a POSA would have understood gate electrode 111 to act in this manner and that it is isolated to prevent any current from flowing into the gate. Thus, a POSA would have understood that the MISFETs disclosed in Fujishima, including the one shown in Figures 6(b) and 8, include current conduction paths in the **semiconductor substrate** between the **source finger electrodes** and **drain finger electrodes**. *Id.*

- d. [1c]: at least one of said drain finger electrodes having a drain finger electrode main body and a drain finger electrode end,

84. It is my opinion that Fujishima discloses [1c] because Fujishima discloses a **drain electrode 113** that has a **drain finger main body** and **drain finger electrode end**. See Fujishima, Fig. 6(b).



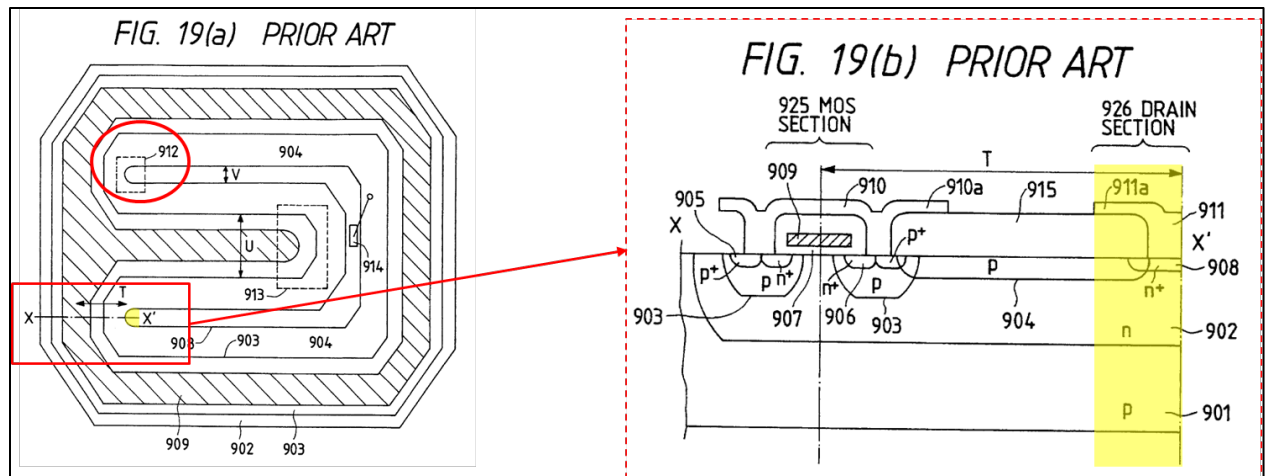
Fujishima, Fig. 6(b) (annotated).

85. A POSA would have understood Figure 6(b) to show that Fujishima’s **drain electrode 113** has two portions: (i) a **drain finger main body** that is situated on **semiconductor substrate**; and (ii) a **drain finger end** that is elevated above the surface of **substrate** such that a portion of the **drain finger end** is not on the same plane (i.e., non-coplanar) as the **drain finger main body**. Fujishima, 8:59-9:2, Figs. 1(b), 6(b); *see id.* Fujishima, 13:37-51. Fujishima explains that the **drain finger end**

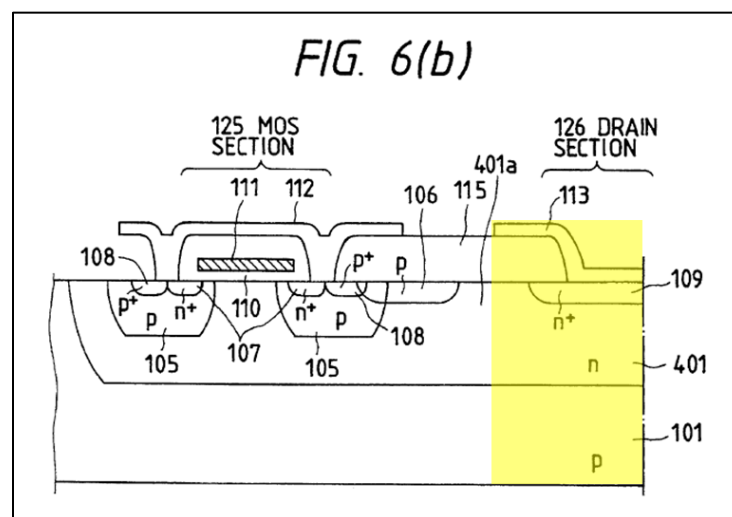
is a field plate portion that projects over the insulating film 115. As Fujishima explains (and a POSA would have understood), this electrode structure alleviates the “concentration of the electric field at the” **drain finger end** enabling the device higher voltage withstanding capability. Fujishima, 8:59-9:2, 14:14-28. For example, Fujishima explains that “it is possible to prevent a breakdown of the drain corner portion due to the concentration of the electric field”.

86. Fujishima also explains that Figures 6(a) and 6(b) provide views of the “drain corner portion 912,” which is the “tip” or “terminating end” of a drain electrode (as shown in a red circle in annotated Figure 19(a) below). Fujishima, 2:65-3:29. Specifically, Figure 6(a) is a “plan view in which a portion of the drain layer, which exhibits a protruding shape in a plan view and is shown as the drain corner portion 912 in FIG. 19(a), is illustrated in enlarged form.” *Id.*, 13:36-51. Figure 6(b) is a “is a cross-sectional view thereof taken along line X--X' in FIG. 6(a).” *Id.* Further, Fujishima explains that this drain corner portion has a high electric field concentration, which a POSA would have understood as a common issue at the time of the alleged invention. *Id.*

87. Figure 19(b) shows a cross section of the drain corner portion of Figure 19(a), including the tip or terminating end of the drain electrode, as indicated by the yellow highlighting below:



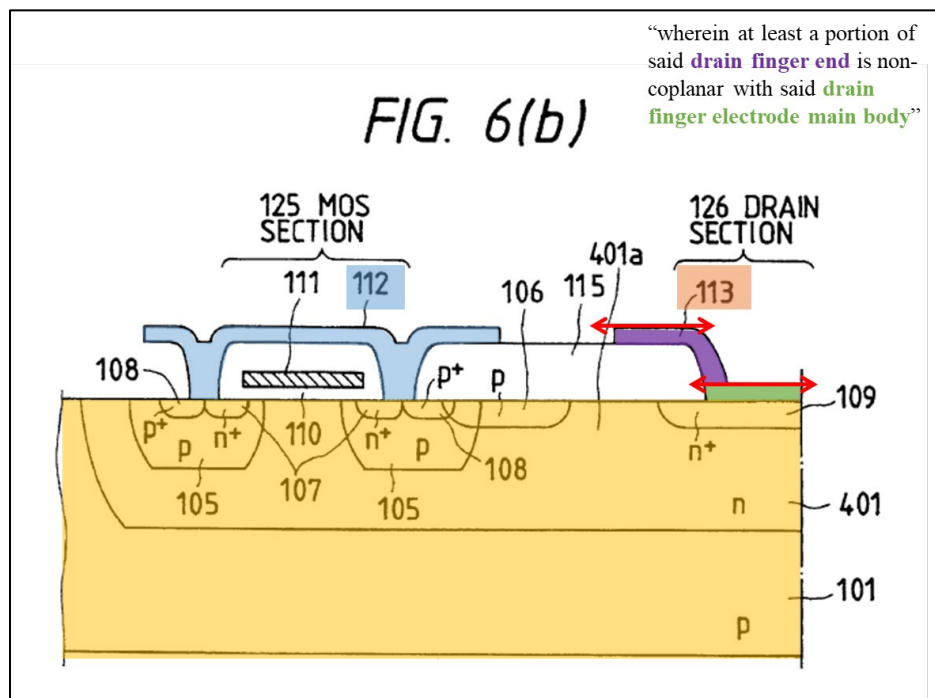
Fujishima, Figs. 19(a), 19(b) (annotated). Figure 6(b), provides a similar cross section showing the drain section 126 that includes drain electrode 113:



Fujishima, Fig. 6(b) (annotated); *see also id.*, Fig. 6(a). Thus, a POSA would have understood that Figure 6(b) shows the “tip” or “terminating end” of a drain electrode 113 where the electric field is known to build up in concentration.

- e. [1d]: wherein at least a portion of said drain finger end is non-coplanar with said drain finger electrode main body.

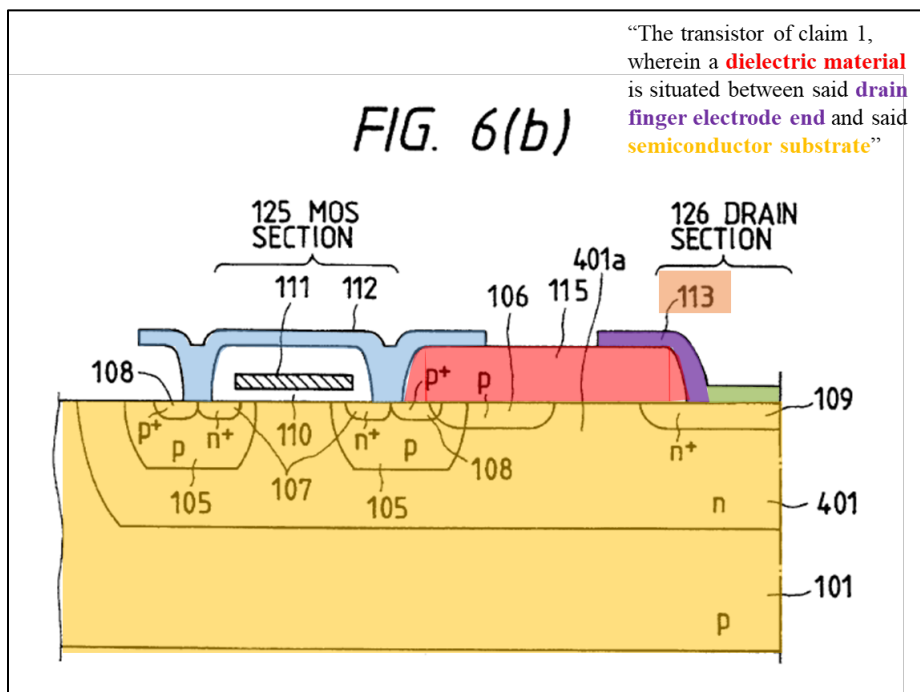
88. It is my opinion that Fujishima discloses [1d] because the **drain finger electrode end** is non-coplanar with the **drain finger electrode main body** for at least the reasons explained for [1c], Section XI.A.2.d. *See* Fujishima, Fig. 6(b).



Fujishima, Fig. 6(b) (annotated). As shown in the Figure, at least a portion of the **drain finger electrode end** is non-coplanar with respect to the **drain finger electrode main body** because the **end** is on a horizontal plane that is not on the same horizontal plane as any part of the **main body**. Fujishima explains that this configuration alleviates the electric field at the drain finger electrode end, as I explained in Section XI.A.1. Fujishima, 12:23-31.

3. **Claim 2 – The transistor of claim 1, wherein a dielectric material is situated between said drain finger electrode end and said semiconductor substrate.**

89. It is my opinion that Fujishima discloses claim 2 because it discloses an **insulating film 115** situated between the **drain finger electrode end** and **semiconductor substrate**. See Fujishima, Fig. 6(b).



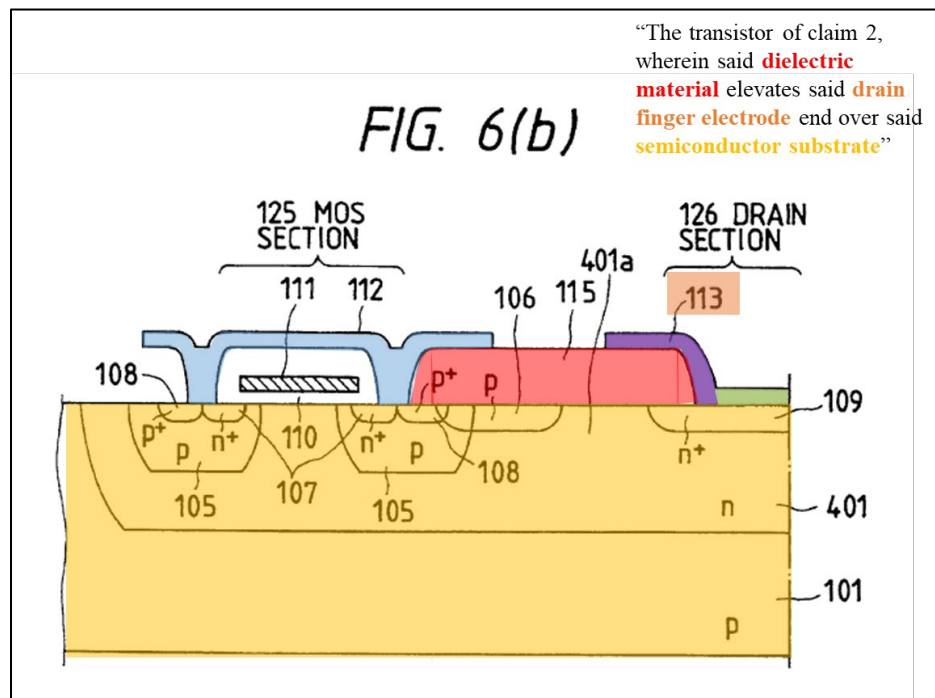
Fujishima, Fig. 6(b) (annotated).

90. As the annotated version of Figure 6(b) above shows, an **insulating film 115** is situated between the **drain finger electrode end** and **substrate**, which alleviates the electric field at the **drain finger electrode end** and provides the device benefits explained for [1c], Sections XI.A.2.c-XI.A.2.d. Fujishima, 8:59-9:2, Figs. 1(b), 6(b). The '755 patent explains that “dielectric material [] includes one or more dielectrics, such as any combination of silicon nitride, silicon oxide, oxynitride, *or*

other insulating material.” ’755 Pat., 10:10-22. Thus, a POSA would have understood that Fujishima’s **insulating film 115** is a dielectric material under the ’755 patent’s description of such a material as any “insulating material.” ’755 Pat., 10:23-29, *see* ’755 Pat., 10:10-22.

4. Claim 3 – The transistor of claim 2, wherein said dielectric material elevates said drain finger electrode end over said semiconductor substrate.

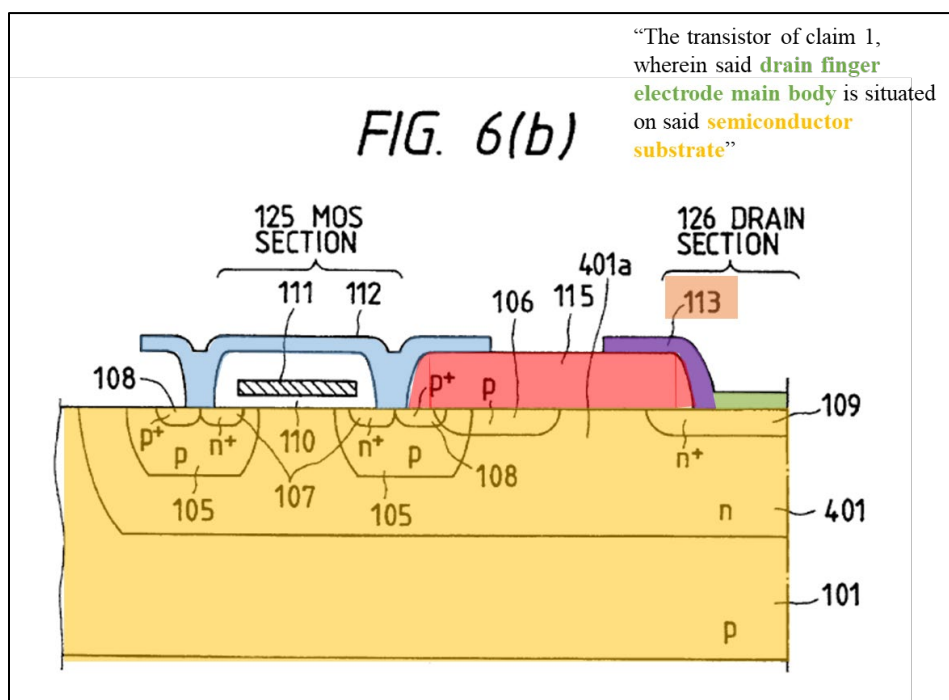
91. It is my opinion that Fujishima discloses claim 3 because it discloses that the **insulating film 115** elevates the **drain finger end** over the **semiconductor substrate**. *See* Fujishima, Fig. 6(b); Sections VII.A.2.c-VII.A.2.d. A POSA would have recognized that Figure 6(b) shows that the **insulating film 115** elevates the **drain finger end** over the **semiconductor substrate**.



Fujishima, Fig. 6(b) (annotated).

5. Claim 4 – The transistor of claim 1, wherein said drain finger electrode main body is situated on said semiconductor substrate.

92. It is my opinion that Fujishima discloses claim 4 because it discloses that the **drain finger main body** is situated on the **semiconductor substrate**. See Fujishima, Fig. 6(b); Sections XI.A.2.c-XI.A.2.d. A POSA would have recognized that Figure 6(b) shows that the **drain finger main body** is situated on the **semiconductor substrate**.



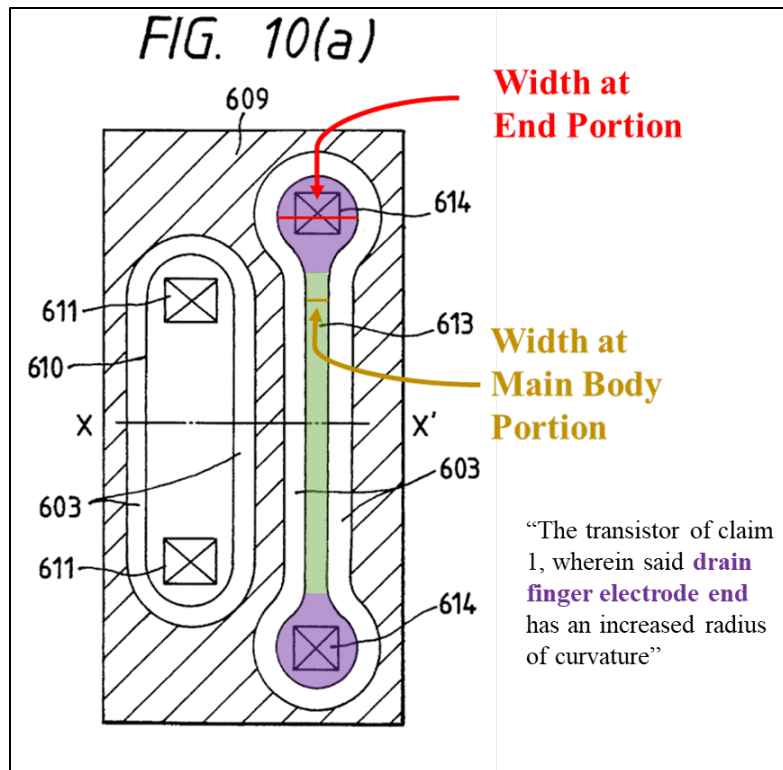
Fujishima, Fig. 6(b) (annotated).

6. Claim 5 – The transistor of claim 1, wherein said drain finger electrode end has an increased radius of curvature.

93. It is my opinion that Fujishima discloses claim 5 because it discloses an ellipsoidal shape for the **drain finger end** that has an increased radius of

curvature resulting in the width of the **drain finger end** being greater than the width of the **drain finger main body**. For **Ground 1B**, it is also my opinion that a POSA would have also found claim 5 obvious in view of Fujishima's disclosures. Additionally, it is also my opinion that a POSA would have been motivated to combine Fujishima's embodiments to achieve claim 5.

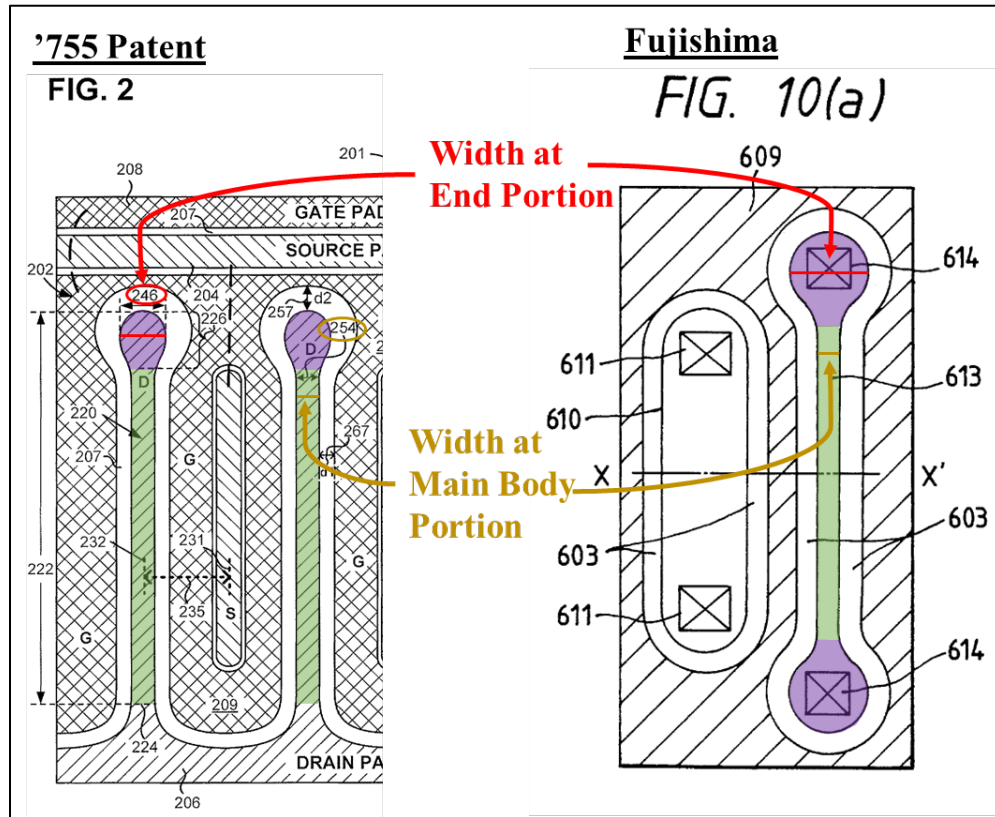
94. First, for **Ground 1A**, Fujishima discloses in its in its "Summary of the Invention" a **drain electrode** structure in which the "**width of a portion where the drain pad opening portion is not formed**" (i.e., the width at the **drain finger electrode main body**) "is set to be smaller than a **width of the drain pad opening portion**" (i.e., the width at the **drain finger electrode end**), and this configuration is further depicted in annotated Figure 10(a) below. Fujishima, 5:14-22, Figs. 10(a), 12; *see* Fujishima, 5:22-36, 17:16-18:6, 6:45-53, 3:3-23, 20:56-21:12, Figs. 12-16.



Fujishima, Fig. 10(a) (annotated). Figures 10(a)-10(b) show that the drain section 613 includes **drain electrode 608** and a POSA would have understood that Fujishima's Figures 10(a) and 12 depict the **drain finger electrode end** and **drain finger electrode main body** of **drain electrode 608**, as indicated by the annotations in the Figure above.

95. A POSA would have understood that Fujishima's disclosures are consistent with the '755 patent's description of the drain finger electrode end having an increased radius of curvature. For example, the '755 Patent explains that a "**drain finger electrode end**[] 226" has an "increased radius of curvature ... resulting in **increased width 246** of curved **drain finger electrode ends 226** relative to **width 254** of [the main body of] **drain finger electrode 220**." '755 Pat., 5:9-13, Fig. 2;

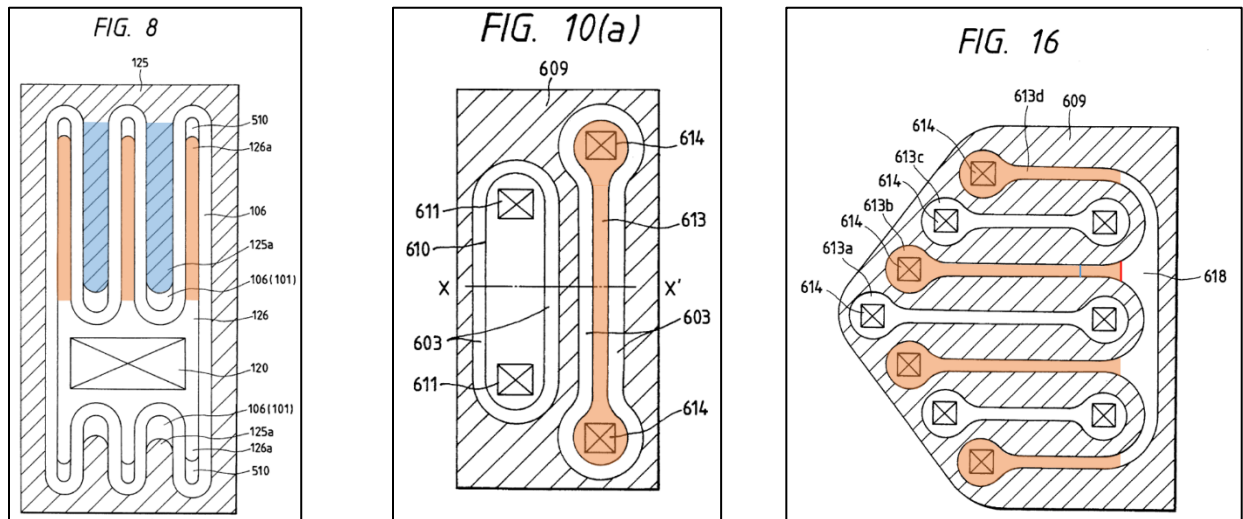
see id., 5:13-16. As explained above and shown below, Fujishima discloses the same structure.



'755 Pat., Fig. 2 (excerpted and annotated); Fujishima, Fig. 10(a) (annotated). The '755 patent defines “**width 254** [] as the width of drain finger electrode 220 just before the transition to curved drain finger electrode end 226.” As explained above, Fujishima discloses the same structure.

96. **Second, for Ground 1B**, it would have been obvious to a POSA to implement the **drain finger electrode end** of Fujishima's **drain electrode 113** that is part of drain section 126 (*see* Section XI.A.2.b) with an ellipsoid shape, as disclosed in, for example, Figures 10(a) and 12. A POSA would have understood

Fujishima discloses various MISFET configurations to improve the overall device, including different configurations options for the shape of the drain finger electrodes including (1) where the width of the electrode finger is consistent throughout (*see* Fujishima, Figs. 7(a), 8-9 and corresponding disclosure); (2) where the finger ends have an ellipsoid shape with a width greater than the main body portion (*see* Fujishima, Fig. 10(a), 12 and corresponding disclosures), and (3) where one side has an connection portion 618 and the other side has ellipsoid shaped finger ends with a width greater than the main body portion (*see* Fujishima, Fig. 16 and corresponding disclosures).



Fujishima, Figs. 8, 10(a), 16 (annotated). Thus, it would have been obvious to a POSA to configure the **drain finger end** of Fujishima's **drain electrode 113** with an ellipsoid shape because doing so would simply implement an option that Fujishima itself discloses, as explained above, and provide an improved device with a higher withstand voltage (*see* Fujishima, 5:14-22, 17:41-54) and reduced electric

field at the **drain finger electrode end**. In fact, a POSA would have understood that a drain finger electrode end with a sharper edge (as shown in Figure 8) promotes a higher electric field as compared to a curved end configuration (as shown in Figures 10(a) and 16), thus this understanding would have motivated a POSA to modify the electrode configuration shown in Figure 8 with one with more curvature, as shown in Figures 10(a) and 16 to reduce the negative electric field effects caused by high electric field concentrations.

97. **Third, for Ground 1B**, it is my opinion that a POSA would have been motivated to combine Fujishima's embodiments so that the drain finger electrode end has an increased radius of curvature. Specifically, a POSA would have been motivated to modify the shape of the **end portion** of Fujishima's **drain finger** shown in Figure 8 with the shape of the **end portion** of **drain finger 613** shown in Figures 10(a) and 12, which show a **drain finger electrode end** with an increased radius of curvature, including for the reasons noted above, such as the benefits of using a curved configuration as opposed to a sharp edge, as well as the benefits Fujishima touts. As I explained in Section VI.B, it was already well known to change the configuration or geometry of the finger-like portions of these electrodes to address electric field issues. A POSA would have further recognized that Fujishima's presentation of multiple options for the shape of the end portion of the drain finger meant that different shapes have different benefits and applications.

Because these options are presented in the same reference, a POSA would have been motivated to (and found it would have been obvious to) modify the Figure 8 embodiment with the Figures 10(a) and 12 embodiments. This similarly supports that a POSA would have had a reasonable expectation of success in making this modification as Fujishima initially explains implementing a MISFET with the shape shown in Figure 8 and then describes implementing the same type of MISFET with the shape shown in Figures 10(a) and 12, including various benefits of this modification, as explained above. Fujishima, 3:38-43, 15:40-59, 17:16-18:6, 18:20-33. Moreover, a POSA would have also had a reasonable expectation of success in making this modification because the modification is simply geometrical and implemented during the design phase, and such types of modifications were well known, as I explained in Section VI.B. Specifically, a POSA would have understood that the geometry and configuration of the electrode structure is based on developing computer-aided designs (CAD), including a mask design layer that corresponds to the electrode structure, and that fabricating the transistor with the electrode structure by implementing the mask design layer created during the planning process. Moreover, modifying the geometry and configuration of an electrode, such as increasing the curvature of the drain finger electrode end, simply requires making a design change to the mask design layer on a computer. The fabrication process

would be implemented in the same manner—i.e., uploading the revised design mask to the fabrication system so it can implement the desired electrode structure.

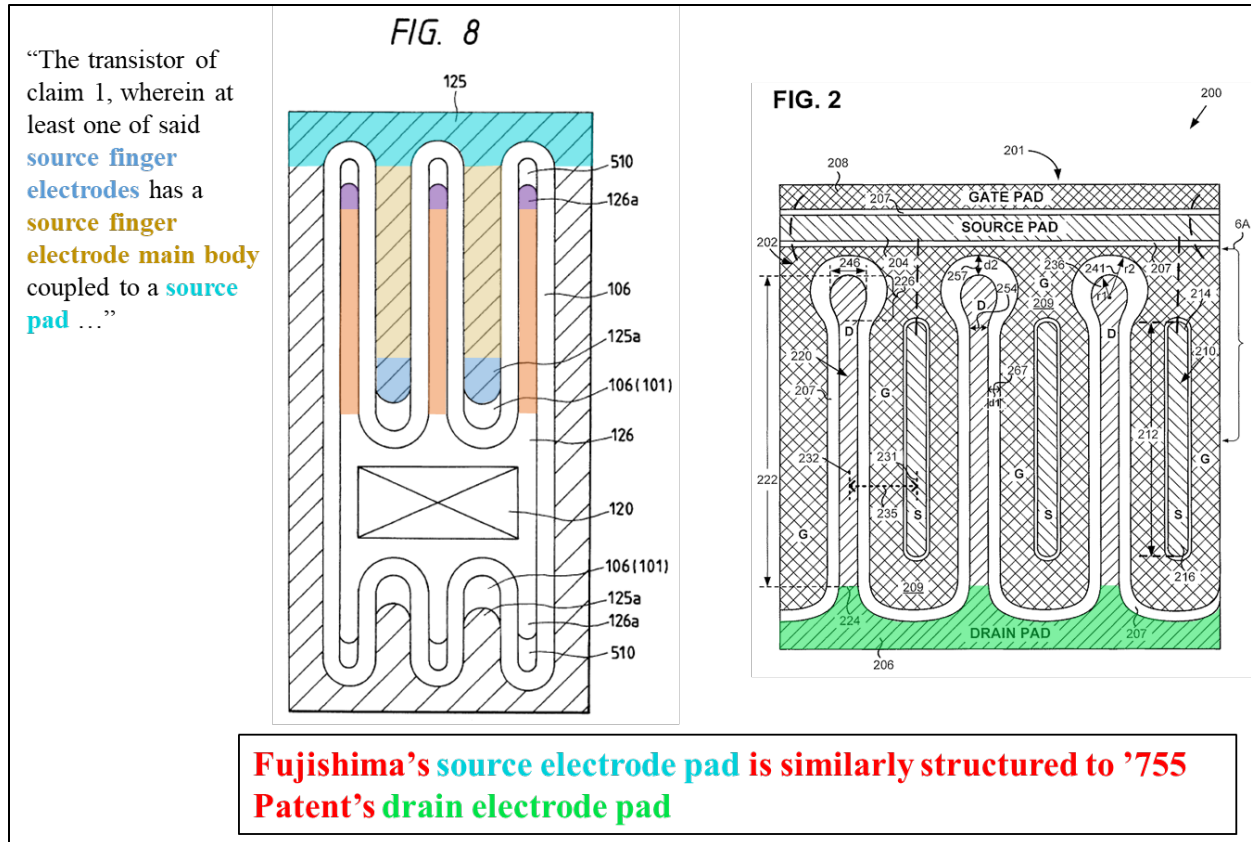
98. Thus, it would have been obvious to a POSA to configure the **drain finger end** of Fujishima's **drain electrode 113** with an ellipsoid shape because doing so would simply combine prior art elements according to known methods (i.e., combining Fujishima's MISFET and ellipsoid shape electrode finger configuration) or substituting one known element for another (i.e., substituting the planar configuration for the ellipsoid shape electrode finger configuration) to yield predictable results (i.e., Fujishima's MISFET with a ellipsoid-shaped drain finger end). Additionally, a POSA would have also found it obvious to do so because it applies a known technique to a known device (i.e., using a ellipsoid-shaped drain finger end to Fujishima's MISFET) and provides an improved device with a higher withstand voltage (*see* Fujishima, 5:14-22, 17:41-54) and reduced electric field at the **drain finger electrode end**—benefits providing a clear teaching, suggestion, or motivation to make the combination.

7. **Claim 6 – The transistor of claim 1, wherein at least one of said source finger electrodes has a source finger electrode main body coupled to a source pad, said drain finger electrode end extending beyond said source finger electrode main body.**

99. **For Ground 1B**, it is my opinion that Fujishima renders obvious claim 6 because it discloses (i) a **source finger electrode** with a main body portion (*see*

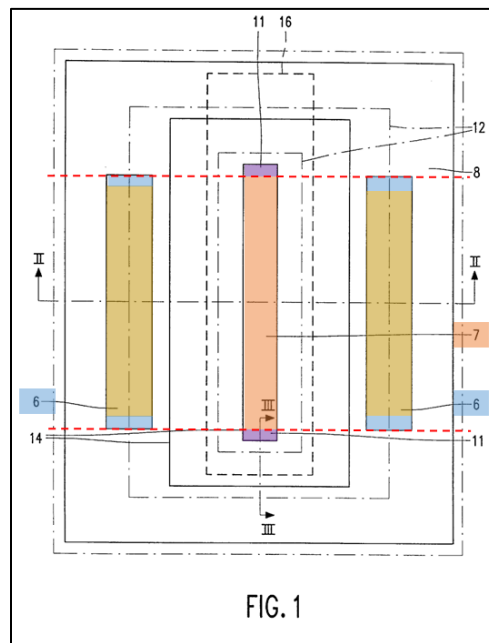
Section XI.A.2.b), which a POSA would have understood to be coupled to a source pad, and (ii) that the **end portion** of Fujishima's **drain finger electrode** (*see id.*) extends past the main body of the **source finger electrode**, as it was well-known at the time of the invention to extend the **end portion** of the **drain finger electrode** beyond the **source finger electrode** main body.

100. First, a POSA would have understood that Fujishima discloses a **source finger electrode** with a **main body portion** connected to a **source pad**, as shown in annotated Figure 8. The '755 patent describes a **source pad** as electrically coupled to the **main body portion** of the **source finger electrodes** and adjacent to the **drain finger electrode ends**. '755 Pat., 4:26-33, 4:64-5:8. Fig. 2. A POSA would have understood that Fujishima's Figure 8 discloses a **source pad** because (i) this portion is electrically coupled to the **main body portion** given that the **source pad** and **main body** are connected, (2) the **source pad** is adjacent to the Fujishima's **drain finger electrode ends**, and (3) the electrode pad structure of the **source pad** is similar to the electrode pad structure disclosed in the '755 patent—specifically the **drain electrode pad**.



Fujishima, Fig. 8 (annotated); '755 Pat., Fig. 2 (annotated). Moreover, a POSA would have understood that the **main body portion** connects to a **source pad** to enable the external circuit access to the **source finger electrodes**, including to components of the “integrated circuit device” that Fujishima's MISFET is a part of. Fujishima, 10:37-42, 11:65-12:3. A POSA would have understood that Fujishima's source pad provides numerous benefits, including providing uniform current distribution across source fingers, providing a low-resistance path to lower parasitic resistance, and offering a centralized, low-inductance point for source fingers to connect that helps manage parasitic inductance.

101. Second, it is my opinion that a POSA would have found it obvious to extend the **end portion** of Fujishima's **drain finger electrode** beyond the **main body portion** of the **source finger electrode** because such a configuration was well known and conventional at the time of the invention. Ludikhuize, Abstract, 4:26-33, Fig. 1; Ex-1021, 144. For example, Figure 1 from Ludikhuize (a patent issued in 1999) shows “**source fingers 6**” that have a **main body portion** coupled to a source pad and a “**drain finger 7**” that has “**tips 11**” that extend past the **source finger electrode**, including the **main body portion**.



Ludikhuize, Fig. 1 (annotated).

102. Additionally, a 2008 IEEE publication similarly shows that the drain finger electrode end extends past the source finger main body. Ex-1021, 144. This publication identifies the “Source fingertip region” in Figure 7. As the figure below

shows, the bottom drain finger electrode has an end portion that extends beyond the end of source finger electrode main body, the latter of which is shown by a red dotted line:

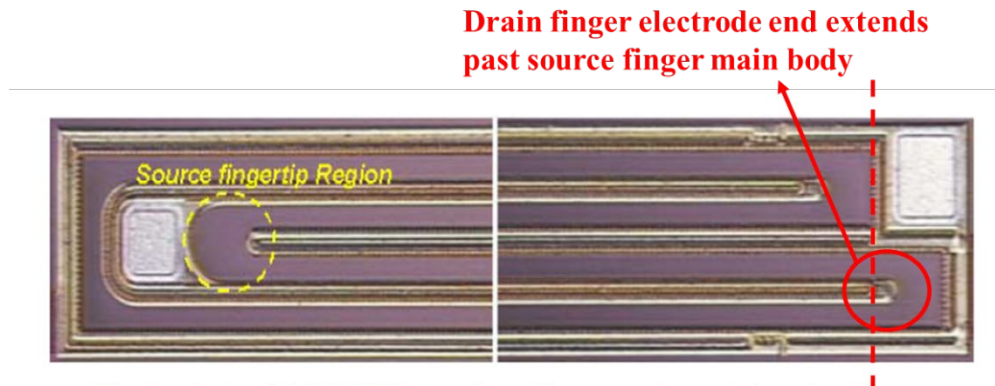
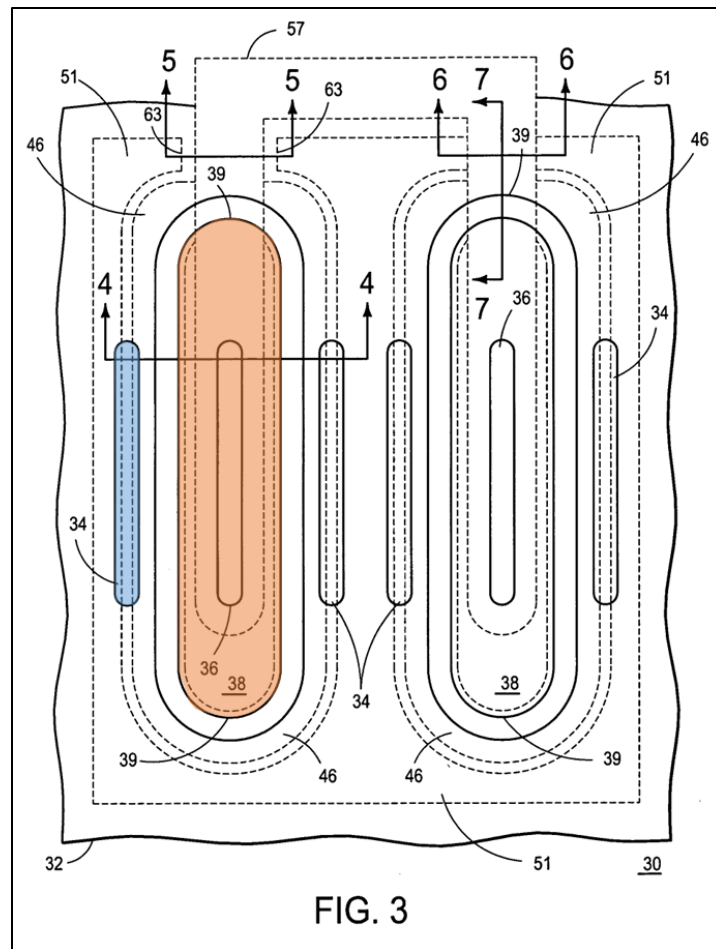


Fig.7 Actual LDMOS top view for experimental evaluations

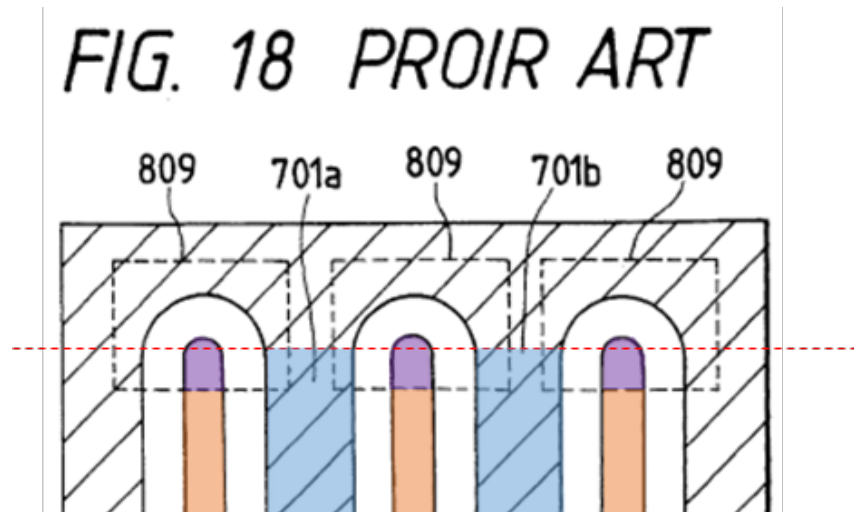
Ex-1021, 144 (yellow annotations in original, red annotations added).

103. Additionally, a 2005 patent publication discloses **drain finger electrodes** longer than the **source finger electrodes**, such that the drain electrodes extend past the source electrodes on both sides. *See* Ex-1041 ¶20 (explaining that Fig. 3 shows drain fingers 39 and source regions 34); Fig. 3 (showing that drain fingers 39 are longer and extend past the source regions 34), 35 (noting that a “further advantage is that the drain finger design is flexible to include long drain fingers), 16-17 (noting that the disclosed “structure according to the present invention eliminates electric field crowding issues associated with fingertip regions”); *see also id.*; ¶¶ 5, 8, 19.



Ex-1041, Fig. 3 (annotated).

104. In fact, Fujishima's own description of the prior art disclose such a configuration:



Fujishima, Fig. 18 (excerpted and annotated). As I explained in Section VI.B, it was already well known to change the configuration or geometry of the finger-like portions of these electrodes to address electric field issues.

105. A POSA would have understood that this combination would have been routine because implementing specific dimensions for electrode fingers (which was well known at the time of the alleged invention) is a simple design change that involves a scaling or length adjustment and can be implemented during the planning phases. *See* Ludikhuize, 4:21-26, 2:36-41 (showing that this configuration was well known). Thus, it is my opinion that a POSA would have found it straightforward with a reasonable expectation of success to modify Fujishima's electrode structure such that the tips of the drain finger electrode extend beyond the main body of the source finger electrode, and such types of modifications were well known, as I explained in Section VI.B. Moreover, a POSA would have also had a reasonable expectation of success in making this modification because the modification is

simply geometrical and implemented during the design phase. Specifically, a POSA would have understood that the geometry and configuration of the electrode structure is based on developing computer-aided designs (CAD), including a mask design layer that corresponds to the electrode structure, and that fabricating the transistor with the electrode structure by implementing the mask design layer created during the planning process. Moreover, modifying the geometry and configuration of an electrode, such as extending the drain finger electrode end, simply requires making a design change to the mask design layer on a computer. The fabrication process would be implemented in the same manner—i.e., uploading the revised design mask to the fabrication system so it can implement the desired electrode structure.

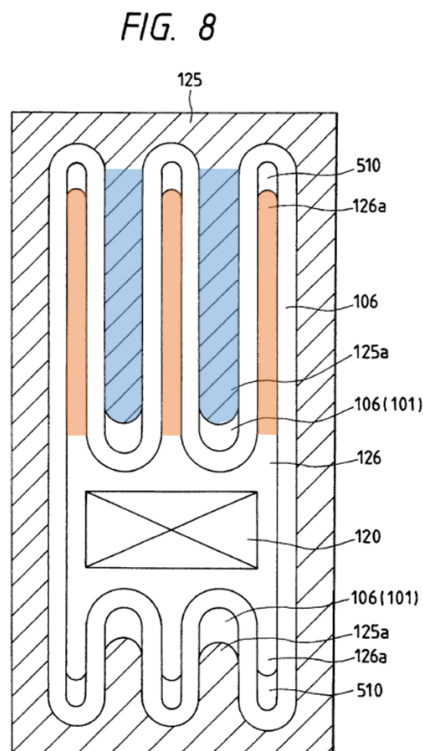
106. A POSA would have been motivated to make this modification because it would have (i) furthered Fujishima's goals of lowering the negative electric field effect at the **end portion** of Fujishima's **drain finger electrode**, which was a known benefit in the art (as I explained above with discussing Ludikhuizen and Hossain 438, citing Ludikhuizen, Abstract, 4:26-33, Figs. 11, 4; Ex-1041, ¶¶20, 35, 16-17, 5, 8, 19, Fig. 3), (ii) increased transistor breakdown voltage, (iii) lowered current convergence and Kirk effect and the drain finger electrode tips, (iv) increased transistor safe operating area, and (iv) decreased manufacturing costs and materials needed.

107. A POSA would also have been motivated to make the modification because it simply combines prior art elements (Fujishima's MISFET and well-known and conventional transistor and electrode configurations to extend the drain finger end portion past the source finger main body) according to known methods to yield predictable results (using longer drain finger electrodes relative to source finger electrodes, as known in the art). This modification is also a simple substitution of one known element (Fujishima's drain finger electrode configuration shown in Figure 8) for another (well-known and conventional drain finger electrode configurations, which are similarly disclosed in Fujishima's description of the prior art in Figure 18) to obtain predictable results (a transistor configuration that reduces the negative electric field effect at the end portions of the drain finger electrode, as well as provides additional benefits noted above). It also uses a known technique (the well-known and conventional configuration to extend the drain finger electrode end) to improve similar devices (transistors disclosed in Fujishima and well known in the art) in the same way (to reduce the negative electric field effect).

8. Claim 7 – The transistor of claim 1, wherein said drain finger electrodes are longer than said source finger electrodes.

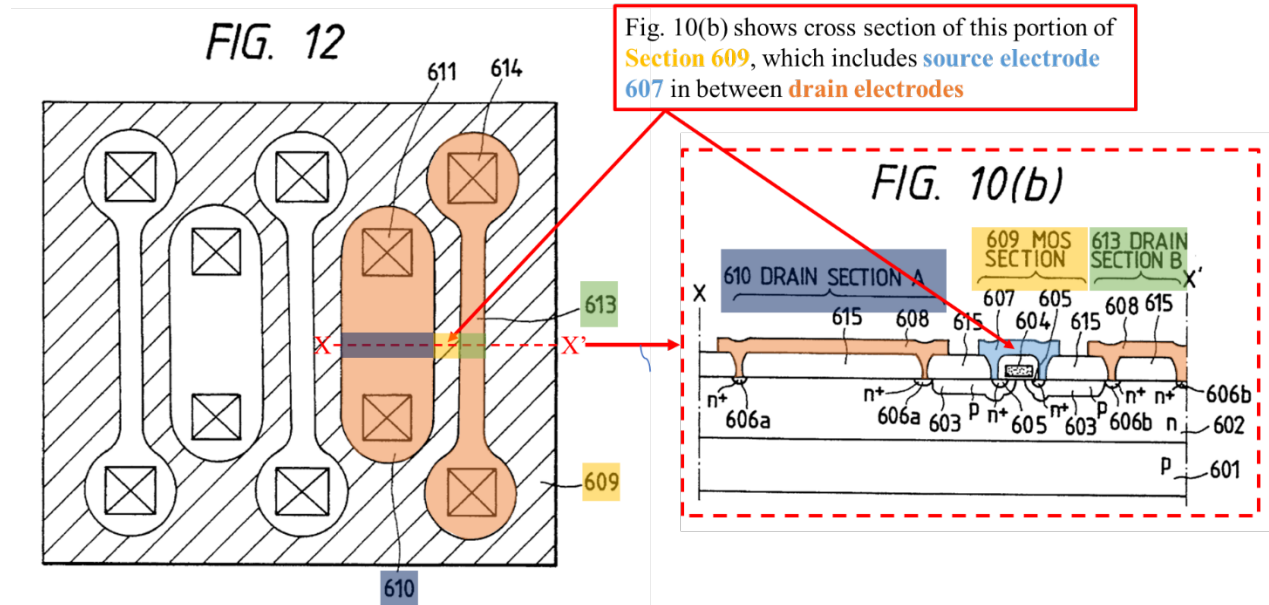
108. **For Ground 1B**, it is my opinion that Fujishima renders obvious claim 7 because a POSA would have found it obvious to configure Fujishima's **drain finger electrodes** so they are longer than the **source finger electrodes**.

109. As I explained for claim 6, Fujishima renders obvious extending the **end portion** of Fujishima's **drain finger electrode** past the **main body portions** of the **source finger electrode**, which a POSA would have understood to apply to each of the interdigitated **drain finger electrodes** and **source finger electrode**. See Section XI.A.7. Moreover, a POSA would have understood that Fujishima's Figure 8 discloses that the **drain finger electrodes** also extend past the **source finger electrodes** on the side opposite of the **end portions** of Fujishima's **drain finger electrodes** (i.e., the bottom side in annotated Figure 8 below):



Fujishima, Fig. 8 (annotated). Thus, it is my opinion that Fujishima discloses or renders obvious that the **drain finger electrodes** are longer than the **source finger electrodes**.

110. Additionally, it is my opinion that a POSA would have found it obvious to extend both tips of the **drain finger electrodes** past both tips the **source finger electrodes** so that Fujishima's **drain finger electrodes** are longer than the **source finger electrodes**. As I explained for claim 5, Section XI.A.6, Fujishima discloses or renders obvious implementing **drain finger electrodes** with two terminating ends, both of which have an ellipsoid shape, as disclosed in Figures 10(a) and 12, with the latter figure depicted below:



Fujishima, Figs. 10(b), 12 (annotated). Figure 10(b) depicts a cross section of Figure 12 showing that the **source electrode 607** is between drain electrodes 608 (with one drain electrode 608 being a part of drain section A 610 and another drain electrode being a part of drain section B 613). Fujishima, Figs. 10(a), 10(b), 12, 16:67-17:15.

111. In such a configuration, a POSA would have understood that it would have been obvious and beneficial to extend the tips on both sides of the **drain finger**

electrodes in drain section B past both tips of the **source finger electrodes** for the reasons as I explained for claim 6 that support extending the drain finger electrode end—and that there would be a reasonable expectation of success in making such a modification. *See* Section XI.A.7; Ludikhuize, Abstract, 4:26-33, Figs. 11, 4; Ex-1021; Ex-1041, ¶¶20, 35, 16-17, 5, 8, 19, Fig. 3. Specifically, a POSA would have had a reasonable expectation of success in making this modification because the modification is simply geometrical and implemented during the design phase. Specifically, a POSA would have understood that the geometry and configuration of the electrode structure is based on developing computer-aided designs (CAD), including a mask design layer that corresponds to the electrode structure, and that fabricating the transistor with the electrode structure by implementing the mask design layer created during the planning process. Moreover, modifying the geometry and configuration of an electrode, such as extending the drain finger electrodes, simply requires making a design change to the mask design layer on a computer. The fabrication process would be implemented in the same manner—i.e., uploading the revised design mask to the fabrication system so it can implement the desired electrode structure.

112. A POSA would have understood that such a modification simply combines prior art elements (Fujishima's drain finger electrode with two terminating ends and well-known and conventional transistor and electrode configurations to

extend the drain finger end portion past the source finger ends on both sides) according to known methods to yield predictable results (using longer drain finger electrodes relative to source finger electrodes, as known in the art). It is also a simple substitution of one known element (Fujishima's drain finger electrode configuration shown in Figure 8) for another (well-known and conventional drain finger electrode configurations, which are similarly disclosed in Fujishima's description of the prior art in Figure 18) to obtain predictable results (a transistor configuration that reduces the negative electric field effect at the end portions of the drain finger electrode, as well as provides additional benefits noted in Section XI.A.7, such as reducing the Kirk effect and current convergence). It also uses a known technique (the well-known and conventional configuration to extend the drain finger electrode ends) to improve similar devices (transistors disclosed in Fujishima and well known in the art) in the same way (to reduce the negative electric field effect).

9. Claim 8 – The transistor of claim 1, wherein said transistor is a high-electron-mobility transistor (HEMT).

113. It is also my opinion that Fujishima discloses or renders obvious claim 8. **For Ground 1A**, Fujishima discloses MISFETs and a POSA, at the time of the alleged invention, would have understood that MISFETs describe a variety of types of well-known and conventional transistors in 2012, including GaN MIS-HEMTs. **For Ground 1B**, a POSA would have motivated to apply Fujishima's teachings to a GaN HEMT device and render obvious claim 8.

114. **For Ground 1A**, the '755 patent explains that “transistor 200” is a “field-effect transistor (FET)” and provides numerous options of the type of specific FET, including a “heterostructure FET (“HFET”) that is implemented as a “high-electron-mobility transistor (HEMT).” ’755 Pat., 3:60-4:3, 2:2-7, 1:28-55. Similarly, Fujishima discloses a “MISFET” (*see* Section XI.A.1), and a POSA would have understood that a Fujishima’s teachings apply to a variety of types of well-known and conventional MISFETs in 2012, including, for example, MIS-HEMTs or, specifically, GaN MIS-HEMTs, as these types of transistors includes an insulating layer between the gate and semiconductor channel. *See* Ex-1015 ¶¶3-4, 24 (describing HEMT as a type of FET and a GaN HEMT with a “MIS structure” (i.e., a MIS-HEMT)); Ex-1016 ¶¶46-47 (describing a GaN HEMT device as a “FET having a MIS (Metal Insulator Semiconductor) structure”); Ex-1017 ¶¶5-10, 42, 56, 87; Ex-1020 (describing a AlGaIn/GaN HEMTs as a FET); Ex-1018, 155; Imada (comparing GaN MIS-HEMTs and HEMTs); Kanamura (disclosing Al-GaN and GaN MIS-HEMTs); Okino (comparing Al-GaN MIS-HEMTs and HEMTs); Ex-1013 ¶¶35-37 (describing a AlGaIn/GaN HEMT with a MIS structure); Ex-1014 ¶¶6-7, 99 (disclosing a GaN/AlGaIn “metal-insulator-semiconductor (MIS) HEMT device[s]”); Beach, 1:65-2:20, 5:17-21 (disclosing a “MISFET constructed using III-nitride materials” that is a GaN HEMT); Ex-1019; Sections VI.A-VI.B (where I

explained that MOSFETs and GaN MIS-HEMTs—both of which were MISFETs—had similar electrode structure); Ex-1020.

115. **For Ground 1B**, it is my opinion that a POSA would have found it obvious to apply Fujishima's concepts specifically to HEMTs (e.g., GaN HEMTs or InGaAs HEMTs), which were well-known and conventional by the time of the alleged invention, including with a transistor structure similar to the one disclosed in Fujishima. For example, a 2006 U.S. patent publication, Sriram, disclosed a GaN HEMT device with interdigitated source and drain electrodes similar to Fujishima's disclosed transistor and that the GaN HEMT has a lateral transistor structure similar to Fujishima's disclosed transistor. Sriram, ¶¶16, 39, Figs. 1 and 5.

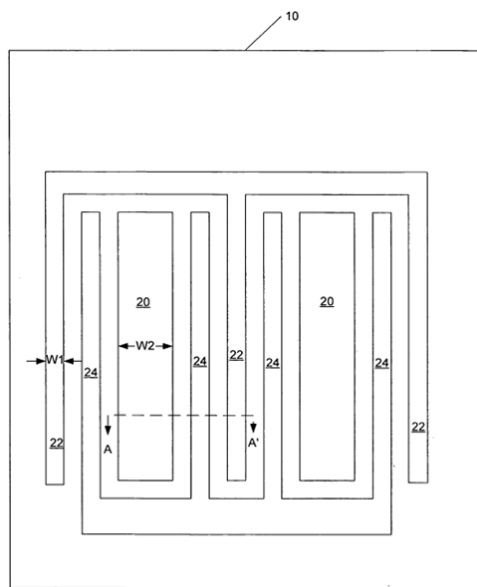


Figure 1

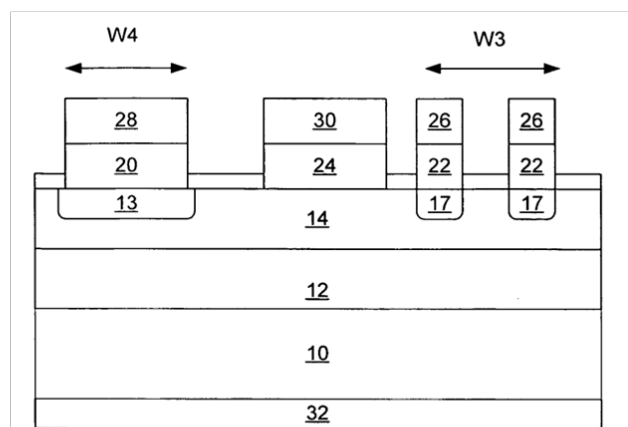


Figure 5

116. As another example, another 2006 U.S. patent publication, Asano, disclosed a InGaAs HEMT with interdigitated source and drain electrodes and that

the InGaAs HEMT has a lateral transistor structure with non-coplanar drain end portion and drain main body similar to Fujishima's disclosed transistor, as explained further in Section XII.B. Asano ¶¶55-56, Figs. 3A, 4B.

117. Moreover, as I explained above, there are numerous publications describing GaN HEMTs. *See* Ex-1010-1017; *see* Section XI.A.1.

118. As I also explained in Sections VI.A-VI.B, MOSFETs and GaN MIS-HEMTs—both of which were MISFETS—had similar electrode structure, further supporting the proposed modification.

119. Thus, it is also my opinion that a POSA would have found this combination obvious given that the concepts from Fujishima relevant to the claimed invention can be generally applied toward lateral transistors with source and drain electrodes, which would include GaN or InGaAs HEMTs.

120. A POSA would have also understood that this combination would have been routine because a POSA would have understood Fujishima's disclosures relied upon for claim 1 (*see* Section XI.A.2) are directed toward the electrode structure of a transistor and such disclosures would be applied similarly to GaN HEMTs or InGaAs HEMTs, which a POSA would understand to have had similar electrode structures—including for the reasons I explained in Sections VI.A-VI.B. Moreover, it was well known at the time of the alleged invention to apply FET configuration techniques to HEMT devices, and such modifications were common and routinely

performed. *See* Ex-1018 (Quay), 70-71 (“parameters of the MISFET are very similar to those of the HEMT”); Ex-1044, 862, 867 (explaining that existing MOSFET models can be used for analyzing and modeling HEMT devices and circuits); Ex-1042, 1, 3-9, 27 (explaining similarities between MOSFETs and GaN HEMTs, as well as explaining how “features of MOSFET circuit models that can be adopted for GaN HEMT modelling”); Ex-1043, 1, 12-13 (explaining that “GaN-HEMTs can be modeled by selected equations from the standard MOSFET” modeling”). This is especially true for features relating to the electrode layout for electric field management purposes, as electric field management around the drain finger electrode for lateral MOSFETs and HEMTs are substantially similar. Moreover, applying Fujishima’s principles in this manner to GaN HEMTs or InGaAs HEMTs would have furthered Fujishima’s goals of providing an improved transistor for high frequency applications, as GaN HEMTs or InGaAs HEMTs provide high electron mobility resulting in “higher saturated electron drift velocities,” which are preferred for high frequency applications (which Fujishima is used for) “because the higher velocity translates to shorter times from source to drain” (i.e., faster switching speeds). Sriram, ¶6. Thus, a POSA would have had a reasonable expectation of success and found it straightforward to incorporate Fujishima’s disclosures relied upon for claim 1 to conventional GaN HEMTs or InGaAs HEMTs.

121. It is also my opinion that a POSA would have been motivated to combine these prior art elements according to known methods (i.e., applying Fujishima's technique of raising drain electrodes to well-known GaN or InGaAs HEMTs) to yield predictable results (i.e., incorporating the benefits touted by Fujishima into GaN or GaAs HEMTs—with HEMTs themselves providing additional benefits over other transistors, such as higher breakdown voltage, high electron mobility, lower on-resistance reducing conduction losses, high power density, high efficiency (e.g., higher power conversion efficiency), lower switching losses, use of smaller passive components, better thermal conductivity, reduced parasitic capacitance, superior low temperature performance, fast switching speeds, among others). *See* Ex-1025, 376-377 (listing numerous advantages of HEMTs); Beach, 1:25-60, 3:59-65 (listing numerous benefits of GaN HEMTs). Using Fujishima in a HEMT would have been obvious because it would be the use of known technique (Fujishima's technique of raising drain electrodes to improve withstand voltage) to improve similar devices (the known HEMT devices) in the same way (using the same Fujishima raised drain electrode technique in HEMT). The combination is also a simple substitution of one known element (Fujishima's drain finger electrode configuration with an elevated end in a MISFET) for another (well known GaN or InGaAs HEMTs with a drain finger electrode end that is flat) to obtain predictable results (a GaN or InGaAs HEMTs with a drain finger electrode

configuration that simply raises the drain finger electrode end portion so that it is elevated). And a POSA would have applied Fujishima to HEMTs with a reasonable expectation of success because applying FET configuration to HEMTs was common and routinely performed as FETs generally share similar working principles and structures, includes those relevant to the '755 patent. Ex-1018 (Quay), 70-71 (“parameters of the MISFET are very similar to those of the HEMT”); Ex-1044, 862, 867 (explaining that existing MOSFET models can be used for analyzing and modeling HEMT devices and circuits); Ex-1042, 1, 3-9, 27 (explaining similarities between MOSFETs and GaN HEMTs, as well as explaining how “features of MOSFET circuit models that can be adopted for GaN HEMT modelling”); Ex-1043, 1, 12-13 (explaining that “GaN-HEMTs can be modeled by selected equations from the standard MOSFET” modeling”). This is especially true for features relating to the electrode layout for electric field management purposes, as electric field management around the drain finger electrode for lateral MOSFETs and HEMTs are substantially similar.

122. A POSA would have found it obvious that Fujishima’s concepts applying to a MISFET would also apply to HEMTs because various types of MISFETs were well known at the time of the alleged invention, including MIS-HEMTs such as GaN or Al-GaN MIS-HEMTs, as I explained above in this section and in Sections VI.A-VI.B.

10. Claim 9 – The transistor of claim 1, wherein said transistor comprises a group III-V transistor.

123. It is also my opinion that Fujishima discloses or renders obvious claim 9 for the reasons noted for claim 8 because (i) Fujishima discloses MISFETs, which a POSA would have understood to include GaN MIS-HEMTs (**Ground 1A**) or, (ii) alternatively, it would have been obvious to apply Fujishima's concepts to GaN or InGaAs HEMTs, which were well-known at the time (**Ground 1B**). *See* Section XI.A.9.

124. As described in the '755 patent, GaN HEMTs (which includes GaN MIS-HEMTs since a GaN MIS-HEMT adds an insulating layer to a GaN HEMT) and InGaAs HEMTs are group III-V transistors. '755 Pat., 2:1-7 ("Gallium nitride or GaN, as used herein, refers to a III-Nitride compound semiconductor"), 1:47-51 ("Group III-V heterostructure field-effect transistors (group III-V HFETs)" include group III-V high electron mobility transistors (group III-V HEMTs), such as "III-Nitride HEMTs"), 4:9-21 ("transistor 200 may be configured to provide a group III-V HFET, such as a III-Nitride HEMT. III-Nitride materials include gallium nitride (GaN) and/or its alloys, such as aluminum gallium nitride (AlGaN), indium gallium nitride (InGaN), and aluminum indium gallium nitride (AlInGaN)"). Foundational textbooks also explain this concept of Group III-V transistors, including that "compound semiconductors are also denoted by the position of the atoms in the

periodic chart, e.g., GaAs, AlAs, InP are called III-V (three-five) semiconductors.”

Ex-1025, 6, 49-52, 540-41.

125. Thus, for **Ground 1A**, a POSA would have understood that Fujishima’s disclosure of GaN MIS-HEMTs, as explained in Section XI.A.9, also discloses a group III-V transistor.

126. Additionally, for **Ground 1B**, a POSA would have understood that Fujishima rendering obvious the application of Fujishima’s concepts to GaN HEMTs also renders obvious applying Fujishima’s concepts to a group III-V transistor. It is also my opinion that a POSA would have been motivated to combine these prior art elements (i.e., Fujishima’s concepts and GaN HEMTs) and would have had a reasonable expectation of success making the combination for the reasons I explained in Section XI.A.9.

11. Independent Claim 10

a. [10pre]: A transistor comprising:

127. If the preamble is limiting, it is my opinion that Fujishima discloses [10pre] for the reasons I explained for [1pre]. *See* Section XI.A.2.a.

b. [10a]: drain finger electrodes interdigitated with source finger electrodes;

128. It is my opinion that Fujishima discloses [10a] for the reasons I explained for [1a]. *See* Section XI.A.2.b.

- c. **[10b]: a gate region configured to control current conduction in a semiconductor substrate between said drain finger electrodes and said source finger electrodes;**

129. It is my opinion that Fujishima discloses or renders obvious [10b] for the reasons I explained for [1b]. *See* Section XI.A.2.b. Fujishima discloses or renders obvious “current conduction in a semiconductor substrate between said drain finger electrodes and said source finger electrodes” for the reasons I stated in Section XI.A.2.b.

130. Moreover, a POSA would have understood that Fujishima discloses a gate region because it discloses a “gate electrode.” Fujishima, Claim 1, 8:46-49, 3:61-63, 4:29-34, Fig. 6(b). Fujishima further explains that electrons flow from the source to the drain when voltage is applied to the gate electrode. *Id.*, 2:29-37. A POSA would have understood that Fujishima’s gate electrode controls the conduction between the drain and source electrodes, including based on the magnitude of the voltage applied—i.e., a higher voltage results in more electron flow and higher conduction—which is consistent with Fujishima’s own disclosures. *See* Fujishima, 2:29-37; Beach 1:61-67, 5:29-35 (describing a MISFET and noting that the “gate contact [] controls the conduction channel between the two ohmic contacts”).

- d. **[10c]: at least one of said drain finger electrodes having a drain finger electrode end and a drain finger electrode main body,**

131. It is my opinion that Fujishima discloses [10c] for the reasons I explained for [1c]. *See* Section XI.A.2.d.

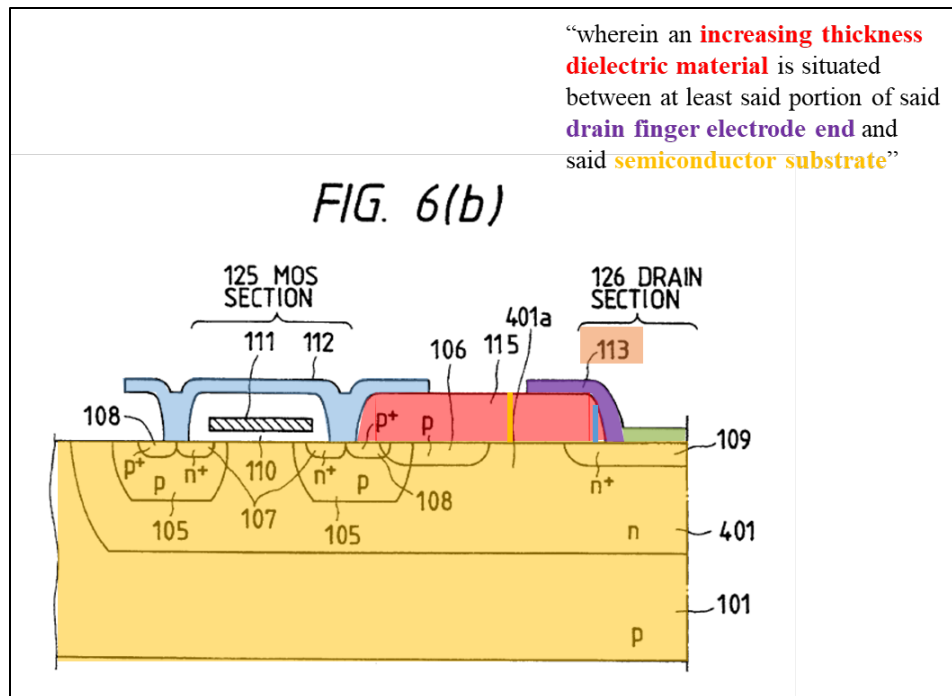
- e. **[10d] wherein at least a portion of said drain finger end is non-coplanar with said drain finger electrode main body;**

132. It is my opinion that Fujishima discloses [10d] for the reasons I explained for [1d]. *See* Section XI.A.2.e.

- f. **[10e]: wherein an increasing thickness dielectric material is situated between at least said portion of said drain finger electrode end and said semiconductor substrate.**

133. It is my opinion that Fujishima discloses [10e] for at least the reasons explained for claim 2. *See* Section XI.A.3. Fujishima discloses “wherein ... a dielectric material is situated between at least said portion of said drain finger electrode end and said semiconductor substrate” for the reasons I stated in Section XI.A.3.

134. A POSA would have understood that Fujishima discloses that the **dielectric material** has an “increasing thickness” because the thickness of Fujishima’s **insulating film 115** increases from its outer edges to the center, as indicated by annotated Figure 6(b) below:



Fujishima, Fig. 6(b) (annotated). The thickness of **insulating film 115** shown at the blue line is less than the thickness of the **film** shown at the yellow line.

- 12. Claim 11 – The transistor of claim 10, wherein said increasing thickness dielectric material elevates said drain finger electrode end over said semiconductor substrate.**

135. It is my opinion that Fujishima discloses claim 11 for the reasons I explained for [10e] and claim 3. *See* Sections XI.A.11.f, XI.A.4.

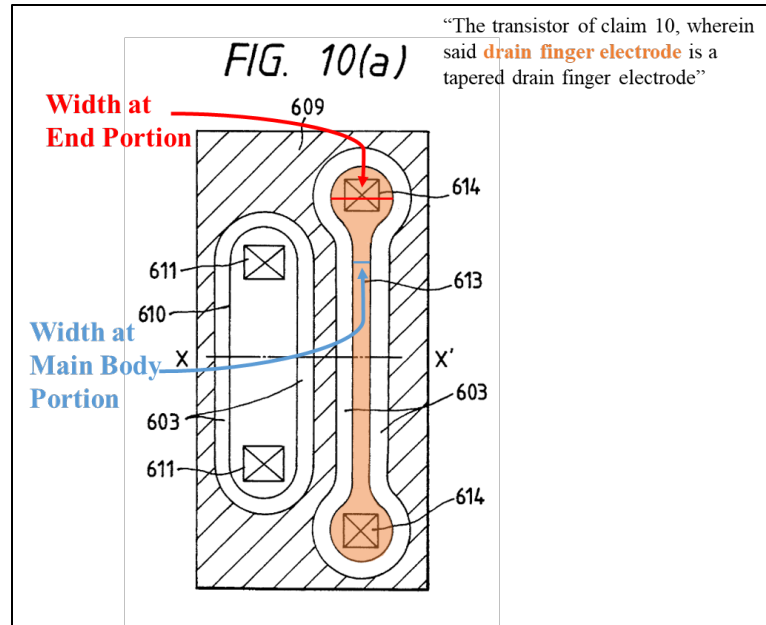
- 13. Claim 12 – The transistor of claim 10, wherein said drain finger electrode end is substantially an ellipsoid.**

136. It is my opinion that Fujishima discloses claim 12 for the reasons I explained for claim 5. *See* Section XI.A.6.

14. Claim 13 – The transistor of claim 10, wherein said drain finger electrode is a tapered drain finger electrode.

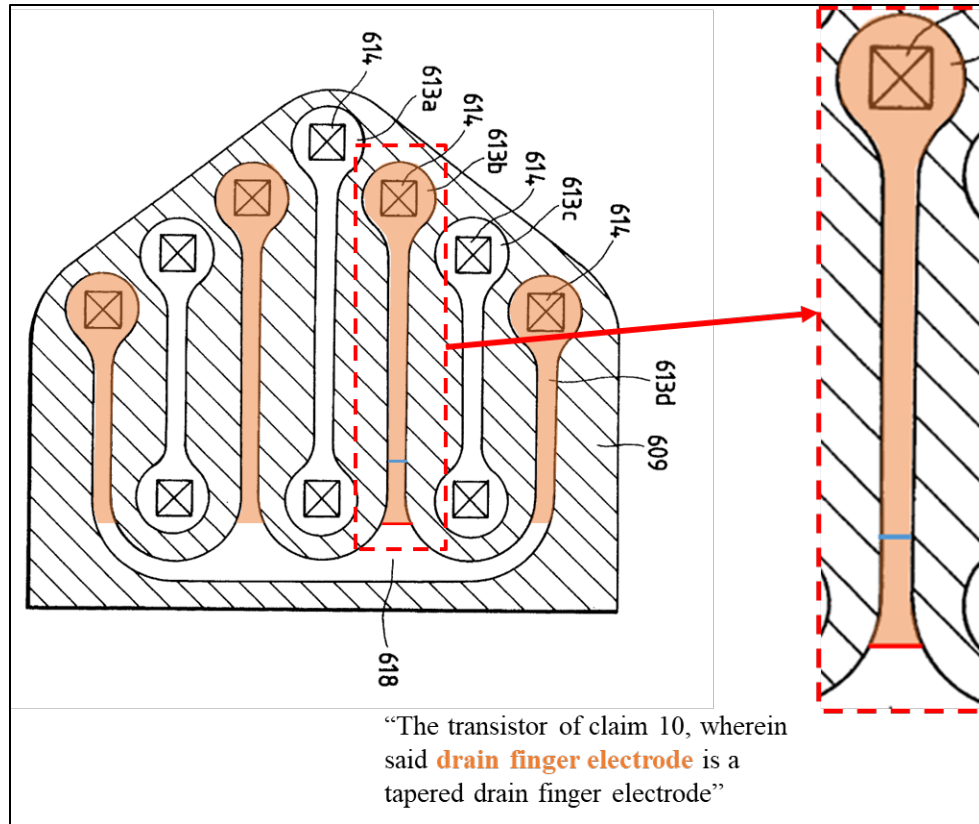
137. **For Ground 1A**, it is my opinion that Fujishima discloses claim 13 because Fujishima's **drain finger electrode** is tapered. **For Ground 1B**, it is my opinion that a POSA would have found claim 13 obvious in view of Fujishima's disclosures, especially in view of the applicant of the '755 patent admitting that this limitation recites subject matter that was prior art at the time of the alleged invention. *Id.* **Also for Ground 1B**, it is my opinion that a POSA would have been motivated to combine Fujishima's embodiments to achieve claim 13.

138. **First, for Ground 1A**, a POSA would have understood that Fujishima discloses a **drain finger electrode** structure that incorporates tapering in two ways. For the first way, Fujishima discloses a **drain electrode** structure in which the “**width of a portion where the drain pad opening portion is not formed**” “is set to be smaller than a **width of the drain pad opening portion**” and this configuration is further depicted in annotated Figure 10(a) below. Fujishima, 5:19-22



Fujishima, Fig. 10(a) (annotated). A POSA would have understood this figure as showing that the **drain finger electrode** tapers from a top portion (i.e., the portion where the red line is located) to a smaller width in the middle of the electrode (i.e., the portion where the blue line is located).

139. For the second way, Fujishima discloses a **drain electrode** structure that incorporates tapering in a different manner. As shown in annotated Figure 16 below, this structure has a smaller width near the center of the **electrode** (as shown by the blue line) relative to a width of the **electrode** near the connection 618 (as shown by the red line).



Fujishima, Fig. 16 (annotated). A POSA would have understood this structure as showing that the **drain finger electrode** tapers from an end portion away near connection 618 (i.e., the portion where the red line is located) to a smaller width in the middle of the electrode (i.e., the portion where the blue line is located). Thus, it is my opinion that Fujishima discloses claim 13.

140. **Second, for Ground 1B**, it would have been obvious to a POSA to implement Fujishima’s **drain electrode 113** (see Section XI.A.2.b) with a tapered configuration because this type of modification was well known in view of the ’755 patent applicant’s admissions that such feature was prior art at the time of the alleged invention. The ’755 patent explains that “tapered source and drain finger designs are

described in [Beach],” which is a U.S. patent that issued in 2008—four years before the time of the invention. ’755 Pat., 8:43-55. The ’755 patent also explained that tapered configurations were conventional, known, and provided “further improvements in high current carrying transistors,” such as “higher breakdown voltages and lower ON-resistance.” *Id.* I have been advised by counsel that these statements constitute applicant admitted prior art and that such admissions can supply missing claim limitations that were generally known in the art prior to the invention or demonstrate the knowledge of a POSA at the time of the invention. This is consistent with my understanding of the art at the time of the alleged invention, in that tapered electrode configurations were well known and conventional, including how it is disclosed in Beach.

141. As shown in annotated Figure 3 below, Beach discloses drain finger electrodes in which “each finger taper[s] from a base to a tip thereof, [with] the base being wider than the tip”:

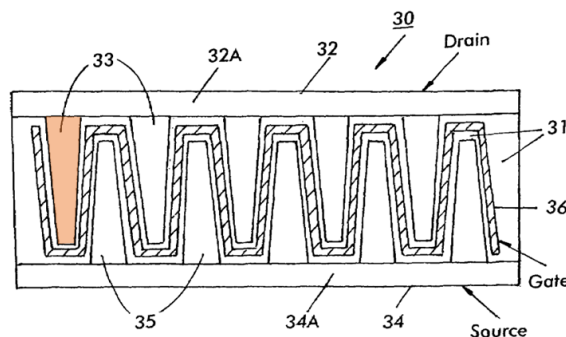


FIG. 3

Beach, Claim 1, Abstract, 5:57-6:11. Beach explains that “tapered finger design balances current flow in the electrode fingers to reduce device resistance while permitting a more compact construction.” *Id.*, Abstract. Thus, it is my opinion that Fujishima, in view of Applicant’s admissions, renders obvious tapered drain finger electrodes and claim 13, as a POSA would have found it obvious to implement Fujishima’s **drain electrode 113** with a tapered configuration, in view of the applicant’s admission and Beach’s disclosures.

142. A POSA would have found this modification to be routine because implementing specific geometry for electrode fingers (i.e., tapered drain finger electrode, as the applicant admitted prior art discloses above) is a simple design change of making the base width larger than the tip width and can be implemented during the planning phases. As I explained in Section VI.B, it was already well known to change the configuration or geometry of the finger-like portions of these electrodes to address electric field issues. Thus, it is my opinion that a POSA would have found it straightforward with a reasonable expectation of success to modify Fujishima’s electrode structure such that the drain finger electrode was tapered, as the applicant admitted prior art discloses. Moreover, a POSA would have had a reasonable expectation of success in making this modification because the modification is simply geometrical and implemented during the design phase, as such types of modifications were well known, as I explained in Section VI.B.

Specifically, a POSA would have understood that the geometry and configuration of the electrode structure is based on developing computer-aided designs (CAD), including a mask design layer that corresponds to the electrode structure, and that fabricating the transistor with the electrode structure by implementing the mask design layer created during the planning process. Moreover, modifying the geometry and configuration of an electrode, such as tapering the drain finger electrode, simply requires making a design change to the mask design layer on a computer. The fabrication process would be implemented in the same manner—i.e., uploading the revised design mask to the fabrication system so it can implement the desired electrode structure.

143. A POSA would have been motivated to make the modification to (i) increase device power rating, (ii) decreasing device dimensions and permit a more compact device construction, (iii) reducing device resistance and balance current flow, and (iv) decreases power loss due to current variation across the electrode finger. Beach, Abstract, 3:1-8, 4:6-33, 4:53-64, 6:1-11, 6:24-48, 6:57-61. Beach explains that the “tapered finger design balances current flow in the electrode fingers to reduce device resistance while permitting a more compact construction,” “lowers on-resistance,” “improve[s] resistance-area product,” balances the current flow, reduces size without sacrificing rating, “improve[s] power efficiency” and reduces

power loss, and “prevent[s] high electric fields from being formed in particular locations (i.e., the electrode finger tips). *Id.*

144. A POSA would have understood that this combination simply combines prior art elements (Fujishima’s and the applicant admitted prior art transistor and electrode configurations) according to known methods to yield predictable results (using tapered drain finger electrodes). It is also a simple substitution of one known element (Fujishima’s drain finger electrode configuration shown in Figure 8) for another (the applicant admitted prior art’s tapered drain finger electrode configuration in Figure 3) to obtain predictable results (a configuration of the drain finger electrode of a transistor that reduces the negative electric field effect). It also uses a known technique (the applicant admitted prior art’s tapered drain finger electrode configuration) to improve similar devices (transistors disclosed in Fujishima and the applicant admitted prior art) in the same way (to reduce the negative electric field effect). *Id.*

145. **Third, for Ground 1B**, it is my opinion that a POSA would have been motivated to combine embodiments in Fujishima in a manner that discloses this limitation. Specifically, a POSA would have been motivated to modify the shape of Fujishima’s **drain finger** shown in Figure 8 with the shape of **drain finger** shown in Figure 10(a) or Figure 16—both of which include tapered electrode configurations, as explained above. A POSA would have recognized that Fujishima’s presentation

of multiple options for the shape of the end portion of the drain finger meant that different shapes have different benefits and applications. Moreover, because these options are presented in the same reference, a POSA would have been motivated to (and found it would have been obvious to) modify the Figure 8 embodiment with the Figure 10(a) embodiment or Figure 16 embodiment, as well as that such a modification would have had a reasonable expectation of success. *Id.* A POSA would have had a reasonable expectation of success in making this modification because the modification is simply geometrical and implemented during the design phase. Specifically, a POSA would have understood that the geometry and configuration of the electrode structure is based on developing computer-aided designs (CAD), including a mask design layer that corresponds to the electrode structure, and that fabricating the transistor with the electrode structure by implementing the mask design layer created during the planning process. Moreover, modifying the geometry and configuration of an electrode, such as tapering the drain finger electrode, simply requires making a design change to the mask design layer on a computer. The fabrication process would be implemented in the same manner—i.e., uploading the revised design mask to the fabrication system so it can implement the desired electrode structure.

146. Thus, it is my opinion that it would have been obvious to a POSA to configure Fujishima's **drain electrode 113** with a tapered shape because doing so

would simply combine prior art elements according to known methods (i.e., combining Fujishima's MISFET and tapered shape electrode finger configuration) or substituting one known element for another (i.e., substituting the planar configuration for the tapered shape electrode finger configuration) to yield predictable results (i.e., Fujishima's MISFET with a tapered-shaped drain finger electrode). Additionally, a POSA would have also found it obvious to do so because it applies a known technique to a known device (i.e., using a tapered-shaped drain finger electrode in Fujishima's MISFET) and provides an improved device with a higher withstand voltage and reduced electric field—benefits providing a clear teaching, suggestion, or motivation to make the combination.

15. Claim 14 – The transistor of claim 10, wherein said transistor is a high-electron-mobility transistor (HEMT).

147. It is my opinion that Fujishima discloses claim 14 for the reasons explained for claim 8. *See* Section XI.A.9.

B. Ground 1C: Fujishima and Ludikhuize Render Obvious Claims 6-7

148. Claims 6 and 7 are directed to a drain finger electrode longer than the source finger electrode (claim 7) and that the end portions of the drain finger electrode extends beyond the source finger electrode main body (Claim 6). It is my opinion that Ludikhuize discloses both limitations and a POSA would have found it obvious to combine Fujishima and Ludhikhuize.

1. Ludikhuize

149. Ludikhuize relates generally to transistors (Ludikhuize, 3:1-15, 3:46-54, Claim 1), identifying a double-diffused MOSFET as one example. *Id.*, 3:15-17. This is similar to the '755 patent and Fujishima, both of which are generally directed to a broad category of transistors and disclose MOSFETs as a specific example. '755 Pat., 3:64-65 (also disclosing MOSFETs); Fujishima, 7:5-7 (same). Ludikhuize strives to configure transistors to prevent electrical “breakdown [that] arises at the end faces of the drain fingers owing to current convergence at the ends of the fingers.” *Id.*, Abstract, Fig. 1. To address electrical breakdown, Ludikhuize configures its transistor so the “source fingers are shorter than the drain fingers,” as Figure 1 shows:

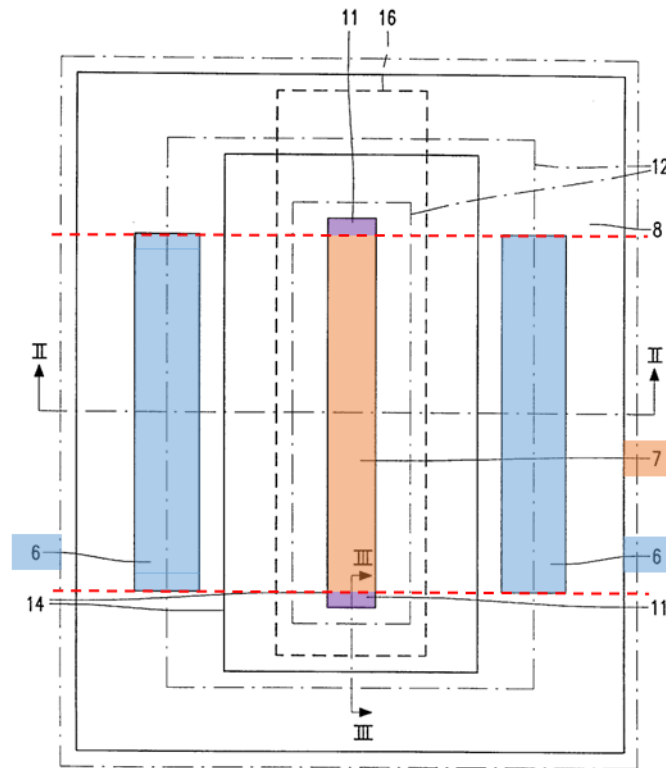
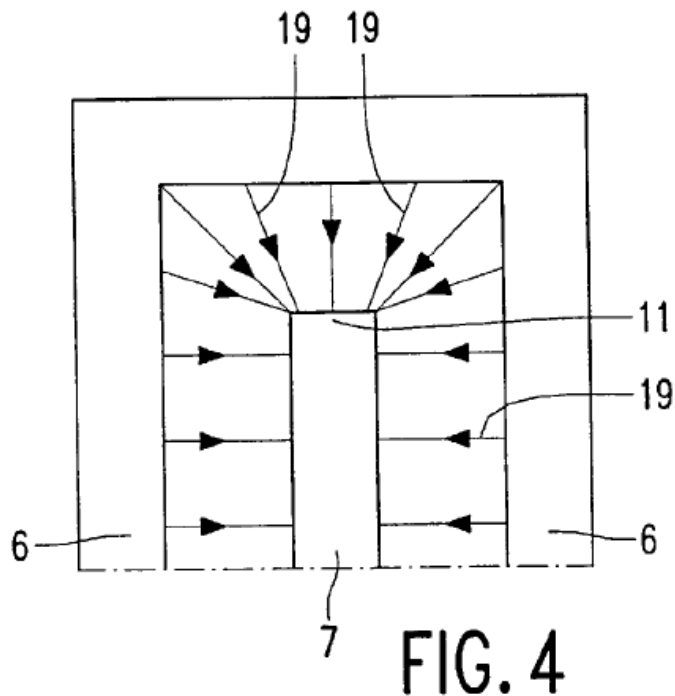


FIG. 1

Ludikhuize, Fig. 1 (annotated). Ludikhuize explains that having longer drain fingers than source fingers increases the safe operating area of the transistor by reducing the Kirk effect and current convergence (and negative electric field effect) at the **tips** of the **drain finger electrodes**. Ludikhuize, Abstract, 4:26-33, Figs. 11, 4.



Ludikhuize, Fig. 4. Figure 4 shows the concentration of the electric field at the end portions 11 of drain finger 7, and that the concentration is higher at the end portions.

2. General Motivations to Combine

150. It is my opinion that a POSA would have found it obvious to combine Fujishima and Ludikhuize, which disclose complementary systems and methods for configuring transistors and addressing similar problems: improving overall transistor performance by alleviating negative electric field effects within the transistor. A POSA would have thus considered Ludikhuize when reading the disclosure of Fujishima, including to improve on Fujishima's disclosures.

151. As I explained in Section XI.A.1., Fujishima relates to the configuration of MISFETs, which describe a broad category of transistors at the time of the alleged

invention. As I explained in Section XI.A.1, Fujishima discloses lateral power transistors with interdigitated drain finger electrodes and source finger electrodes and describes various transistor configuration options for the source and drain finger electrodes. *See* Section XI.A.1. As I also explained in Section XI.A.1, these various configurations improve the overall transistor device, including by minimizing the negative electric field effect at the ends of the drain electrode.

152. Similarly, as I explained in Section XI.B.1, Ludikhuize discloses “lateral” transistors with “interdigitated source/drain configuration.” Ludikhuize, Abstract. Additionally, a POSA would have understood that Ludikhuize discloses configuration options for transistors that help prevent electrical breakdown due to an electric field concentration at the drain finger electrode end portions. Specifically, Ludikhuize discusses a configuration in which the source finger electrodes are shorter than the drain finger electrodes such that both ends of the drain finger electrodes extend beyond the source finger electrodes. *See* Section XI.B.1.

153. A POSA would have also understood that Fujishima and Ludikhuize are also similar and analogous to the '755 patent, which generally discloses high voltage field-effect transistors (FETs) (including MISFETs and MOSFETs, as Fujishima and Ludikhuize disclose). '755 Pat., 3:56-4:8; *see* Section VI.A-VI.B (where I explain that MOSFETs are MISFETs and the similar electrode structures across FETs). The '755 patent is specifically directed to making changes to the

electrode structure to help alleviate negative electric field impact and improve the robustness of a transistor, including elevating the tips of the finger of a drain electrode, increasing the curvature of the drain electrode tips, and tapering the electrode fingers. *Id.*, 3:53-55, 4:64-5:8, 8:43-59, 10:5-22, Fig. 6C.

154. Thus, a POSA would have understood that Fujishima and Ludikhuizen are analogous art to the '755 patent and combinable with each other because they belong to the same field of endeavor and are reasonably pertinent to similar problems. Given that Fujishima and Ludikhuizen disclose similar systems that operate in a similar manner and are directed to similar problems, a POSA would have also been motivated to combine their teachings.

3. Claim 6 – The transistor of claim 1, wherein at least one of said source finger electrodes has a source finger electrode main body coupled to a source pad, said drain finger electrode end extending beyond said source finger electrode main body.

155. It is my opinion that Fujishima and Ludikhuizen render obvious claim 6. Specifically, Ludikhuizen discloses “source fingers 6” that have a main body portion coupled to a source pad and a “drain finger 7” that has “tips 11” that extend past the source finger electrode, including the main body portion. Ludikhuizen, Abstract, Figs. 1, 3.

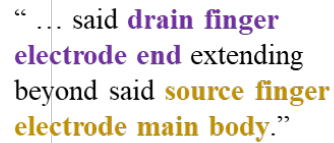
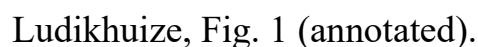


FIG. 1

portions. Ludikhuize, Fig. 1. Fujishima discloses a source pad, as claimed (as I

explained in Section XI.A.7), however, a POSA would have also understood that the **main body portions** of **source fingers 6** in Ludikhuize couple to a source pad because (i) Ludikhuize discloses a high-voltage transistor (*id.*, 4:42-45) since it discusses applying “high voltages” to the device, (ii) such devices include transistors that connect to a circuit external to the transistor, and (iii) the **main body portions** of **source fingers 6** couple to a source pad to enable the external circuit access to the source electrode. The source pad acts as an interface and connects all **source fingers 6** enabling wire bonding to be connected to the source pad, instead of each individual finger, which provides a simpler manufacturing process. The source pad also reduces the resistance for current flow as it allows current to spread into a large area. Ludikhuize discloses a drain pad as it notes that the disclosed device can have multiple drain fingers (or “digits,” as Ludikhuize also uses that term interchangeable) that are “interconnected at one side,” which a POSA would understand to mean a drain pad interconnecting the multiple drain fingers. Ludikhuize, 3:32-37. A POSA would have further understood that Ludikhuize’s device would also include a source pad, similar to the disclosed drain pad, that interconnects the multiple source fingers. Moreover, a POSA would have understood that Ludikhuize’s source pad provides numerous benefits, including providing uniform current distribution across source fingers, providing a low-resistance path

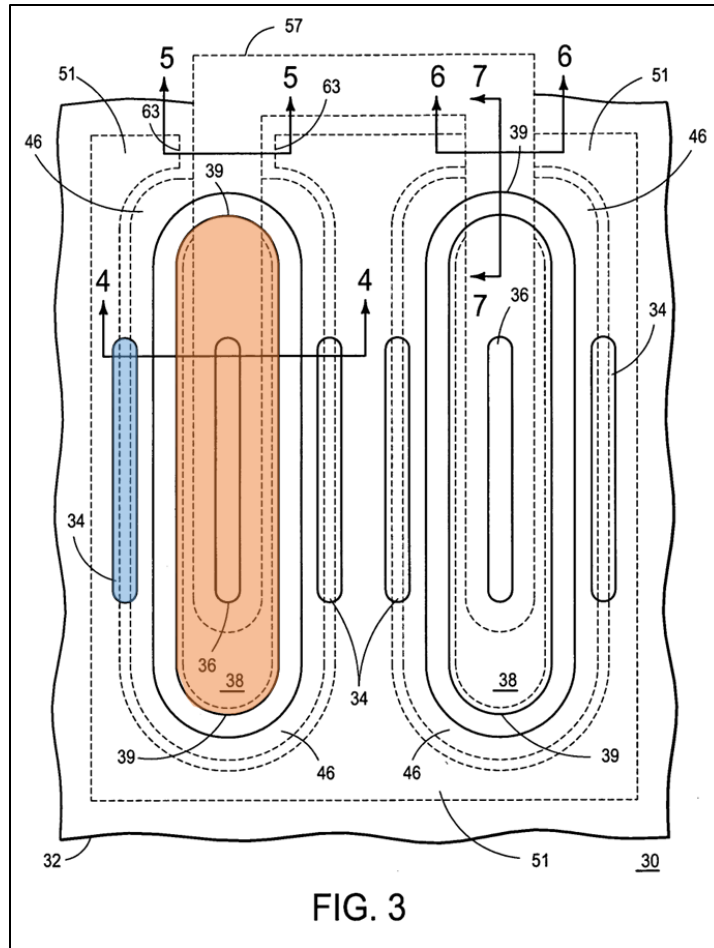
157. Ludikhuize discloses extending the “**tips 11**” of “**drain finger 7**” beyond the **main body portions** of the **source fingers 6**. Ludikhuize, Fig. 1. Ludikhuize explains that the “**source fingers** are [made] shorter than the **drain finger[]** at the ends of the[**drain finger[]**” to increase the safe operating area of the transistor (Ludikhuize, Abstract, Fig. 1) and lower the electric field concentration at the tips of the drain finger, among other benefits noted above. Ludikhuize, 2:42-50; *see id.*, 1:62-2:19, 4:4-33, 3:46-54, 2:36-41, Fig. 4, Claim 1.



158. As I explained, POSA would have had general motivations to combine Fujishima and Ludikhuize. *See* Section XI.B.2. It is also my opinion that a POSA would have also had specific motivations to combine Fujishima's and Ludikhuize's teachings to extend the end portion of Fujishima's drain finger electrode (e.g., as shown in Fujishima's Figure 8) beyond the main body portion of the source finger electrode (e.g., as shown in Fujishima's description of the prior art in Figure 18); *see* Section XI.A.7.

159. It is my opinion that a POSA would have found this combined configuration obvious because both references disclose similar types of transistors with specific configurations of the end portion of a drain finger electrode that minimizes the concentration of electric field at this end portion and provides improvements to the transistor device. Fujishima, 2:54-3:33, 3:44-52, 6:13-33, 12:23-40, Fig. 6(b); Ludikhuize, Abstract, Fig. 1, 2:42-50; *see id.*, 1:62-2:19, 4:4-33, 3:46-54, 2:36-41, Fig. 4, Claim 1; *see* Section VI.A-VI.B (where I explain that MOSFETs are MISFETs and the similar electrode structures across FETs). Thus, Fujishima and Ludikhuize both directly teach and suggest modifying electrode configurations to help minimize electric field concentrations, and this would have strongly motivated a POSA to consider and combine the teachings of these references directed toward the same goal.

160. A POSA would have understood that this combination would have been routine because implementing specific dimensions for electrode fingers (i.e., Ludikhuize's disclosure of source fingers being shorter than drain fingers, as explained above) is a simple design change that involves a scaling or length adjustment and can be implemented during the planning phases. In fact, Ludikhuize even explains that this modification is "simple." Ludikhuize, 4:21-26, 2:36-41. As I explained in Section VI.B, it was already well known to change the configuration or geometry of the finger-like portions of these electrodes to address electric field issues. For example, a 2005 patent publication discloses **drain finger electrodes** longer than the **source finger electrodes**, such that the drain electrodes extend past the source electrodes on both sides. *See* Ex-1041 ¶20 (explaining that Fig. 3 shows drain fingers 39 and source regions 34); Fig. 3 (showing that drain fingers 39 are longer and extend past the source regions 34), 35 (noting that a "further advantage is that the drain finger design is flexible to include long drain fingers), 16-17 (noting that the disclosed "structure according to the present invention eliminates electric field crowding issues associated with fingertip regions"); *see also id.*; ¶¶ 5, 8, 19.



Ex-1041, Fig. 3 (annotated).

161. Thus, a POSA would have found it straightforward with a reasonable expectation of success to modify Fujishima's electrode structure such that the tips of the drain finger electrode extend beyond the main body of the source finger electrode, as Ludikhuize discloses. Specifically, a POSA would have had a reasonable expectation of success in making this modification because the modification is purely geometrically and implemented during the design phase. Specifically, a POSA would have understood that the geometry and configuration of the electrode structure is based on developing computer-aided designs (CAD),

including a mask design layer that corresponds to the electrode structure, and that fabricating the transistor with the electrode structure by implementing the mask design layer created during the planning process. Moreover, modifying the geometry and configuration of an electrode, such as extending the drain finger electrode end, simply requires making a design change to the mask design layer on a computer. The fabrication process would be implemented in the same manner—i.e., uploading the revised design mask to the fabrication system so it can implement the desired electrode structure.

162. A POSA would have been motivated to make the combination to (i) increase transistor breakdown voltage, (ii) lower electric field concentration, current convergence, and Kirk effect and the drain finger electrode tips, (iii) increase transistor safe operating area, and (iv) decrease manufacturing costs and materials needed. *See* Section XI.B.1; *see also* Ex-1041, ¶¶20, 35, 16-17, 5, 8, 19, Fig. 3 (describing advantages of extending the drain finger electrode past the source finger electrode).

163. A POSA would have understood that the combination simply combines prior art elements (Fujishima's and Ludikhuize transistor and electrode configurations) according to known methods to yield predictable results (using longer drain finger electrodes relative to source finger electrodes, as both references disclose). *See* Section XI.A.7. It is also a simple substitution of one known element

(Fujishima's drain finger electrode configuration shown in Figure 8) for another (Ludikhuize's drain finger electrode configuration, which is similarly disclosed in Fujishima's description of the prior art in Figure 18) to obtain predictable results (a transistor configuration that reduces the negative electric field effect at the end portions of the drain finger electrode, as both references seek to do). It also uses a known technique (Ludikhuize's drain finger electrode configuration) to improve similar devices (transistors disclosed in Fujishima and Ludikhuize) in the same way (to reduce the negative electric field effect).

4. Claim 7 – The transistor of claim 1, wherein said drain finger electrodes are longer than said source finger electrodes.

164. It is my opinion that Fujishima and Ludikhuize render obvious claim 7 at least for the reasons they render obvious claim 6. As I explained for claim 6, Ludikhuize discloses drain finger electrodes that are longer than source finger electrodes. *See* Section XI.B.3; Ludikhuize, Fig. 1, 3:28-37, 4:58-67. Additionally, A POSA would have been motivated to combine Fujishima and Ludikhuize and would have had a reasonable expectation of success making the combination for the reasons I explained for claim 6, including because the combination asserted for claim 6 discloses drain finger electrodes longer than source finger electrodes.

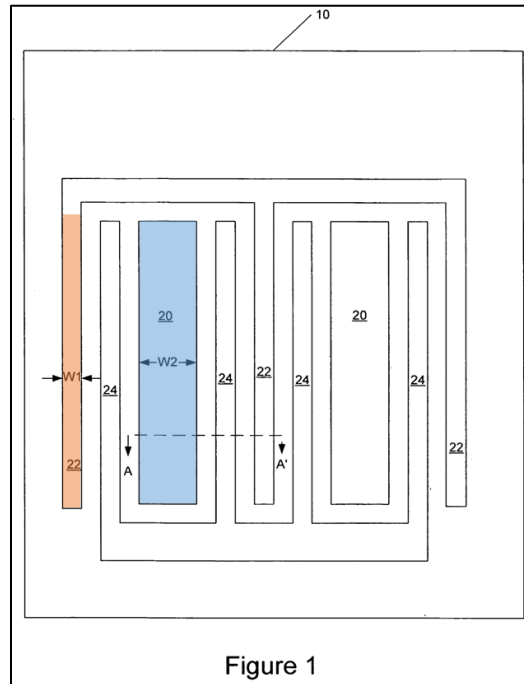
C. Ground 1D: Fujishima and Sriram Render Obvious Claims 8-9 and 14

165. Claims 8-9 and 14 limit the transistor to a high-electron mobility transistor (HEMT) (claims 8 and 14) or a group III-V transistor (claim 9). As the '755 patent explains, a transistor can be a “group III-V HEMT[,]” such as a GaN HEMT. '755 Pat., 2:2-5, 4:9-15. Sriram discloses a GaN HEMT similarly structured to Fujishima's MISFET, including interdigitated source and drain finger electrodes with a main body and an end portion, and a POSA would have found it obvious to combine Fujishima and Sriram. *See* Sections VI.A-VI.B (where I explained that MISFETs and GaN HEMTs had similar electrode structure).

1. Sriram

166. Sriram discloses semiconductor devices “desirable for high frequency applications,” specifically looking at the “type of structure” of “conventional [Field Effect Transistors] FETs [with] interdigitated structures ... having a source, a drain and a gate.” Sriram ¶¶4-5, 11, Figs. 1-2. Like Fujishima, Sriram discusses structural improvements for conventional transistor devices, including (i) integrated designs that allow for use of plurality of transistors with a more packed design to save space (*id.*, ¶9) and (ii) modifying the dimensions of the **drain finger electrodes** and **source finger electrodes**, as shown in Figure 1 below, to reduce the source capacitance of the transistor. *Id.*, ¶¶37, 40, 42, 11, Fig. 1. A POSA would have understood that reduced C_{ds} enhances switching speed, reduces power losses, improves high-

frequency performance, minimizes noise, and provides more control over electric field effects to reduce risk of field-induced breakdown during high-speed switching.



167. Sriram explains that its disclosure applies to a variety of types of lateral power transistors known in 2006—six years before the alleged date of the invention—including “GaN HEMTs, GaN HEMT MMICs ... GaAs HEMTs, GaAs HEMT MMICs, GaAs pHEMTs, GaAs pHEMT MMICs and the like.” *Id.*, ¶¶43, 2 (“present invention relates to microelectronic devices”), 11, 16, 42 (“Furthermore, embodiments of the present invention are not limited to MESFETs, but may be utilized with other devices.”), Abstract, Figs. 2, 3E, 5-6; *see id.*, Claims 1, 8-10, 18-19, 22, 30-32, 40-41.

168. Sriram also explains the benefits of high electron mobility devices (such as HEMTs)—noting that “semiconductor materials which have a high electron

mobility were preferred because more current could be developed with a lesser [electric] field, resulting in faster response times when a field is applied,” making such materials more preferable for high frequency applications. *Id.*, ¶6.

2. General Motivations to Combine

169. It is my opinion that a POSA would have found it obvious to combine Fujishima and Sriram, which disclose complementary systems and methods for configuring transistors and addressing similar problems: improving overall transistor performance by, for example, alleviating negative electric field effects within the transistor.

170. Similar to Fujishima (*see* Section XI.B.2), a POSA would have understood that Sriram discloses interdigitated drain and source fingers in a lateral power transistor and configuration options for transistors that help prevent electrical breakdown due to negative electric field effects. *See* Section XI.C.1; *see* Section VI.A-VI.B (where I explain that FETs, like those disclosed in Fujishima and Sriram, share similar electrode structures). Specifically, Sriram discusses modifying the dimensions of drain and source finger electrodes to reduce source capacitance of the transistor device, which reduces risk of electric field-induced breakdown during high-speed switching. *See* Section XI.C.1.

171. Fujishima and Sriram are also similar. I describe the '755 patent above in Section XI.B.2 and, for the same reasons as I presented there and the descriptions of Beach I provide, Beach and the '755 patent are similar.

172. Thus, a POSA would have understood that Fujishima and Sriram are analogous art to the '755 patent and combinable with each other because they belong to the same field of endeavor are reasonably pertinent to similar problems. Because Fujishima and Sriram disclose similar systems that operate in a similar manner and are directed to similar problems, a POSA would have also been motivated to combine their teachings. I provide additional specific motivations to combine for the combination below for specific claim elements.

3. Claim 8 - The transistor of claim 1, wherein said transistor is a high-electron-mobility transistor (HEMT).

173. It is my opinion that Fujishima and Sriram render obvious claim 8. Sriram discloses a GaN HEMT. Sriram, ¶¶16 (“the transistor may be a ... a gallium Nitride (GaN) HEMT”), 43, 63; *see id.* ¶¶5-6.

174. As I explained above, a POSA would have had general motivations to combine Fujishima and Sriram. *See* Section XI.C.2. It is also my opinion that a POSA would have also had specific motivations to combine Fujishima’s and Sriram’s teachings to apply Fujishima’s disclosures to GaN HEMTs. *See* Section XI.A.7.

175. A POSA would have found this combination obvious because both references are directed to improving the operation of high power transistors in high frequency applications. For example, Fujishima's invention is directed to improving power transistors used in power integrated circuits "for switching power sources," which a POSA would understand as needing high frequency transistors. Fujishima, 2:54-64. Similarly, Sriram describes improvements to high power transistors used for high frequency applications. Sriram ¶¶4-5, 11, Abstract, Claim 1; *see id.* ¶¶6-10. Thus, based on the disclosures and goals of both references, a POSA would have been motivated to consider and combine the teachings of these references.

176. A POSA would have also understood that this combination would have been routine because a POSA would have understood Fujishima's disclosures relied upon for claim 1 (*see* Section XI.A.2) are directed toward the electrode structure of a transistor and such disclosures would be applied similarly to GaN HEMTs disclosed in Sriram that have a similar electrode structure. As I explained in Sections VI.A-VI.B, FETs like those disclosed in Fujishima and Sriram had similar electrode structure, further supporting the proposed modification. Moreover, it was well known at the time of the alleged invention to apply FET configuration techniques to HEMT devices, and such modifications were common and routinely performed. *See* Ex-1018 (Quay), 70-71 ("parameters of the MISFET are very similar to those of the HEMT"); Ex-1044, 862, 867 (explaining that existing MOSFET models can be used

for analyzing and modeling HEMT devices and circuits); Ex-1042, 1, 3-9, 27 (explaining similarities between MOSFETs and GaN HEMTs, as well as explaining how “features of MOSFET circuit models that can be adopted for GaN HEMT modelling”); Ex-1043, 1, 12-13 (explaining that “GaN-HEMTs can be modeled by selected equations from the standard MOSFET” modeling”); *see* Section VI.B. This is especially true for features relating to the electrode layout for electric field management purposes, as electric field management around the drain finger electrode for lateral MOSFETs and HEMTs are substantially similar. For example, Sriram’s GaN HEMTs are lateral power transistors with interdigitated drain and source fingers, and the drain electrodes have a main body portion and end portion. *See* Sections XI.C.1, XI.C.2. In fact, Fujishima discloses a describes a specific type of transistor—MISFETs, and one type of MISFET well known by the time of the alleged invention were GaN MIS-HEMTs, which are a type of GaN HEMTs. *See* Sections XI.A.1 and XI.A.9; Section VI.B. Moreover, a POSITA would have further understood that applying Fujishima’s principles in this manner to GaN HEMTs would have furthered Fujishima’s goals of providing an improved transistor for high frequency applications (which Fujishima is used for), as GaN HEMTs provide high electron mobility resulting in “higher saturated electron drift velocities,” which are preferred for high frequency applications “because the higher velocity translates to shorter times from source to drain” (i.e., faster switching speeds). Sriram, ¶6. Thus,

it is my opinion that a POSA would have had a reasonable expectation of success and found it straightforward to incorporate Fujishima's disclosures relied upon for claim 1 to Sriram's GaN HEMT—a device that was well known by 2006, six years before the alleged invention date.

177. It is also my opinion that a POSA would also have been motivated to make the combination for additional benefits, as GaN HEMTs provide numerous benefits over conventional transistors including (i) higher breakdown voltage, (ii) lower on-resistance reducing conduction losses, (iii) lower switching losses, (iv) higher power conversion efficiency, (v) use of smaller passive components, (vi) better thermal conductivity, (vii) reduced parasitic capacitance, and (viii) higher power density. *See* Beach, 1:25-60, 3:59-65 (listing numerous benefits of GaN HEMTs); Ex-1025, 376-77.

178. A POSA would have understood that the combination simply combines prior art elements according to known methods (applying Fujishima's technique of raising drain electrodes to Sriram's GaN HEMT with interdigitated drain and source electrodes) to yield predictable results (making the drain finger electrode end elevated so that it is non-coplanar with the main body, as disclosed in Fujishima, to the GaN HEMT, which itself provides numerous benefits as noted above). Using Fujishima in a GaN HEMT would have been obvious because it would be the use of known technique (Fujishima's technique of raising drain electrodes to improve

withstand voltage) to improve similar devices (Sriram's GaN HEMT) in the same way (using the same Fujishima raised drain electrode technique in a GaN HEMT). It is also a simple substitution of one known element (Fujishima's drain finger electrode configuration with an elevated end in a MISFET) for another (Sriram's drain finger electrode configuration with flat end in a GaN HEMT) to obtain predictable results (a GaN HEMT with a drain finger electrode configuration that simply raises the drain finger electrode end portion so that it is elevated). And a POSA would have applied Fujishima to HEMTs with a reasonable expectation of success because applying FET configuration to HEMTs was common and routinely performed. *See* Section XI.A.9; Ex-1018 (Quay), 70-71 ("parameters of the MISFET are very similar to those of the HEMT"); Ex-1044, 862, 867 (explaining that existing MOSFET models can be used for analyzing and modeling HEMT devices and circuits); Ex-1042, 1, 3-9, 27 (explaining similarities between MOSFETs and GaN HEMTs, as well as explaining how "features of MOSFET circuit models that can be adopted for GaN HEMT modelling"); Ex-1043, 1, 12-13 (explaining that "GaN-HEMTs can be modeled by selected equations from the standard MOSFET" modeling"); *see* Section VI.B (where I explain that FETs have similar electrode structure). This is especially true for features relating to the electrode layout for electric field management purposes, as electric field management around the drain finger electrode for lateral MOSFETs and HEMTs are substantially similar.

4. Claim 9 - The transistor of claim 1, wherein said transistor comprises a group III-V transistor.

179. It is also my opinion that Fujishima and Sriram render obvious claim 9 because they disclose a GaN HEMT, which is a group III-V transistor, for the reasons I explained for claim 8. *See* Section XI.C.3. A POSA would have understood that the '755 patent explains that GaN HEMTs are group III-V transistors. '755 Pat., 2:1-7 ("Gallium nitride or GaN, as used herein, refers to a III-Nitride compound semiconductor"), 1:47-51 ("Group III-V heterostructure field-effect transistors (group III-V HFETs)" include group III-V high electron mobility transistors (group III-V HEMTs), such as "III-Nitride HEMTs"), 4:9-21 ("transistor 200 may be configured to provide a group III-V HFET, such as a III-Nitride HEMT. III-Nitride materials include gallium nitride (GaN) and/or its alloys, such as aluminum gallium nitride (AlGaN), indium gallium nitride (InGaN), and aluminum indium gallium nitride (AlInGaN)"). Foundational textbooks also explain this concept of Group III-V transistors, including that "compound semiconductors are also denoted by the position of the atoms in the periodic chart, e.g., GaAs, AlAs, InP are called III-V (three-five) semiconductors." Ex-1025, 6, 49-52, 540-41.

180. Thus, a POSA would have understood that Fujishima and Sriram render obvious a GaN HEMT incorporating Fujishima's concepts relating to the end portion of the drain finger electrode (as explained in Section XI.C.3) also renders obvious applying Fujishima's concepts to a group III-V transistor, as a GaN HEMT is a group

III-V transistor. A POSA would have been motivated to combine these prior art elements (i.e., Fujishima's concepts and Sriram's GaN HEMTs) and would have had a reasonable expectation of success making the combination for the reasons I explained in Section XI.C.3.

5. Claim 14 - The transistor of claim 10, wherein said transistor is a high-electron-mobility transistor (HEMT).

181. It is my opinion that Fujishima and Sriram render obvious claim 14 for the reasons I explained that for claim 8. *See* Section XI.C.3.

D. Ground 1E: Fujishima and Beach Render Obvious Claim 13

182. Claim 13 requires the drain finger electrode to be tapered. The '755 patent explains that that Beach discloses "tapered drain and source finger electrodes." '755 Pat., 8:43-55 ("In some implementations, further improvements in high current carrying transistors can be realized with higher breakdown voltages and lower ON-resistance through use of tapered drain and source finger electrodes, which may be implemented in combination with a curved drain finger electrode end having an increased radius of curvature, corresponding to curved drain finger electrode ends 226/326/426 in respective FIGS. 2, 3B, and 4. Such tapered source and drain finger designs are described in U.S. Pat. No. 7,417,257 [(Beach)]").

1. Beach

183. Beach discloses "a FET device with an interdigitated design for current carrying electrodes, where the interdigitated fingers have bases with a greater

dimension than a dimension of the tips.” Beach, 4:19-24, Abstract (“Fingers of the interdigitated electrode pattern have tips with smaller dimensions than the remainder of the fingers.”); *see id.*, 4:37-39, 5:50-53. “The tapered finger design balances current flow in the electrode fingers to reduce device resistance while permitting a more compact construction.” *Id.*, Abstract, Claim 1. Beach’s disclosed finger electrode configuration to “prevent[s] high electric fields from being formed in particular locations.” *Id.*, 6:49-62.

184. A POSA would have understood that Figure 3 below shows “interdigitated [drain] fingers 33 and [source fingers] 35” with the tapered configuration:

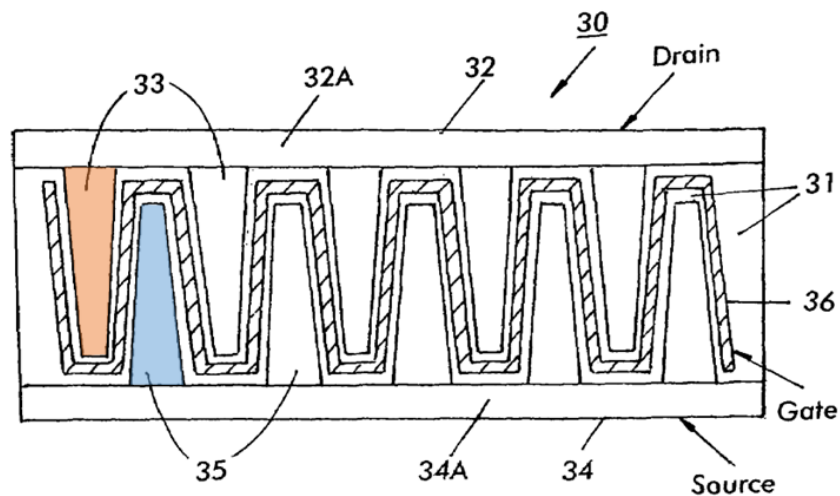


FIG. 3

Beach, Fig. 3 (annotated).

2. General Motivations to Combine

185. I have been advised by counsel that the statements in the '755 patent relating to Beach ('755 Pat., 8:43-55) are admissions that constitute applicant admitted prior art and that such admissions can support a motivation to combine particular disclosures or demonstrate the knowledge of a POSA at the time of the invention, including that they show that the admitted prior art (i.e., Beach) was analogous to the prior art to the '755 patent directed towards similar problems. This is consistent with how a POSA would have understood Beach—in that a POSA would have found it obvious to combine Fujishima and Beach, which disclose complementary systems and methods for configuring transistors and addressing similar problems: improving overall transistor performance by, for example, alleviating negative electric field effects within the transistor through modifying the electrode geometry. *See* Beach, 6:49-62, 4:18-24, Abstract, Fig. 3; Section XI.A.1.

186. It is also my opinion that, similar to Fujishima (*see* Section XI.B.2), Beach discloses lateral transistors with interdigitated source and drain finger electrodes. Beach, Abstract, 4:12-24, 4:31-33, 5:51-67, Figs. 1, 3; *see id.*, Claims 1, 6; *see also* Sections VI.A-VI.B (where I explain that FETs have similar electrode structure.). Beach also discloses tapering the drain and source finger electrodes to “prevent[s] high electric fields from being formed in particular locations.” *Id.*, 6:49-62, 4:18-24, Abstract; *see* Section XI.D.1.

187. Beach is similar to the '755 patent. I describe the '755 patent above in Section XI.B.2 and, for the same reasons as I presented there and the descriptions of Beach I provide, Beach and the '755 patent are similar.

188. Thus, a POSA would have understood that Fujishima and Beach are analogous art to the '755 patent and combinable with each other because they belong to the same field of endeavor are reasonably pertinent to similar the problems. Given that Fujishima and Beach disclose similar systems that operate in a similar manner and are directed to similar problems, a POSA would have been motivated to combine their teachings. Additional specific motivations to combine for the combination are provided below for specific claim elements.

3. Claim 13 - The transistor of claim 10, wherein said drain finger electrode is a tapered drain finger electrode.

189. It is my opinion that Fujishima and Beach render obvious claim 13. Specifically, Beach discloses a tapered **drain finger electrode**, as shown below in Figure 3. Beach, Abstract, 6:1-11 (“ ... because interdigitated fingers 33, 35 are provided with larger dimension bases than is the case after their tips ...”); *see id.*, 6:38-48, 4:21-25, 6:57-61.

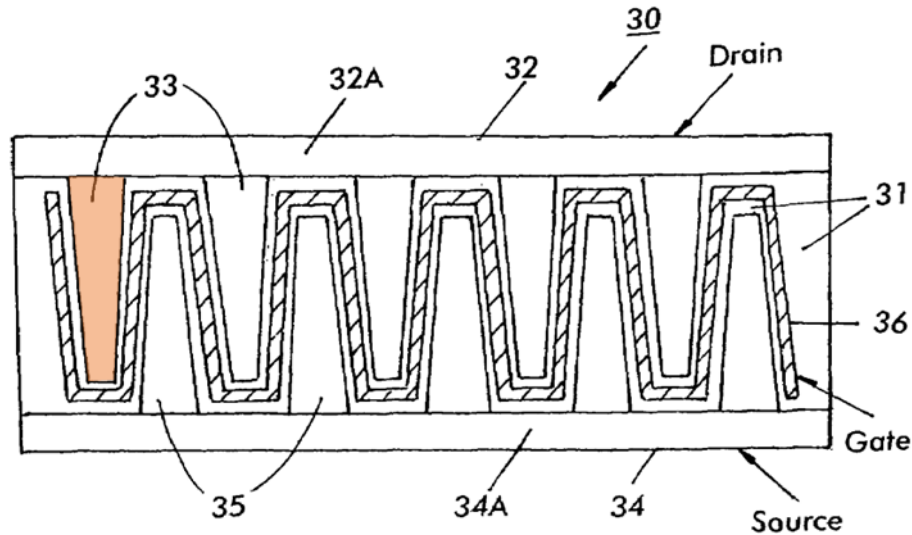


FIG. 3

Beach, Fig. 3 (annotated).

190. As I explained above, a POSA would have had general motivations to combine Fujishima and Beach. *See* Section XI.D.2.

191. As discussed in Section XI.D.2, the applicant of the '755 patent conceded that Beach—specifically Beach’s “tapered drain and source finger electrode[]” designs—was prior art and that such a configuration provided “higher breakdown voltages and lower ON-resistance.” ’755 Pat., 8:43-55. I have been advised by counsel that these statements regarding Beach in the ’755 patent (’755 Pat., 8:43-55) can support a motivation to combine particular disclosures or demonstrate the knowledge of a POSA at the time of the invention. This is consistent with my understanding of the art at the time of the alleged invention, in that tapered

electrode configurations were well known and conventional, including how it is disclosed in Beach.

192. It is also my opinion that a POSA would have also had additional specific motivations to combine Fujishima's and Beach's teachings to taper Fujishima's drain finger electrode, as Beach discloses. *See* Section XI.A.14.

193. It is my opinion that a POSA would have found this combined configuration obvious because both references disclose specific configurations a drain finger electrode in similar types of transistors that minimizes the concentration of electric field and provides improvements to the transistor device. Fujishima, 2:54-64, 3:1-33, 3:44-52, 6:13-33, 12:23-40, Fig. 6(b); Beach 4:6-25, 6:57-61; *see id.*, Abstract, 5:51-53, 6:1-11, 1:25-39. Thus, a POSA would have understood that both Fujishima and Beach directly teach modifying electrode configurations to help minimize electric field concentrations, and this would have strongly motivated a POSA to consider and combine the teachings of these references, as they are directed toward the same goal.

194. A POSA would have found this combination would have been routine because implementing specific geometry for electrode fingers (i.e., Beach's tapered drain finger electrode, as explained above) is a simple design change of making the base width larger than the tip width and can be implemented during the planning phases. As I explained in Section VI.B, it was already well known to change the

configuration or geometry of the finger-like portions of these electrodes to address electric field issues. Thus, it is my opinion that a POSA would have found it straightforward with a reasonable expectation of success to modify Fujishima's electrode structure such that the drain finger electrode was tapered, as Beach discloses. Moreover, a POSA would have had a reasonable expectation of success in making this modification because the modification is simply geometrical and implemented during the design phase, and such types of modifications were well known, as I explained in Section VI.B. Specifically, a POSA would have understood that the geometry and configuration of the electrode structure is based on developing computer-aided designs (CAD), including a mask design layer that corresponds to the electrode structure, and that fabricating the transistor with the electrode structure by implementing the mask design layer created during the planning process. Moreover, modifying the geometry and configuration of an electrode, such as tapering the drain finger electrode, simply requires making a design change to the mask design layer on a computer. The fabrication process would be implemented in the same manner—i.e., uploading the revised design mask to the fabrication system so it can implement the desired electrode structure.

195. A POSA would have been motivated to make the combination to (i) increase device power rating, (ii) decreasing device dimensions and permitting a more compact device construction, (iii) reducing device resistance and balance

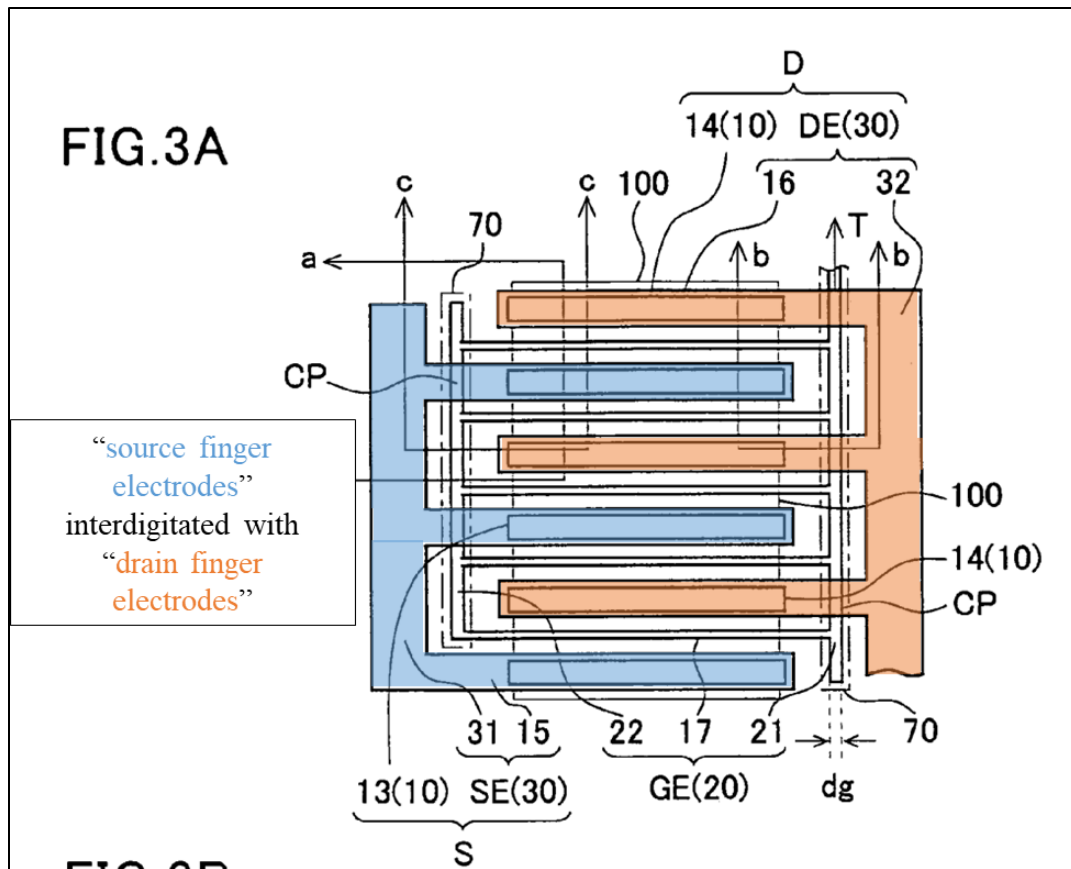
current flow, (iv) decreases power loss due to current variation across electrode finger. Beach, Abstract, 3:1-8, 4:6-33, 4:53-64, 6:1-11, 6:24-48, 6:57-61, Beach explains that the “tapered finger design balances current flow in the electrode fingers to reduce device resistance while permitting a more compact construction,” “lowers on-resistance,” “improve[s] resistance-area product,” balances the current flow, reduces size without sacrificing rating, “improve[s] power efficiency” and reduces power loss, and “prevent[s] high electric fields from being formed in particular locations (i.e., the electrode finger tips). *Id*

196. A POSA would have understood that the combination simply combines prior art elements (Fujishima’s and Beach’s transistor and electrode configurations) according to known methods to yield predictable results (using tapered drain finger electrodes, as both references disclose). *See* Section XI.A.14. It is also a simple substitution of one known element (Fujishima’s drain finger electrode configuration shown in Figure 8) for another (Beach’s tapered drain finger electrode configuration in Figure 3) to obtain predictable results (a configuration of the drain finger electrode of a transistor that reduces the negative electric field effect, as both references seek to do). It also uses a known technique (Beach’s tapered drain finger electrode configuration) to improve similar devices (transistors disclosed in Fujishima and Beach) in the same way (to reduce the negative electric field effect). *Id*.

XII. ASANO GROUNDS 2A-2B: ASANO ANTICIPATES (2A) AND RENDERS OBVIOUS (2B) CLAIMS 1-4 AND 8-9**A. Asano**

197. Asano discloses group III-V FETs (Asano ¶¶19, 55), explaining that its “FET may be any of a MESFET (Metal Semiconductor Field Effect Transistor), a GaAs JFET (Junction FET) and a HEMT (High Electron Mobility Transistor).” Asano ¶¶55, 74, 110.

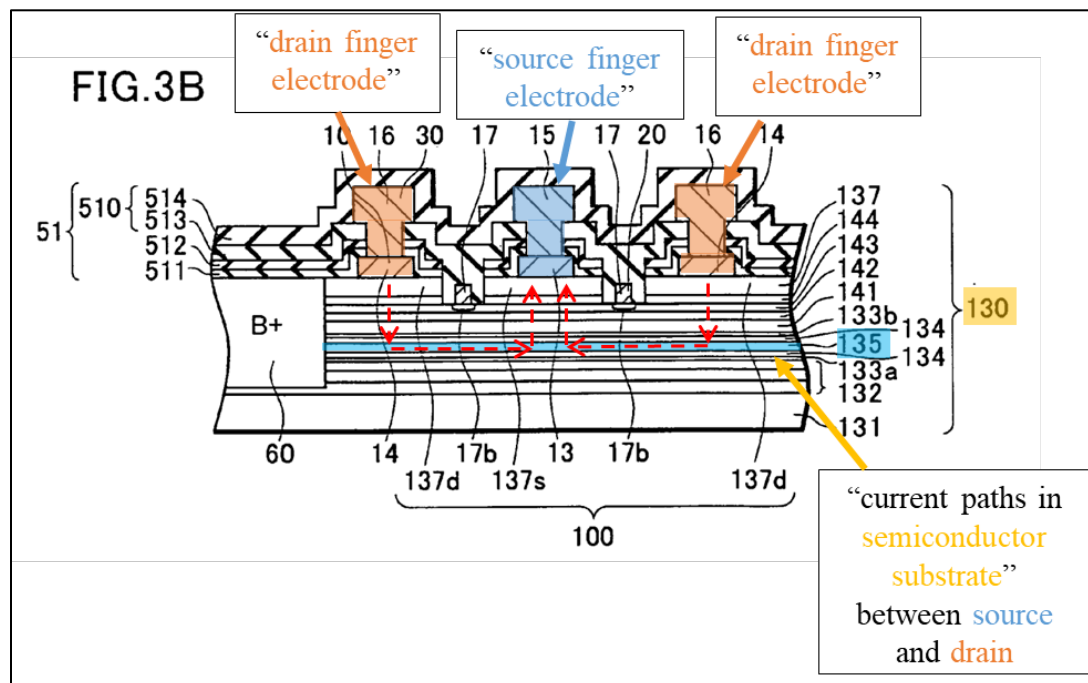
198. Asano discloses “a plurality of source electrodes elongated in a first direction, a plurality of drain electrodes elongated in the first direction, the source electrodes and the drain electrodes being positioned alternatively with respect to a second direction” (i.e., interdigitated). Asano, Abstract. Specifically, a POSA would have understood Asano as describing a plurality of source electrodes interdigitated with a plurality of drain electrodes, especially in view of how these electrodes are depicted in Fig. 3A:



Asano, Fig. 3A (annotated). Asano further explains that “the strip-shaped first source and drain electrodes 13 and 14 are disposed on the operation region 100, and come into contact with source and drain regions.” Asano ¶75. And “the strip-shaped second source and drain electrodes 15 and 16 are disposed while overlapping the first source and drain electrodes.” *Id.* Thus, a POSA would have understood that these disclosures in Asano are describing “source finger electrodes” interdigitated with “drain finger electrodes,” as shown in the annotated version of Figure 3A above.

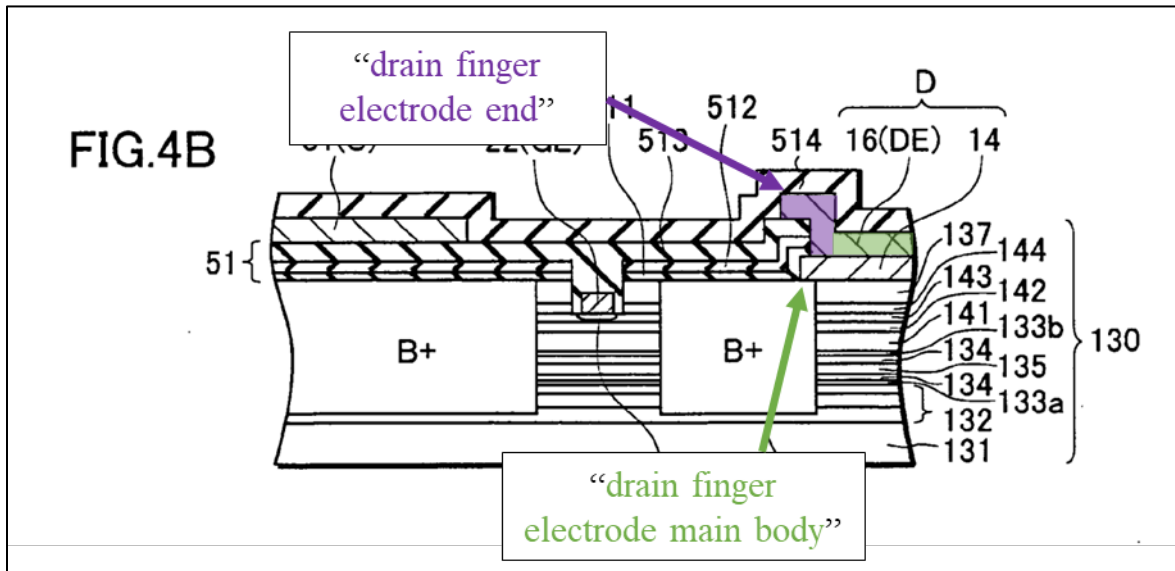
199. Asano’s Fig. 3B shows the drain and source electrodes formed on a substrate that “is obtained by growing undoped buffer layers 132 on a semi-

Figure below:



Asano, Fig. 3B (annotated).

200. Asano's Fig. 4B shows the **end of its drain finger electrode** elevated above the plane of its **drain electrode finger main body**, by interposing "nitride film 513" underneath the end portion. Asano, Fig. 4B, ¶¶101, 186.



Asano, Fig. 4B (annotated).

B. Claim 1

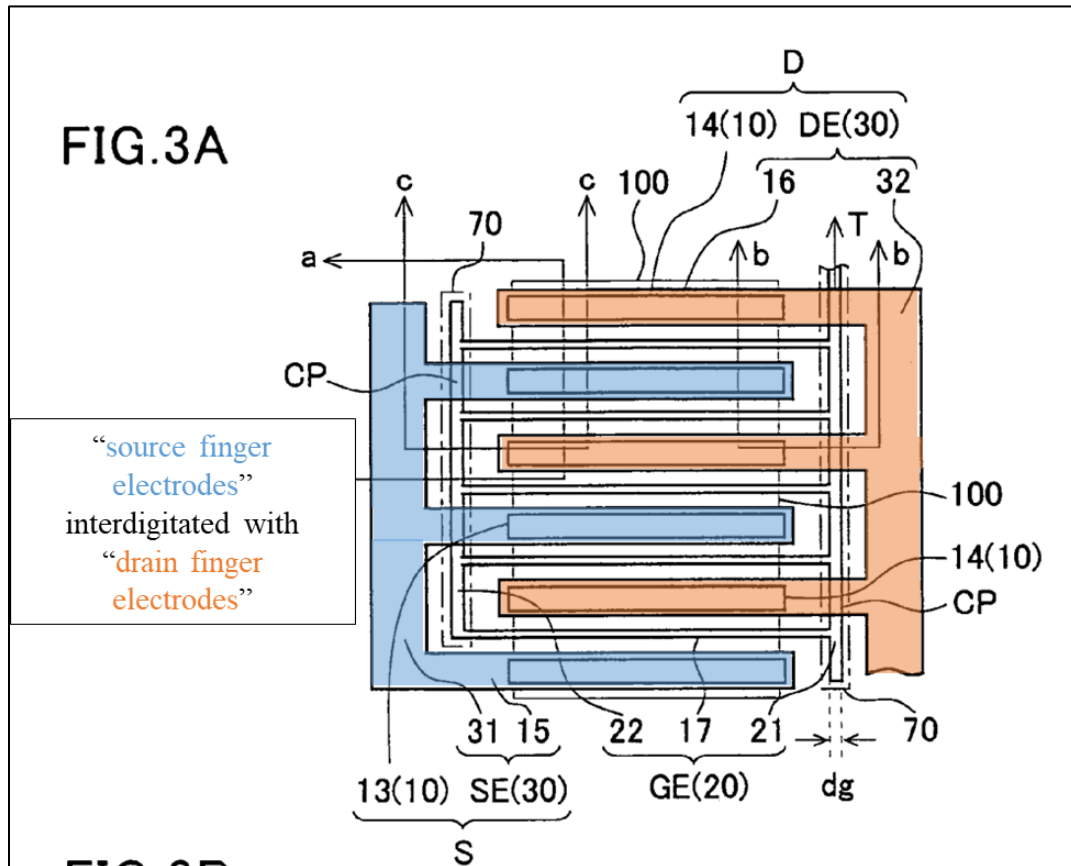
1. [1pre]: A transistor comprising:

201. If the preamble is limiting, it is my opinion that Asano discloses it because Asano states that its "invention provides a field effect **transistor**." Asano ¶¶19, 55, claims 1-12.

2. [1a]: drain finger electrodes interdigitated with source finger electrodes;

202. It is my opinion that Asano discloses or renders obvious [1a] because it discloses "**a plurality of source electrodes** elongated in a first direction, a **plurality**

of drain electrodes elongated in the first direction, the source electrodes and the drain electrodes being positioned alternatively with respect to a second direction” (interdigitated). Asano, Abstract, ¶19, Claim 1; *see also* Exs-1028-1029 (describing and depicting interdigitated structures).



Asano, Fig. 3A (annotated).

203. Asano has two source electrodes or two drain electrodes on each finger, it explains, “the strip-shaped first source and drain electrodes 13 and 14 are disposed on the operation region 100, and come into contact with the source and drain regions,” and “the strip-shaped second source and drain electrodes 15 and 16 are disposed while overlapping the first source and drain electrodes 13 and 14.” Asano

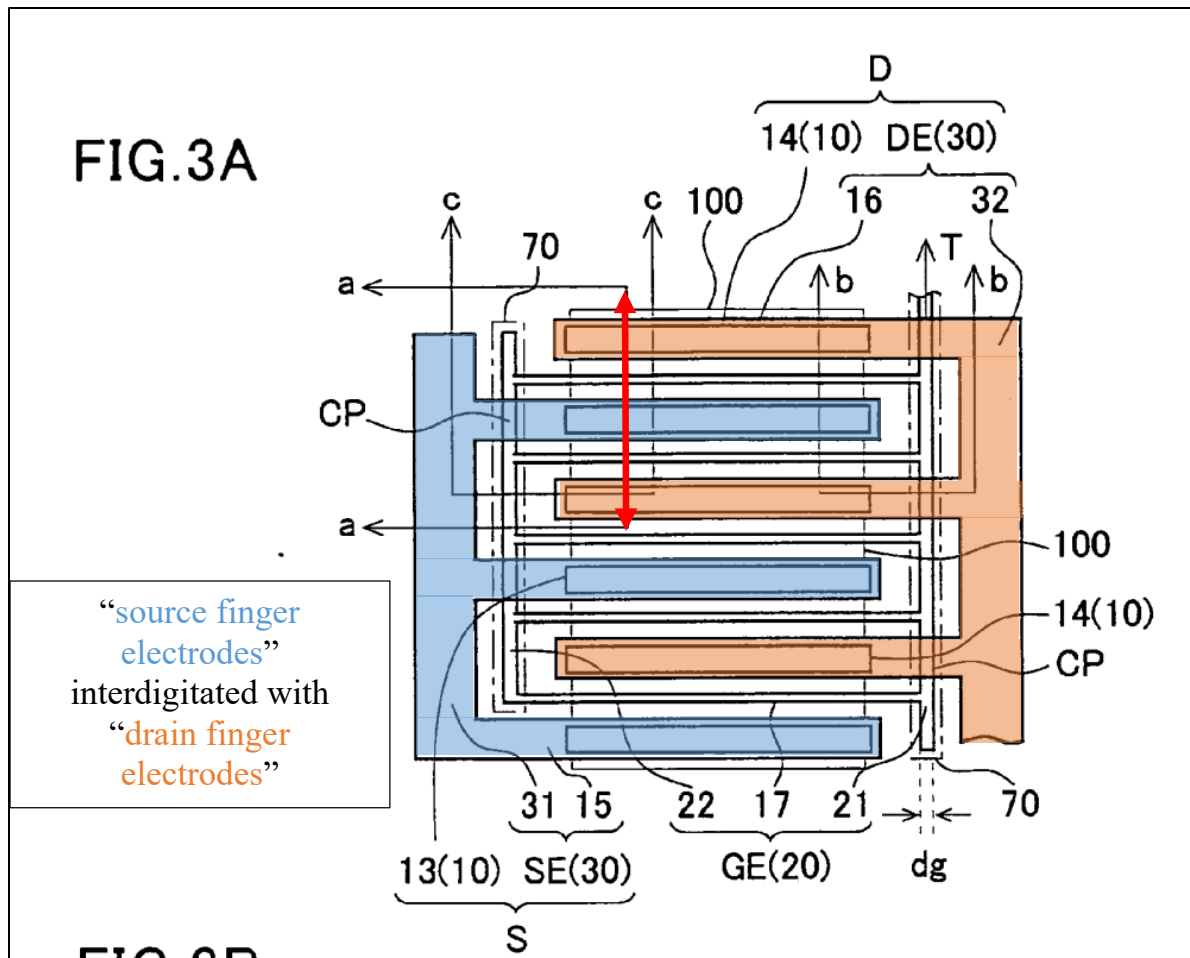
¶75. Either the first set of source and drain electrodes (i.e., source electrode 13 and drain electrode 14), second set (i.e., source electrode 15 and drain electrode 16), or both collectively satisfy the claimed source finger electrodes and drain finger electrodes, respectively, because a POSA would have understood all of these configurations to show an interdigitated pattern for the source finger electrodes and drain finger electrodes, as explained in Section XII.A above. Asano explains that the two drain electrodes make up the drain wiring electrode DE. Asano ¶63.

204. **For Ground 2B**, to the extent a single combined source finger electrode and single combined drain finger electrode is needed, that configuration would have been obvious. A POSA would have understood that source finger electrodes 13 and 15 work together as a single source finger electrode (i.e., the claimed **source finger electrodes**) and drain finger electrodes 14 and 16 work together as a single drain finger electrode (i.e., the claimed **drain finger electrodes**). This is consistent with Asano's disclosures that explain that the two drain electrodes make up the drain wiring electrode DE. Asano ¶63, Fig. 4B. It is my opinion that a POSA would have understood that drain finger electrodes 14 and 16 would constitute a single drain finger electrode because (i) electrodes 14 and 16 have the same metallic structure, are interconnected, and closely manufactured such that they are seen as a singular electrode and (ii) electrodes 14 and 16 serve the same purpose of providing electrical contact point for the transistor.

3. [1b]: current conduction paths in a semiconductor substrate between said drain finger electrodes and said source finger electrodes;

205. It is my opinion that Asano discloses [1b] because it discloses a HEMT in which channel regions create current paths for electron flow through channel layer 135 from the source finger electrodes 13 and 15 to the drain finger electrodes 14 and 16.

206. Asano explains, “[i]n **a substrate structure** of the HEMT, for example, a buffer layers, electron supply layers, **a channel (electron transit) layer**, a cap layer and the like are grown on a semi-insulating GaAs substrate.” Asano ¶56. Asano’s Fig. 3B is a “cross-sectional view **along the line a-a** in Fig. 3A,” which cuts across two drain finger electrodes and one source finger electrode. Asano ¶81.



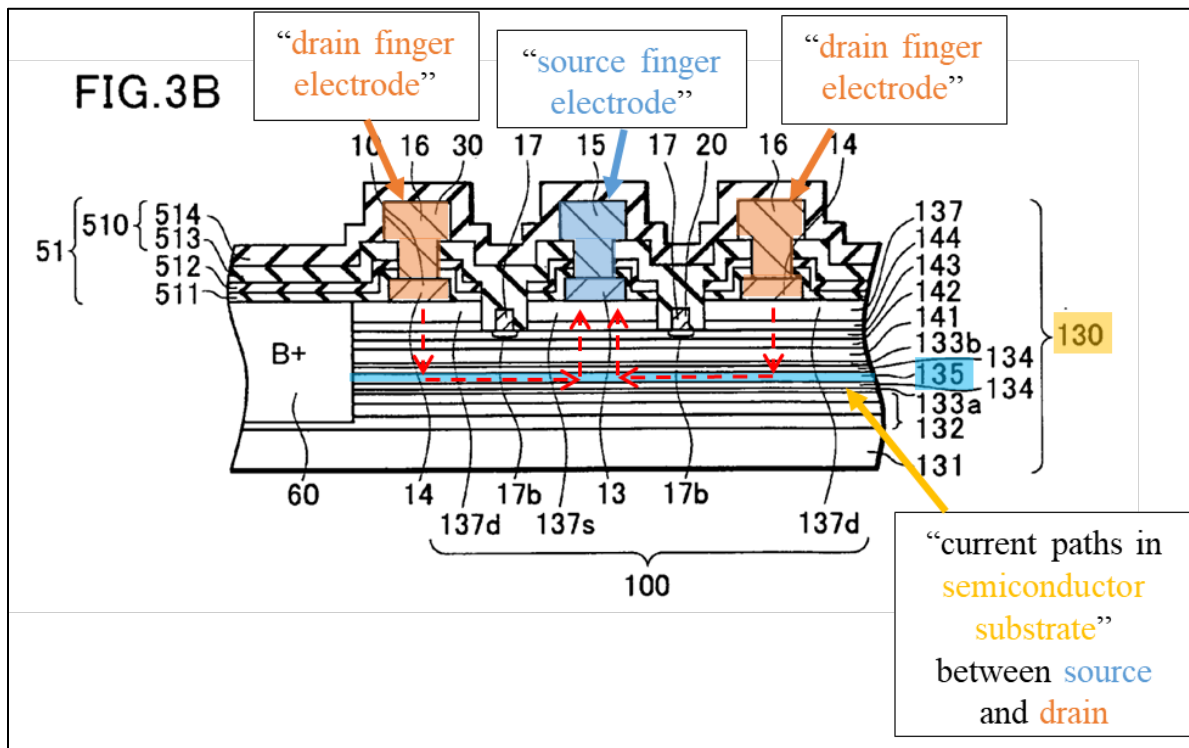
Asano, Fig. 3A (annotated).

207. Asano explains:

A substrate 130 is obtained by growing undoped buffer layers 132 on a semi-insulating GaAs substrate 131 and growing, on the buffer layers 132, a first electron Supply layer 133a that is an n⁺ type AlGaAs layer, a spacer layer 134, a **channel (electron transit) layer 135** that is an undoped InGaAs layer, a spacer layer 134, a second electron supply layer (n⁺ type AlGaAs layer) 133b, a first

undoped layer 141, a second undoped layer 142, a third undoped layer 143, a stable layer 144, and a cap layer 137.

Asano ¶81. Fig. 3B shows Asano's **channel layer 135** in **substrate 130** that creates the current path, as shown by the red line, between **source finger electrodes 13 and 15** and **drain finger electrodes 14 and 16**.



Asano, Fig. 3B (annotated).

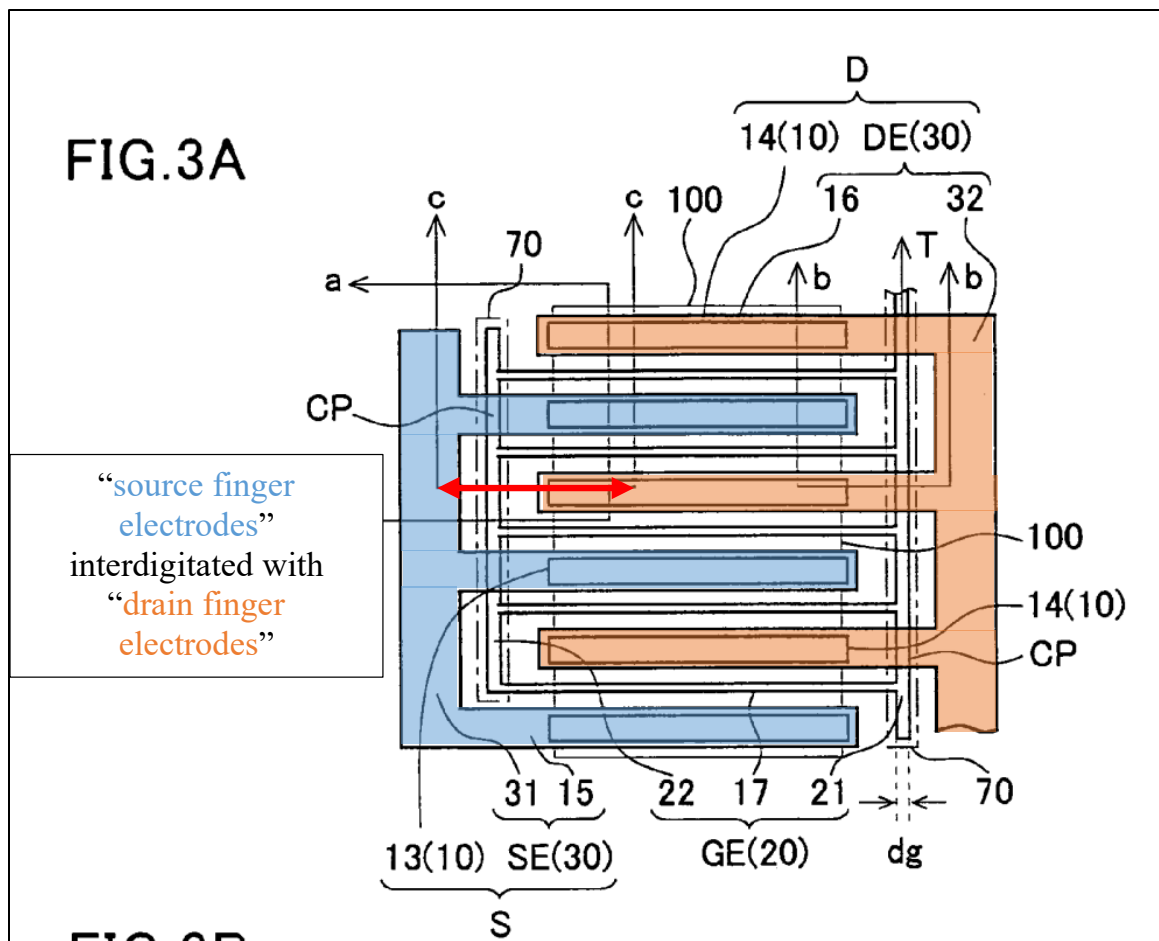
208. A POSA would have understood that Fig. 3A shows that Asano has multiple drain finger electrodes and multiple source finger electrodes, which are disposed between gate electrodes in an active area of the transistor. See Asano ¶¶76-77. A POSA would have further understood that **channel layer 135** creates a current path between each adjacent source and drain, thus constituting multiple current paths

in the device, two of which are shown above in the annotated version of Fig. 3B—specifically indicated by the red arrows.

4. [1c]: at least one of said drain finger electrodes having a drain finger electrode main body and a drain finger electrode end,

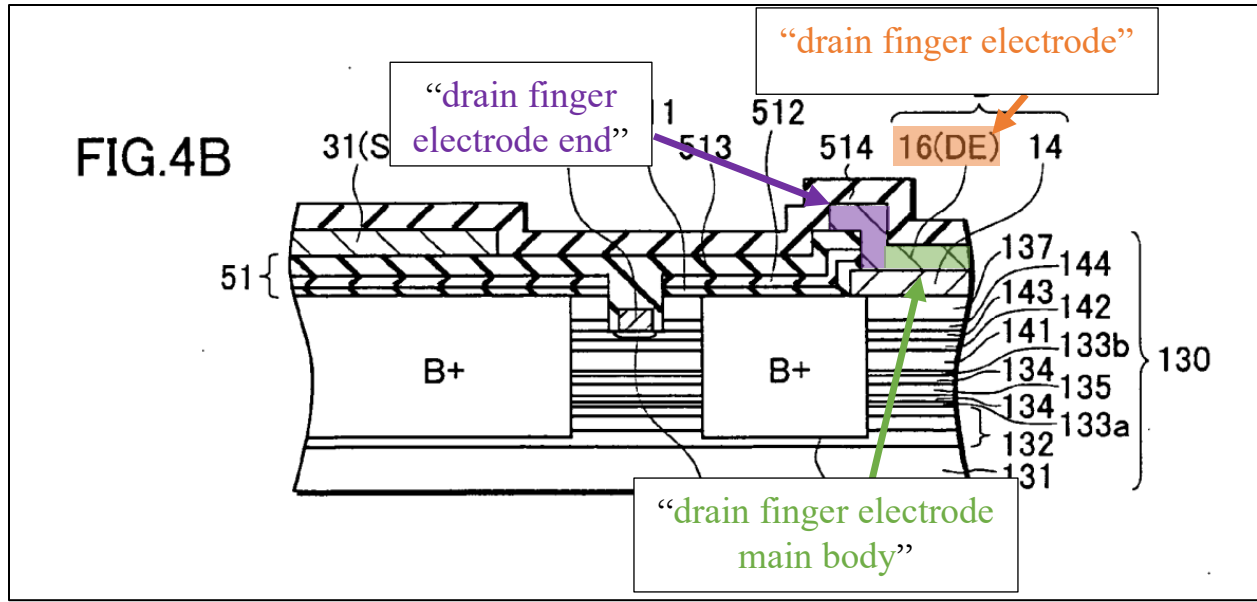
209. It is my opinion Asano discloses or renders obvious [1c] because Asano’s drain finger electrode 16 or collectively, drain finger electrode 14/16, has a main body and an end.

210. As explained for [1a], Asano discloses interdigitated **source finger electrodes** and **drain finger electrodes**. Figure 4B is a cross-sectional view of the interdigitated electrodes “**along the line c-c** in Fig. 3A.” Asano ¶110.



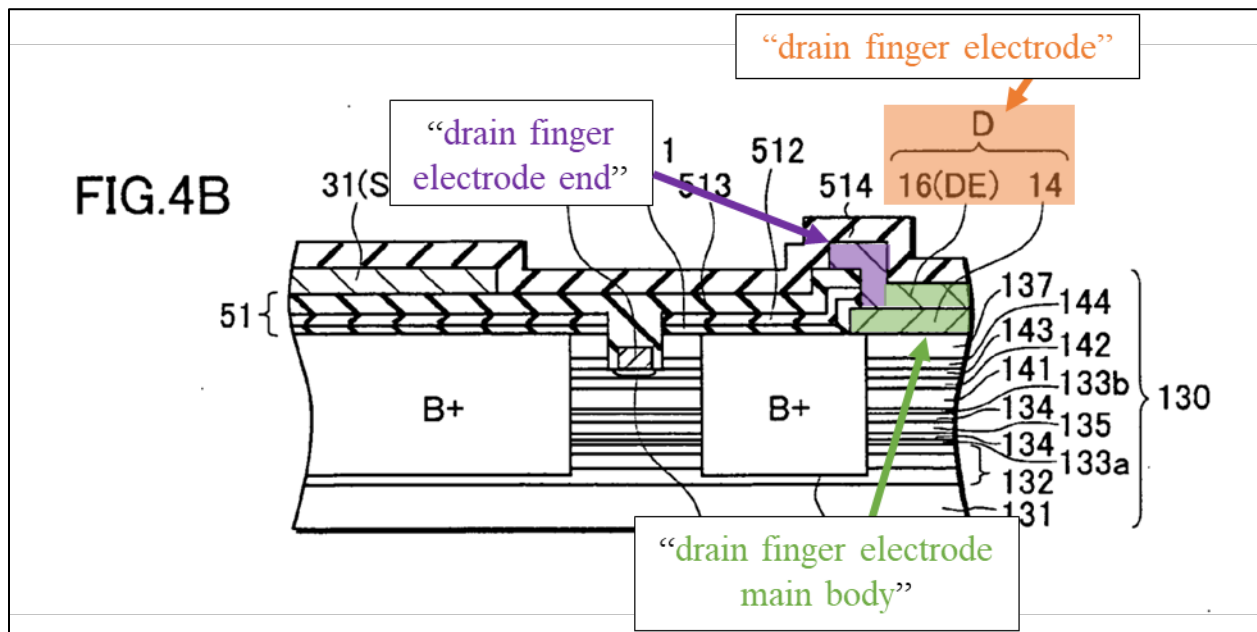
Asano, Fig. 3A (annotated).

211. A POSA would have understood that Asano’s Fig. 4B shows that its **drain finger electrode 16** has a **drain finger electrode end** at the elevated tip of a **drain finger electrode main body**. Asano, Fig. 4B. Specifically, this understanding is shown in annotated Figure 4B below:



Asano, Fig. 4B (annotated).

212. Additionally, for mapping the drain finger electrode to the drain electrodes 14/16 collectively or for **Ground 2B**, it is also my opinion that drain finger electrode 14 constitutes part of the drain finger electrode main body, as shown in Asano's Fig. 4B.

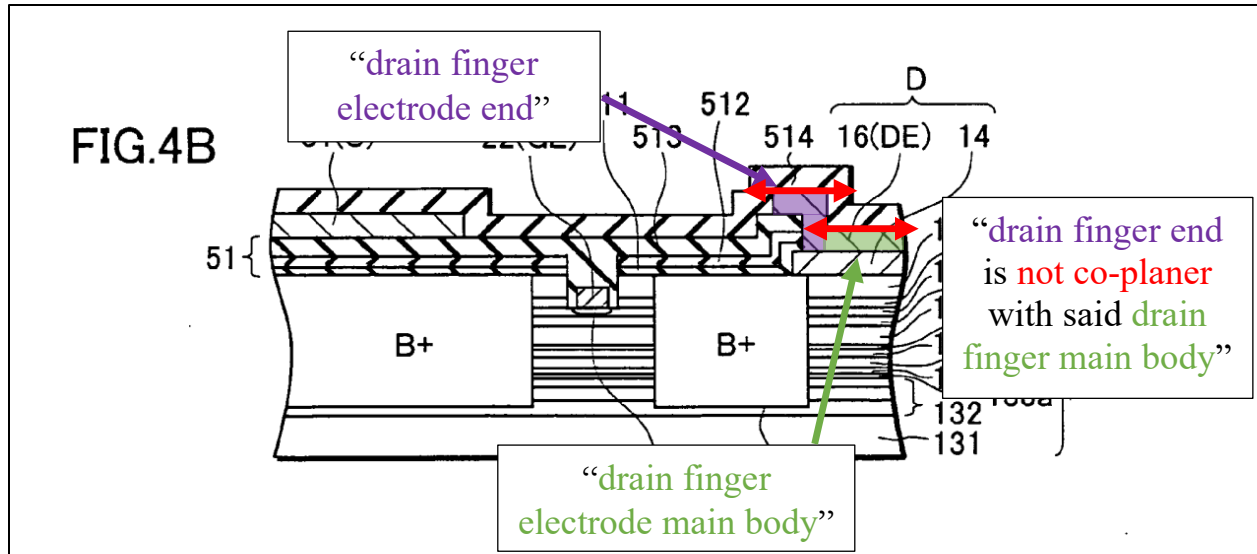


Asano, Fig. 4B (annotated). As I explained in [1b], a POSA would have would have understood that drain finger electrodes 14 and 16 work together as a single drain finger electrode.

5. [1d]: wherein at least a portion of said drain finger end is non-coplanar with said drain finger electrode main body.

213. It is my opinion that Asano discloses or renders obvious [1d] because the end portion of drain finger electrode 16 is elevated and not co-planar with drain finger electrode 16's main body or the main body of the combined drain electrode 14/16.

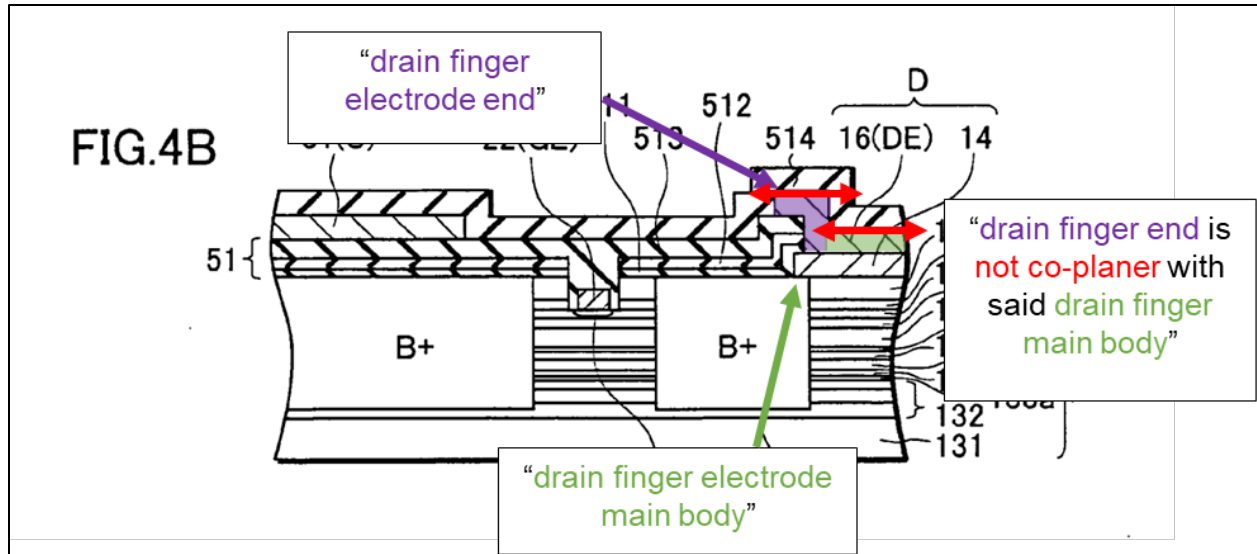
214. For **Ground 2A**, A POSA would have undersrtood that Asano's Fig. 4B shows the **drain finger electrode end** elevated above the plane of the **drain electrode finger main body**, as depicted by the two red arrows on different planes in the annotated version of the figure below. A POSA would have further understood that the Fig. 4B shows a "nitride film 513" underneath the end portion elevating the **drain finger electrode end**, elevating it to a non-coplanar position relative to the **drain finger electrode main body**. Asano, Fig. 4B, ¶¶101, 186.



Asano, Fig. 4B (annotated).

215. Additionally, for mapping the drain finger electrode to the drain electrodes 14/16 collectively or for **Ground 2B**, a POSA would have also understood that Asano’s Fig. 4B similarly shows the **drain finger electrode end** elevated above the plane of the **drain electrode finger main body**, as depicted by the two red arrows on different planes in the annotated version of the figure below.

Asano, Fig. 4B, ¶¶101, 186.



Asano, Fig. 4B (annotated).

216. Under both mappings, as the Figures show, at least a portion of the **drain finger electrode end** is non-coplanar with respect to the **drain finger electrode main body** because the **end** is on a horizontal plane that is not on the same horizontal plane as any part of the **main body**. Additionally, Asano explains the issue of having a high electric field at the **drain finger electrode end**, and a POSA would have understood that the non-coplanar structure presented in Asano, as explained above, would alleviate such electric field effect. Asano ¶¶137, 143, 233, Figs. 3A-4B.

C. Claim 2 – The transistor of claim 1, wherein a dielectric material is situated between said drain finger electrode end and said semiconductor substrate.

217. It is my opinion that Asano discloses or renders obvious claim 2 because nitride film 513 is situated between the drain finger electrode end and semiconductor substrate 130.

218. For Ground 2A, Asano discloses **nitride film 513**, which a POSA would have understood to be a dielectric material because it is, as Asano describes it, an insulating material with a dielectric constant. Asano ¶¶182, 56. A POSITA would have understood that nitride films were commonly used in transistor devices as a dielectric, insulating material, for example the most popular, silicon nitride. Ex-1018 (Quay), Section 4.64 at 184-187 (explaining silicon nitride as the most popular dielectric film in group III-V transistor devices). In fact, this is consistent with how the '755 patent describes a dielectric material—specifically that the material can be any “insulating material.” '755 Pat., 10:23-29.

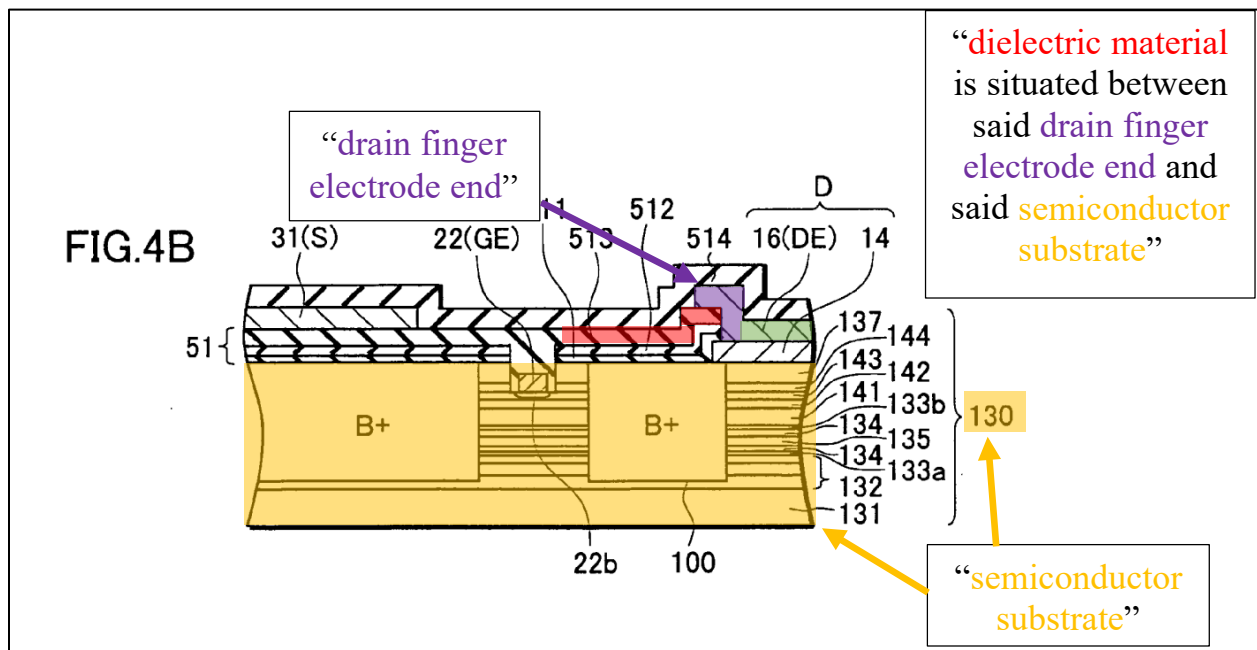
219. A POSA would have also understood that Asano discloses a semiconductor substrate 130, as it states: “In **a substrate structure** of the HEMT, for example, a buffer layers, electron supply layers, **a channel (electron transit) layer**, a cap layer and the like are grown on a semi-insulating GaAs substrate.” Asano ¶56. Asano further explains the layers comprised in the substrate:

A substrate 130 is obtained by growing undoped buffer layers 132 on a semi-insulating GaAs substrate 131 and

growing, on the buffer layers 132, a first electron supply layer 133a that is an n⁺ type AlGaAs layer, a spacer layer 134, a channel (electron transit) layer 135 that is an undoped InGaAs layer, a spacer layer 134, a second electron supply layer (n⁺ type AlGaAs layer) 133b, a first undoped layer 141, a second undoped layer 142, a third undoped layer 143, a stable layer 144, and a cap layer 137.

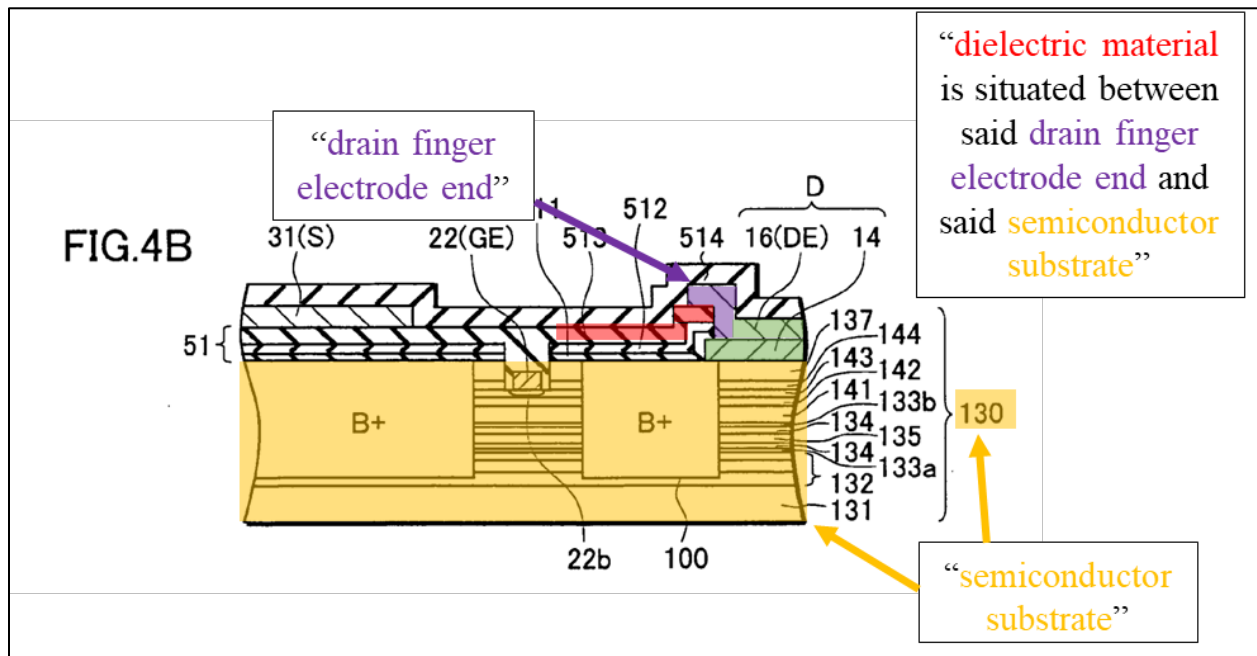
Asano ¶81.

220. Moreover, a POSA would have understood that Asano's Figure 4B shows "nitride film 513" situated between drain finger electrode end and semiconductor substrate 130. Asano, Fig. 4A, ¶¶101, 186.



Asano, Fig. 4B (annotated).

221. Additionally, for mapping the drain finger electrode to the drain electrodes 14/16 collectively or for **Ground 2B**, a POSA would have also understood that Asano's Figure 4B shows "**nitride film 513**" situated between **drain finger electrode end** and **semiconductor substrate 130**. Asano, Fig. 4A, ¶¶101, 186.



Asano, Fig. 4B (annotated).

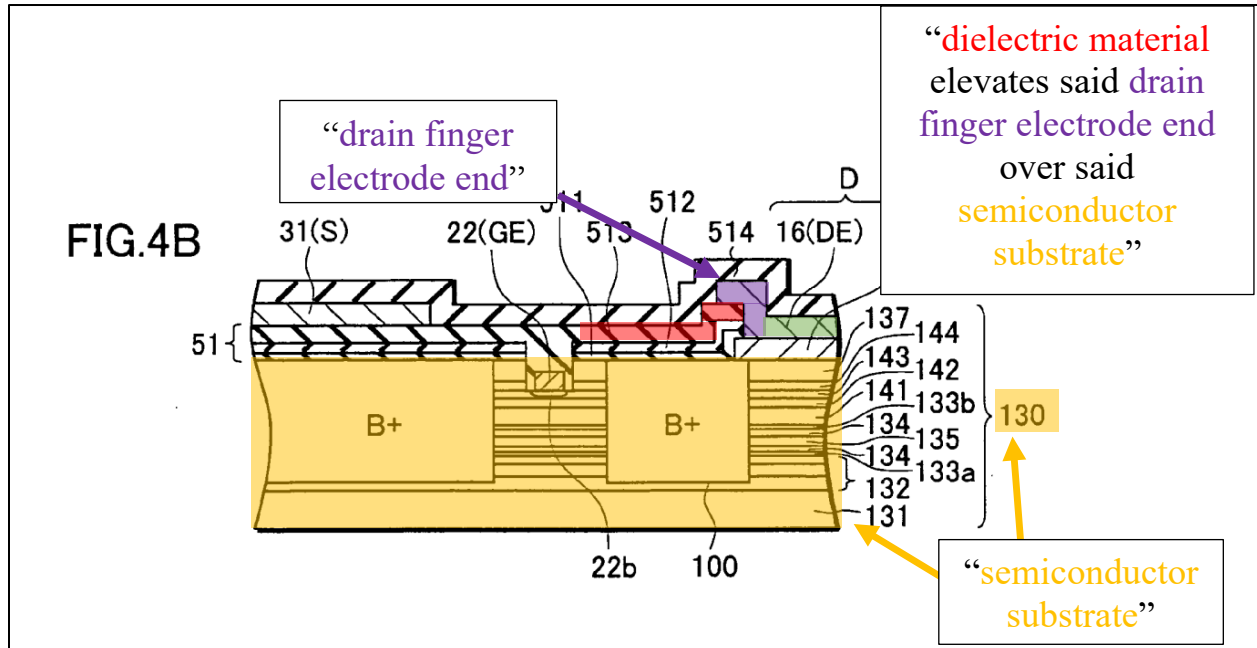
D. Claim 3 – The transistor of claim 2, wherein said dielectric material elevates said drain finger electrode end over said semiconductor substrate.

222. It is my opinion that Asano discloses or renders obvious claim 3 because nitride film 513 elevates the drain finger electrode end over semiconductor substrate 130. *See also* claim 2.

223. As explained for claim 2, **nitride film 513** is a dielectric material.

224. As explained for claim 2, **substrate 130** is a semiconductor substrate.

225. For **Ground 2A**, A POSA would have further understood that Asano's Figure 4B shows that the **"nitride film 513"** elevates **drain finger electrode end** over **semiconductor substrate 130** because **nitride film 513** is situated between the **drain finger electrode end** and **semiconductor substrate 130**, elevating the **drain finger electrode end** above the plane of **semiconductor substrate 130**. Asano, Fig. 4B, ¶¶101, 186.



Asano, Fig. 4B (annotated).

226. Additionally, for mapping the drain finger electrode to the drain electrodes 14/16 collectively or for **Ground 2B**, a POSA would have also understood Asano's Fig. 4B shows that **"nitride film 513"** elevates **drain finger electrode end** over **semiconductor substrate 130** because **nitride film 513** is

FIG.4B

“drain finger electrode end”

“dielectric material elevates said drain finger electrode end over said semiconductor substrate”

“semiconductor substrate”

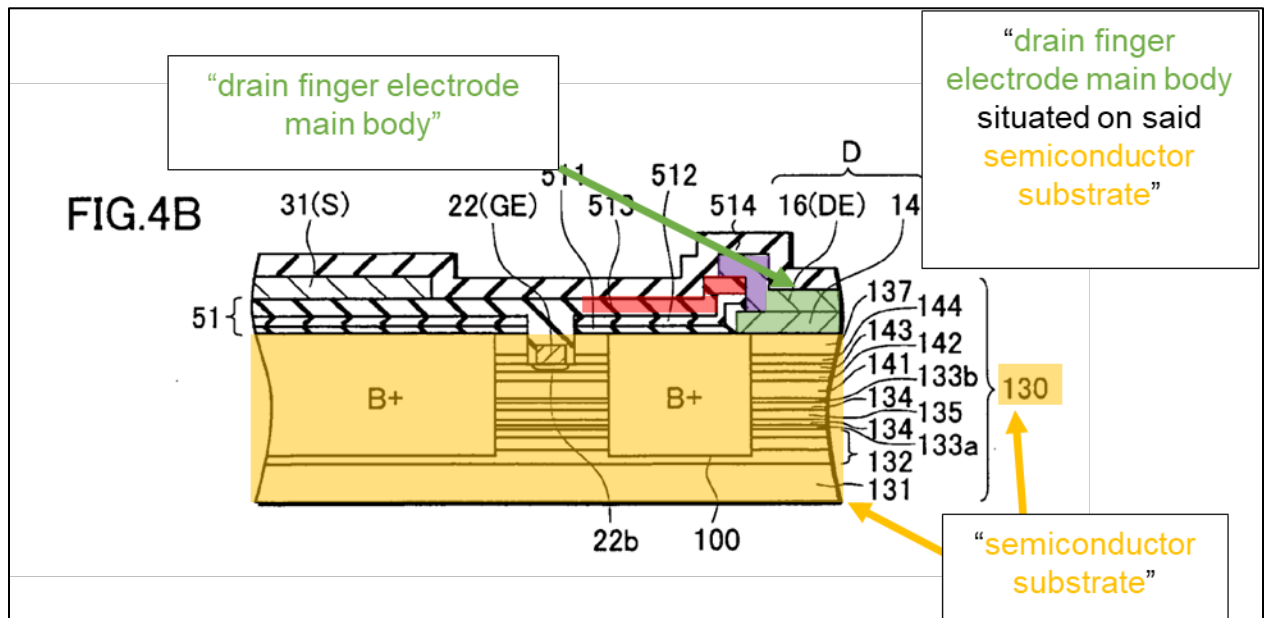
Labels in the diagram include: 31(S), 22(GE), 51, 512, 513, 514, 16(DE), D, 137, 144, 143, 142, 141, 133b, 134, 135, 133a, 132, 131, 22b, 100, B+, and 130.

E. Claim 4 – The transistor of claim 1, wherein said drain finger electrode main body is situated on said semiconductor substrate.

228. As explained for [1c], drain finger electrode 16 has a **drain finger electrode main body**.

141

230. For mapping the drain finger electrode to the drain electrodes 14/16 collectively or for **Ground 2B**, a POSA would have further understood that Asano's Figure 4B shows that the **drain finger electrode main body 14** is situated directly on **semiconductor substrate 130**, as shown in the annotated version of Figure 4B below. Asano, Fig. 4B, ¶¶101, 186.



Asano, Fig. 4B (annotated).

F. Claim 8 – The transistor of claim 1, wherein said transistor is a high-electron-mobility transistor (HEMT).

231. It is my opinion that Asano discloses or renders obvious claim 8 because its transistor is a HEMT.

232. Asano discloses FETs (Asano ¶19, 55), explaining that a “*FET may be* any of a MESFET (Metal Semiconductor Field Effect Transistor), a GaAs JFET (Junction FET) *and a HEMT (High Electron Mobility Transistor).*” Asano ¶55

(emphasis added). And it describes its invention “mainly using the HEMT.” *Id.* Figs. 3 and 4 referenced for claims 1-4, refer to “FET 1-1”—a HEMT. Asano ¶74, 110.

G. Claim 9 – The transistor of claim 1, wherein said transistor comprises a group III-V transistor.

233. It is my opinion that Asano discloses or renders obvious claim 9 because its transistor comprises semiconductor substrate 130 stack that includes various group III-V layers, like those made of AlGaAs and InGaAs.

234. Asano explains:

A substrate 130 is obtained by growing undoped buffer layers 132 on a semi-insulating GaAs substrate 131 and growing, on the buffer layers 132, a first electron **Supply layer 133a that is an n+ type AlGaAs layer**, a spacer layer 134, a **channel (electron transit) layer 135 that is an undoped InGaAs layer**, a spacer layer 134, a **second electron supply layer (n+ type AlGaAs layer) 133b**, a first undoped layer 141, a second undoped layer 142, a third undoped layer 143, a stable layer 144, and a cap layer 137.

Asano ¶81.

235. A POSA would have understood that a group III-V transistor includes layers comprising alloys made of metals from group III and group V of the periodic table. Ex-1025, 6, 49-52, 540-41. Group III of the periodic table includes B, **Al, Ga**, and In. Group V of the periodic table includes N, P, **As**, and Sb. Therefore, alloys

like GaAs, AlGaAs, and InGaAs included in Asano's transistor, are group III-V because they include metals from both group III and group V of the periodic table. In fact, the '755 patent explains this concept: "*As used herein, the phrase "group III-V" refers to a compound semiconductor including at least one group III element and at least one group V element.* By way of example, a group III-V semiconductor may take the form of a III-Nitride semiconductor. "III-Nitride", or "III-N", refers to a compound semiconductor that includes nitrogen and at least one group III element such as *aluminum (Al)*, gallium (Ga), *indium (In)*, and boron (B), and including but not limited to any of its alloys, such as *aluminum gallium nitride (Al_xGa_(1-x)N)*, *indium gallium nitride (In_yGa_(1-y)N)*, aluminum indium gallium nitride (Al_xIn_yGa_(1-x-y)N), *gallium arsenide phosphide nitride (GaAsaPbN(1-a-b))*, *aluminum indium gallium arsenide phosphide nitride (Al_xIn_yGa_(1-x-y)AsaPbN(1-a-b))*, for example." '755 Pat., 1:27-55, 4:9-21 ("transistor 200 may be configured to provide a group III-V HFET, such as a III-Nitride HEMT. III-Nitride materials include gallium nitride (GaN) and/or its alloys, such as aluminum gallium nitride (AlGaN), indium gallium nitride (InGaN), and aluminum indium gallium nitride (AlInGaN).") (emphasis added). Foundational textbooks also explain this concept of Group III-V transistors, including that "compound semiconductors are also denoted by the position of the atoms in the periodic chart, e.g., GaAs, AlAs, InP are called III-V (three-five) semiconductors." Ex-1025, 6, 49-52, 540-41.

XIII. CONCLUSION

236. For the reasons set forth in Sections XI-XII, it is my opinion that one skilled in the art would have found claims 1-14 of the '755 patent to be anticipated or obvious.

237. In signing this declaration, I understand that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I acknowledge that I may be subject to cross-examination in this case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

238. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Date: October 22, 2024

Respectfully submitted,

A handwritten signature in black ink, appearing to read 'Yuji Zhao', written in a cursive style.

Yuji Zhao, PhD