

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE AMERICA, INC.,
PETITIONER,

V.

INFINEON TECHNOLOGIES AUSTRIA AG,
PATENT OWNER.

IPR2025-00010
U.S. Patent 9,070,755

PETITION FOR *INTER PARTES* REVIEW

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LIST OF EXHIBITS

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Ex-1001	U.S. Patent No. 9,070,755 (“the ’755 patent”)
Ex-1002	Excerpts from Prosecution History of the ’755 Patent
Ex-1003	Expert Declaration of Dr. Yuji Zhao (“Zhao”)
Ex-1004	Curriculum Vitae of Dr. Yuji Zhao
Ex-1005	U.S. Patent No. 5,523,599 to Fujishima et al. (“Fujishima”)
Ex-1006	U.S. Patent No. 5,910,670 to Ludikhuize (“Ludikhuize”)
Ex-1007	U.S. Patent Publication No. 2006/0091498 to Sriram et al. (“Sriram”)
Ex-1008	U.S. Patent No. 7,417,257 to Beach et al. (“Beach”)
Ex-1009	U.S. Patent Publication No. 2006/0255403 Asano et al. (“Asano”)
Ex-1010	Kanamura et al., <i>High power and high gain AlGaIn/GaN MIS-HEMTs with high-k dielectric layer</i> , Phys. Stat. Sol., 5, No. 6, 2037–2040 (2008)
Ex-1011	Okino et al., <i>Drain Current DLTS of AlGaIn–GaN MIS-HEMTs</i> , IEEE Electron Device Letters, Vol. 25, No. 8 (2004)
Ex-1012	Imada et al., <i>Enhancement-Mode GaN MIS-HEMTs for Power Supplies</i> , The 2010 International Power Electronics Conference (2010)
Ex-1013	U.S. Patent Publication No. US2011/0073912 to Marui et al.
Ex-1014	U.S. Patent Publication No. US2010/0171150 to Smith et al.
Ex-1015	U.S. Patent Publication No. US2012/0146097 to Endo et al.
Ex-1016	U.S. Patent Publication No. US2009/0278236 to Sato et al.

Exhibit	Description
Ex-1017	U.S. Patent Publication No. US2010/0193842 to Sato et al.
Ex-1018	Excerpts from Rudiger Quay, Gallium Nitride Electronics (2008)
Ex-1019	Mishra et al., <i>AlGaN/GaN HEMTs—An Overview of Device Operation and Applications</i> , <i>Proceedings of the IEEE</i> , Vo. 90, No. 6 (2002)
Ex-1020	Wu et al., <i>Very-High Power Density AlGaIn/GaN HEMTs</i> , <i>IEEE Transactions on Electronic Devices</i> , Vol. 48, No. 3 (2001)
Ex-1021	S.H. Lee et al., <i>700V Lateral DMOS with New Source Fingertip Design</i> , <i>Proceedings of the 20th International Symposium on Power Semiconductor Devices & IC's</i> (2008)
Ex-1022	Excerpts from Prosecution History of the U.S. Patent No. 9,564,498 (the “’498 patent”)
Ex-1023	U.S. Patent Publication No. 2004/0178443 (“Hossain 443”)
Ex-1024	U.S. Patent Publication No. 2011/0121389 (“De Boet”)
Ex-1025	Excerpts from Umesh K. Mishra et al., <i>Semiconductor Device Physics and Design</i> (2008)
Ex-1026	Public Version of Ex. 36C to Infineon’s ITC Complaint - Domestic Industry Claim Chart for ’755 Patent
Ex-1027	Steven Leibson, <i>A Brief History of the MOS transistor, Part 1: Early Visionaries</i> , <i>Electronic Engineering Journal</i> (Apr. 3, 2023), https://www.eejournal.com/article/a-brief-history-of-the-mos-transistor-part-1-early-visionaries/
Ex-1028	R. P. Jindal, <i>Noise Associated with Distributed Resistance of MOSFET Gate Structures in Integrated Circuits</i> , <i>IEEE Transactions on Electron Devices</i> , Vol. ED-31, No. 10 (October 1984)

Exhibit	Description
Ex-1029	Evangelos F. Tsakas et al., <i>Noise Associated with Interdigitated Gate Structures in RF Submicron MOSFETs</i> , IEEE Transactions on Electron Devices, Vol. 47, No. 9 (September 2000)
Ex-1030	Order Staying and Conditionally Closing Case, Infineon Tech. Austria AG v. Innoscience (Suzhou) Tech. Company, Ltd., No. 4:24-cv-01553 (N.D. Ca. Aug. 30, 2024), ECF No. 56
EX-1031	Infineon's Preliminary Response, Innoscience America, Inc. v. Infineon Techs. Austria AG, No. IPR2024-00975 (PTAB Sept. 20, 2024), Pap. No. 6
EX-1032	Hiroshi Iwai et al., <i>The Transistor was Invented 75 Years Ago: A Big Milestone in Human History</i> , The Electrochemical Society Interface (Winter 2022)
EX-1033	Cassiano Ferro Moraes, <i>Understanding Transistors: What They Are and How They Work</i> , Wevolver (Nov. 6, 2023), https://www.wevolver.com/article/understanding-transistors-what-they-are-and-how-they-work
EX-1034	RS, <i>A Complete Guide to MOSFET Transistors</i> (Jan. 16, 2023), https://uk.rs-online.com/web/content/discovery/ideas-and-advice/mosfet-guide
EX-1035	A. Blicher et al., Encyclopedia of Physical Science and Technology, Vol. 5, p. 831-849 (Robert A. Meyers, 3d. ed. 2003)
EX-1036	D. W. Runton et al., <i>History of GaN</i> , IEEE Microwave Magazine (May 2013)
EX-1037	Qorvo, <i>What You Need to Know About GaN Technology</i> (Feb. 15, 2023), https://www.qorvo.com/design-hub/blog/what-you-need-to-know-about-gan-technology
EX-1038	W. F. Perina et al., <i>Effect of interface traps on the different conduction mechanisms of MISHEMT from 200 K to 450 K</i> , 2024

Exhibit	Description
	38th Symposium on Microelectronics Technology and Devices (SBMicro) (Sept. 2024)
EX-1039	Jui-Sheng Wu et al., <i>Recent Progress of E-mode Gallium Nitride Metal–Insulator–Semiconductor -High Electron Mobility Transistors with Hybrid Ferroelectric Charge Trap Gate (FEG-HEMT) for Power Switching Applications</i> , Physica Status Solidi (a) - Applications and Materials Science, Vol. 220, No. 16 (Aug. 2023)
EX-1040	Sonu Daryanani, <i>GaN Power HEMT > 650 V: A Parametric Analysis and Comparison to SiC MOSFET</i> , Power Electronics News (Jun. 23, 2022), https://www.powerelectronicsnews.com/gan-power-hemt-650-v-a-parametric-analysis-and-comparison-to-sic-mosfet/
EX-1041	U.S. Patent Publication No. 2005/0127438 (“Hossain 438”)
EX-1042	Enrico Bottaro et al., <i>Circuit Models of Power MOSFETs Leading the Way of GaN HEMT Modelling—A Review</i> , Energies 2022, 15, 2415 (May 7, 2022)
EX-1043	Utkarsh Jadli, <i>Modeling Power GaN-HEMTs Using Standard MOSFET Equations and Parameters in SPICE</i> , Electronics 2021, 10, 130 (January 9, 2021)
EX-1044	Shreepad Karmalkar, <i>A New Equivalent MOSFET Representation of a HEMT to Analytically Model Non-Linear Charge Control for Simulation of HEMT Devices and Circuits</i> , IEEE Transactions on Electron Devices, Vol. 44, No. 5 (May 1997)

I. INTRODUCTION

Petitioner requests cancellation of claims 1-14 of the '755 patent, which alleges priority to 2012 and claims a transistor with interdigitated source and drain finger electrodes.

Independent claims 1 and 10 require a drain finger electrode having an end portion that is non-coplanar (e.g., elevated) to the rest of the electrode. Dependent claims 2-9 and 11-13 recite well known elements: (i) using a dielectric material under the end portion, (ii) conventional electrode design features, such as extending the drain electrode end portion or making it ellipsoidal, and (iii) applying the non-coplanar design to a HEMT or group III-V transistor—specific types of transistors, which were conventional by 2012.

The '755 patent issued without the Office asserting any prior art rejections. Notably, during prosecution of a continuation of the '755 patent, the Office rejected proposed claims substantially similar to the '755 patent claims as anticipated or rendered obvious solely by Fujishima—one of the primary references applied in this Petition. The applicant overcame Fujishima by amending the claims to include a limitation not found in the '755 patent claims.

The Petitioner also presents a second primary reference—Asano—that anticipates or renders obvious a majority of the '755 patent claims.

II. RELIEF REQUESTED

Petitioner requests review under the following:

Exhibit	Prior Art
Ex-1005	Fujishima (filed on 2/14/1994 and issued on 6/4/1996) qualifies as prior art under pre-AIA 35 U.S.C. §§102(a)-(b) and (e).
Ex-1006	Ludikhuize (filed on 12/22/1997 and issued on 6/8/1999) qualifies as prior art under pre-AIA 35 U.S.C. §§102(a)-(b) and (e).
Ex-1007	Sriram (filed on 10/29/2004 and published on 5/4/2006) qualifies as prior art under pre-AIA 35 U.S.C. §§102(a)-(b) and (e).
Ex-1008	Beach (filed on 12/13/2006, published on 4/26/2007, and issued on 8/26/2008) qualifies as prior art under pre-AIA 35 U.S.C. §§102(a)-(b) and (e).
Ex-1009	Asano (filed on 4/27/2006 and published on 11/16/2006) qualifies as prior art under pre-AIA 35 U.S.C. §§102(a)-(b) and (e).

Grounds		Challenged Claims	Basis	Prior Art
Fujishima Grounds	1A	1-5, 8-14	§102	Fujishima
	1B	1-14	§103	Fujishima
	1C	6-7	§103	Fujishima and Ludikhuizen
	1D	8-9, 14	§103	Fujishima and Sriram
	1E	13	§103	Fujishima and Beach
Asano Grounds	2A	1-4, 8-9	§102	Asano
	2B	1-4, 8-9	§103	Asano

Zhao ¶69.

III. TECHNOLOGY OVERVIEW

A. History of Transistors

Field-Effect Transistors (FETs), developed in the 1920s, are a key technology in modern electronics and used extensively in various electronic devices. Zhao ¶48; Ex-1027. MISFETs, emerging in the 1960s, are a type of FET that provides an insulating layer to improve device control. *Id.* Thereafter, MOSFETs (Metal-Oxide-Semiconductor FETs), a type of MISFET, were developed and are still one of the dominant transistor types. *Id.* MOSFETs are considered MISFETs because they include an insulating layer (e.g., silicon dioxide layer). Zhao ¶48.

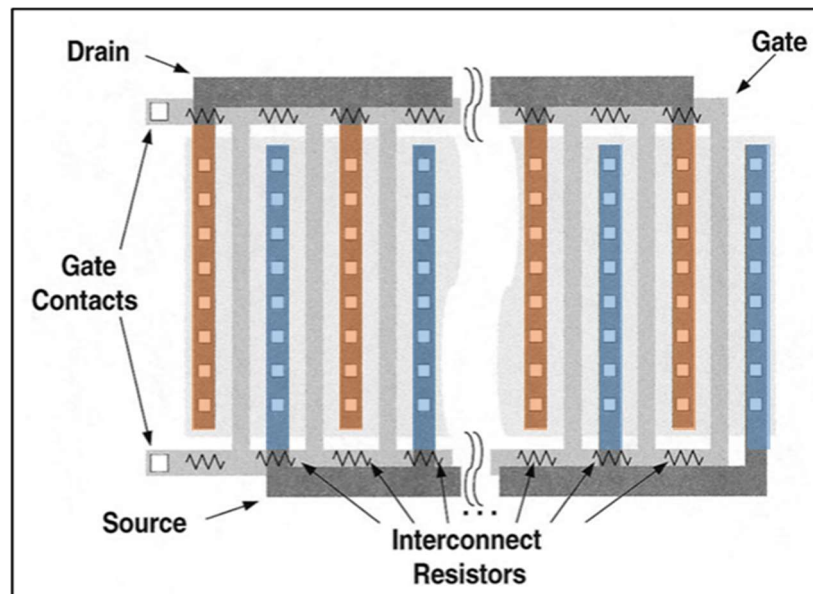
In the 1990s, GaN HEMTs, another type of FET, were introduced, providing higher-power and higher-frequency performance. Zhao ¶49. Thereafter, GaN

MIS-HEMTs, which combines features of GaN HEMTs and MISFETs, were developed and commercialized in the early 2000s. *Id.*

B. Electrode Structure Commonalities

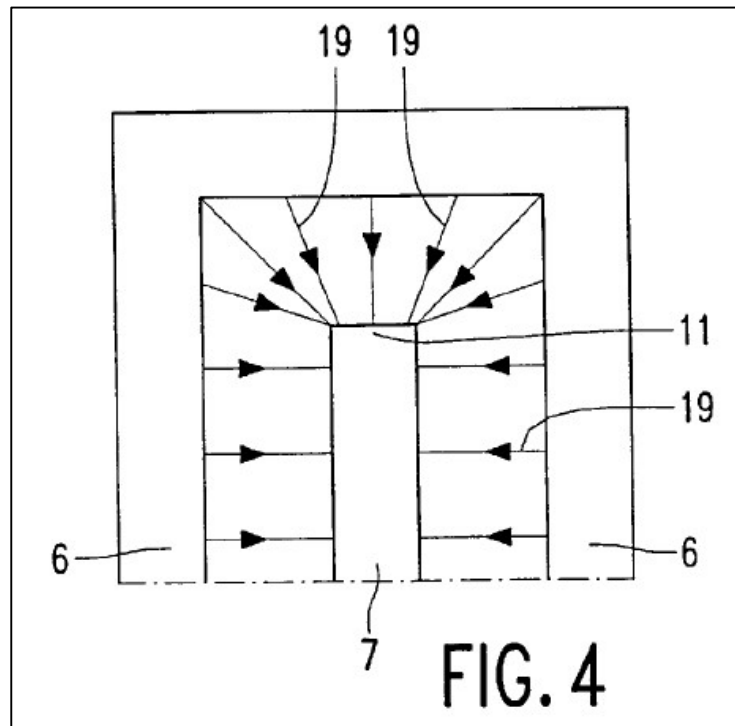
FETs, including MISFETs, MOSFETs, GaN HEMTs, and GaN MIS-HEMTs, share a basic electrode structure that facilitates current control including (i) a source electrode where charge carriers originate, (ii) a drain electrode where charge carriers exit, and (iii) a gate electrode that controls the charge carrier flow between the source and drain. Zhao ¶50.

FETs can have an interdigitated structure design with **source** and **drain** electrodes having finger-like portions alternatively repeating, as shown below, which provides device benefits.

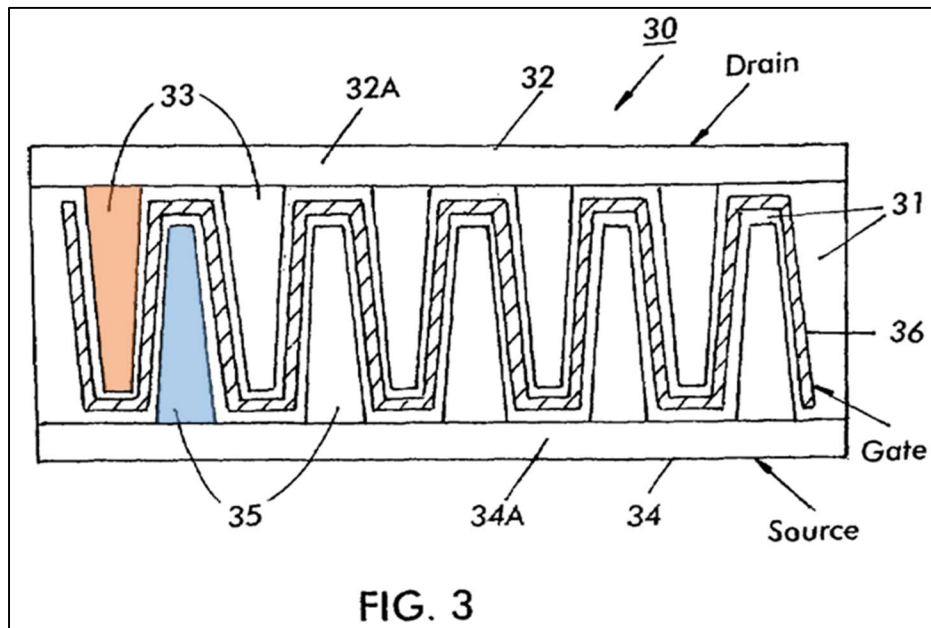


Ex-1029, 1746; Zhao ¶51.

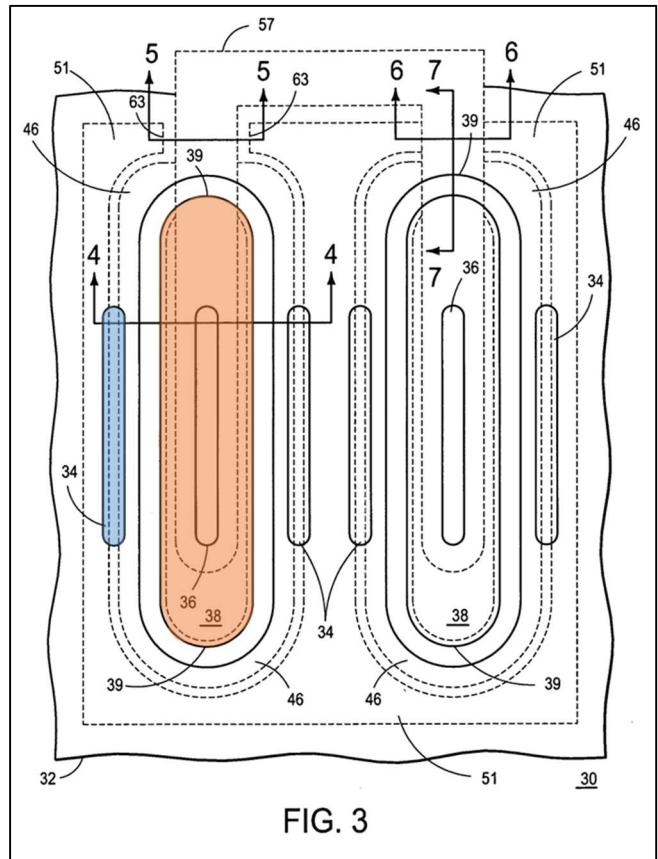
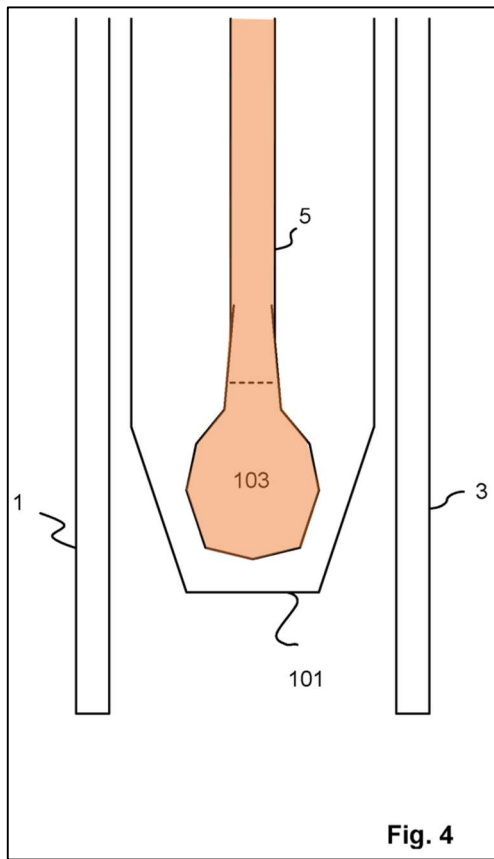
One problem was current convergence at the drain finger electrode *end* causing increased electric field and creating device issues. Ludikhuize, 4:4-26, Fig. 4; Zhao ¶52.



Ludikhuize, Fig. 4. It was also well known to change the drain finger electrode geometry to address this issue. Zhao ¶53. A 2007 patent described tapered fingers for controlling high currents at the end portions. Beach, Fig. 3, Claim 1, Abstract, 5:57-6:11.

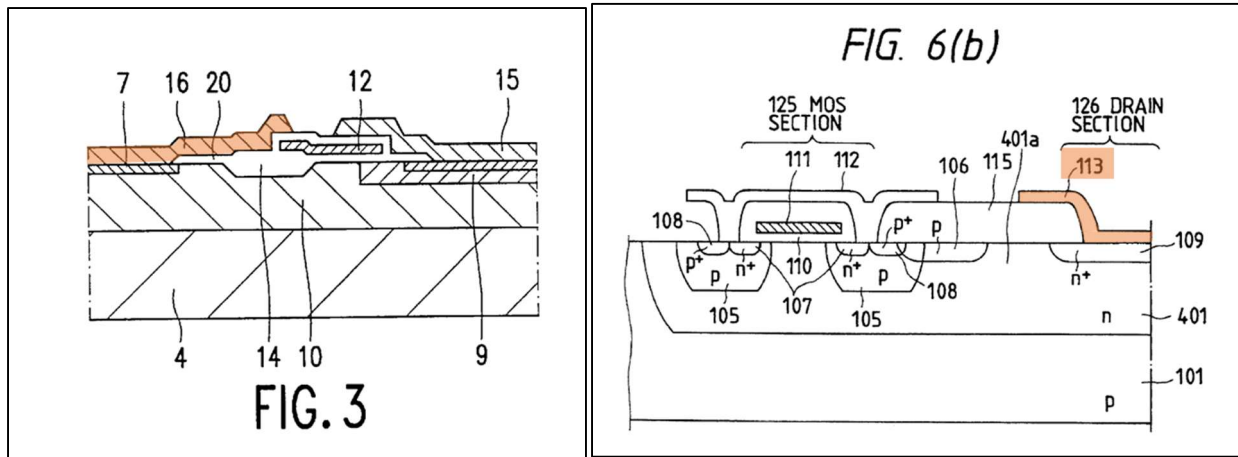


Id. Fig. 3 (showing **drain** and **source** electrodes), Claim 1, Abstract, 5:57-6:11. A 2011 publication disclosed increasing the curvature of the end portion of a **drain electrode** to reduce the electric field at the end and a 2005 publication disclosed longer **drain electrodes** extending past the **source electrodes** for the same purpose. Ex-1024 ¶¶37-38; Ex-1041 ¶¶20, 5, 16, 35.

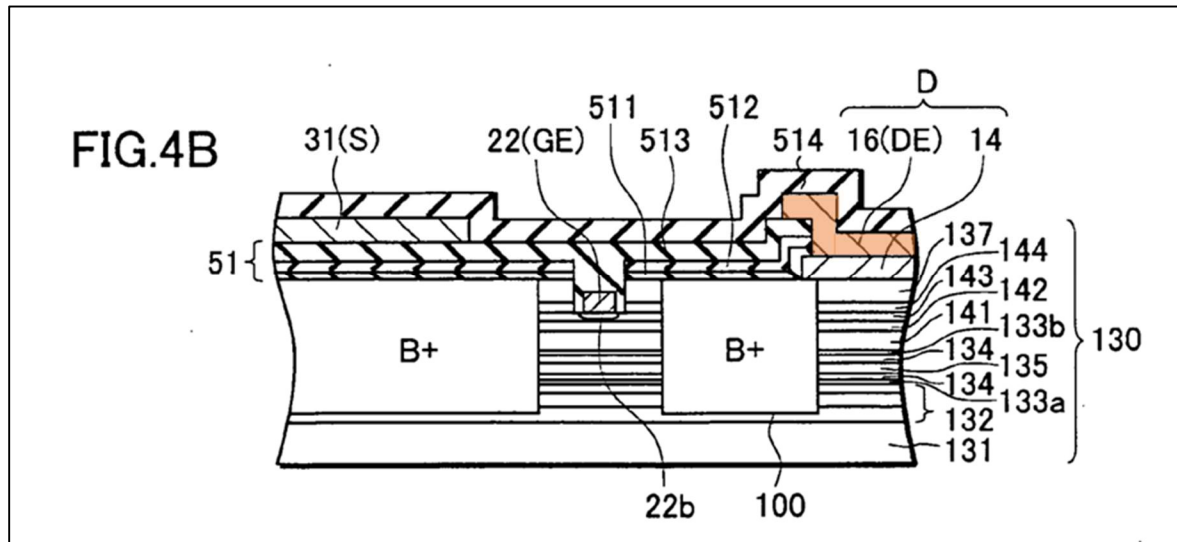


Ex-1024, Fig. 4 (annotated); Ex-1041, Fig. 3 (annotated); Zhao ¶¶54-55.

A 1999 patent, Ludikhuize, and a 1996 patent, Fujishima, describe elevating the end portion of the **drain finger** to alleviate the electric field. Fujishima, 8:59-9:2, 10:66-11:8, 12:27-32; Ludikhuize, Figs. 1, 3, 4:43-57.



Ludikhuize, Fig. 3; Fujishima, Fig. 6(b) (annotated); Zhao ¶¶56-57. A 2006 publication, Asano, depicts a similar configuration, which a POSA would have understood to have the same effect. Zhao ¶58.



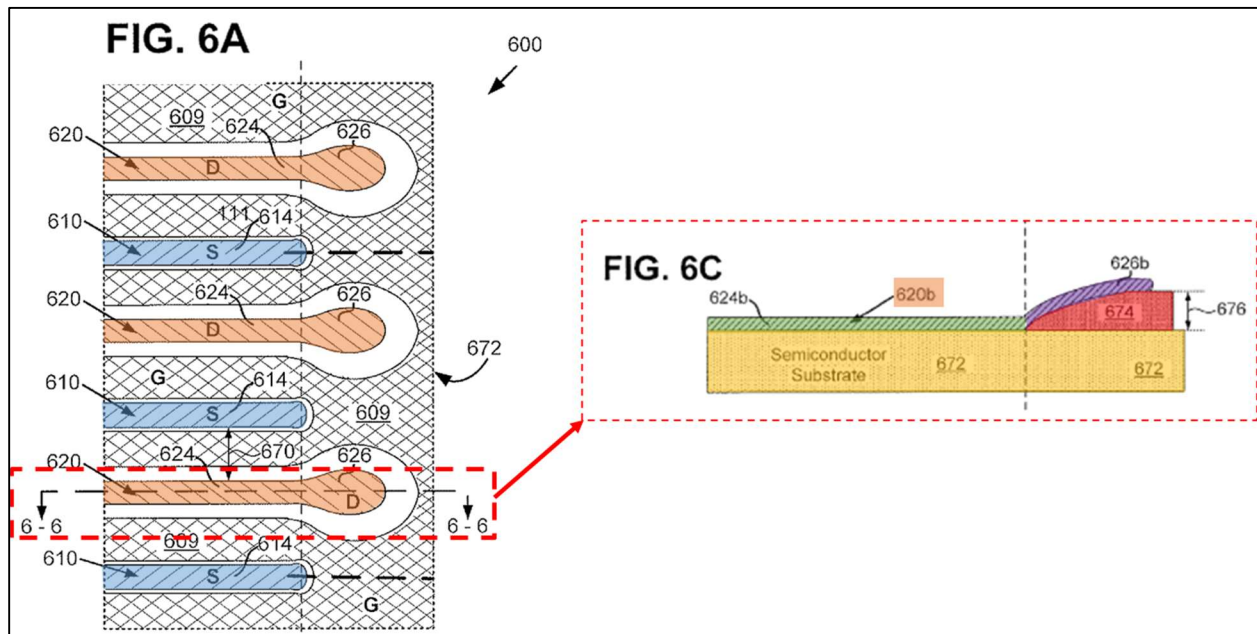
Asano, Fig. 4B.

IV. '755 PATENT

A. Overview

The '755 patent describes an electrode structure addressing “high termination electric fields” “present at the drain finger electrode ends” which reduce the device breakdown voltage. '755 Pat., 2:17-21, 2:24-29, Abstract. Its electrode structure applies to all types of “field-effect transistor (FET),” including a (i) “high-electron-mobility transistor (HEMT)” and (ii) “metal-insulator-semiconductor FET (MISFET), such as a metal-oxide-semiconductor FET (MOSFET),” among others. '755 Pat., 3:55-4:3, 2:2-7, 1:28-55.

Figure 6A shows **drain finger electrodes 620** and **source finger electrodes 610** and Figure 6C shows a **drain finger electrode** with a **main body portion 624b** and **end portion 626b**, which is elevated over a **substrate 672** using a **dielectric material 674**.



The '755 patent discloses additional electrode structure designs, including (i) the **end portion** having an ellipsoid shape ('755 Pat., 5:27-42), (ii) the **end portion** extending past the main body of a **source finger electrode** (*id.*, 5:43-51), and (iii) **drain finger electrodes** longer than **source finger electrodes** (*id.*). The '755 patent also describes a tapered **drain finger electrode** but concedes that “tapered source and drain finger designs [were] described” in Beach four years before the alleged time of invention. *Id.*, 8:43-55; Zhao ¶¶59-61.

B. Relevant Prosecution History

During prosecution, the examiner issued no rejections, and the Notice of Allowance analyzes no prior art. Ex-1002, pgs. 5-18.

After issuance, applicant filed a Continuation Application No. 14/750,262 (eventually issuing as the '498 patent). Ex-1022, pgs. 1-56. During prosecution of

the continuation, the examiner finally rejected proposed claims over Fujishima. *Id.*, pgs. 70-73. The rejected claims are substantially similar to the '755 patent claims:

'755 Patent Claims	Proposed '498 Patent Claims Rejected over Fujishima in Prosecution of '498 Patent
10. A transistor comprising: drain finger electrodes interdigitated with source finger electrodes; a gate region configured to control current conduction in a semiconductor substrate between said drain finger electrodes and said source finger electrodes; at least one of said drain finger electrodes having a drain finger electrode end and a drain finger electrode main body, wherein at least a portion of said drain finger end is non-coplanar with said drain finger electrode main body; wherein an increasing thickness dielectric material is situated between at least said portion of said drain finger electrode end and said semiconductor substrate.	10. A transistor comprising: drain finger electrodes and source finger electrodes situated on a semiconductor substrate; said drain finger electrodes interdigitated with source finger electrodes; a gate region configured to control current conduction in said semiconductor substrate between said drain finger electrodes and said source finger electrodes; at least one of said drain finger electrodes having a drain finger electrode main body and a drain finger electrode end having an increased elevation relative to said drain finger electrode main body; wherein a dielectric material insulates said drain finger electrode end from said semiconductor substrate.
11. The transistor of claim 10, wherein said increasing thickness dielectric	11. The transistor of claim 10, wherein said dielectric material provides said

material elevates said drain finger electrode end over said semiconductor substrate. <i>*The scope of claims 1-3 are covered by the scope of claims 10-11.</i>	increased elevation of said drain finger electrode end relative to said drain finger electrode main body.
4. The transistor of claim 1, wherein said <i>drain finger electrode main body is situated on said semiconductor substrate.</i>	21. The transistor of claim 10, wherein said <i>drain finger electrode main body is situated on said semiconductor substrate.</i>
6. The transistor of claim 1, <i>wherein at least one of said source finger electrodes has a source finger electrode main body coupled to a source pad, said drain finger electrode end extending beyond said source finger electrode main body.</i>	13. The transistor of claim 10, <i>wherein at least one of said source finger electrodes has a source finger electrode main body coupled to a source pad, said drain finger electrode end extending beyond said source finger electrode main body.</i>
7. The transistor of claim 1, <i>wherein said drain finger electrodes are longer than said source finger electrodes.</i>	14. The transistor of claim 10, <i>wherein said drain finger electrodes are longer than said source finger electrodes.</i>
'755 Patent Claims	Proposed Claims Rejected as Obvious over Fujishima in Prosecution of '498 Patent
14. The transistor of claim 10, <i>wherein said transistor is a high-electron-mobility transistor (HEMT).</i> <i>*The scope of claim 8 is covered by the scope of claim 14.</i>	22. The transistor of claim 10, <i>wherein said transistor is a high-electron-mobility transistor (HEMT).</i>
9. The transistor of claim 1, <i>wherein said transistor comprises a group III-V transistor.</i>	23. The transistor of claim 10, <i>wherein said transistor comprises a group III-V transistor.</i>

'755 Patent Claims¹	Proposed Claims Rejected as Obvious over Fujishima and Hossain 443 in Prosecution of '498 Patent
5. The transistor of claim 1, <i>wherein said drain finger electrode end has an increased radius of curvature.</i>	12. The transistor of claim 10, <i>wherein said drain finger electrode end has an increased radius of curvature.</i>
12. The transistor of claim 10, <i>wherein said drain finger electrode end is substantially an ellipsoid.</i>	24. The transistor of claim 10, <i>wherein said drain finger electrode end is substantially an ellipsoid.</i>
13. The transistor of claim 10, <i>wherein said drain finger electrode is a tapered drain finger electrode.</i>	25. The transistor of claim 10, <i>wherein said drain finger electrode is a tapered drain finger electrode.</i>

'755 Pat., 11:17-12:35; Ex-1022, pgs. 70-73, 58-60.

In response, applicant amended the independent claim to recite an additional limitation that the “drain finger electrodes extend[] beyond said source finger electrodes so as to be situated closer to said source pad than said source finger electrodes”—a limitation not present in any of the '755 patent claims. Ex-1022, 77. The applicant’s only rebuttal to the examiner’s Fujishima rejection mimicked its claim amendment, noting that Fujishima failed to disclose the additional limitation. *Id.*, pgs. 82-83. The examiner issued an allowance relying upon the prior art’s failure to disclose this additional limitation. *Id.*, pg. 94.

¹ As explained in Sections VII.A.6, VII.A.13, and VII.A.14, the examiner erred in finding that Fujishima does not disclose or render obvious these limitations.

V. LEVEL OF ORDINARY SKILL

A person of ordinary skill in the art (“POSA”) would have possessed at least a four-year degree in electrical engineering or a closely related field, and at least two years of experience in semiconductor device design. Additional education could substitute for professional experience and vice versa. Zhao ¶¶66-68.

VI. CLAIM CONSTRUCTION

The Board construes claims per *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). For the purposes of this IPR, the plain meaning of each term can be applied. Zhao ¶¶62-65.

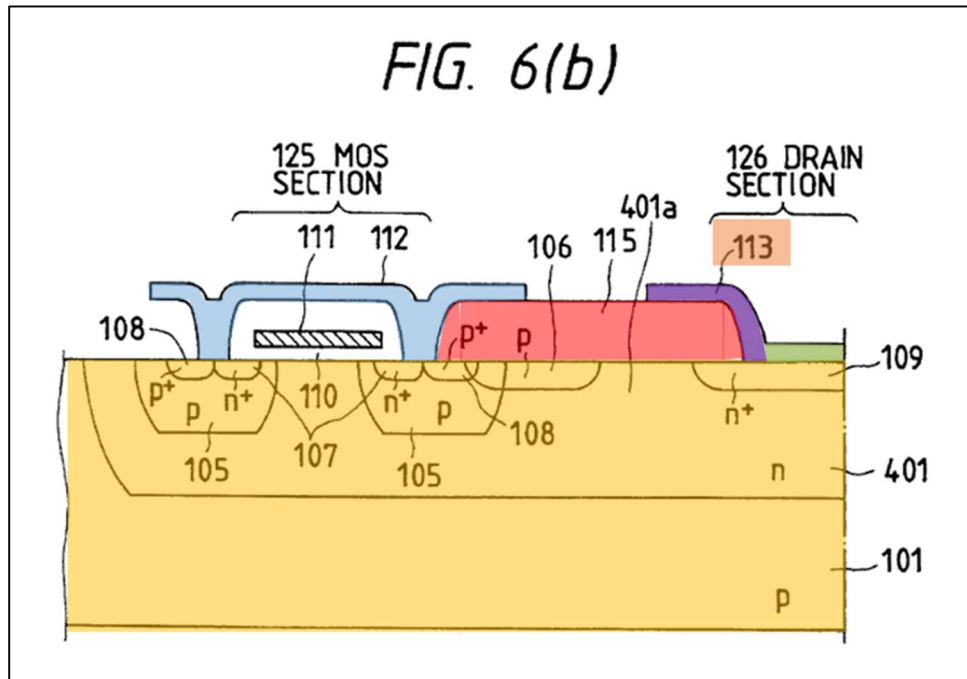
VII. FUJISHIMA GROUNDS 1A-1E ANTICIPATE AND/OR RENDER OBVIOUS CLAIMS 1-14.

A. Grounds 1A-1B: Fujishima Anticipates and/or Renders Obvious Claims 1-14.

1. Fujishima

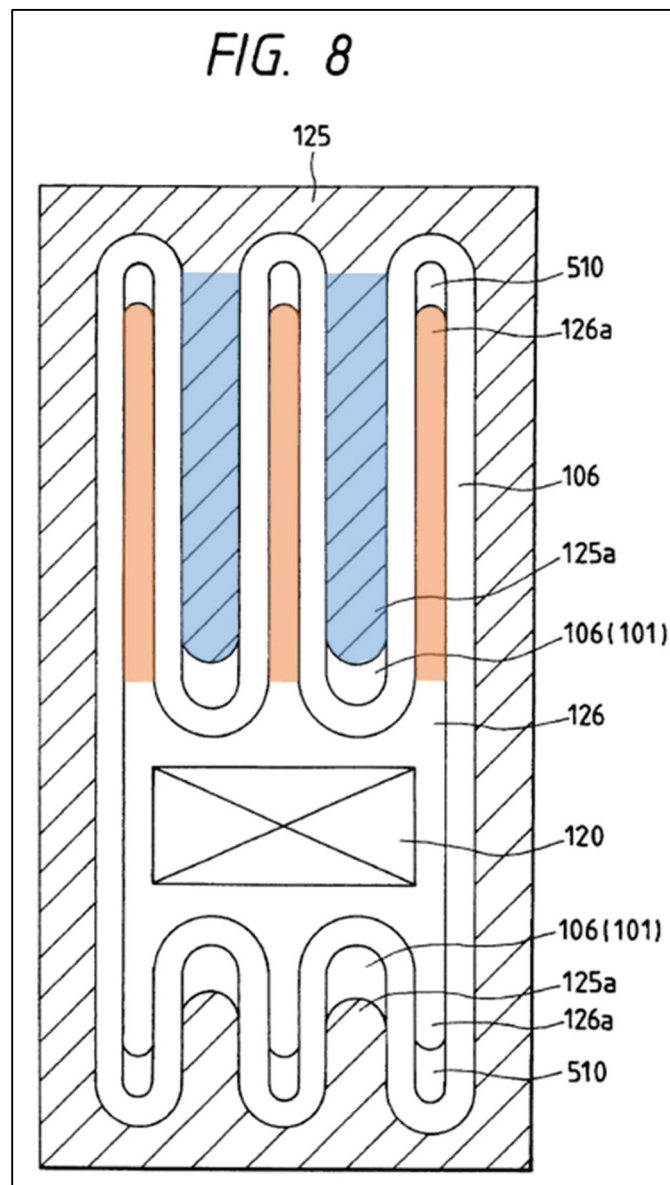
Fujishima discloses different configurations for a “Metal Insulator Semiconductor” field effect transistors—or MISFETs. Fujishima, 1:6-13; ’755 Pat., 3:56-65. Fujishima’s transistors minimize negative electric field effects at the drain finger electrodes’ ends by projecting the ends over an insulating film. Fujishima, 2:65-3:34, 3:44-52, 6:13-33, 12:23-40, 10:66-11:4, Fig. 6(b).

Figure 6(b) shows a MISFET comprising **a drain electrode** with **a main body** that is non-coplanar with an elevated **end portion**, **source electrode**, **substrate**, and **an insulating layer 115**.



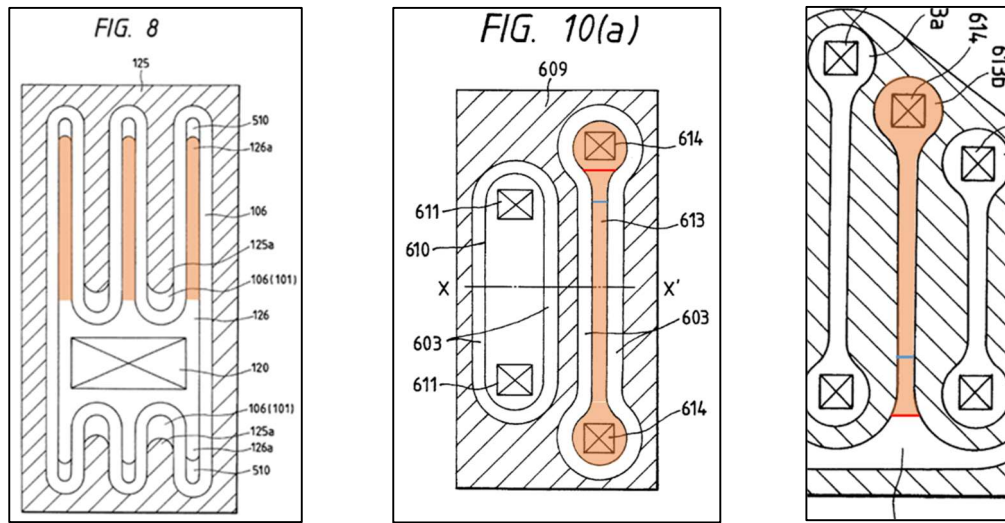
Id., Fig. 6(b) (annotated).

Figure 8's top view of the same MISFET depicts multiple **drain finger electrodes** and **source finger electrodes** “juxtaposed in an interdigitated manner” with current flowing in-between:



Id., Fig. 8 (annotated), 13:37-51; Zhao ¶¶70-74.

Fujishima discloses options for **drain finger electrode** designs, including (i) Figure 8's design, (ii) Figure 10(a)'s design with the **drain finger electrode end portion** tapering into an ellipsoid shape, and (iii) Figure 16's tapered **drain electrode** design. Fujishima, 5:14-22, 17:29-54; Zhao ¶¶75.



Fujishima, Figs. 8, 10(a) (annotated), Fig. 16 (annotated and excerpted).

2. Independent Claim 1

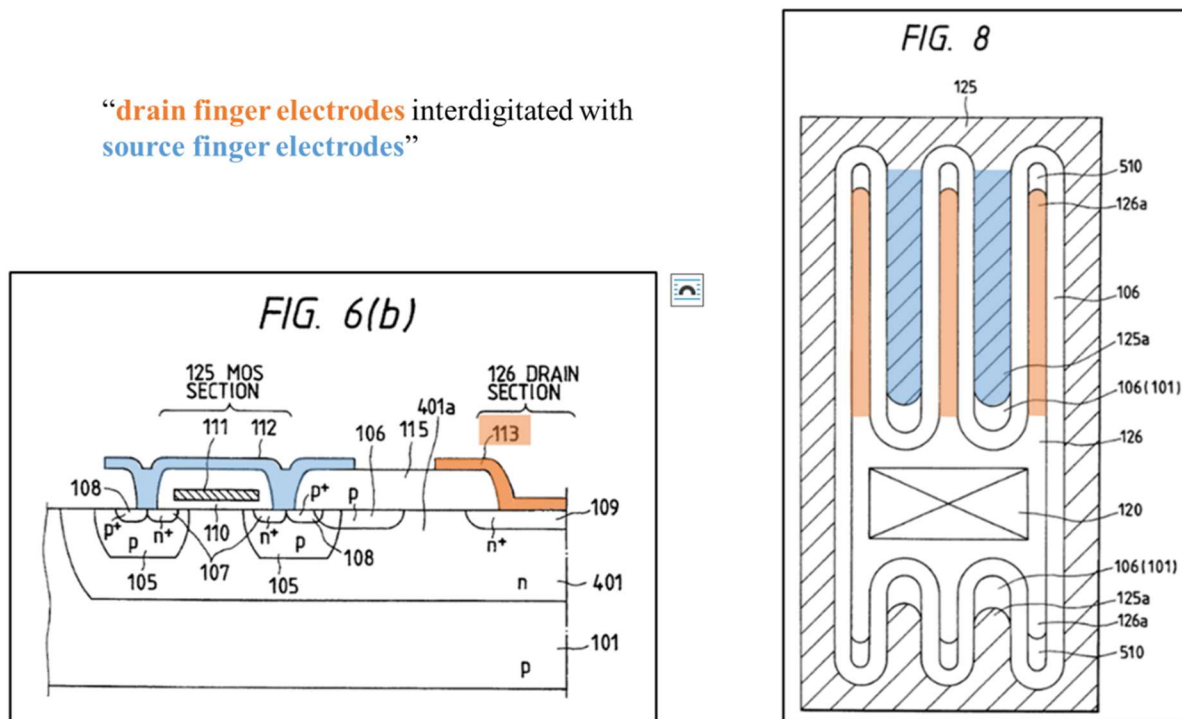
a. [1pre]: A transistor comprising:

If the preamble is limiting, Fujishima’s “high voltage MIS field effect *transistor*” discloses or renders obvious [1pre]. Fujishima, Abstract, 1:6-19, 13:37-40; Zhao ¶76.

b. [1a]: drain finger electrodes interdigitated with source finger electrodes;

Fujishima discloses [1a] because it discloses **drain finger electrodes** and **source finger electrodes** that “are juxtaposed in an interdigitated manner.” Fujishima, 15:9-24, Figs. 6(b), 8; Zhao ¶77.

Figure 6(b) shows a drain section 126 with **drain electrode 113** and a MIS section 125² with a **source electrode 112**. Fujishima, Fig. 6(b), 8:38-59, 1:19-22, 13:47-51, 15:9-16, 16:38-45; *see id.*, 10:66-11:4, Fig. 17. Figure 8 is a top view of the device in Figure 6(b), showing the “overall planar structure” including the **drain finger electrodes** and **source finger electrodes**. *Id.*, 13:41-44.

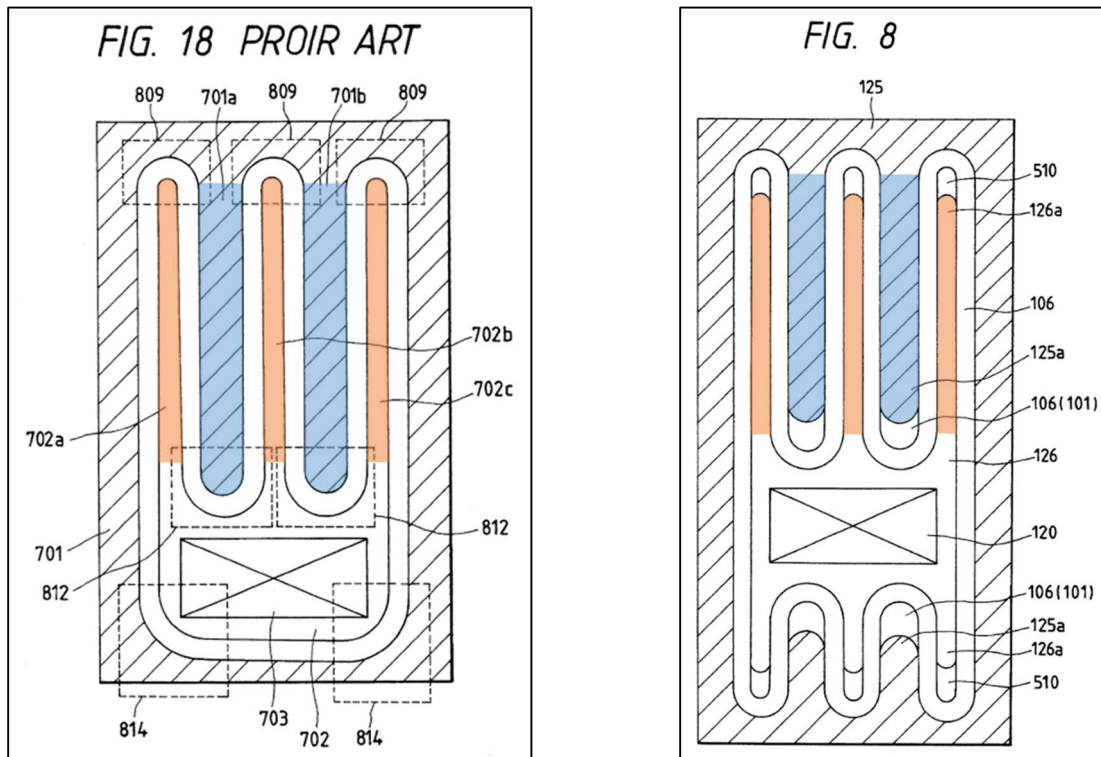


Fujishima, Figs. 6(b), 8 (annotated). Fujishima explains that the MIS Section 125 (including **source electrode 112**) and drain section 126 (including **drain electrode**

² Fujishima’s disclosures interchangeably use “MIS Section” and “MOS Section.”

113) “are juxtaposed in an interdigitated manner.” *Id.*, 15:9-24, Fig. 8; *see also* Ex-1028-1029; Zhao ¶78.

Fujishima’s Figure 18 provides additional context for Figure 8, as both figures disclose similar structures. Zhao ¶79.



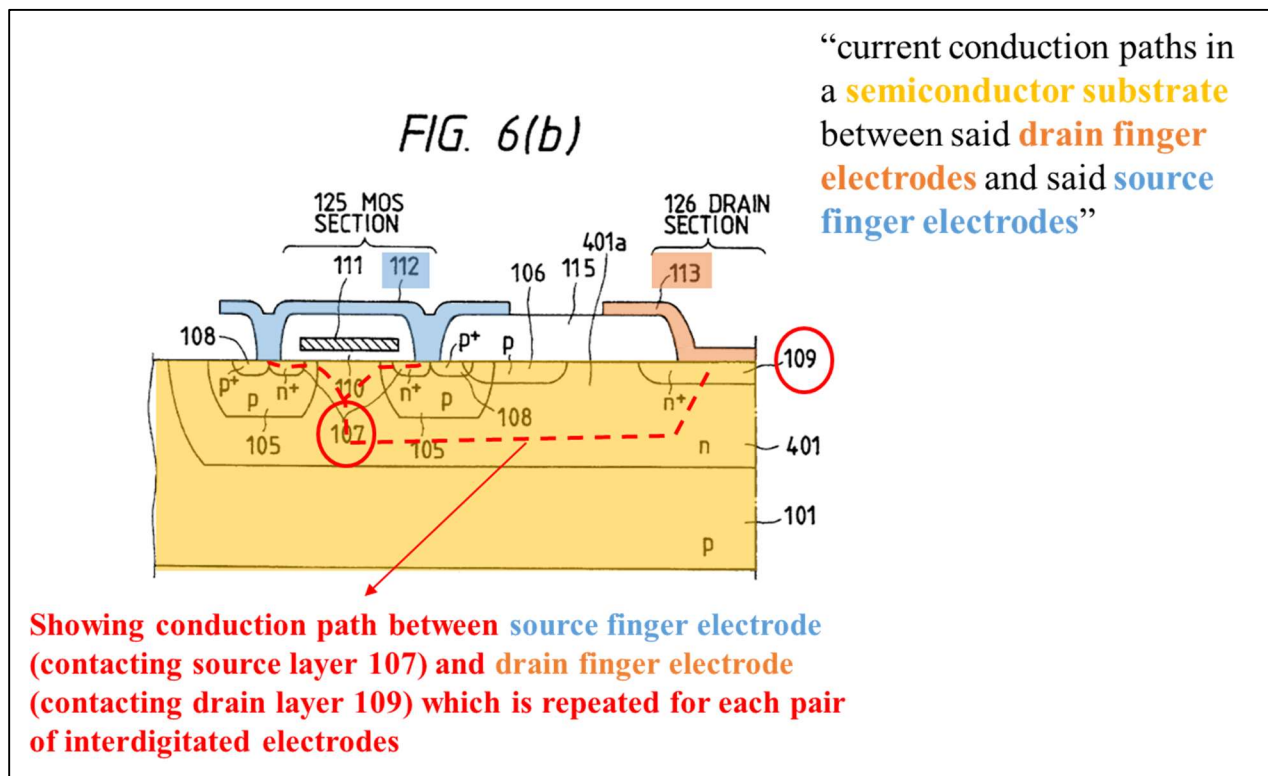
Fujishima, Figs. 18, 8 (annotated). Figure 18 discloses an input terminal region 701 and a drain output terminal region 702 that “interdigitated” with **three drain regions 702a to 702c (i.e., drain finger electrodes)** “formed between adjacent” **input terminal regions 701a to 701b (i.e., source finger electrodes)**. *Id.*, 1:30-44, Fig. 18 (showing drain finger ends 809 in an active area of the transistor with high electric field concentrations), 3:23-34; Zhao ¶79. Thus, a POSA would have understood

these disclosures further support that Figure 8 discloses **drain finger electrodes** interdigitated with **source finger electrodes**. Fujishima, Fig. 8 (showing drain finger ends in an active area of the transistor similar to Figure 18 with high electric field concentrations); Zhao ¶79.

c. [1b]: current conduction paths in a semiconductor substrate between said drain finger electrodes and said source finger electrodes;

Fujishima discloses or renders obvious [1c] because (i) it discloses current paths through the **substrate** between the **source finger electrodes** to the **drain finger electrodes** (**Ground 1A**) or (ii) a POSA would have understood that Fujishima's lateral MISFET includes current conduction paths between these **drain finger electrodes** and **source finger electrodes** (**Ground 1B**). Zhao ¶80.

Fujishima discloses a “current path” for electron charge carriers from the MIS section 125 (with **source electrode 112**) to the drain section 126 (with **drain electrode 113**). Fujishima, 5:62-67, Fig. 6(b); Zhao ¶81; *see* Fujishima, 5:46-48, 10:11-19, 10:43-52.



Fujishima, Fig. 6(b) (annotated). Specifically, electrons flow from the source layer 107 (connected to **source electrode 112**) to the drain layer 109 (connected to **drain electrode 113**)—causing current flow from the **drain** to the **source**.³ Fujishima, 12:19-40, 10:49-53, 8:59-63, Fig. 6(b); Zhao ¶82; see Fujishima, 2:29-37. Thus, a

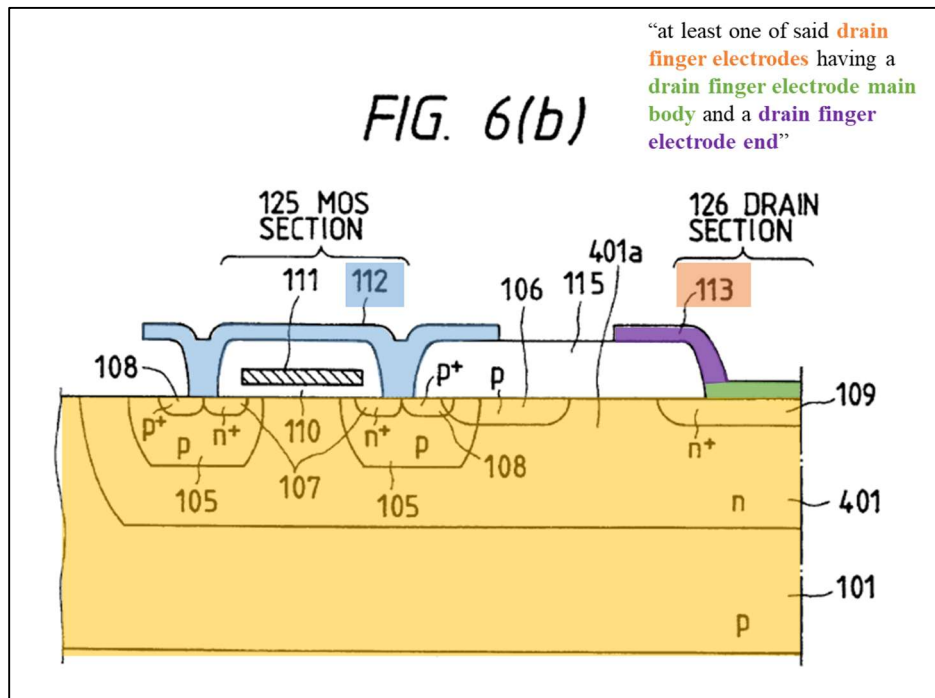
³ The '755 patent explains that the “semiconductor substrate” can be “a III-Nitride material stack, such as a HEMT material stack, silicon, and/or other semiconductor material.” '755 Pat., 9:34-37. Fujishima’s semiconductor substrate includes semiconductor material with various doped regions—all of which are formed in the substrate. Fujishima, Fig. 6(b), 8:41-46, 8:59-62; Zhao ¶82.

POSA would have understood that Fujishima's MISFET includes current conduction paths in the substrate between the **source finger electrodes** and **drain finger electrodes**, and that current conduction paths are provided in the substrate for all the interdigitated **drain finger electrodes** and **source finger electrodes**. Zhao ¶82; *see* Section VII.A.2.b. This is consistent with Infineon's statements in another IPR proceeding explaining that FETs generally include a gate electrode that "control[s] the flow of electrical current between the source and drain." Ex-1031, 7.

For Ground 1B, a POSA would have found it obvious that Fujishima's MISFETs practice limitation [1b], as a transistor's fundamental purpose is to control the flow of electrical current over a current conduction path between drain and source electrodes (Ex-1025, 356; EX-1031, 7) and, thus, Fujishima's MISFETs operate to enable charge carriers to flow over current conduction paths in the **substrate** between the **source finger electrodes** and **drain finger electrodes**. Zhao ¶83; *see* Section VII.A.2.b.

- d. **[1c]: at least one of said drain finger electrodes having a drain finger electrode main body and a drain finger electrode end,**

Fujishima discloses [1c] because its **drain electrode 113** has a **drain finger main body** and **drain finger electrode end**. *See* Fujishima, Fig. 6(b); Zhao ¶84.

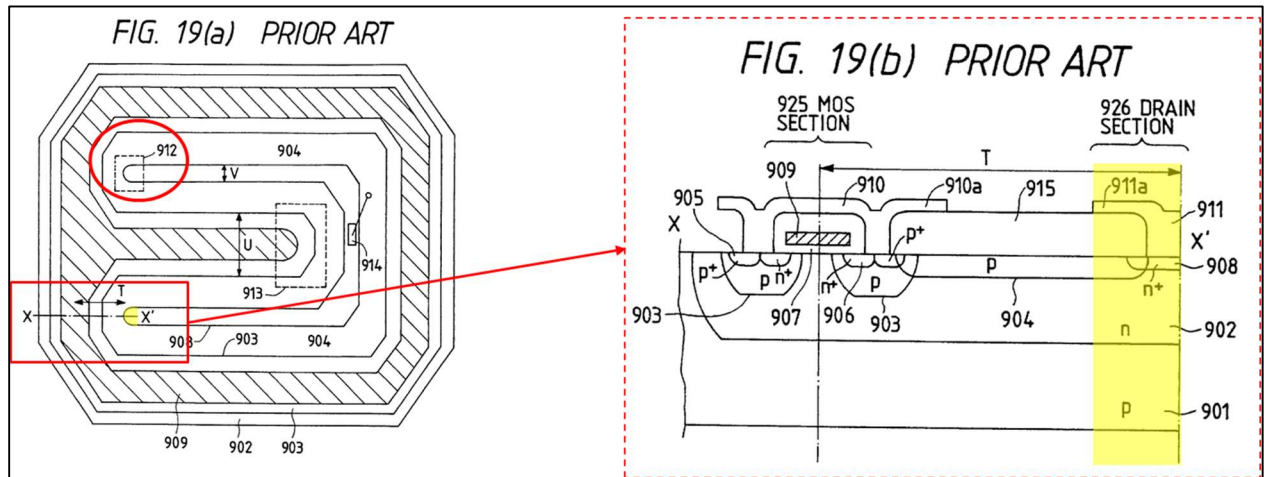


Fujishima, Fig. 6(b) (annotated).

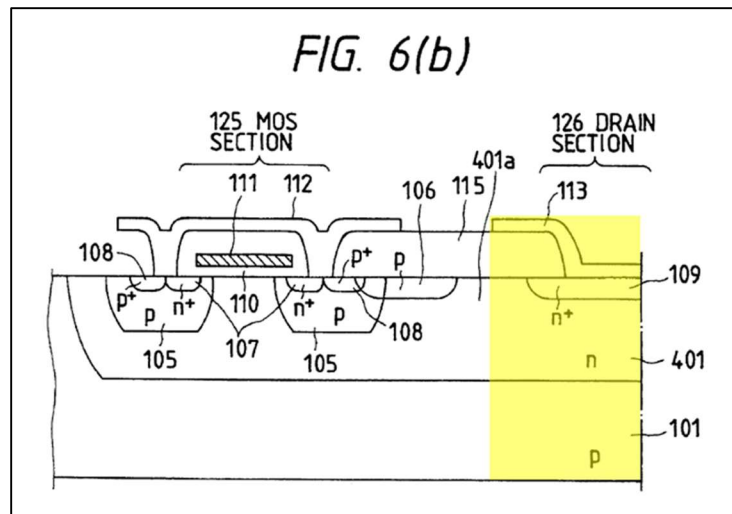
As Figure 6(b) shows, Fujishima’s **drain electrode 113** has two portions: (i) a **main body** that is situated on **substrate**; and (ii) an **end** that is elevated above the **substrate** such that a portion of the **end** is not on the same plane (i.e., non-coplanar) as the **main body**. Fujishima, 8:59-9:2, Figs. 1(b), 6(b); Zhao ¶85; *see* Fujishima, 13:37-51. This electrode structure alleviates the “concentration of the electric field at the” **end** enabling the device higher voltage-withstanding capability. Fujishima, 8:59-9:2, 14:14-28; Zhao ¶85.

Fujishima explains that Figure 6(b) provides a view of the “drain corner portion 912,” which is the “tip” of a drain electrode (as shown in a red circle in Figure 19(a) below) and has a high electric field concentration. Fujishima, 2:65-3:29,

Figs. 6(a)-6(b), 19(a)-19(b). Figure 19(b) shows a cross section of the drain corner portion of Figure 19(a), including the tip of the drain electrode, as indicated by the yellow highlighting:



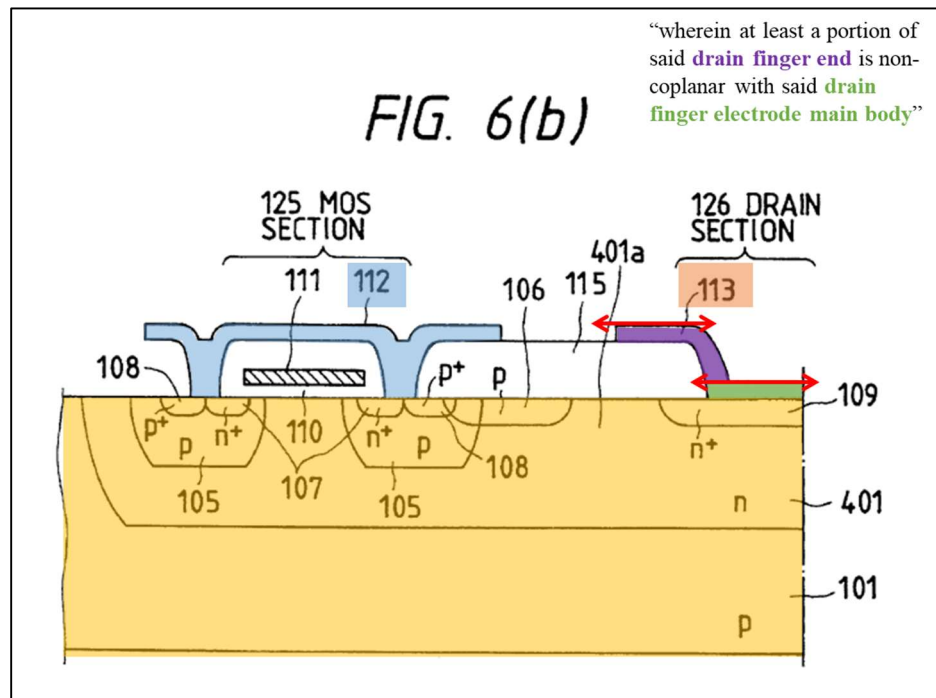
Fujishima, Figs. 19(a), 19(b) (annotated); Zhao ¶¶86-87. Figure 6(b) provides a cross section similarly showing the drain electrode tip:



Fujishima, Figs. 6(b) (annotated), 6(a).

- e. [1d]: wherein at least a portion of said drain finger end is non-coplanar with said drain finger electrode main body.

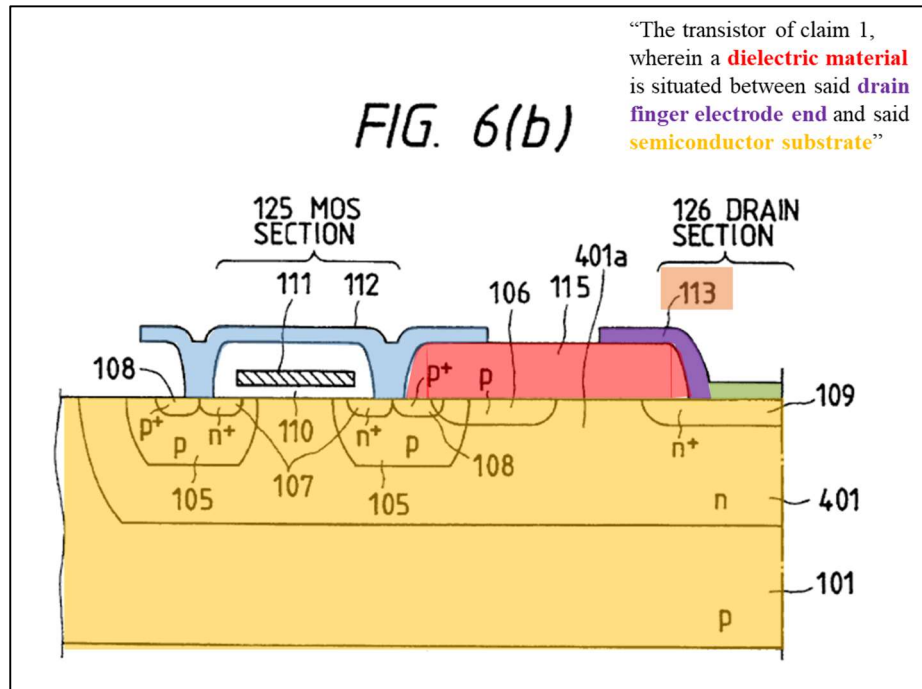
Fujishima discloses [1d] because the drain finger electrode end is non-coplanar with the drain finger electrode main body for at least the reasons explained for [1c]. Section VII.A.2.d; Fujishima, Fig. 6(b); Zhao ¶88.



Fujishima, Fig. 6(b) (annotated). As shown, at least a portion of the end is non-coplanar with respect to the main body because the end is on a horizontal plane that is not on the same horizontal plane as any part of the main body. *Id.*; Zhao ¶88. This configuration alleviates the electric field at the end. Fujishima, 12:23-31; Zhao ¶88; see Section VII.A.1.

3. **Claim 2 – The transistor of claim 1, wherein a dielectric material is situated between said drain finger electrode end and said semiconductor substrate.**

Fujishima discloses claim 2 because it discloses an **insulating film 115** situated between the **drain finger electrode end** and **substrate**.

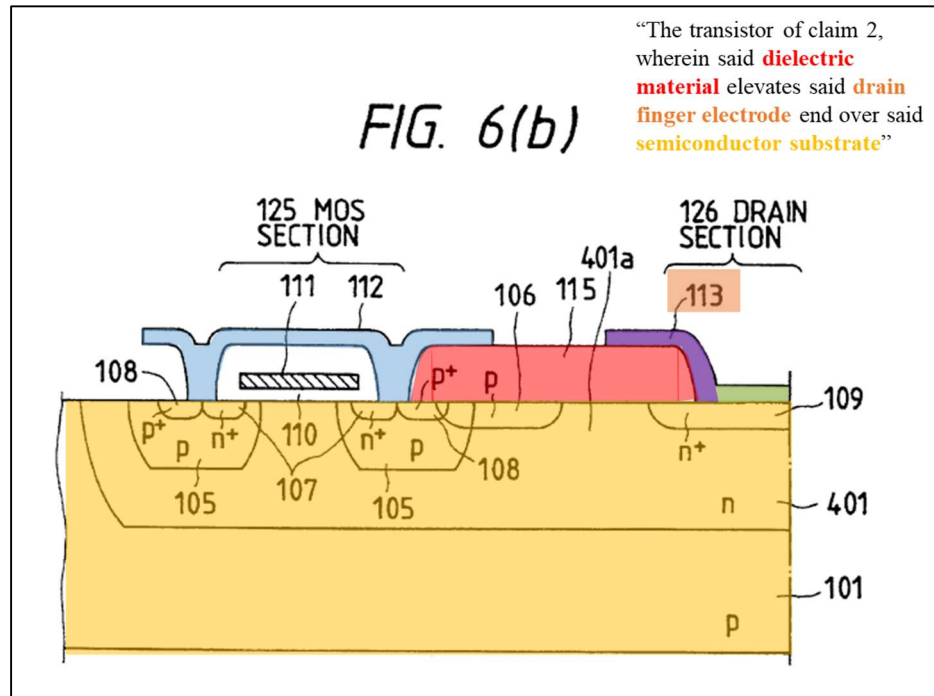


Fujishima, Fig. 6(b) (annotated); Zhao ¶89.

Figure 6(b) shows **insulating film 115** situated between the **end portion** and **substrate**. Fujishima, 8:59-9:2, Figs. 1(b), 6(b); Zhao ¶90; Sections VII.A.2.c-VII.A.2.d. The **insulating film** is a dielectric material under the '755 patent's description of such a material as any "insulating material." '755 Pat., 10:23-29, 10:10-22; Zhao ¶90.

4. **Claim 3 – The transistor of claim 2, wherein said dielectric material elevates said drain finger electrode end over said semiconductor substrate.**

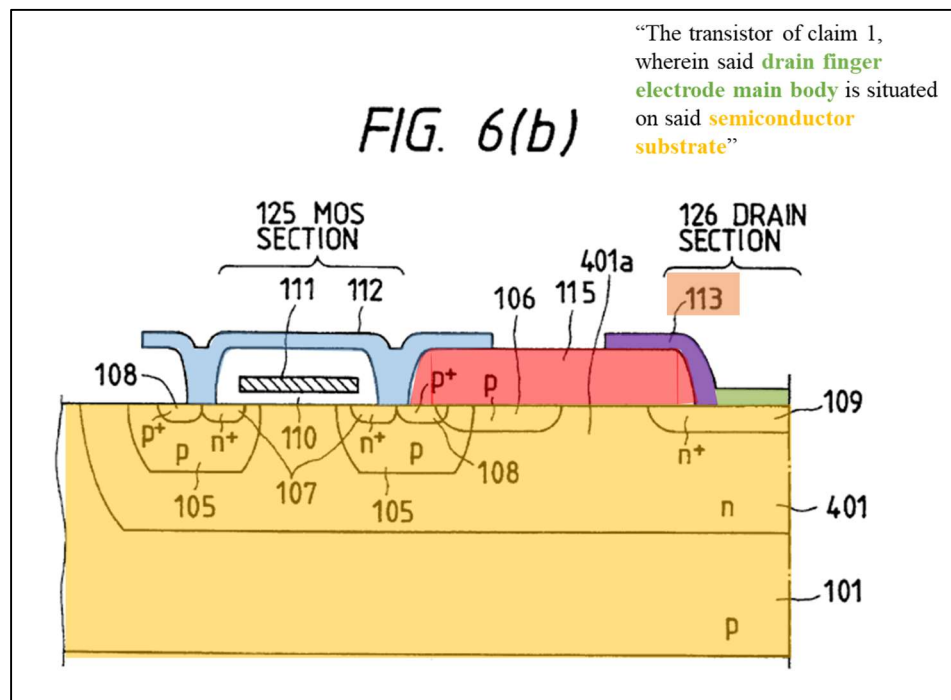
Fujishima discloses claim 3 because it discloses that the **insulating film 115** elevates the **drain finger end** over the **substrate**.



Fujishima, Fig. 6(b) (annotated); Zhao ¶91; Sections VII.A.2.c-VII.A.2.d.

5. **Claim 4 – The transistor of claim 1, wherein said drain finger electrode main body is situated on said semiconductor substrate.**

Fujishima discloses claim 4 because it discloses that the **drain finger main body** is situated on the **substrate**.



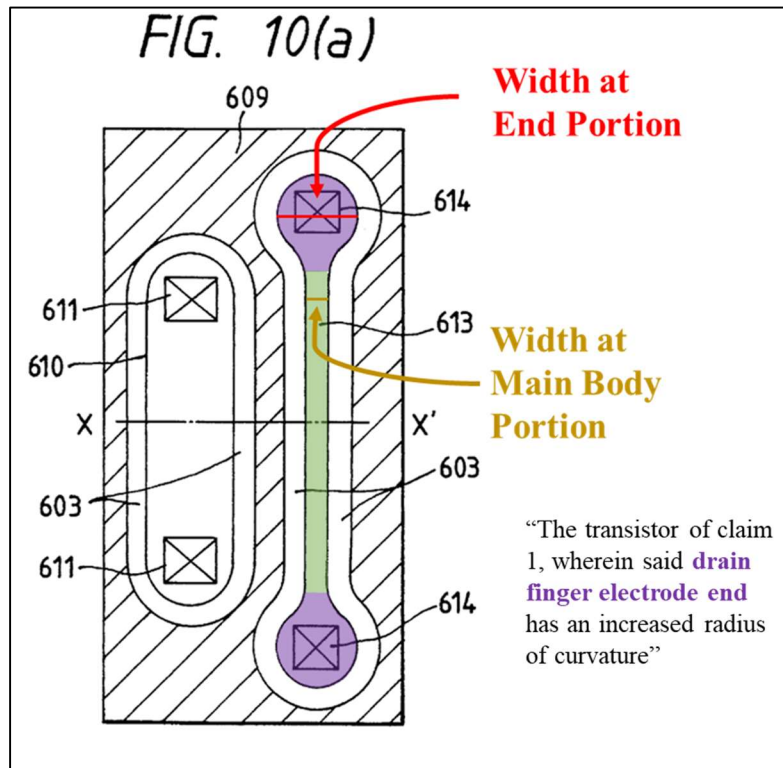
Fujishima, Fig. 6(b) (annotated); Zhao ¶92; Sections VII.A.2.c-VII.A.2.d.

6. Claim 5 – The transistor of claim 1, wherein said drain finger electrode end has an increased radius of curvature.

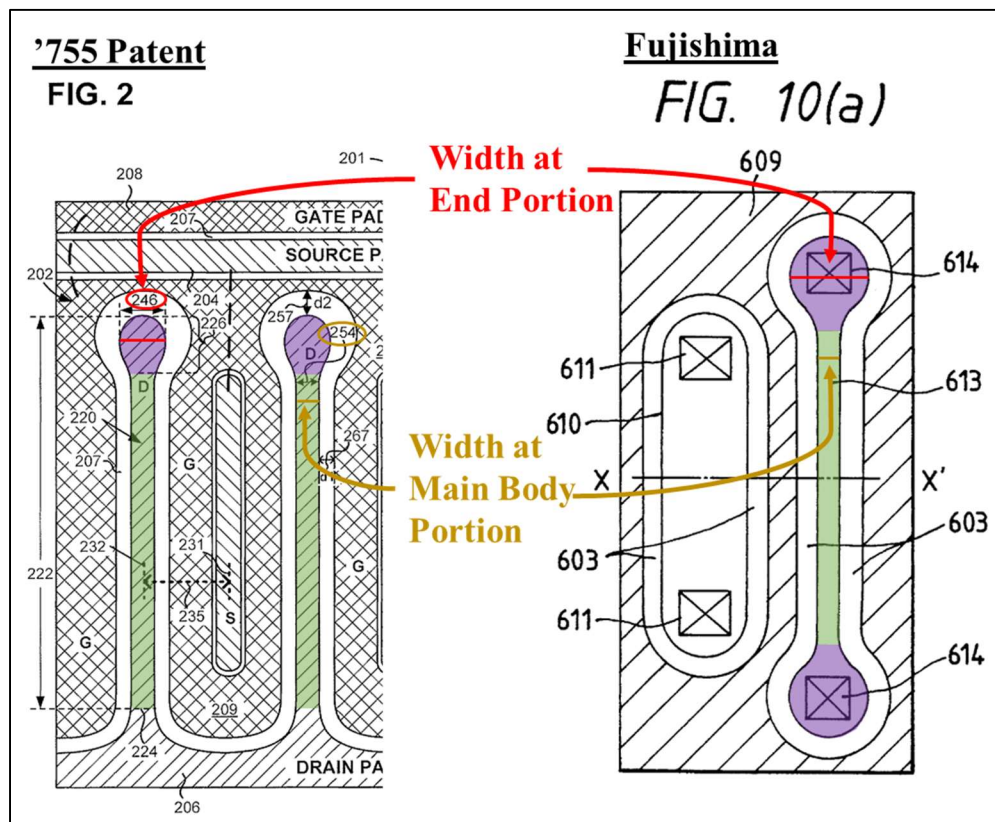
For Ground 1A, Fujishima discloses claim 5 because it discloses an ellipsoidal shape for the **drain finger end** that has an increased radius of curvature resulting in the width of the **end** being greater than the width of the **drain finger main body**. Zhao ¶93. **For Ground 1B**, a POSA would have (i) found claim 5 obvious in view of Fujishima’s disclosures or (ii) been motivated to combine Fujishima’s embodiments to achieve claim 5. *Id.*

First, for Ground 1A, in its Summary of the Invention, Fujishima discloses a **drain electrode** structure in which the “**width of a portion where the drain pad opening portion is not formed**” (i.e., the width at the **drain finger electrode main**

body) “is set to be smaller than a **width of the drain pad opening portion**” (i.e., the width at the **drain finger electrode end**), and is shown in Figure 10(a). Fujishima, 5:14-22, Figs. 10(a), 12; Zhao ¶94; see Fujishima, 5:22-36, 17:16-18:6, 6:45-53, 3:3-23, 20:56-21:12, Figs. 12-16.

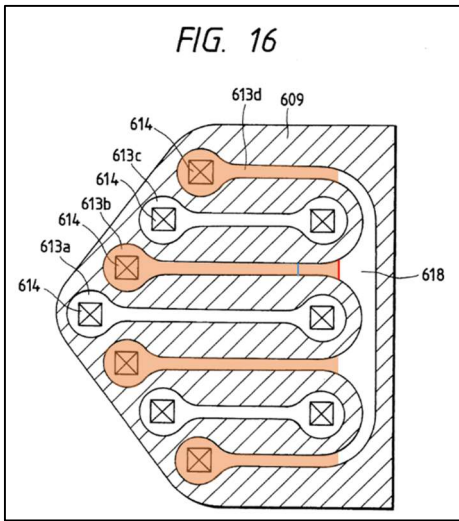


Fujishima, Fig. 10(a) (annotated). This is consistent with the ’755 patent, which explains that a “**drain finger electrode end**” has an “increased radius of curvature ... resulting in **increased width** of curved **drain finger electrode ends** relative to **width** of [the main body of] **drain finger electrode**.” ’755 Pat., 5:9-13, Fig. 2; see *id.*, 5:13-16. Zhao ¶95.



'755 Pat., Fig. 2 (excerpted and annotated); Fujishima, Fig. 10(a) (annotated).

Second, for Ground 1B, it would have been obvious to a POSA to implement the **drain finger electrode end** of Fujishima's **drain electrode 113** (see Section VII.A.2.b) with an ellipsoid shape, as disclosed in, for example, Figures 10(a) and 12. Zhao ¶96. Fujishima discloses various options for the shape of the drain finger electrodes including (1) an electrode finger with consistent width (Fujishima, Figs. 7(a), 8-9 and corresponding disclosures); (2) electrode finger ends with an ellipsoid shape (see Fujishima, Figs. 10(a), 12 and corresponding disclosures), and (3) electrode fingers with a connection portion 618 (see Fujishima, Fig. 16 and corresponding disclosures). Zhao ¶96.



Fujishima, Figs. 8, 10(a), 16 (annotated). Thus, it would have been obvious to a POSA to configure the **drain finger end** of Fujishima's **drain electrode 113** with an ellipsoid shape because doing so would simply implement an option that Fujishima itself discloses to provide an improved device with a higher withstand voltage (*id.*, 5:14-22, 17:41-54) and reduced electric field at the **end**. Zhao ¶96.

Third, for Ground 1B, a POSA would have been motivated to combine Fujishima's embodiments so that the **drain finger electrode end** has an increased radius of curvature. A POSA would have been motivated to modify the shape of the **end portion** of Fujishima's **drain finger** shown in Figure 8 with the shape of the **end portion** of **drain finger 613** that has an increased radius of curvature, as shown in Figures 10(a) and 12. A POSA would have recognized that Fujishima's presentation of multiple options for the **end portion** shape meant that different shapes have different benefits and applications. Zhao ¶97. Because these options are

presented in the same reference, a POSA would have been motivated (and found it would have been obvious) to modify the Figure 8 embodiment with the Figures 10(a) and 12 embodiments. *Id.* This similarly supports that a POSA would have had a reasonable expectation of success in making this modification, as Fujishima initially explains implementing a MISFET with the shape shown in Figure 8 and then describes implementing the same type of MISFET with the shape shown in Figures 10(a) and 12, including various benefits of this modification. Fujishima, 3:38-43, 15:40-59, 17:16-18:6, 18:20-33; Zhao ¶97. Moreover, a POSA would have had a reasonable expectation of success in making this modification because it is a simple design change that (i) can be implemented during the planning process, (ii) only modifies the electrode geometry, which is a simple change, and (iii) still utilizes the same fabrication process. Zhao ¶97.

Thus, it would have been obvious to a POSA to configure the **drain finger end** of Fujishima's **drain electrode 113** with an ellipsoid shape because doing so would simply combine prior art elements according to known methods (i.e., combining Fujishima's MISFET and ellipsoid shape electrode configuration) or substituting one known element for another (i.e., substituting the planar configuration for the ellipsoid shape electrode configuration) to yield predictable results (i.e., Fujishima's MISFET with an ellipsoid-shaped drain finger end). Zhao ¶98. Additionally, a POSA would have also found it obvious to do so because it

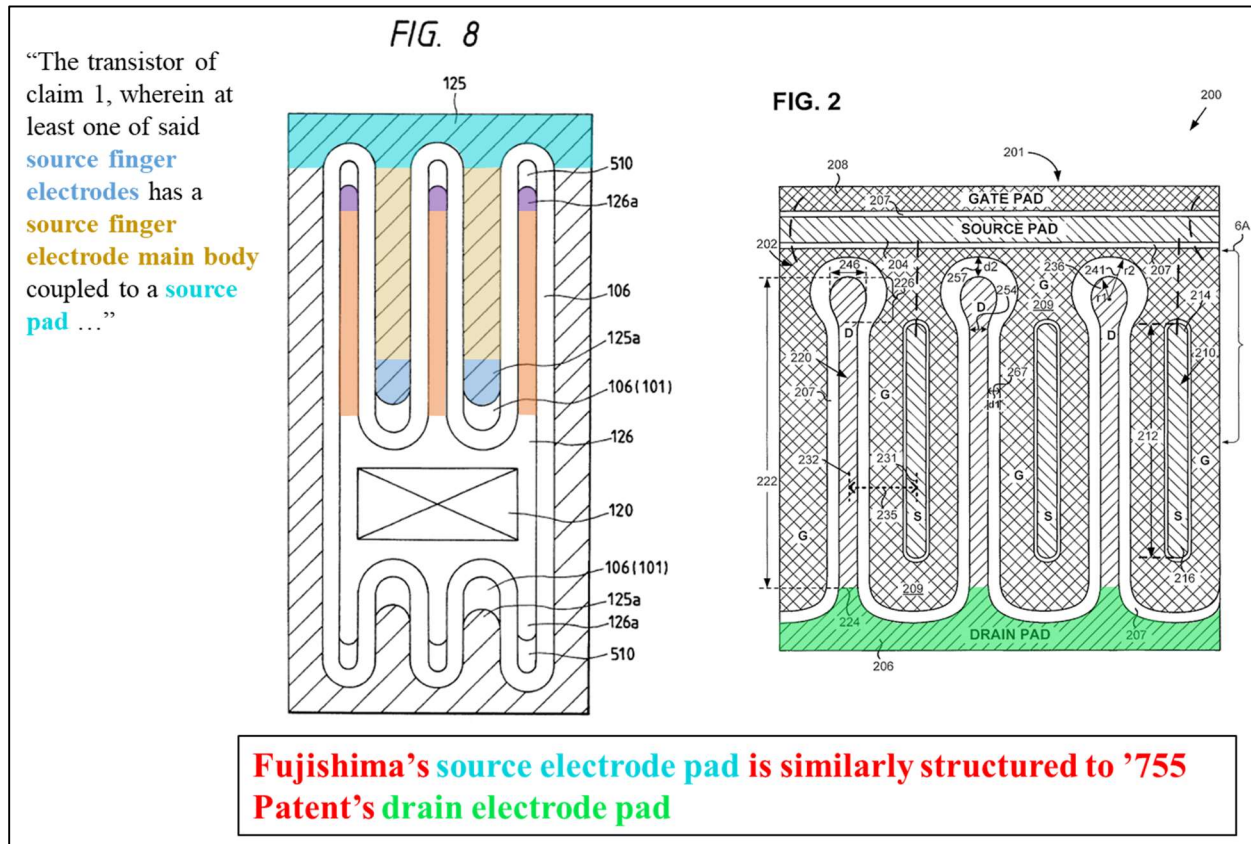
applies a known technique to a known device (i.e., using an ellipsoid-shaped drain finger end to Fujishima's MISFET) and provides an improved device with a higher withstand voltage (*see* Fujishima, 5:14-22, 17:41-54) and reduced electric field at the **drain finger electrode end**—benefits providing a clear teaching, suggestion, or motivation to make the combination. Zhao ¶98.

7. **Claim 6 – The transistor of claim 1, wherein at least one of said source finger electrodes has a source finger electrode main body coupled to a source pad, said drain finger electrode end extending beyond said source finger electrode main body.**

For Ground 1B, Fujishima renders obvious claim 6 because it discloses (i) a **source finger electrode** with a main body portion (*see* Section VII.A.2.b), which a POSA would have understood to be coupled to a source pad, and (ii) that the **end portion** of Fujishima's **drain finger electrode** (*see id.*) extends past the main body of the **source finger electrode**, as this configuration was well-known at the time of the invention. Zhao ¶99.

First, Fujishima's Figure 8 discloses a **source finger electrode** with a **main body portion** connected to a **source pad**. Zhao ¶100. A POSA would have understood that Fujishima's Figure 8 discloses a **source pad** (as depicted below) because it is consistent with how the '755 patent describes the source pad (*id.*; '755 Pat., 4:26-33, 4:64-5:8, Fig. 2) in that (i) the **source pad** in Figure 8 is electrically coupled to the **main body portion** given that the **source pad** and **main body** are

connected, (2) the **source pad** is adjacent to the Fujishima's **drain finger electrode ends**, and (3) the electrode pad structure of the **source pad** is similar to the **drain electrode pad** structure disclosed in the '755 patent. Zhao ¶100.

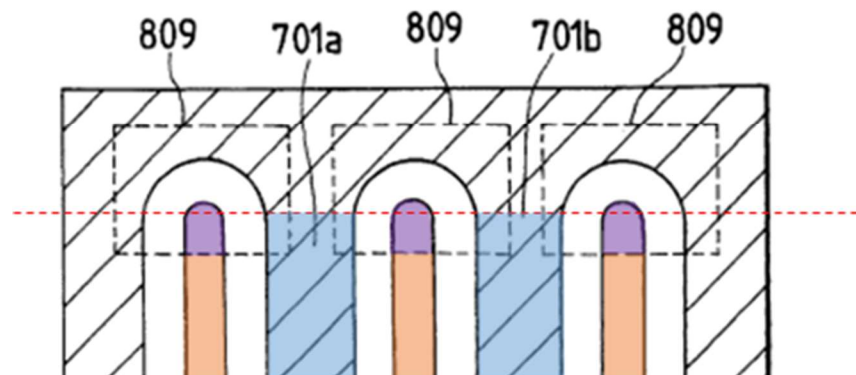


Fujishima, Fig. 8 (annotated); '755 Pat., Fig. 2 (annotated). Moreover, a POSA would have understood that the **main body portion** connects to a **source pad** to enable the **source finger electrodes** circuit access to components of the “integrated circuit device” external to Fujishima's MISFET. Zhao ¶100; Fujishima, 10:37-42, 11:65-12:3. A POSA would have understood that Fujishima's source pad provides numerous benefits, including providing uniform current distribution across source

fingers, providing a low-resistance path to lower parasitic resistance, and offering a centralized, low-inductance point for source fingers to connect that helps manage parasitic inductance. Zhao ¶100.

Second, a POSA would have found it obvious to extend the **end portion** of Fujishima's **drain finger electrode** beyond the **main body portion** of the **source finger electrode** because such a configuration was well known and conventional at the time of the invention. Zhao ¶¶101-103; Ex-1041 ¶¶20, 35, 16-17, 5, 8, 19, Fig. 3; Ludikhuize, Abstract, 4:26-33, Fig. 1; Ex-1021, 144. In fact, Fujishima's own description of the prior art discloses such a configuration:

FIG. 18 PROIR ART



Fujishima, Fig. 18 (excerpted and annotated); Zhao ¶104.

This combination would have been routine because implementing specific dimensions for electrode fingers (which was well known at the time of the alleged invention) is a simple design change during the planning phase that involves a

scaling or length adjustment. Zhao ¶105; Ludikhuize, 4:21-26, 2:36-41. Thus, a POSA would have found it straightforward with a reasonable expectation of success to modify Fujishima's electrode structure such that the drain finger electrode tips extend beyond the source finger electrode main body, including because it is a simple design change that (i) can be implemented during the planning process, (ii) only modifies the electrode geometry, which is an uncomplicated change, and (iii) still utilizes the same fabrication process. Zhao ¶105.

A POSA would have been motivated to make this modification because it would have (i) furthered Fujishima's goals of lowering the electric field at the **end portion** of the **drain finger electrode**, which was a known benefit in the art (Ludikhuize, Abstract, 4:26-33, Figs. 11, 4; Ex-1041 ¶¶20, 35, 16-17, 5, 8, 19, Fig. 3), (ii) increased transistor breakdown voltage, (iii) lowered current convergence and Kirk effect and the drain finger electrode tips, (iv) increased transistor safe operating area, and (iv) decreased manufacturing costs and materials needed. *Id.*; Zhao ¶106.

The modification simply combines prior art elements (Fujishima's MISFET and well-known electrode configurations to extend the drain finger end past the source finger main body) according to known methods to yield predictable results (using longer drain finger electrodes relative to source finger electrodes, as known in the art). Zhao ¶107. It is also a simple substitution of one known element (Fujishima's drain finger electrode configuration) for another (well-known drain

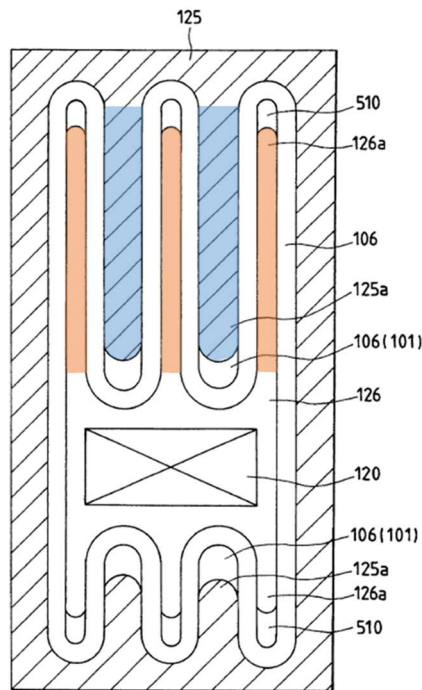
finger electrode configurations) to obtain predictable results (a transistor configuration that reduces the electric field at the end of the drain finger electrode and provides additional benefits noted above). *Id.* It also uses a known technique (the well-known configuration to extend the drain finger electrode end) to improve similar devices (transistors disclosed in Fujishima and well known in the art) in the same way (to reduce the negative electric field effect). *Id.*

8. Claim 7 – The transistor of claim 1, wherein said drain finger electrodes are longer than said source finger electrodes.

For Ground 1B, Fujishima renders obvious claim 7 because a POSA would have found it obvious to configure Fujishima's **drain finger electrodes** so they are longer than the **source finger electrodes**. Zhao ¶108.

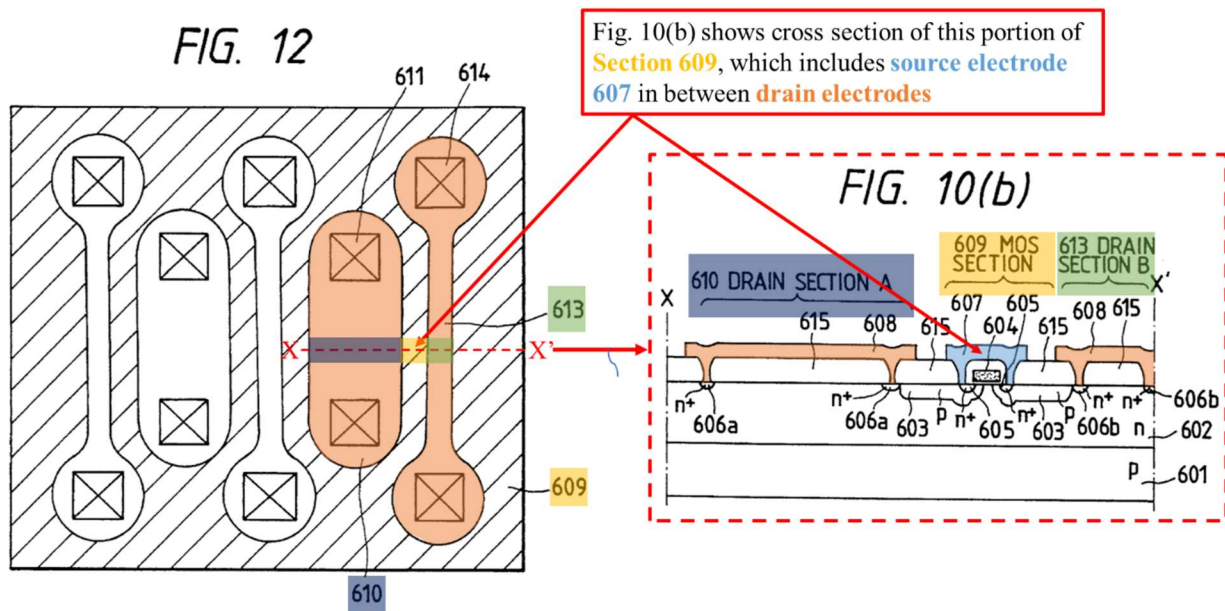
As explained for claim 6, Fujishima renders obvious extending the **end portions** of Fujishima's **drain finger electrodes** past the **main body portions** of the **source finger electrodes**. *Id.* ¶109; Section VII.A.7. Moreover, Fujishima discloses that the **drain finger electrodes** also extend past the **source finger electrodes** on the side opposite of the **end portions** of Fujishima's **drain finger electrodes** (i.e., the bottom side of Figure 8):

FIG. 8



Fujishima, Fig. 8 (annotated). Thus, Fujishima renders obvious **drain finger electrodes** that are longer than the **source finger electrodes**. Zhao ¶109.

Additionally, it would have been obvious to extend both tips of the **drain finger electrodes** to make these electrodes longer than the **source finger electrodes** on both sides. Zhao ¶110. As explained for claim 5, Section VII.A.6, Fujishima discloses or renders obvious implementing **drain finger electrodes** with two terminating ends, both of which have an ellipsoid shape:



Fujishima, Figs. 10(b), 12 (annotated). Figure 10(b) depicts a cross section of Figure 12 showing that the **source electrode 607** is between drain electrodes 608. *Id.*, Figs. 10(a), 10(b), 12, 16:67-17:15.

In such a configuration, a POSA would have understood that it would have been obvious and beneficial to extend the tips on both sides of the **drain finger electrodes** in drain section B past both tips of the **source finger electrodes** for the reasons explained for claim 6 that support extending the drain finger electrode end—and that there would be a reasonable expectation of success in making such a modification, which was well known. *See* Section VII.A.7; Ludikhuizen, Abstract, 4:26-33, Figs. 11, 4; Ex-1041 ¶¶20, 35, 16-17, 5, 8, 19, Fig. 3. Specifically, a POSA would have had a reasonable expectation of success in making this modification because it is a simple design change that (i) can be implemented during the planning

process, (ii) only modifies the electrode geometry, which is an uncomplicated change, and (iii) still utilizes the same fabrication process. Zhao ¶¶110-111.

Such a modification simply combines prior art elements (Fujishima's drain finger electrode with two terminating ends and well-known electrode configurations to extend the drain finger end portion past the source finger ends on both sides) according to known methods to yield predictable results (using longer drain finger electrodes relative to source finger electrodes, as known in the art). Zhao ¶112. It is also a simple substitution of one known element (Fujishima's Figure 8 drain finger electrode configuration) for another (well-known drain finger electrode configurations) to obtain predictable results (a transistor configuration that reduces the electric field at the end portions of the drain finger electrode and provides additional benefits noted above). *Id.*; Section VII.A.7. It also uses a known technique (the well-known configuration to extend the drain finger electrode ends) to improve similar devices (transistors disclosed in Fujishima and well known in the art) in the same way (to reduce the negative electric field effect). Zhao ¶112.

9. Claim 8 – The transistor of claim 1, wherein said transistor is a high-electron-mobility transistor (HEMT).

Fujishima discloses or renders obvious claim 8. **For Ground 1A**, Fujishima discloses MISFETs, and a POSA, at the time of the alleged invention, would have understood that MISFETs describe a variety of types of well-known transistors,

including GaN MIS-HEMTs. Zhao ¶113. **For Ground 1B**, a POSA would have motivated to apply Fujishima’s teachings to a GaN HEMT device and render obvious claim 8. *Id.*

For Ground 1A, the ’755 patent explains that “transistor 200” is a “field-effect transistor (FET)” and provides numerous options of FETs, including a “high-electron-mobility transistor (HEMT).” ’755 Pat., 3:60-4:3, 2:2-7, 1:28-55. Similarly, Fujishima discloses a “MISFET,” and a POSA would have understood that a Fujishima’s teachings apply to a variety of types of well-known and conventional MISFETs in 2012, including, for example, MIS-HEMTs or, specifically, GaN MIS-HEMTs. Zhao ¶¶70, 114; *see* Ex-1015 ¶¶3-4, 24 (describing HEMT as a type of FET and a GaN HEMT with a “MIS structure” (i.e., a MIS-HEMT)); Ex-1016 ¶¶46-47; Ex-1017 ¶¶5-10, 42, 56, 87; Ex-1020; Imada (comparing GaN MIS-HEMTs and HEMTs); Ex-1018, 155; Kanamura (disclosing Al-GaN and GaN MIS-HEMTs); Okino (comparing Al-GaN MIS-HEMTs and HEMTs); Ex-1013 ¶¶35-37; Ex-1014 ¶¶6-7, 99; Beach, 1:65-2:20, 5:17-21; Ex-1025, 375-78, 393-94, 402-03; Ex-1019-1020;

For Ground 1B, a POSA would have found it obvious to apply Fujishima’s concepts specifically to HEMTs (e.g., GaN HEMTs or InGaAs HEMTs), which were well-known by the time of the alleged invention, including with a transistor structure

similar to Fujishima's structure. Zhao ¶¶115-118; Sriram ¶¶16, 39, Figs. 1, 5; Asano ¶¶55-56, Figs. 3A, 4B; Ex-1013 ¶¶2-14; *see* Sections VII.A.1, VIII.A.2.e.

A POSA would have further found this obvious given that the concepts from Fujishima relevant to the claimed invention can be generally applied toward lateral transistors with source and drain electrodes, which would include GaN or InGaAs HEMTs. Zhao ¶119. This combination would have been routine because a POSA would have understood Fujishima's disclosures relied upon for claim 1 (*see* Section VII.A.2) are directed toward the electrode structure of a FET and it would be common to apply such disclosures to GaN or InGaAs HEMTs, which a POSA would understand to have had similar electrode structures, especially for electric field management purposes. Zhao ¶120; Ex-1018, 70-71 ("parameters of the MISFET are very similar to those of the HEMT"); Ex-1044; Ex-1042 Ex-1043. Moreover, applying Fujishima's principles in this manner to GaN or InGaAs HEMTs would have furthered Fujishima's goals of providing an improved transistor for high frequency applications, as GaN or InGaAs HEMTs provide high electron mobility resulting in "higher saturated electron drift velocities," which are preferred for high frequency applications "because the higher velocity translates to shorter times from source to drain" (i.e., faster switching speeds). Sriram ¶6; Zhao ¶120. Thus, a POSA would have had a reasonable expectation of success and found it straightforward to

incorporate Fujishima's disclosures relied upon for claim 1 to conventional GaN or InGaAs HEMTs. Zhao ¶120.

A POSA would have been motivated to combine these prior art elements according to known methods (i.e., applying Fujishima's technique of raising drain electrodes to well-known GaN or InGaAs HEMTs) to yield predictable results (i.e., incorporating the benefits touted by Fujishima into GaN or InGaAs HEMTs—with HEMTs themselves providing additional benefits over other transistors, such as higher breakdown voltage, high electron mobility, lower on-resistance reducing conduction losses, high power density, high efficiency (e.g., higher power conversion efficiency), lower switching losses, use of smaller passive components, better thermal conductivity, reduced parasitic capacitance, superior low temperature performance, fast switching speeds, among others). Zhao ¶121; Ex-1025, 376-77; Beach, 1:25-60, 3:59-65. Using Fujishima in a HEMT would have been obvious because it would use a known technique (Fujishima's technique of raising drain electrodes to improve withstand voltage) to improve similar devices (the known HEMT devices) in the same way (using the same Fujishima raised drain electrode technique in a HEMT). Zhao ¶121. The combination is also a simple substitution of one known element (Fujishima's drain finger electrode configuration with an elevated end in a MISFET) for another (well-known GaN or InGaAs HEMTs with a drain finger electrode end that is flat) to obtain predictable results (a GaN or InGaAs

HEMT with a drain finger electrode configuration that simply elevates the drain finger electrode end portion). *Id.* And a POSA would have applied Fujishima to HEMTs with a reasonable expectation of success because applying FET configuration to HEMTs was common and routinely performed for the features at issue here, including relating to electric field management. *Id.*; Ex-1018, 70-71 (“parameters of the MISFET are very similar to those of the HEMT”); Ex-1044; Ex-1042; Ex-1043.

A POSA would have found it obvious that Fujishima’s concepts applying to a MISFET would also apply to HEMTs because various types of MISFETs were well known at the time of the alleged invention, including MIS-HEMTs such as GaN or Al-GaN MIS-HEMTs, as explained above. Zhao ¶122.

10. Claim 9 – The transistor of claim 1, wherein said transistor comprises a group III-V transistor.

Fujishima discloses or renders obvious claim 9 for the reasons noted for claim 8 because (i) Fujishima discloses MISFETs, which a POSA would have understood to include GaN MIS-HEMTs (**Ground 1A**) or, (ii) alternatively, it would have been obvious to apply Fujishima’s concepts to GaN or InGaAs HEMTs, which were well-known at the time (**Ground 1B**). *See* Section VII.A.9; Zhao ¶123.

As described in the '755 patent, GaN HEMTs (which includes GaN MIS-HEMTs) and InGaAs HEMTs are group III-V transistors. '755 Pat., 2:1-7, 1:47-51, 4:9-21; Zhao ¶124; Ex-1025, 6, 49-52, 540-41.

Thus, for **Ground 1A**, Fujishima's disclosure of GaN MIS-HEMTs, as explained in Section VII.A.9, also discloses a group III-V transistor. Zhao ¶125.

Additionally, for **Ground 1B**, Fujishima rendering obvious the application of Fujishima's concepts to GaN or InGaAs HEMTs also renders obvious applying Fujishima's concepts to a group III-V transistor. Zhao ¶126. A POSA would have been motivated to combine these prior art elements (i.e., Fujishima's concepts and GaN HEMTs) and would have had a reasonable expectation of success making the combination for the reasons explained in Section VII.A.9.

11. Independent Claim 10

a. [10pre]: A transistor comprising:

If the preamble is limiting, Fujishima discloses [10pre] for the reasons explained for [1pre]. *See* Section VII.A.2.a; Zhao ¶127.

b. [10a]: drain finger electrodes interdigitated with source finger electrodes;

Fujishima discloses [10a] for the reasons explained for [1a]. *See* Section VII.A.2.b; Zhao ¶128.

c. [10b]: a gate region configured to control current conduction in a semiconductor substrate between said

drain finger electrodes and said source finger electrodes;

Fujishima discloses or renders obvious [10b] for the reasons explained for [1b]. *See* Section VII.A.2.b (explaining that Fujishima discloses or renders obvious “current conduction in a semiconductor substrate between said drain finger electrodes and said source finger electrodes”); Zhao ¶129.

Fujishima discloses a gate region because it discloses a “gate electrode.” Fujishima, Claim 1, 8:46-49, 3:61-63, 4:29-34, Fig. 6(b); Zhao ¶130. Fujishima further explains that electrons flow from the source to the drain when voltage is applied to the gate electrode. Fujishima, 2:29-37; Zhao ¶130. A POSA would have understood that Fujishima’s gate electrode controls the conduction between the drain and source electrodes, including based on the magnitude of the voltage applied—i.e., a higher voltage results in more electron flow and higher conduction—which is consistent with Fujishima’s own disclosures. Zhao ¶130; *see* Fujishima, 2:29-37; Beach, 1:61-67, 5:29-35.

d. [10c]: at least one of said drain finger electrodes having a drain finger electrode end and a drain finger electrode main body,

Fujishima discloses [10c] for the reasons explained for [1c]. *See* Section VII.A.2.d; Zhao ¶131.

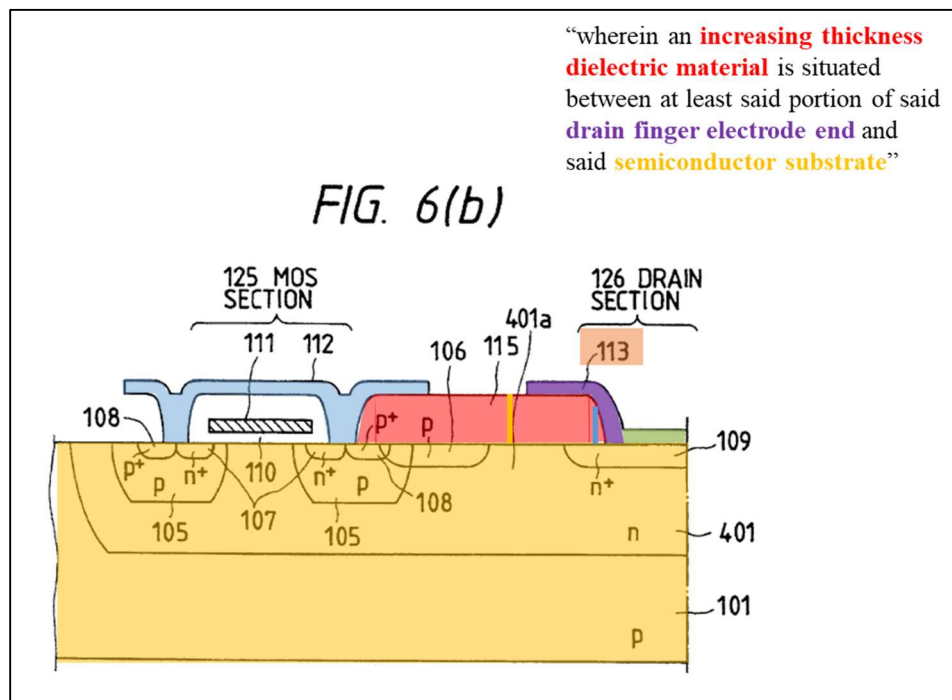
- e. **[10d] wherein at least a portion of said drain finger end is non-coplanar with said drain finger electrode main body;**

Fujishima discloses [10d] for the reasons explained for [1d]. *See* Section VII.A.2.e; Zhao ¶132.

- f. **[10e]: wherein an increasing thickness dielectric material is situated between at least said portion of said drain finger electrode end and said semiconductor substrate.**

Fujishima discloses [10e] for at least the reasons explained for claim 2. *See* Section VII.A.3 (explaining that Fujishima discloses “wherein ... a dielectric material is situated between at least said portion of said drain finger electrode end and said semiconductor substrate”); Zhao ¶133.

Fujishima’s Figure 6(b) discloses that the **dielectric material** has an “increasing thickness” because the thickness of Fujishima’s **insulating film 115** increases from its outer edges (blue line) to the center (yellow line):



Fujishima, Fig. 6(b) (annotated); Zhao ¶134.

- 12. Claim 11 – The transistor of claim 10, wherein said increasing thickness dielectric material elevates said drain finger electrode end over said semiconductor substrate.**

Fujishima discloses claim 11 for the reasons explained for [10e] and claim 3.

See Sections VII.A.11.f, VII.A.4; Zhao ¶135.

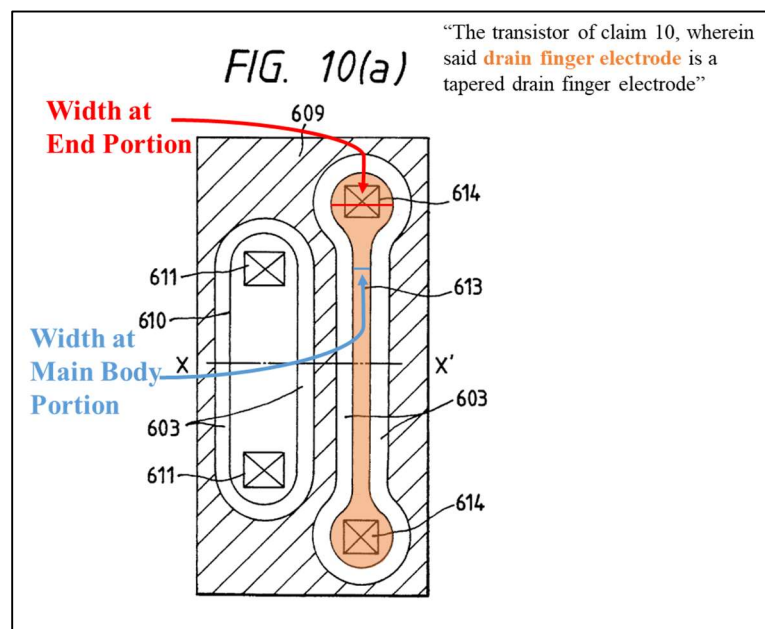
- 13. Claim 12 – The transistor of claim 10, wherein said drain finger electrode end is substantially an ellipsoid.**

Fujishima discloses claim 12 for the reasons explained for claim 5. See Section VII.A.6; Zhao ¶136.

14. Claim 13 – The transistor of claim 10, wherein said drain finger electrode is a tapered drain finger electrode.

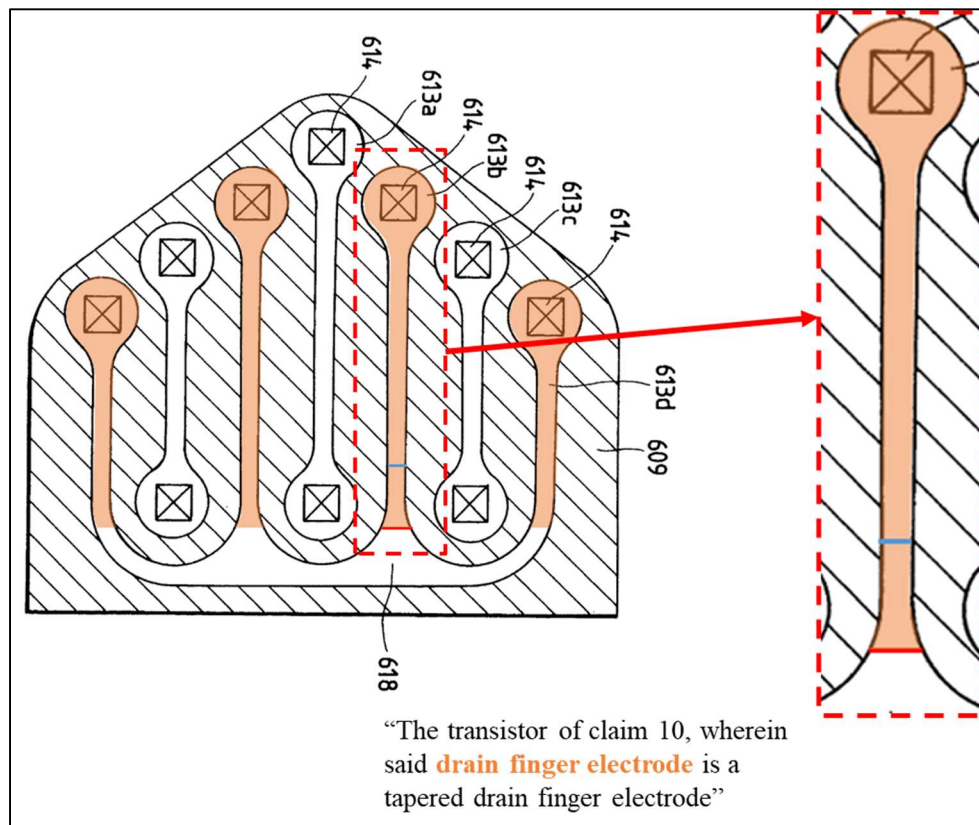
For Ground 1A, Fujishima discloses claim 13 because its **drain finger electrode** is tapered. Zhao ¶137. For Ground 1B, a POSA would have (i) found claim 13 obvious in view of Fujishima’s disclosures or (ii) been motivated to combine Fujishima’s embodiments to achieve claim 13. *Id.*

First, for Ground 1A, Fujishima discloses a **drain finger electrode** structure that incorporates tapering in two ways. For the first way, Fujishima discloses a **drain electrode** structure in which the “**width of a portion where the drain pad opening portion is not formed**” “is set to be smaller than a **width of the drain pad opening portion**”—thus tapering from a top portion (red line) to a smaller width in the middle of the electrode (blue line). Fujishima, 5:19-22; Zhao ¶138.



Fujishima, Fig. 10(a) (annotated).

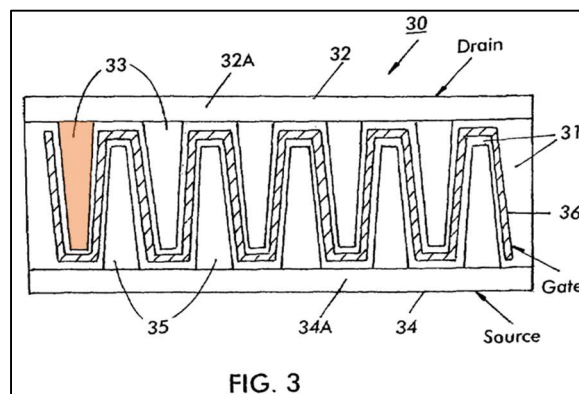
For the second way, Fujishima discloses a **drain electrode** structure that incorporates tapering in a different manner. Specifically, this structure has a smaller width near the center of the **electrode** relative to a width of the **electrode** near the connection 618—thus tapering from an end portion near the connection 618 (red line) to a smaller width in the middle of the electrode (blue line). Zhao ¶139.



Fujishima, Fig. 16 (annotated).

Second, for Ground 1B, it would have been obvious to a POSA to implement Fujishima’s **drain electrode 113** (see Section VII.A.2.b) with a tapered configuration because this type of modification was well known, as conceded by applicant’s admissions in the ’755 patent conceding that “tapered source and drain

finger designs” were described in 2008 in Beach—four years before the time of the invention—and provided benefits including “higher breakdown voltages and lower ON-resistance.” ’755 Pat., 8:43-55; *see* Director Vidal Updated Guidance on the Treatment of Statements of the Applicant in the Challenged Patent in Inter Partes Reviews Under § 311(b) (June 9, 2022) (explaining that admissions can be used to “supply missing claim limitations that were generally known in the art prior to the invention” or “demonstrate the knowledge of a [POSA] at the time of the invention.”). Beach discloses drain finger electrodes in which “each finger taper[s] from a base to a tip thereof, [with] the base being wider than the tip”:



Beach, Fig. 3, Claim 1, Abstract, 5:57-6:11. Thus, Fujishima, in view of Applicant’s admissions regarding Beach’s disclosures, renders obvious tapered drain finger electrodes and claim 13, as a POSA would have found it obvious to implement Fujishima’s **drain electrode 113** with a tapered configuration. Zhao ¶¶140-142.

This modification would have been routine and had a reasonable expectation of success because implementing specific geometry for electrode fingers (i.e.,

tapered drain finger electrode, as the applicant-admitted-prior-art (AAPA) discloses) is a simple design change, making the base width larger than the tip width, and can be implemented during the planning phases. Zhao ¶142. A POSA would have had a reasonable expectation of success in making this modification because it is a simple design change that (i) can be implemented during the planning process, (ii) only modifies the electrode geometry, which is an uncomplicated change, and (iii) still utilizes the same fabrication process. *Id.*

A POSA would have been motivated to make the combination to (i) increase device power rating, (ii) decrease device dimensions, (iii) reduce device resistance and balance current flow, and (iv) decrease power loss. Zhao ¶143; Beach, Abstract, 3:1-8, 4:6-33, 4:53-64, 6:1-11, 6:24-48, 6:57-61.

The combination simply combines prior art elements (Fujishima's and the AAPA's transistor and electrode configurations) according to known methods to yield predictable results (using tapered drain finger electrodes). Zhao ¶144. It is also a simple substitution of one known element (Fujishima's drain finger electrode configuration shown in Figure 8) for another (the AAPA's tapered drain finger electrode configuration in Figure 3) to obtain predictable results (a configuration of the drain finger electrode of a transistor that reduces the negative electric field effect). *Id.* It also uses a known technique (the AAPA's tapered drain finger electrode

configuration) to improve similar devices (transistors disclosed in Fujishima and the AAPA) in the same way (to reduce the negative electric field effect). *Id.*

Third, for Ground 1B, a POSA would have been motivated to combine embodiments in Fujishima in a manner that discloses this limitation. Specifically, a POSA would have been motivated to modify the shape of Fujishima's **drain finger** shown in Figure 8 with the shape of **drain finger** shown in Figure 10(a) or Figure 16—both of which include tapered electrode configurations, as explained above. Zhao ¶145. A POSA would have recognized that Fujishima's presentation of multiple options for the shape of the end portion of the drain finger meant that different shapes have different benefits and applications. *Id.* Moreover, because these options are presented in Fujishima, a POSA would have been motivated (and found it would have been obvious) to modify the Figure 8 embodiment with the Figure 10(a) embodiment or Figure 16 embodiment, as well as that such a modification would have had a reasonable expectation of success, including because it is a simple design change that (i) can be implemented during the planning process, (ii) only modifies the electrode geometry, which is an uncomplicated change, and (iii) still utilizes the same fabrication process. *Id.*

Thus, it would have been obvious to a POSA to incorporate tapering to Fujishima's **drain electrode 113** because doing so would simply combine prior art elements according to known methods (i.e., combining Fujishima's MISFET and

Fujishima's tapered shape electrode finger configuration) or substituting one known element for another (i.e., substituting Fujishima's planar configuration for its tapered shape electrode finger configuration) to yield predictable results (i.e., Fujishima's MISFET with Fujishima's tapered-shaped drain finger electrode). Zhao ¶146. Additionally, a POSA would have also found it obvious to do so because it applies a known technique to a known device (i.e., using a tapered-shaped drain finger electrode in Fujishima's MISFET) and provides an improved device with a higher withstand voltage and reduced electric field—benefits providing a clear teaching, suggestion, or motivation to make the combination. *Id.*

15. Claim 14 – The transistor of claim 10, wherein said transistor is a high-electron-mobility transistor (HEMT).

Fujishima discloses claim 14 for the reasons explained for claim 8. *See* Section VII.A.9; Zhao ¶147.

B. Ground 1C: Fujishima and Ludikhuize Render Obvious Claims 6-7.

Claims 6 and 7 are directed to a drain finger electrode longer than the source finger electrode (claim 7) and that the end portion of the drain finger electrode extends beyond the source finger electrode main body (Claim 6). Zhao ¶148. Ludikhuize discloses both limitations and a POSA would have found it obvious to combine Fujishima and Ludikhuize. *Id.*

1. Ludikhuize

Ludikhuize relates generally to transistors and addresses breakdown issues from current convergence at drain finger ends by implementing **source fingers** shorter than **drain fingers**. Ludikhuize, Abstract, 3:1-17, 3:46-54, Claim 1; '755 Pat., 3:64-65; Fujishima, 7:5-7 (same).

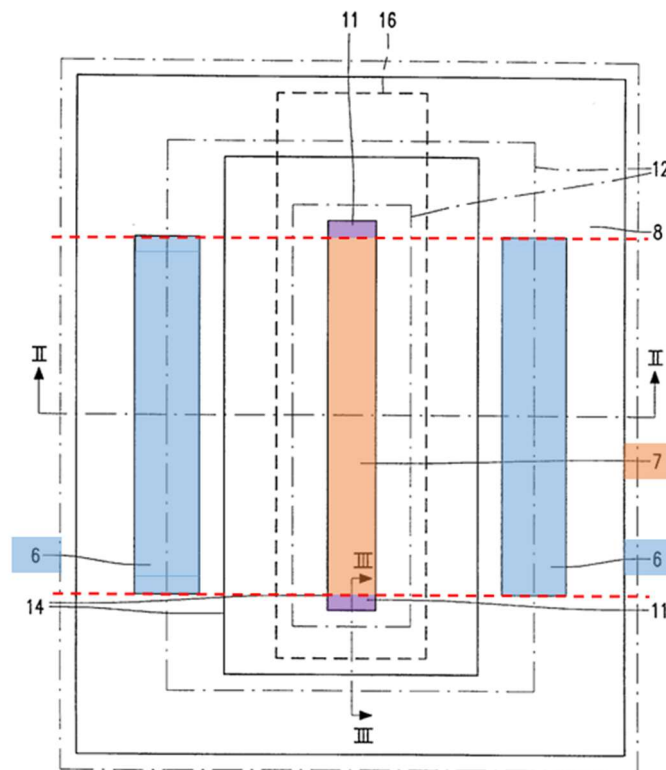
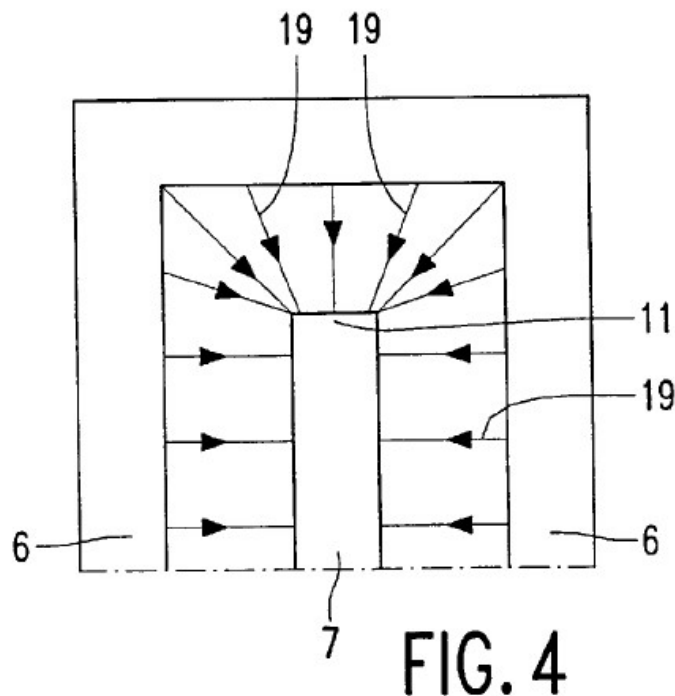


FIG. 1

Ludikhuize, Fig. 1 (annotated). This increases the safe operating area of the transistor and reduces the Kirk effect and current convergence at the **drain finger electrode tips**. Ludikhuize, Abstract, 4:26-33, Figs. 11, 4; Zhao ¶149.



Ludikhuize, Fig. 4.

2. General Motivations to Combine

A POSA would have found it obvious to combine Fujishima and Ludikhuize, which disclose complementary systems and methods for configuring transistors and improve overall transistor performance by alleviating negative electric field effects within the transistor. Zhao ¶150.

Fujishima relates to various configurations of MISFETs. *See* Sections VII.A.1, VII.A.9. Fujishima's transistor has a lateral structure with the drain, source, and gate on the same surface of the substrate. Fujishima, 13:37-51, Fig. 6(b); Zhao ¶¶70, 151. These various configurations improve the overall transistor device,

including by minimizing the electric field at the ends of the drain electrode. *See* Section VII.A.1; Zhao ¶¶71, 151.

Similarly, Ludikhuize discloses “lateral” transistors with “interdigitated source/drain configuration.” Ludikhuize, Abstract. Additionally, it discloses configuring transistors with shorter source fingers to prevent electrical breakdown due to electric fields. Section VII.B.1; Zhao ¶152.

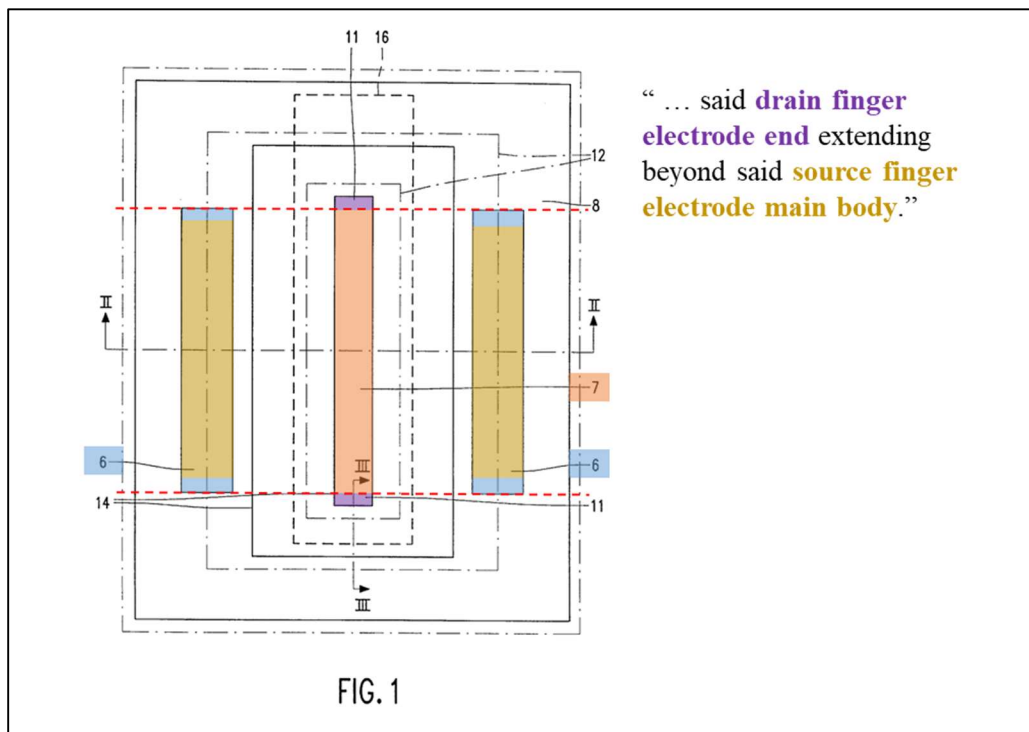
Fujishima and Ludikhuize are also similar and analogous to the ’755 patent, which generally discloses high voltage FETs. ’755 Pat., 3:56-4:8; Zhao ¶153. The ’755 patent is specifically directed to making design changes to the electrode structure to help alleviate negative electric field impact and improve the robustness of a transistor, including elevating the tips of the finger of a drain electrode, increasing the curvature of the drain electrode tips, and tapering the electrode fingers. ’755 Pat., 3:53-55, 4:64-5:8, 8:43-59, 10:5-22, Fig. 6C; Zhao ¶153.

Thus, Fujishima and Ludikhuize are analogous art to the ’755 patent and combinable with each other because they belong to the same field of endeavor, disclose comparable systems that operate similarly, and are reasonably pertinent to similar problems. Zhao ¶154.

- 3. Claim 6 – The transistor of claim 1, wherein at least one of said source finger electrodes has a source finger electrode main body coupled to a source pad, said drain finger**

electrode end extending beyond said source finger electrode main body.

Fujishima and Ludikhuize render obvious claim 6. Zhao ¶155. Specifically, Ludikhuize discloses “**source fingers 6**” that have a **main body portion** coupled to a source pad and a “**drain finger 7**” that has “**tips 11**” that extend past the **source finger electrode**, including the **main body portion**. *Id.*

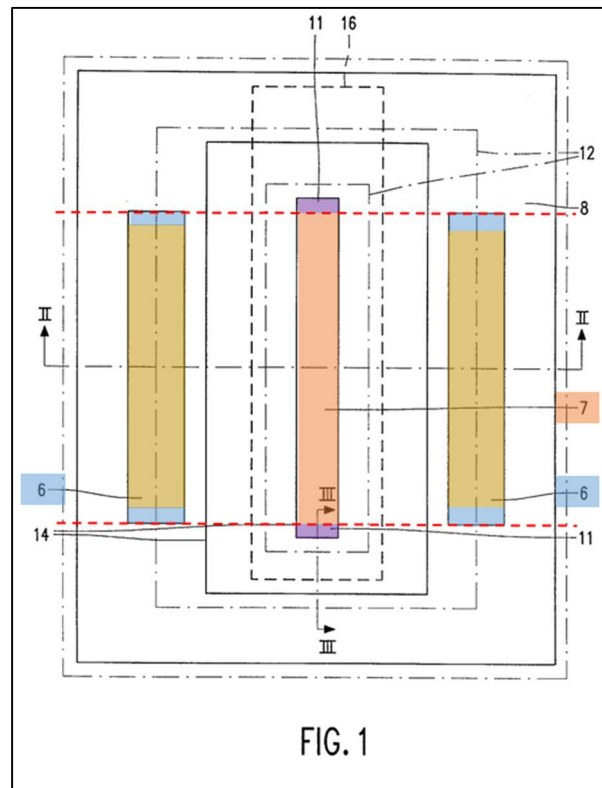


Ludikhuize, Fig. 1 (annotated), Abstract, Fig. 3.

Ludikhuize discloses “source and drain electrodes 15 and 16” that are connected to **source fingers 6** with **main body portions** and **drain finger 7**, and a POSA would have understood that these fingers constitute the claimed source finger electrodes and drain finger electrodes. Ludikhuize, Fig. 1, 3:28-36, 3:60-61, 4:58-

67; Zhao ¶156. Fujishima discloses the claimed source pad (*see* Section VII.A.7), however, a POSA would have also understood that the **main body portions** of **source fingers 6** in Ludikhuize couple to a source pad because (i) Ludikhuize discloses a high-voltage transistor, (ii) such devices include transistors that connect to a circuit external to the transistor, and (iii) the **main body portions** of **source fingers 6** couple to a source pad to enable the external circuit access to the source electrode. Zhao ¶156. In fact, Ludikhuize discloses a drain pad and a POSA would have understood that the device would similarly include a source pad. *Id.*; Ludikhuize, 3:32-37. A POSA would have understood that Ludikhuize’s source pad provides numerous benefits, including providing uniform current distribution across **source fingers**, providing a low-resistance path to lower parasitic resistance, and offering a centralized, low-inductance point for **source fingers** to connect that helps manage parasitic inductance. Zhao ¶156.

Ludikhuize discloses extending the “**tips 11**” of “**drain finger 7**” beyond the **main body portions** of the **source fingers 6**. Ludikhuize, Fig. 1; Zhao ¶157. Ludikhuize explains that the “**source fingers** are [made] shorter than the **drain finger[]** at the ends of the[] **drain finger[]**” to increase the safe operating area (Ludikhuize, Abstract, Fig. 1) and lower the electric field concentration at the drain finger tips. Ludikhuize, 2:42-50; *see id.*, 1:62-2:19, 4:4-33, 3:46-54, 2:36-41, Fig. 4, Claim 1.



Ludikhuize, Fig. 1 (annotated); Zhao ¶157.

In addition to general motivations to combine Fujishima and Ludikhuize (*see* Section VII.B.2), a POSA would have also had specific motivations to combine these references to extend the end portion of Fujishima's drain finger electrode beyond the main body portion of the source finger electrode. Zhao ¶158; *see* Section VII.A.7.

A POSA would have found this combined configuration obvious because both references disclose similar types of transistors with specific configurations of a drain finger electrode end portion that minimizes the concentration of electric field at this end portion and provides improvements to the transistor device. Zhao ¶159; Fujishima, 2:54-64, 2:65-3:33, 3:44-52, 6:13-33, 12:23-40, Fig. 6(b); Ludikhuize,

Abstract, Fig. 1, 2:42-50; *see id.*, 1:62-2:19, 4:4-33, 3:46-54, 2:36-41, Fig. 4, Claim 1; Ex-1041 ¶¶20, 35, 16-17, 5, 8, 19, Fig. 3. Thus, Fujishima and Ludikhuize both directly teach and suggest modifying electrode configurations to help minimize electric field concentrations, and this would have strongly motivated a POSA to consider and combine the teachings of these references directed toward the same goal. Zhao ¶159.

This combination would have been routine because implementing specific dimensions for electrode fingers (i.e., Ludikhuize’s disclosure of source fingers being shorter than drain fingers) is a simple design change that involves a scaling or length adjustment and can be implemented during the planning phases—which Ludikhuize describes as “simple.” *Id.* ¶160; Ludikhuize, 4:21-26, 2:36-41. Thus, a POSA would have found it straightforward with a reasonable expectation of success to modify Fujishima’s electrode structure such that the tips of the drain finger electrode extend beyond the main body of the source finger electrode, as Ludikhuize discloses. Zhao ¶¶160-161. Specifically, a POSA would have had a reasonable expectation of success in making this modification because it is a simple design change that (i) can be implemented during the planning process, (ii) only modifies the electrode geometry, which is a simple change, and (iii) still utilizes the same fabrication process. *Id.*

A POSA would have been motivated to make the combination to (i) increase transistor breakdown voltage, (ii) lower electric field concentration, current convergence, and Kirk effect and the drain finger electrode tips, (iii) increase transistor safe operating area, and (iv) decrease manufacturing costs and materials needed. Zhao ¶162; Ex-1041 ¶¶20, 35, 16-17, 5, 8, 19, Fig. 3; *see* Section VII.B.1.

The combination simply combines prior art elements (Fujishima's and Ludikhuize's electrode configurations) according to known methods to yield predictable results (using longer drain finger electrodes relative to source finger electrodes). Zhao ¶163; *see* Section VII.A.7. It is also a simple substitution of one known element (Fujishima's Figure 8 drain finger electrode configuration) for another (Ludikhuize's drain finger electrode configuration) to obtain predictable results (a transistor configuration that reduces the electric field at the end portions of the drain finger electrode, as both references seek to do). Zhao ¶163. It also uses a known technique (Ludikhuize's drain finger electrode configuration) to improve similar devices (transistors disclosed in Fujishima and Ludikhuize) in the same way (to reduce the electric field). *Id.*

4. Claim 7 – The transistor of claim 1, wherein said drain finger electrodes are longer than said source finger electrodes.

Fujishima and Ludikhuize render obvious claim 7 at least for the reasons they render obvious claim 6. Zhao ¶164. Ludikhuize discloses drain finger electrodes that

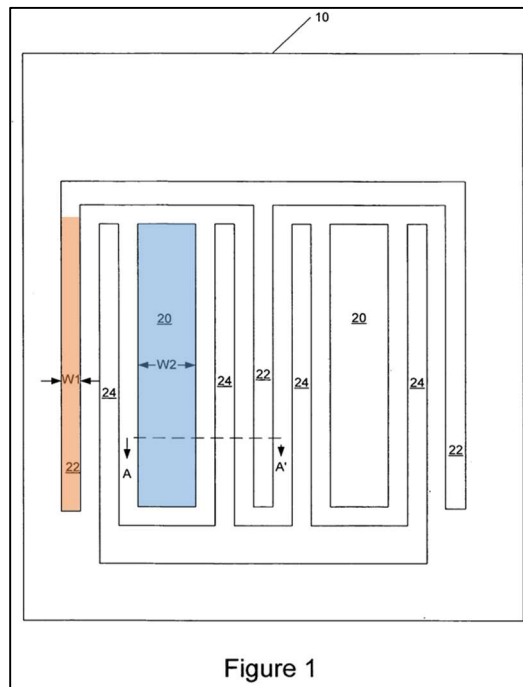
are longer than source finger electrodes. *See* Section VII.B.3; Ludikhuize, Fig. 1, 3:28-37, 4:58-67. A POSA would have been motivated to combine Fujishima and Ludikhuize and would have had a reasonable expectation of success making the combination for the reasons explained for claim 6, including because the combination asserted for claim 6 discloses drain finger electrodes longer than source finger electrodes. *See* Section VII.B.3; Zhao ¶164.

C. Ground 1D: Fujishima and Sriram Render Obvious Claims 8-9 and 14.

Claims 8-9 and 14 limit the transistor to a high-electron mobility transistor (HEMT) (claims 8 and 14) or a group III-V transistor (claim 9). Zhao ¶165. As the '755 patent explains, a transistor can be a “group III-V HEMT[,],” such as a GaN HEMT. '755 Pat., 2:2-5, 4:9-15; Zhao ¶165. Sriram discloses a GaN HEMT similarly structured to Fujishima's MISFET, including interdigitated source and drain electrodes and drain electrodes with a main body and end portion, and a POSA would have found it obvious to combine Fujishima and Sriram. Zhao ¶165.

1. Sriram

Sriram discloses high-frequency semiconductor devices (FETs) with “interdigitated structures...having a source, a drain and a gate.” Sriram ¶¶4-5, 11, Figs. 1-2.



Id., Fig. 1.

Sriram discloses a variety of types of lateral power transistors known in 2006—six years before the alleged date of the invention—including “GaN HEMTs,” “GaAs HEMTs,” *id.* ¶¶43, 2, 11, 16, 42, Abstract, Figs. 2, 3E, 5-6; *see id.*, Claims 1, 8-10, 18-19, 22, 30-32, 40-41, which “were preferred” for high-frequency applications because they produce current with lesser electric field and provide faster response times. *Id.* ¶6; Zhao ¶¶166-168.

2. General Motivations to Combine

A POSA would have found it obvious to combine Fujishima and Sriram, which disclose complementary systems and methods for configuring transistors and

improving overall transistor performance by, for example, alleviating negative electric field effects. Zhao ¶169.

Similar to Fujishima (*see* Section VII.B.2), Sriram discloses interdigitated drain and source fingers in a lateral power transistor and configuration options for transistors that help prevent electrical breakdown due to negative electric field effects. Zhao ¶170. Specifically, like Fujishima, Sriram makes structural improvements, modifying the dimensions of drain and source finger electrodes to reduce device source capacitance, which reduces risk of electric field-induced breakdown during high-speed switching, and integrated designs that allow for use of plurality of transistors with a more packed design to save space. *See* Sriram ¶¶9, 37, 40-42, 11; Zhao ¶¶166, 170 (explaining benefits of reduced source capacitance).

Fujishima and Sriram are also similar to the '755 patent, as previously described, including in Section VII.B.2. Zhao ¶171.

Thus, Fujishima and Sriram are analogous art to the '755 patent and combinable with each other because they belong to the same field of endeavor, are comparable systems that operate in a similar manner, and are reasonably pertinent to similar problems. Zhao ¶172.

3. Claim 8 - The transistor of claim 1, wherein said transistor is a high-electron-mobility transistor (HEMT).

Fujishima and Sriram render obvious claim 8. Zhao ¶173. Sriram discloses a GaN HEMT. *Id.*; Sriram ¶¶16, 43, 63; *see id.* ¶¶5-6.

In addition to general motivations to combine Fujishima and Sriram (*see* Section VII.C.2), a POSA would have also had specific motivations to combine the references to apply Fujishima's disclosures to GaN HEMTs. Zhao ¶174; *see* Section VII.A.9.

A POSA would have found this combination obvious because both references are directed to improving the operation of high power transistors in high frequency applications. Zhao ¶175. Fujishima's invention is directed to improving power transistors used in power integrated circuits "for switching power sources," which a POSA would understand as needing high frequency transistors. Fujishima, 2:54-64; Zhao ¶175. Similarly, Sriram describes improvements to high power transistors used for high frequency applications. Sriram ¶¶4-5, 11, Abstract, Claim 1; *see id.* ¶¶6-10. Thus, based on the disclosures and goals of both references, a POSA would have been motivated to consider and combine the teachings of these references. Zhao ¶175.

This combination would have been routine because a POSA would have understood Fujishima's disclosures relevant to claim 1 (*see* Section VII.A.2) are

directed toward the electrode structure and it would have been common to apply these disclosures to Sriram's GaN HEMTs that have a similar structure, especially as they relate to electric field management. Zhao ¶176; Ex-1018, 70-71 ("parameters of the MISFET are very similar to those of the HEMT"); Ex-1044; Ex-1042; Ex-1043. For example, Sriram's GaN HEMTs are lateral power transistors with interdigitated drain and source fingers, and the drain electrodes have a main body portion and end portion. Zhao ¶176; Sections VII.C.1-VII.C.2. In fact, Fujishima's MISFETs include GaN MIS-HEMTs, which are a type of GaN HEMT. *See* Sections VII.A.1, VII.A.9. Moreover, applying Fujishima's principles in this manner to GaN HEMTs would have furthered Fujishima's goals of providing an improved transistor for high frequency applications, as GaN HEMTs provide high electron mobility resulting in "higher saturated electron drift velocities," which are preferred for high frequency applications "because the higher velocity translates to shorter times from source to drain" (i.e., faster switching speeds). Sriram ¶6; Zhao ¶176. Thus, a POSA would have had a reasonable expectation of success and found it straightforward to incorporate Fujishima's disclosures relied upon for claim 1 to Sriram's GaN HEMT—a device that was well known by 2006, six years before the alleged invention date. Zhao ¶176.

A POSA would also have been motivated to make the combination for additional benefits, as GaN HEMTs provide numerous benefits over conventional

transistors including (i) higher breakdown voltage, (ii) lower on-resistance reducing conduction losses, (iii) lower switching losses, (iv) higher power conversion efficiency, (v) use of smaller passive components, (vi) better thermal conductivity, (vii) reduced parasitic capacitance, and (viii) higher power density. Zhao ¶177; *see* Beach, 1:25-60, 3:59-65; Ex-1025, 376-77.

The combination simply combines prior art elements according to known methods (applying Fujishima's technique of raising drain electrodes to Sriram's GaN HEMT with interdigitated drain and source electrodes) to yield predictable results (making the drain finger electrode end elevated so that it is non-coplanar with the main body, as disclosed in Fujishima, to the GaN HEMT, which itself provides numerous benefits, as noted above). Zhao ¶178. Using Fujishima in a GaN HEMT would have been obvious because it would be the use of known technique (Fujishima's technique of raising drain electrodes to improve withstand voltage) to improve similar devices (Sriram's GaN HEMT) in the same way (using the same Fujishima raised drain electrode technique in a GaN HEMT). *Id.* It is also a simple substitution of one known element (Fujishima's drain finger electrode configuration with an elevated end in a MISFET) for another (Sriram's drain finger electrode configuration with flat end in a GaN HEMT) to obtain predictable results (a GaN HEMT with a drain finger electrode configuration that simply raises the drain finger electrode end portion so that it is elevated). *Id.* And a POSA would have applied

Fujishima to HEMTs with a reasonable expectation of success because applying FET configuration to HEMTs was common and routinely performed for the features at issue here, including relating to electric field management. *See* Section VII.A.9; Zhao ¶178; Ex-1018, 70-71 (“parameters of the MISFET are very similar to those of the HEMT”); Ex-1044; Ex-1042; Ex-1043.

4. Claim 9 - The transistor of claim 1, wherein said transistor comprises a group III-V transistor.

Fujishima and Sriram render obvious claim 9 because they disclose a GaN HEMT, which is a group III-V transistor, for the reasons explained for claim 8. Zhao ¶179; *See* Section VII.C.3. The ’755 patent explains that GaN HEMTs are group III-V transistors. ’755 Pat., 2:1-7, 1:47-51, 4:9-21; Ex-1025, 6, 49-52, 540-41; Zhao ¶179.

Thus, Fujishima and Sriram rendering obvious applying Fujishima’s concepts to GaN HEMTs, specifically elevating the end portion of the drain finger electrode (*see* Section VII.C.3), also renders obvious applying Fujishima’s concepts to a group III-V transistor. Zhao ¶180. A POSA would have been motivated to combine these prior art elements (i.e., Fujishima’s concepts and Sriram’s GaN HEMTs) and would have had a reasonable expectation of success in making the combination. *Id.*; Section VII.C.3.

5. Claim 14 - The transistor of claim 10, wherein said transistor is a high-electron-mobility transistor (HEMT).

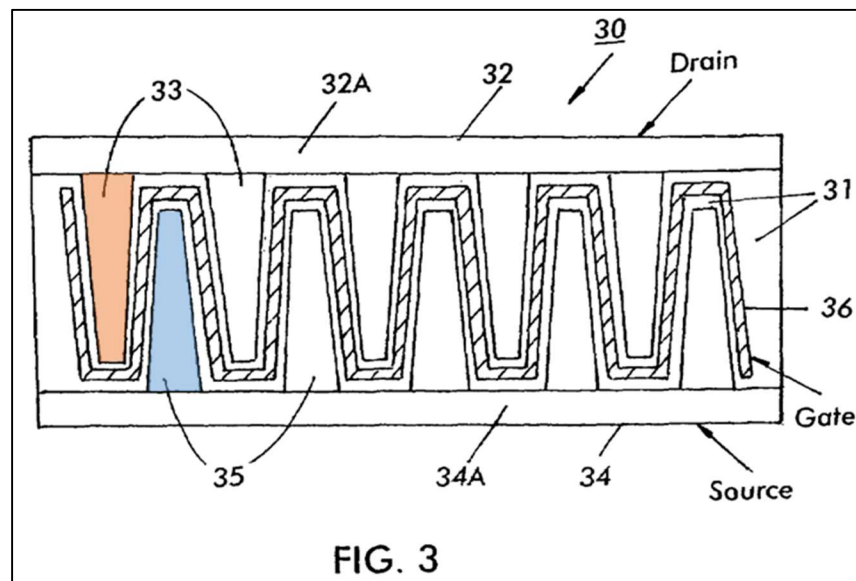
Fujishima and Sriram render obvious claim 14 for the reasons the combination renders obvious claim 8. *See* Section VII.C.3; Zhao ¶181.

D. Ground 1E: Fujishima and Beach Render Obvious Claim 13.

Claim 13 requires the drain finger electrode to be tapered. Zhao ¶182. The '755 patent concedes that Beach discloses “tapered drain and source finger electrodes.” '755 Pat., 8:43-55; Zhao ¶182.

1. Beach

Beach discloses “a FET device with an interdigitated” **drain** and **source** electrodes, each with fingers “hav[ing] bases with a greater dimension than a dimension of the tips” (i.e., a tapered design) that reduces device resistance, promotes compact construction, and prevents high electric fields. Beach, 4:19-24, Abstract, Claim 1, 6:49-62; *see id.*, 4:37-39, 5:50-53.



Id., Fig. 3 (annotated); Zhao 卐卐183-184.

2. General Motivations to Combine

The '755 patent admits that Beach was prior art, which supports a motivation to combine Fujishima and Beach because this admission concedes that Beach is analogous to the '755 patent and similarly directed towards improving overall transistor performance by alleviating electric field within the transistor by modifying the electrode geometry. '755 Pat., 8:43-55; Zhao ¶185.

A POSA would have found it obvious to combine Fujishima and Beach, which disclose complementary systems and methods for configuring transistors and improving overall transistor performance by alleviating electric field within the transistor by modifying the electrode geometry. Beach, 6:49-62, 4:18-24, Abstract, Fig. 3; Section VII.A.1; Zhao ¶185.

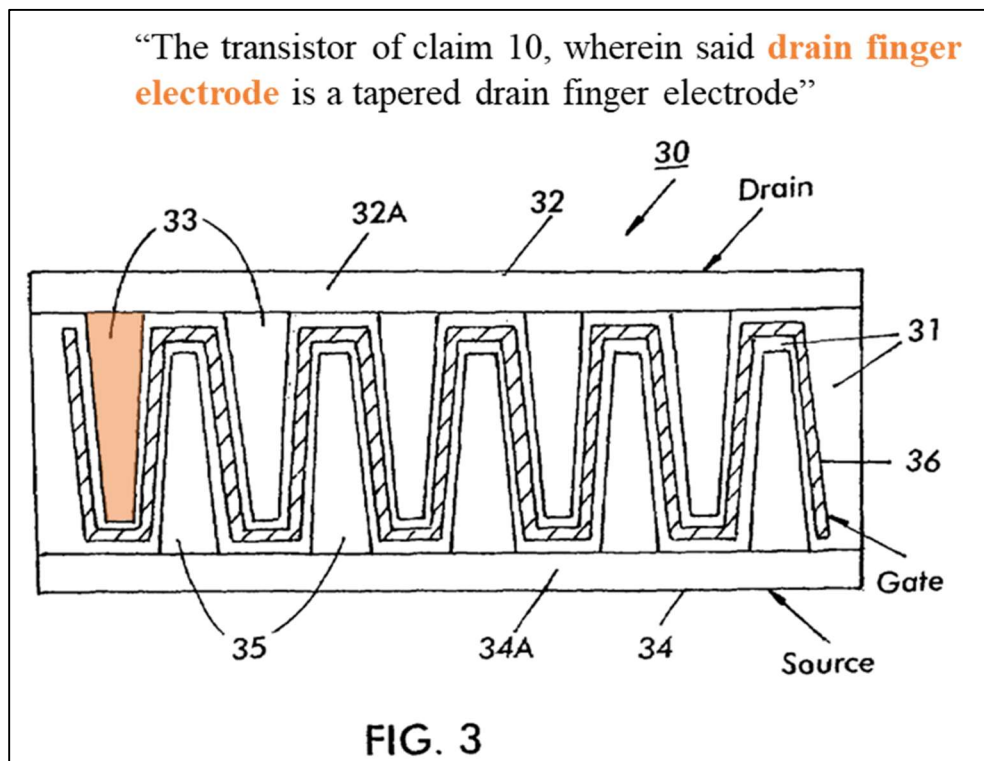
Similar to Fujishima (*see* Section VII.B.2), Beach discloses lateral transistors with interdigitated source and drain finger electrodes. Beach, Abstract, 4:12-24, 4:31-33, 5:51-67, Figs. 1, 3; *see id.*, Claims 1, 6. Beach discloses tapering these electrodes to “prevent high electric fields from being formed.” *Id.*, 6:49-62, 4:18-24, Abstract; *see* Section VII.D.1; Zhao ¶186.

Beach is similar to the '755 patent, as previously described, including in Section VII.B.2. Zhao ¶187.

Thus, Fujishima and Beach are analogous art to the '755 patent and combinable with each other because they belong to the same field of endeavor, disclose comparable systems that operate similar, and are reasonably pertinent to similar problems. Zhao ¶188.

3. Claim 13 - The transistor of claim 10, wherein said drain finger electrode is a tapered drain finger electrode.

Fujishima and Beach render obvious claim 13. Zhao ¶189. Specifically, Beach discloses a tapered **drain finger electrode**. Beach, Abstract, 6:1-11; *see id.*, 6:38-48, 4:21-25, 6:57-61.



Id., Fig. 3 (annotated).

In addition to the general motivations to combine Fujishima and Beach (*see* Section VII.D.2), the AAPA in the '755 patent also supports a motivation to combine Fujishima and Beach's disclosures relating to tapered drain finger electrodes, as well as demonstrates that a POSA knew of tapered drain finger electrodes at the time of the alleged invention. *See* Director Vidal Updated Guidance on the Treatment of Statements of the Applicant in the Challenged Patent in Inter Partes Reviews Under § 311(b) (June 9, 2022). The '755 patent concedes that Beach's "tapered drain and source finger electrode[]" designs were prior art and provided "higher breakdown voltages and lower ON-resistance." '755 Pat., 8:43-55. Thus, a POSA would have

been motivated to combine Fujishima and Beach based on the AAPA. Zhao ¶¶190-191.

A POSA would have also had additional specific motivations to combine the references. Zhao ¶192; *see* Section VII.A.14. A POSA would have found this combined configuration obvious because both references disclose specific configurations for a drain finger electrode in similar types of transistors that minimizes the concentration of electric field and provides improvements to the transistor device, which would have strongly motivated a POSA to combine these references. Zhao ¶193; Fujishima, 2:54-64, 3:1-33, 3:44-52, 6:13-33, 12:23-40, Fig. 6(b); Beach, 4:6-25, 6:57-61; *see id.*, Abstract, 5:51-53, 6:1-11, 1:25-39.

This combination would have been routine because implementing specific geometry for electrode fingers (i.e., Beach's tapered drain finger electrode) is a simple design change of making the base width larger than the tip width and can be implemented during the planning phases. Zhao ¶194. Thus, a POSA would have found it straightforward with a reasonable expectation of success to modify Fujishima's electrode structure such that the drain finger electrode was tapered, as Beach discloses. *Id.* A POSA would have had a reasonable expectation of success in making this modification because it is a simple design change that (i) can be implemented during the planning process, (ii) only modifies the electrode geometry, which is a simple change, and (iii) still utilizes the same fabrication process. *Id.*

A POSA would have been motivated to make the combination to (i) increase device power rating, (ii) decrease device dimensions and permit a more compact device construction, (iii) reduce device resistance and balance current flow, and (iv) decrease power loss due to current variation across the electrode finger. Zhao ¶195; Beach, Abstract, 3:1-8, 4:6-33, 4:53-64, 6:1-11, 6:24-48, 6:57-61.

The combination simply combines prior art elements (Fujishima's and Beach's transistor and electrode configurations) according to known methods to yield predictable results (using tapered drain finger electrodes). Zhao ¶196; *see* Section VII.A.14. It is also a simple substitution of one known element (Fujishima's Figure 8 drain finger electrode configuration) for another (Beach's Figure 3 tapered drain finger electrode configuration) to obtain predictable results (a configuration of the drain finger electrode of a transistor that reduces the electric field, as both references seek to do). Zhao ¶196. It also uses a known technique (Beach's tapered drain finger electrode configuration) to improve similar devices (transistors disclosed in Fujishima and Beach) in the same way (to reduce the electric field). *Id.*

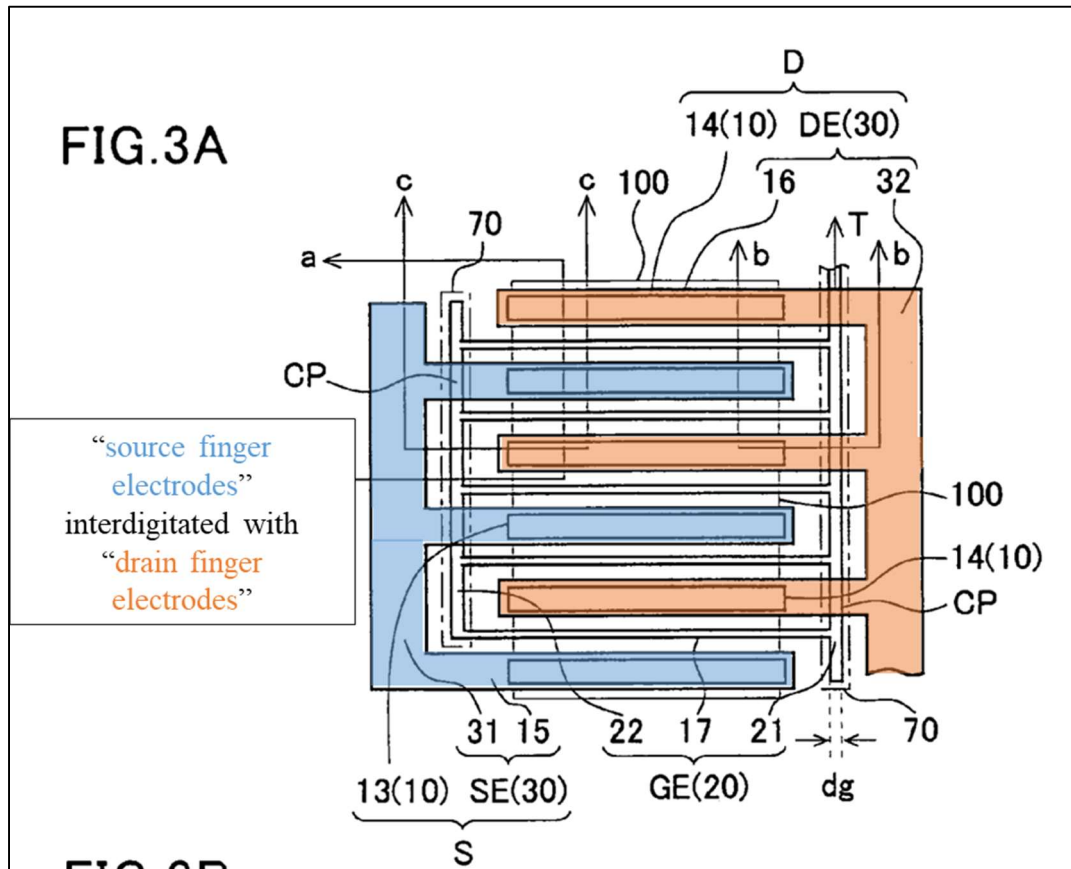
VIII. ASANO GROUNDS 2A-2B

A. Asano Anticipates (2A) and/or Renders Obvious (2B) Claims 1-4 and 8-9.

1. Asano

Asano discloses group III-V FETs (Asano ¶¶19, 55), including “a HEMT (High Electron Mobility Transistor),” *id.* ¶¶55, 74, 110, with a plurality of [source](#)

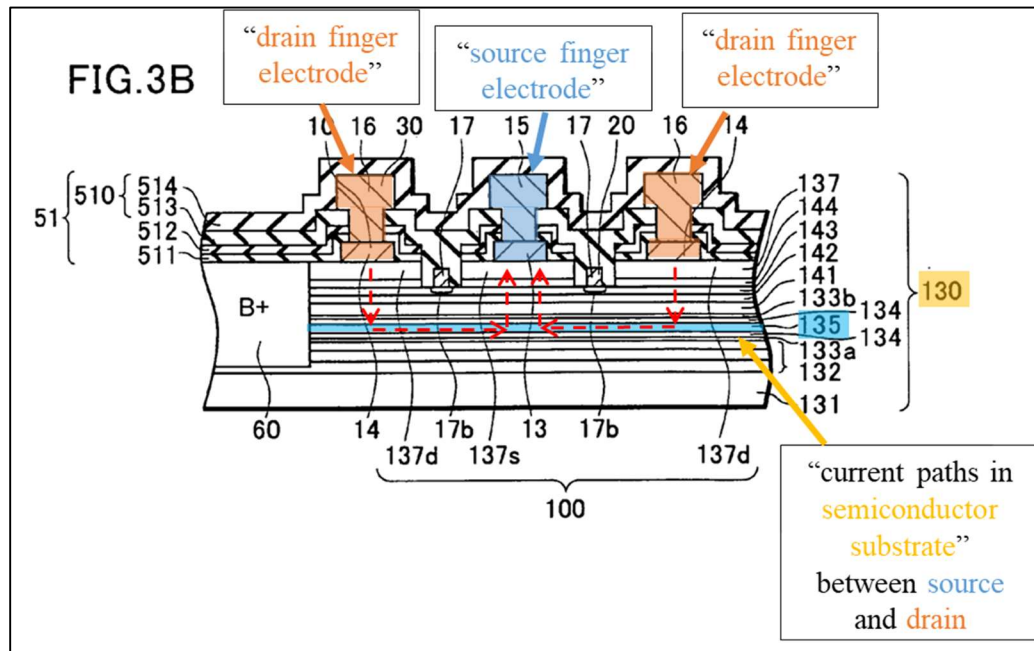
electrodes and **drain electrodes** in an “alternative[]” repeating pattern (interdigitated). *Id.*, Abstract.



Id., Fig. 3A (annotated). It discloses drain electrodes 14 and 16 and source electrodes 13 and 15 that are “strip-shaped” and disposed in operation region 10. *Id.* ¶75.

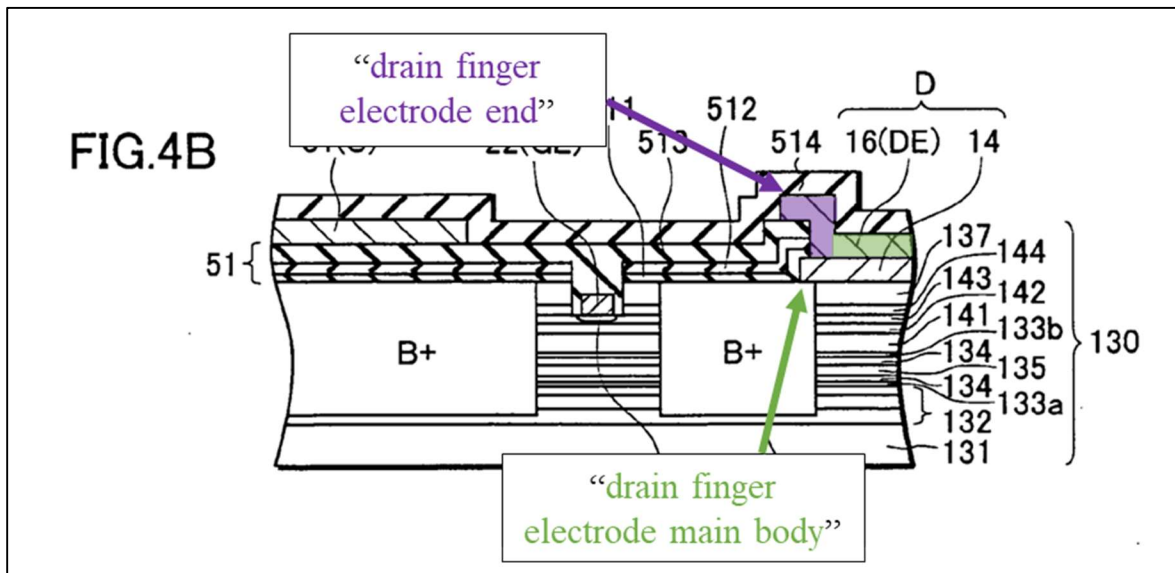
Figure 3B shows the drain and source electrodes formed on a substrate with multi-layer stack, including a semi-insulating GaAs substrate 13, undoped buffer layers 132, a first and second n⁺ type AlGaAs electron supply layers 133a and 133b, a spacer layer 134, **an undoped InGaAs channel (electron transit) layer 135**, a first, second, and third undoped layers 141-143, a stable layer 144, and a cap layer

137. Asano ¶81. Asano's **channel layer 135** in **substrate 130** creates the current path, between **source finger electrodes 13 and 15** and **drain finger electrodes 14 and 16**. Zhao ¶¶197-199; '755 Pat., 9:34-37 (describing a substrate as a material stack).



Asano, Fig. 3B (annotated).

Asano's Figure 4B shows the **end of its drain finger electrode** elevated above the plane of its **drain electrode finger main body** by interposing “nitride film 513” underneath the end portion. Asano, Fig. 4B, ¶¶101, 186.



Asano, Fig. 4B (annotated); Zhao ¶200.

2. Claim 1

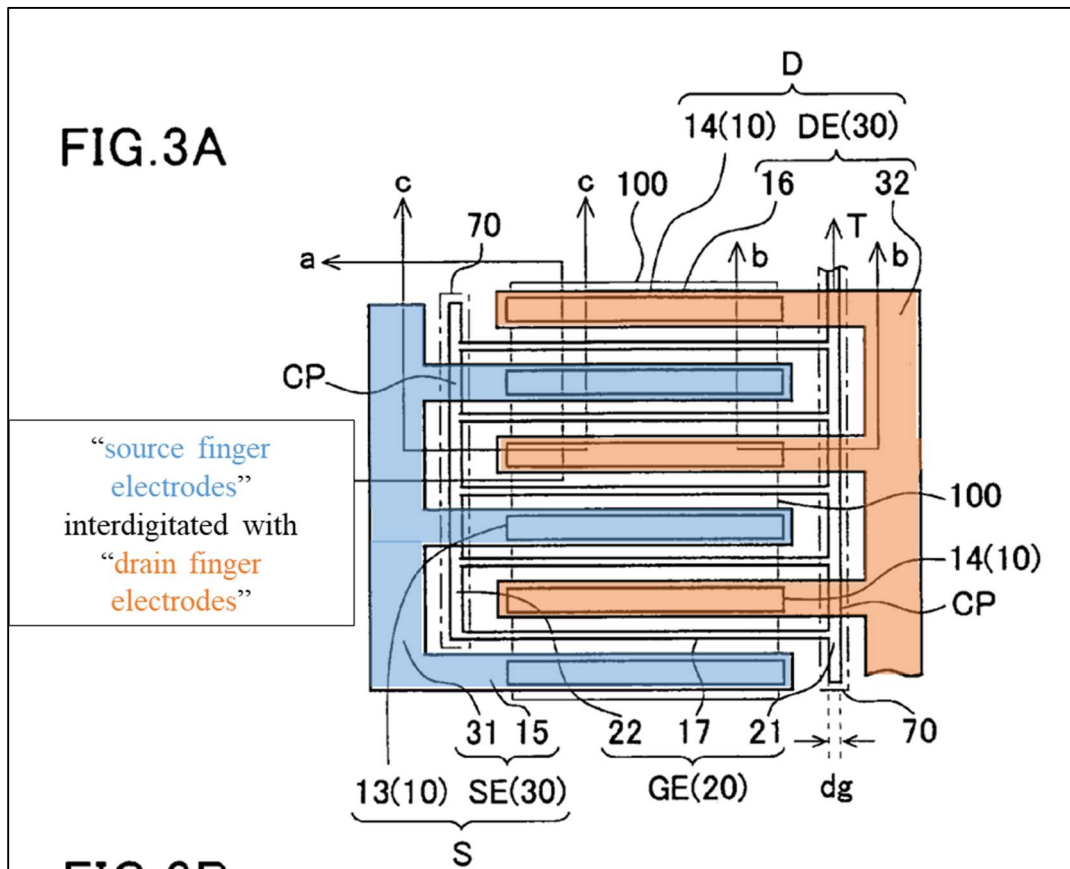
a. [1pre]: A transistor comprising:

If the preamble is limiting, Asano’s “field effect **transistor**” discloses it.

Asano ¶¶19, 55, Claims 1-12; Zhao ¶201.

b. [1a]: drain finger electrodes interdigitated with source finger electrodes;

Asano discloses or renders obvious [1a] because it discloses “**a plurality of source electrodes**” and “**drain electrodes**” elongated in a first direction and “being positioned alternatively with respect to a second direction” (interdigitated). Asano, Abstract, ¶19, Claim 1; Zhao ¶202; *see also* Ex-1028-1029.



Asano, Fig. 3A (annotated).

Asano has two source electrodes 13 and 15 or two drain electrodes 14 and 16 on each finger. Asano ¶¶75, 63, 66. Either the first set of source and drain electrodes (i.e., 13/14), second set (i.e., 15/16), or both collectively satisfy the claimed source finger electrodes and drain finger electrodes, respectively, because all are interdigitated. *Id.* ¶¶63; Zhao ¶203. **For Ground 2B**, to the extent a single combined source finger electrode and single combined drain finger electrode is needed, that configuration would have been obvious. Zhao ¶204. As Dr. Zhao explains, source finger electrodes 13 and 15 work together as a single source finger electrode (i.e.,

the claimed **source finger electrode**) and drain finger electrodes 14 and 16 work together as a single drain finger electrode (i.e., the claimed **drain finger electrode**), consistent with Asano's disclosures. *Id.*; Asano ¶63, Fig. 4B.

c. [1b]: current conduction paths in a semiconductor substrate between said drain finger electrodes and said source finger electrodes;

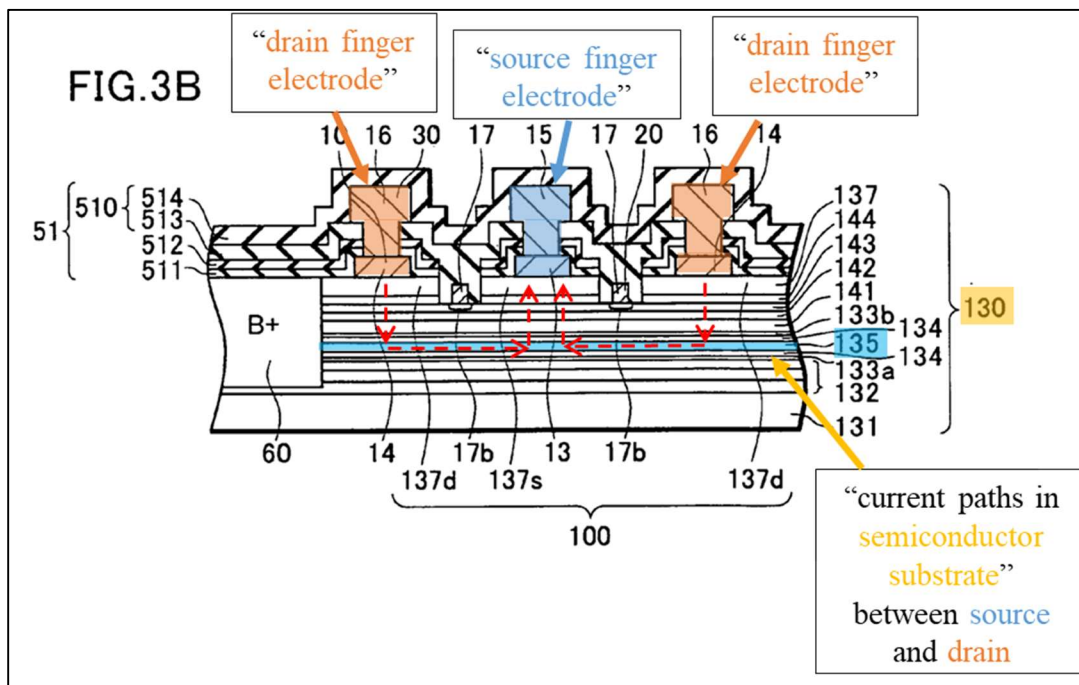
Asano discloses [1b] because it discloses a HEMT in which channel regions create current paths for electron flow through channel layer 135 from the source finger electrodes 13 and 15 to the drain finger electrodes 14 and 16. Zhao ¶205.

Asano's HEMT includes a **substrate structure** with **a channel (electron transit) layer**. Asano ¶56, 81; Section VIII.1; Zhao ¶¶206-207. Asano's Figure 3B is a "cross-sectional view **along the line a-a** in Fig. 3A" cutting across two drain finger electrodes and one source finger electrode. Asano ¶81.



Id., Fig. 3A (annotated).

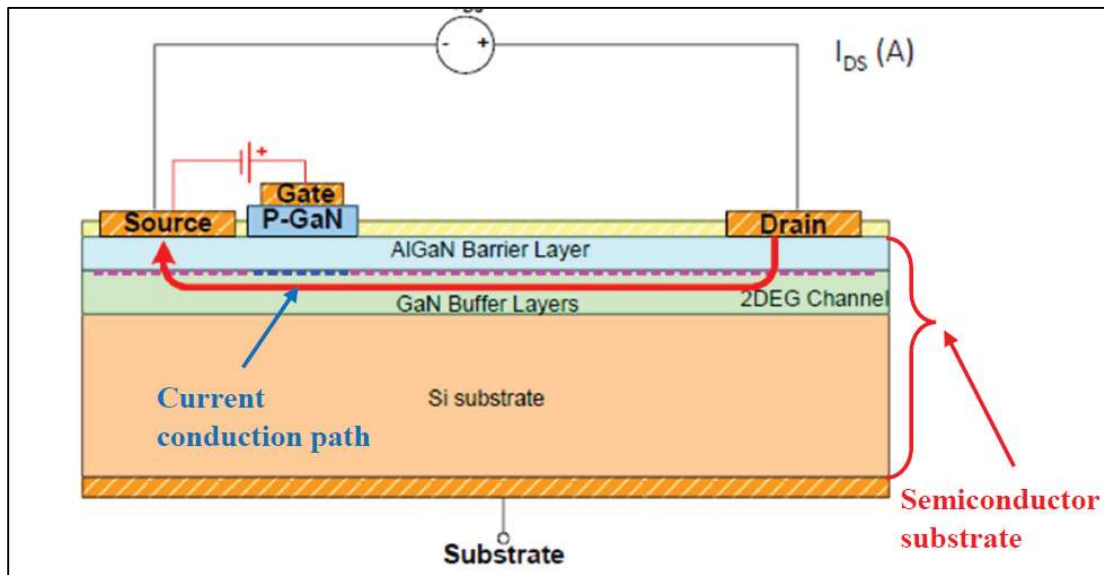
In Figure 3B, Asano's **channel layer 135 in substrate 130** creates the current path (dotted red line) between **source finger electrodes 13 and 15** and **drain finger electrodes 14 and 16**.



Asano, Fig. 3B (annotated).

Asano has multiple drain finger electrodes and source finger electrodes disposed between gate electrodes in an active area of the transistor. *See* Asano Fig. 3A, ¶¶76-77; Zhao ¶208. A POSA would have understood that **channel layer 135** creates a current path between each adjacent **source** and **drain**, constituting multiple current paths in the device, two of which are shown in Figure 3B. Zhao ¶208.

This is consistent with Infineon's understanding of this limitation. Ex-1026, 5, 8. Infineon explained that HEMT devices, like Asano's device, have current conduction paths between drain finger electrodes and source finger electrodes—providing the below exemplary figure:

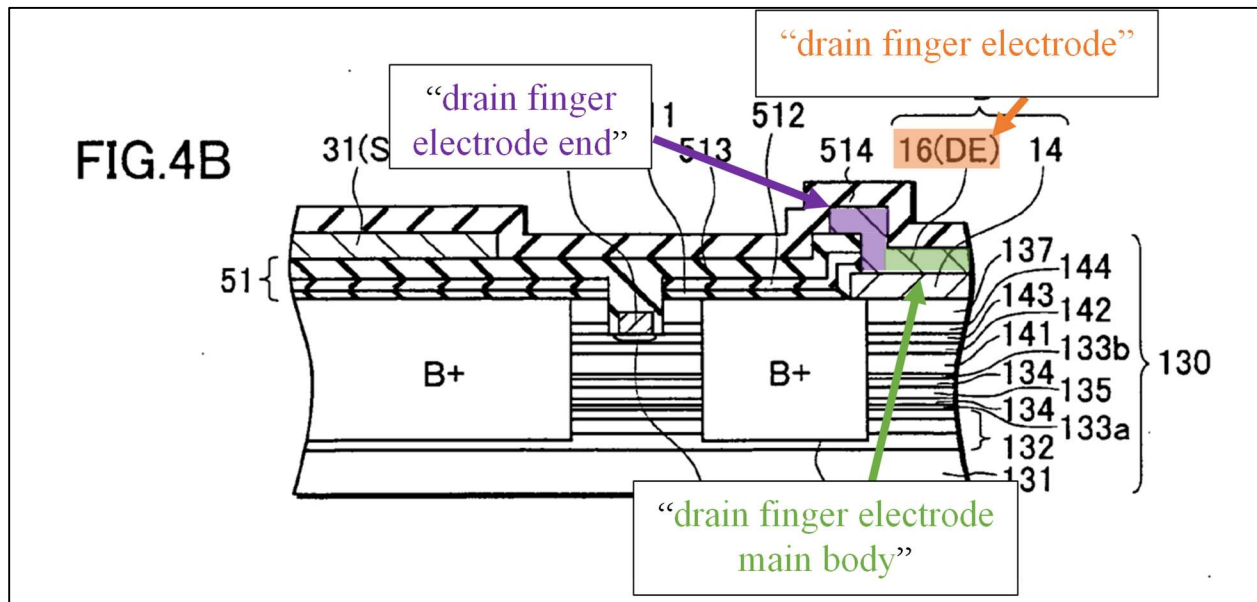


Id., 8. Moreover, this is also consistent with Infineon’s statements in another IPR proceeding explaining that FETs generally include a gate electrode that “control[s] the flow of electrical current between the source and drain.” Ex-1031, 7.

- d. **[1c]: at least one of said drain finger electrodes having a drain finger electrode main body and a drain finger electrode end,**

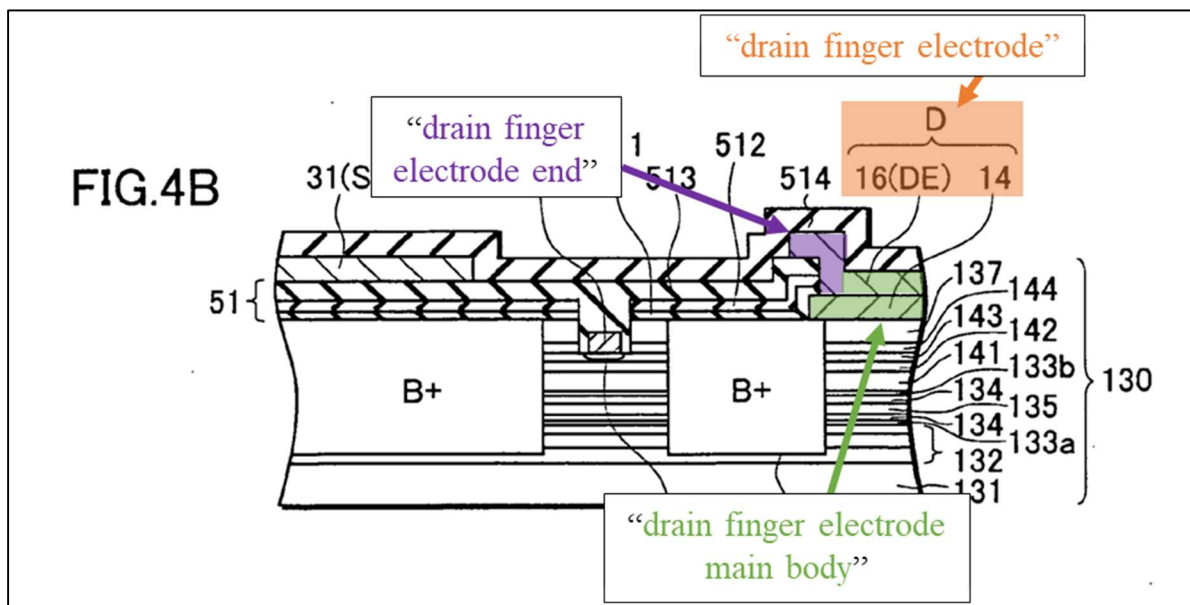
Asano discloses or renders obvious [1c] because drain finger electrode 16 or collectively, drain finger electrode 14/16, has a main body and an end. Zhao ¶209.

Asano’s Figure 4B shows a cross-sectional view of interdigitated **source finger electrodes** and **drain finger electrodes** (Section VIII.A.2.b) “**along the line c-c** in Fig. 3A.” Asano ¶110.



Asano, Fig. 4B (annotated); Zhao ¶¶210-211.

Additionally, for mapping the drain finger electrode to the drain electrodes 14/16 collectively or for **Ground 2B**, drain finger electrode 14 constitutes part of the drain finger electrode main body, as shown in Asano's Figure 4B.

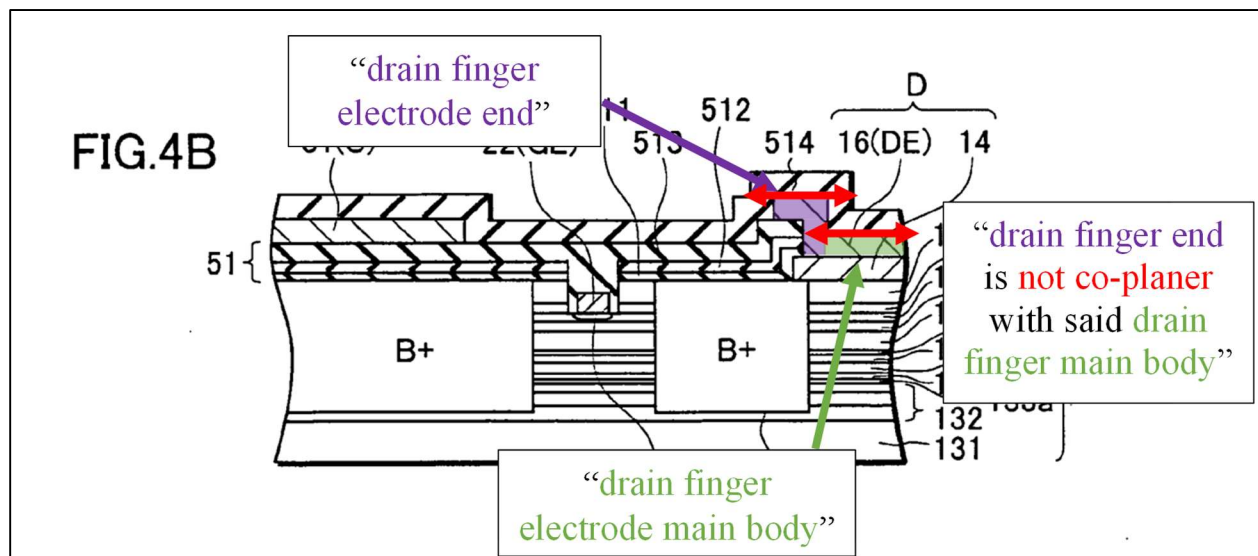


Asano, Fig. 4B (annotated); Zhao ¶212.

- e. [1d]: wherein at least a portion of said drain finger end is non-coplanar with said drain finger electrode main body.

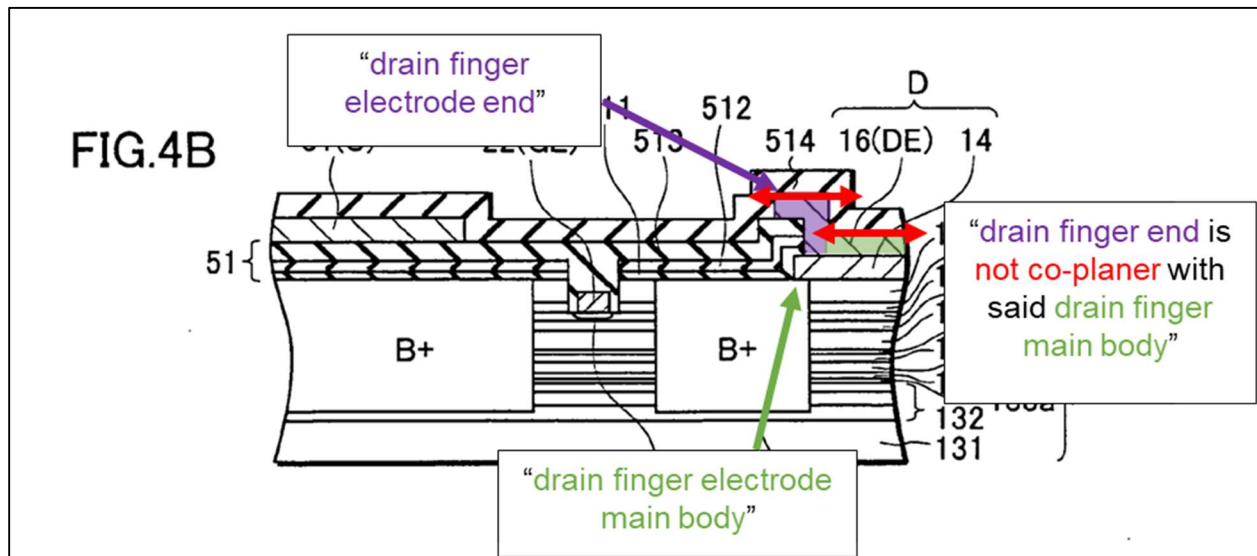
Asano discloses or renders obvious [1d] because the end portion of drain finger electrode 16 is elevated and not co-planar with drain finger electrode 16's main body or the main body of the combined drain electrode 14/16. Zhao ¶213.

For **Ground 2A**, Asano's Figure 4B shows a "nitride film 513" elevating the **drain finger electrode end** to a non-coplanar position above the plane of the **drain electrode finger main body**.



Asano, Fig. 4B (annotated), ¶¶101, 186; Zhao ¶214.

Additionally, for mapping the drain finger electrode to the drain electrodes 14/16 collectively or for **Ground 2B**, Asano's Figure 4B also shows the **drain finger electrode end** elevated above the plane of the **drain electrode finger main body**.



Asano, Fig. 4B (annotated), ¶¶101, 186; Zhao ¶215.

Under both mappings, at least a portion of the **drain finger electrode end** is non-coplanar with respect to the **drain finger electrode main body** because the **end** is on a horizontal plane that is not on the same horizontal plane as any part of the **main body**. Zhao ¶216. Moreover, a POSA would have understood that this configuration would have helped alleviate the high electric field at the **drain finger electrode end**. *Id.*; Asano ¶¶137, 143, 233, Figs. 3A-4B.

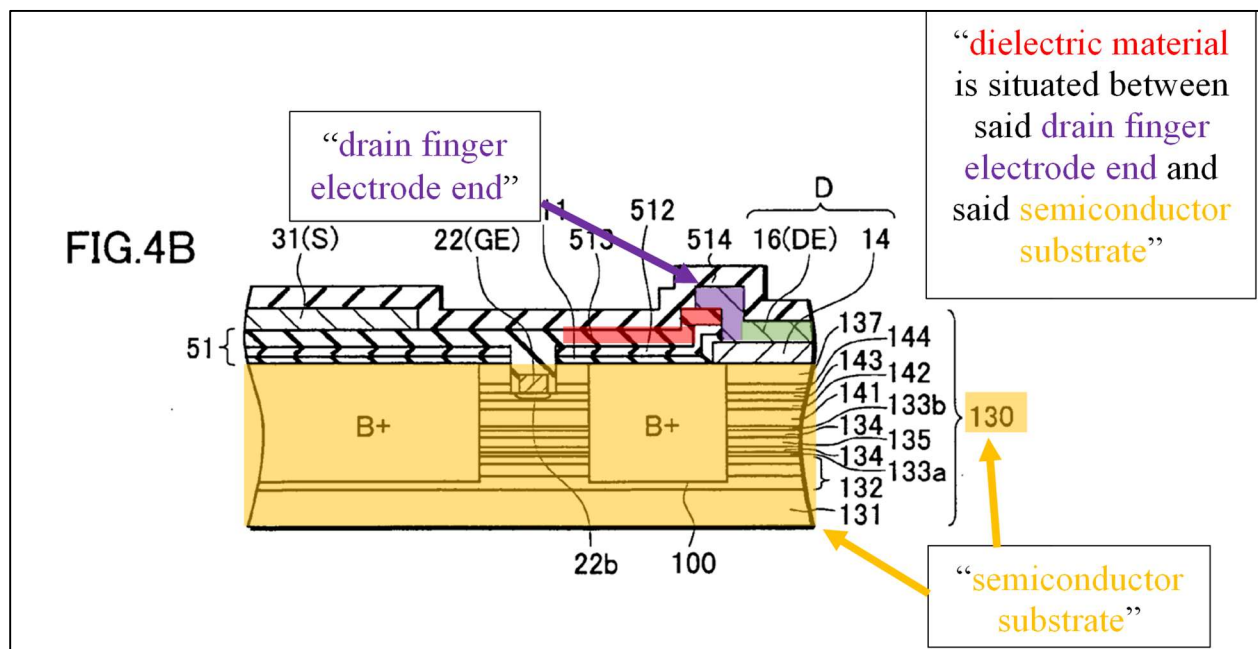
3. Claim 2 – The transistor of claim 1, wherein a dielectric material is situated between said drain finger electrode end and said semiconductor substrate.

Asano discloses or renders obvious claim 2 because nitride film 513 is situated between the drain finger electrode end and semiconductor substrate 130. Zhao ¶217.

For Ground 2A, Asano discloses **nitride film 513**, which is a dielectric material because it is an insulating material with a dielectric constant. Asano ¶¶182,

56. As Dr. Zhao explains, a POSA would have understood that nitride films were commonly used in transistor devices as a dielectric, insulating material, for example, silicon nitride. Zhao ¶218 (citing Ex-1018, 184-87). This **nitride film 513** is a dielectric material under the '755 patent's description of such a material as any "insulating material." '755 Pat., 10:23-29, 10:10-22; Zhao ¶218.

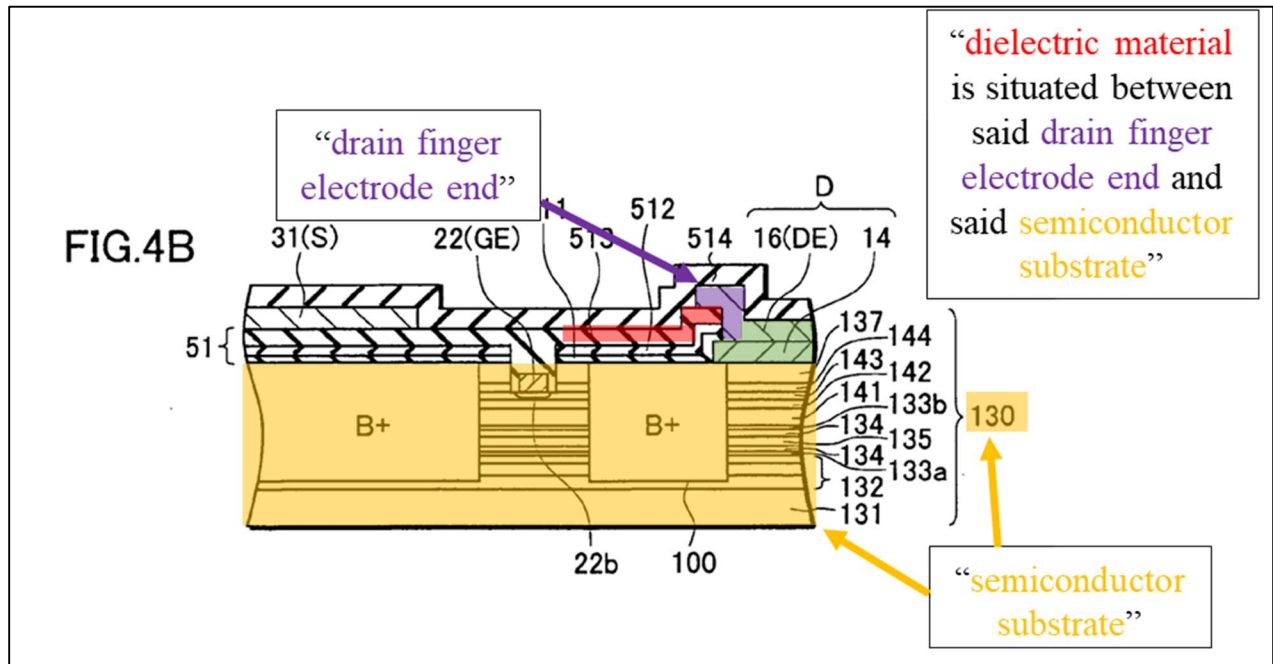
Asano discloses a **semiconductor substrate 130**. Asano ¶56, 81; Section VIII.A.1. Figure 4B shows **"nitride film 513"** situated between **drain finger electrode end** and **substrate 130**.



Asano, Figs. 4B (annotated), 4A, ¶¶101, 186; Zhao ¶¶219-220.

Additionally, for mapping the drain finger electrode to the drain electrodes 14/16 collectively or for **Ground 2B**, Figure 4B similarly shows **"nitride film 513"**

situated between **drain finger electrode end** and **substrate 130**. Asano, Fig. 4A, ¶¶101, 186.



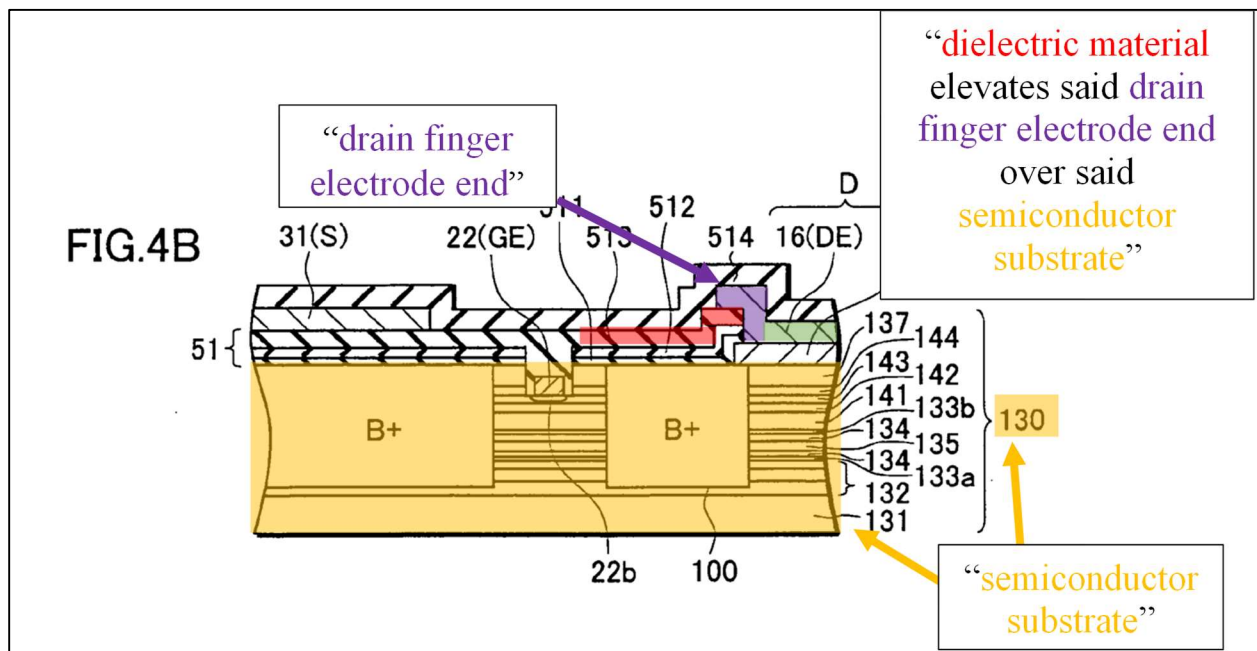
Id., Figs. 4B (annotated), 4A, ¶¶101, 186; Zhao ¶221.

4. **Claim 3 – The transistor of claim 2, wherein said dielectric material elevates said drain finger electrode end over said semiconductor substrate.**

Asano discloses or renders obvious claim 3 because nitride film 513 elevates the drain finger electrode end over semiconductor substrate 130. Zhao ¶222.

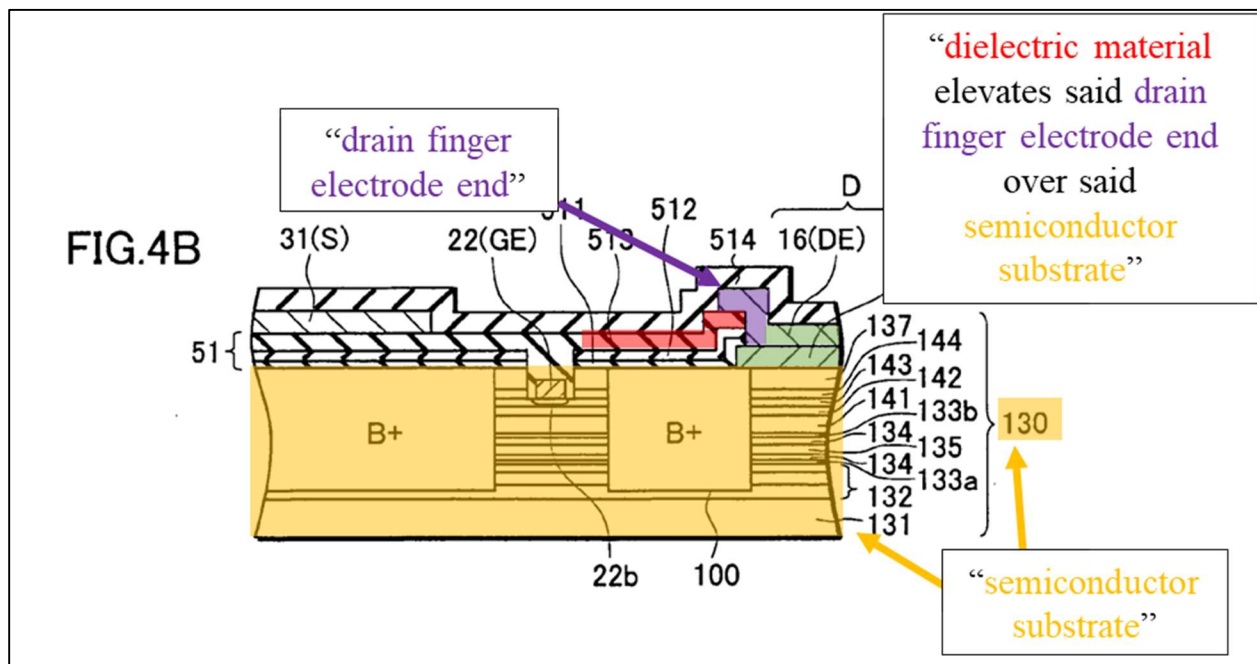
Nitride film 513 is a dielectric material and **substrate 130** is a semiconductor substrate. Section VIII.A.3.

For **Ground 2A**, Figure 4B shows that “**nitride film 513**” elevates **drain finger electrode end** over **substrate 130** because **film 513** is situated between the **end** and **substrate 130**, elevating the **end** above the plane of **substrate 130**.



Asano, Fig. 4B (annotated), ¶¶101, 186; Zhao ¶¶223-225.

Additionally, for mapping the drain finger electrode to the drain electrodes 14/16 collectively or for **Ground 2B**, Asano's Figure 4B shows that “**nitride film 513**” elevates **drain finger electrode end** over **substrate 130** for the same reasons noted for Ground 2A.

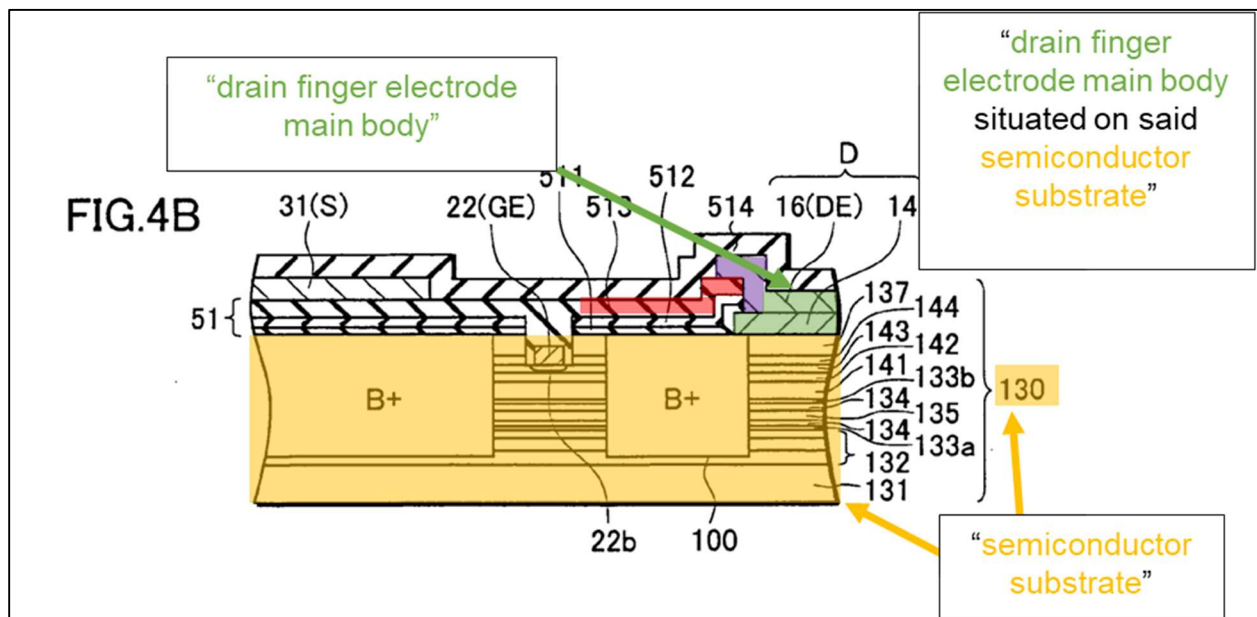


Asano, Fig. 4B (annotated), ¶¶101, 186; Zhao ¶226.

5. Claim 4 – The transistor of claim 1, wherein said drain finger electrode main body is situated on said semiconductor substrate.

Asano discloses or renders obvious claim 4 because its drain finger electrode 14's main body sits directly on top of substrate 130 (Section VIII.A.3) and drain finger electrode 16 has a **drain finger electrode main body** (Sections VIII.A.2.c-VIII.A.2.d). Zhao ¶¶227-229.

For mapping the drain finger electrode to the drain electrodes 14/16 collectively or for **Ground 2B**, Asano's Figure 4B shows that the **drain finger electrode main body 14** is situated directly on **substrate 130**.



Asano, Fig. 4B (annotated), ¶¶101, 186; Zhao ¶230.

6. Claim 8 – The transistor of claim 1, wherein said transistor is a high-electron-mobility transistor (HEMT).

Asano discloses or renders obvious claim 8 because its transistor is a HEMT.

Zhao ¶231.

Asano discloses FETs (Asano ¶¶19, 55), explaining that a “FET may be ... a HEMT.” *Id.* ¶¶55, 74, 110, Figs. 3-4; Zhao ¶232.

7. Claim 9 – The transistor of claim 1, wherein said transistor comprises a group III-V transistor.

Asano discloses or renders obvious claim 9 because its transistor comprises substrate 130 stack that includes various group III-V layers, like those made of “AlGaAs” and “InGaAs.” Asano ¶81; Zhao ¶¶233-234.

A POSA would have understood that a group III-V transistor includes layers comprising alloys made of metals from groups III and V of the periodic table. Zhao ¶235; Ex-1025, 6, 49-52, 540-41. Group III of the periodic table includes B, **Al**, **Ga**, and In. Group V of the periodic table includes N, P, **As**, and Sb. Therefore, alloys like GaAs, AlGaAs, and InGaAs included in Asano's transistor, are group III-V because they include metals from both group III and group V of the periodic table. Zhao ¶235; '755 Pat., 1:27-55, 4:9-21.

IX. DISCRETIONARY DENIAL IS NOT WARRANTED

A. *Fintiv* Denial Is Improper

Under the Office's interim guidance, dated June 21, 2022, ("*Interim Procedures*"), *Fintiv* does not apply. The parallel ITC Investigation does not implicate *Fintiv*. *Interim Procedures*, 7.

The *Fintiv* factors in view of the parallel district court action weigh strongly in favor of institution because the district court case has minimal investment from the Court or Parties, does not have a trial date, and has been stayed. Ex-1030.

B. §325(d) Denial Is Improper

The factors in *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8, 17-18 (PTAB Dec. 15, 2017) and *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6, 8-11 (PTAB Feb. 13, 2020) (precedential) favor institution.

Advanced Bionics, step 1 (*BD* factors (a), (b), (d)) favor institution because Asano, Ludikhuize, and Sriram were not before the Office during prosecution. Ex-1002, pgs. 2-4, 15-28; '755 Pat., Cover.

Advanced Bionics, step 2, (*BD* factors (c), (e), (f)) favor institution because the cited references are not cumulative of those before the Office during prosecution. Indeed, no references were meaningfully addressed by the Office during prosecution, and the claims were never rejected. Ex-1002. The Examiner stated that the claims were allowable because “there is no teaching or suggestion in the art of record disclosing a transistor ... wherein at least a portion of the drain finger end is non-coplanar.” *Id.*, pgs. 11. The prior art cited in this Petition teaches that limitation.

X. MANDATORY NOTICES UNDER 37 C.F.R. §42.8

C. Real Party-in-Interest

The real parties-in-interest are Innoscience America, Inc.; Innoscience (Zhuhai) Technology Company, Ltd.; and Innoscience (Suzhou) Technology Holding Company, Ltd.

D. Related Matters

To the best of Petitioner’s knowledge, the '755 patent is involved in:

Name	Number	Forum	Filed
<i>Infineon Techs. Austria AG v. Innoscience (Suzhou) Tech. Co., Ltd. et al.</i>	3:24-cv-01553	N.D. Cal.	March 13, 2024

<i>In re Certain Semiconductor Devices and Products Containing the Same</i>	337-TA-1414	ITC	July 26, 2024
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E. Lead and Backup Counsel Information

Petitioner provides the following designation of counsel:

Lead Counsel	Back-Up Counsel
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Petitioners consent to electronic service at the following email address:
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F. Standing

The '755 patent is available for IPR. Petitioner is not barred or estopped.

XI. CONCLUSION

Petitioner requests the Board institute this IPR and find all claims unpatentable.

Dated: October 22, 2024

/Lionel M. Lavenue/
Lionel M. Lavenue, Lead Counsel
Reg. No. 46,859

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(a)(1)(i), the undersigned hereby certifies that the foregoing PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 9,070,755 contains 13,614 words, excluding parts of this Petition exempted under § 42.24(a), as measured by the word-processing system used to prepare this paper.

Dated: October 22, 2024

By: Lionel M. Lavenue/
Lionel M. Lavenue, Lead Counsel
Reg. No. 46,859

CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing **Petition for *Inter Partes* Review of U.S. Patent No. 9,070,755, the Power of Attorney, and Exhibits 1001 through 1044** were served on October 22, 2024, by Priority Mail Express, or by means at least as fast and reliable as Priority Mail Express on the correspondence address of record indicated in the Patent Office's Patent Center website for the '755 patent:

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Dated: October 22, 2024

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