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Reznik

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(54) **PARALLEL INTERFERENCE CANCELLATION RECEIVER FOR MULTIUSER DETECTION OF CDMA SIGNALS**

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(65) **Prior Publication Data**

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(60) Provisional application No. 60/160,259, filed on Oct. 19, 1999.

(51) **Int. Cl.**[7] **H04B 1/69**
(52) **U.S. Cl.** **375/148**
(58) **Field of Search** 375/130, 144, 375/147, 148, 285, 229, 234, 346; 370/441, 342, 335

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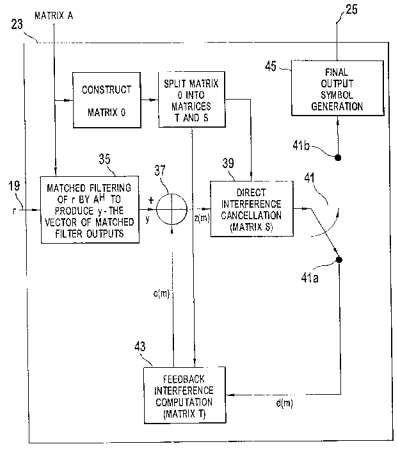
(57) **ABSTRACT**

A parallel interference cancellation receiver that reduces impulse response interference using a model of the received signal similar to that used in block linear equalizers. Block linear equalizers comprise decorrelating receivers, zero-forcing receivers, minimum mean square error receivers and the like. The invention comprises an interference computation processor feedback loop for correcting the output of a direct interference canceller. The m iterative process removes interferers from the output symbols of a matched-filter. The PIC receiver uses received signal models of the various block linear equalizers that do not assume that each subchannel consists of several distinct paths. The receiver estimates the impulse response characteristic of each subchannel as a whole.

61 Claims, 9 Drawing Sheets



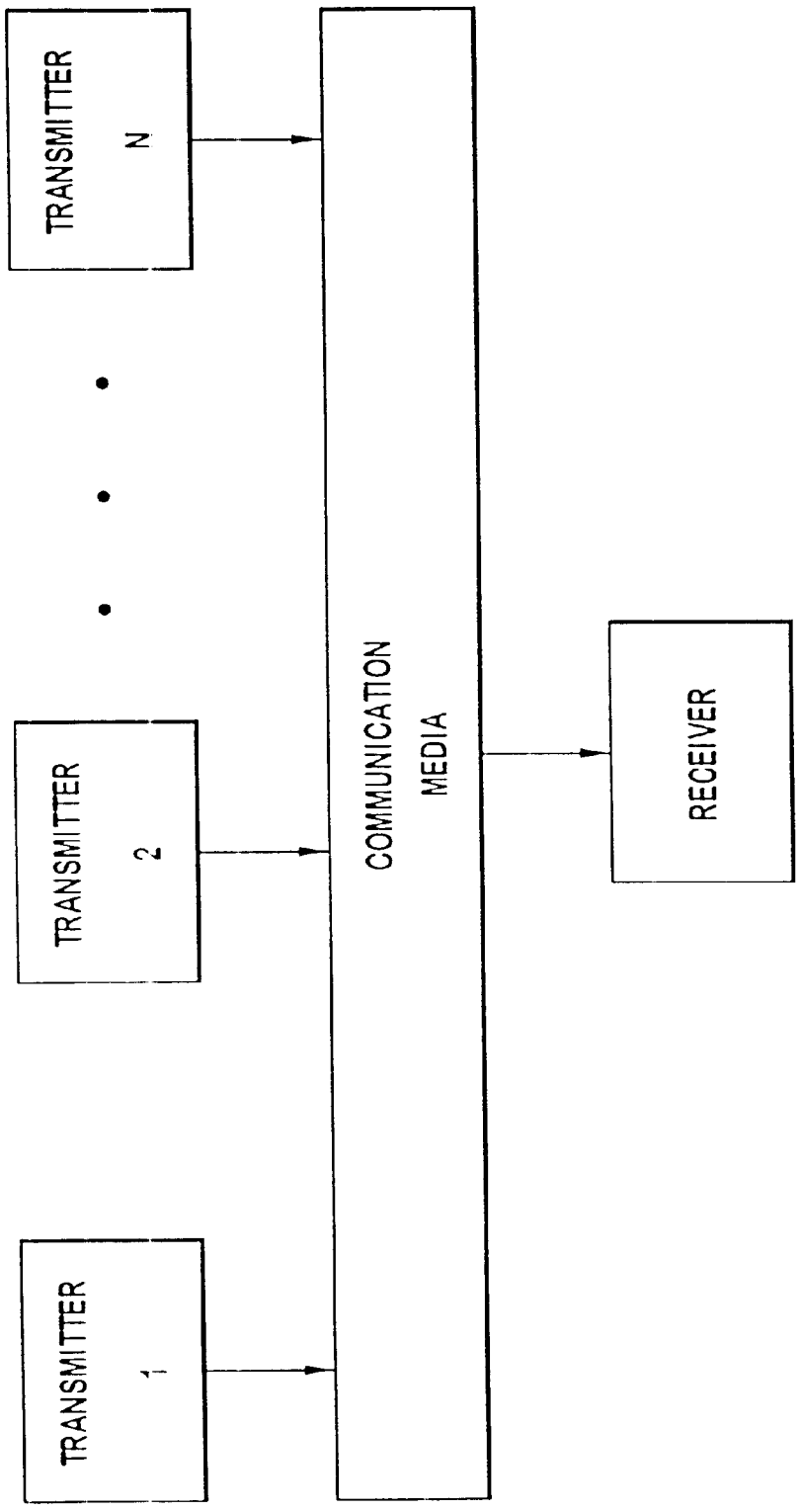


FIG. 1
PRIOR ART

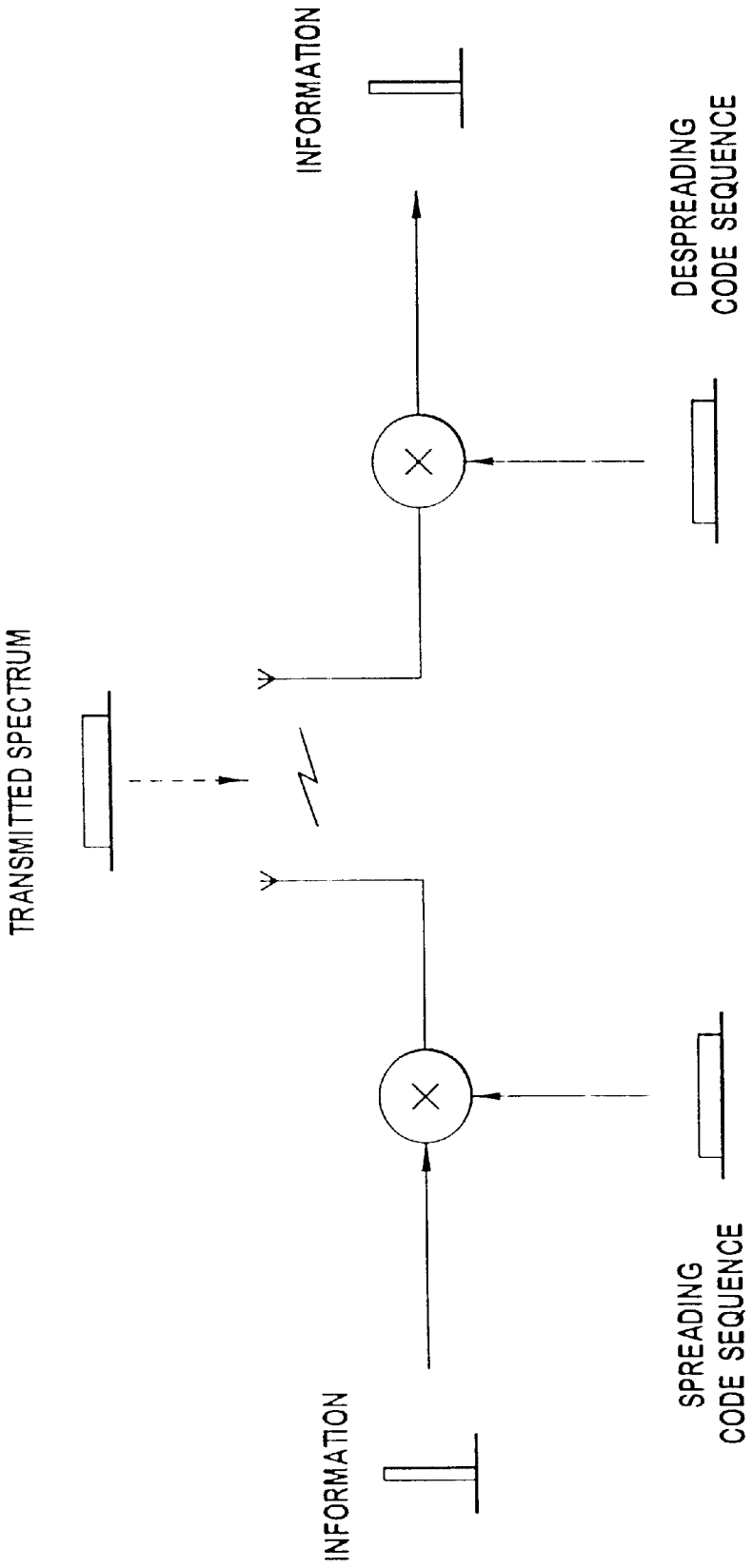


FIG. 2
PRIOR ART

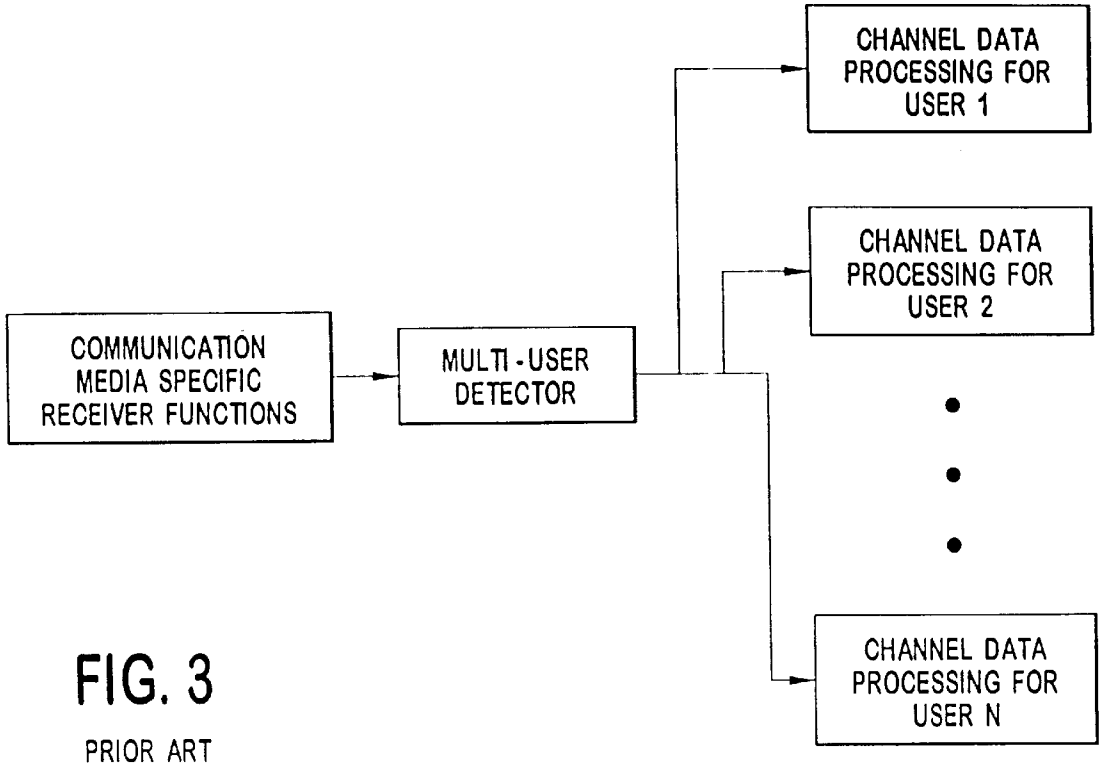


FIG. 3
PRIOR ART

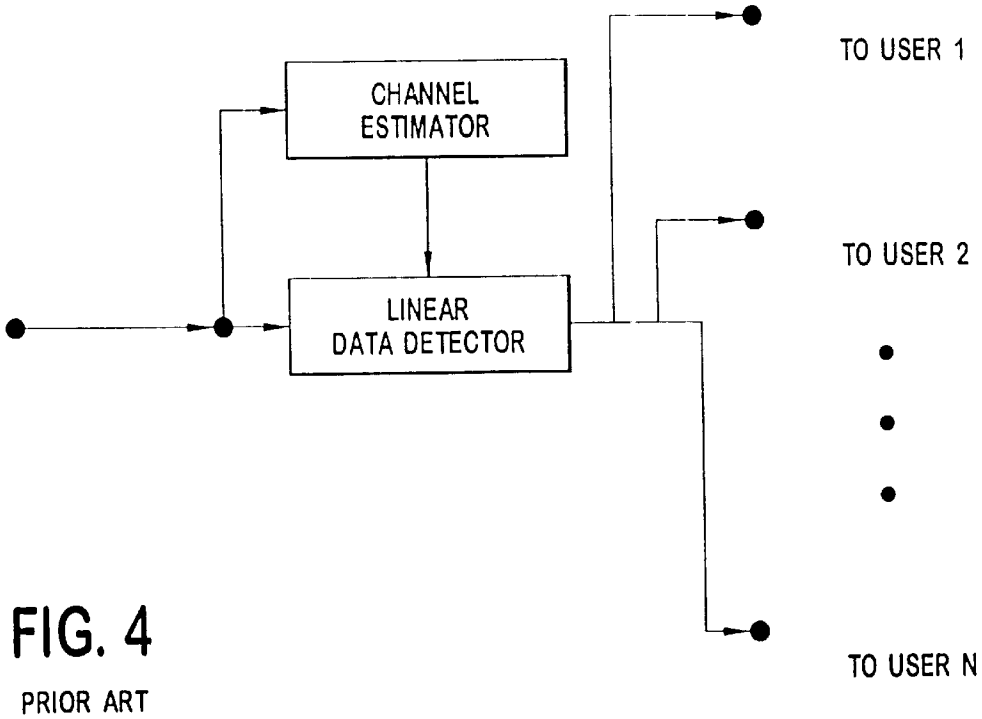


FIG. 4
PRIOR ART

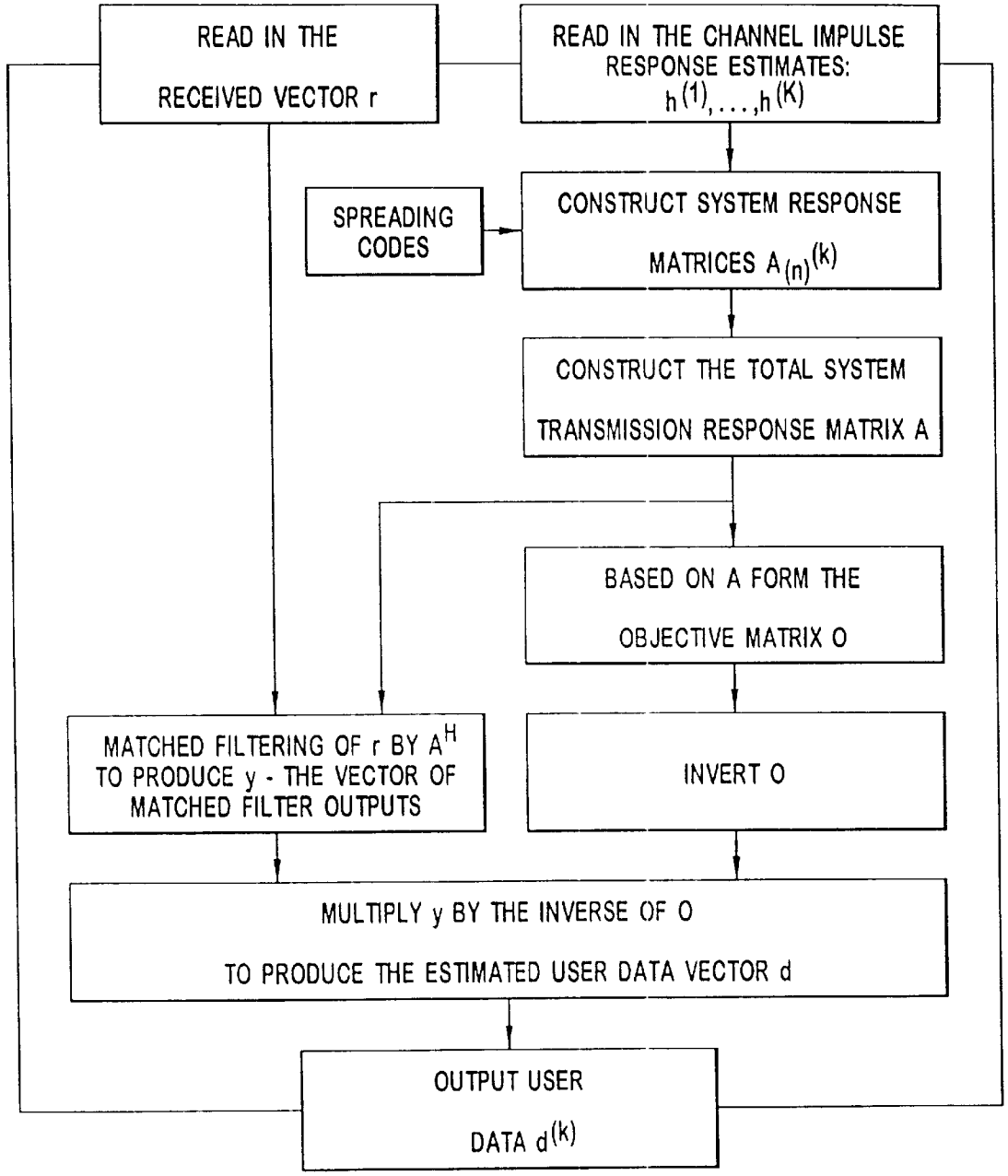


FIG. 5
PRIOR ART

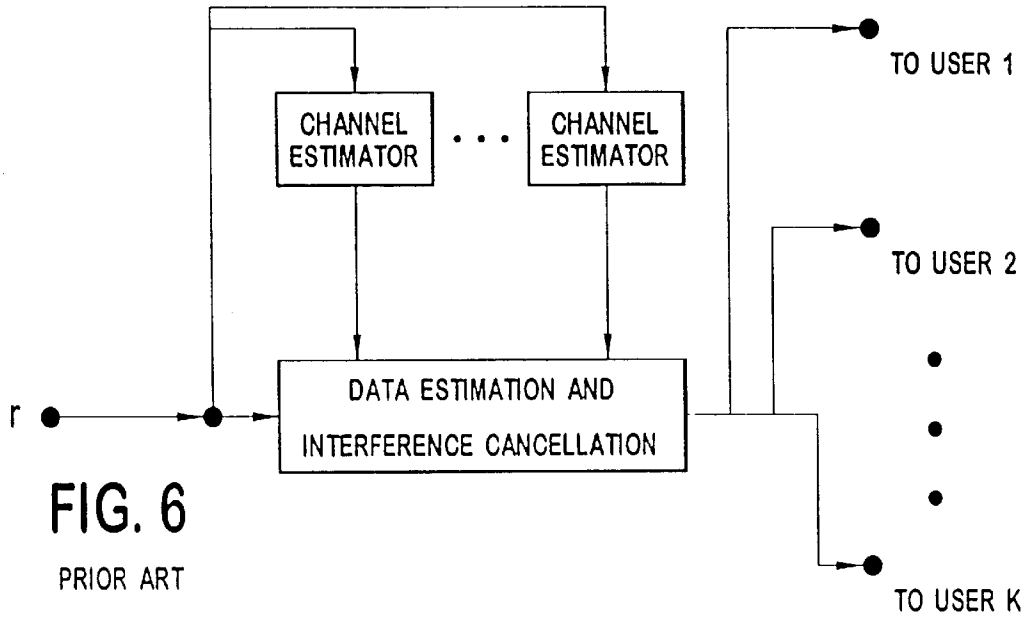


FIG. 6
PRIOR ART

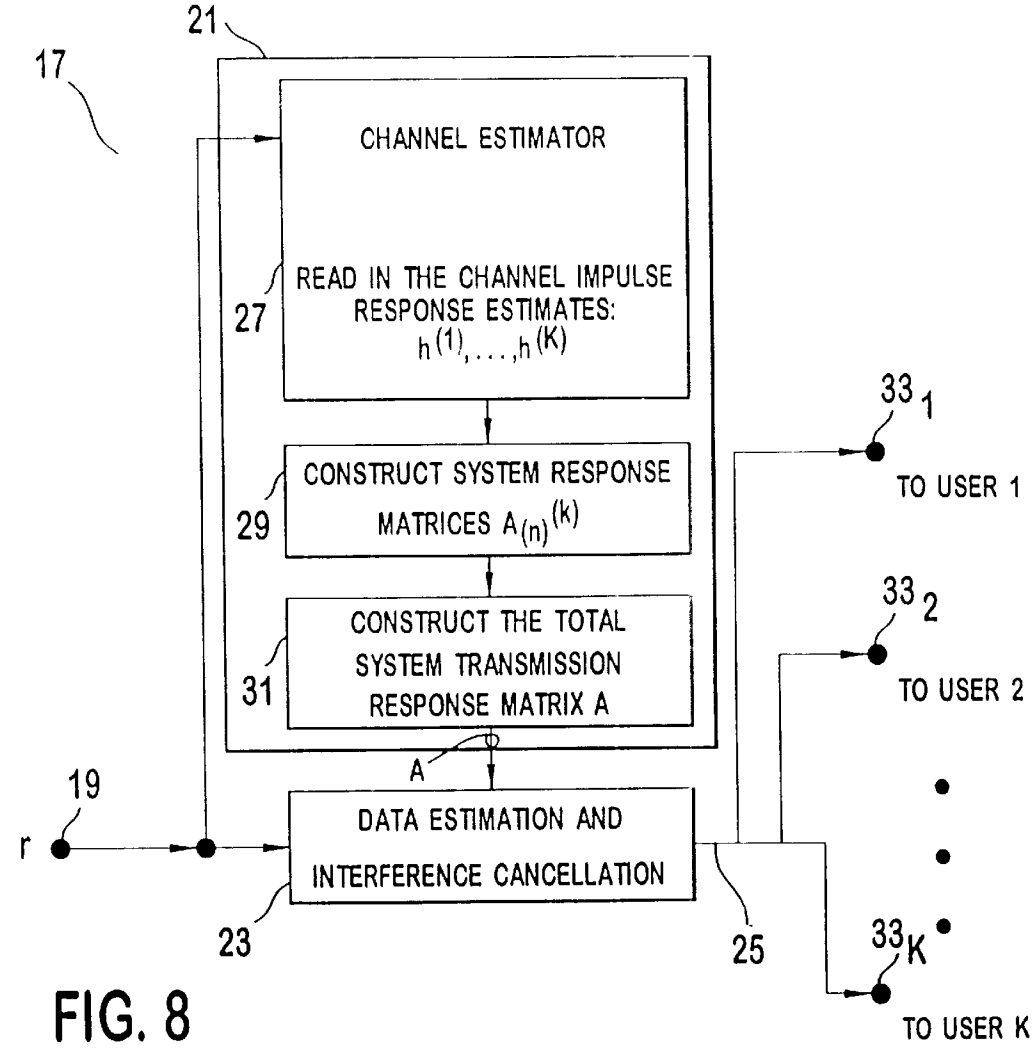


FIG. 8

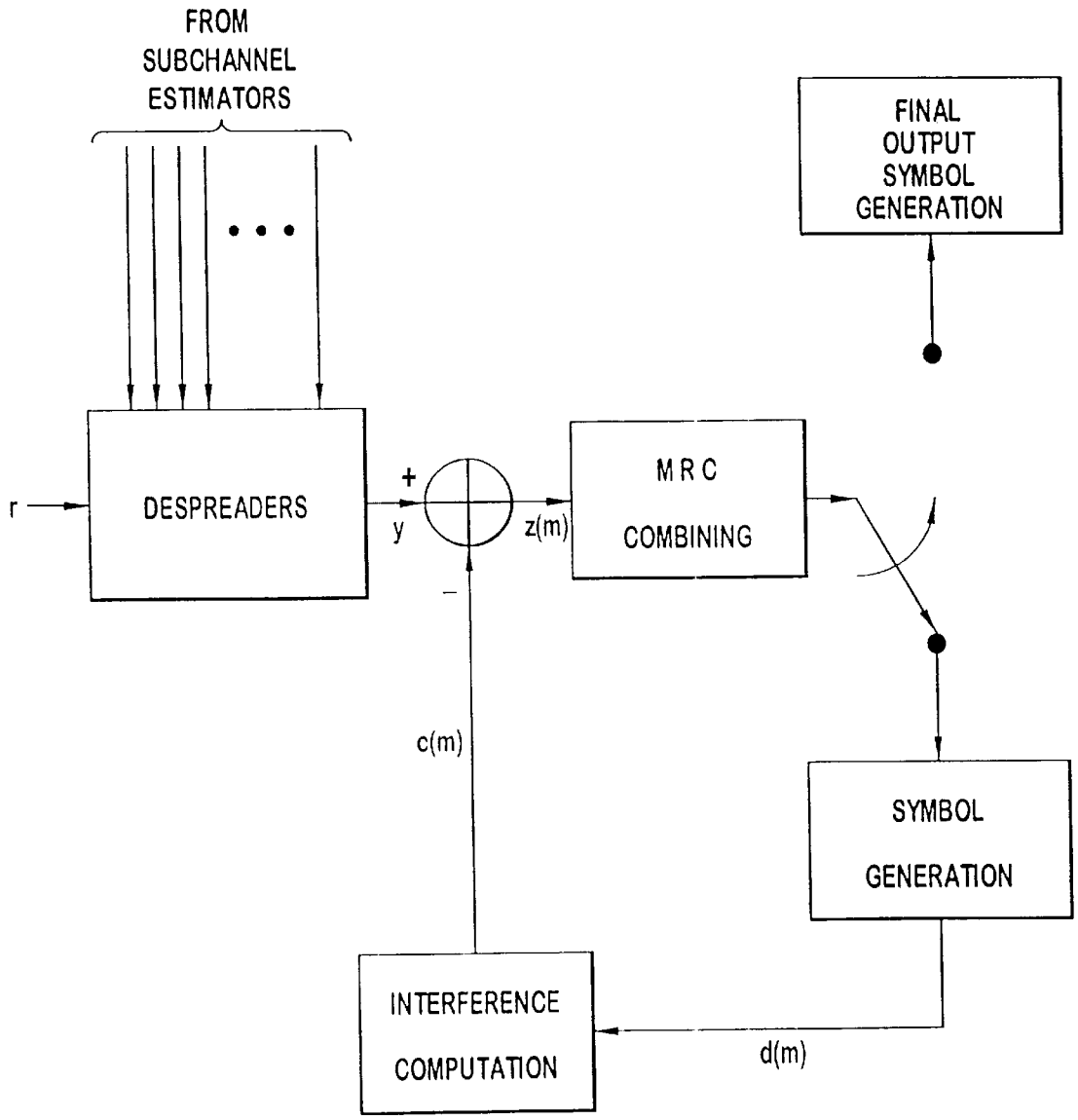
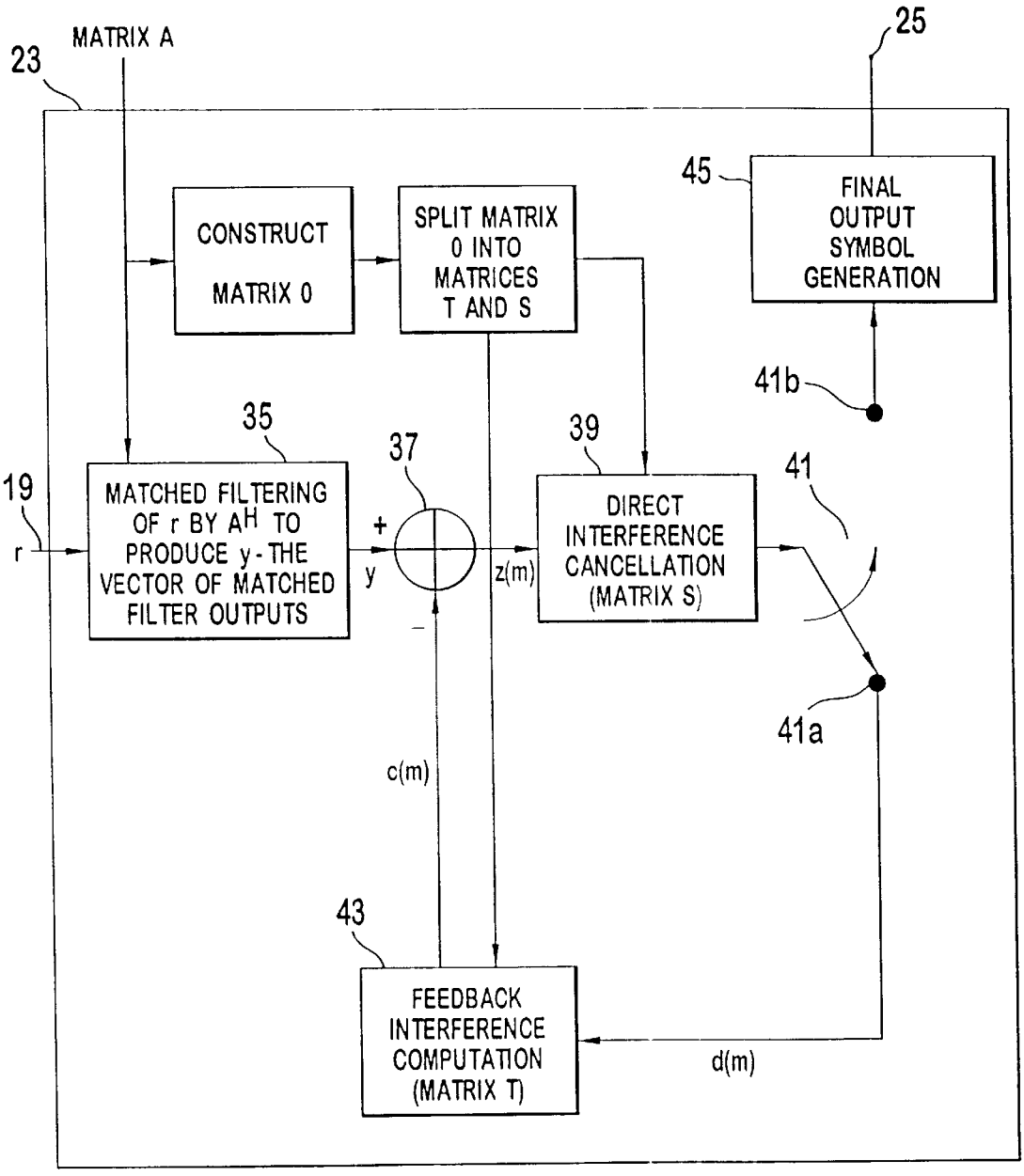


FIG. 7
PRIOR ART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25
45
FINAL OUTPUT SYMBOL GENERATION
CONSTRUCT MATRIX 0
SPLIT MATRIX 0 INTO MATRICES T AND S
41b
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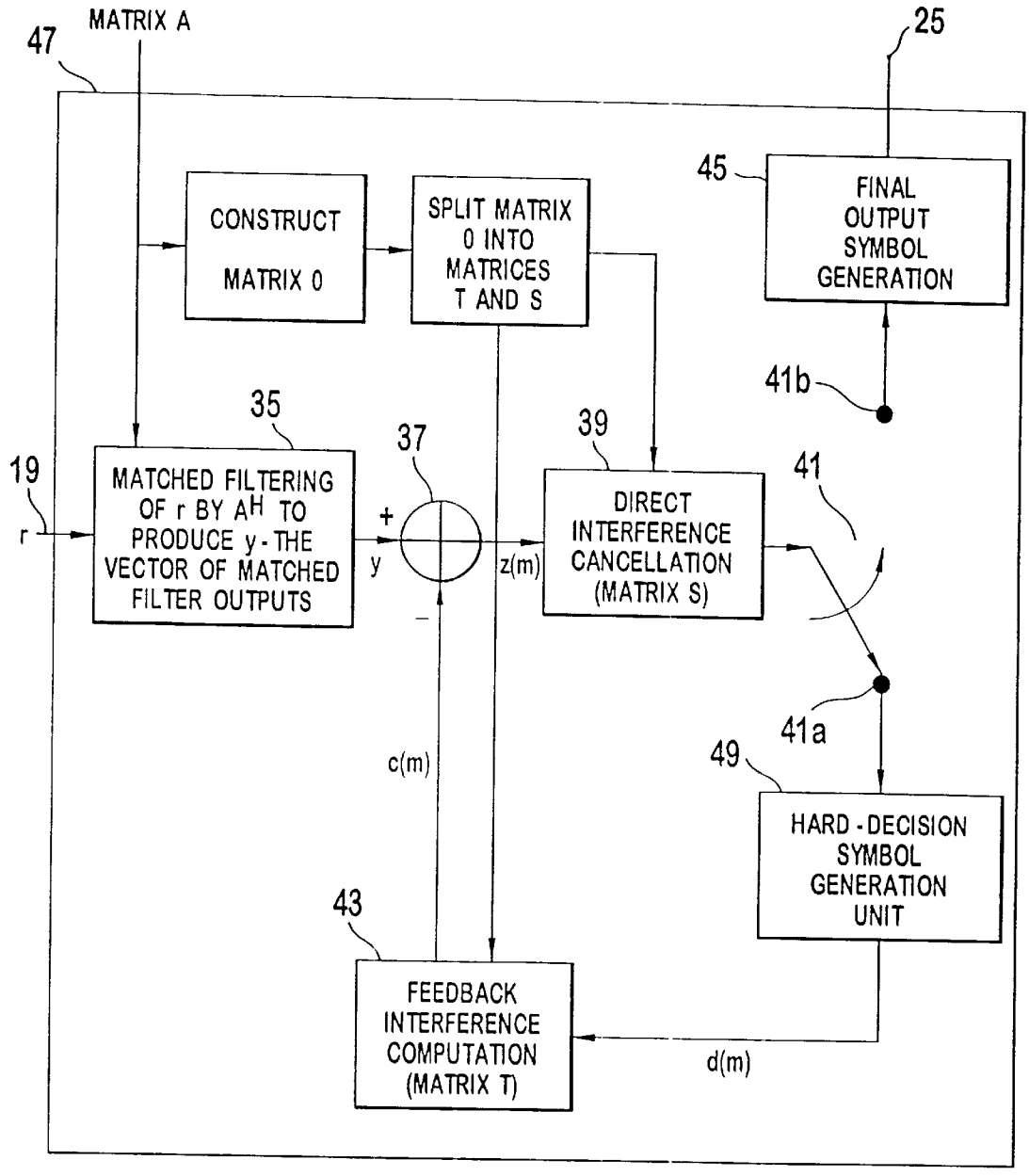
41
19
r
MATCHED FILTERING OF r BY A^H TO PRODUCE y - THE VECTOR OF MATCHED FILTER OUTPUTS
+
y
z(m)
DIRECT INTERFERENCE CANCELLATION (MATRIX S)
41a
c(m)
43
FEEDBACK INTERFERENCE COMPUTATION (MATRIX T)
d(m)

FIG. 9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MATCHED FILTERING OF r BY A^H TO PRODUCE y - THE VECTOR OF MATCHED FILTER OUTPUTS
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DIRECT INTERFERENCE CANCELLATION (MATRIX S)
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HARD - DECISION SYMBOL GENERATION UNIT
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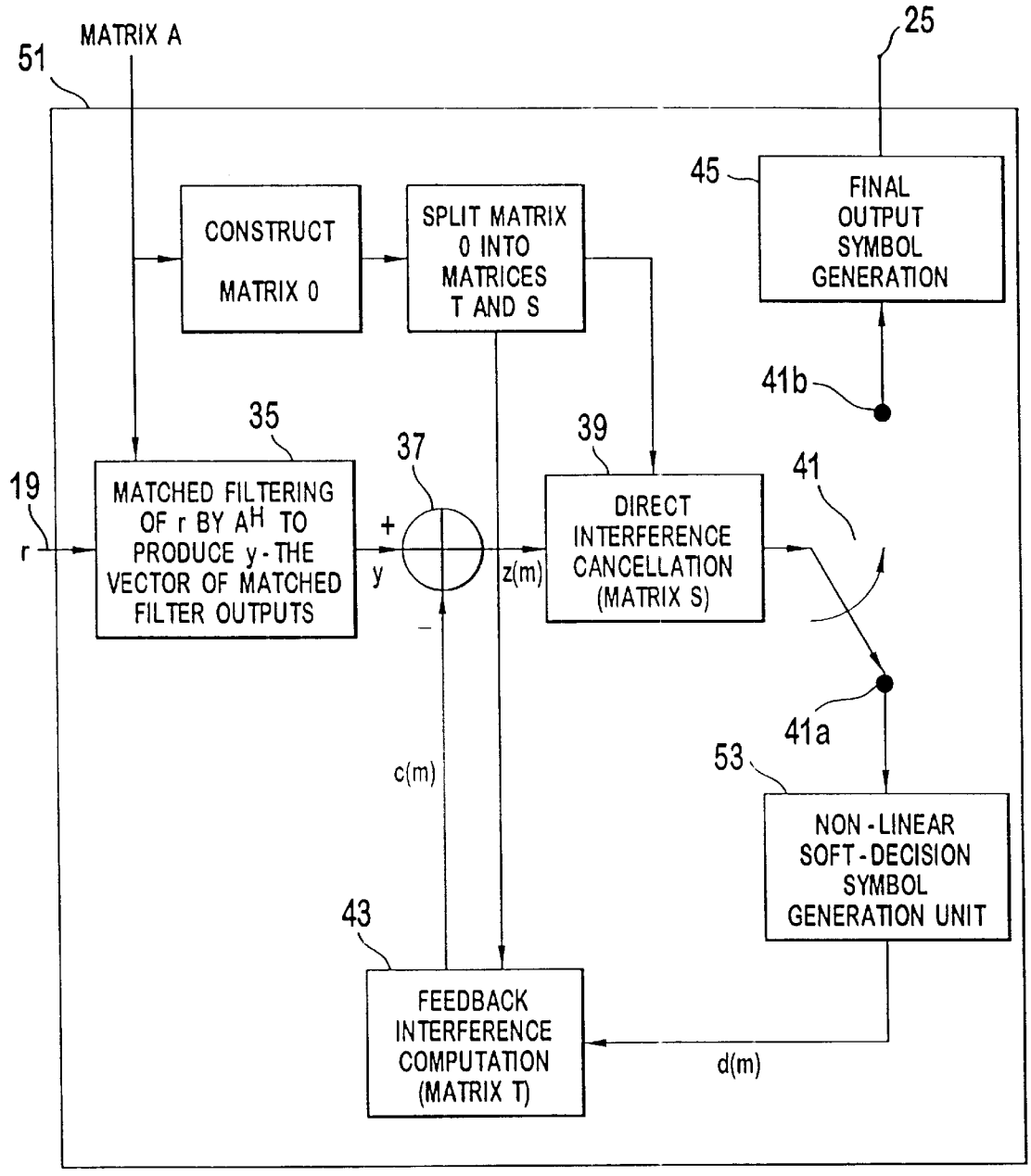
FEEDBACK INTERFERENCE COMPUTATION (MATRIX T)
d(m)

FIG. 10


MATRIX A
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CONSTRUCT MATRIX 0
SPLIT MATRIX 0 INTO MATRICES T AND S
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r
MATCHED FILTERING OF r BY A^H TO PRODUCE y - THE VECTOR OF MATCHED FILTER OUTPUTS
+
y
z(m)
DIRECT INTERFERENCE CANCELLATION (MATRIX S)
41a
53
c(m)
NON - LINEAR SOFT - DECISION SYMBOL GENERATION UNIT
43
FEEDBACK INTERFERENCE COMPUTATION (MATRIX T)
d(m)

FIG. 11

PARALLEL INTERFERENCE CANCELLATION RECEIVER FOR MULTIUSER DETECTION OF CDMA SIGNALS

This application is a continuation of PCT/US00/03537, filed Feb. 11, 2000, which claims priority from U.S. Provisional Application No. 60/160,259, filed Oct. 19, 1999.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to multiple access digital communication systems. More specifically, the invention relates to a parallel interference cancellation receiver system and method for the simultaneous reception of data from multiple users.

2. Description of the Related Art

A multiple-access communication system allows a plurality of users to access the same communication medium to transmit or receive information. The media may comprise, for example, a network cable in a local area network or lan, a copper wire in the classic telephone system, or an air interface for wireless communication.

A prior art multiple access communication system is shown in FIG. **1**. The communication media is referred to as a communication channel. Communication techniques such as frequency division multiple access or FDMA, time division multiple access or TDMA, carrier sense multiple access or CSMA, code division multiple access or CDMA and others allow access to the same communication medium for more than one user. These techniques can be mixed together creating hybrid varieties of multiple access schemes. For example, time division duplex or TDD mode of the proposed third generation W-CDMA standard is a combination of TDMA and CDMA.

An example CDMA prior art communication system is shown in FIG. **2**. CDMA is a communication technique in which data is transmitted with a broadened band (spread spectrum) by modulating the data to be transmitted with a pseudo-noise signal. The data signal to be transmitted may have a bandwidth of only a few thousand Hertz distributed over a frequency band that may be several million Hertz. The communication channel is being used simultaneously by K independent subchannels. For each subchannel, all other subchannels appear as interference.

As shown, a single subchannel of a given bandwidth is mixed with a unique spreading code which repeats a predetermined pattern generated by a wide bandwidth, pseudo-noise (pn) sequence generator. These unique user spreading codes are typically pseudo-orthogonal to one another such that the cross-correlation between the spreading codes is close to zero. A data signal is modulated with the pn sequence producing a digital spread spectrum signal. A carrier signal is then modulated with the digital spread spectrum signal and transmitted in dependence upon the transmission medium. A receiver demodulates the transmission extracting the digital spread spectrum signal. The transmitted data is reproduced after correlation with the matching pn sequence. When the spreading codes are orthogonal to one another, the received signal can be correlated with a particular user signal related to the particular spreading code such that only the desired user signal related to the particular spreading code is enhanced while the other signals for all other users are not enhanced.

Each value of the spreading code is known as a chip and has a chip rate that is the same or faster than the data rate. The ratio between the chip rate and the subchannel data rate is the spreading factor.

To extend the possible range of values of the data signal, a symbol is used to represent more than two binary values. Ternary and quaternary symbols take on three and four values respectively. The concept of a symbol allows for a greater degree of information since the bit content of each symbol dictates a unique pulse shape. Depending upon the number of symbols used, an equal number of unique pulse or wave shapes exist. The information at the source is converted into symbols which are modulated and transmitted through the subchannel for demodulation at the destination.

The spreading codes in a CDMA system are chosen to minimize interference between a desired subchannel and all other subchannels. Therefore, the standard approach to demodulating the desired subchannel has been to treat all other subchannels as interference, similar to interference that manifests itself in the communication medium. Receivers designed for this process are single-user, matched filter and RAKE receivers.

Since different subchannels do interfere with each other somewhat, another approach is to demodulate all subchannels at a receiver. The receiver can listen to all of the users transmitting at once by running a decoding algorithm for each of them in parallel. This ideology is known as multiuser detection. Multiuser detection can provide a significant performance improvement over single-user receivers.

Referring to FIG. **3**, a system block diagram of a prior art CDMA receiver using a multiuser detector is shown. As one skilled in this art realizes, the receiver may include such functions as radio frequency or rf down conversion and associated filtering for radio frequency channels, analog-to-digital conversion or optical signal demodulation for a specific communication media. The output of the receiver is a processed signal, either analog or digital, containing the combined spread signals of all active subchannels. The multiuser detector performs multiuser detection and outputs a plurality of signals corresponding to each active subchannel. All or a smaller number of the total number of subchannels may be processed.

Optimal multiuser detectors are computationally intensive devices performing numerous complex mathematic operations and are therefore difficult to implement economically. To minimize expense, suboptimal multiuser detectors such as linear detectors and parallel interference cancellation or PIC receivers have been developed requiring less computational complexity as a compromise approximating the performance of optimal detectors. Linear detectors include decorrelators, minimum mean square error or MMSE detectors, zero-forcing block linear equalizers or ZF-BLEs and the like. PIC receivers are usually designed as multistage iterative receivers and are soft-decision (SD) or hard-decision (HD) based.

A system block diagram of a prior art linear multiuser detector for synchronous or asynchronous CDMA communication is shown in FIG. **4**. Data output from the communication media specific receiver (as in FIG. **3**) is coupled to a subchannel estimator which estimates the impulse response of each symbol transmitted in a respective subchannel. The linear detector uses the impulse response estimates along with a subchannel's spreading code to demodulate each subchannel's data. The data is output to subchannel data processing blocks for respective users.

To effect parallel detection of K subchannel users in a physical system, linear multiuser detector methods are executed as fixed gate arrays, microprocessors, digital signal processors or DSPs and the like. Fixed logic systems allow for greater system speed while microprocessor driven systems offer programming flexibility. Either implementation that is responsible for the multiuser detection performs a sequence of mathematic operations. To describe the

functions, the following variables typically define the structure and operation of a linear multiuser detector:

K=the total number of users/transmitters that are active in the system.

N_c=the number of chips in a data block. The number of chips is required since with varying spreading factors this number is a measure common to all users. For the case of synchronous CDMA, a symbol from the user with the largest spreading factor may constitute a block of data. Therefore, N_c can be reduced to be equal to the largest spreading factor.

W=the communication channel impulse response length in chips. This is generally a predefined parameter of the system.

$Q^{(k)}$=the spreading factor of user k. The spreading factor is equal to the number of chips that are used to spread a symbol of user's data. A system knows the spreading factors in advance and does not need to estimate them from the received data.

$N_s^{(k)}$=the number of symbols sent by user k. $N_s^{(k)}=N_c/Q^{(k)}$.

$$N_s^T = \sum_{k=1}^{K} N_s^{(k)} = \text{the total number of symbols sent.}$$

$d^{(k)}$=the data (information) sent by user k. The data is presented in the form of a vector, where a vector is an array of data indexed by a single index variable. For the purposes of vector and matrix operations which follow, all vectors are defined as column vectors. The n^{th} element of $d^{(k)}$ is the n^{th} symbol transmitted by the k^{th} user.

$h^{(k)}$=the impulse response of the subchannel experienced by user k presented as a vector. This quantity needs to be estimated at the receiver. The receiver's estimates of the subchannel impulse responses are referred to as $h^{(k)}$. The elements of the vector $h^{(k)}$ are typically complex numbers, which model both amplitude and phase variations that can be introduced by the subchannel.

$v^{(k)}$=the spreading code of user k, presented as a vector. For the purposes of linear multiuser detection, it is useful to think of vectors containing the section of the spreading code which spreads a particular symbol. Therefore, the vector $v^{(k,n)}$ is defined as the spreading code which is used to spread the n^{th} symbol sent by the k^{th} user. Mathematically, it is defined as: $v_i^{(k,n)}=v_i^{(k)}$ for $(n-1)Q^{(k)}+1 \leqq i \leqq nQ^{(k)}$ and 0 for all other i, where i is the index of vector elements.

$r^{(k)}$=a vector which represents user k's data, spread by the spreading sequence $v^{(k)}$ and transmitted through that user's subchannel $h^{(k)}$. The vector $r^{(k)}$ represents channel observations performed during the period of time when a block of data arrives. The i^{th} element of the vector $r^{(k)}$ can be defined as:

$$r_i^{(k)} = \sum_{n=1}^{N_s^{(k)}} d_n^{(k)} \sum_{j=1}^{W} h_j^{(k)} v_{i-j+1}^{(k,n)}. \qquad \text{Equation 1}$$

The signal received at the receiver includes all user signals $r^{(k)}$ plus noise. Therefore, we can define the received data vector r as follows:

$$r = \sum_{k=1}^{K} r^{(k)} + n. \qquad \text{Equation 2}$$

The vector n in Equation 2 represents noise introduced by the communication channel.

FIG. **5** shows a system and method of a prior art linear multiuser detector. The estimated subchannel impulse response vectors $h^{(k)}$ and the spreading codes $v^{(k)}$ are used to create a system transmission response matrix for each user k. A matrix is a block of numbers indexed by two indexing variables. The matrix is arranged in a rectangular grid, with the first indexing variable being a row index and the second indexing variable being a column index.

A system transmission response matrix for user k is typically denoted as $A^{(k)}$. The i^{th}-row, n^{th}-column element is denoted as $A_{i,n}^{(k)}$ and is defined as:

$$A_{i,n}^{(k)} = \sum_{j=1}^{W} h_j^{(k)} v_{i-j+1}^{(k,n)}. \qquad \text{Equation 3}$$

Each column of the matrix $A^{(k)}$ corresponds to a matched filter response for a particular symbol sent by user k during the period of interest. Referring back to FIG. **5**, the received data r is matched to a combination of all user's spreading codes and subchannel impulse responses. Therefore, $A^{(k)}$ contains $N_s^{(k)}$ matched filter responses. The columns of $A^{(k)}$ are of the form

$$A_n^{(k)} = \begin{bmatrix} 0 \\ \vdots \\ 0 \\ b_n^{(k)} \\ 0 \\ \vdots \\ 0 \end{bmatrix} \qquad \text{Equation 4}$$

where each vector $b_n^{(k)}$ has a dimension of

$$Q^{(k)}+W-1, \qquad \text{Equation 5}$$

and is offset from the top of the matrix $A_n^{(k)}$ by

$$Q^{(k)}(n-1). \qquad \text{Equation 6}$$

Since the spreading codes are not periodic over symbol times; $b_i^{(k)} \neq b_j^{(k)}$ for $i \neq j$. The elements of a vector which may be non-zero values are referred to as the support of the vector. Therefore, $b_n^{(k)}$ is the support of $A_n^{(k)}$.

Once a system transmission matrix for each user is created, a total system transmission response matrix, denoted as A is created by concatenating the system transmission matrices for all the users as shown below:

$$A=[A^{(1)}, \ldots, A^{(k)}, \ldots, A^{(K)}]. \qquad \text{Equation 7}$$

In accordance with prior art modulation techniques, the elements of $h^{(k)}$ can be complex numbers. It then follows that the non-zero elements of A can be complex numbers.

An example total system transmission response matrix A for a prior art multiuser detector assembled in accordance with Equations 4, 5, 6 and 7 is

$$A = \left[\begin{array}{cccccccc|cccc} b_{1,1}^{(1)} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & b_{1,1}^{(2)} & 0 & 0 & 0 \\ b_{1,2}^{(1)} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & b_{1,2}^{(2)} & 0 & 0 & 0 \\ b_{1,3}^{(1)} & b_{2,1}^{(1)} & 0 & 0 & 0 & 0 & 0 & 0 & b_{1,3}^{(2)} & 0 & 0 & 0 \\ b_{1,4}^{(1)} & b_{2,2}^{(1)} & 0 & 0 & 0 & 0 & 0 & 0 & b_{1,4}^{(2)} & 0 & 0 & 0 \\ b_{1,5}^{(1)} & b_{2,3}^{(1)} & b_{3,1}^{(1)} & 0 & 0 & 0 & 0 & 0 & b_{1,5}^{(2)} & b_{2,1}^{(2)} & 0 & 0 \\ 0 & b_{2,4}^{(1)} & b_{3,2}^{(1)} & 0 & 0 & 0 & 0 & 0 & b_{1,6}^{(2)} & b_{2,2}^{(2)} & 0 & 0 \\ 0 & b_{2,5}^{(1)} & b_{3,3}^{(1)} & b_{4,1}^{(1)} & 0 & 0 & 0 & 0 & b_{1,7}^{(2)} & b_{2,3}^{(2)} & 0 & 0 \\ 0 & 0 & b_{3,4}^{(1)} & b_{4,2}^{(1)} & 0 & 0 & 0 & 0 & 0 & b_{2,4}^{(2)} & 0 & 0 \\ 0 & 0 & b_{3,5}^{(1)} & b_{4,3}^{(1)} & b_{5,1}^{(1)} & 0 & 0 & 0 & 0 & b_{2,5}^{(2)} & b_{3,1}^{(2)} & 0 \\ 0 & 0 & 0 & b_{4,4}^{(1)} & b_{5,2}^{(1)} & 0 & 0 & 0 & 0 & b_{2,6}^{(2)} & b_{3,2}^{(2)} & 0 \\ 0 & 0 & 0 & b_{4,5}^{(1)} & b_{5,3}^{(1)} & b_{6,1}^{(1)} & 0 & 0 & 0 & b_{2,7}^{(2)} & b_{3,3}^{(2)} & 0 \\ 0 & 0 & 0 & 0 & b_{5,4}^{(1)} & b_{6,2}^{(1)} & 0 & 0 & 0 & 0 & b_{3,4}^{(2)} & 0 \\ 0 & 0 & 0 & 0 & b_{5,5}^{(1)} & b_{6,3}^{(1)} & b_{7,1}^{(1)} & 0 & 0 & 0 & b_{3,5}^{(2)} & b_{4,1}^{(2)} \\ 0 & 0 & 0 & 0 & 0 & b_{6,4}^{(1)} & b_{7,2}^{(1)} & 0 & 0 & 0 & b_{3,6}^{(2)} & b_{4,2}^{(2)} \\ 0 & 0 & 0 & 0 & 0 & b_{6,5}^{(1)} & b_{7,3}^{(1)} & b_{8,1}^{(1)} & 0 & 0 & b_{3,7}^{(2)} & b_{4,3}^{(2)} \\ 0 & 0 & 0 & 0 & 0 & 0 & b_{7,4}^{(1)} & b_{8,2}^{(1)} & 0 & 0 & 0 & b_{4,4}^{(2)} \\ 0 & 0 & 0 & 0 & 0 & 0 & b_{7,5}^{(1)} & b_{8,3}^{(1)} & 0 & 0 & 0 & b_{4,5}^{(2)} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & b_{8,4}^{(1)} & 0 & 0 & 0 & b_{4,6}^{(2)} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & b_{8,5}^{(1)} & 0 & 0 & 0 & b_{4,7}^{(2)} \end{array}\right] \quad \begin{array}{l} A^{(1)} \\ A^{(2)} \end{array}$$

Equation 8

for two users (k=2), having sixteen chips in a data block (N_c=16), a channel impulse response length of four (W=4) and a spreading factor for the first user of two ($Q^{(1)}$=2) and a spreading factor for the second user of four ($Q^{(2)}$=4). In the resultant total system transmission response matrix A, $b_{n,i}^{(k)}$ denotes the i^{th} element of the combined system and channel response for the n^{th} symbol of the k^{th} user.

The received data r is processed using the total system transmission response matrix A which represents a bank of matched filter responses to create a vector of matched-filter outputs which is denoted as y. The matched filtering operation is defined as

$$y = A^H r. \qquad \text{Equation 9}$$

The matrix A^H represents the Hermitian (or complex) transpose of the matrix A. The Hermitian transpose is defined as $A_{ij}^H = \overline{A}_{ji}$ where the over-bar denotes the operation of taking a conjugate of a complex number. The matched filter outputs are then multiplied by the inverse of an objective matrix O. The objective matrix O represents the processing which differentiates each type of linear receiver. It is derived from the system transmission matrix A.

The zero-forcing block linear equalizer (ZF-BLE) receiver is a linear receiver with an objective matrix specified as $O=A^HA$. The minimum mean square error block linear equalizer (MMSE-BLE) receiver is a linear receiver with an objective matrix specified as $O=A^HA+\sigma^2I$ where σ^2 is the variance of the noise present on each of the symbols of the received data vector r and the matrix I is known as an identity matrix. An identity matrix is square and symmetric with 1's on its main diagonal and zeros everywhere else. The size of the identity matrix is chosen so as to make the addition operation valid according to the rules of linear algebra.

For a decorrelator (decorrelating receiver), matrix A is simplified by ignoring the channel responses $h^{(k)}$, considering only the spreading codes and their cross-correlation (interference) properties. A cross-correlation matrix, commonly referred to as R, is generally constructed for decorrelator type receivers. This matrix can be constructed by assuming that W=1 and $h_i^{(k)}$=1 in the definition of A above (i.e. the channel response of every subchannel is an impulse). Then the cross correlation matrix R is the objective matrix O as defined for the ZF-BLE receiver. A decorrelator often serves as a sub-process of a more complex multiuser detection receiver. Once the objective matrix is created, the multiuser detector will invert the matrix, denoted as O^{-1}.

The inverse of the objective matrix is then multiplied by the matched filter output vector y to produce estimates of the data vector d where $d(estimate)=O^{-1}y$. The inversion of the objective matrix O is a complex, computationally intensive process. The number of operations required to perform this process increases as the cube of the size of the matrix O. For most asynchronous CDMA receivers, the size of O is very large which makes the process of inversion impracticable. Techniques using linear algebra reduce the complexity of taking the inverse of the objective matrix. However, these techniques may be impracticable for some applications.

Unlike linear receivers, PIC receivers do not invert the objective matrix O. Therefore, PIC receivers offer an alternative that is less complex than linear multiuser detectors. FIG. **6** shows a typical prior-art PIC receiver. The received data vector r is input to a plurality of channel estimators which independently estimate each user's subchannel impulse response. The subchannel impulse responses are output to a data estimation and interference cancellation processor which estimates the received data for all users in parallel. The estimated received data is output to subchannel data processing blocks for further processing.

Shown in FIG. **7** is the prior art data estimation and interference cancellation process used in PIC receivers. The PIC receiver presumes that each subchannel consists of L distinct signal paths from a given user's transmitter to a receiver due to the transmission media. For each path L, the relative delays, amplitudes and phases are estimated at the

receiver by the subchannel estimation processors shown in FIG. **6**. For each of the L distinct paths of each user K present in the system, the PIC receiver allocates a despreader matched to the specific code of a respective user and the specific time delay of each path. Therefore, a total of KL despreaders are allocated in the despreader bank. Each despreader produces estimates of the received data from its respective user. The L data estimates for different paths of the same user's subchannel are combined to produce a complete data estimate of the transmitted user's data. As shown in FIG. **7**, the common prior art combining method is maximal ratio combining or MRC. Other combining methodologies exist in the prior art and can be used. The combined data estimates are output to a symbol generation processor which generates estimated symbol information which is output to the interference cancellation processor.

The spreading codes for each user K and the relative delays between the KL paths are known by the interference cancellation processor. The information is used to produce estimates of the interference that each user's received path (i.e., 1, 2, 3 . . . L) contributes to another user's L signal paths and to the signals received on L−1 signal paths of the same user. The interference estimates are subtracted from the despreader outputs which are again passed to the combining processor to produce revised data estimates. The revised data estimates are again used to generate revised interference estimates which are used to produce another set of revised data estimates. In theory, the process can be repeated indefinitely. However, in practice, the process terminates after two or three iterations.

The distinction between an SD-PIC and an HD-PIC lies in the symbol generation process. For the SD-PIC, the symbol generation process generates confidence information about the decisions made on the received symbols, for the HD-PIC, the symbol generation circuit does not generate confidence information for the received symbols. The difference refers only to the internal processing of the data estimation unit of the receiver. Both types of PIC receivers are capable of producing soft and hard decision symbol estimates for further processing by the dedicated subchannel data processors shown in FIG. **6**. This is shown in FIG. **7** by placing a final output data symbol generator for generating the final receiver output and may be different from the internal data symbol generation circuit.

An inherent problem with prior art PIC receivers resides in the received signal model that is used. Prior art PIC receivers assume that each subchannel consists of L discrete paths that the transmitted signal undergoes in the transmission media. The separation of the despreading and channel matching (performed by the combining processor) operations is the result of this assumption. However, a receiver constructed with this assumption can only correct for interference resulting from non-orthogonalities in the spreading sequences, more commonly known as multiple access interference or MAI. It cannot correct for interferences between one user's various symbols due to the time spreading of these symbols during transmission in the communication channel. This form of signal corruption is more commonly known as inter-symbol interference or ISI. ISI contributes to a phenomenon referred to as "the fat finger effect."

The fat finger effect occurs when two paths from the same user have such a small relative time delay that the delay cannot be resolved by the receiver as two distinct paths. The receiver fails to estimate the data from either of the two paths thereby affecting all users resulting in poor receiver performance.

Since all prior art PIC receivers use the simplifying assumption of L paths to separate the despreading and the channel combining operations, a PIC receiver using the accurate received signal model of a linear multiuser detector is desired.

SUMMARY OF THE INVENTION

A parallel interference cancellation receiver system and method is presented that reduces impulse response interference using a model of the received signal similar to that used in block linear equalizers. Block linear equalizers comprise decorrelating receivers, zero-forcing receivers, minimum mean square error receivers and the like. The invention comprises an interference computation processor feedback loop for correcting the output of a direct interference canceller. The m iterative process removes interferers from the output symbols of a matched-filter. The PIC receiver uses received signal models of the various block linear equalizers that do not assume that each subchannel consists of several distinct paths. The receiver estimates the impulse response characteristic of each subchannel as a whole.

Accordingly, it is an object of the present invention to provide a system and method of receiving and decoding a plurality of signals over a CDMA interface.

It is another object of the present invention to provide a PIC receiver system and method having greater accuracy with less required computations.

Other objects and advantages of the system and method will become apparent to those skilled in the art after reading a detailed description of the preferred embodiment.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a simplified block diagram of a prior art multiple access communication system.

FIG. **2** is a simplified block diagram of a prior art CDMA communication system.

FIG. **3** is a simplified block diagram of a prior art CDMA receiver with multiuser detection.

FIG. **4** is a simplified block diagram of a prior art multiuser detector.

FIG. **5** is a block diagram of a prior art linear multiuser detector.

FIG. **6** is a system block diagram of a prior art PIC receiver.

FIG. **7** is a system block diagram of a prior art PIC data estimation and interference cancellation processor.

FIG. **8** is a system block diagram of a PIC receiver of the present invention.

FIG. **9** is a system block diagram of a linear soft-decision PIC receiver of the present invention.

FIG. **10** is a system block diagram of a hard-decision PIC receiver of the present invention.

FIG. **11** is a system block diagram of a non-linear soft-decision PIC receiver of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The embodiments will be described with reference to the drawing figures where like numerals represent like elements throughout.

Shown in FIG. **8** is a parallel interference cancellation receiver **17** of the present invention for detecting, after reception, a plurality of users transmitting over a common CDMA channel. The receiver **17** comprises an input **19** for inputting data from all users k transmitted in a discreet block of time in the form of an input vector r containing the combined data from each user's subchannel, a channel estimation processor **21** for deriving individual impulse response estimates $h^{(k)}$ for each user and assembling a total system response matrix A, a data estimation and interference canceller **23** for generating interference free user data $d^{(k)}$ and an output **25** for outputting user data $d^{(k)}$ for each user k

from the received channel data r in the form of an output vector. The parallel interference canceller **17** comprises a plurality of processors having collateral memory which perform various vector and matrix operations. Alternate embodiments may implement the invention **17** using fixed gate arrays and DSPs performing the functions of the various processors. The total number of users K and the spreading factor $Q^{(k)}$ for each user (k=1, 2, 3 . . . K) are known a priori by a teaching transmission or by pre-loading into the PIC receiver **17**.

After demodulation, the received signal r is input **19** to the channel estimator processor **21** where individual k subchannel impulse response estimates are modeled **27** as vectors $h^{(k)}$ to correct inter-symbol interference or ISI caused by a subchannel's own symbols and MAI caused by symbols from other user's subchannels for all received data signals. The individual k subchannel impulse response estimates $h^{(k)}$ are input to a first memory **29** where it is combined with the same user's spreading code (Equation 3) creating a system transmission response estimate matrix $A_n^{(k)}$ for that user. Each system transmission response estimate matrix $A_n^{(k)}$ is output to a second memory **31** where a total system transmission response matrix A is assembled. The total system transmission response matrix A is comprised of all system transmission impulse response estimate matrices $A_n^{(k)}$ (Equation 7). The total system transmission response matrix A contains joint information about all of the subchannels in use by the active transmitters and contains information about any possible cross-channel and inter-symbol interference present in the received data signal r.

The total system transmission response matrix A is output to the data detection and interference canceller **23** which performs an estimation of transmitted data based on the received data vector r. The data detection processor **23** estimates subchannel data symbols and outputs a received data vector $d^{(k)}$to per-subchannel processing units $\mathbf{33}_1$, $\mathbf{33}_2$, $\mathbf{33}_3$, . . . $\mathbf{33}_K$ such as interleavers, Viterbi decoders, and the like.

The data estimation and interference canceller **23** is shown in FIG. **9**. The data detection processor **23** is comprised of a matched-filter **35** which match-filters the input **19** data vector r producing a vector of matched-filter outputs y, an adder **37** for removing feedback interference c from the matched-filter **35** outputy, a direct interference canceller **38** for deriving estimates of the user data $d^{(k)}$, an iteration counter/switch **41**, a feedback interference processor **43** and a symbol generator **45** for assembling symbols from the estimated user data $d^{(k)}$.

To obtain user data $d^{(k)}$ for a specific user from the combined user data r, the user data r must be filtered using a matched-filter **35** or the like. One knowledgeable in this art recognizes that a matched-filter **35** requires a response characteristic whose elements are complex conjugates of the combination of the spread pulse shape and the user's subchannel impulse response to produce an output with a level representative. of the signal prior to transmission. Signals r input **19** to the filter **35** which do not match with a given response characteristic produce a lower output.

The matched-filter **35** is similar to the matched-filtering operations performed by linear multiuser receivers. The matched-filter **35** operation is described by Equation 9 unlike the despreading operation of prior art parallel interference cancellation receivers. The input user data r is matched to the spreading code $v^{(k)}$ and the subchannel impulse response $h^{(k)}$ for each particular subchannel k. Each element of the matched-filter **35** output vector y is a first rough estimate of the corresponding symbol in the transmitted data vector d.

The total system transmission response matrix A provides the response characteristics to the matched-filter **35**. Each column of the system response matrix A is a vector which represents the response characteristics of a particular symbol. The received data vector r is input to the matched-filter **35** where it is matched with every response characteristic from the total system transmission response matrix A to produce the matched-filter output vector y. Each element of output vector y corresponds to a preliminary estimate of a particular symbol transmitted by a given user.

The matched-filter **35** output vector y is input to the direct interference canceller **39**. The direct interference canceller **39** performs a partial interference cancellation operation on the matched-filter **35** output vector y. The operation may be a scaling operation or a more complex operation. The partial interference canceled vector y is output as data symbol estimates d and is input to the feedback interference processor **43** through an iteration/counter switch **41***a*.

The feedback interference processor **43** uses the direct interference canceller **39** output estimates d to arrive at interference estimates output as a vector c that were not previously canceled by the direct interference canceller **39**. The interference estimates c are subtracted from the matched-filter **35** output vector y. The result z is the matched-filter **35** output vector y less the subtracted interference estimates c. The iterative interference subtraction process may be repeated m times depending upon the degree of desired signal correction. After m iterations, the interferers are removed from the matched-filter **35** output y and the iteration/counter switch **41** is thrown **41***b* outputting d for final output symbol generation **45**.

The operation of the direct interference canceller **39**/feedback interference processor **43** negative feedback control loop shown in FIG. **9** represents an m iteration receiver. For example, if m=2, the PIC receiver **17** has repeated the cancellation process twice. With c(m) as the interference vector output by the feedback interference processor **43** and d(m) as the symbol estimates vector output by the direct interference canceller **39**, for the m^{th} iteration,

$$\vec{d}(m)=S(\vec{y}-\vec{c}(m)) \text{ and} \qquad \text{Equation 10}$$

$$\vec{c}(m)=T\vec{d}(m-1) \qquad \text{Equation 11}$$

where the direct interference canceller **39** performs a multiplication of the matched filter output vector y by a matrix S and the feedback interference processor **43** performs a multiplication of the symbol estimates d by a matrix T. The initial condition of d(m) is 0. One skilled in this art recognizes that other initial conditions can be chosen without significantly affecting the operation of the system.

The output of the direct interference canceller **39** is the vector d(m) after the last iteration m. As in prior art parallel interference cancellation receivers, this output is processed by the final output symbol generator **45** which produces hard or soft-decision information on the output symbol estimates depending on the system requirements.

Depending upon the number of iterations m performed by the present invention **17**, the output of the data estimation and interference canceller d(m) can be written as

$$\vec{d}(m)=(ST+I)^{-1}S\vec{y}+(-1)^m(ST)^{m+1}(ST+I)^{-1}S\vec{y} \qquad \text{Equation 12}$$

where the steady-state response is,

$$\vec{d}_{ss}=(ST+I)^{-1}S\vec{y} \qquad \text{Equation 13}$$

and the transient response is,

$$\vec{d}_t(m)=(-1)^m(ST)^{m+1}(ST+I)^{-1}S\vec{y}. \qquad \text{Equation 14}$$

The PIC receiver **17** converges to the steady-state response if the transient response approaches zero as the

number of iterations increase. When this occurs, the receiver **17** converges to the steady-state response given in Equation 13 as explained in the technical paper by A. Reznik entitled, *A new class of PIC multiuser receivers and their relationship to ZF-BLE and MMSE-BLE multiuser receivers*, internal InterDigital Communications Corporation presentation, Oct. 19, 1999, the disclosure thereof incorporated by reference.

The steady-state response of prior art linear receivers such as ZF-BLE, MMSE-BLE and others and decorrelators is defined as

$$\vec{d}=O^{-1}\vec{y} \qquad \text{Equation 15}$$

where O is the objective matrix.

Referring back to Equations 13 and 15; if matrices S and T are selected such that $(ST+I)^{-1}S=O^{-1}$ and if the receiver **17** defined by Equations 10 and 11 converges, it will converge to the linear receiver defined by the objective matrix O. Linear algebra requires that in order to have $(ST+I)^{-1}S=O^{-1}$, matrices S, T, and O must satisfy the following identity:

$$O=T+S^{-1}. \qquad \text{Equation 16}$$

Rather than having to invert the objective matrix O, Equation 16 splits objective matrix O into two discrete matrices, T and S^{-1}. Matrix T defines the feedback interference processor **43**. Matrix S (the inverse of matrix S^{-1}) defines the direct interference canceller **39**. The present invention **17** replaces the inversion of matrix O with an inversion of another matrix (S^{-1}) and a series of matrix multiplications in the feedback loop.

An advantage of the present invention **17** lies in the fact that matrix S^{-1} requires significantly less complexity to invert than the original objective matrix O. For example, matrix S^{-1} may be a diagonal matrix (a matrix with non-zero entries only on the main diagonal). The inversion of a diagonal matrix only involves the inversion of each individual element lying on the main diagonal.

Furthermore, to improve the performance of the PIC **17**, the main diagonal of the matrix T should contain all zeros. This is shown and described in the above referenced article authored by A. Reznik.

Combining the two formulations of matrices T and S with Equation 16, a specific form for a general PIC receiver is created. Given a linear receiver with an objective matrix O, matrix S is defined as

$$S^{-1}=diag(O) \qquad \text{Equation 17}$$

where diag(X) defines a matrix where the main diagonal entries are equal to the main diagonal entries of X and all other elements of the matrix are equal to zero. Using Equation 16 and solving for matrix T yields

$$T=O-S^{-1}. \qquad \text{Equation 18}$$

Since the direct interference canceller **39** performs the multiplication of z(m) by matrix S (which is the inverse of diag(O)), the canceller **39** performs a scaling of each individual element of the vector z(m). The matrix multiplication of d(m) with matrix T performed in the feedback interference processor **43** computes the interference components. A receiver containing this architecture is referred to as a parallel interference cancellation receiver with full interference cancellation in the feedback or a PIC-fI receiver.

For a system that requires a zero-forcing mechanism, the receiver must converge to the ZF-BLE linear receiver. The ZF-PIC-fI of the present invention **17** uses the ZF-BLE objective matrix $O=A^HA$. Therefore, matrices S and T are defined as

$$S^{-1}=diag(A^HA) \text{ and} \qquad \text{Equation 19}$$

$$T=A^HA-diag(A^HA). \qquad \text{Equation 20}$$

For a system that requires a minimum mean square error reception mechanism, the receiver must converge to the MMSE-BLE linear receiver. The MMSE-PIC-fI receiver of the present invention **17** uses the MMSE-BLE objective matrix $O=A^HA+\sigma^2I$. Therefore, matrices S and T are defined as

$$S^{-1}=diag(A^HA)+\sigma^2I \text{ and} \qquad \text{Equation 21}$$

$$T=A^HA-diag(A^HA). \qquad \text{Equation 22}$$

For a system that requires a decorrelator receiver, total system response matrix A which is assembled in the channel estimator processor **21**, is assembled as a cross-correlation matrix ignoring the channel effects. The receiver structure is identical to the ZF-PIC-fI structure previously described, but uses the modified version of the A matrix.

As one skilled in this art realizes, other PIC receivers with full interference cancellation performed in the feedback loop (PIC-fI receivers) can be constructed using the system and method of the present invention **17** in conjunction with all existing linear receiver models. The two linear receiver models, ZF-BLE and MMSE, have been shown as exemplary embodiments. Using the method of the present invention **17**, a linear receiver is first chosen determining convergence.

An alternative embodiment of the present invention **17** which uses the same system architecture **23** delegates the cancellation of inter-symbol interference or ISI to the direct interference canceller **39**. The feedback interference processor **43** is used to cancel multi-access interference or MAI. This embodiment is referred to as a parallel interference canceller with direct ISI cancellation or PIC-dISI. As described in the referenced article by A. Reznik, this approach is more complex than the PIC-fI, but provides improved performance.

For a system that requires a zero-forcing mechanism, the receiver must converge to a ZF-BLE linear receiver. Using the system and method of the present invention **17**, the receiver is referred to as a ZF-PIC-dISI receiver with its S and T matrices defined as

$$S^{-1}=\begin{pmatrix} A^{(1)H}A^{(1)} & & & 0 \\ & \ddots & & \\ & & A^{(k)H}A^{(k)} & \\ & & & \ddots \\ 0 & & & A^{(K)H}A^{(K)} \end{pmatrix} \text{ and} \qquad \text{Equation 23}$$

$$T=A^HA-S^{-1}. \qquad \text{Equation 24}$$

For a system that requires a minimum mean square error reception mechanism, the receiver must converge to an MMSE-BLE linear receiver. Using the system and method of the present invention **17**, the receiver is referred to as an MMSE-PIC-dISI receiver with its S and T matrices defined as

$$S^{-1} = \begin{pmatrix} A^{(1)H}A^{(1)} & & 0 \\ & \ddots & \\ & A^{(k)H}A^{(k)} & \\ & & \ddots \\ 0 & & A^{(K)H}A^{(K)} \end{pmatrix} + \sigma^2 I \text{ and} \quad \text{Equation 25}$$

$$T = A^H A - S^{-1} + \sigma^2 I. \quad \text{Equation 26}$$

For a system that requires a decorrelator receiver, total system response matrix A which is assembled in the channel estimator processor **21**, is assembled as a cross-correlation matrix ignoring the channel effects. The receiver structure is identical to the ZF-PIC-dISI structure previously described, but uses the modified version of the A matrix.

Other PIC receivers with direct ISI cancellation can be constructed using the system and method of the present invention **17** in conjunction with all existing linear receiver models. Two linear receivers, the ZF-BLE and MMSE-BLE, have been shown embodied in the PIC-dISI receiver structure. As in the PIC-fI receivers, a linear receiver is first chosen determining convergence.

The receivers described above converge well when the levels of interference are low. Multiple access systems such as the frequency division duplex or FDD mode of the proposed UMTS 3^{rd} generation Wideband CDMA standard with accurate power control exhibits low interference levels. As previously described, the present invention **17** is not limited to the receivers described. Any choice of matrices S and T may provide a viable receiver structure. Given an objective matrix O, Equation 16 defines any number of receiver structures that converge to a linear receiver defined by the objective matrix O. The different choices of S and T imply a different choice for the complexity and performance of a desired receiver. Better receiver **17** performance is obtained when exploiting the performance of the direct interference canceller **39** as in the case of the PIC-dISI receivers. However, delegating more effort to the direct interference canceller **39** requires computing the inverse of a more complicated matrix, thereby increasing the complexity of the receiver. This is seen by setting the matrix T to 0. The result is the prior art linear receiver model which has to invert the objective matrix O.

The above describes linear soft-decision parallel interference cancellation receivers. Hard-decision parallel interference cancellation receivers **47** are obtained by adding a symbol generator into the feedback path making hard decisions **49** on the symbol estimates d(m) as shown in FIG. **10**. Non-linear soft-decision parallel interference cancellation receivers **51** can be obtained by replacing the hard symbol generator **49** with a non-linear soft-decision symbol generator **53** as shown in FIG. **11**.

While the present invention has been described in terms of the preferred embodiments, other variations which are within the scope of the invention as outlined in the claims below will be apparent to those skilled in the art.

What is claimed is:

1. An interference canceller for use in a receiver that separates received communication signals (r) from a plurality of transmitters over a CDMA interface into a plurality of desired signals ($d^{(k)}$), the interference canceller comprising:

a channel estimation processor for receiving the communication signals (r) producing individual impulse response estimates (A) for the plurality of desired signals ($d^{(k)}$), said impulse response estimates coupled to a data estimation and interference canceller, said channel estimation processor further comprises:

a channel estimator coupled to the communication signals (r) for outputting channel impulse response estimates ($h^{(k)}$) for the plurality of desired signals ($d^{(k)}$), said channel estimator coupled to a system response matrix assembler;

said system response matrix assembler outputting system response matrices ($A_{(n)}^{(k)}$) for the plurality of desired signals ($d^{(k)}$); and

said system response matrices ($A_{(n)}^{(k)}$) assembled into a total system response matrix (A) output; and

said data estimation and interference canceller receiving the communication signals (r) and said impulse response estimates (A) and outputting the plurality of desired signals ($d^{(k)}$), said data estimation and interference canceller further comprises:

a matched-filter coupled to the communication signals (r) and said channel estimation processor output (A) for outputting estimates of the desired signals with selective signals (y) to a first input of a summer;

said summer having an output (z(m)) coupled to a direct interference canceller;

said direct interference canceller outputting scaled estimates of the desired signals with selective signals (d(m)) of the plurality of desired signals ($d^{(k)}$) to an input of an iteration counter;

said iteration counter having a first output coupled to a feedback interference processor;

said feedback interference processor outputting interference estimates (c(m)) of the selective signals to a second input of said summer; and

said interference estimates (c(m)) subtracted from said matched-filter output (y) for m iterations by said iteration counter whereby said iteration counter outputs said estimates of the desired signals (d(m)) as the plurality of desired signals ($d^{(k)}$) absent said selective signals through a second output.

2. The interference canceller according to claim **1** wherein said direct interference canceller operation defined by an S matrix and said feedback interference processor operation defined by a T matrix related by

$$O = T + S^{-1}$$

where matrix O is an objective matrix that defines a receiver structure.

3. The interference canceller according to claim **2** wherein said matrix S defined as

$S = (diag(O))^{-1}$ and

said matrix T defined as

$$T = O - diag(O).$$

4. The interference canceller according to claim **2** wherein said objective matrix O as a zero-forcing block linear equalizer.

5. The interference canceller according to claim **3** wherein said objective matrix O as a minimum mean square error block linear equalizer.

6. The interference canceller according to claim **3** wherein said total system response matrix (A) as a decorellator and said objective matrix O as a zero-forcing block linear equalizer.

7. The interference canceller according to claim **2** wherein said matrix S defined such that said direct interference canceller performs cancellation of inter-symbol interference (ISI) of each selective signal and said matrix T defined such that said feedback interference processor computes multi-access interference (MAI) contributed to each selective signal by said desired signals ($d^{(k)}$).

8. The interference canceller according to claim 7 wherein said matrix S defined as

$$S=\begin{bmatrix} A^{(1)H}A^{(1)} & & & 0 \\ & \ddots & & \\ & & A^{(k)H}A^{(k)} & \\ & & & \ddots \\ 0 & & & A^{(K)H}A^{(K)} \end{bmatrix}^{-1} \text{ and}$$

said matrix T defined as

$$T=O-S^{-1}.$$

9. The interference canceller according to claim 8 wherein said objective matrix O as a zero-forcing block linear equalizer.

10. The interference canceller according to claim 8 wherein said total system response matrix (A) as a decorellator and said objective matrix O as a zero-forcing block linear equalizer.

11. The interference canceller according to claim 7 wherein said matrix S defined as

$$S=\left[\begin{bmatrix} A^{(1)H}A^{(1)} & & & 0 \\ & \ddots & & \\ & & A^{(k)H}A^{(k)} & \\ & & & \ddots \\ 0 & & & A^{(K)H}A^{(K)} \end{bmatrix}+\sigma^2 I\right]^{-1};$$

said matrix T defined as

$$T=A^HA-S^{-1}\sigma^2 I; \text{and}$$

said objective matrix O defined as a minimum mean square error block linear equalizer.

12. The interference canceller according to claim 2 wherein a hard decision symbol generator coupled between said first output of said iteration counter and said feedback interference processor input producing hard decisions on said desired signal estimates ($d^{(m)}$).

13. The interference canceller according to claim 12 wherein said matrix S defined as

$$S=(diag(O))^{-1} \text{ and}$$

said matrix T defined as

$$T=O-diag(O).$$

14. The interference canceller according to claim 13 wherein said objective matrix O as a zero-forcing block linear equalizer.

15. The interference canceller according to claim 13 wherein said objective matrix O as a minimum mean square error block linear equalizer.

16. The interference canceller according to claim 13 wherein said system response matrix (A) as a decorellator and said objective matrix O as a zero-forcing block linear equalizer.

17. The interference canceller according to claim 12 wherein said matrix S defined such that said direct interference canceller performs cancellation of inter-symbol interference (ISI) of each selective signal and said matrix T defined such that said feedback interference processor computes multi-access interference (MAI) contributed to each selective signal by said desired signals ($d^{(k)}$).

18. The interference canceller according to claim 17 wherein said matrix S defined as

$$S=\begin{bmatrix} A^{(1)H}A^{(1)} & & & 0 \\ & \ddots & & \\ & & A^{(k)H}A^{(k)} & \\ & & & \ddots \\ 0 & & & A^{(K)H}A^{(K)} \end{bmatrix}^{-1} \text{ and}$$

said matrix T defined as

$$T=A^HA-S^{-1}.$$

19. The interference canceller according to claim 18 wherein said objective matrix O as a zero-forcing block linear equalizer.

20. The interference canceller according to claim 18 wherein said total system response matrix (A) as a decorellator and said objective matrix O as a zero-forcing block linear equalizer.

21. The interference canceller according to claim 17 further wherein said matrix S defined as

$$S=\left[\begin{bmatrix} A^{(1)H}A^{(1)} & & & \\ & \ddots & & \\ & & A^{(k)H}A^{(k)} & \\ & & & \ddots \\ & & & A^{(K)H}A^{(K)} \end{bmatrix}+\sigma^2 I\right]^{-1};$$

said matrix T defined as

$$T=A^HA-S^{-1}\sigma^2 I; \text{ and}$$

said objective matrix O defined as a minimum mean square error block linear equalizer.

22. The interference canceller according to claim 2 wherein a non-linear soft decision symbol generator coupled between said first output of said iteration counter and said feedback interference processor input producing non-linear soft decisions on said desired signal estimates (d(m)).

23. The interference canceller according to claim 22 wherein said matrix S defined as

$$S=(diag(O))^{-1} \text{ and}$$

said matrix T defined as

$$T=O-diag(O).$$

24. The interference canceller according to claim 23 wherein said objective matrix O as a zero-forcing block linear equalizer.

25. The interference canceller according to claim 23 wherein said objective matrix O as a minimum mean square error block linear equalizer.

26. The interference canceller according to claim 23 wherein said total system response matrix (A) as a decorellator and said objective matrix O as a zero-forcing block linear equalizer.

27. The interference canceller according to claim 22 wherein said matrix S defined such that said direct interference canceller performs cancellation of inter-symbol interference (ISI) of each selective signal and said matrix T defined such that said feedback interference processor computes multi-access interference (MAI) contributed to each selective signal by said desired signals ($d^{(k)}$).

28. The interference canceller according to claim 27 wherein said matrix S defined as

$$S=\begin{bmatrix} A^{(1)H}A^{(1)} & & & 0 \\ & \ddots & & \\ & & A^{(k)H}A^{(k)} & \\ & & & \ddots \\ 0 & & & A^{(K)H}A^{(K)} \end{bmatrix}^{-1} \text{ and}$$

said matrix T defined as

$$T=A^{H}A-S^{-1}.$$

29. The interference canceller according to claim **28** wherein said objective matrix O as a zero-forcing block linear equalizer.

30. The interference canceller according to claim **28** wherein said total system response matrix (A) as a decorellator and said objective matrix O as a zero-forcing block linear equalizer.

31. The interference canceller according to claim **27**, wherein said matrix S defined as

$$S=\left[\begin{bmatrix} A^{(1)H}A^{(1)} & & & \\ & \ddots & & \\ & & A^{(k)H}A^{(k)} & \\ & & & \ddots \\ & & & A^{(K)H}A^{(K)} \end{bmatrix}+\sigma^{2}I\right]^{-1};$$

said matrix T defined as

$$T=A^{H}A-S^{-1}+\sigma^{2}I; \text{ and}$$

said objective matrix O defined as a minimum mean square error block linear equalizer.

32. A method for separating received signals (r) from a plurality of transmitters over a CDMA interface into a plurality of desired signals ($d^{(K)}$), comprising the steps of:

a) creating a total system response matrix (A) from impulse response estimates ($h^{(k)}$) from the received signals (r);

b) filtering the received signals (r) with said total system response matrix (A) producing estimates of the desired signals with selective signals (y);

c) choosing a receiver structure (O) to converge to;

d) deriving an S matrix from said receiver structure;

e) deriving a T matrix from said receiver structure;

f) scaling said filter output (y) as desired signal estimates (d(m)) by multiplying by said matrix S;

g) computing interference estimates (c(m)) by multiplying said scaled output (d(m)) by said matrix T;

h) subtracting (z(m)) said interference estimates (c(m)) from said filter output (y);

i) scaling said filter output minus said interference estimates (z(m)) as desired signal estimates (d(m)) by multiplying with said matrix S;

j) repeating steps g) through i) for m iterations; and

k) outputting said desired signal estimates (d(m)) as the plurality of desired signals ($d^{(k)}$) absent said selective signals.

33. The method according to claim **32** wherein said matrix S defined as

$$S=(diag(O))^{-1} \text{ and}$$

said matrix T defined as

$$T=O-diag(O).$$

34. The method according to claim **33** wherein step c) comprises choosing said receiver structure (O) as a zero-forcing block linear equalizer.

35. The method according to claim **23** wherein step c) comprises choosing said receiver structure (O) as a minimum mean square error block linear equalizer.

36. The method according to claim **33** wherein step a) comprises creating said total system response matrix A as a decorellator and step c) comprises choosing said receiver structure (O) as a zero-forcing block linear equalizer.

37. The method (17) according to claim **32** wherein defining said matrix S such that said scaling performs cancellation of inter-symbol interference (ISI) of each selective signal and defining said matrix T such that said computing interference estimates computes multi-access interference (MAI) contributed to each selective signal by said desired signals ($d^{(K)}$), respectively.

38. The method according to claim **37** wherein said matrix S defined as

$$S=\begin{bmatrix} A^{(1)H}A^{(1)} & & & 0 \\ & \ddots & & \\ & & A^{(k)H}A^{(k)} & \\ & & & \ddots \\ 0 & & & A^{(K)H}A^{(K)} \end{bmatrix}^{-1} \text{ and}$$

said matrix T defined as

$$T=O-S^{-1}.$$

39. The method according to claim **38** wherein step c) comprises choosing said receiver structure (O) as a zero-forcing block linear equalizer.

40. The method according to claim **38** wherein step c) comprises creating said total system response matrix (A) as a decorellator and step c) comprises choosing said receiver structure (O) as a zero-forcing block linear equalizer.

41. The method according to claim **37** wherein said matrix S is defined as

$$S=\left[\begin{bmatrix} A^{(1)H}A^{(1)} & & & \\ & \ddots & & \\ & & A^{(k)H}A^{(k)} & \\ & & & \ddots \\ & & & A^{(K)H}A^{(K)} \end{bmatrix}+\sigma^{2}I\right]^{-1};$$

said matrix T is defined as

$$T=A^{H}A-S^{-1}+\sigma^{2}I; \text{ and}$$

said receiver structure (O) as a minimum mean square error block linear equalizer.

42. The method according to claim **32** wherein step g) comprises producing hard decisions on said desired signal estimates (d(m)).

43. The method according to claim **42** wherein said matrix S defined as

ti $S=(diag(O))^{-1}$ and

said matrix T defined as

$$T=O-diag(O).$$

44. The method according to claim 43 wherein step c) comprises choosing said receiver structure (O) as a zero-forcing block linear equalizer.

45. The method according to claim 43 wherein step c) comprises choosing said receiver structure (O) as a minimum mean square error block linear equalizer.

46. The method according to claim 43 wherein step a) comprises creating said total system response matrix A as a decorellator and step c) comprises choosing said receiver structure (O) as a zero-forcing block linear equalizer.

47. The method according to claim 42 wherein further comprises defining said matrix S such that said scaling performs cancellation of inter-symbol interference (ISI) of each selective signal and defining said matrix T such that said computing interference estimates computes multi-access interference (MAI) contributed to each selective signal by said desired signals ($d^{(K)}$), respectively.

48. The method according to claim 47 wherein said matrix S is defined by

$$S=\begin{bmatrix} A^{(1)H}A^{(1)} & & & 0 \\ & \ddots & & \\ & & A^{(k)H}A^{(k)} & \\ & & & \ddots \\ 0 & & & A^{(K)H}A^{(K)} \end{bmatrix}^{-1} \text{ and}$$

said matrix T is defined by

$$T=O-^{-1}.$$

49. The method according to claim 48 wherein step c) comprises choosing receiver structure (O) as a zero-forcing block linear equalizer.

50. The method according to claim 48 wherein step c) comprises creating said total system response matrix (A) as a decorellator and step c) comprises choosing said receiver structure (O) as a zero-forcing block linear equalizer.

51. The method (17) according to claim 47 wherein said matrix S is defined by

$$S=\left[\begin{bmatrix} A^{(1)H}A^{(1)} & & & \\ & \ddots & & \\ & & A^{(k)H}A^{(k)} & \\ & & & \ddots \\ & & & A^{(K)H}A^{(K)} \end{bmatrix}+\sigma^2 I\right]^{-1};$$

said matrix T is defined by

$$T=A^{H}A-S^{-1}+\sigma^2 I; \text{ and}$$

said receiver structure (O) as a minimum mean square error block linear equalizer.

52. The method according to claim 32 wherein step g) is comprises producing non-linear soft decisions on said desired signal estimates (d(m)).

53. The method according to claim 52 wherein said matrix S defined as

$$S=(diag(O))^{-1} \text{ and}$$

said matrix T defined as

$$T=O-diag(O).$$

54. The method according to claim 53 wherein step c) comprises choosing said receiver structure (O) as a zero-forcing block linear equalizer.

55. The method according to claim 53 wherein step c) comprises choosing said receiver structure (O) as a minimum mean square error block linear equalizer.

56. The method according to claim 53 wherein step a) comprises creating said total system response matrix A as a decorellator and step c) comprises choosing said receiver structure (O) as a zero-forcing block linear equalizer.

57. The method according to claim 52 further comprising defining said matrix S such that said scaling performs cancellation of inter-symbol interference (ISI) of each selective signal and defining said matrix T such that said computing interference estimates computes multi-access interference (MAI) contributed to each selective signal by said desired signals ($d^{(K)}$), respectively.

58. The method according to claim 57 wherein said matrix S is defined by

$$S=\begin{bmatrix} A^{(1)H}A^{(1)} & & & 0 \\ & \ddots & & \\ & & A^{(k)H}A^{(k)} & \\ & & & \ddots \\ 0 & & & A^{(K)H}A^{(K)} \end{bmatrix}^{-1} \text{ and}$$

said matrix T is defined by

$$T=O-S^{-1}.$$

59. The method according to claim 58 wherein step c) comprises choosing said receiver structure (O) as a zero-forcing block linear equalizer.

60. The method according to claim 58, wherein step a) comprises creating said total system response matrix (A) as a decorellator and step c) comprises choosing said receiver structure (O) as a zero-forcing block linear equalize.

61. The method according to claim 57 wherein said matrix S is defined by

$$S=\left[\begin{bmatrix} A^{(1)H}A^{(1)} & & & \\ & \ddots & & \\ & & A^{(k)H}A^{(k)} & \\ & & & \ddots \\ & & & A^{(K)H}A^{(K)} \end{bmatrix}+\sigma^2 I\right]^{-1};$$

said matrix T is defined by

$$T=A^{H}A-S^{-1}\sigma^2 I; \text{ and}$$

said receiver structure (O) as a minimum mean square error block linear equalizer.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,724,809 B2
DATED : April 20, 2004
INVENTOR(S) : Alexander Reznik

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 3,
Lines 23-24, after "k.", insert a line break such that the equation "$N_s^{(k)} = N_c / Q^{(k)}$" appears all on the same line.

Column 9,
Line 42, after the word "filter", delete "outputy" and insert therefor -- output y --.
Line 54, after ther word "representative", delete ".".

Column 14,
Line 52, after the word "claim", delete "2" and insert therefor -- 3 --.

Column 15,
Line 34, delete "$T = A^H A - S^{-1}\sigma^2 I$" and insert therefor -- $T = A^H A - S^{-1} + \sigma^2 I$ --.
Line 42, after the word "estimates", delete "$(d^{(m)})$" and insert therefor -- (d(m)) --.
Line 56, after the word "said", insert -- total --.

Column 16,
Line 33, delete "$T = A^H A - S^{-1}\sigma^2 I$" and insert therefor -- $T = A^H A - S^{-1} + \sigma^2 I$ --.

Column 18,
Line 7, after the word "claim", delete "23" and insert therefor -- 33 --.
Line 63, delete "ti".

Column 19,
Line 29, delete "$T = O -^{-1}$" and insert therefor -- $T = O - S^{-1}$ --.
Line 53, after the word "g)", delete "is".

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

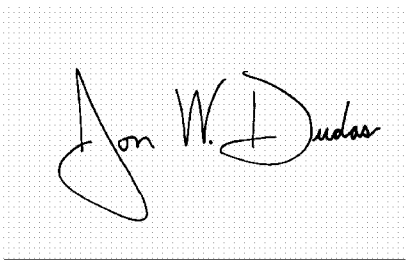
PATENT NO. : 6,724,809 B2
DATED : April 20, 2004
INVENTOR(S) : Alexander Reznik

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 20,
Line 41, after the word "linear", delete "equalize" and insert therefor -- equalizer --
Line 54, delete "$T = A^H A - S^{-1} \sigma^2 I$" and insert therefor -- $T = A^H A - S^{-1} + \sigma^2 I$ --.

Signed and Sealed this

Fifth Day of July, 2005



JON W. DUDAS
Director of the United States Patent and Trademark Office