A High-Efficiency Linear RF Power Amplifier With a Power-Tracking Dynamically Adaptive Buck-Boost Supply

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***Abstract*—Energy efficiency of RF transceivers is critical and paramount for longer battery life in portable devices, which is improved by operating the power amplifiers (PAs) with higher efficiency. In this paper, the applicability of dynamic-converter-supplied RF PAs' efficiency-enhancement schemes is compared and evaluated for code-division multiple-access (CDMA) applications. The tradeoffs involved in designing switching converters with wide bandwidth (BW) and high efficiency over wide loading conditions are considered. Given the highly variable nature of the batteries (e.g., 2.7–4.2 V for Li ion), to operate the systems at their peak performance levels, even when the battery is close to fully discharged, and to achieve higher average efficiency, a power-tracking dynamically adaptive noninverting buck-boost converter-supplied PA topology is proposed. To demonstrate the validity of the scheme, a prototype system was designed and tested using a 915-MHz carrier frequency with a 1.25-MHz baseband BW CDMA signal. The supply voltage for the PA (operating in a class-A/class-AB configuration) is adjusted dynamically from 0.5 to 3.6 V, depending on the input RF power from a 3.0-V input supply, which can vary from 2.4 to 3.4 V. The dynamic-supply PA meets the adjacent-channel power-ratio requirements of CDMA IS-95 specifications, and the overall error vector magnitude remains less than 6% throughout its output power range from −50 to 27 dBm. The weighted average efficiency of the dynamically adaptive system (6.78%) is 4.43 times compared to the fixed supply PA efficiency (1.53%), which translates to a *88% increase in battery life*, assuming that the PA consumes 20% of the total transceiver power.**

***Index Terms*—Battery life, buck-boost dc–dc converter, code-division multiple-access (CDMA) portable applications, dynamic supplies.**

I. Introduction

WITH THE explosive growth of RF portable devices and their increasing functional densities (e.g., voice, video, and data), efficient power-saving techniques are intrinsic in prolonging battery lifetime. Consequently, energy-efficient RF power amplifiers (PAs) are key components in mobile battery-operated systems [e.g., cellular phones, personal digital assistants (PDAs)] because they determine and dominate the total power consumption of their respective systems [1]. In spite of the introduction of a wide variety of efficient PAs (e.g., class B, class C, class D, class E, and class F), performance is often nonlinear, resulting in considerable out-of-band radiation and interference in adjacent channels. The amplification of nonconstant envelope RF modulation, such as offset quadrature phase-shift keying (OQPSK) used in code-division multiple-access (CDMA) mobile handsets, requires linear PAs to satisfy the adjacent-channel power ratio (ACPR) requirements. To maintain acceptable linearity and minimize distortion, the PAs are typically operated in class-A or class-AB configuration, which implies a low efficiency and further degrades under time-varying envelope modulation since the PAs are operated in backoff (in the valleys of the envelope) relative to their peak power (in the peaks of the envelope).

In state-of-the-art telecommunication systems, power control of RF transmitters is a key requirement. The mobile units transmit power at variable levels so that the signal strength for all the users is similar to maximize the system capacity, which requires the PAs to operate at 10–40-dB backoff from the peak power [2]. Consequently, the PAs operate with very low efficiency for most of the time, consuming a large part of the battery energy in portable handsets. Therefore, achieving high efficiency in PAs over wide loading range (for longer battery life) while maintaining the high degree of required linearity has been a major issue in low-power mobile communications.

Techniques such as Doherty amplifier [1], [3], [4] and linear amplification with nonlinear control (LINC) [1], [3] have been reported for the purpose of improving PA efficiency. Due to their complexity and the wide baseband bandwidth (BW) of the CDMA signals, these systems are not attractive for system-on-chip (SOC) solutions. Doherty amplifier for extended power range [4] has been demonstrated for CDMA signals using microstrip power-division and combination networks. However, integrated-circuit (IC) realization of the scheme requires use of on-chip power division and combination schemes, which are inherently lossy because of increased metal resistance at high frequencies (skin effect) and substrate coupling [5].

A linearization scheme (for nonlinear PAs) using a buck converter (e.g., envelope elimination and recombination (EER) [6], [7]) and efficiency-enhancement schemes (for linear PAs) using boost [8], [9], buck [10], and single-ended-primary-inductance converters (SEPICs) [11] have been reported in the literature. While the boost converter supplies a higher voltage to the PA, when needed, a fixed battery supply is applied under power backoff where a lower supply can be used, consequently degrading the overall system efficiency. Although buck-converter

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supplied systems operate efficiently with a wide range of PA supply voltages, their inability to operate at the peak-performance level when the required PA supply is higher than the terminal voltage (during the period when the battery terminal voltage is lower than its nominal value) makes it unattractive for use in a portable environment. Since a SEPIC uses two inductors and two capacitors (which are external to the IC) to transform energy from the battery to the load, its practice is not suitable for cost-effective portable applications, where a decrease in the external-component count is key, especially when considering SOC solutions. Therefore, to operate the portable RF systems at their peak-performance level, even with a battery that is close to fully discharged, and maintain high efficiency over a wide loading range, a power-tracking noninverting buck-boost converter-supplied PA topology is proposed in this paper. The functionality and performance of the proposed system is experimentally demonstrated by means of a prototype noninverting buck-boost converter and a laterally diffused metal-oxide semiconductor (LDMOS) PA circuit.

Section II reviews the requirements of CDMA PAs and the tradeoffs involved in designing high-efficiency wide-BW portable dynamic supplies. A comparative analysis of the efficiency enhancement schemes using dynamic supplies for CDMA applications is presented in Section III. In Section IV, the proposed system is described and its hardware implementation is discussed. Experimental results of the prototype amplifier and discussions are offered in Section V. Conclusions are offered in Section VI.

II. Background

A. CDMA PA Requirements

Since the time-domain CDMA signal exhibits large peak-to-average ratio [2], the PA is normally designed for the peaks to meet linearity requirements, thereby suffering from degraded power efficiency in the valleys of the envelope because of the lower signal swing and, consequently, increased voltage drop. Intuitively, to prolong battery life, the PA should be operated with high efficiency throughout the baseband signal envelope (e.g., peaks, valleys, and intermediate points), which can be achieved by making the supply of the PA follow the envelope profile of the input signal at any power level. To amplify the envelope signal accurately, the BW of the signal-processing circuit (dc–dc converter in the case of dynamic supplies) must be higher than the envelope-signal BW.

Power control is essential to ensure the CDMA system operates smoothly [12]. Since all users share the same RF band, each user appears to others as random noise. The power of an individual user must, therefore, be carefully controlled to prevent any one user from unnecessarily interfering with the others who are sharing the same frequency band. The other objectives of power control are to overcome the near–far problem [12] and to maximize channel capacity. The transmitted power usage probability density for CDMA applications [2] for rural and urban areas shown in Fig. 1 illustrates that the PA operates mostly at 15–20-dB backoff from the peak power. Consequently, an amplifier designed for a maximum output power of 27 dBm exhibits very low efficiency at 5-dBm output power, which correspond to 22-dB backoff, thereby wasting battery energy. In a CDMA/wide-band code-division multiple-access (WCDMA) architecture, transmitted power is adjusted (up or down) by 1 dB every 1.2 ms/666 μs, as requested by the base station, and the handset may enter or exit data-transmission mode once every 10 ms [13], [14].

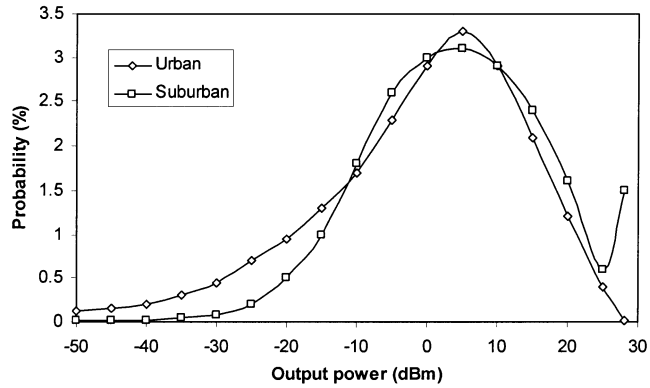

Fig. 1. Probability curves for transmit power level in urban and suburban environments [2].

Although the peak dc-to-RF efficiency of the PA occurs at the peak output power, the PA itself rarely operates at that power level (Fig. 1). Therefore, it is extremely important to calculate the average efficiency when considering the optimum PA configuration. The weighted average efficiency of the PA is defined as the ratio of average RF output power ($P_{\mathrm{RF_out_avg}}$) and average input supply power ($P_{\mathrm{SUPPLY_in_avg}}$), and is given by [2]

$$\eta_{\mathrm{avg}} = \frac{\int_0^{P_{\mathrm{RF_out,max}}} P_{\mathrm{RF_out}} p(P_{\mathrm{RF_out}}) dP_{\mathrm{RF_out}}}{\int_0^{P_{\mathrm{RF_out,max}}} P_{\mathrm{SUPPLY_in}}(P_{\mathrm{RF_out}}) p(P_{\mathrm{RF_out}}) dP_{\mathrm{RF_out}}} \quad (1)$$

where $P_{\mathrm{RF_out}}$, $p(P_{\mathrm{RF_out}})$, and $P_{\mathrm{SUPPLY_in}}(P_{\mathrm{RF_out}})$ are RF output power, the probability of operating at RF output power and the supply power required at $P_{\mathrm{RF_out}}$, respectively. This quantity is the measure of the effectiveness of the PA to convert the battery-stored energy into transmitted energy at the antenna [2]. Obviously, for increased battery life, the PA and any additional circuit (e.g., dynamic converter supply) either used for achieving linearity or improving efficiency must operate with high efficiency across all loading conditions.

B. Dynamic Converter Supplies

Switching regulators, in spite of their complexity and noisy characteristics, are most suitable for battery-dependent applications because of their high efficiency compared to linear regulators and charge pumps. Furthermore, switching regulators are capable of producing output voltages that are both lower (*buck* converter) and higher (*boost* converter) than their respective input voltages. In contrast to conventional dc–dc converters, dynamic converters' output voltages vary with time, depending on a time-varying control signal. In principle, any dc–dc converter can be used as a dynamic supply provided it is stable under varying operating conditions, and the circuit's BW is sufficiently high to follow the control signal.

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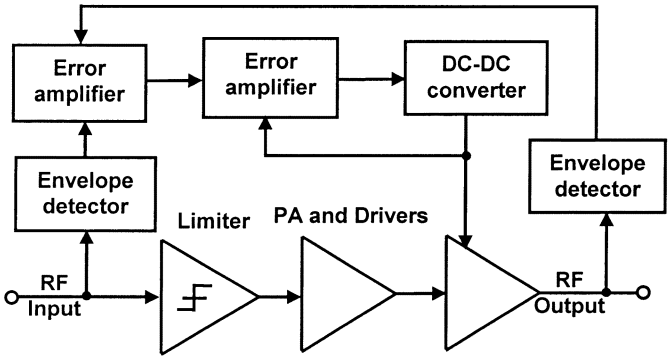

	CDMA IS-95	WCDMA
Baseband BW	1.25 MHz	3.84 MHz
Converter BW	5 MHz	15.36 MHz
Switching Frequency	25 MHz	76.8 MHz

Fig. 2. Kahn envelope elimination and restoration scheme and requirements of the dc–dc converter for CDMA IS-95 and WCDMA specifications.

1) Efficiency Perspective: The efficiency of a switching regulator (η) is the ratio of the output ($P_{\rm OUT}$) to the input ($P_{\rm IN}$) power, and is given by

$$\eta = \frac{P_{\rm OUT}}{P_{\rm OUT} + P_{\rm LOSS}} \tag{2}$$

where $P_{\rm LOSS}$ is the total power loss in the converter, which is the sum of the conduction losses and switching losses. Conduction loss is dependent on the load current—the higher the load current, the higher the conduction loss. On the other hand, switching loss is proportional to the switching frequency, which is independent of loading conditions. Under light loads, the efficiency of the converter is dictated by its switching losses; therefore, a lower switching frequency should be used during low loading conditions to achieve high overall converter efficiency. Unfortunately, the size of the external inductor and capacitor increase with lower switching frequency if the ripple voltage is to remain low for accuracy, which is inconsistent with low external component count and cost-effective SOC solutions for portable applications.

2) BW Perspective: The feedback compensation network in a dc–dc converter is designed to maximize the BW while still ensuring a stable operation. Generally, the closed-loop BW of a dc–dc converter is limited to one-tenth of the switching frequency [15], but it can be extended to one-fifth of the switching frequency if careful design practices are exercised. For a wider BW, the converter switching frequency must be increased, which increases switching losses and, consequently, lowers light-load efficiency. In boost and buck-boost converters, the right half plane (RHP) zero must be designed to reside far from the unity-gain frequency (UGF), which can be accomplished by selecting a smaller power inductor value. Having a smaller inductor, however, increases the root mean square (rms) current rating of the power switches and induces more conduction losses in the current-flowing path.

III. Efficiency Enhancement Schemes Using Dynamic Supplies

Reported schemes targeted toward improving the efficiency of RF PAs using dynamic supplies can be broadly classified in two categories, which are: 1) nonlinear PAs with a linearization circuit and 2) linear PAs with an efficiency-enhancement circuit. The control signal for the dynamic supply can be either generated from: 1) the PA's input signal using a directional coupler and a detector circuit or 2) the baseband processor either as an analog signal or digital data, which can be converted back to an analog signal using a digital-to-analog converter (DAC). While the control signal generation using a PA's input signal is suitable for a standalone PA, obtaining a control signal from the baseband processor is conducive toward complete system implementation of the radio transceiver. In Section III-A, the PA schemes are discussed for standalone applications where the control signal is generated from the PA's input signal, which can be easily extended to the other type of systems.

A. Nonlinear PAs With a Linearizing Circuit

Although class-B, class-C, class-D, class-E, and class-F PAs show high efficiency, they are often not suitable for linear applications because they introduce nonlinearities spurs in adjacent channels. However, with a suitable linearizing circuit, such as EER [6], these efficient PAs have been used for modulation schemes requiring linear amplification [7]. The EER technique [6] combines a nonlinear RF PA with an envelope amplifier, the schematic of which is shown in Fig. 2. The envelope amplifier is built with a pulsewidth modulated (PWM) buck converter. While EER achieves high peak-power efficiency, the necessarily high-frequency switching converter results in lower efficiency at power backoff (higher switching loss). To suppress the fourth-order harmonics in the envelope amplifier, the desired converter BW must be four times the envelope BW [16]. Accordingly, numerical values of the dc–dc converter's BW and switching frequency for CDMA and WCDMA applications are given in Fig. 2.

Although EER shows improvement in peak-power efficiency [6], due to the high converter switching frequency requirement and, consequently, higher switching losses, light-load converter efficiency is degraded, thereby decreasing the overall system efficiency. Other challenges in designing an IC implementation of the EER scheme are: 1) an RF delay line is required for accurate recombination of the envelope signal and the constant amplitude RF signal; 2) difficulty in detecting and restoring low-power envelope signals (-80 dBm); 3) substantial AM-to-PM conversion in active limiters at high frequencies corrupts the RF signal phase [16]; and 4) the envelope detector and dynamic converter supply must be linear. At present, the Kahn EER technique has only been shown for 30-KHz baseband applications (North American Digital Cellular (NADC) applications) [7].

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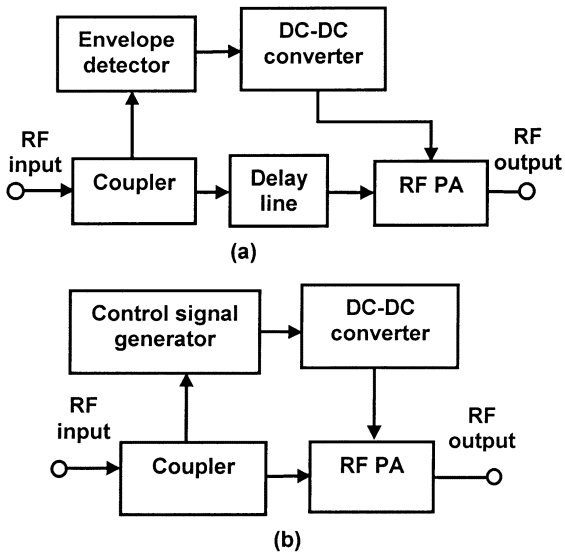

Fig. 3. Generalized functional block diagram of the: (a) envelope-follower linear PA and (b) envelope-tracking linear PA.

TABLE I
COMAPATIVE EVALUATION OF LINEARIZATION AND EFFICIENCY-ENHANCEMENT SCHEMES USING DYNAMIC SUPPLY

Technique	Advantages	Disadvantages
Kahn EER	• High peak-power efficiency	• Large converter BW and higher switching frequency results in degraded light-load efficiency • Stringent requirement of detector linearity, limiter phase distortion, and delay mismatch
Envelope-Follower PA	• Close to peak-power efficiency	• Large converter BW and higher switching frequency results in degraded light-load efficiency • Detector linearity requirement and delay mismatch
Envelope-Tracking PA	• Lower converter BW and lower switching frequency results in higher light-load efficiency	• Low peak power efficiency (but average efficiency is what matters for battery life!)

B. Linear PAs With an Efficiency-Enhancement Circuit

Efficiency of linear PAs is improved by dynamically varying the bias point, which is determined by the baseband signal (envelope) characteristics. Linear PAs with dynamic supplies have been investigated with bias control at the input and output of the amplifier (gate/base and drain/collector in MOSFETs and bipolar junction transistors (BJTs), respectively [8], [9], [18]). A theoretical evaluation of the efficiency enhancement resulting from dual bias control is reported in [19] and experimental results for a similar architecture have been demonstrated in [10]. All of these schemes can be broadly classified in two categories, which are: 1) the envelope-follower PA and 2) the envelope-tracking PA.

1) Envelope-Follower PA: The block diagram representation of an envelope follower PA is shown in Fig. 3(a), where the supply voltage and current of the PA is changed dynamically by following the complete envelope. The supply voltage is adjusted dynamically by a boost converter [8], [9] only when the required supply voltage is greater than the battery voltage. To vary the bias current with constant supply, the gate voltage is changed according to the envelope signal [18] and a theoretical dual bias (both supply voltage and bias current) control scheme is proposed in [19]. By following the envelope completely, the peak-load efficiency of the system is improved. However, higher BW requirement and subsequently higher switching frequency (same as in the EER scheme presented in Fig. 2) results in lower converter efficiency at light loads. As before, requirement of an RF delay line (equal to the delay of envelope signals while amplified through the converter, which is of the order of microseconds) and the resulting delay mismatch issues [20] makes this scheme unattractive for IC implementation.

2) Envelope-Tracking PA: To mitigate the requirement of an RF delay line and overcome the problems of delay mismatch, instead of following the envelope completely, the supply voltage is adjusted dynamically using a buck converter according to the rms value of the envelope signal [10]. A generalized block diagram of such a scheme is shown in Fig. 3(b). Since the converter does not follow the complete envelope, switching frequency can be lower than what is required for the EER and the envelope follower technique, thereby achieving increased light-load efficiency and, consequently, longer battery life. However, with the highly variable nature of the batteries used in portable applications, the buck-converter supplied systems cannot be operated at their peak performance when the required supply is higher than battery voltage. A comparative evaluation of the dynamic supply schemes discussed in this section is presented in Table I, which states that the envelope-tracking PA is the best scheme for dynamically changing the supply voltage and current to maintain high efficiency over wide loading conditions.

IV. PROPOSED SYSTEM AND HARDWARE IMPLEMENTATION

A. System Architecture

Since power control is incorporated in CDMA systems, dynamically changing the supply voltage and current as a function of power (termed as *power tracking*), which changes at a much slower rate compared to the envelope, is the best option for achieving higher light load efficiency and, consequently, increased battery life. For low-voltage portable applications, a noninverting buck-boost converter is needed to operate the RF system at its peak performance level throughout the battery voltage span from a freshly charged to a fully discharged condition. To achieve the dual objectives of higher average efficiency and peak system performance, irrespective of battery condition, a power-tracking PA is proposed. The schematic of the circuit is the same as the one shown in Fig. 3(b), with the exception that a power detector is used for the control-signal generation circuit, and the dc–dc converter is a noninverting synchronous buck-boost converter. The power detector, which uses the RF input, generates a control voltage that determines the output voltage of the buck-boost converter. The PA supply

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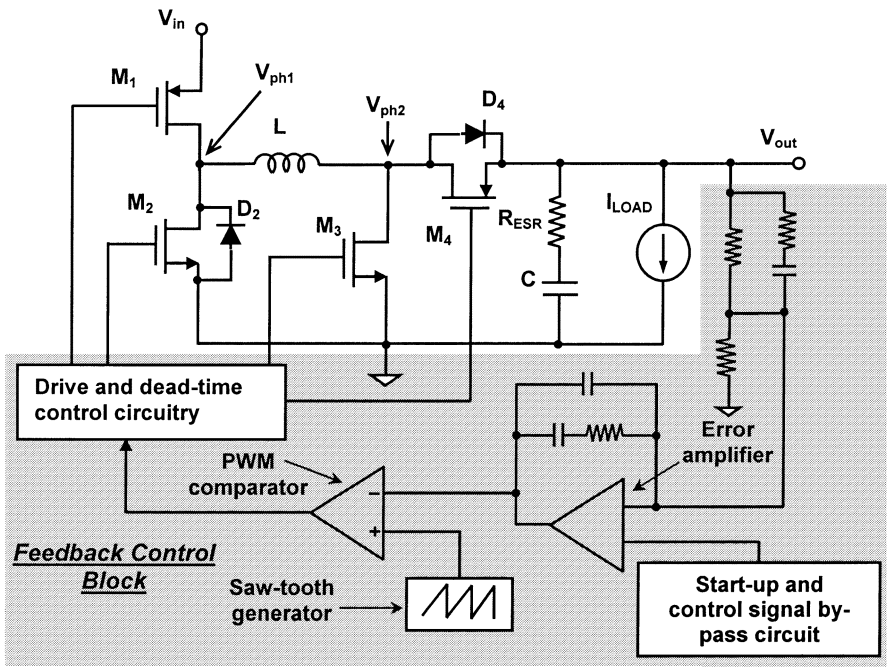

Fig. 4. Voltage-mode synchronous buck-boost converter.

current is also adjusted dynamically, the details of which are explained in Section IV-B.

B. Hardware Implementation

1) Directional Coupler and Power Detector: A microstrip branch-line directional coupler [21] with coupling coefficient of 5 dB was designed and fabricated on a printed-circuit board (PCB) having a thickness 0.032 in, permittivity (ε_r) of 4.8, and loss tangent ($\tan\delta$) of 0.022. A commercial power detector (LTC 5505-2, Linear Technology, Milpitas, CA [22]) is used to detect the RF power generating a dc voltage proportional to its input power.

2) Noninverting Buck-Boost Converter: A noninverting buck-boost converter is essentially a cascade combination of a buck converter followed by a boost converter, where a single inductor-capacitor combination is used for both. The schematic of a voltage-mode synchronous buck-boost converter is shown in Fig. 4. During the on time of switches M_1 and M_3, the energy is stored in the magnetic field of inductor L. When switches M_1 and M_3 are turned off, M_2 and M_4 are turned on and the inductor energy is released to charge output capacitor C, and also provide the load current. Depending on the ratio of the on time to the total switching period [known as the *duty cycle* (D)], an output voltage both higher and lower than the input voltage is generated *on-the-fly*.

A 2.2-μH power inductor and a 47-μF output capacitor with equivalent series resistance (ESR) of 70 mΩ were chosen for the prototype converter power stage defining the peak inductor current to 3.0 A (peak-to-peak ripple current 1.5 A) and the output ripple voltage to 275 mV maximum, with a switching frequency of 500 kHz. For a constant switching frequency, a smaller inductor results in higher peak-current rating of the inductor and power switches, which requires a larger capacitor to achieve a specified output ripple voltage. A lower output ripple is critical for the overall system performance because any noise in the converter output directly couples to the PA output, which, consequently, increases spurious out-of-band distortion and degrades in-band modulation accuracy. Since large instantaneous values of current flows in and out of the output capacitor, the majority of the ripple is due to the ESR of the capacitor; hence, an output capacitor with a smaller ESR value is desirable.

In continuous conduction mode (CCM), the buck-boost converters' open-loop small-signal response shows a pair of complex-conjugate poles (related by inductor L, capacitor C, and duty cycle D), an RHP zero (related by inductor L, duty cycle D, steady-state output voltage, and load current) and a left half-plane (LHP) zero (due to the ESR of the capacitor). Since the duty cycle varies dynamically to generate a time-varying output voltage, locations of the poles and RHP zero change. Therefore, the error amplifier's frequency compensation scheme is designed for the maximum value of the duty cycle, which results in the lowest pole and RHP zero frequencies. A type-III compensation scheme is used, which has two zeros at the complex-conjugate poles' frequency and three poles—the first at the origin, the second at the desired UGF, and the third at a higher frequency (to ensure rolloff). The converter is designed for a closed-loop BW of 20 kHz.

A fixed dead-time control scheme is used in the prototype for generating nonoverlapping clock signals to prevent "shoot-through" current, which is an unnecessary power loss resulting when the rectifier (M_2 and M_4) and pass transistors (M_1 and M_3) conduct simultaneously. The duty cycle of the converter was limited to less than unity by choosing the error amplifier's positive rail supply smaller than the peak sawtooth voltage, which prevents M_1 and M_3 to be ON for a long time during the converter start up and thereby eliminating the possibility of damaging the transistors (M_1, M_3) and the inductor

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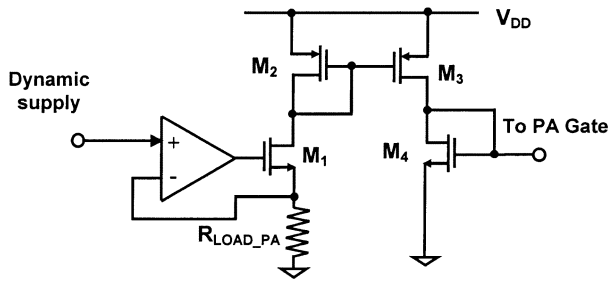

Fig. 5. Dynamic gate bias generation circuit.

(L). A slow-start circuit was incorporated in the prototype to reduce the initial transients and prevent catastrophic failures. After the converter completes the start up, the control signal from the RF detector enables the reference signal for the converter. The details of the design and implementation of the dynamic noninverting buck-boost converter can be found in [23].

3) PA and Dynamic Gate Bias Generation Circuit: An evaluation board of an LDMOS PA using the California Eastern Laboratory's (CEL) NE5520279A [24] operating in a class-A/class-AB configuration was used for the prototype system. The schematic of the circuit used for generating the dynamic gate bias in the prototype PA system is shown in Fig. 5. At any given instant, the output of the buck-boost converter is impressed across resistance $R_{\mathrm{LOAD_PA}}$, the value of which is equal to the PAs load-line resistance [1] for the prototype implementation. However, in IC design, the control voltage, resistor $R_{\mathrm{LOAD_PA}}$, and current mirrors can be suitably scaled down. The amplifier forces M_1's source voltage to be equal to the dynamic supply, thereby setting a proportional current through M_1 and M_2. This current is reflected in M_3 (current mirror M_2 and M_3) and flows through M_4, which generated the desired gate voltage for the PA. As the PAs supply changes with changes in RF input power, the gate voltage is also adjusted.

V. Experimental Results and Discussions

The buck-boost converter designed for the prototype linear PA system is capable of generating a dynamically variable output voltage between 0.4–4 V with load currents up to 0.65 A from an input supply of 2.4–3.4 V. The worst case response time of the converter for a 0.4–4 V output-step response is less than 300 μs and to a load-current step of 0–0.5 A is within 200 μs, yielding only a transient error of 40 mV in the output voltage. For brevity, all the experimental results of the prototype PA system presented here are for the converter input supply of 3.0 V.

The prototype PA system was tested with a CDMA IS-95 signal for a center frequency of 915 MHz and a 1.25-MHz baseband signal BW. Out-of-band linearity of the PA in CDMA applications is measured by ACPR, which is defined as the ratio of power in a specified BW at an offset from the center frequency to the channel power. In the CDMA IS-95 Standard, the first ACPR is measured as the ratio of the power in 30 kHz BW at an offset of 885 kHz from the center frequency to the power in 1.25 MHz channel BW. The second ACPR is measured as the ratio of the power in 30-kHz BW at an offset of 1.98 MHz from the center frequency to the channel power. Variations of the first and second ACPR for the PA using a fixed and dynamic supply is presented in Fig. 6(a), which shows that out-of-band linearity of the PA is not significantly degraded with the dynamic supply. The first and second ACPR values at the peak output power are less than −44 dBc and −60 dBc, respectively, and remains within the limits throughout the output power range, thereby satisfying the CDMA IS-95 requirements. The degradation of ACPR values at low power is attributed to the noise floor of the measurement system. The gain of the dynamic supply PA is reduced at lower output power levels [see Fig. 6(b)] because of the lower drain bias current and, consequently, decrease in the transistor's transconductance. In a CDMA transmitter, the gain of the last stage of the PA can be calibrated with the driver stages and variable gain amplifiers to achieve the dynamic range of the transmitter output power.

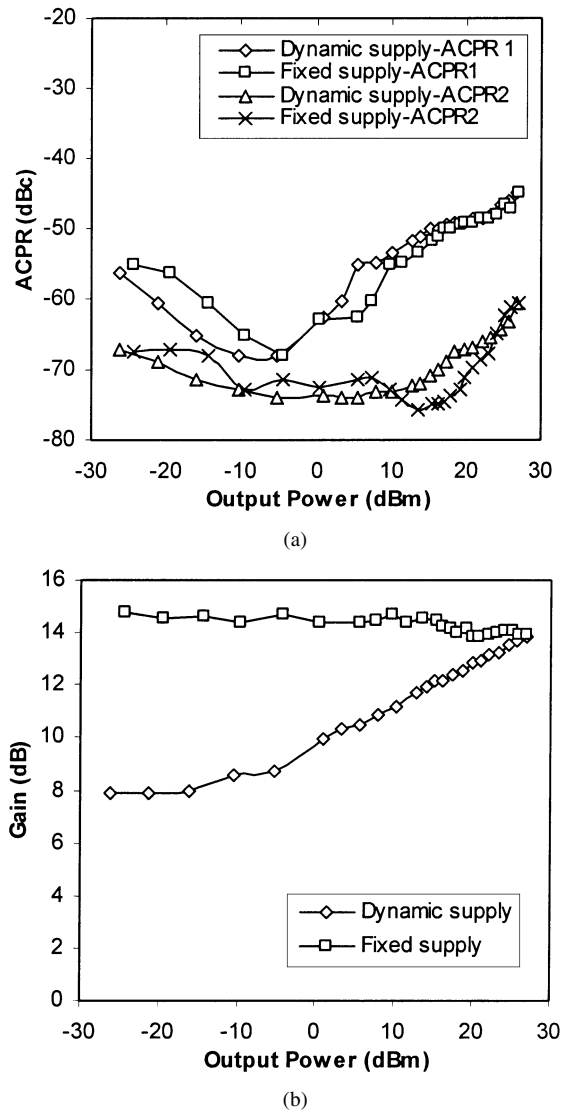

Fig. 6. Comparison of: (a) first and second ACPR and (b) gain of the dynamic-supply and fixed-supply PA.

Modulation accuracy of digitally modulated signals, e.g., CDMA, is expressed using error vector magnitude (EVM), which is the scalar distance between the ideal reference signal and measured signal [25]. Since the converter used in the

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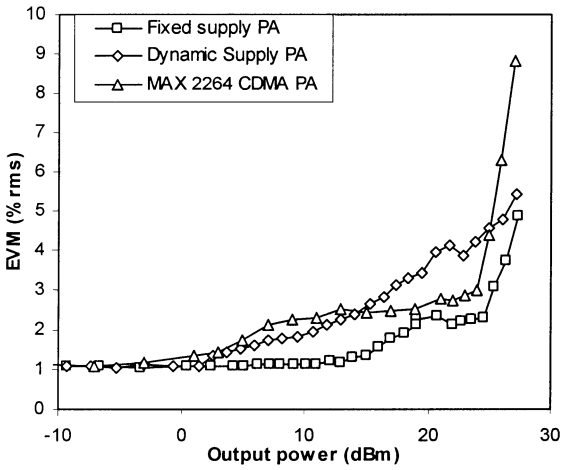
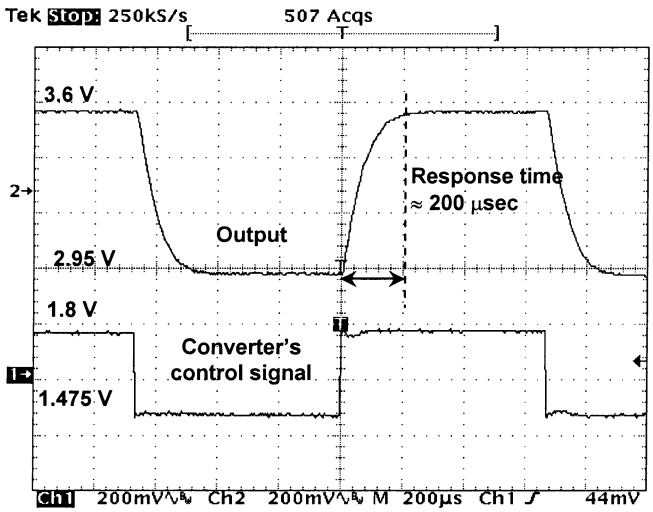
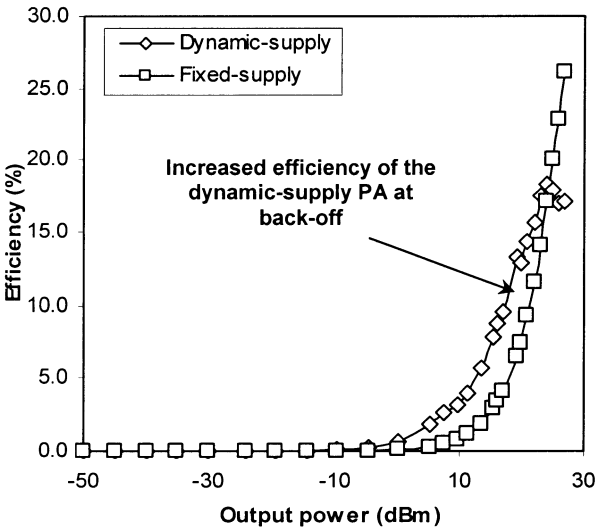


(a)

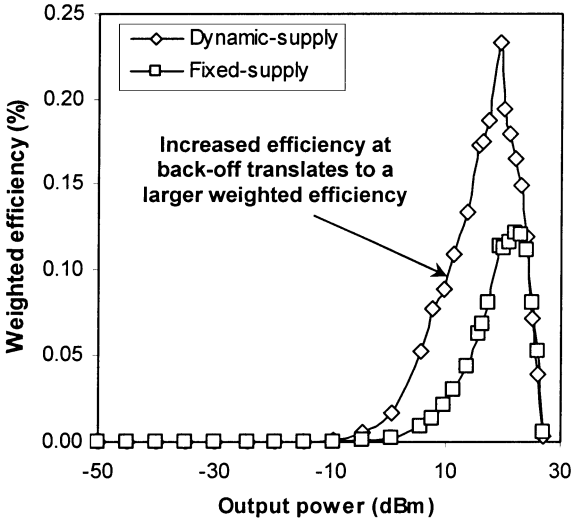


(b)

Fig. 7. (a) Comparison of the EVM results of the dynamic supply PA with the fixed supply PA and MAX2265 CDMA PA. (b) Dynamic converter's response to a worst case power adjustment from 26 (2.95 V) to 27 dBm (3.6 V).



(a)



(b)

Fig. 8. Comparison of: (a) efficiency and (b) weighted efficiency of the dynamic- and fixed-supply PA.

prototype system has a switching frequency of 500 kHz, the switching ripple falls within the transmitting channel BW of 1.25 MHz around the carrier center frequency. To investigate the effect of the switching power supply ripple on the in-band linearity of the prototype PA, EVM of the RF output signal was measured at various power levels. The overall EVM numbers obtained for the dynamic supply PA along with the fixed supply PA and a commercial CDMA PA (MAX2264) for different output power is shown in Fig. 7(a), which infers that the ripple in the PA's power supply marginally degrades the EVM, but remains within a factor of 6%. At peak output power, although the output ripple of the converter increases due to a higher load current, its effect on EVM is slightly greater than the fixed supply PA, but well below the commercial CDMA PA.

To verify the dynamic response capabilities of the system for CDMA IS-95 specifications (transmit power is adjusted by 1 dB every 1.2 ms, as requested by the base station [14]), a step stimulus was applied to the converters' control so as to change the PAs supply from 2.95 (output power of 26 dBm) to 3.6 V (output power of 27 dBm). From the experimental results shown in Fig. 7(b), it is seen that the converter responds to the worst case power adjustment within 200 μs. Although the calculated 1-dB step is for a change from 3.2 to 3.6 V, a higher step was chosen to ensure that the converter is guaranteed to respond, as per requirement, well within the specified time limit. The ACPR and EVM performance of the dynamic supply PA during the transient period was not possible to quantify since these tests are performed at a given power, which is adjusted manually from a RF source. Transmitter level system specification, e.g., bit error rate (BER), may be used to gauge the performance of the PA during the transient step change, which requires further investigation.

Drain efficiency, which is the ratio of RF output power to the input supply power, is the measure of PAs ability to convert battery power into usable RF power at the transmitter antenna. Therefore, all the discussions offered here are with respect to the drain efficiency. Efficiency curves for the PA with fixed and dynamic supply are illustrated in Fig. 8(a), which shows that the PA with a dynamically adaptive supply exhibits higher efficiency at backoff power. The efficiency curves for both the

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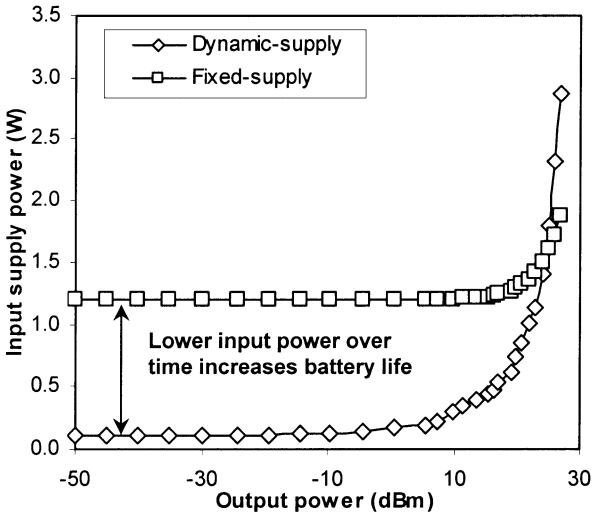
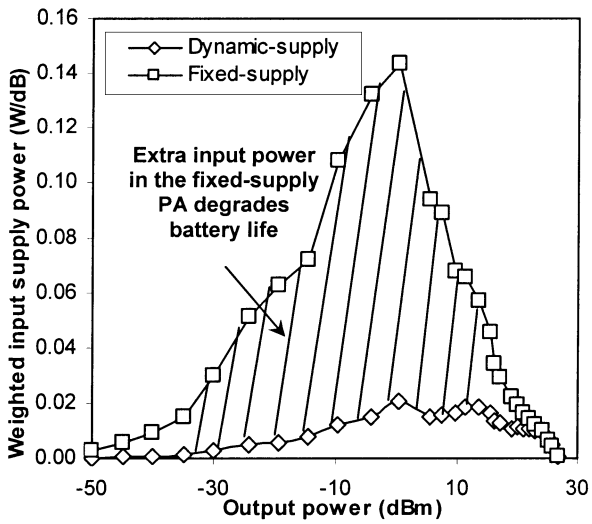


(a)



(b)

Fig. 9. Comparison of the: (a) input supply power and (b) weighted input supply power of the dynamic- and fixed-supply PA.

fixed- and dynamic-supply PA are multiplied with the probability distribution curve for urban usage (Fig. 1) and the resulting weighted efficiency curves are presented in Fig. 8(b), which shows that the increased efficiency of the dynamic-supply PA is significant in the region of maximum output power distribution—most operated region. In the low output power range (less than −10 dBm), the efficiency curves [in Fig. 8(a) and (b)] are not distinguishable because the overall system efficiency degrades to very small values. However, while the input supply power for the fixed-supply PA remains constant at lower output power, the dynamic-supply PA tracks the input RF power to adjust both the voltage and current, resulting in reduced input supply power [see Fig. 9(a)], thereby exhibiting higher overall efficiency.

To estimate the battery life improvement, weighted input supply power profiles for both fixed- and dynamic-supply PA (using the same procedure adopted to obtain Fig. 8(b), but considering input power) are shown in Fig. 9(b). Clearly, the average input supply power, which is equal to the area under the weighted input power curve, for the dynamic-supply PA

TABLE II
COMPARISON OF REPORTED EFFICIENCY ENHANCEMENT SCHEMES USING DYNAMIC SUPPLIES AND THE WORK PRESENTED IN THIS PAPER

Scheme	Fixed supply efficiency	Dynamic supply efficiency
Buck-converter supplied AlGaAs/InGaAs MESFET PA [10]	2.2 %	11.2 %
Boost converter supplied GaAs MESFET PA [8]*	3.89 %	6.38 %
Buck-boost converter supplied LDMOS PA in this work	**1.53 %**	**6.78 %**

*Output power probability distribution profile used in [8] is not the same.

is much smaller than that of the fixed-supply PA for the same average output power. The weighted average efficiency of the dynamic-supply PA [calculated using (1)] is *4.43 times greater* than the fixed-supply scheme, which translates into a battery life improvement depending on the percentage of transmitter power consumed by the PA stage. This efficiency enhancement is compared with other results reported in the literature (Table II) and the prototype system proposed in this paper delivers comparable performance with respect to the other systems, but it is also to operate at peak system performance with a battery close to fully discharged, not to mention its inherent improved battery life performance. Since the buck-boost converter supplied LDMOS PA operates with a lower supply voltage and current than the boost converter supplied GaAs MESFET PA [8] under light loading conditions, a higher average efficiency is achieved. On the other hand, the converter used in the prototype (which was designed for functionality and not optimized for efficiency) showed efficiency of 10%–65% over 0.4–4-V output, compared to the high-efficiency buck converter used in [10], resulted in a lower average efficiency. By using a buck-boost converter with high efficiency over a wide loading range, the system efficiency can be further improved. Moreover, the overall system efficiency also depends on the peak-power efficiency of the PA, irrespective of its type (e.g., GaAs HBT/MESFET, SiGe HBT, etc.)—a PA with higher peak-power efficiency can be operated with higher efficiency over its loading range with a dynamic supply scheme, thereby improving overall system efficiency.

VI. CONCLUSION

A 27-dBm linear prototype PA for CDMA signals with a dynamically adaptive buck-boost converter supply using a LDMOS transistor has been presented. The overall increase in system efficiency with a dynamic supply implies *88% improvement in battery life* (assuming that the PA consumes 20% of the total transceiver power) when compared to a fixed supply PA, while maintaining the linearity (ACPR) requirements of CDMA IS-95 specifications. The overall EVM for the dynamic-supply PA degrades marginally over the EVM of a fixed-supply PA. The dynamically adaptive buck-boost converter's response to a worst case power adjustment of 1 dB in 1.2 ms is within 200 μs. A comprehensive analysis of the suitability of various efficiency enhancement schemes using dynamic supplies for CDMA portable applications shows that the adjustment of the PA supply voltage and current as

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a function of power (*power tracking*) can be accomplished with a lower switching frequency converter, therefore, having increased light-load efficiency and, consequently, longer battery life. With the increased demand for high-efficiency RF PAs in portable wireless applications, the dynamically adaptive buck-boost converter supplied PA plays a pivotal role in maintaining peak performance, irrespective of the battery condition, while maximizing battery life.

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Dr. Rincón-Mora is a member of Tau Beta Pi, Eta Kappa Nu, Phi Kappa Phi, and the Society of Hispanic Professional Engineers. He was named Outstanding Ph.D. graduate by the Georgia Institute of Technology. He was the recipient of the National Hispanic in Technology Award presented by the Society of Professional Hispanic Engineers. He was inducted into the Council of Outstanding Young Engineering Alumni by the Georgia Institute of Technology. He was the recipient of the Charles E. Perry Visionary Award presented by the Florida International University. He was also the recipient of a Commendation Certificate presented by the Lieutenant Governor of California.

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