

MICROWAVE POWER AMPLIFIERS WITH DIGITALLY-CONTROLLED POWER SUPPLY VOLTAGE FOR HIGH EFFICIENCY AND HIGH LINEARITY

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ABSTRACT

A power amplifier architecture is presented which comprises a basic amplifier with an efficient, high modulation bandwidth DC-DC converter. The amplifier and the DC-DC converter are controlled by a digital signal processor that provides input signal pre-distortion, supply voltage optimization and equalization. Experimental results at 950MHz showed ACPR values acceptable for IS-95 CDMA handset applications. With variable power supply, the overall efficiency improved by a factor of 1.4x (when averaged over representative conditions of usage).

INTRODUCTION

Efficiency of power amplifiers can be significantly improved by employing a DC-DC converter which varies the power supply voltage in accordance with the envelope of the input signal [1-2]. This technique (known as "envelope tracking" or "dynamic supply voltage" amplifier) improves the amplifier efficiency when the output power is below its saturated value, which can be a large fraction of the time in cellular phone applications.

In past work [1], we have shown that such amplifiers can be implemented using GaAs HBT-based DC-DC converters, which can be modulated at bandwidths of 1MHz, and have efficiencies of up to 80%. The power supply control voltage was derived from an analog envelope detector.

Amplifiers based on this architecture have inherent non-linearities associated with them. Non-linearities stem from two sources. One source is the fact that the amplifier gain and phase characteristics change with a change in the power supply voltage, and thus the signal dependent power supply voltage is a source of AM-AM and AM-PM distortion. The other stems from the time delay and the finite frequency response of the DC-DC converter.

In this work we demonstrate that digital control of the DC-DC converter, coupled with digital predistortion of the amplifier input signal, can improve the amplifier linearity while optimizing efficiency. Application of DSP allows

flexibility in the algorithm for power supply selection, ability to equalize the delay and the frequency response of the DC-DC converter, as well as ability to predistort the RF signal to overcome the associated AM-AM conversion.

The amplifier architecture reported here is a significant step towards realization of a "smart" power amplifier, in which the amplifier parameters are dynamically varied in accordance with the signal requirements in order to maximize performance.

AMPLIFIER STRUCTURE

A GaAs MESFET amplifier was used in conjunction with a DC-DC converter implemented with a GaAs HBT, as shown schematically in Fig.1a and b. Fig 1a shows the previously reported system based on an envelope detector to control the power supply voltage; Fig 1b illustrates the modified DSP-based system reported in this paper.

GaAs HBT based DC-DC converters were implemented as hybrid circuits or as partially integrated circuits. The converter efficiency was approximately 80%.

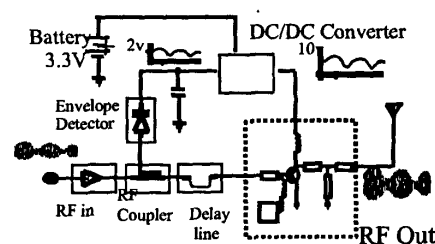


Figure 1a: Amplifier architecture with dynamic supply voltage under analog control

Fig. 2 shows the relationship between power supply voltage and instantaneous output power that was implemented, and for comparison the peak-to-peak voltage swing at the given output power.

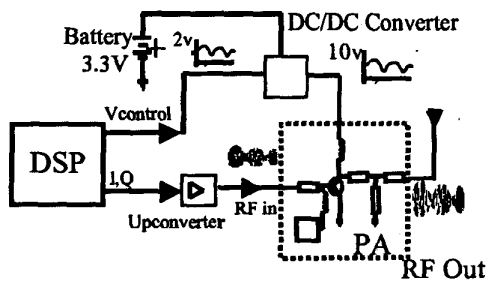


Figure 1b: Amplifier architecture with dynamic supply voltage under digital control

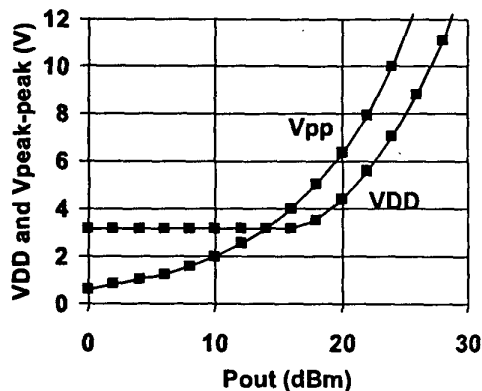


Fig.2: Algorithm of VDD vs output power. Also shown is peak-to-peak drain voltage

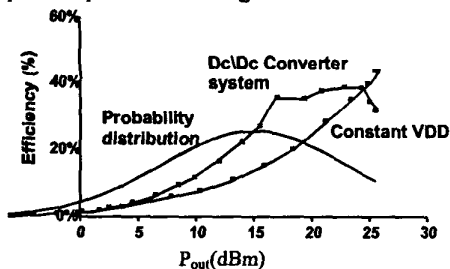


Fig.3: Measured efficiency of amplifier with constant VDD and with dc/dc converter, at different output power levels. Also shown is a representative distribution of output power for wireless application.

The choice of supply voltage kept the amplifier in Class AB operation over a wide range of output powers. The overall system efficiency depends on the efficiency of the amplifier at different power levels and the efficiency of the DC-DC converter. The efficiency of the system is shown as

a function of output power in Fig.3. This demonstrates that while at maximum output power the inclusion of the DC-DC converter is detrimental to efficiency, at lower output powers it is highly advantageous. A suitable average efficiency can be computed based on power usage probabilities. A representative probability distribution of output power in cellular phone applications is shown in Fig. 3. The overall efficiency increases by a factor of typically $\times 1.4$

The linearity of the dynamic supply voltage amplifier is typically worse than the amplifier with fixed supply voltage because of the variation of gain with supply voltage. The power amplifier gain as a function of output power at various power supply voltages is shown in Fig.4. No particular design optimization of the MESFET-based amplifier was done to minimize the gain variations. From these data, substantial changes in gain as a function of output power could be inferred, leading to undesirable AM-AM conversion. We have shown that fixed predistortion can be used to overcome this nonlinearity to a considerable extent [4]. Part of the distortion, however, cannot be compensated within the framework of a memoryless nonlinear system since there is an inherent delay and a frequency-dependent transfer function between the measured signal envelope and the DC-DC converter output. The frequency response of the DC-DC converter displays a roll-off at frequencies above 700kHz. Fig. 5 shows the frequency response of the DC-DC converter. The technique reported here allows for compensation of all these sources of nonlinearity (on an open loop basis).

ALGORITHM

The DSP computes an appropriate control voltage for the DC-DC converter according to the signal envelope, taking into account the DC and AC response of the converter. It also computes a predistorted input signal for both the I and the Q channel to be fed into the amplifier, using the amplifiers AM-AM and AM-PM characteristics for this supply voltage.

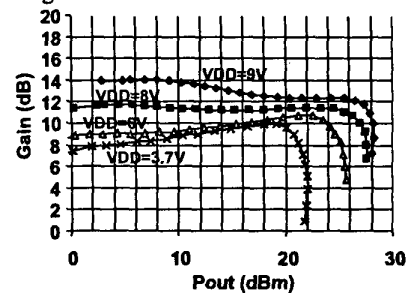


Fig. 4: Measured variation of PA gain with V_{dd} .

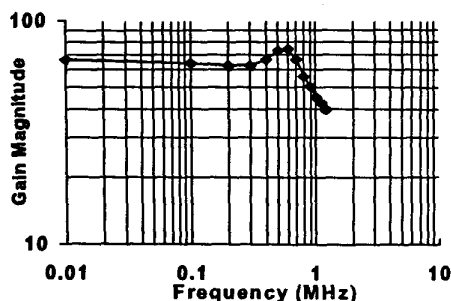


Fig. 5: Frequency response of the DC-DC Converter

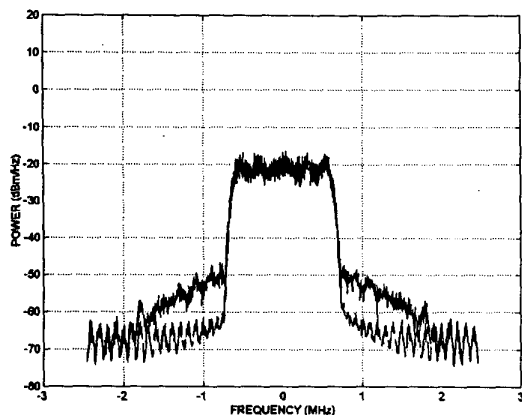


Fig. 6: Simulated amplifier output, with and without predistortion

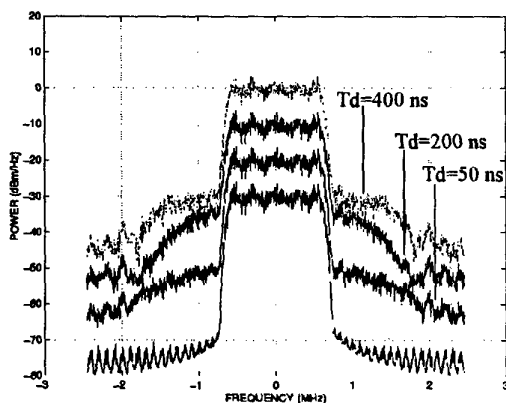


Fig. 7: Amplifier response to the predistorted input with different time delays in the DC-DC converter

The predistorted I and Q are given by:

$$I_d = (1/G_d)(I \cos \phi_d + Q \sin \phi_d) \quad (1)$$

$$Q_d = (1/G_d)(-I \sin \phi_d + Q \cos \phi_d) \quad (2)$$

where G_d and ϕ_d describe the gain and phase deviations of the amplifier as a function of input power induced by the power supply variation. The DSP computations are carried out at baseband. The I and Q signals must then be upconverted and amplified to provide the inputs to the power amplifier. In a cellular phone realization the computations can be performed in the same DSP that generates the conventional signal. In our experiments, the signals were precomputed using MATLAB in a conventional PC, and then stored in the memory of arbitrary waveform generators (high speed digital-to-analog converters). They were subsequently read out and upconverted to feed into the power amplifier. Fig. 6 shows the simulated amplifier response to the input signal with and without predistortion, indicating that the AM-AM and AM-PM of the amplifiers are significant and can be overcome by predistortion (at least under optimal conditions). Fig. 7 shows the simulated amplifier response to the predistorted input signal with different time delays introduced into the DC-DC converter. The results indicate that the ACPR is quite sensitive to the timing relationships between the supply voltage and input signal.

EXPERIMENTAL RESULTS

With the use of the DSP, the output frequency spectrum for an IS-95 CDMA input signal was considerably improved. A representative output spectrum for an output power of 28dBm is shown in Fig. 8 (together with the spectrum obtained without predistortion for comparison). An improvement of 8 dB in ACPR was observed. The value of ACPR with predistortion is -44 dBc (which exceeds the IS-95 minimum specification of -42dBc) at the largest output power (and is better at lower output power). The linearization by DSP allows increasing the output power by about 4 dBm (and thus improving efficiency) while staying within the specifications of the IS-95 signals.

CONCLUSIONS

An amplifier architecture is demonstrated which can provide improved efficiency and linearity for CDMA signals. The architecture employs a high speed DC-DC converter, which can be integrated with the power amplifier [5] and DSP control over amplifier input signal as well as power supply voltage. The system can flexibly implement a variety of algorithms for system optimization. Application of DSP to amplifier control is becoming increasingly cost-effective [6]. However, this approach requires integrated design of the overall transmitter since

the DSP function and the power amplifier must be closely coupled.

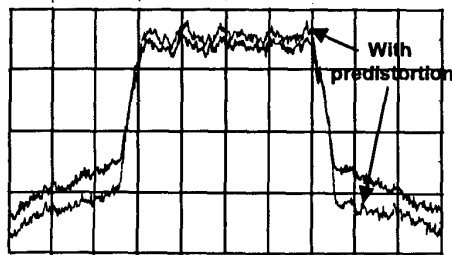


Fig.8: Measured output power spectra for an IS-95 CDMA signal with and without predistortion and equalization (30 kHz resolution bandwidth, 3MHz span). The corresponding ACPR values are -44dBc and -36dBc .

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