

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2025-00034
U.S. Patent No. 10,879,254
Issue Date: December 29, 2020

Title: THREE - DIMENSIONAL MEMORY DEVICES HAVING THROUGH
ARRAY CONTACTS AND METHODS FOR FORMING THE SAME

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 10,879,254
PURSUANT TO 35 U.S.C. §§311-319 and 37 C.F.R. §42**

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LISTING OF EXHIBITS

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1001	U.S. Patent No. 10,879,254 to Guo et al. (“the ’254 Patent”)
1002	File History of U.S. Patent No. 10,879,254 (“the ’254 FH”)
1003	Declaration of Dr. Jack C. Lee (“Lee”)
1004	<i>Curriculum Vitae</i> of Dr. Jack C. Lee
1005	U.S. Patent No. 10,777,501 to Nakajima et al. (“Nakajima”)
1006	U.S. Patent Publ. No. 2019/0198524 to Fujiki et al. (“Fujiki”)
1007	U.S. Patent No. 10,658,378 to Tao et al.
1008	Michelsoni, “3D Flash Memories” (2016)
1009	U.S. Patent Publ. No. 2017/0179026 to Toyama et al. (“Toyama”)
1010	U.S. Patent No. 10,354,980 to Mushiga et al. (“Mushiga”)
1011	U.S. Patent Publ. No. 2019/0229125 to Zhou et al.
1012	PCT Publication No. WO 2019/042103 A1 to Dai et al.
1013	U.S. Patent No. 10,679,721 to Kim et al.
1014	Aritome, “NAND Flash Memory Technologies” (“Aritome”)
1015	U.S. Patent No. 10,290,643 to Kai et al. (“Kai”)
1016	U.S. Patent No. 9,859,297 to Park et al. (“Park”)
1017	U.S. Patent Publ. No. 2018/0308559 to Kim et al. (“Kim”)
1018	U.S. Patent No. 8,945,996 to Tang et al.
1019	U.S. Patent No. 10,115,632 to Masamori et al.

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1020	U.S. Patent No. 5,945,717 to Chevallier
1021	U.S. Patent No. 10,347,487 to Lee et al.
1022	Ronse, “Optical lithography—a historical perspective,” C. R. Physique 7 (2006) (“Ronse”)
1023	U.S. Patent Publ. No. 2019/0081061 to Tessariol et al. (“Tessariol”)
1024	U.S. Patent No. 9,620,514 to Kai et al.
1025	Hwang, “Atomic Layer Deposition for Semiconductors,” Springer (2014) (“Hwang”)
1026	U.S. Patent No. 10,515,799 to Wang et al.
1027	U.S. Patent No. 9,570,460 to Kanakamedala et al.
1028	U.S. Patent No. 9,728,546 to Serov et al.
1029	Excerpt from YMTC’s Exemplary Infringement Claim Chart for U.S. Patent No. 10,879,254 (Ex. A-2 to Disclosure of YMTC II Asserted Claims and Infringement Contentions, dated October 2, 2024) (“Ex. A-2, YMTC’s Contentions”) [PROTECTIVE ORDER MATERIAL – FILED UNDER SEAL]
1030	U.S. Patent No. 11,075,084 to Shen et al.
1031	U.S. Patent No. 10,304,852 to Cui et al. (“Cui”)
1032	U.S. Patent No. 9,793,139 to Sharangpani et al.
1033	Minute Order (case schedule), Dkt. No. 141, dated September 18, 2024 in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL

Petition for *Inter Partes* Review of U.S. Patent No. 10,879,254

EXHIBIT NO.	DESCRIPTION
1034	Combined Civil and Criminal Federal Court Management Statistics (December 31, 2023), available at https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distcomparison1231.2023.pdf
1035	Plaintiff and Counterclaim Defendant Yangtze Memory Technologies Company, LTD.'s Disclosure of YMTC II Asserted Claims and Infringement Contentions, dated October 2, 2024 in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1036	Docket from <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:24-cv-04223-RFL which has been consolidated with Case No. 3:23-cv-05792-RFL

LISTING OF CHALLENGED CLAIMS

Ref. #	Listing of Challenged Claims
Claim 1:	
[1.PRE]	A method for forming a three-dimensional (3D) memory device, comprising:
[1.A]	forming a stack comprising a plurality of dielectric/sacrificial layer pairs on a substrate;
[1.B]	forming a channel structure extending vertically through the stack;
[1.C]	forming a first opening extending vertically through the stack;
[1.D]	forming a spacer on a sidewall of the first opening;
[1.E]	forming a through array contact (TAC) extending vertically through the stack by depositing a conductor layer over the spacer in the first opening; and
[1.F]	after forming the TAC, forming a slit extending vertically through the stack.
Claim 2:	
[2]	The method of claim 1, further comprising prior to forming the first opening, forming a dummy channel structure extending vertically through the stack.
Claim 3:	
[3]	The method of claim 1, wherein forming the first opening comprises simultaneously etching the first opening through the stack and a second opening outside of the stack.
Claim 4:	
[4]	The method of claim 3, wherein forming the TAC comprises depositing the conductor layer in the first opening to form the TAC and in the second opening to form a peripheral contact.

Ref. #	Listing of Challenged Claims
Claim 5:	
[5.PRE]	The method of claim 1, wherein forming the spacer on the sidewall of the first opening comprises:
[5.A]	depositing a dielectric layer on the sidewall and a bottom surface of the first opening; and
[5.B]	removing part of the dielectric layer that is deposited on the bottom surface of the first opening.
Claim 6:	
[6]	The method of claim 5, wherein the deposition of the dielectric layer comprises atomic layer deposition (ALD), and the removal of the part of the dielectric layer comprises anisotropic etching on the bottom surface of the first opening.
Claim 7:	
[7.PRE]	The method of claim 1, wherein forming the spacer on the sidewall of the first opening comprises:
[7.A]	forming a plurality of shallow recesses by removing parts of the sacrificial layers abutting the sidewall of the first opening;
[7.B]	depositing a dielectric layer filling in the shallow recesses and on the sidewall and a bottom surface of the first opening; and
[7.C]	removing part of the dielectric layer that is deposited on the bottom surface of the first opening.
Claim 8:	
[8]	The method of claim 7, wherein the removal of the part of the dielectric layer comprises isotropic etching on the sidewall and the bottom surface of the first opening.

Ref. #	Listing of Challenged Claims
Claim 9:	
[9.PRE]	The method of claim 1, wherein forming the first opening comprises:
[9.A]	simultaneously etching the first opening through the stack, a second opening outside of the stack, and a third opening through the stack,
[9.B]	wherein a lateral dimension of the third opening is smaller than lateral dimensions of the first and second openings.
Claim 10:	
[10.PRE]	The method of claim 9, wherein forming the spacer on the sidewall of the first opening comprises:
[10.A]	depositing a dielectric layer (i) fully filling in the third opening to form a dummy channel structure and (ii) partially filling in the first opening and the second opening; and
[10.B]	removing parts of the dielectric layer that are deposited on a bottom surface of the first opening and on a bottom surface of the second opening.
Claim 11:	
[11.PRE]	A method for forming a three-dimensional (3D) memory device, comprising:
[11.A]	forming a stack comprising a plurality of dielectric/sacrificial layer pairs on a substrate;
[11.B]	forming a channel structure extending vertically through the stack;
[11.C]	forming a dummy channel structure extending vertically through the stack;
[11.D]	simultaneously etching a first opening through the stack and a second opening outside of the stack;

Ref. #	Listing of Challenged Claims
[11.E]	simultaneously forming a first spacer on a sidewall of the first opening and a second spacer on a sidewall of the second opening;
[11.F]	depositing a conductor layer (i) filling in the first opening to form a through array contact (TAC) and (ii) filling in the second opening to form a peripheral contact; and
[11.G]	after forming the TAC and peripheral contact, forming a slit extending vertically through the stack.
Claim 12:	
[12.PRE]	The method of claim 11, wherein forming the first spacer on the sidewall of the first opening comprises:
[12.A]	depositing a dielectric layer on the sidewall and a bottom surface of the first opening; and
[12.B]	removing part of the dielectric layer that is deposited on the bottom surface of the first opening.
Claim 13:	
[13]	The method of claim 12, wherein the deposition of the dielectric layer comprises atomic layer deposition (ALD), and the removal of the part of the dielectric layer comprises anisotropic etching on the bottom surface of the first opening.
Claim 14:	
[14.PRE]	The method of claim 11, wherein forming the first spacer on the sidewall of the first opening comprises:
[14.A]	forming a plurality of shallow recesses by removing parts of the sacrificial layers abutting the sidewall of the first opening;
[14.B]	depositing a dielectric layer filling in the shallow recesses and on the sidewall and a bottom surface of the first opening; and

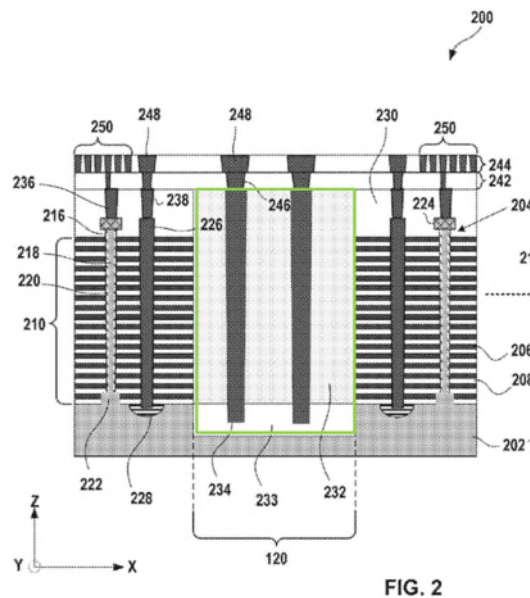
Ref. #	Listing of Challenged Claims
[14.C]	removing part of the dielectric layer that is deposited on the bottom surface of the first opening.
Claim 15:	
[15]	The method of claim 14, wherein the removal of the part of the dielectric layer comprises isotropic etching on the sidewall and the bottom surface of the first opening.
Claim 17:	
[17]	The method of claim 11, wherein the dielectric layers in the dielectric/sacrificial layer pairs comprise silicon oxide, the sacrificial layers in the dielectric/sacrificial layer pairs comprise silicon nitride, and the first and second spacers comprise silicon oxide.
Claim 18:	
[18.PRE]	A method for forming a three-dimensional (3D) memory device, comprising:
[18.A]	forming a stack comprising a plurality of dielectric/sacrificial layer pairs on a substrate;
[18.B]	forming a channel structure extending vertically through the stack;
[18.C]	simultaneously etching a first opening through the stack, a second opening outside of the stack, and a third opening through the stack, wherein a lateral dimension of the third opening is smaller than lateral dimensions of the first and second openings;
[18.D]	depositing a dielectric layer (i) fully filling in the third opening to form a dummy channel structure and (ii) partially filling in the first opening and the second opening;
[18.E]	removing parts of the dielectric layer that are deposited on a bottom surface of the first opening and on a bottom surface of the second opening;

Ref. #	Listing of Challenged Claims
[18.F]	depositing a conductor layer (i) filling in the first opening to form a through array contact (TAC) and (ii) filling in the second opening to form a peripheral contact; and
[18.G]	after forming the TAC and peripheral contact, forming a slit extending vertically through the stack.
Claim 20:	
[20]	The method of claim 18, further comprising prior to etching the first, second, and third openings, forming a staircase structure at one side of the stack.

I. INTRODUCTION

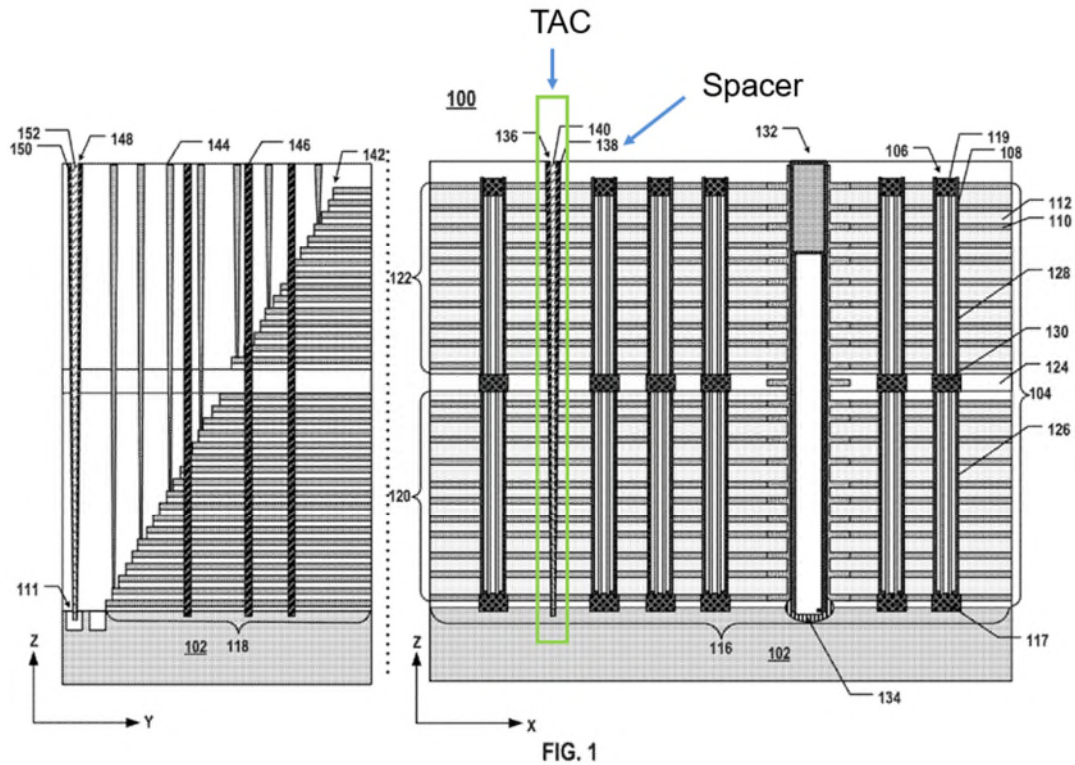
Petitioner Micron Technology, Inc. (“Petitioner”) respectfully requests *inter partes* review of claims 1-15, 17-18, and 20 (the “Challenged Claims”) of U.S. Patent No. 10,879,254 (Ex. 1001, the “’254 Patent”) assigned to Yangtze Memory Technologies Co., Ltd (“Patent Owner” or “PO”).

The ’254 Patent relates to three-dimensional (3D) memory devices with “through array contacts” (“TACs”). The ’254 Patent alleges that there are issues with forming TACs through a “barrier structure.” Ex. 1001, 4:55-5:20. The below depicts such a barrier structure, i.e., a large oxide rectangular block:



Ex. 1007 (U.S. Pat. 10,658,378), Fig. 2¹. Instead of a barrier structure, the ’254 Patent teaches employing a thin spacer (138) for each TAC.

¹ Annotations added throughout unless noted.



Ex. 1001, Abstract, 4:55-5:20, Fig. 1. In addition, the '254 Patent teaches forming a slit (element 132 above)—a structure that was textbook material—*after* forming the TAC. The slit extends in the y-direction (into the page or screen) and can separate the array into blocks.

Claim 1 is representative. It recites forming a stack of alternating dielectric and sacrificial gates—a basic building block of 3D NAND devices. It then recites the basic manufacturing steps of forming a TAC: (1) forming an opening, (2) forming a spacer on the sidewall, and (3) forming the TAC by filling the remaining hole with conductive material. Finally, after forming the TAC, it recites forming a slit. The file history includes no substantive Office Actions. But the Notice of

Allowance suggests this final temporal requirement was the alleged point of novelty.

See §VI.

The Petition demonstrates that TACs with a spacer were, in fact, well known in the prior art. What's more, it was known to form slits **after** forming such TACs. The Petition relies on one primary reference: Nakajima. Nakajima was not in front of the Examiner.

Just like the '254 Patent, Nakajima discloses TACs (C4s) that do not extend through a barrier structure:

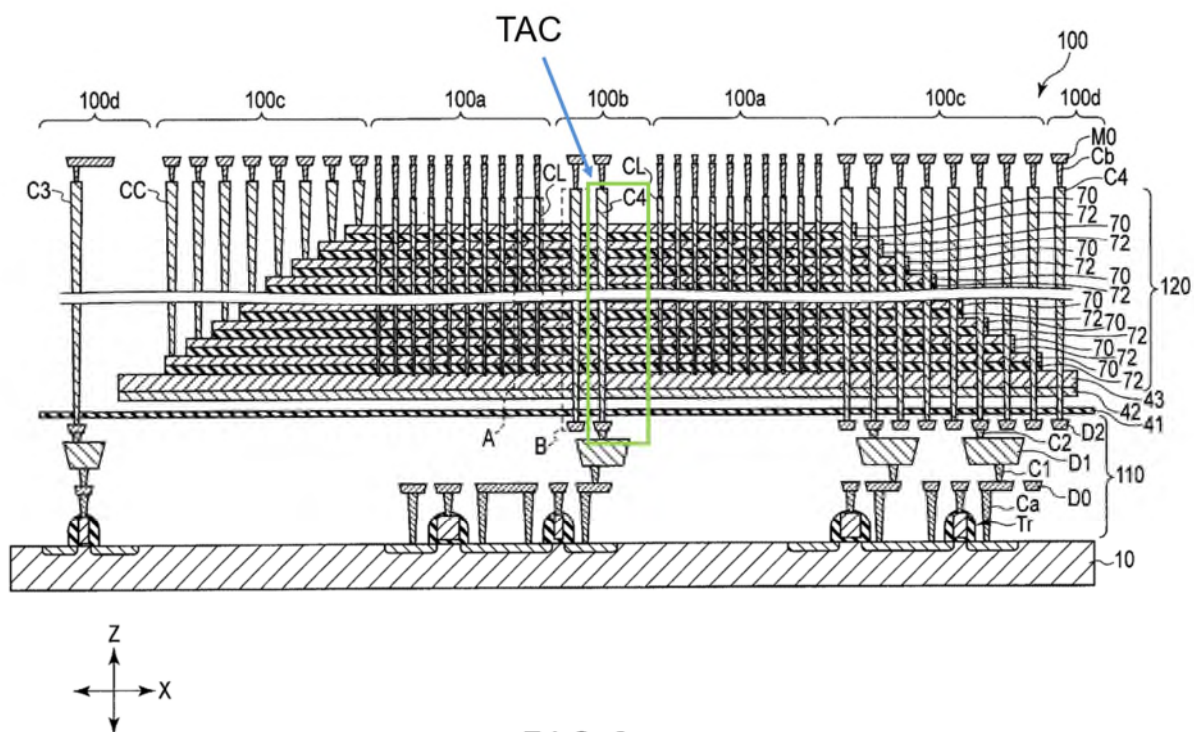
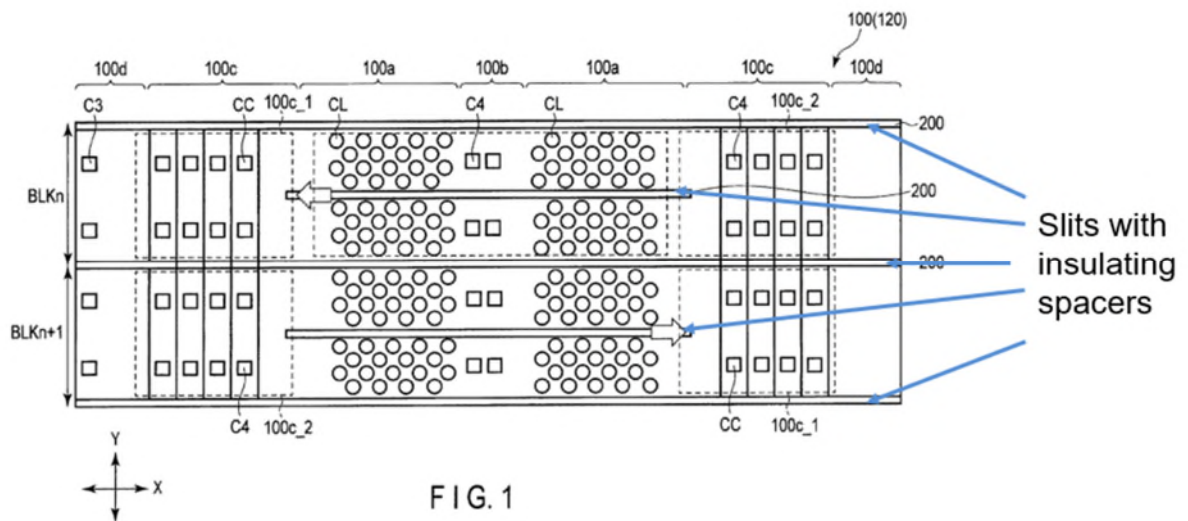


FIG. 2

Ex. 1005 (“Nakajima”), Fig. 2. And Nakajima discloses the exact same steps to form the TAC: “[a] hole H1 extending in the Z-direction is formed Next, . . .

The silicon oxide layer 81 is conformally formed along the bottom and the side surface of the hole H1. . . . Next, the metal layer 82 is formed on the inner surface of the silicon oxide layer 81 in the hole H1.” *Id.*, 7:8-65.

What’s more, immediately after forming the TACs, Nakajima discloses: “***Next, although not shown in the drawing, slits are formed*** in the layer stack 120.” *Id.*, 8:11-8:15.² The slits (and C4 TACs) are shown in a different figure:



Nakajima, Fig. 1.

The dependent claims simply recite (1) additional basic, well-known 3D NAND structures, e.g., dummy channels, and (2) additional basic, well-known 3D NAND manufacturing steps, e.g., forming two holes at once and atomic-layer

² Emphasis added throughout unless noted.

deposition. Some of these features are taught by Nakajima, while the rest were well within the knowledge of a POSITA.

Petitioner requests that the Board institute trial and find the Challenged Claims unpatentable under §103.

II. MANDATORY NOTICES

A. Real Party-in-Interest

Petitioner Micron Technology, Inc. and its subsidiaries, including Micron Consumer Products Group LLC, are the real-parties in interest.

B. Related Matters

According to USPTO assignment records, the '254 Patent is currently assigned to Yangtze Memory Technologies, Co., Ltd. ("YMTC" or "PO"). On July 12, 2024, YMTC asserted the '254 Patent and U.S. Patent Nos. 10,672,711, 10,879,164, 10,886,291, 11,101,276, 11,145,666, 11,450,604, 11,482,532, 11,568,941, 11,581,322, and 12,010,838 against Micron (the "YMTC2 case"). On August 21, 2024, the litigation was consolidated with *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC*, Case No. 3:23-cv-05792-RFL (N.D. Cal., filed November 9, 2023) ("Co-Pending Litigation").

In addition to this Petition, Petitioner is filing (or has filed) petitions for *inter partes* review of each asserted patent in the Co-Pending Litigation:

Petition for *Inter Partes* Review of U.S. Patent No. 10,879,254

Patent	PTAB Proceeding	Wave
10,658,378 (claims 15-17 and 19-20)	IPR2024-00788	Wave 1 Petitions
10,861,872 (claims 1-6 and 11-13)	IPR2024-00789	
10,868,031	IPR2024-00790	
10,937,806 (claims 8-9 and 11-12)	IPR2024-00791	
10,950,623	IPR2024-00794	
11,468,957	IPR2024-00792	
11,501,822	IPR2024-00795	
11,600,342 (claims 1-6 and 8-20)	IPR2024-00793	
10,658,378 (claims 1-7 & 18)	IPR2024-00909	Wave 2 Petitions
10,861,872 (claims 7-10)	IPR2024-00910	
10,937,806 (claim 10)	IPR2024-00911	
11,600,342 (claim 7)	IPR2024-00912	
10,672,711	IPR2025-TBD	Wave 3 Petitions
10,879,164	IPR2025-TBD	
10,879,254	IPR2025-00034	
10,886,291	IPR2025-TBD	
11,101,276	IPR2025-TBD	
11,145,666	IPR2025-TBD	
11,450,604	IPR2025-00035	
11,482,532	IPR2025-TBD	
11,568,941	IPR2025-TBD	

Patent	PTAB Proceeding	Wave
11,581,322	IPR2025-TBD	
12,010,838	IPR2025-TBD	

The Director and the Board should allow this Petition under 35 U.S.C. §314(a), 35 U.S.C. §325(d), and/or 37 C.F.R. §42.108(a).

C. Counsel, Service, and Fee Information

Petitioner designates the following counsel:

Lead Counsel	Back-Up Counsel
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Petitioner consents to service by electronic mail at the following addresses:

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PTABDocketJ3B3@orrick.com, and Micron-YMTC_ohs@orrick.com. Pursuant to 37 C.F.R. §42.10(b), Petitioner's Power of Attorney is attached.

The USPTO is authorized to charge the fee specified by 37 C.F.R. §42.15(a), and any other required fees, to Deposit Account No. 15-0665.

III. REQUIREMENTS FOR *INTER PARTES* REVIEW

A. Grounds for Standing

Petitioner certifies that the '254 Patent is available for IPR, and that Petitioner is not barred or estopped from requesting this IPR. Petitioner was served with a complaint alleging infringement of the '254 Patent on July 12, 2024. This Petition was filed within 1 year of this date.

B. Identification of Challenge and Statement of Precise Relief Requested

Petitioner requests *inter partes* review of claims 1-15, 17-18, and 20. This Petition is supported by the accompanying Declaration of Dr. Jack C. Lee (Ex. 1003 ("Lee")), a leading expert in the 3D NAND field.

This Petition assumes that the '254 Patent is entitled to its earliest listed priority date: the August 21, 2018, PCT filing. Ex. 1001, Cover, p. 2.

Petitioner relies on the following primary reference:

(1) U.S. Patent No. 10,777,501, Nakajima (Ex. 1005). Nakajima was filed on July 3, 2018, and is prior art under at least AIA §102(a)(2). Nakajima, Cover.

Petitioner challenges the claims on the following ground:

Ground	Claim(s)	Prior Art Asserted
1	1-15, 17-18, and 20	Obvious under §103 based on Nakajima and the knowledge of a POSITA

Nakajima was not cited or discussed during prosecution of the '254 Patent.

IV. INSTITUTION SHOULD BE GRANTED

Petitioner has established a reasonable likelihood of success on the merits. All other requirements for IPR have been met. The Board should institute IPR.

A. There are No Grounds for a §314 Discretionary Denial in this Case

There is a pending district court action involving the '254 Patent. The PTAB has explained that it “will not ... discretionarily deny institution in view of parallel district court litigation where a petition presents compelling evidence of unpatentability.” 6/21/22 Interim Procedure, 2, 4-5. Petitioner submits that it presents a compelling case here: the claims of the '254 Patent are unambiguously unpatentable.

Petitioner also notes that the factors considered by the Board when assessing whether to institute IPR in light of a parallel proceeding collectively weigh in favor of institution. *See Apple Inc. v. Fintiv, Inc.*, Case No. IPR2020-00019, Paper No. 11 (Mar. 20, 2020) (precedential). In particular: the district court may stay the case, any potential trial will occur years from now, little district court work has occurred, petitioner diligently prepared this petition, and the petition is substantively strong.

1. Possibility of a Stay

Petitioner intends to seek a stay if the Board institutes IPR. Until this issue is adjudicated, any attempt to predict the outcome would require speculation. This factor is neutral. *See Sand Revolution II, LLC v. Continental Intermodal Grp. – Trucking LLC*, IPR2019-01393, Paper 24, 7 (PTAB June 16, 2020) (informative); *Fintiv*, 6-9, 12 (similar).

2. Proximity of the Court’s Trial Date

On September 18, 2024, the district court entered a scheduling order which set a trial date of June 15, 2026. *See* Ex. 1033. As a result, if IPR proceedings are instituted, they should be completed before the scheduled trial date. *See also* Ex. 1034 (statistics indicating that it takes on average 48.9 months to reach trial in district court). This weighs strongly in favor of institution.

3. Investment in the Parallel Proceeding

Regarding the Co-Pending Litigation, to date, the parties and the district court have invested very little in the parallel proceeding. Indeed, beyond engaging in some motion practice regarding the pleadings and consolidation, little substantive progress has been made. *See* §II.B. Virtually no progress has been on the Wave 3 patents (which includes the '254 Patent). The parties are over a month away from completing the exchange of contentions for the Wave 3 patents (from the YMTC2 case) and have not taken any depositions in the entire Co-Pending Litigation. Fact discovery is in its infancy. No claim construction positions have been exchanged

for the Wave 3 patents, no claim construction order has issued, no infringement or invalidity expert discovery has occurred, and no summary judgment motions have been filed. This weighs in favor of institution. *See Sand Revolution*, 10-11.

The Board also has explained that institution is appropriate where “the petitioner filed the petition expeditiously....” *Fintiv*, 11. Here, on July 12, 2024, PO asserted eleven Wave 3 patents against Petitioner—asserting 149 claims for the Wave 3 patents. Ex. 1035. Petitioner proceeded with diligence, starting the filing of eleven petitions approximately three months after being served with the YMTC2 complaint. Ex. 1036. This also weighs strongly in favor of institution.

4. Issue Overlap

Should the Board institute, Micron stipulates that it will not advance in District Court on any ground asserted in this Petition. Micron submits that this eliminates any potential overlap in issues between the proceedings here and in District Court. The Board has found that such stipulations weigh in favor of institution. *Sand Revolution*, 11-12.

5. Party Overlap

Both Petitioner and Patent Owner are parties in the parallel proceeding. This, however, is of little moment as there is often party overlap when there is a parallel proceeding.

6. Other Circumstances

Here, Petitioner submits that its petition has significant substantive merit. It

is premised on clear, understandable prior art that the Patent Office did not previously consider. Thus, this factor also weighs in favor of institution.

B. Denial Under §325(d) Would Be Inappropriate

The Examiner did not consider Nakajima, and thus denial under §325(d) would be inappropriate. Moreover, the '254 Patent's apparent point of novelty is forming the slits after the TACs. *See* §VI. Nakajima discloses exactly that. *See* §IX.A.

V. TECHNOLOGY BACKGROUND

The '254 Patent relates to three-dimensional (3D) NAND flash memory. “NAND” flash memory is a particular type of flash memory where cells form a structure similar to that of a NAND (not-AND) logic gate. Ex. 1008, 14. At the core of a NAND flash memory is a “memory cell,” which stores information as electrical charge. Lee, ¶¶ 39-43.

Initially, a NAND flash memory was “planar,” that is, two-dimensional (2D). In 2D NAND flash memory, all memory cells lie on a 2D plane (*i.e.*, the x-y plane) on the surface of a memory chip as shown below:

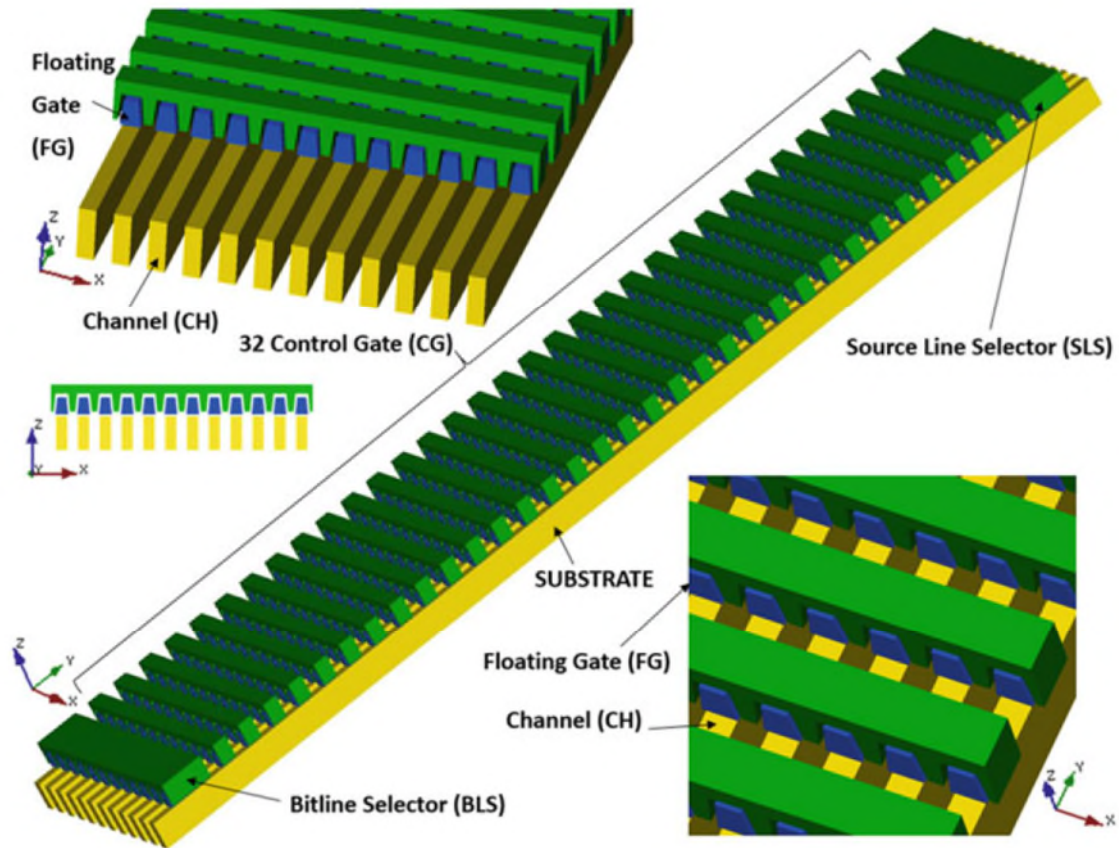


Fig. 3.9 Bird's-eye view of a planar NAND string

Ex. 1008, 86; Lee, ¶ 44.

Well before the priority date of the '254 Patent, Petitioner and others had developed techniques for manufacturing 3D NAND flash memory. In a 3D NAND flash memory, memory cells exist in vertical, cylindrical NAND flash “strings”:

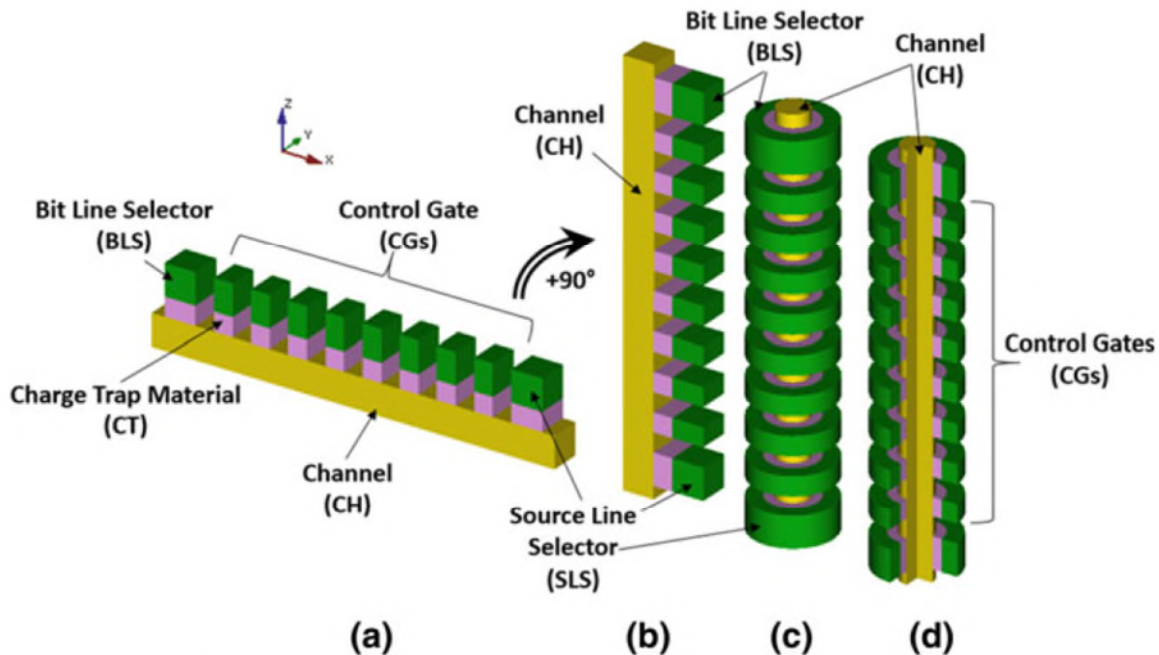


Fig. 4.1 NAND Flash string with horizontal gate and vertical channel: **a** planar, **b** planar rotated by 90°, **c** vertical channel with cylindrical shape and **d** its cross section

Ex. 1008, 102. As labeled in Figure 4.1, above, each NAND string includes a “cylindrical channel.” Ex. 1008, 58; Lee, ¶¶ 45-48.

A number of architectures for constructing a memory device out of NAND strings were known in the art. For example, in the well-known BiCS (Bit Cost Scalable) architecture, various “contacts,” that is, electrical connections, are on top of the memory array. These include source line contacts (for providing a ground connection to the memory cells):

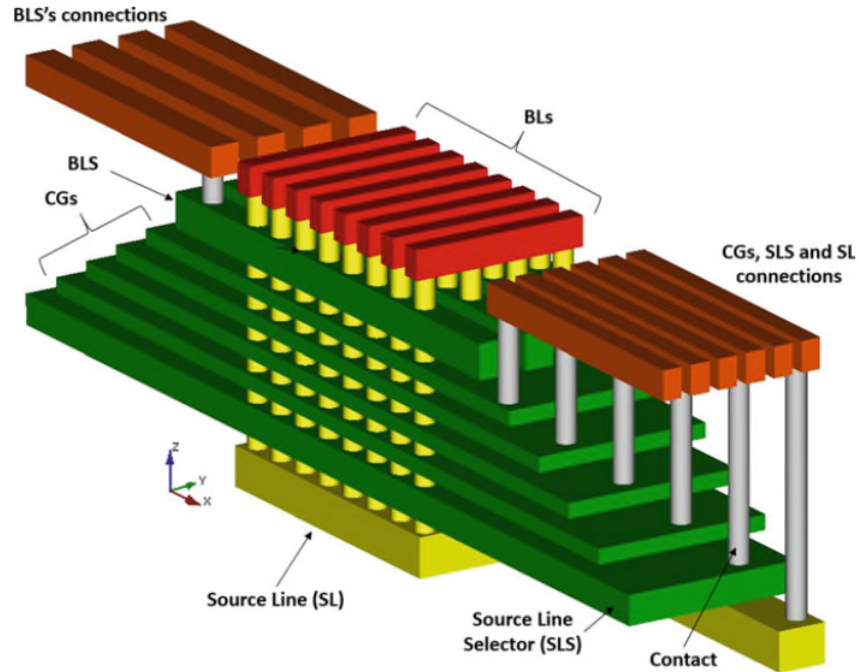


Fig. 4.13 Top bird's eye view of BiCS with gate connections

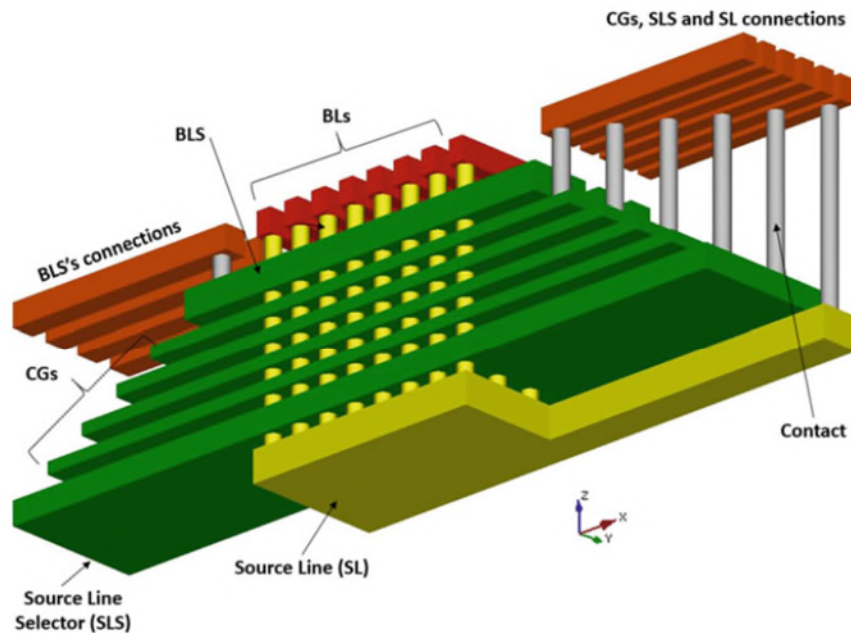


Fig. 4.14 Bottom bird's-eye view of BiCS with gate connections

Ex. 1008, 109-110; Lee, ¶ 49. The above illustrates source line contacts that extend from the top of the device to the bottom, but do not travel through the stack. It was

well known, however, to form such contacts directly through the memory stack. The below provides several examples:

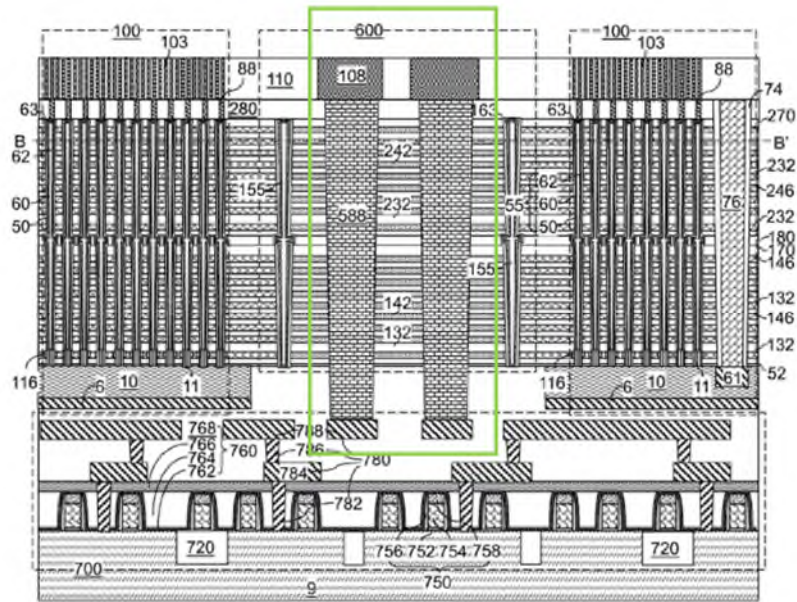


FIG. 69A

Ex. 1009 (U.S. Pat. Pub. 2017/0179026, Toyama), Title (“Through-Memory-Level Via Structures”), [0367], Fig. 69A (588).

array contacts through the array. *E.g.*, Ex. 1012 (WO 2019/042103) (Fig. 2, 248) and Ex. 1013 (U.S. Pat. 10,679,721), Fig. 1 (110), Abstract (“TAC”); Lee, ¶¶ 50-51.

The memory cells’ control gates form a staircase structure as shown below:

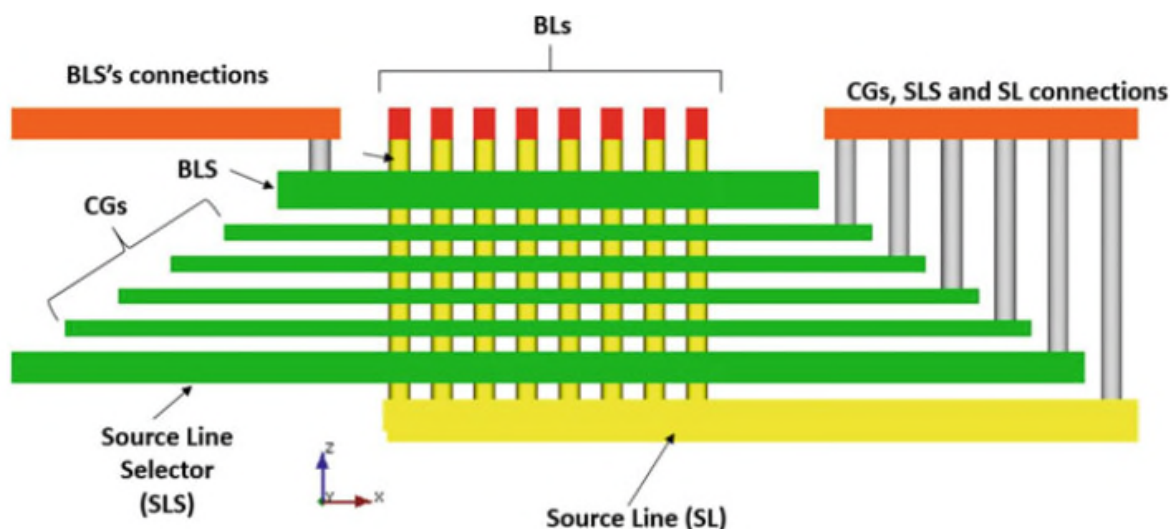


Fig. 4.12 Vertical cross section of BiCS with gate connections

Ex. 1008, 109 (green control gates forming a staircase). Each control gate delivers a control signal to a number of memory cells at the same horizontal level in the 3D NAND memory device. The memory cells that a single control gate controls are together a “word,” and the control gate is a “word line.” Ex. 1014 (Aritome), 38-40. Reflecting this, the grey columns contacting the top surface of the control gates (shown above in green) are “word line contacts.” Lee, ¶¶ 52-53.

Various modifications to the BiCS structure were known, including the use of slit structures, which extend vertically through the memory stack and extend laterally through the device, to serve as source line contacts for the NAND strings. As can be seen, these slits also segment the array into blocks:

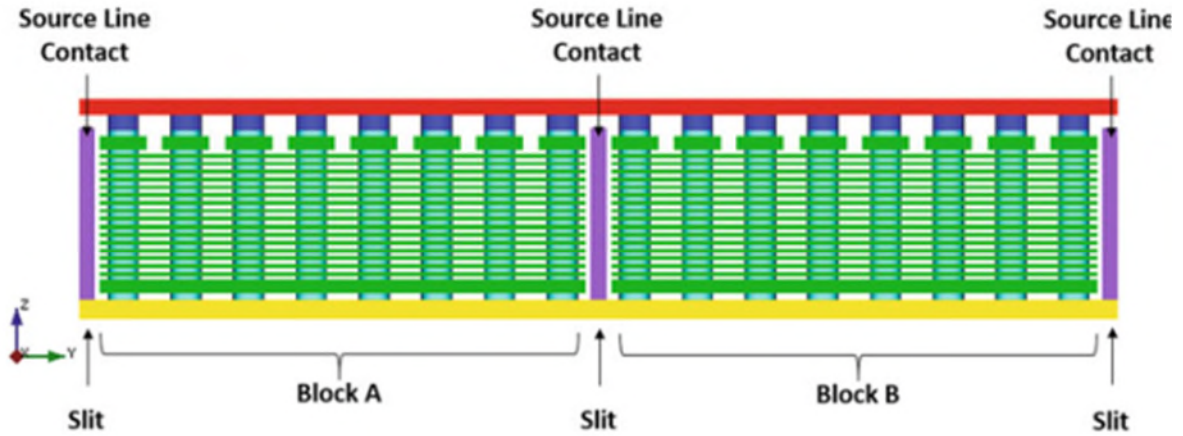


Fig. 6.8 Side view of Fig. 6.7

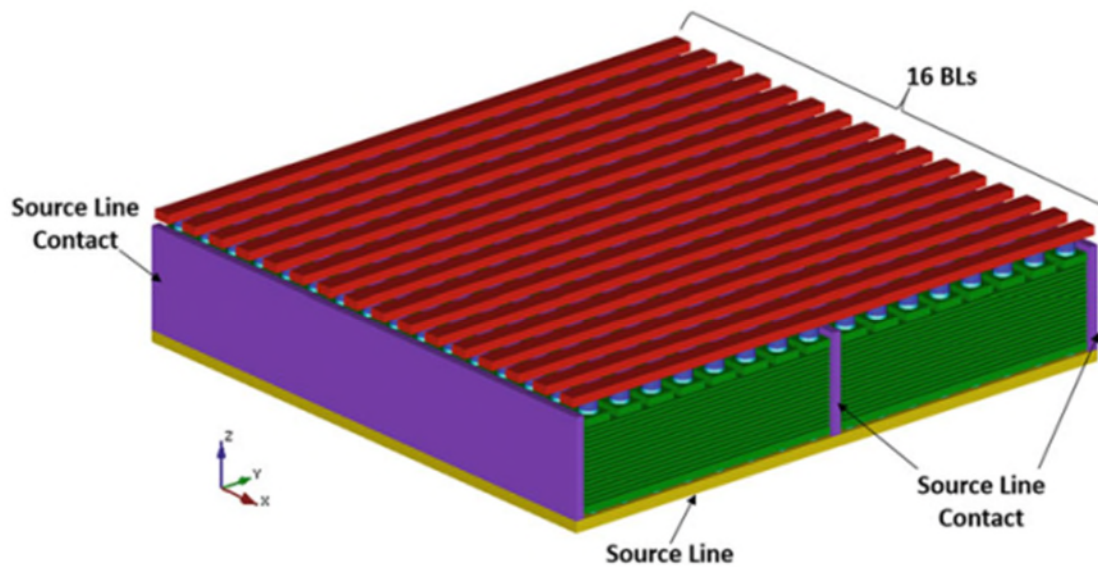


Fig. 6.7 Array slits

Ex. 1008, 185.

In each of the above figures, there are various gaps between the depicted structures. In a real 3D NAND memory device, these gaps are not merely empty space, but instead are filled with an insulating material (also known as a “dielectric”). One purpose of the dielectric is to prevent electrical signals from one conductive

structure from interfering with the electrical signals in other structures. Another purpose of the dielectric is to provide structural support to prevent the conductive structures from collapsing. The stack of alternating gate layers (wordlines) and insulating layers is known as the memory stack. Lee, ¶¶ 54-58.

In sum, techniques for manufacturing 3D NAND memory stacks, TACs, and slits were well-known in the art before the '254 Patent's priority date. Lee, ¶ 59.

VI. THE '254 PATENT AND ITS PROSECUTION HISTORY

The '254 Patent is entitled “Three-dimensional memory devices having through array contacts and methods for forming the same” and primarily relates to “through array contacts” in a 3D memory device. As the title indicates, the '254 Patent refers to contacts that extend through the memory stack as “through array contacts” (“TACs”). Ex. 1001, 8:28-60. The '254 Patent alleges there are issues with forming TACs through a “barrier structure.” *Id.*, 4:55-5:20. The '254 Patent does not depict a barrier structure (or a barrier structure with TACs). But a “barrier structure” appears to refer to rectangular block of oxide, i.e., after etching out a rectangular area of the stack, filling that void with oxide (providing an insulating structure for pure conductive core TACs) to form the barrier structure. Such a structure from another YMTC patent (the assignee of the '254 Patent) is shown below:

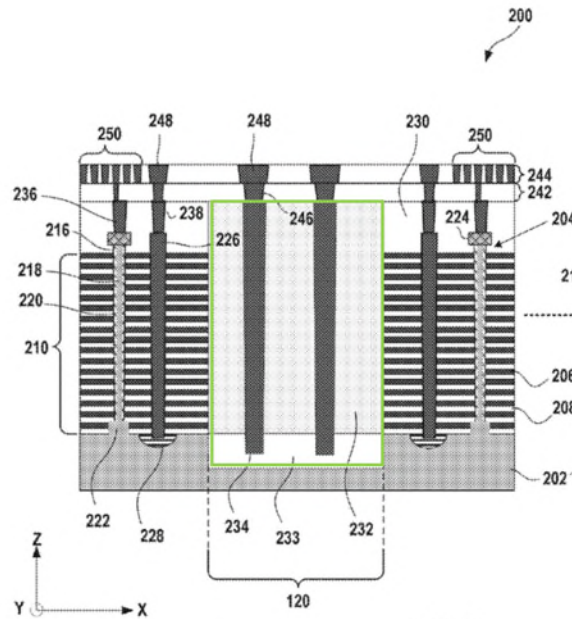


FIG. 2

Ex. 1007 (U.S. Pat. 10,658,378), Fig. 2 (120). As an alternative, the '254 Patent teaches employing a thin spacer (138) for each TAC.

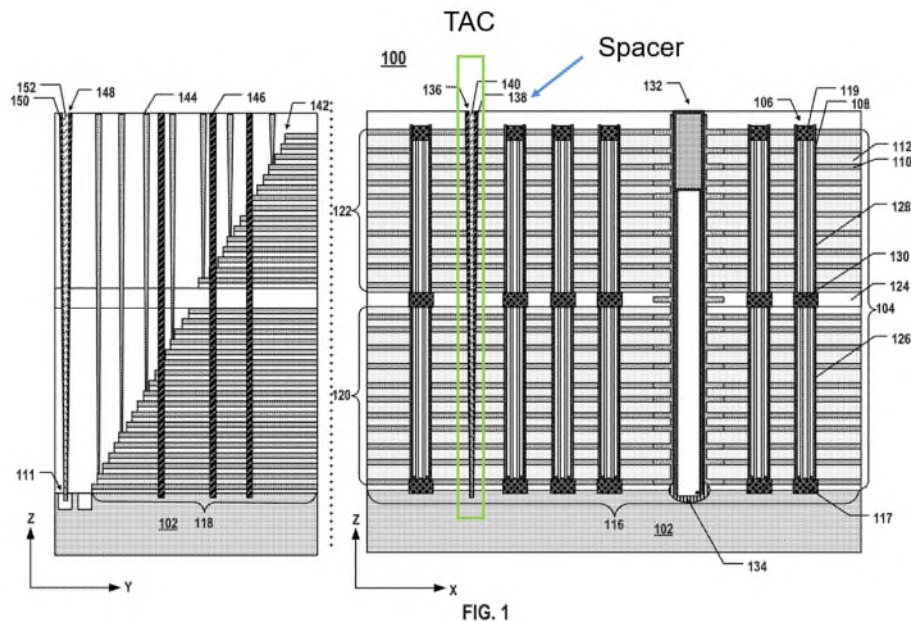
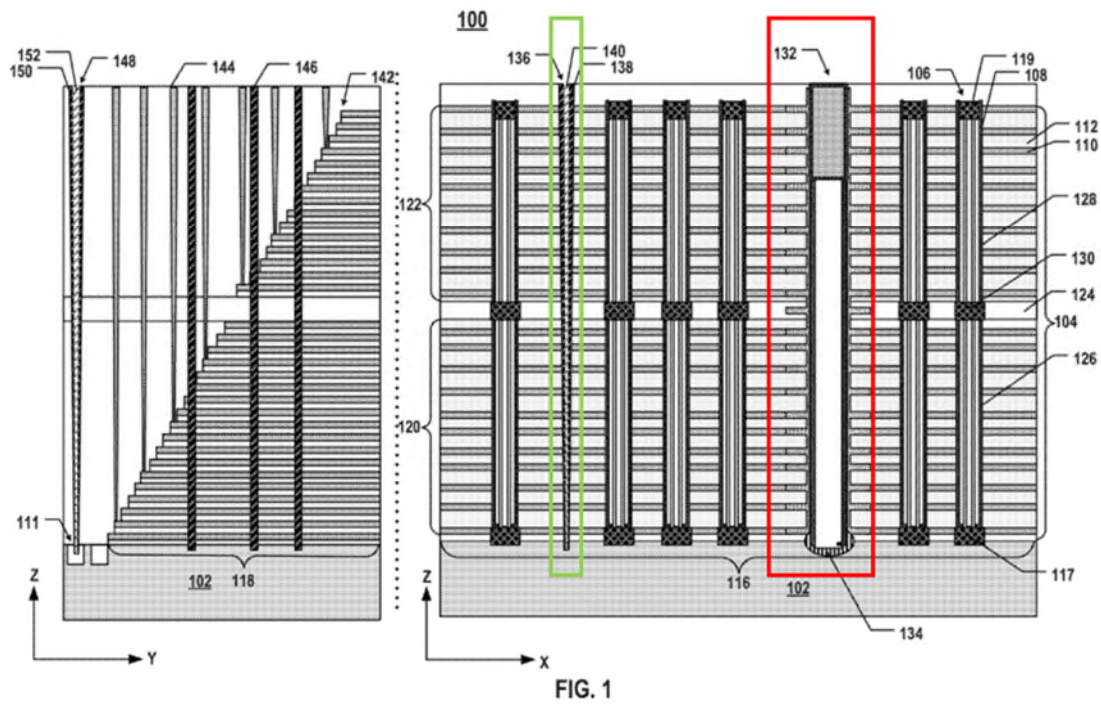


FIG. 1

Ex. 1001, Abstract, 4:55-5:20. The TACs include a dielectric spacer (138) to insulate the TAC from the memory stack (e.g., the conductive gate layers) and a

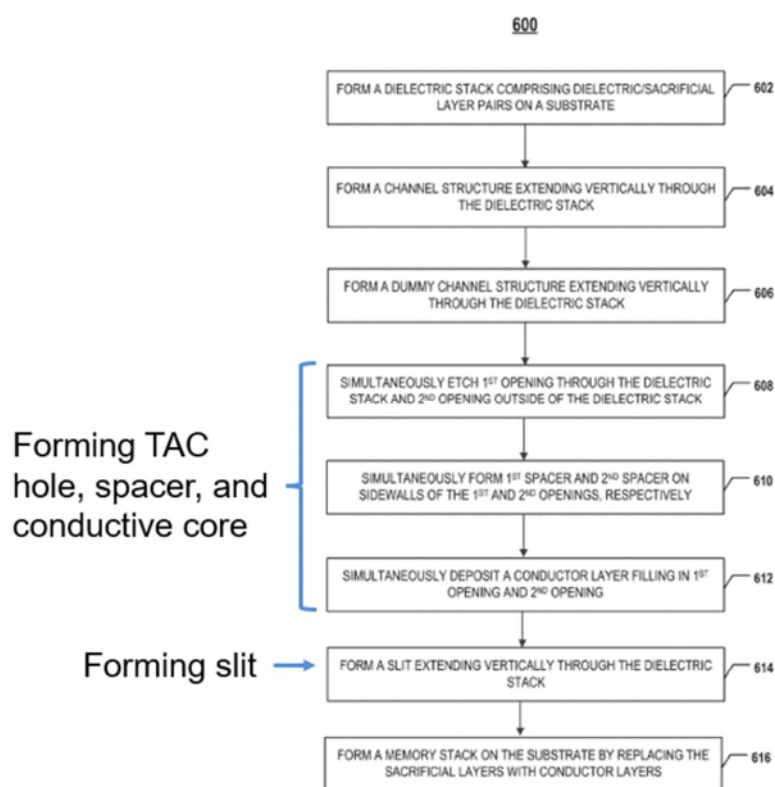
conductive core (140). *Id.*, 8:45-60. The conductive core enables the TAC to connect devices above and below the array. *Id.*, 4:55-59. But as §V discusses, contacts that travel through the memory stack—with a spacer instead of a barrier structure—were well known. Lee, ¶¶ 62-64.

As the below file history summary demonstrates, the '254 Patent's alleged point of novelty appears to be forming a slit *after* the TACs. Indeed, the Abstract highlights this timing requirement—which is a limitation of each independent claim. Ex. 1001, Abstract. Like TACs, slits were well known. *See* §V. Shown below in red, the slit structure (which fills the open slit) can include a conductor core and dielectric spacer, and thereby interconnect a source voltage (above the array) to a common source in the substrate (below the array). Ex. 1001, 8:1-27. The slit can extend laterally (in the Y-direction, into the page) and therefore segment the array into blocks. *Id.* The slit (while a void) can be used in the gate replacement process to replace the sacrificial gates with conductive gates. *Id.*, 14:44-62.



Id., Fig. 1; Lee, ¶ 65-66.

Figure 6 depicts the process flow and illustrates that the '254 Patent describes forming the slits ***after*** forming the TACs:



Ex. 1001, Fig. 6; *see also id.*, Fig. 3B, 12:24-63 (forming TACs holes), Fig. 3C-E, 12:64-14:19 (various ways to form spacer), Fig. 3F, 14:20-43 (forming conductive core for TAC), Fig. 5A, 14:44-15:12 (forming slit), Fig. 5A, 15:12-24 (filling slit); Lee, ¶¶ 66-67.

There were no substantive Office Actions in the '254 Patent's file history (only approval of a terminal disclaimer on 10/12/2020) or in the file history of the '254 Patent's parent application. On 10/26/2020, the claims were allowed, and the Notice of Allowance indicates that the alleged point of novelty is "forming a spacer on a sidewall of the first opening; forming a through array contact (TAC) extending

vertically through the stack by depositing a conductor layer over the spacer in the first opening; and after forming the TAC, forming a slit extending vertically through the stack.” Ex. 1002, 133-34; Lee, ¶ 68.

VII. CLAIM CONSTRUCTION

For purposes of this Petition, Petitioner submits that the terms of the ’254 Patent’s claims do not require further construction and should receive their plain and ordinary meaning. Lee, ¶¶ 69-72.

VIII. LEVEL OF ORDINARY SKILL IN THE ART

A POSITA in the field of the ’254 Patent would have had a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) monolithic 3D structures and NAND memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience). This POSITA would have been aware of and generally knowledgeable about 3D NAND’s structure, how it is manufactured, and its component parts. Lee, ¶¶ 34-38.

IX. DESCRIPTION OF THE PRIOR ART

A. Nakajima

Just like the alleged point of novelty of the ’254 Patent, Nakajima discloses forming a TAC through the memory stack and then forming the slit.

Nakajima refers to its TACs as “C4”: “The contact area 100*b* includes contacts C4. A contact C4 couples an interconnect in an upper layer of the layer stack 120 and an interconnect in a lower layer of the layer.” Nakajima, 2:66-3:2.

Nakajima discloses: “A process of manufacturing the contact C4 will be described below. ... [a] hole H1 extending in the Z-direction is formed Next, . . . The silicon oxide layer 81 is conformally formed along the bottom and the side surface of the hole H1. Next, as shown in FIG. 10, a portion of the silicon oxide layer 81 that is located at the bottom of the hole H1 is removed Next, the metal layer 82 is formed on the inner surface of the silicon oxide layer 81 in the hole H1 . . . ***Next, although not shown in the drawing, slits are formed*** in the layer stack 120 by the RIE method using a mask layer. The slits penetrate the insulation layers 44 and 64 and the layer stack 120, to reach the polysilicon layer 43.” Nakajima, 7:8-8:15. Lee, ¶¶ 75-77.

The TACs and slits are shown respectively below:

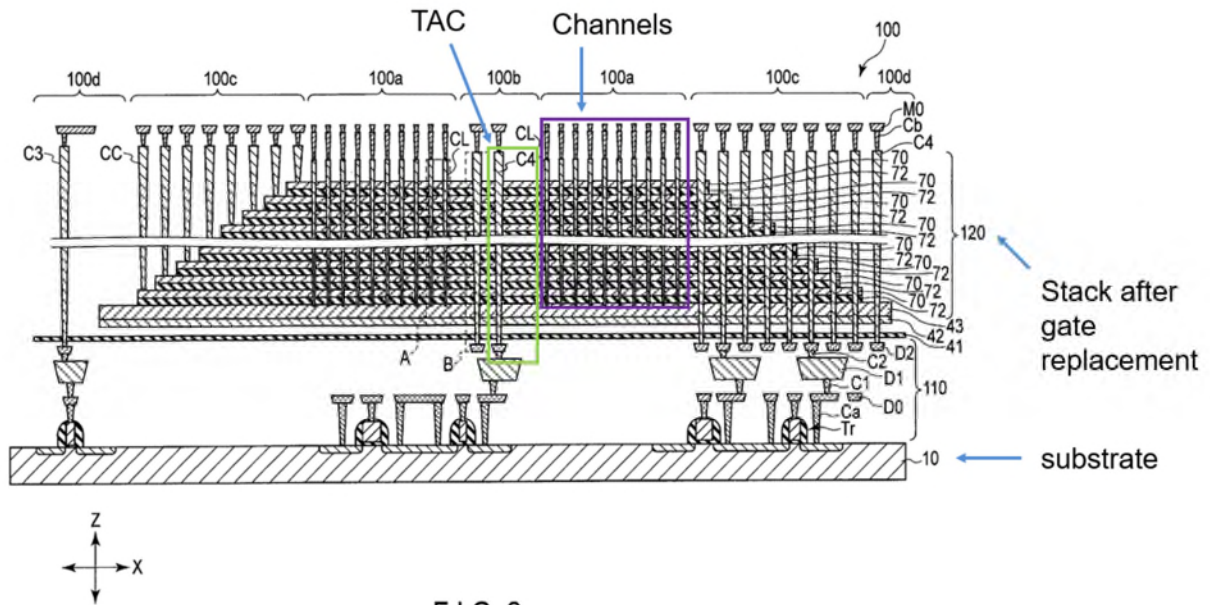


FIG. 2

Nakajima, Fig. 2.

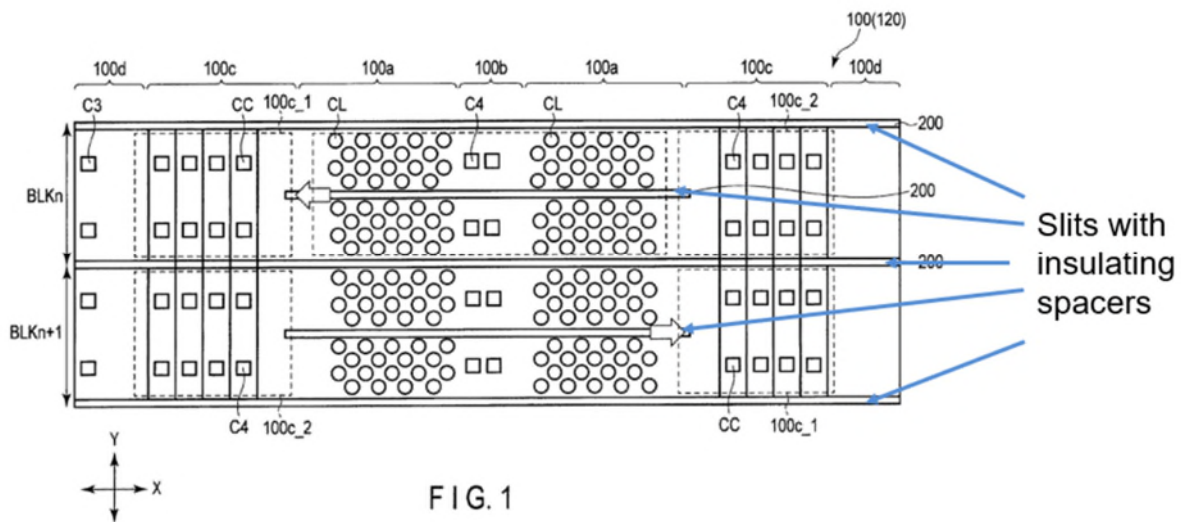


FIG. 1

Id., Fig. 1; Lee, ¶ 77.

X. GROUND 1: NAKAJIMA IN VIEW OF THE KNOWLEDGE OF A POSITA RENDER OBVIOUS CLAIMS 1-15, 17-18, AND 20

A. Claim 1:

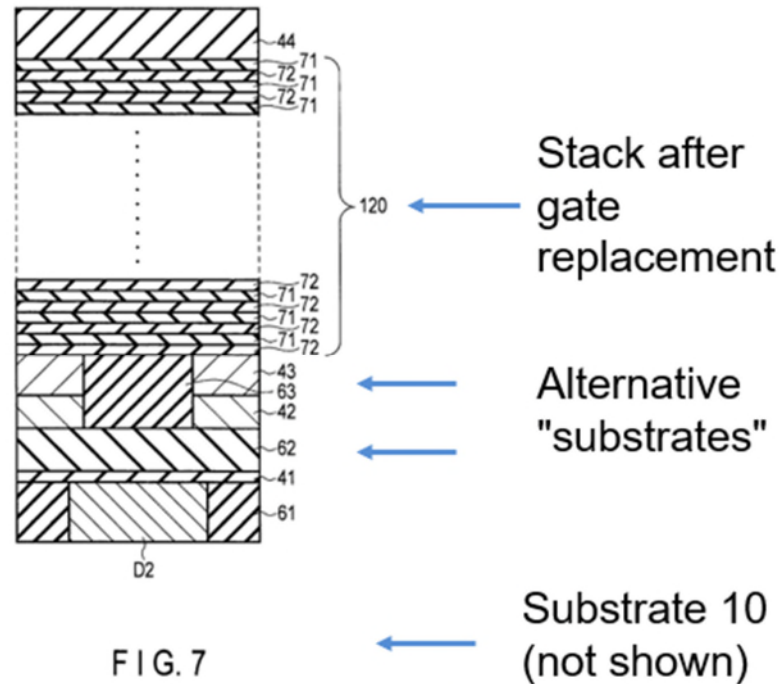
1. [1.PRE] “A method for forming a three-dimensional (3D) memory device, comprising:”

Nakajima discloses a method for forming a three-dimensional (3D) memory device (“semiconductor device 100”). Nakajima, 1:14-16 (“Embodiments described herein relate generally to a semiconductor device and a method of manufacturing the same.”), 2:26-30 (“A semiconductor device 100 ... In this embodiment, a three-dimensionally-stacked type NAND flash memory will be described as an example of the semiconductor device.”), Figs. 6-12, 7:5-9 (describing fabrication). Lee, ¶ 78.

2. [1.A] “forming a stack comprising a plurality of dielectric/sacrificial layer pairs on a substrate;”

Nakajima discloses forming a stack (“layer stack” 120) comprising a plurality of dielectric (“silicon oxide layers” 72)/sacrificial layer (“sacrifice layers 71”) pairs on a substrate (e.g., “substrate 10”).

As an initial matter, note that the ’254 Patent defines “on” broadly: “It should be readily understood that the meaning of ‘on,’ ... in the present disclosure should be interpreted in the broadest manner such that ‘on’ not only means ‘directly on’ something *but also includes the meaning of “on” something with an intermediate feature or a layer therebetween.*” Ex. 1001, 3:52-61. The ’254 Patent also defines

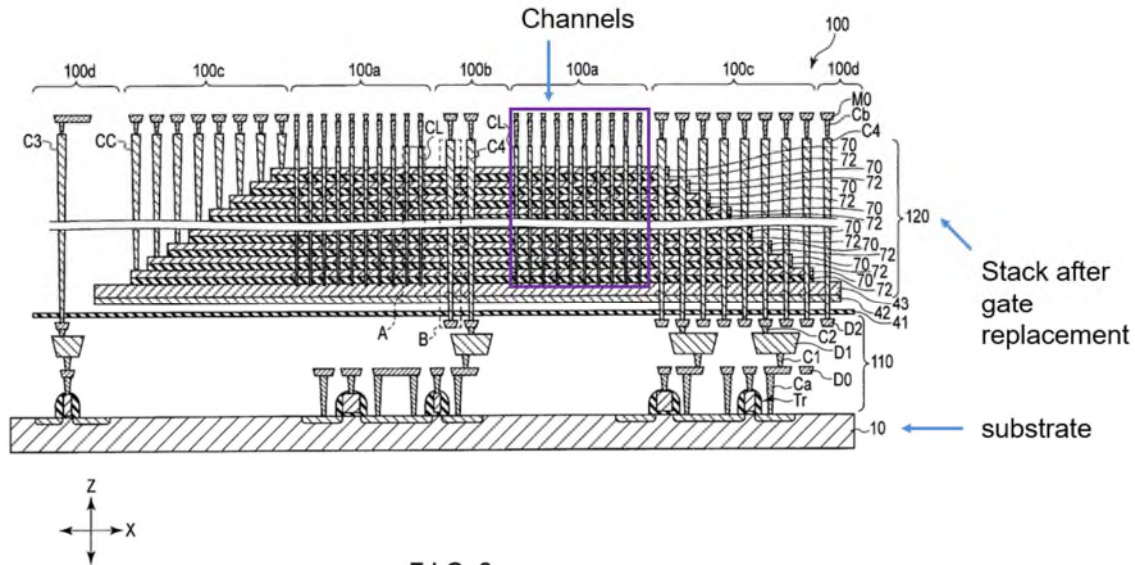


Nakajima, Fig. 7.

3. [1.B] “forming a channel structure extending vertically through the stack;”

Nakajima discloses, or renders obvious, forming a channel structure (a “pillar structure” “CL” 120) extending vertically through the stack (120). Lee, ¶ 83.

First, Nakajima discloses a channel structure, namely, pillar structures CL:



Nakajima, Fig. 2, 5:16-21 (“The pillar structures CL continuously extend in the insulation layer 44 and in the layer stack 120 in the stacking direction (Z-direction). The pillar structures CL include a core layer 50, a semiconductor layer 20, and a memory layer 30, which are provided in the mentioned order from the center.”); Lee, ¶ 84.

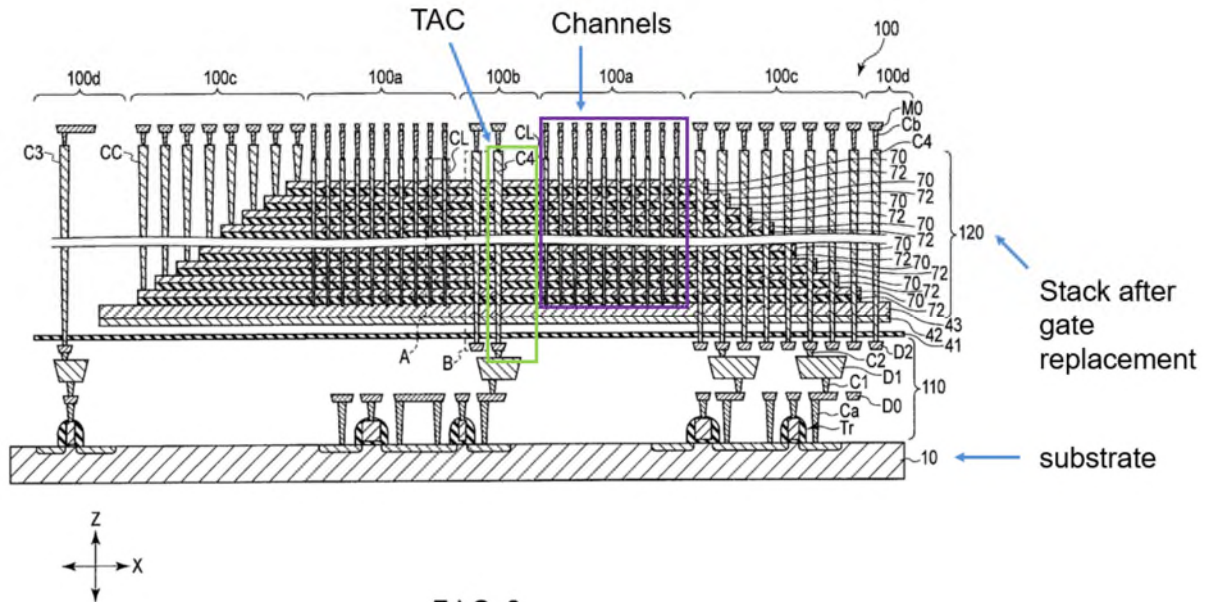
Note that the channel structure extends through the memory stack (120) down to polysilicon layer 43: “**A semiconductor layer 20 is provided around the core layer 50 in a pillar structure CL.** Namely, the semiconductor layer 20 is provided between the core layer 50 and the memory layer 30. The semiconductor layer 20 includes a body layer 20b ... **A lower end of the body layer 20b contacts the polysilicon layer 43.**” Nakajima, 5:26-33; see also *id.*, Fig. 3; Lee, ¶ 85.

To the extent that PO were to argue that forming the channels must occur before the TACs and slits, it would be incorrect, because this limitation does not recite when it occurs (compare the final limitation, which does state a relative time when it occurs). Regardless, Nakajima would have been understood to disclose, and at least renders obvious, forming the channels before the TACs and slits. As claim [9] discusses, it would further be obvious to etch the TACs and dummy holes at the same time. Nakajima focuses on the manufacture of the TACs, and thus starts the description of the manufacturing process there. Nakajima, 7:5-8. There, Nakajima discloses forming the TACs (C4s), forming the slits, and then replacing the sacrificial gates. *Id.*, 7:5-8:23. Nakajima describes that the channel pillars support the structure during the gate replacement process, and thus it would have been understood, and certainly obvious, that Nakajima discloses forming the channels before the TACs (C4) and slits, because the description assumes that the channels have already been made before the C4 structures. *Id.*, 8:24-33; Lee, ¶ 86. Indeed, as the claim [2] analysis demonstrates, it was known, advantageous, and routine to form channels and dummy structures before fabricating the TACs and slits, and performing the gate line replacement process. *See* Claim [2] analysis.

4. [1.C] “forming a first opening extending vertically through the stack;”

Nakajima discloses forming a first opening (H1) extending vertically through the stack (120). Lee, ¶ 87.

As seen in the final memory device (Figure 2), Nakajima discloses contacts C4, to which this and the following two limitation relate.



Nakajima, Fig. 2. Note that the C4 extends through the stack and includes a metal core (“metal layer 82”) and dielectric spacer (“silicon oxide layer 81”). *Id.*, 6:45-52. Lee, ¶ 88.

Regarding the manufacturing of C4, Nakajima discloses forming a first opening (“hole H1”) extending vertically through the stack (120): “[A] hole H1 extending in the Z-direction is formed in the insulation layers 44, 62, and 63, and the layer stack 120, as shown in FIG. 8. The hole H1 is formed by, for example, reactive ion etching (RIE) using a mask layer not shown in the drawing. The hole H1 penetrates the insulation layers 44, 62, and 63, and the layer stack 120, to reach the silicon nitride layer 41.” Nakajima, 7:37-43.

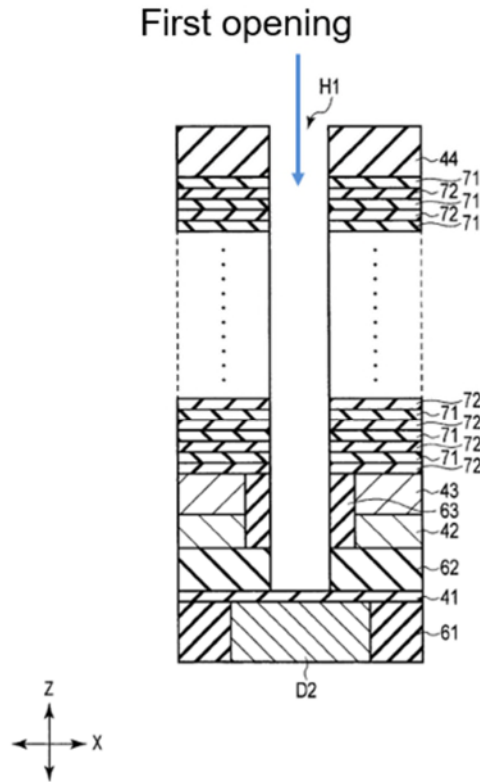


FIG. 8

Id., Fig. 8; Lee, ¶ 89.

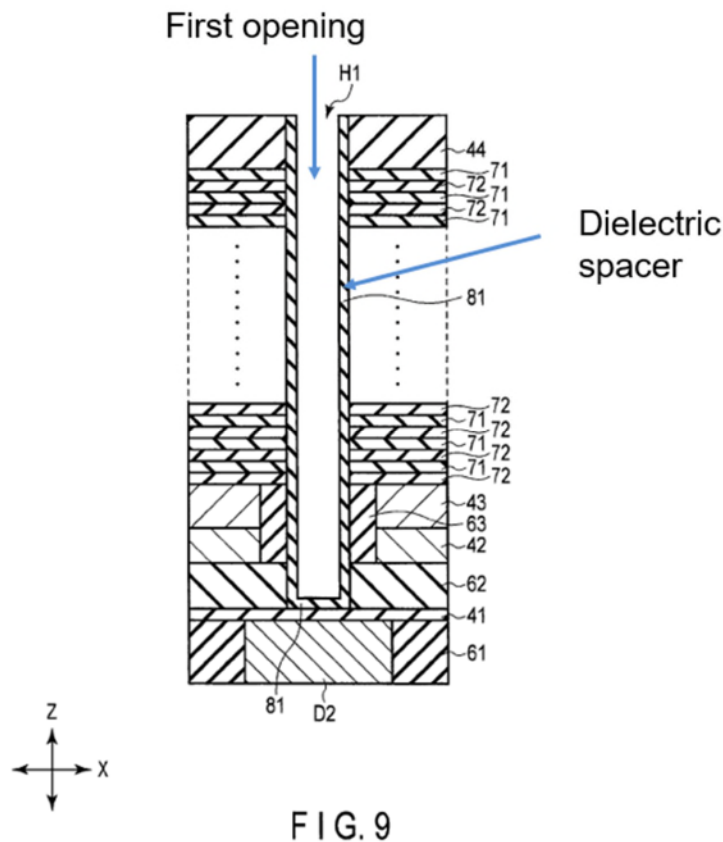
As shown above, and consistent with the C4 structure that fills the hole, the hole extends through the entire stack (layers 71/72) as shown above. Lee, ¶ 89.

5. [1.D] “forming a spacer³ on a sidewall of the first opening;”

Nakajima discloses forming a spacer (“oxide layer 81”) on a sidewall (“inner surfaces”) of the first opening (“hole H1”): “Next, the silicon oxide layer 81 is formed on the inner surfaces of the layer stack 120 and the insulation layers 44, 62,

³ The '254 Patent describes a “spacer” as a dielectric material, e.g., silicon oxide, on the sidewalls of the hole. Ex. 1001, 8:45-60.

and 63 in the hole H1, and on the silicon nitride layer 41, as shown in FIG. 9. The silicon oxide layer 81 is conformally formed along the bottom and the side surface of the hole H1.” Nakajima, 7:44-49; Lee, ¶¶ 90-91.

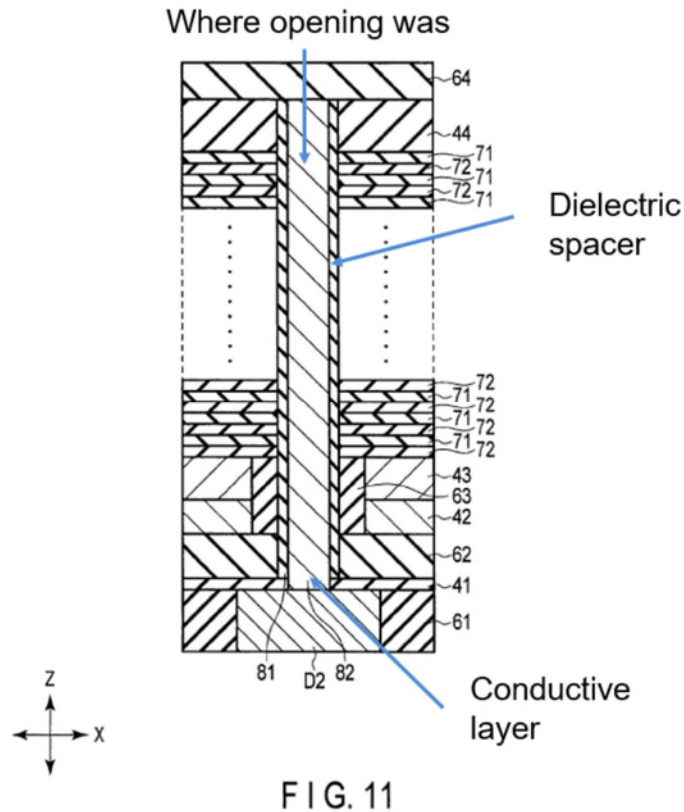


Id., Fig. 9.

6. [1.E] “forming a through array contact (TAC) extending vertically through the stack by depositing a conductor layer over the spacer in the first opening; and”

Nakajima discloses forming a through array contact (TAC) (“C4”) extending vertically through the stack by depositing a conductor layer (“metal layer 82”) over the spacer (“oxide layer 81”) in the first opening (“hole H1”). Recall that the C4

extends through the stack and includes a metal core (“metal layer 82”) and dielectric spacer (“silicon oxide layer 81”). Nakajima, 6:45-52. “[T]he metal layer 82 is formed on the inner surface of the silicon oxide layer 81 in the hole H1.” *Id.*, 7:62-63.



Nakajima, Fig. 11; Lee, ¶¶ 92-93.

Note that the '254 Patent forms the conductive layer “over the spacer” in the same way, i.e., filling a hole with a spacer on the outer walls of the holes. Ex. 1001, Figs. 3E-F, 13:62-64, 14:20-44; Lee, ¶ 94.

Nakajima’s C4 extends through the stack (see above) and interconnects devices that are above and below the stack: “A contact C4 couples an interconnect

in an upper layer of the layer stack 120 and an interconnect in a lower layer of the layer stack 120 with each other.” Nakajima, 2:66-3:2; Lee, ¶ 95.

The limitation [1.F] recites “after forming the TAC, forming a slit,” and this limitation recites “forming the TAC.” Note that to the extent that PO argues that “forming the TAC” must include forming connections thereon, PO is incorrect for at least two reasons. Or put another way, to the extent that PO argues that the claims require forming connections thereon before “forming a slit,” PO is incorrect for at least two reasons. First, the claim language defines the final step of forming the TAC as filling it with a conductive core (“forming a through array contact (TAC) extending vertically through the stack by depositing a conductor layer”). Second, the specification does not describe forming connections on the TAC before forming the slit. Ex. 1001, 14:20-57, Fig. 6 (steps 612, 614); Lee, ¶ 96.

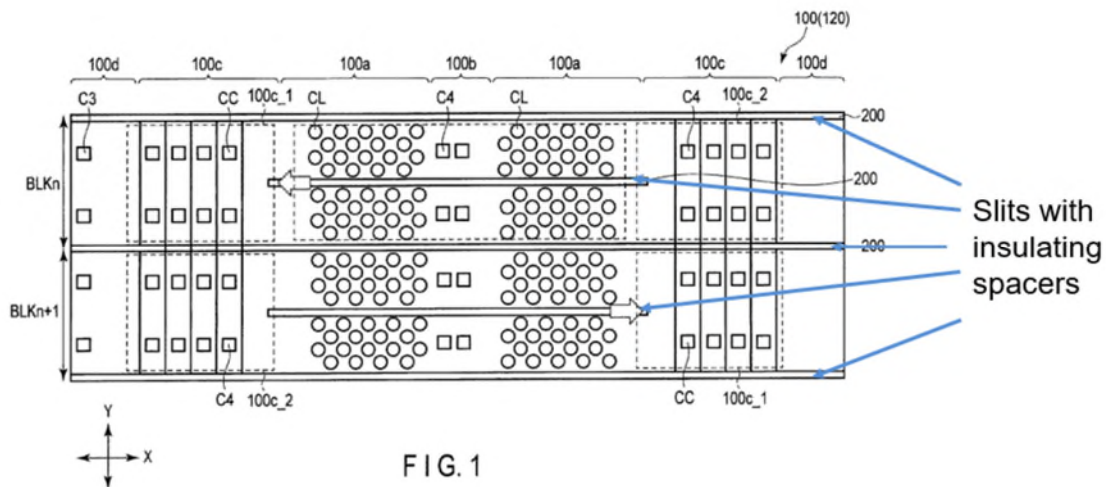
7. [1.F] “after forming the TAC, forming a slit extending vertically through the stack.”

Nakajima discloses after forming the TAC (C4), forming a slit (“slit”) extending vertically through the stack (“layer stack” 120). Lee, ¶ 97.

After forming the TAC (Nakajima, 7:62-65), Nakajima discloses forming slits that extend vertically through the stack, i.e., from above the stack (layer 64) to below the stack (layer 43): “Next, although not shown in the drawing, slits are formed in the layer stack 120 by the RIE method using a mask layer. The slits penetrate the

insulation layers 44 and 64 and the layer stack 120, to reach the polysilicon layer 43.” Nakajima, 8:12-15, Fig. 11.

Note that the slits (which become “isolation” structures 200) extend laterally along the X direction: “Thereafter, an insulation layer is formed on the side surface and at the bottom of the slits, although not shown in the drawing. Thereby, the slits are filled, and the isolation section 200 shown in FIG. 1 is formed.” Nakajima, 8:34-37.



Id., Fig. 1; Lee, ¶¶ 98-99.

B. Claim 2:

1. [2] “The method of claim 1, further comprising prior to forming the first opening, forming a dummy channel structure extending vertically through the stack.”

Nakajima in view of the knowledge of a POSITA renders this limitation obvious.

As an initial matter, as the analysis under [1.B] demonstrates, it would have been understood, or at least obvious, that Nakajima forms channel structures before its TAVs (C4s), i.e., “prior to forming the first opening.” Lee, ¶¶ 100-101.

In view of the knowledge of a POSA, it would have been obvious to implement some of Nakajima’s channels as dummy channels. Lee, ¶ 104. Kai confirms the knowledge of a POSITA. Kai, for example, discloses forming active and dummy channels, which provide structural support. Ex. 1015 (U.S. Pat. 10,290,643, Kai), 9:23-26 (defining “support opening” as “a structure in which a support structure (such as a support pillar structure) that mechanically supports other elements is subsequently formed”), 9:45-48 (“support openings 19” extend through stack), 10:20-27 (forming channels in support openings). Kai refers to the dummy channels as “support pillar 20” and active channels as “memory stack structured.” *Id.*, 16:28-38; Fig. 15A, 25:58-63 (dummy support channels (20) have no connection to the upper level, whereas the active channel structures (55) include contacts (88)). Park, likewise, discloses active and dummy, supporting channels. Ex. 1016 (U.S. Pat. 9,859,297, Park), 6:19-26, 7:45-51. Kim, too, forms dummy channels and dummy channels through the stack at the same time. Ex. 1017 (U.S. Pat. Pub. 2018/0308559, Kim) [0047] (“The stack structure ST may be penetrated with a plurality of dummy holes DH on the connection region CTR,” “DS may physically support,” and listing same materials as channels), [0071] (“The channel holes CH

and the dummy holes DH may be formed at the same time.”), [0072] (same time), Fig. 13 (DH through stack on edge). It was known that to perform this gate replacement process, “support pillars” were necessary. Ex. 1018 (U.S. Pat. 8,945,996), 5:64-6:2, 7:19-23; Lee, ¶¶ 105-07.

A POSITA would have been motivated to employ dummy channels through the stack for several reasons. First, it is advantageous to use dummy channels as support structures because they can be made by the same process and at the same time as the active channels. Ex. 1015 (Kai), 10:20-27; Lee, ¶ 108. Second, dummy channels do not require connections to the upper-level devices, thereby not consuming space above the structures while also serving as support structures. Ex. 1016 (Park), 8:55-65; Lee, ¶ 108. Third, it was well known to include dummy support members, including ones that travel through the entire stack or partially through the stack. Ex. 1015 (Kai), Fig. 6A (support members 20), 16:28-38. It was well known that adding additional dummy channels “provide[s] additional structural support during replacement of the [sacrificial gate layers].” Ex. 1019 (U.S. Pat. 10,115,632), 30:14-27; *see also id.*, 15:3-22 (structures 20 are dummy channel structures). Lee, ¶ 104. Fourth, adding the additional dummy structures would result in reducing the likelihood of defective bits on the edge of the memory cell region, because the addition of the additional rows extends the memory cell pattern for those respective columns into the dummy region. Lee, ¶ 102. It was well known that

when a pattern stops (instead of extending into the dummy region), defects occur on the edge. *Id.* (citing Ex. 1020 (U.S. Pat. 5,945,717), 8:47-53 and Ex. 1021 (U.S. Pat. 10,347,487), 2:20-43 to explain the edge effect). Fifth, adding the additional dummy structures would result in an overall more uniform feature pattern, which reduces processing issues. *Id.*, ¶ 103 (citing Ex. 1022 (Ronse), 11 to explain this processing issue).

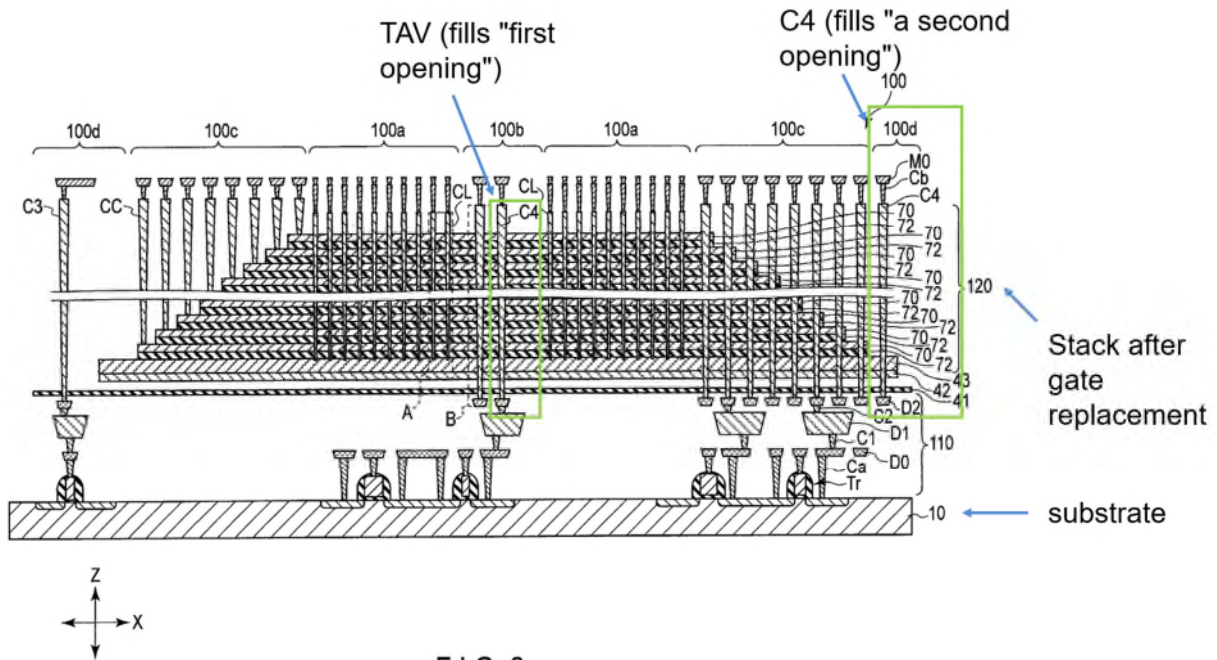
Adding dummy structures would have been routine and a POSITA would have had a high expectation of success. First, as the above discusses, Nakajima already discloses forming channel structures, and the same materials are used for dummy channels. Second, for the reasons above, the additional dummy channel structures would actually reduce processing issues. Lee, ¶ 109. Third, as the above demonstrates, dummy channels were commonplace. *Id.*

C. Claim 3:

1. [3] **“The method of claim 1, wherein forming the first opening comprises simultaneously etching the first opening through the stack and a second opening outside of the stack.”**

Nakajima discloses, or renders obvious, this limitation.

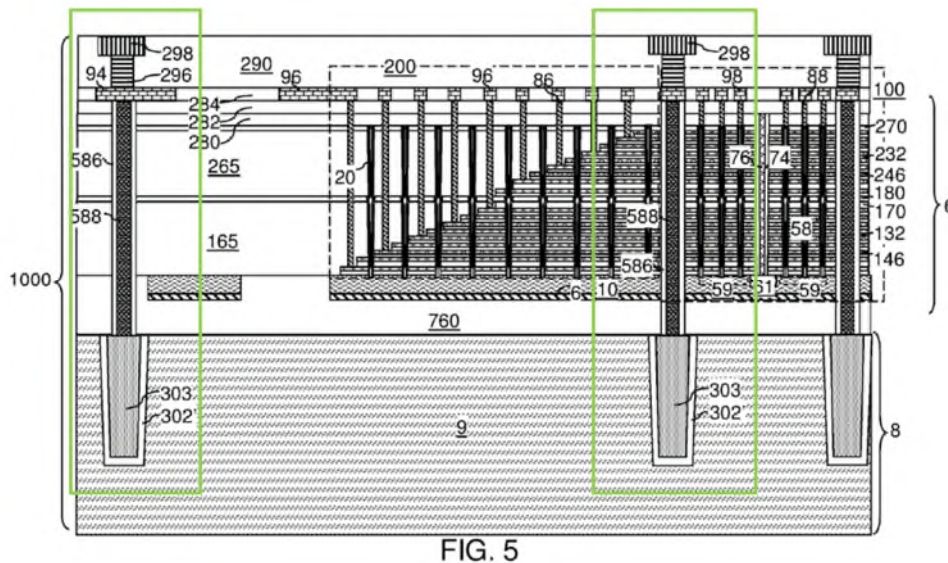
As the [1.C] analysis demonstrates, Nakajima discloses forming holes H1 through the stack for its TAVs (C4). One C4 structure, however, is outside of the stack (on the right below):



Nakajima, Fig. 2. Nakajima only discloses one step for creating the H1 holes. *Id.*, 7:37-43. And Nakajima only discloses one set of steps for forming the C4 contacts. *Id.*, 7:5-8:11. Thus, it would have been understood that Nakajima forms the first and a second hole at the same time. Lee, ¶¶ 110-12.

At a minimum, forming both holes simultaneously would have been obvious, because it would reduce processing time. Indeed, all the structural elements of the C4s are the same, so using a single set of processing steps to make all C4s would be straightforward (simply creating more instances) and significantly reduce processing time. Lee, ¶ 113. And it would have been routine and highly predictable. As the above figure illustrates, Nakajima's process is already able to etch the C4 holes in various places, regardless of whether the holes extend through all or only a portion

of the stack. And elsewhere, Nakajima discloses etching contact CC (which travel partially through the stack) and C3 (which do not travel through the stack) at the same time. Nakajima, 17:33-45. Indeed, it was known and routine to etch holes at the same time through either the full stack or only small portions of the stack, because it saves processing time. *E.g.*, Ex. 1023 (U.S. Pat. Pub. 2019/0081061, Tessariol), [0037] (“dummy-structure openings 56 and via openings 54 are formed at the same time (i.e., simultaneously)”), Fig. 9 (extending through different number of stack layers). And it was well known to create through-contacts in the peripheral region and through the stack at the same time. For example, Mushiga discloses forming through-array contacts (588), including the cavities, insulating spacers, and conductive cores, at the same time:



Ex. 1010 (Mushiga), Fig. 5, 10:31-58; Lee, ¶¶ 114-15.

D. Claim 4:

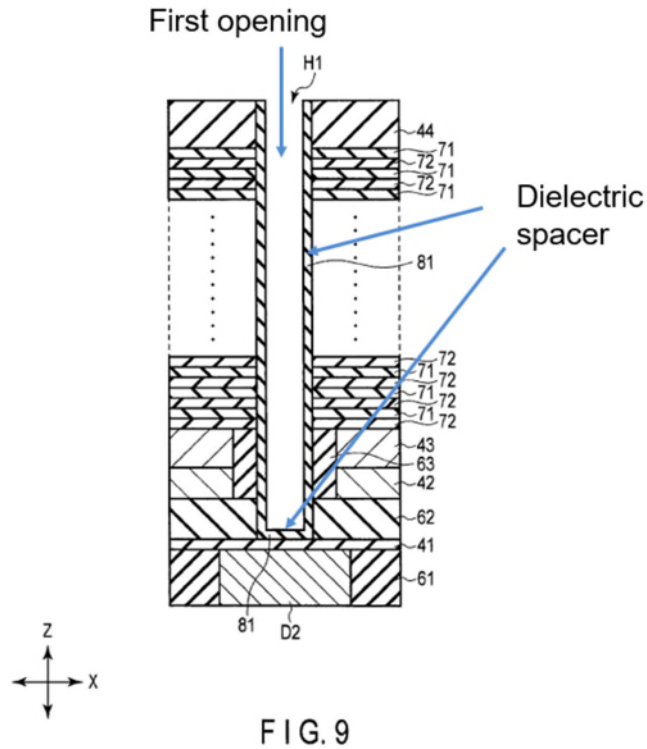
1. **[4] The method of claim 3, wherein forming the TAC comprises depositing the conductor layer in the first opening to form the TAC and in the second opening to form a peripheral contact.”**

Nakajima discloses this limitation. The claim [3] analysis demonstrates that Nakajima discloses a C4 outside the memory stack, i.e., a peripheral contact. Ex. 1001, 10:2 (peripheral contact 148), Fig. 1. The claim [1.E] analysis demonstrates that Nakajima discloses depositing a conductor layer in these openings, i.e., to form a TAC (for the C4 in the stack) and a peripheral contact (for the C4 outside the stack). Lee, ¶¶ 116-17.

E. Claim 5:

1. **“[5.PRE] The method of claim 1, wherein forming the spacer on the sidewall of the first opening comprises: [5.A] depositing a dielectric layer on the sidewall and a bottom surface of the first opening; and”**

Nakajima discloses these limitations: “silicon oxide layer 81 is conformally formed along the bottom and the side surface of the hole H1.” Nakajima, 7:44-49.



Id., Fig. 9; Lee, ¶ 118.

2. [5.B] “removing part of the dielectric layer that is deposited on the bottom surface of the first opening.”

Nakajima discloses this limitation: “Next, as shown in FIG. 10, a portion of the silicon oxide layer 81 that is located at the bottom of the hole H1 is removed by, for example, RIE using a mask layer not shown in the drawing, so that the silicon nitride layer 41 is exposed.” Nakajima, 7:50-53.

ALD

Nakajima does not detail the type of deposition technique to deposit the oxide liner, but deposits “silicon oxide layer 81 ... conformally” (*see* [1.D] analysis). It was well known to deposit a dielectric liner, including silicon oxide, in a hole or trench through a memory stack via ALD. Ex. 1009 (Toyama), [0226] (backside trench 79), [0313] (moat trenches 579); Ex. 1024 (U.S. Pat. 9,620,514), 35:51-61 (forming “dielectric spacer” by first forming “silicon oxide layer” via “ALD”); Ex. 1023 (Tessariol), [0063] (ALD), [0038] (conductive vias 58). A POSITA would have been motivated to employ ALD given that Nakajima expressly requires a conformal deposition. ALD became popular in large part due to its ability to deposit material conformally for 3D structures. Ex. 1025 (Hwang), 12 (“better conformality over three-dimensional (3D) structures”) 13 (“unprecedented conformality over the 3D structures”). And ALD was highly predictable, as it was textbook material and routine to implement before the ’254 patent was filed. *Id.*; *see also* Ex. 1009 (Toyama), [0226], [0313]; Ex. 1023 (Tessariol), [0063], [0038]; Lee, ¶¶ 120-22.

Anisotropic Etching

Nakajima would have been understood (and it certainly would have been obvious) to disclose the removal of the bottom portion of the dielectric ([5.B]) via anisotropic etching: “Next, as shown in FIG. 10, a portion of the silicon oxide layer 81 that is located at the bottom of the hole H1 is removed by, for example, RIE using

a mask layer not shown in the drawing, so that the silicon nitride layer 41 is exposed.” Nakajima, 7:50-53. First, this Nakajima’s RIE is anisotropic, because it is a directional etch (with nearly vertical sidewalls). Ex. 1026 (U.S. Pat. 10,515,799), 6:63-65 (“For example, channel hole 120 can be formed by anisotropic reactive ion etching (RIE).”); Ex. 1027 (U.S. Pat. 9,570,460), 11:55-58 (“The at least one memory film 7, 9, 11 and cover layer 410 may be etched using RIE or another suitable anisotropic wet or dry etching method to form the opening 417.”); Lee, ¶ 123. That is precisely what Nakajima discloses in removing the bottom portion of the liner. *Id.*

Further, it was well known, and obvious, that to form a material, including a dielectric liner, on only the sidewall of a hole, the typical approach involves a deposition and then an etch—such as an anisotropic etch—to remove the deposition on the bottom portion. Ex. 1028 (U.S. Pat. 9,728,546), 34:62-35:3 (“The dielectric liners 141 can be formed, for example, by formation of a dielectric material layer including a first dielectric material, and by a subsequent anisotropic etch (such as a reactive ion etch) that removes horizontal portions of the dielectric material layer to form dielectric spacers 141”), 17:41-46 (“Each first semiconductor channel portion 601 can be formed on inner sidewalls of each memory film 50 by deposition of a semiconductor material layer and a subsequent anisotropic etch of the semiconductor

material layer.”). Removing the bottom portion has the obvious benefit of enabling a subsequent conductive core to connect to the underlying element. Lee, ¶ 124.

G. Claim 7:

1. [7.PRE] “The method of claim 1, wherein forming the spacer on the sidewall of the first opening comprises: [7.A] “forming a plurality of shallow recesses by removing parts of the sacrificial layers abutting the sidewall of the first opening;”

Nakajima renders obvious this limitation under PO’s incorrect interpretation and renders it obvious under the correct interpretation.

As an initial matter, the ’254 Patent makes clear that these limitations relate to an intentional etch that forms actual recesses in the sacrificial layers. Ex. 1001, 13:47-61, Fig. 3D. For infringement, however, PO interprets this claim to include largely undetectable and unintentional alleged recesses. Ex. 1029 (Ex. A-2, YMTC’s Contentions), 30. As is well known, a typical etch through a stack of silicon oxide and silicon nitride layers does not have the exact same selectivity towards each of silicon oxide and silicon nitride, and will result in uneven sidewalls, such that there are recesses in either the oxide layers or the sacrificial layers. Ex. 1030, (U.S. Pat. 11,075,084), 2:59-67 (In “3D NAND memory, it is important to have an etching gas which can etch both SiO₂ and SiN layers (or both SiO₂ and p-Si layers) without selectivity. In another words, ***it is a challenge to find an etch gas that has similar high etch rates of SiO₂ and SiN in terms of getting a smooth***

sidewall of high aspect ratio holes in 3D NAND memory.”); Lee, ¶ 126. Thus, under PO’s apparent interpretation, these various prior art etches that would form the hole for C4 would create these unintentional “shallow recesses,” which may be in the silicon nitride sacrificial layers depending on the etch type. Ex. 1030, (U.S. Pat. 11,075,084), 2:59-67; Lee, ¶ 126.

PO’s Incorrect Claim Interpretation

Nakajima discloses etching through a silicon nitride and silicon oxide stack (see claim [1.A], [1.C]). And typical prior art etches that were both well known and beneficial in that they create holes through the stack, e.g., for contacts, were also known to result in lateral recesses in either the dielectric spacers or sacrificial layers. Ex. 1030, (U.S. Pat. 11,075,084), 2:59-67; Lee, ¶ 127. Thus, Nakajima renders this limitation obvious under PO’s incorrect claim interpretation, because such unintentional recesses would naturally result.

The Correct Claim Interpretation

Nakajima renders this limitation obvious in view of the knowledge of a POSITA. It was well known that an option for a TAC or other through-memory structures was to have a ribbed shape, that is, forming recesses in one of the stack layers. For example, Cui (U.S. Pat. 10,304,852, Ex. 1031) discloses contacts 183 that travel through the staircase and through the entire array. Ex. 1031 (Cui), Fig. 14A, 25:51-53 (e.g., 183 contact on right of region 200); see also Ex. 1015 (Kai),

11:9-34 (“laterally recessed”). Cui depicts an embodiment in which the sidewalls of this contact are straight (“cylindrical via cavity”). Ex. 1031 (Cui), Fig. 15A, 25:63-26:22. And it depicts an alternative embodiment that intentionally creates large recesses in the conductor layers (“ribbed via cavity”). *Id.*, Fig. 16A, 26:23-33.

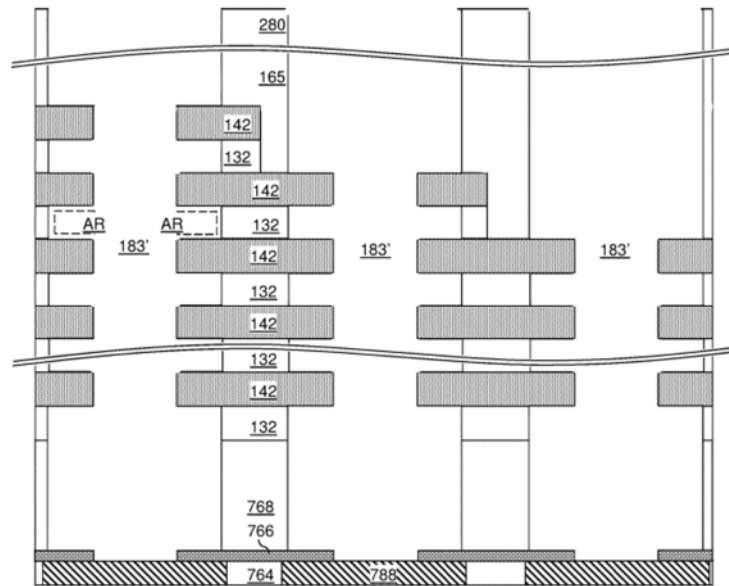


FIG. 16A

Id., Fig. 16A; Lee, ¶ 128.

The ribbed via cavity serves the same purpose as the '254 Patent, namely, providing additional area for the dielectric liner. Ex. 1001, 13:48-61; Lee, ¶ 129. Accordingly, in view of the knowledge of a POSITA, it would have been obvious, and a POSITA would have been motivated to, create a ribbed via cavity in Nakajima's C4 holes. It would have been advantageous because it was known to create “rib regions.” Ex. 1031 (Cui), 26:23-34. This creates additional area for the dielectric material. Lee, ¶ 129. There are only two options for creating such rib

regions: in the sacrificial gates or in the conductive layers. Both were known and result in the same benefit. Ex. 1031 (Cui), Fig. 16A, 26:23-33 (recesses in conductive layers); Ex. 1015 (Kai), 11:9-34 (recesses in sacrificial gates). Lee, ¶ 130. A POSITA would have had a high expectation of success in forming the rib regions because the isotropic and selective etches were well known. *E.g.*, Ex. 1031 (Cui), 26:33-45; Ex. 1015 (Kai), 11:9-34 (recesses in sacrificial gates); Lee, ¶ 131. Indeed, the '254 Patent provides virtually no explanation on creating these known rib regions. Ex. 1001, 17:46-56.

2. [7.B] “depositing a dielectric layer filling in the shallow recesses and on the sidewall and a bottom surface of the first opening; and”

Nakajima renders this limitation obvious. For the reasons set forth above for claim [7.PRE-A], it would have been obvious to form the shallow recesses in Nakajima's C4 holes, and Nakajima discloses forming a dielectric liner (spacer) in that hole. *See* Claim [5.PRE-5.B]; Lee, ¶ 132. Recall that Nakajima discloses depositing a conformal liner, thus the liner will fill the shallow recesses. *Id.*

3. [7.C] “removing part of the dielectric layer that is deposited on the bottom surface of the first opening.”

Nakajima renders this limitation obvious in view of the knowledge of a POSITA. For the reasons set forth above for claim [7.PRE-B], it would have been obvious to form a liner in the hole with shallow recesses, and Nakajima discloses

removing the bottom portion of that dielectric liner (spacer). See Claim [5.C]; Lee, ¶ 133.

H. Claim 8:

1. [8] **“The method of claim 7, wherein the removal of the part of the dielectric layer comprises isotropic etching on the sidewall and the bottom surface of the first opening.”**

Nakajima renders this limitation obvious in view of the knowledge of a POSITA.

As an initial matter, the '254 Patent describes using an isotropic etch because the dielectric material on the bottom will be thicker than on the sidewalls, thereby allowing for a non-directional etch. Ex. 1001, 14:1-19. This was well known. For example, Mushiga (Ex. 1010) describes depositing a liner (586) such that the liner is thicker at the bottom (at the interface of the substrate) and then performing an isotropic etch because of this fact to remove the bottom dielectric. Ex. 1010 (Mushiga), 10:38-42, 12:30-53; Lee, ¶ 135. That the bottom liner is thicker is what allows for the isotropic etch, which is advantageous because directional etching is not necessary given the thicker bottom oxide. *Id.* Note that isotropic etch does not pose the same potential damage issues of anisotropic etches. *Id.*; Lee, ¶ 135. A POSITA would have had a high expectation of success, because isotropic etches were generally well known, including for this very application. Ex. 1010 (Mushiga), 12:30-53; Lee, ¶ 135.

I. Claim 9:

1. [9.PRE] “The method of claim 1, wherein forming the first opening comprises: [9.A] “simultaneously etching the first opening through the stack, a second opening outside of the stack, and a third opening through the stack,”

Nakajima renders obvious these limitations in view of the knowledge of a POSITA.

First, as the claim [3] analysis explains, Nakajima discloses, or renders obvious, simultaneously etching the C4s at the same time, including the first hole all the way through the stack and another hole outside the stack, here “a second opening”:

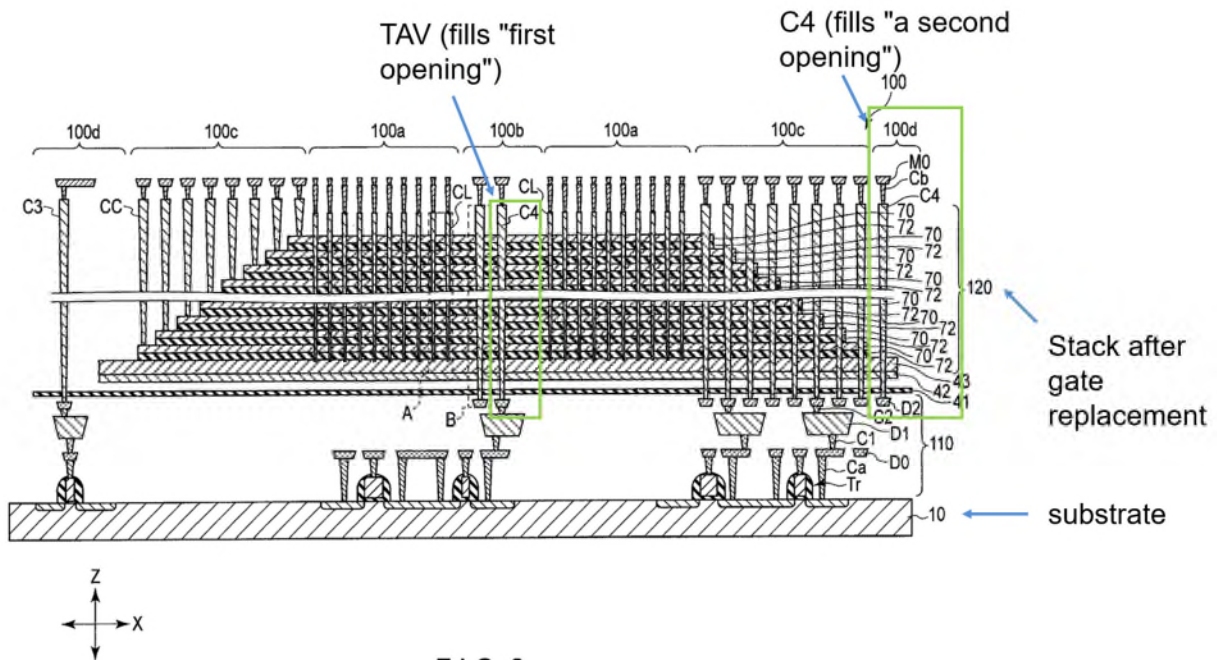


FIG. 2

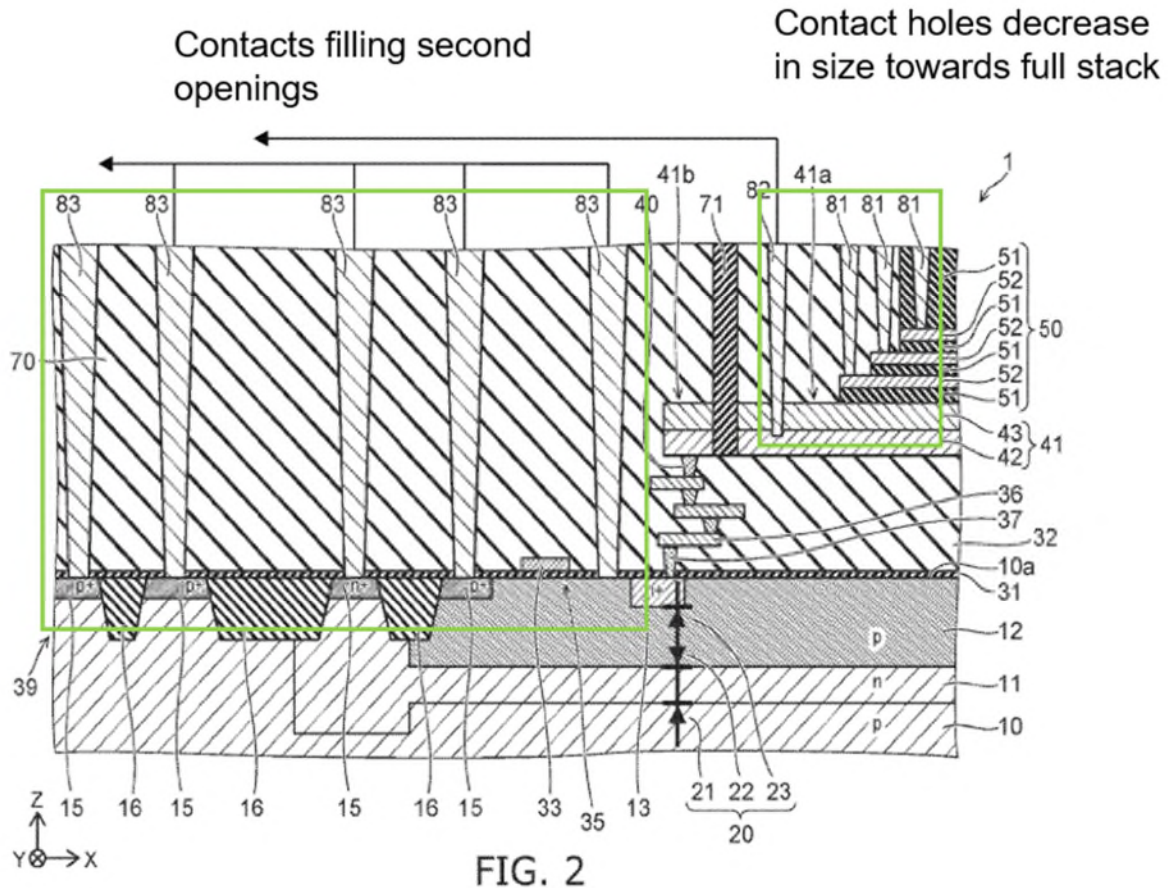
Nakajima, Fig. 2; Lee, ¶ 137.

Second, the claim [2] analysis demonstrates that it would have been obvious to further etch dummy holes, including dummy channel holes. Such a hole through the array constitutes a “third hole.” Lee, ¶ 138. For the same reasons in claim [3], it would have been obvious to etch all these holes at the same time, because for example, it saves processing time and was well known. Lee, ¶ 139.

2. **[9.B] “wherein a lateral dimension of the third opening is smaller than lateral dimensions of the first and second openings.”**

Nakajima renders this limitation obvious in view of the knowledge of a POSITA.

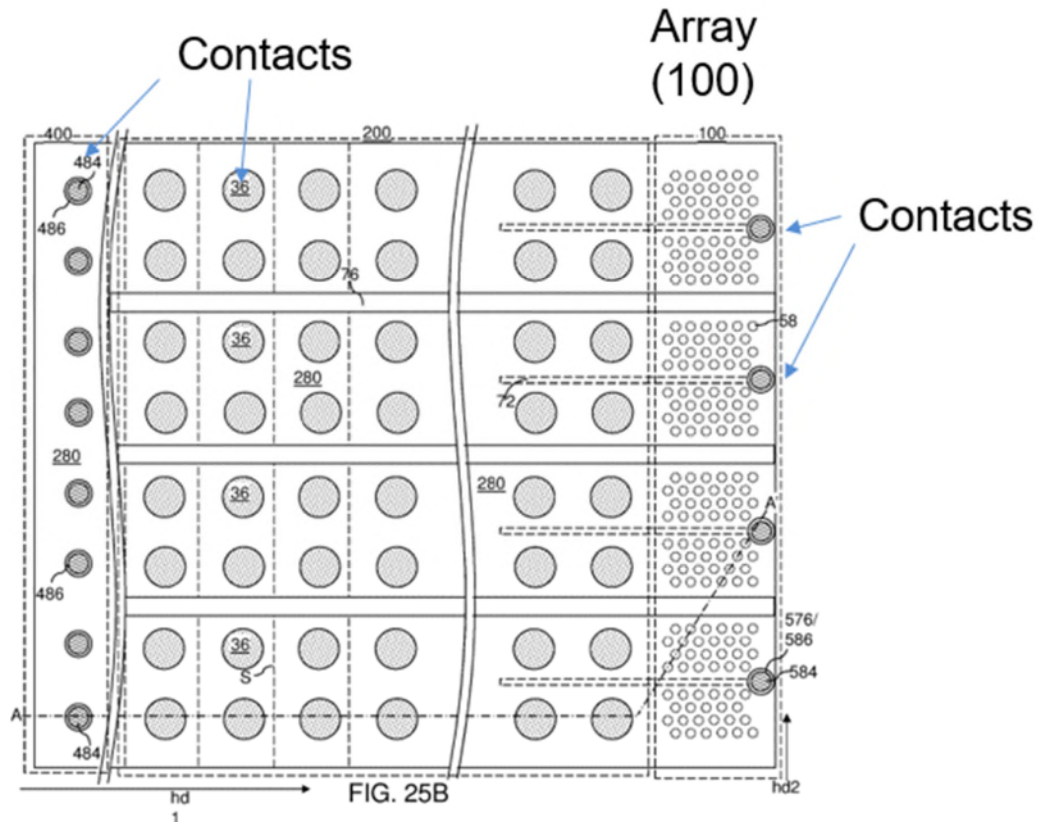
To start, the lateral dimensions of via structures typically get smaller towards the array, because the array contains millions or billions of channel structures. Lee, ¶ 142. This is shown below:



Ex. 1006 (Fujiki), Fig. 2. Thus, it would have been obvious that the second hole, which is outside of the array, will have the largest lateral dimension, consistent with Fujiki's figure 2. Outside the array, there is more room to operate without creating issues, such as short circuits, so using larger structures (e.g., that have less resistance) is possible and desirable due to larger process margins. Lee, ¶ 142.

Next, it would have been obvious that the third hole will have the smallest lateral dimensions. Per the claim [9.A] analysis, the third hole is a dummy hole, e.g., a dummy channel hole. Channel holes are miniscule in size relative to contacts. For

example, below is a top-down view showing channel structures in region 100 versus various contacts:



Ex. 1031 (Cui), Fig. 25B; Lee, ¶ 143. A POSITA would have understood the above figure to illustrate relative size differences in the dense array and the less dense peripheral, because of the inclusion of relative more channel structures. Lee, ¶ 143. Also note the height difference in Figure 2 above. The contacts 83 are longer, and as a natural result of etches that taper (as shown in Figure 2), the lateral width of the top is naturally wider. Lee, ¶ 143. Further, the third holes are dummy holes. This means an active structure, such as a channel structure, will not fill the dummy hole. As a result, such features do not present process margin issues, and employing

smaller feature is not an issue. For example, as claim [10] demonstrates, a simple insulator fill may occupy the dummy hole.

J. Claim 10:

[10.PRE] “The method of claim 9, wherein forming the spacer on the sidewall of the first opening comprises: [10.A] “depositing a dielectric layer (i) fully filling in the third opening to form a dummy channel structure and (ii) partially filling in the first opening and the second opening; and”

Nakajima in view of the knowledge of a POSITA renders this limitation obvious.

First, the claim [1.D] analysis demonstrates that Nakajima discloses depositing a dielectric liner on the first opening and second opening (C4s), i.e., partially filling those holes. Lee, ¶ 145.

Second, one way to fill a dummy hole was to completely fill it with an oxide, here the insulating liner. As the claim [2] analysis demonstrates, one known beneficial use of dummy structures was as a support pillar. A common support pillar was a solid dielectric, e.g., oxide, pillar. Ex. 1032 (U.S. Pat. 9,793,139), 15:21-36 (“dielectric support pillar 7P”). The benefit of the complete fill is more support relative to only a partial fill. *Id.*; Lee, ¶ 146.

1. **[10.B] “removing parts of the dielectric layer that are deposited on a bottom surface of the first opening and on a bottom surface of the second opening.”**

Nakajima renders this limitation obvious in view of the knowledge of a POSITA.

The claim [5.B] analysis demonstrates that Nakajima discloses removing the bottom portion, and it would have been obvious to do so for each contact, so that the proper interconnection path can be made with good electrical coupling. Lee, ¶ 147.

K. Claim 11:

1. **[11.PRE] “A method for forming a three-dimensional (3D) memory device, comprising:”**

This limitation is identical to [1.PRE] and Nakajima discloses it for the same reasons.

2. **[11.A] “forming a stack comprising a plurality of dielectric/sacrificial layer pairs on a substrate;”**

This limitation is identical to [1.A] and Nakajima discloses it for the same reasons.

3. **[11.B] “forming a channel structure extending vertically through the stack;”**

This limitation is identical to [1.B] and Nakajima discloses it, or renders it obvious, for the same reasons.

4. **[11.C] “forming a dummy channel structure extending vertically through the stack;”**

Nakajima renders obvious forming a dummy channel structure that extends vertically through the stack for the reasons set forth in [2].

5. **[11.D] “simultaneously etching a first opening through the stack and a second opening outside of the stack;”**

This limitation is present in [3], and Nakajima discloses it, or renders it obvious, for the same reasons.

6. **[11.E] “simultaneously forming a first spacer on a sidewall of the first opening and a second spacer on a sidewall of the second opening;”**

The claims [3]-[4] analysis demonstrates that Nakajima discloses, or renders obvious, forming the C4s at the same time, and thus forming the spacers in the first and second holes at the same time.

7. **[11.F] “depositing a conductor layer (i) filling in the first opening to form a through array contact (TAC) and (ii) filling in the second opening to form a peripheral contact; and”**

This limitation is substantively the same as claim [4] (but recites “depositing” instead of “filling”), and Nakajima discloses it, or renders it obvious, for the same reasons (as shown it completely fills the hole).

8. [11.G] “after forming the TAC and peripheral contact, forming a slit extending vertically through the stack.”

This limitation is substantively the same as [1.F] (the above demonstrates it would have been obvious to form all TACs at the same time), and Nakajima discloses it for the same reasons.

L. Claim 12:

[12.PRE] “The method of claim 11, wherein forming the first spacer on the sidewall of the first opening comprises:

[12.A] “depositing a dielectric layer on the sidewall and a bottom surface of the first opening; and”

[12.B] “removing part of the dielectric layer that is deposited on the bottom surface of the first opening.”

These limitations are substantively the same as [5.PRE-B] (“first” here refers to the TAC through the array of claim 5), and Nakajima discloses them for the same reasons.

M. Claim 13:

1. [13] “The method of claim 12, wherein the deposition of the dielectric layer comprises atomic layer deposition (ALD), and the removal of the part of the dielectric layer comprises anisotropic etching on the bottom surface of the first opening.”

This limitation is identical to [6], and Nakajima renders it obvious for the same reasons.

N. Claim 14:

[14.PRE]-[14.C]

These limitations are effectively identical to claim [7.PRE-7C], and Nakajima renders them obvious for the same reasons. These limitations recite “first” to require that the steps apply to the TAC. Claim 7 steps are on the TAC.

O. Claim 15:

1. **[15] “The method of claim 14, wherein the removal of the part of the dielectric layer comprises isotropic etching on the sidewall and the bottom surface of the first opening.”**

This limitation is identical to claim [8], and Nakajima renders it obvious for the same reasons.

P. Claim 17:

1. **[17] “The method of claim 11, wherein the dielectric layers in the dielectric/sacrificial layer pairs comprise silicon oxide, the sacrificial layers in the dielectric/sacrificial layer pairs comprise silicon nitride, and the first and second spacers comprise silicon oxide.”**

Nakajima discloses this limitation. Nakajima, 7:26-36 (“sacrifice layers 71 are silicon nitride layers, and the insulation layers 44, 62, 63, and 72 are silicon oxide layers”), 7:44-49 (“silicon oxide layer 81 is conformally formed along the bottom and the side surface of the hole H1”); Lee, ¶ 161.

Q. Claim 18:

- 1. [18.PRE] “A method for forming a three-dimensional (3D) memory device, comprising:”**

This limitation is identical to claim [1.PRE], and Nakajima discloses it for the same reasons.

- 2. [18.A] “forming a stack comprising a plurality of dielectric/sacrificial layer pairs on a substrate;”**

This limitation is identical to claim [1.A], and Nakajima renders it obvious for the same reasons.

- 3. [18.B] “forming a channel structure extending vertically through the stack;”**

This limitation is identical to claim [1.B], and Nakajima renders it obvious for the same reasons.

- 4. [18.C] “simultaneously etching a first opening through the stack, a second opening outside of the stack, and a third opening through the stack, wherein a lateral dimension of the third opening is smaller than lateral dimensions of the first and second openings;”**

This limitation is identical to claim [9.A-B], and Nakajima renders it obvious for the same reasons. Technically, these limitations refer to “a first opening” instead of “the first opening,” but refer to the same element.

5. **[18.D] “depositing a dielectric layer (i) fully filling in the third opening to form a dummy channel structure and (ii) partially filling in the first opening and the second opening;”**

This limitation is identical to claim [10.A], and Nakajima renders it obvious for the same reasons.

6. **[18.E] “removing parts of the dielectric layer that are deposited on a bottom surface of the first opening and on a bottom surface of the second opening;”**

This limitation is identical to claim [10.B], and Nakajima renders it obvious for the same reasons.

7. **[18.F] “depositing a conductor layer (i) filling in the first opening to form a through array contact (TAC) and (ii) filling in the second opening to form a peripheral contact; and”**

This limitation is virtually identical to claim [4], and Nakajima discloses it, or renders it obvious, for the same reasons (again, says “a conductive layer” instead of “the conductive layer” and says “filling”) (as shown it completely fills the hole).

8. **[18.G] “after forming the TAC and peripheral contact, forming a slit extending vertically through the stack.”**

This limitation is substantively the same as claim [1.F] but also includes recites forming the slit after the peripheral contact. As the above illustrates, Nakajima renders obvious forming these contacts at the same time, and thus the claim [1.F] analysis demonstrates that Nakajima discloses it is obvious for the same reasons.

R. Claim 20:

- 1. [20] “The method of claim 18, further comprising prior to etching the first, second, and third openings, forming a staircase structure at one side of the stack.”**

Nakajima would have been understood to disclose, and alternatively render obvious, this limitation.

Nakajima describes after forming the C4 structures, performing the gate line replacement process, i.e., replacing the sacrificial gates with conductive gates. Nakajima, 7:5-8:34. Thus, it would have been understood that Nakajima has already formed the staircase for several reasons. First, as Nakajima describes, forming a staircase requires a process that etches the sacrificial gates and oxide layers. *Id.*, 16:49-55. In other words, the gate replacement process has not been done yet. Thus, when Nakajima discloses the C4, slit, and gate replacement process steps that bring the process to the point of replacing the gates (7:5-8:34), the staircase has already been made, because the staircase is made when the stack is composed of oxide and sacrificial layers. Lee, ¶ 171. Second, attempting to make the staircase region after gate replacement would involve etching through large amounts of conductive gate material, instead of a stack of oxide and silicon nitride layers, which would introduce several problems. *Id.*, ¶ 172. Finally, the peripheral contact extends through a conductive layer that is on the staircase structure:

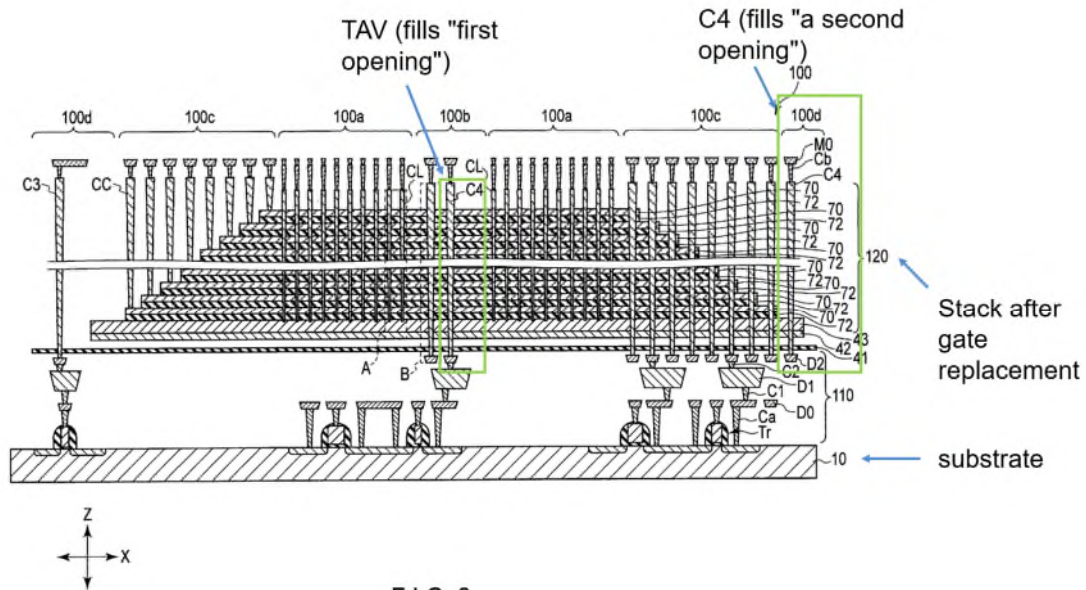


FIG. 2

Nakajima, Fig. 2. As can be seen above, the “second opening” is through an insulator structure that is laid down over the staircase after it is made, and thus it would make little sense to attempt to make such a hole without first making the staircase and overlying it with the dielectric. For this reason, the standard construction is building the stack, the staircase, and then the other elements of the memory device. Ex. 1015 (Kai), Figs. 1-6; Lee, ¶ 173.

XI. SECONDARY CONSIDERATIONS

Petitioner is unaware of any applicable secondary considerations of nonobviousness. None were identified during prosecution. See generally Ex. 1002 (the '254 FH). Even if such considerations existed, none would overcome the strong *prima facie* showing of obviousness.

XII. CONCLUSION

Petitioner respectfully requests that the Board enter a final written decision finding the Challenged Claims unpatentable.

Respectfully submitted,

Dated: October 11, 2024

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CERTIFICATE OF COMPLIANCE

The undersigned certifies that the foregoing PETITION FOR *INTER PARTES* REVIEW complies with the type volume limitation in 37 C.F.R. §42.24(a). According to the utilized word-processing system's word count, the petition—excluding the caption, table of contents, table of exhibits, mandatory notices, certificate of word count, and certificate of service—contains 9,596 words.

Dated: October 11, 2024

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CERTIFICATE OF SERVICE

The undersigned hereby confirms that the foregoing Petition for *Inter Partes* Review and associated documents and exhibits were caused to be served on October 11, 2024 via overnight courier upon the following counsel of record for Patent Owner:

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Copies of this Petition and accompanying documents and exhibits were also served via electronic mail on Patent Owner's counsel of record for related PTAB proceedings and in the related district court litigation – ROPES & GRAY LLP and LATHAM & WATKINS:

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