

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner
v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2025-00034
U.S. Patent No. 10,879,254
Issue Date: December 29, 2020

Title: THREE - DIMENSIONAL MEMORY DEVICES HAVING THROUGH
ARRAY CONTACTS AND METHODS FOR FORMING THE SAME

**DECLARATION OF DR. JACK C. LEE IN SUPPORT OF
PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 10,879,254**

TABLE OF CONTENTS

I. INTRODUCTION	4
II. BACKGROUND AND EXPERT QUALIFICATIONS	4
III. ASSIGNMENT AND MATERIALS CONSIDERED	7
IV. UNDERSTANDING OF THE LAW	10
V. LEVEL OF SKILL IN THE ART	14
VI. TECHNOLOGY BACKGROUND AND STATE OF THE ART	15
VII. THE '254 PATENT	30
A. Effective Filing Date	30
B. Overview	30
C. Prosecution History	35
VIII. CLAIM CONSTRUCTION.....	36
IX. UNPATENTABILITY ANALYSIS.....	37
A. Overview of the Prior Art.....	37
1. Nakajima	37
B. Ground 1: Nakajima in View of the Knowledge of a POSITA Render Obvious Claims 1-15, 17-18, AND 20.....	40
1. Claim 1:.....	40
2. Claim 2:.....	53
3. Claim 3:.....	57
4. Claim 4:.....	60
5. Claim 5:.....	60
6. Claim 6:.....	62

Petition for *Inter Partes* Review of U.S. Patent No. 10,879,254
Declaration of Dr. Jack C. Lee

7.	Claim 7:.....	65
8.	Claim 8:.....	69
9.	Claim 9:.....	70
10.	Claim 10:.....	75
11.	Claim 11:.....	76
12.	Claim 12:.....	78
13.	Claim 13:.....	78
14.	Claim 14:.....	78
15.	Claim 15:.....	78
16.	Claim 17:.....	79
17.	Claim 18:.....	79
18.	Claim 20:.....	81
C.	Secondary Considerations of Non-Obviousness.....	82

I, Dr. Jack C. Lee, declare as follows:

I. INTRODUCTION

1. I have been retained by Micron Technology, Inc. (“Micron”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office (“PTO”). I am not an employee of Micron or any affiliate or subsidiary of Micron.

2. I have been asked to consider whether certain references disclose or teach the features recited in claims 1-15, 17-18, and 20 of U.S. Patent No. 10,879,254, which I refer to herein as the ’254 Patent.

3. My opinions and the bases for my opinions are set forth below.

4. I am being compensated at my standard consulting rate of \$680 per hour for my time. My compensation is based solely on the amount of time that I devote to activity related to this case and is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other financial interest in this proceeding.

II. BACKGROUND AND EXPERT QUALIFICATIONS

5. My *curriculum vitae* (“CV”) is attached hereto as Ex. 1004 and provides an accurate identification of my background, experience, and qualifications as an expert in electronics and NAND memory technology.

6. I received a B.S. degree in Electrical Engineering, with highest honors, in 1980, and an M.S. degree in Electrical Engineering in 1981, both from University of California, Los Angeles. I received a Ph.D. degree in Electrical Engineering in 1988 from University of California, Berkeley (“UC Berkeley”).

7. From 1979 to 1984, I was a Member of Technical Staff at the TRW Microelectronics Center, in the High-Speed Bipolar Device Program. I worked on bipolar device/circuit design, fabrication, and testing. I was promoted to Engineering Group Leader level in 1983.

8. I received several academic honors while at UC Berkeley. For example, I won the Best Paper Award from the Institute of Electrical and Electronics Engineers (“IEEE”) International Reliability Physics Symposium in 1988. I was also awarded a Lectureship with my own teaching assistant from UC Berkeley.

9. After receiving my Ph.D. in August 1988, I joined the faculty at The University of Texas at Austin (“UT Austin”). As a faculty member, I have taught numerous courses in semiconductor device fabrication and design, at both the undergraduate and graduate levels. This includes classes relating to, among other things, 3D NAND technology. I have supervised over 40 students who received their doctoral degrees under my guidance. Since September 2000, I have held the Cullen Trust for Higher Education Endowed Professorship in Engineering in the

Department of Electrical and Computer Engineering at UT Austin. In September 2023, I was promoted to the Professor Emeritus level.

10. My current research and teaching interests include semiconductor devices, semiconductor memory applications (including non-volatile memory), fabrication processes, silicon-on-insulator technologies, electrical and material characterization, reliability and modeling, packaging technologies, dielectric and passivation processes, display technologies, photovoltaic and solar cell technologies, high-K gate dielectrics and electrode, and alternative channel materials. I routinely encounter and address topics relating to NAND flash memory, and more specifically 3D NAND flash memory, in my research. My research has been partially supported by grants from the National Science Foundation, the Texas Advanced Research Program, the Semiconductor Research Corporation (SRC), SEMATECH, Texas Emerging Technology Funds, and others.

11. I have authored over 600 journal publications and conference proceeding papers and have coauthored 8 books and book chapters on semiconductor technologies. Many of these relate to the structure and operation of memory devices, including non-volatile memory such as NAND flash memory and 3D NAND flash memory. I am a named inventor of 9 U.S. patents. I have also received numerous teaching and research awards, e.g., inventor recognition and best paper awards.

12. In 2002, I became an IEEE fellow for my “contributions to the understanding and development of ultra-thin dielectrics and their application to silicon devices.” I was also an IEEE Electron Devices Society Distinguished Lecturer from 2004 to 2016.

13. I have served in various technology consulting and business advisor roles. For example, I have taught short courses on semiconductor device physics and technologies at various semiconductor companies and consortiums (e.g., SEMATECH). I have also organized several international conferences and have given lectures at numerous conferences and symposia, including the International Symposium on VLSI Technologies, the IEEE Symposia on VLSI Technology, and the IEEE International Electron Devices Meeting. These conferences are some of the most prestigious in the field.

III. ASSIGNMENT AND MATERIALS CONSIDERED

14. I have been asked to provide analysis and explain the subject matter of the '254 Patent, including the state of the art when the application underlying the '254 Patent was filed. I have also been asked to consider, analyze, and explain certain prior art to the '254 Patent including how that art relates to claims 1-15, 17-18, and 20 (which I refer to as the “challenged claims”) of the '254 Patent and to provide my opinions regarding whether that art invalidates the challenged claims.

Petition for *Inter Partes* Review of U.S. Patent No. 10,879,254
Declaration of Dr. Jack C. Lee

15. The opinions expressed in this declaration are not exhaustive of opinions I may offer in the future regarding the unpatentability of the challenged claims of the '254 Patent. Therefore, the fact that I do not address a particular point should not be understood to indicate an agreement on my part that any claim complies with the requirements of any other applicable rule.

16. I reserve the right to amend and supplement this declaration in light of additional evidence, arguments, or testimony presented during this IPR or related proceedings on the '254 Patent.

17. In forming the opinions set forth in this declaration, I have considered and relied upon my education, knowledge of the relevant field, knowledge of scientific and engineering principles, and my experience. I have also reviewed and considered the '254 Patent (Ex. 1001), its prosecution history (Ex. 1002), and the following additional materials:

Exhibit	Description
1005	U.S. Patent No. 10,777,501 to Nakajima et al. (“Nakajima”)
1006	U.S. Patent Publ. No. 2019/0198524 to Fujiki et al. (“Fujiki”)
1007	U.S. Patent No. 10,658,378 to Tao et al.
1008	Micheloni, “3D Flash Memories” (2016)
1009	U.S. Patent Publ. No. 2017/0179026 to Toyama et al. (“Toyama”)
1010	U.S. Patent No. 10,354,980 to Mushiga et al. (“Mushiga”)

Petition for *Inter Partes* Review of U.S. Patent No. 10,879,254
Declaration of Dr. Jack C. Lee

Exhibit	Description
1011	U.S. Patent Publ. No. 2019/0229125 to Zhou et al.
1012	PCT Publication No. WO 2019/042103 A1 to Dai et al.
1013	U.S. Patent No. 10,679,721 to Kim et al.
1014	Aritome, “NAND Flash Memory Technologies” (“Aritome”)
1015	U.S. Patent No. 10,290,643 to Kai et al. (“Kai”)
1016	U.S. Patent No. 9,859,297 to Park et al. (“Park”)
1017	U.S. Patent Publ. No. 2018/0308559 to Kim et al.
1018	U.S. Patent No. 8,945,996 to Tang et al.
1019	U.S. Patent No. 10,115,632 to Masamori et al.
1020	U.S. Patent No. 5,945,717 to Chevallier
1021	U.S. Patent No. 10,347,487 to Lee et al.
1022	Ronse, “Optical lithography—a historical perspective,” C. R. Physique 7 (2006) (“Ronse”)
1023	U.S. Patent Publ. No. 2019/0081061 to Tessariol et al. (“Tessariol”)
1024	U.S. Patent No. 9,620,514 to Kai et al.
1025	Hwang, “Atomic Layer Deposition for Semiconductors,” Springer (2014) (“Hwang”)
1026	U.S. Patent No. 10,515,799 to Wang et al.
1027	U.S. Patent No. 9,570,460 to Kanakamedala et al.
1028	U.S. Patent No. 9,728,546 to Serov et al.

Exhibit	Description
1029	Excerpt from YMTC’s Exemplary Infringement Claim Chart for U.S. Patent No. 10,879,254 (Ex. A-2 to Disclosure of YMTC II Asserted Claims and Infringement Contentions, dated October 2, 2024) (“Ex. A-2, YMTC’s Contentions”) [PROTECTIVE ORDER MATERIAL – FILED UNDER SEAL]
1030	U.S. Patent No. 11,075,084 to Shen et al.
1031	U.S. Patent No. 10,304,852 to Cui et al. (“Cui”)
1032	U.S. Patent No. 9,793,139 to Sharangpani et al.

IV. UNDERSTANDING OF THE LAW

18. I am not an attorney, but have been instructed in and applied the law as described in this section.

19. I understand that the first step in comparing a challenged claim to the prior art is for the claim to be properly construed. I address how a person of ordinary skill in the art (POSITA) would have understood the challenged claims of the alleged invention in Sections VIII (no claim terms require express construction) and IX (where I discuss certain claim terms).

20. I have been further instructed and understand that a patent claim is unpatentable and invalid as obvious if the subject matter of the claim as a whole would have been obvious to a POSITA of the claimed subject matter as of the time of the invention at issue. I understand that when assessing the obviousness of claimed subject matter, the following factors are evaluated: (1) the scope and content

of the prior art; (2) the difference or differences between each claim of the patent and the prior art; and (3) the level of ordinary skill in the art at the time the patent was filed.

21. I understand that claimed subject matter may be obvious in view of more than one item of prior art. I understand, however, that it is not enough to show simply that all the limitations of the claimed subject matter are spread throughout the prior art. Instead, for claimed subject matter to be obvious over multiple references, there must be some reason or motivation for a POSITA to combine the prior art references to arrive at the claimed subject matter.

22. I have been informed that, in seeking to determine whether an invention that is a combination of known elements would have been obvious to a POSITA at the time of the invention, one must consider the references in their entirety to ascertain whether the disclosures in those references render the combination obvious to such a person.

23. I have been informed and understand that, while not required, the prior art references themselves may provide a teaching, suggestion, motivation, or reason to combine. The motivation linking two or more prior art references can also come from other sources, including, for instance, economic or market demand or the common sense of a POSITA at the time of the invention.

24. I understand that a particular combination may be proven obvious by showing that it was obvious to try the combination. I have been informed that, if a technique has been used to improve one device, and a POSITA would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

25. I further understand that an obviousness analysis recognizes that market demand, rather than scientific literature, often drives innovation, and that a motivation to combine references also may be supplied by the direction of the marketplace. For example, when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a POSITA has good reason to pursue the known options within his or her technical grasp because the result is likely the product not of innovation but of ordinary skill and common sense.

26. I have been informed that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. Thus, where all the elements of a claim are used in substantially the same manner, in devices in the same field of endeavor, the claim is likely obvious.

27. Additionally, I understand that a patent is likely to be invalid for obviousness if a POSITA can implement a predictable variation or if there existed

at the time of the invention a known problem for which there was an obvious solution encompassed by the patent's claims. Therefore, when a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one.

28. I further understand that combining embodiments related to each other in a single prior art reference would not ordinarily require a leap of inventiveness.

29. I also understand that a POSITA must have had a reasonable expectation of success when combining references for claimed subject matter to be obvious.

30. I have been informed and I understand that factors referred to as "objective indicia of non-obviousness" or "secondary considerations" are also to be considered when assessing obviousness when such evidence is available. I understand that these factors can include: (1) commercial success; (2) long-felt but unresolved needs; (3) copying of the invention by others in the field; (4) initial expressions of disbelief by experts in the field; (5) failure of others to solve the problem the claimed subject matter solved; and (6) unexpected results.

31. I also understand that evidence of objective indicia of non-obviousness must be commensurate in scope with the claimed subject matter. I further understand that there must be a relationship, sometimes referred to as a "nexus," between any such secondary indicia and the claimed invention.

32. Finally, I have been informed that one cannot use hindsight to determine that an invention was obvious.

33. I provide my opinions in this declaration based on the guidelines set forth above.

V. LEVEL OF SKILL IN THE ART

34. I have been informed and understand that the level of ordinary skill in the relevant art at the time of the invention is relevant to inquiries such as the meaning of claim terms, the meaning of disclosures found in the prior art, and the reasons a POSITA may have for combining references.

35. I have been informed and understand that factors that may be considered in determining the level of ordinary skill include: (1) the education of the inventor; (2) the type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) education level of active workers in the relevant field. I have been further informed and understand that a person of ordinary skill in the art (POSITA) is also a person of ordinary creativity.

36. In my opinion, a POSITA in the field of the '254 Patent would have had a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) NAND flash memory devices, or an equivalent level of skill,

knowledge, and experience (e.g., an advanced degree may replace some of the professional experience).

37. In my opinion, this POSITA would also have been aware of and generally knowledgeable about semiconductor manufacturing and 3D NAND's structure, its component parts, how it operates, and how it is controlled.

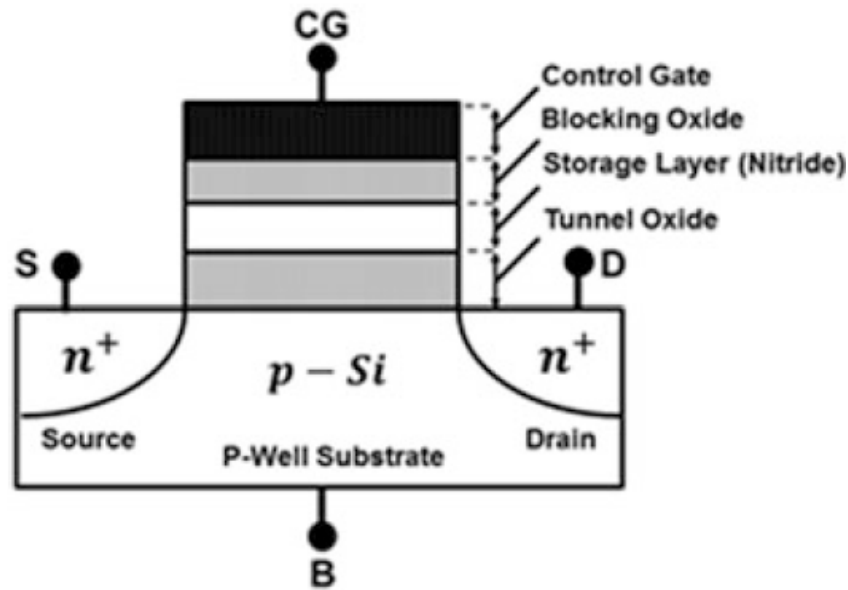
38. In view of my educational background and decades of experience working with semiconductor memory—including non-volatile 3D NAND flash memory—I was a person of more than the ordinary level of skill in the art as of August 2018. In forming my opinion, I have drawn on my academic background and professional experiences. My opinions herein, however, were formed taking into account the perspective of an ordinarily skilled artisan.

VI. TECHNOLOGY BACKGROUND AND STATE OF THE ART

39. I have been asked to provide a brief overview of the technology relevant to the '254 Patent and the state of the art when the '254 priority application was filed.

40. The '254 Patent (and the prior art I discuss herein) relate to three-dimensional (3D) NAND flash memory. “Flash memory” has been known for many decades and is a type of memory that stores information even when power is removed (*viz.*, when the device is turned off).

41. At the heart of flash memory is the “memory cell,” which stores information as electrical charge. An example memory cell is below:



Ex. 1008, 41. In a memory cell, current flows from the “drain” of the device to the “source” of the device, which is typically connected to a low voltage, such as ground. *Id.*, 150 (“[T]he Source Line ... plays the role of the ‘local ground’ for each memory cell.”).

42. The acronym “NAND” refers to a “not-AND” logic gate, and NAND flash memory is a particular type of flash memory where the memory cells form a structure similar to that of a NAND gate. Ex. 1008, 14. The other most common type of flash memory is NOR flash, but NAND offers a higher integration density and occupies a larger market than NOR flash.

43. A NAND flash memory device, like most flash memory devices, has an associated memory controller that controls the read, write, and erase operations

on a memory cell by applying a voltage to that cell's "control gate," labeled as "CG" in the above figures. Ex. 1008, 41.

44. For many years, a NAND flash memory was "planar," that is, two-dimensional (2D). In 2D NAND flash memory, all memory cells lie on a 2D plane (*i.e.*, the x-y plane) on the surface of a memory chip as shown below:

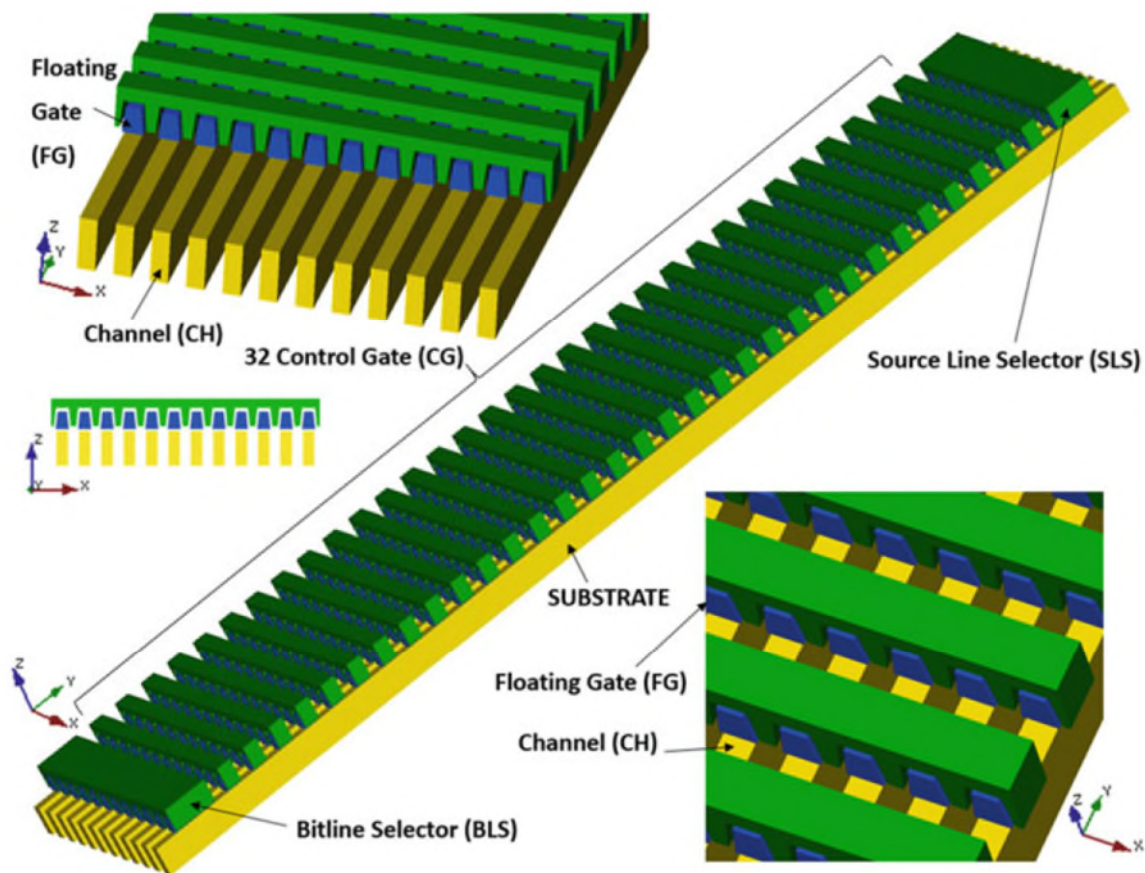


Fig. 3.9 Bird's-eye view of a planar NAND string

Ex. 1008, 86.

45. To boost data storage densities and reduce cost per gigabit, the art developed so-called "three-dimensional (3D) NAND flash cells" starting in about

2006. Ex. 1014, 292. Unlike planar 2D NAND flash memory, in 3D NAND flash memory the memory cells are arranged in vertical, cylindrical NAND flash columns, often referred to as “memory strings.” Conceptually, a modern 3D NAND structure could be conceived by starting from the 2D NAND string building block and turning the 2D NAND string on its side, resulting in a 3D structure with a vertical channel. The following image provides an example:

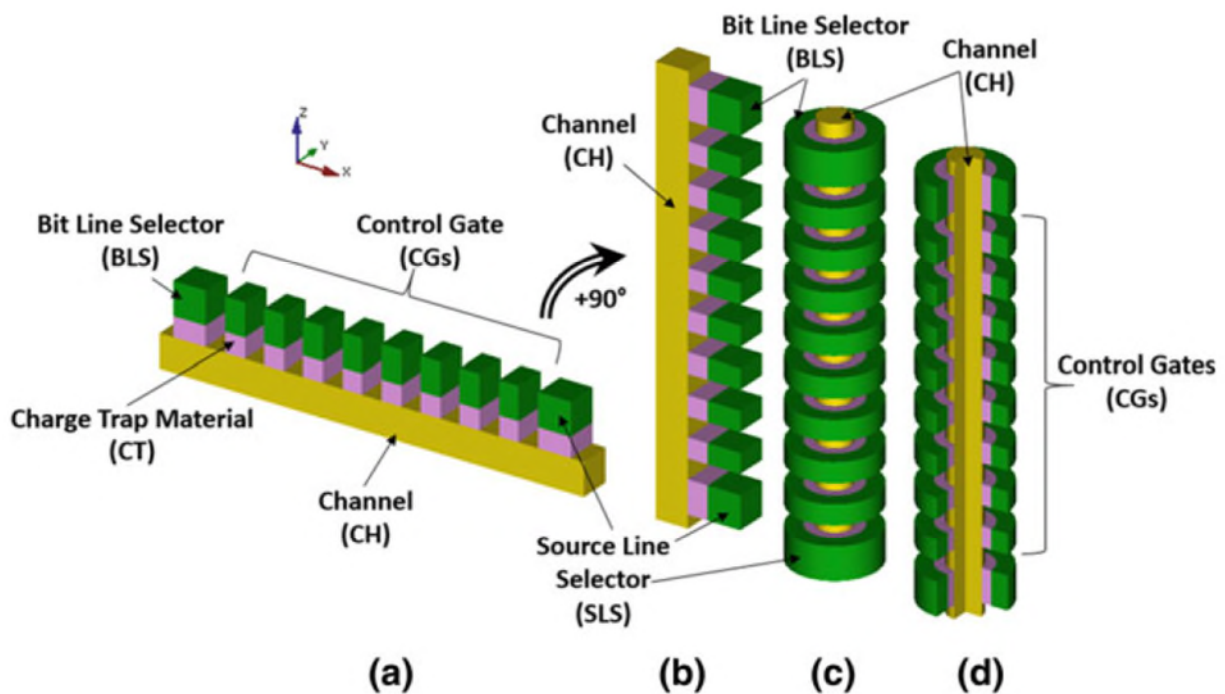


Fig. 4.1 NAND Flash string with horizontal gate and vertical channel: **a** planar, **b** planar rotated by 90°, **c** vertical channel with cylindrical shape and **d** its cross section

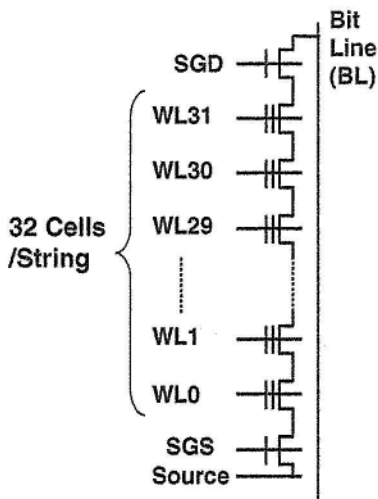
Ex. 1008, 102. As labeled in Figure 4.1, above, each NAND string includes a “cylindrical channel.” *Id.*, 58. The concept of a “channel” was well-known in semiconductor devices and refers to a thin and layer of charge that is formed between the source and drain of a transistor when a voltage is applied to the gate. The

“channel” is highly conductive and allows current to easily flow between the source and drain. The “cylindrical channel” in 3D NAND devices also provides the means for current to flow in a memory string.

46. Multiple of such vertical channels are then repeated in a three-dimensional array. Ex. 1014, 296.

47. As can be seen above, the NAND flash memory “strings” each contain multiple cells “connected in series.” Ex. 1014, 38. The source of one cell is connected to the drain of the next one. Depending on the technology, typically a string consists of 32 to 128 NAND cells.

48. Each end of a string is terminated with a “select transistor.” One is often called the “SGD” (drain-end select gate transistor) and the other one is often called “SGS” (source-end select gate transistor). The “SGD connects” at the string’s drain side “to isolate it from a bit line (BL).” Ex. 1014, 38. Hence, the SGD is also known as the “bit line select transistor” or the “upper select gate.” The SGS connects at the string’s source side “to isolate it from a source line (SL).” *Id.* Since the source line is commonly connected to the ground terminal, SGS is also known as the “ground select transistor” or the “lower select gate.” Word lines are connected to each memory cell control gate. *Id.*, 38-39. A schematic representation of a memory string is shown below:



Ex. 1014, 39.

49. Various architectures for constructing 3D NAND flash memory were known in the art. One such example is the well-known BiCS (Bit Cost Scalable) architecture, where various “contacts” (electrical connections) are formed on top of the memory array. Below are two illustrations of the BiCS architecture show top and bottom perspective views.

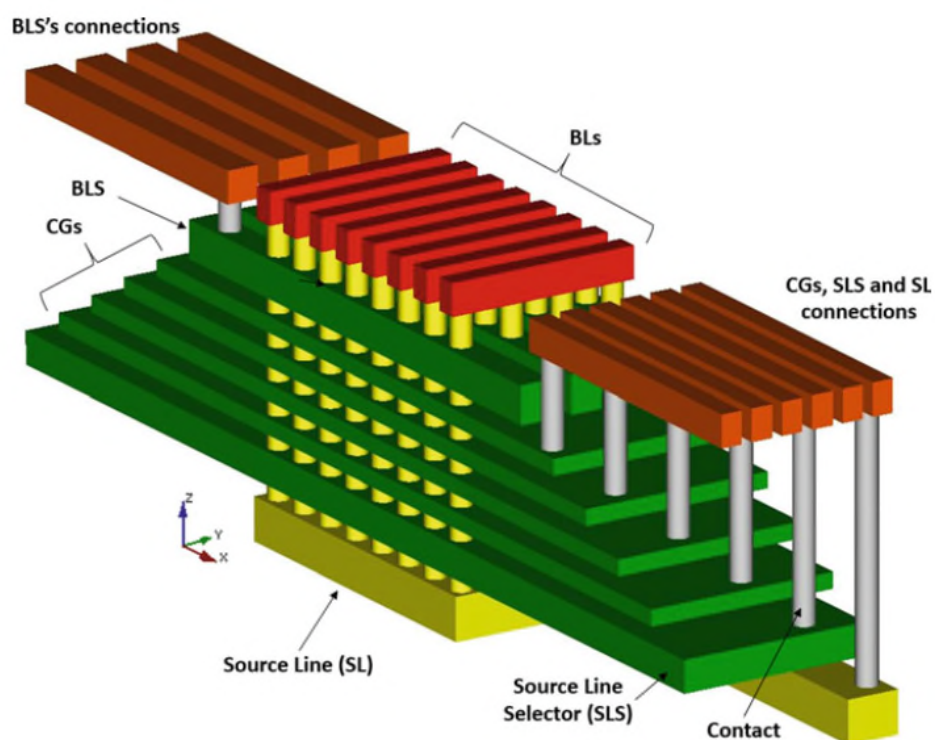


Fig. 4.13 Top bird's eye view of BiCS with gate connections

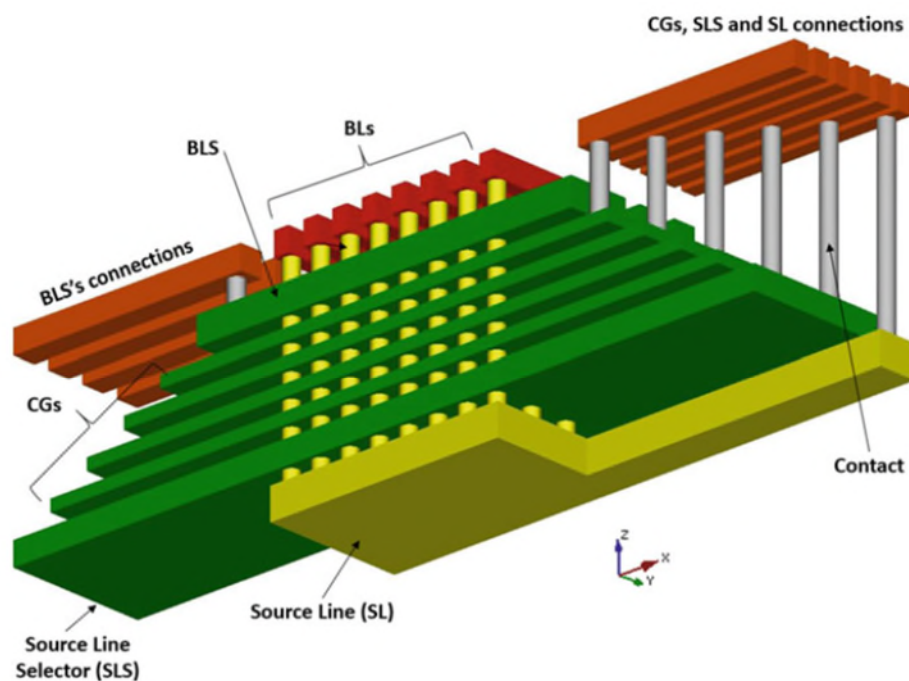
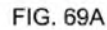


Fig. 4.14 Bottom bird's-eye view of BiCS with gate connections

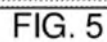
Ex. 1008, 109-110. As is traditional in MOSFET transistors, the “source” terminal connects to a low voltage, such as ground. The same holds true in 3D NAND design, and the BiCS architecture includes source line contacts for providing a low voltage (e.g., ground) connection to the memory strings. This is shown in yellow in the figures above.

50. As can be seen above, the source line contact does not travel directly through the memory stack. It was well known, however, to form contact directly through the memory stack by forming a hole in the stack, an insulating line in the hole, and filling the hole with a conductive material. I provide a few examples below.

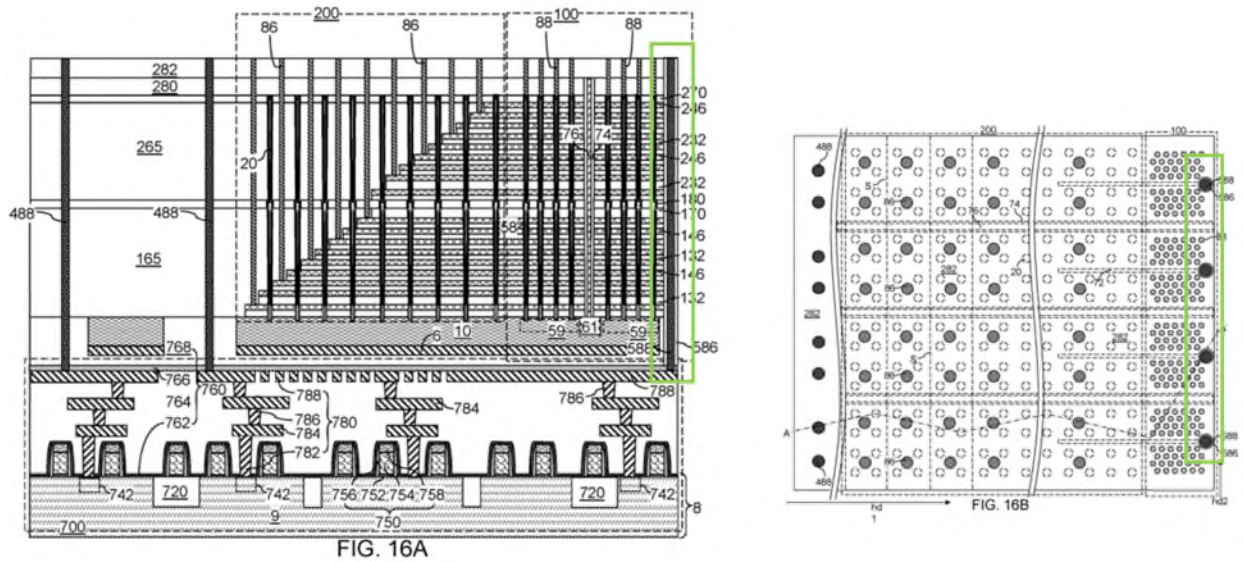
51. The below provides several examples:



69A (588)¹.



Ex. 1010 (Mushiga), 10:31-58, Fig. 5 (588).



Ex. 1011 (U.S. Pat. Pub. 2019/0229125), [0189], Figs. 16A, 16B (588). Indeed, in other prior art patents, the assignee of the '254 Patent discloses forming through-array contacts through the array. *E.g.*, Ex. 1012 (WO 2019042103) (Fig. 2, 248) and Ex. 1013 (U.S. Pat. 10,679,721), Fig. 1 (110), Abstract ("TAC").

52. The individual memory cells in a memory string are accessed by word lines that typically extend horizontally and connect to a control gate for a given cell on each memory string. On the periphery of the 3D NAND device, the word lines form a staircase structure, where each subsequent word line protrudes a short distance beyond the word line above it, like a staircase, as shown below in green.

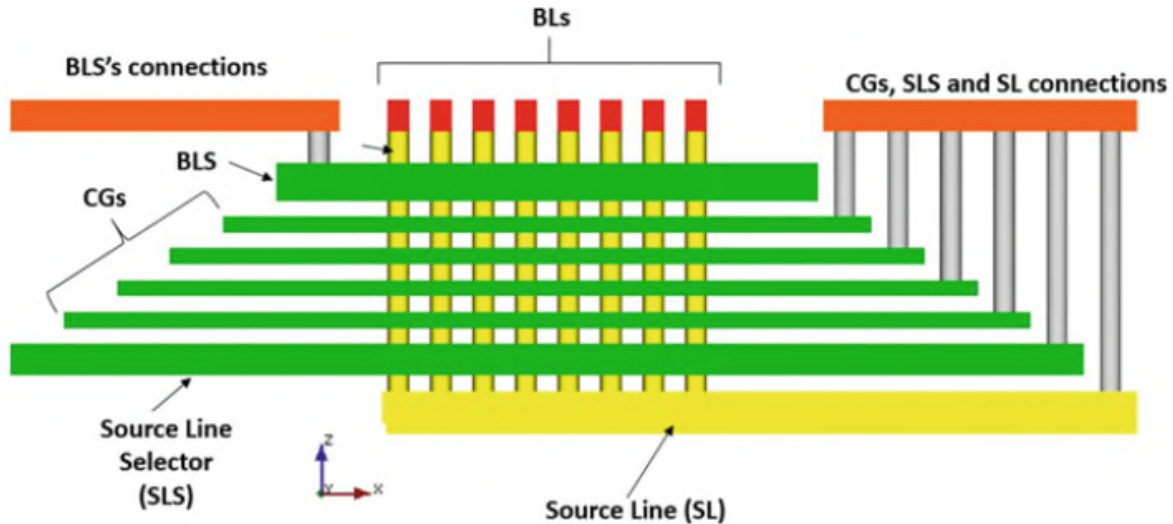


Fig. 4.12 Vertical cross section of BiCS with gate connections

Ex. 1008, 109 (green control gates forming a staircase). As noted, each word line delivers a control signal to a number of memory cells at the same horizontal level in the 3D NAND memory device.

53. The collection of memory cells controlled by a common signal together constitute a “word,” and the control gate is a “word line.” *Id.*; Ex. 1014, 38-40. The grey columns in the figure above, often referred to as “local contacts,” show how the word lines can be controlled by signals on the top surface of the 3D NAND device. In the context of 3D NAND chips, “local contacts” refer to the electrical connections made within the memory device to link various components such as the word lines and source lines. In fact, local contacts are also often referred to as “vias,” which have been widely known and used in all sorts of semiconductor devices for many decades. These vias create vertical electrical connections between the different

layers within the 3D NAND stack. They are integral to the architecture of semiconductor devices generally, including 3D NAND technology where they enable the functional linkage of stacked memory cells across multiple layers. Note that these local contacts can be of various lengths – some long and some very short. For example, the local contacts (the grey columns in the figure above) that connect to the word lines located near the top of the memory stack are very short while the grey column that connect to the source line is much longer. Where local contacts are connecting an existing vertical structure, such as a memory string or slit, the local contacts tend to be relative short.

54. A variety of modifications to the BiCS architecture were known, including the use of slit structures to serve as source line contacts for the NAND strings. Exemplary slit structures are shown in purple below. These particular slit structures function as contacts for connecting to the source (which may be shared by some, or all, memory strings) located on the bottom of the 3D NAND device. Because slits have an insulating liner, they can separate the array into blocks, which are units of the array.

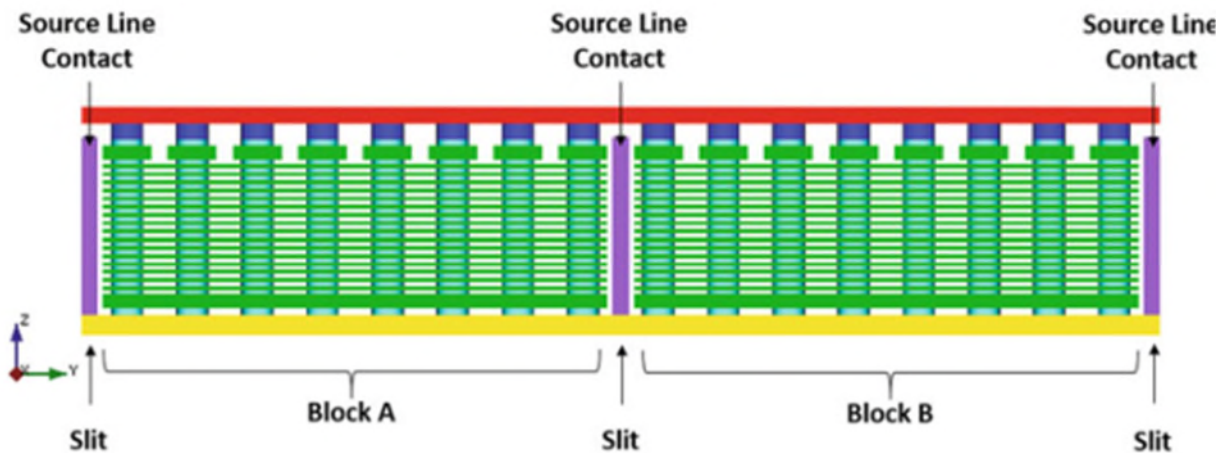


Fig. 6.8 Side view of Fig. 6.7

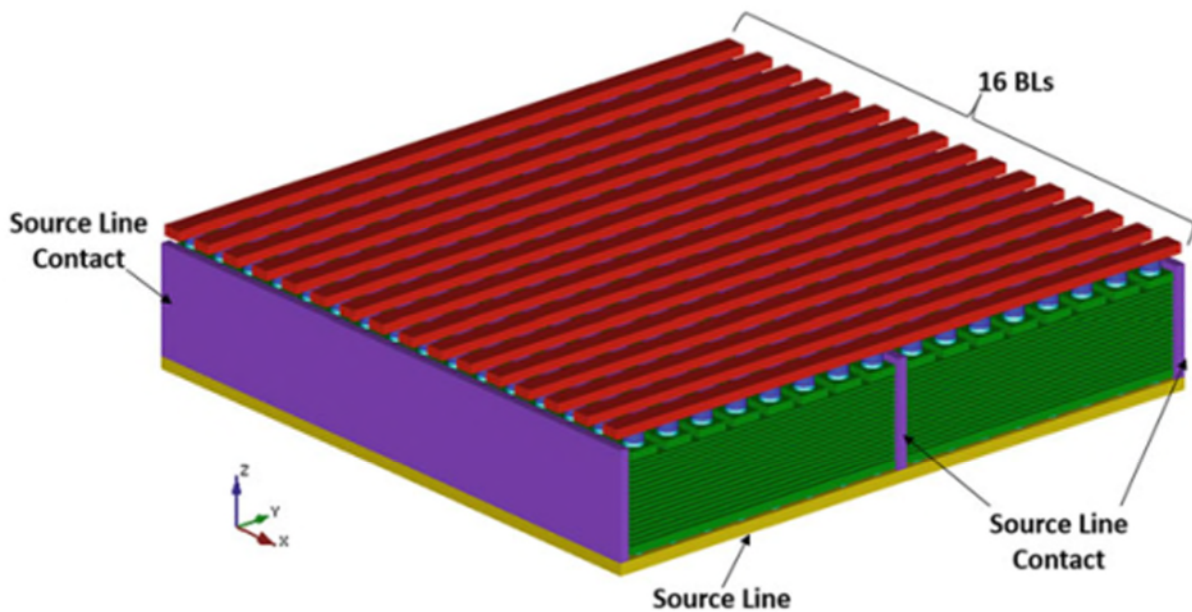


Fig. 6.7 Array slits

Ex. 1008, 185.

55. In both figures above, gaps are shown between the various structures. In actual 3D NAND memory devices, these “gaps” are not empty space; rather, they are filled with insulating material (known as “dielectric” material). Among other

things, dielectrics serve to isolate electrical signals and prevent one conductive structure from interfering with another other. Another function performed by the dielectric is mechanical support to prevent the other structures from collapsing.

56. Well before the effective filing date of the '254 Patent, companies (including Micron) had developed various techniques for manufacturing 3D NAND flash memory, many of which leveraged fabrication principles and materials that had been in use generally in the semiconductor manufacturing industry for decades.

57. The fabrication of 3D NAND memory chips involves etching techniques to construct vertical, high-density storage architectures. These etching processes, fundamental to semiconductor manufacturing, have been well established prior to 2018 but have been adapted for 3D NAND. Here are just a few examples of etching processes used for 3D NAND. Channel hole etching which typically makes use of a dry etching process, e.g., deep reactive ion etching (DRIE) to create vertical channels through the NAND stack. DRIE was developed in the mid-1990s, allows for etching with high aspect ratios, essential for the vertical structures in 3D NAND. Staircase etching involves sequential etching steps to create a staircase-like structure for accessing word lines across each memory layer. This process leverages standard lithographic and etching techniques known long before 2018, adapted to create the precise, repetitive structures needed for multi-layer access. Hard-mask etching process, well-known long before 2018, involves depositing a durable

material like nitrides which is then patterned using photolithography to serve as a mask. The hard mask protects underlying layers during subsequent etching. Selective etching is used to remove specific materials without damaging others by using different chemistries in plasma to target certain layers of materials, again was well-known long before 2018. Spacer etching which involves depositing and then partially removing the material developed to define narrow, uniform spacers (gaps) for cell isolation. Spacer etching processes was developed for lightly-doped drain (LDD) MOSFETs back in the 1980's and adapted for 3D NAND manufacturing process. Each of these processes originates from fundamental techniques known in semiconductor manufacturing well before 2018, adapted for the advanced architecture of 3D NAND.

58. Stacking multiple chips, also known as 3D integration, was just one of many advancements in semiconductor technology that have happened over the years. The concept of 3D integration should not be confused with 3D NAND. Although 3D integration has application to 3D NAND chips, the concept of vertically stacking multiple dies/chips predates 3D NAND by many years and has been used extensively in a variety of chip technologies. This method significantly enhances device performance and functionality while conserving space, addressing the limitations faced by traditional planar scaling methods. Naturally, when stacking multiple dies on top of one another, via structures (also called through-silicon vias

(TSVs) or through-array contacts (TACs)) were implemented to provide connections between different chips in the stack. I discuss and provide examples of TACs above.

59. In summary, techniques for manufacturing 3D NAND memory devices, including TACs and slits, were well-known in the art before the '254 Patent's effective filing date.

VII. THE '254 PATENT

A. Effective Filing Date

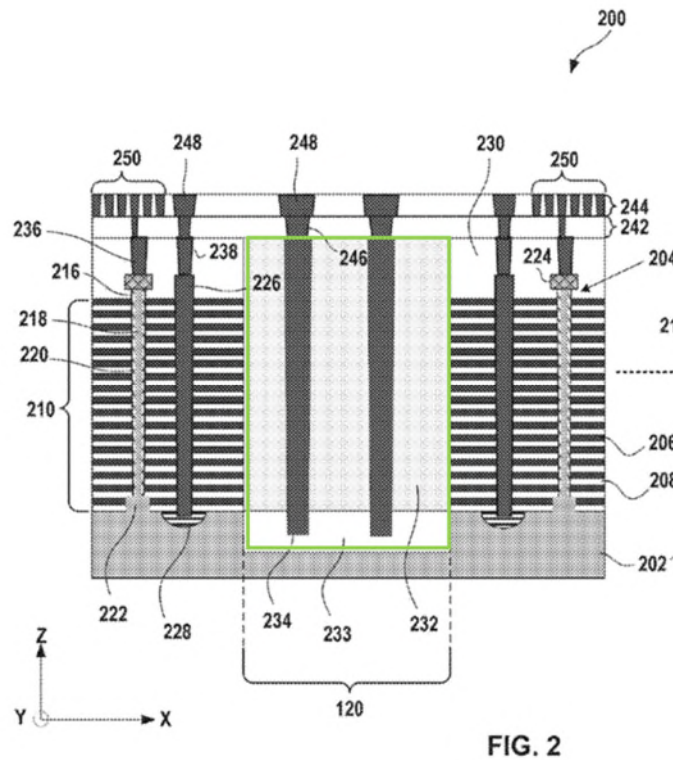
60. Based on my review of the '254 Patent, I note that it also references a PCT application on its face, which was filed August 21, 2018.

61. For purposes of this declaration, I have been asked to assume that August 21, 2018 is the effective filing date of the '254 Patent. My opinions in this declaration were formed from the perspective of a POSITA as of August 21, 2018, including both the knowledge of a POSITA at that time as well as how a POSITA would have understood the '254 Patent and the prior art.

B. Overview

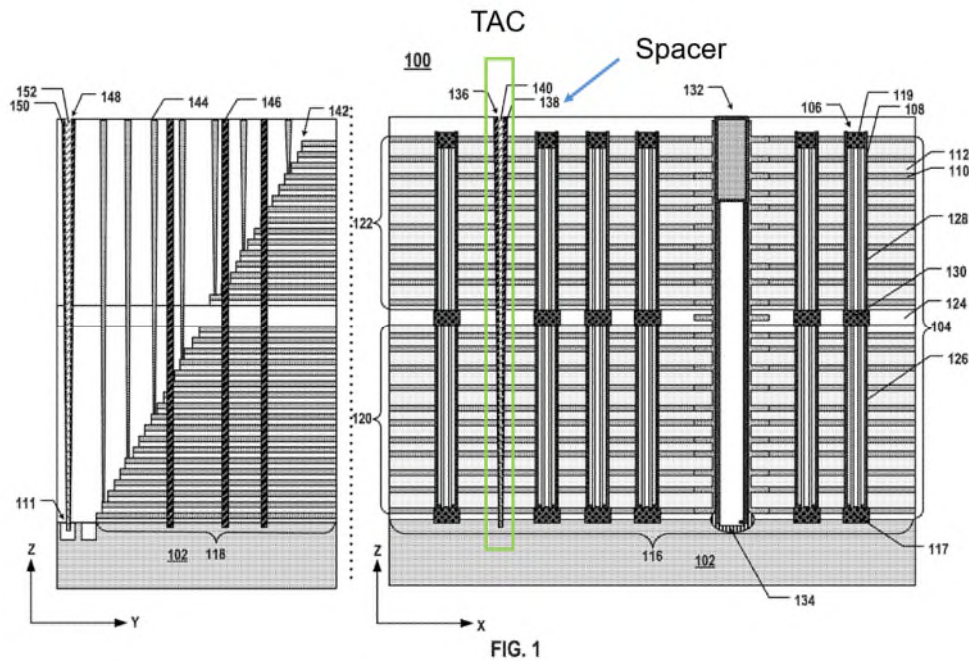
62. The '254 Patent's title specifically highlights TACs: "Three-dimensional memory devices having through array contacts and methods for forming the same." As I describe in Section VI, and as the '254 Patent describes, TACs extend through the memory stack. Ex. 1001, 8:28-60. The '254 Patent alleges there are issues with forming TACs through a "barrier structure." *Id.*, 4:55-5:20.

While the '254 Patent does not depict a barrier structure, it appears that the '254 Patent is referring to, for example, a rectangular block of oxide through which conductive contacts extend. For example, after etching out a rectangular area of the stack and filling that void with oxide forms such a barrier structure. This provides an insulating structure so that pure conductive core TACs can extend through the structure. Below is such a structure from another YMTC patent (the assignee of the '254 Patent):



Ex. 1007 (U.S. Pat. 10,658,378), Fig. 2 (120).

63. Instead of using a barrier structure, the '254 Patent teaches employing a thin spacer (138) for each TAC, which also provides the same insulating function.



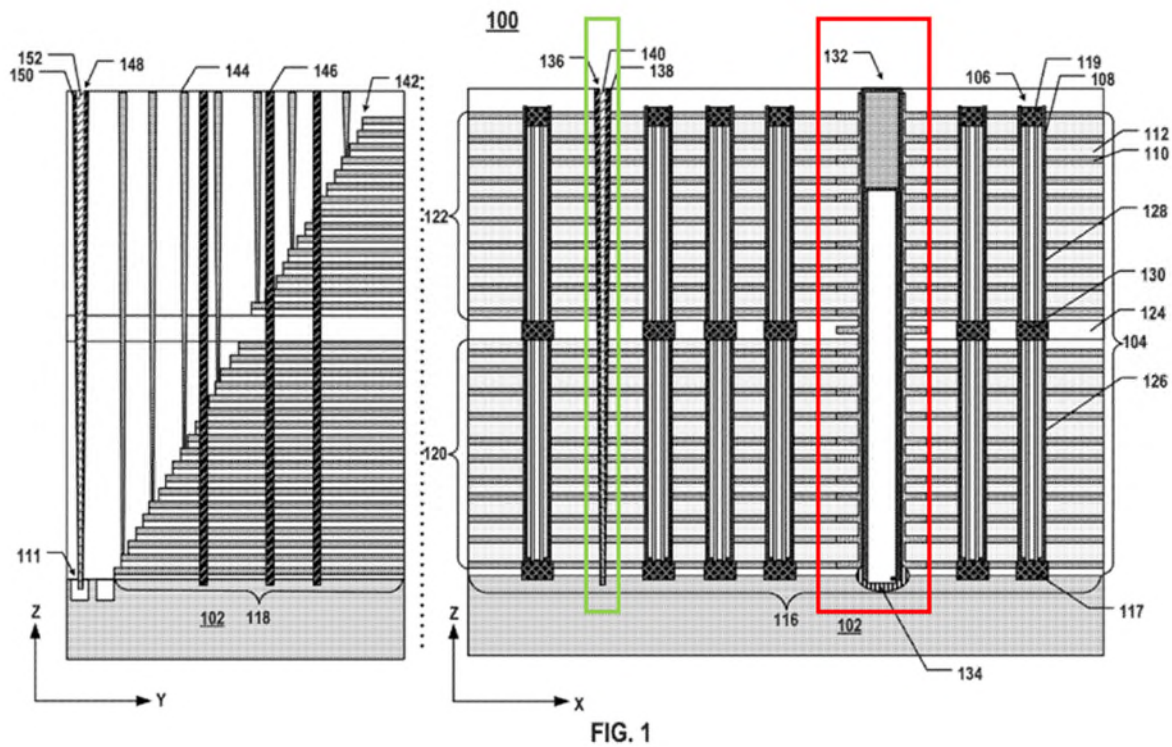
Ex. 1001, Abstract, 4:55-5:20.

64. As shown above, the TACs include a dielectric, e.g., silicon oxide, spacer (138) to insulate the TAC from the memory stack (e.g., the conductive gate layers) and a conductive core (140). Ex. 1001, 8:45-60. Recall that gate layers are conductive, and thus an insulator liner is necessary to prevent short circuiting the gate layers. The conductive core enables the TAC to connect devices above and below the array, i.e., provide an electrical coupling between such devices. *Id.*, 4:55-59.

65. I summarize the file history below. The file history suggests that the Examiner may have found forming a slit after the TACs to be the alleged point of

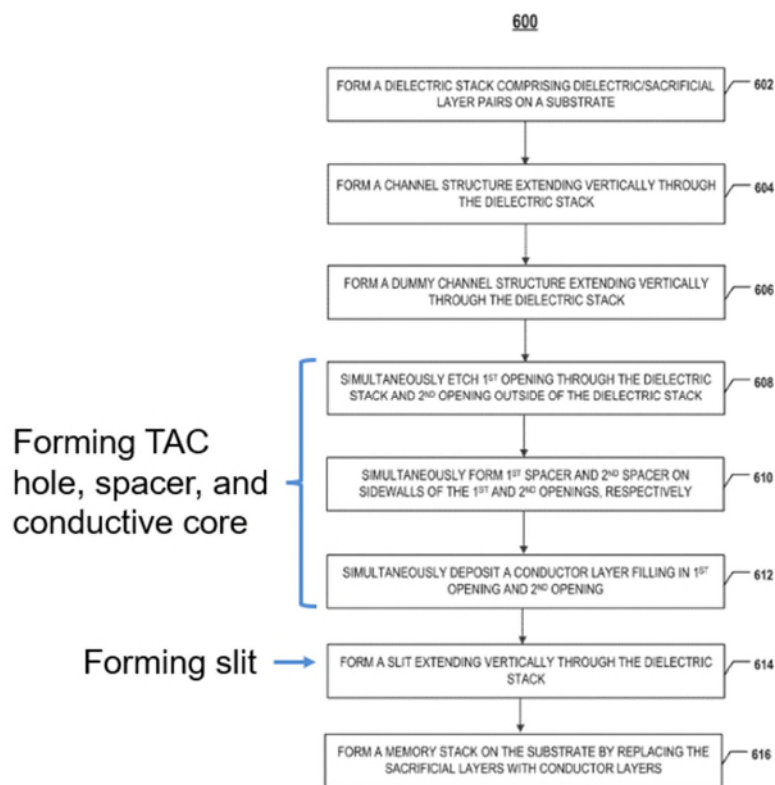
novelty. Ex. 1001, Abstract. The Abstract highlights this timing requirement, and this timing requirement is a requirement of each independent claim.

66. As I describe in Section VI, slits were well known and textbook material. Shown below in red, the slit structure (which fills the open slit) can include a conductor core and dielectric spacer, and thereby interconnect a source voltage (above the array) to a common source in the substrate (below the array). Ex. 1001, 8:1-27. The slit can extend laterally (in the Y-direction, into the page) and therefore segment the array into blocks. *Id.* The slit (while a void) can be used in the gate replacement process to replace the sacrificial gates with conductive gates. *Id.*, 14:44-62. That is, this void allows for the etching of the sacrificial gate and then the deposition of the conductive gates, e.g., forming tungsten conductive gates.



Id., Fig. 1.

67. The '254 Patent's Figure 6 depicts a process flow and the process steps in order. As can be seen, the '254 Patent describes forming the slits after forming the TACs:



Ex. 1001, Fig. 6; *see also id.*, Fig. 3B, 12:24-63 (forming TACs holes), Fig. 3C-E, 12:64-14:19 (various ways to form spacer), Fig. 3F, 14:20-43 (forming conductive core for TAC), Fig. 5A, 14:44-15:12 (forming slit), Fig. 5A, 15:12-24 (filling slit).

C. Prosecution History

68. As noted above, I have reviewed the '254 Patent's file history. The file history is quite short with no rejections over the prior art. On October 26, 2020, the claims were allowed, and the Notice of Allowance highlights forming the TAC and then after forming the TAC, forming the slit: "forming a spacer on a sidewall of the first opening; forming a through array contact (TAC) extending vertically through

the stack by depositing a conductor layer over the spacer in the first opening; and after forming the TAC, forming a slit extending vertically through the stack.” Ex. 1002, 133-34. This strongly suggests that the timing requirement is the alleged point of novelty, because as I describe in Section VI, both of these structures were well known in the art.

VIII. CLAIM CONSTRUCTION

69. I am not a legal expert or an attorney and offer no opinions on the law. I understand that claim construction is a matter of law. However, I have been informed by counsel of the legal standards that apply to claim construction in an *inter partes* review, and I have applied them in forming my opinions. I understand that during an *inter partes* review, the same claim construction standard used in federal district court is applied when addressing the meaning of claim terms.

70. I have been informed that the words of a claim are generally given their plain and ordinary meaning that the term or phrase would have to POSITA at the time of the invention in view of the surrounding claim language, the specification and the file history (collectively, the “intrinsic evidence” or “intrinsic record”).

71. I also understand that courts may consider extrinsic evidence, such as expert and inventor testimony, dictionaries, and learned treatises (collectively, the “extrinsic evidence” or the “extrinsic record”), but that such extrinsic evidence should be given less weight than the intrinsic evidence.

72. In my opinion, the challenged claims do not require further construction and can be afforded their plain and ordinary meaning for purposes of the analysis of the prior art that I am conducting in this declaration.

IX. UNPATENTABILITY ANALYSIS

73. For the reasons I explain in greater detail below, it is my opinion that as of the effective filing date of the '254 Patent, claims 1-15, 17-18, and 20 of the '254 Patent are unpatentable as obvious over the prior art discussed in this declaration.

A. Overview of the Prior Art

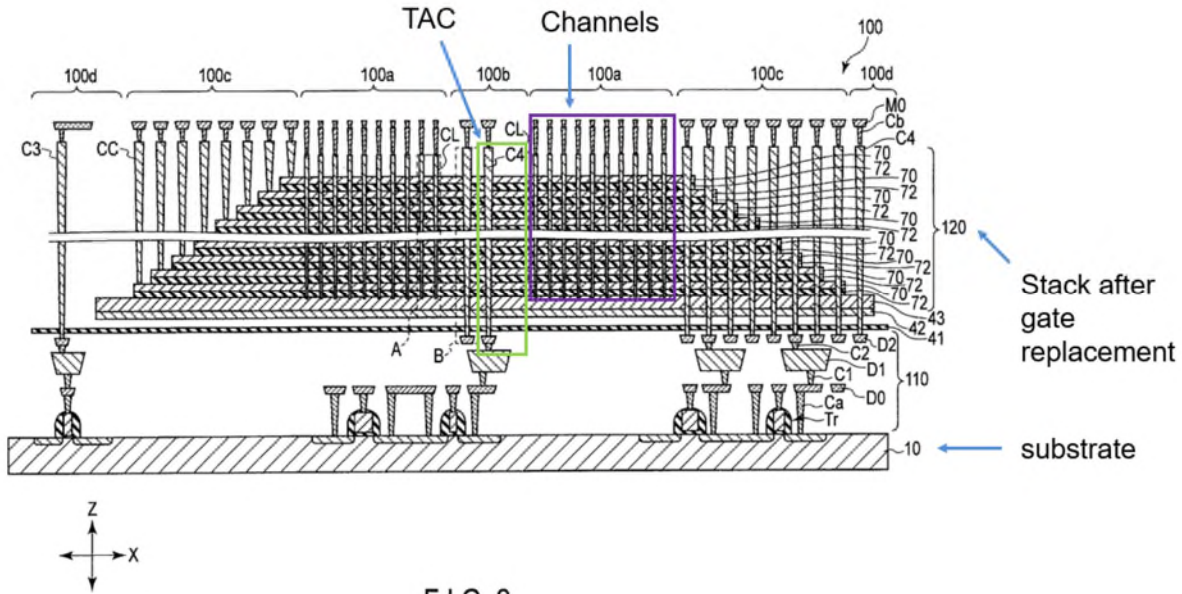
74. The following paragraphs provide an overview of the primary reference that I discuss throughout this declaration.

1. Nakajima

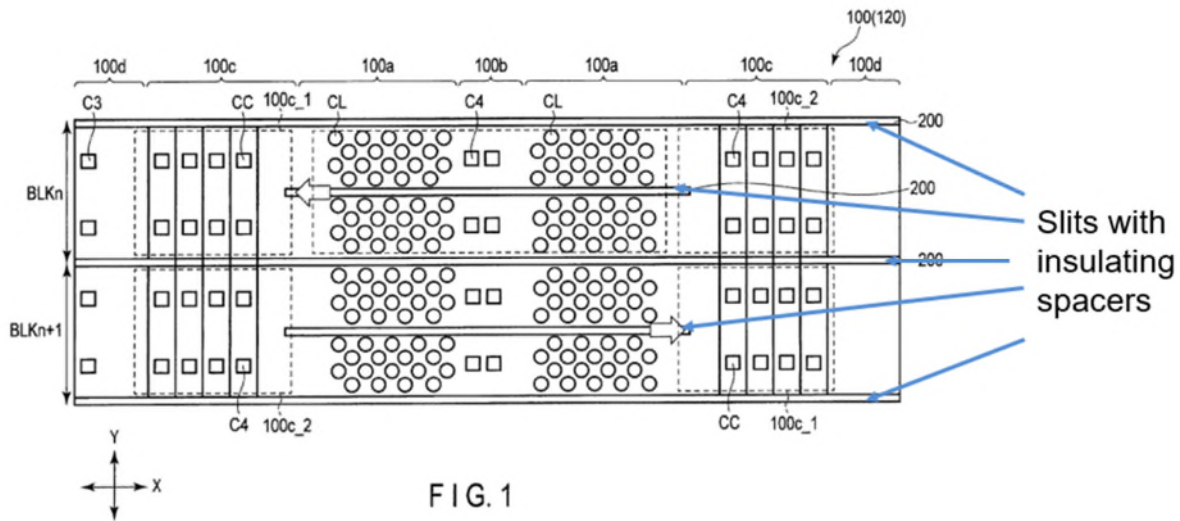
75. Nakajima discloses forming a TAC through the memory stack and then forming the slit. As I discuss in Section VII, this appears to be alleged point of novelty of the '254 Patent.

76. Nakajima refers to its TACs as "C4": "The contact area 100*b* includes contacts C4. A contact C4 couples an interconnect in an upper layer of the layer stack 120 and an interconnect in a lower layer of the layer." Ex. 1005, 2:66-3:2. Contact area 100*b* can be seen below Figures 1 and 2 and is in the memory stack region.

77. Nakajima discloses: “A process of manufacturing the contact C4 will be described below. ... [a] hole H1 extending in the Z-direction is formed Next, . . . The silicon oxide layer 81 is conformally formed along the bottom and the side surface of the hole H1. Next, as shown in FIG. 10, a portion of the silicon oxide layer 81 that is located at the bottom of the hole H1 is removed Next, the metal layer 82 is formed on the inner surface of the silicon oxide layer 81 in the hole H1 . . . Next, although not shown in the drawing, slits are formed in the layer stack 120 by the RIE method using a mask layer. The slits penetrate the insulation layers 44 and 64 and the layer stack 120, to reach the polysilicon layer 43.” Ex. 1005, 7:8-8:15. As can be seen, Nakajima forms the TACs by etching a hole, depositing a dielectric (silicon oxide) liner, removing the bottom portion of the liner (so that the TAC contacts an underlying element), and then filling the remaining hole with a conductive material. The TACs and slits are shown respectively below:



Id., Fig. 2.



Id., Fig. 1.

**B. Ground 1: Nakajima in View of the Knowledge of a POSITA
Render Obvious Claims 1-15, 17-18, AND 20**

1. Claim 1:

[1.PRE] “A method for forming a three-dimensional (3D) memory device, comprising:”

78. I offer no opinion as to whether the preamble is limiting. But Nakajima discloses it. Specifically, Nakajima discloses a method for forming a three-dimensional (3D) memory device (“semiconductor device 100”). Ex. 1005, 1:14-16 (“Embodiments described herein relate generally to a semiconductor device and a method of manufacturing the same.”), 2:26-30 (“A semiconductor device 100 ... In this embodiment, a three-dimensionally-stacked type NAND flash memory will be described as an example of the semiconductor device.”), Figs. 6-12, 7:5-9 (describing fabrication). Note that it is “three-dimensional” because of the memory stack and the vertical memory pillars that extend through the stack.

[1.A] “forming a stack comprising a plurality of dielectric/sacrificial layer pairs on a substrate;”

79. As I discuss below, Nakajima discloses forming a stack (“layer stack” 120) comprising a plurality of dielectric (“silicon oxide layers” 72)/sacrificial layer (“sacrifice layers 71”) pairs on a substrate (e.g., “substrate 10”). I first note that the ’254 Patent states: “It should be readily understood that the meaning of ‘on,’ ... in the present disclosure should be interpreted in the broadest manner such that ‘on’ not only means ‘directly on’ something *but also includes the meaning of “on”*”

something with an intermediate feature or a layer therebetween.” Ex. 1001, 3:52-61².

80. The '254 Patent also defines “substrate” broadly. Specifically, the substrate need not be the bottom, base substrate, and can be a layer above that if it serves as the base, for example, for the memory stack. Specifically, the '254 Patent states: “As used herein, the term ‘substrate’ refers to a material onto which subsequent material layers are added.” Ex. 1001, 4:6-15.

81. These claim elements (except for the sacrificial layers, which are now conductive layers) are shown in Nakajima’s Figure 2 below. Note the below shows conductive gates because at this point, the gate replacement process is complete (recall conductive gates replace the sacrificial gates as part of the gate replacement process).

² Emphasis added throughout unless noted.

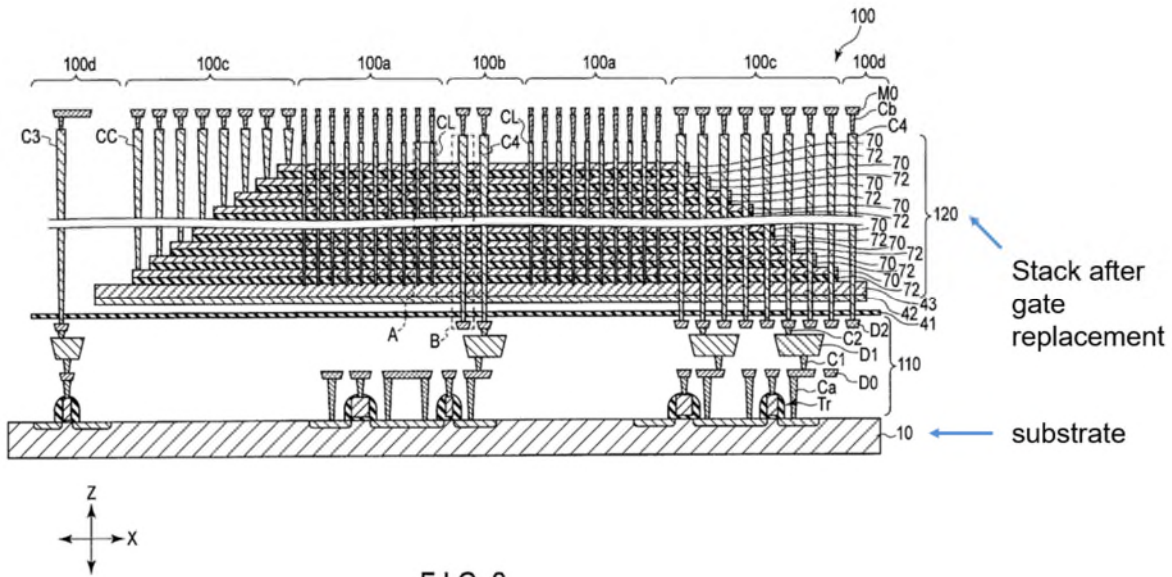
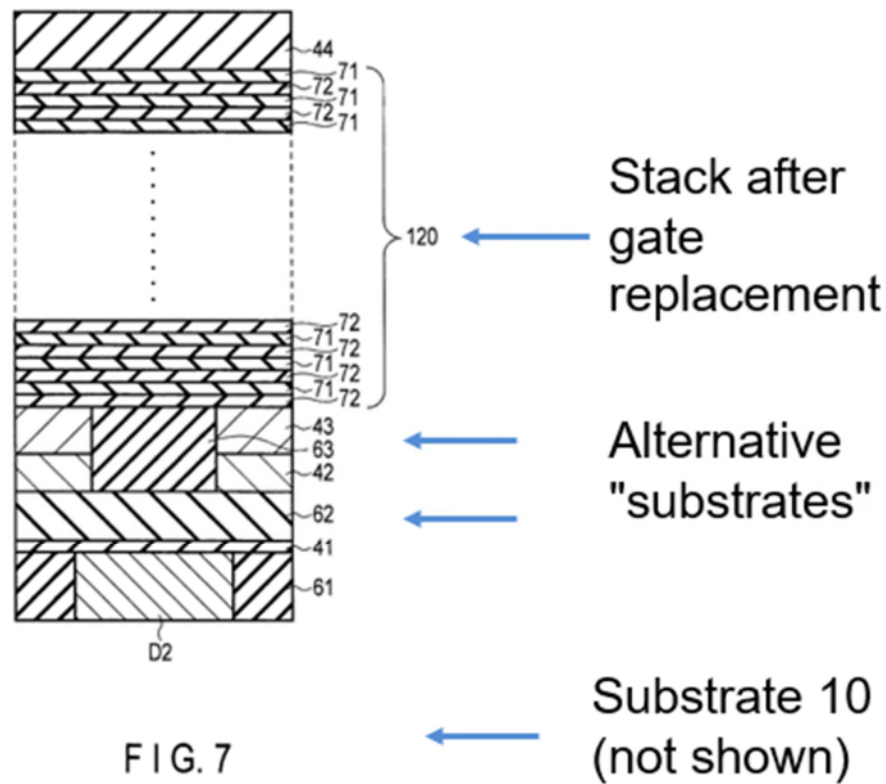


FIG. 2

Ex. 1005, Fig. 2.

82. Given the '254 Patent's definition of "substrate," the substrate may be substrate 10 or polysilicon layer 43. Nakajima describes forming the memory stack on polysilicon layer 43. "Next, the insulation layers 72 and sacrifice layers 71 are alternately stacked on the polysilicon layer 43 and the insulation layer 63. . . . For example, the sacrifice layers 71 are silicon nitride layers, and the insulation layers 44, 62, 63, and 72 are silicon oxide layers." Ex. 1005, 7:26-36. Note that silicon oxide layers are dielectric layers (and a common dielectric layer for this application).



Ex. 1005, Fig. 7.

[1.B] “forming a channel structure extending vertically through the stack;”

83. As I describe below, Nakajima discloses, or renders obvious, forming a channel structure (a “pillar structure” “CL” 120) extending vertically through the stack (120).

84. First, Nakajima discloses a channel structure, namely, pillar structures CL. These channel structures are vertical string of memory cells, wherein the memory cells intersect with respective gate layers (that is, the word lines):



Ex. 1005, Fig. 2, 5:16-21 (“The pillar structures CL continuously extend in the insulation layer 44 and in the layer stack 120 in the stacking direction (Z-direction). The pillar structures CL include a core layer 50, a semiconductor layer 20, and a memory layer 30, which are provided in the mentioned order from the center.”).

85. The channel structure extends through the memory stack (120) down to polysilicon layer 43: “**A semiconductor layer 20 is provided around the core layer 50 in a pillar structure CL.** Namely, the semiconductor layer 20 is provided between the core layer 50 and the memory layer 30. The semiconductor layer 20 includes a body layer 20b ... **A lower end of the body layer 20b contacts the polysilicon layer 43.**” Ex. 1005, 5:26-33; *see also id.*, Fig. 3. Recall that the memory stack is on polysilicon layer, so the channel structures extend completely through it.

Indeed, the channel structure must extend through the stack, because the bottom of the channels must extend into the common source region under the stack.

86. To the extent that PO were to argue that forming the channels must occur before the TACs and slits, I would disagree. I note that this limitation does not recite when it occurs, whereas the final limitation does state a relative time when it occurs (after from the TAC). In any event, Nakajima would have been understood to disclose, and at least renders obvious, forming the channels before the TACs and slits. Nakajima focuses on the manufacture of the TACs, and thus starts the description of the manufacturing process there. Ex. 1005, 7:5-8. This is not uncommon to a POSITA. When Nakajima describes forming the TACs (C4s), he then describes forming the slits and replacing the sacrificial gates. *Id.*, 7:5-8:23. Nakajima describes that the channel pillars support the structure during the gate replacement process, and thus a POSITA would have understood, and it certainly would have been obvious, that Nakajima discloses forming the channels before the TACs (C4) and slits. *Id.*, 8:24-33. Also, in my analysis of claim [2], I describe that it was well known to form channels and dummy structures before fabricating the TACs and slits. This is because these structures beneficially support the stack during the gate line replacement process. See Claim [2] analysis. During that process, the sacrificial gates become voids, and structural support is necessary.

[1.C] “forming a first opening extending vertically through the stack;”

87. As I describe below, Nakajima discloses forming a first opening (H1) extending vertically through the stack (120).

88. As seen in the final memory device (Figure 2), Nakajima discloses contacts C4.

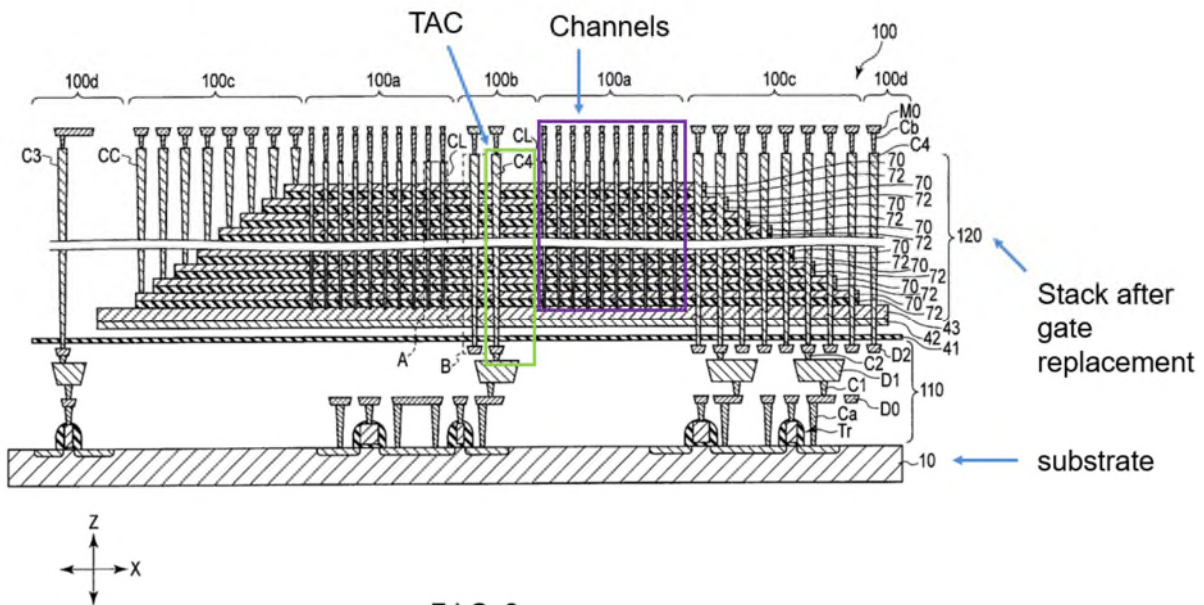


FIG. 2

Ex. 1005, Fig. 2.

89. To form C4, Nakajima first etches a first opening (“hole H1”) extending vertically through the stack (120): “[A] hole H1 extending in the Z-direction is formed in the insulation layers 44, 62, and 63, and the layer stack 120, as shown in FIG. 8. The hole H1 is formed by, for example, reactive ion etching (RIE) using a mask layer not shown in the drawing. The hole H1 penetrates the insulation layers 44, 62, and 63, and the layer stack 120, to reach the silicon nitride layer 41.” Ex.

1005, 7:37-43. That hole must extend through the stack because ultimately, the C4 connects elements above and below the stack.

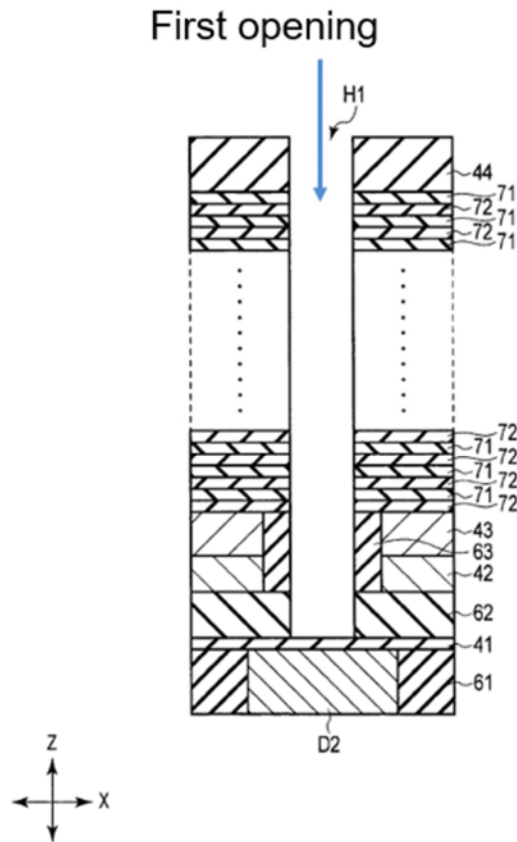


FIG. 8

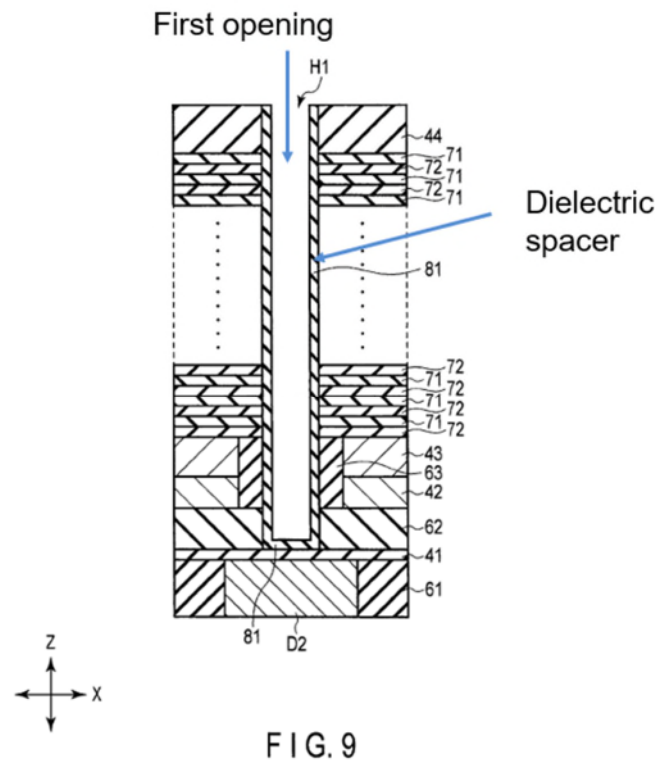
Id., Fig. 8.

[1.D] “forming a spacer³ on a sidewall of the first opening;”

90. As I describe below, Nakajima discloses forming a spacer (“oxide layer 81”) on a sidewall (“inner surfaces”) of the first opening (“hole H1”).

91. Specifically, Nakajima discloses: “Next, the silicon oxide layer 81 is formed on the inner surfaces of the layer stack 120 and the insulation layers 44, 62, and 63 in the hole H1, and on the silicon nitride layer 41, as shown in FIG. 9. The silicon oxide layer 81 is conformally formed along the bottom and the side surface of the hole H1.” Ex. 1005, 7:44-49. As can be seen, the spacer forms on the bottom of the hole, which is a natural result of the deposition.

³ The ’254 Patent describes a “spacer” as a dielectric material, e.g., silicon oxide, on the sidewalls of the hole. Ex. 1001, 8:45-60. An insulating liner refers to the same structure. The spacer separates the conductive core from the memory stack.



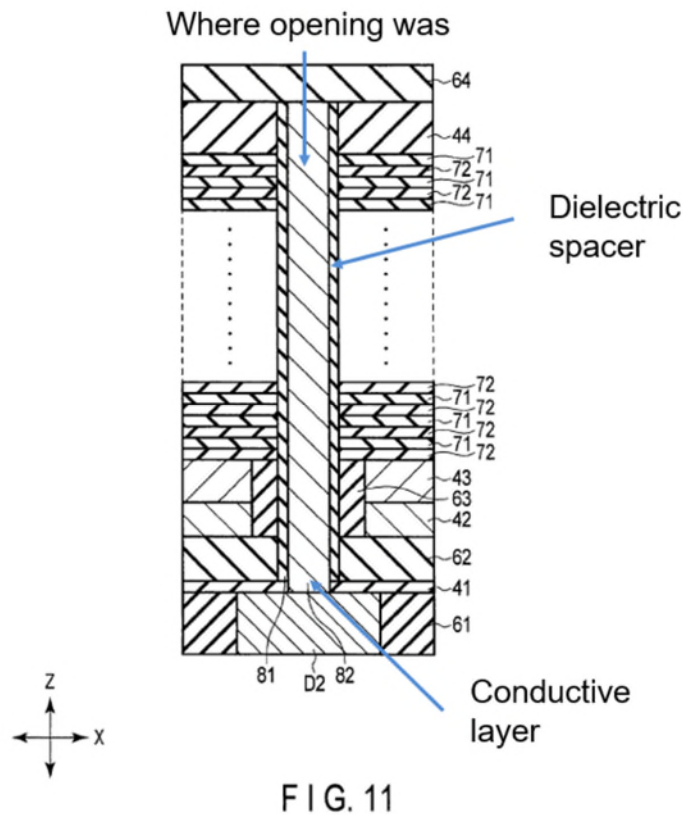
Id., Fig. 9.

[1.E] “forming a through array contact (TAC) extending vertically through the stack by depositing a conductor layer over the spacer in the first opening; and”

92. As I describe below, Nakajima discloses forming a through array contact (TAC) (“C4”) extending vertically through the stack by depositing a conductor layer (“metal layer 82”) over the spacer (“oxide layer 81”) in the first opening (“hole H1”).

93. As I describe above in [1.C], the C4 extends through the stack. The C4 includes a metal core (“metal layer 82”) and dielectric spacer (“silicon oxide layer 81”). Ex. 1005, 6:45-52. “[T]he metal layer 82 is formed on the inner surface of the

silicon oxide layer 81 in the hole H1.” *Id.*, 7:62-63. Note that Nakajima first removes the bottom portion of the spacer (which relates to a subsequent dependent claim).



Ex. 1005, Fig. 11.

94. The '254 Patent uses “over the spacer” to refer to filling the hole (with the spacer) as shown above. Ex. 1001, Figs. 3E-F, 13:62-64, 14:20-44.

95. Nakajima’s C4 extends through the stack and interconnects devices that are above and below the stack: “A contact C4 couples an interconnect in an upper layer of the layer stack 120 and an interconnect in a lower layer of the layer stack

120 with each other.” Ex. 1005, 2:66-3:2. This is because the C4 provides an electrical coupling between elements above and below the stack.

96. Were PO to argue that “forming the TAC” must include forming connections thereon, I would disagree for two reasons. First, the claim language defines the final step of forming the TAC as filling it with a conductive core (“forming a through array contact (TAC) extending vertically through the stack by depositing a conductor layer”). That is, the “TAC” of claim 1 is complete after filling the hole (with the spacer) with the conductive core. Second, the specification does not describe forming connections on the TAC before forming the slit. Ex. 1001, 14:20-57, Fig. 6 (steps 612, 614). This would also be non-standard, because after forming all elements, e.g., also the slit, the manufacturing process moves on to forming interconnects to those structures, e.g., TACs and slits, to couple those elements to elements above the stack.

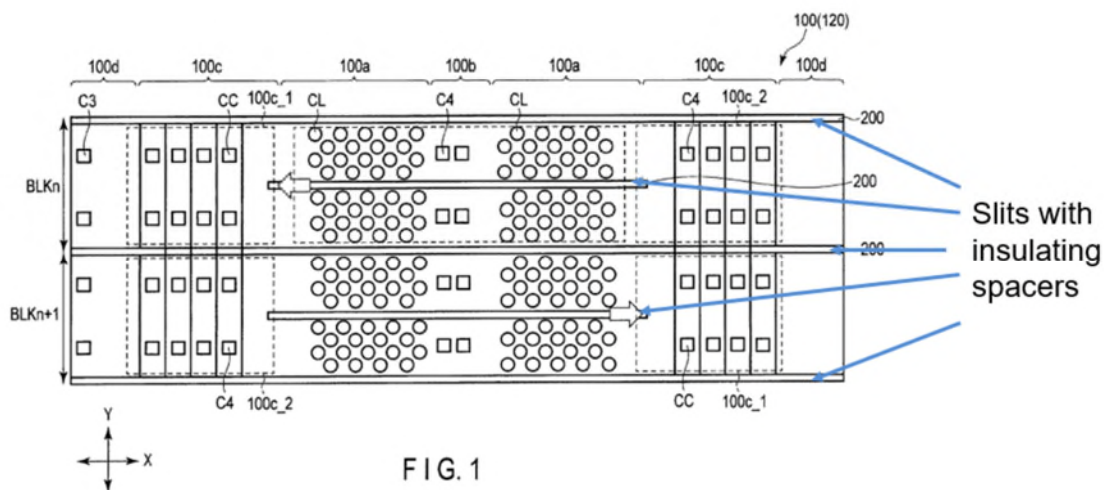
[1.F] “after forming the TAC, forming a slit extending vertically through the stack.”

97. As I describe below, Nakajima discloses after forming the TAC (C4), forming a slit (“slit”) extending vertically through the stack (“layer stack” 120).

98. Nakajima discloses forming the TAC. Ex. 1005, 7:62-65. After this, Nakajima discloses forming slits that extend vertically through the stack, i.e., from above the stack (layer 64) to below the stack (layer 43): “Next, although not shown in the drawing, slits are formed in the layer stack 120 by the RIE method using a

mask layer. The slits penetrate the insulation layers 44 and 64 and the layer stack 120, to reach the polysilicon layer 43.” Ex. 1005, 8:12-15, Fig. 11. I describe slits generally at Section VI. Slits is a well-known term.

99. The slits become “isolation” structures 200 that extend laterally along the X direction. I describe how these separate the array in Section VI. Specifically, Nakajima discloses: “Thereafter, an insulation layer is formed on the side surface and at the bottom of the slits, although not shown in the drawing. Thereby, the slits are filled, and the isolation section 200 shown in FIG. 1 is formed.” Ex. 1005, 8:34-37.



Id., Fig. 1.

2. Claim 2:

[2] “The method of claim 1, further comprising prior to forming the first opening, forming a dummy channel structure extending vertically through the stack.”

100. As I describe below, Nakajima in view of the knowledge of a POSITA render this limitation obvious.

101. With respect to “prior to forming the first opening,” as I demonstrate in my analysis under [1.B], it would have been understood that Nakajima forms the channels before the TACs. As I describe below, it would have been understood and certainly obvious (a POSITA would have been motivated with a reasonable expectation of success) that Nakajima also forms dummy channels for several reasons.

102. First, it has been well known for decades that elements, such as channel structures, at the end of an array are subject to process variations. Ex. 1020 (U.S. Pat. 5,945,717), 8:47-53 (“In a typical flash cell array, cells located at the edge of the array are much more subject to processing variations than the cells not located at the edge. Because of this, it is common to refrain from using the cells at the array edge. Such cells, which extend around the perimeter of the array, are sometimes referred to as dummy cells.”). For modern processes, this has become even a greater issue. Ex. 1021 (U.S. Pat. 10,347,487), 2:20-43 (“Edge of array issues may typically occur at the boundary between a chop mask and pitch double patterning. An abnormality at the edge of an array pattern can cause blowout or shorting issues,

depending on the integration process. Conventionally, an abnormal edge pattern at the edge of array may be controlled by adding a dummy pattern region, which is later sacrificed in processing.”). Thus, one normally employs dummy channel structures at the edge of the array. Otherwise, these channel structures may be defective, and not properly store data.

103. Second, adding dummy channels such that the overall pattern is more consistent was well known for decades, too. Ex. 1022 (Ronse), 11 (“As a result, this technique is particularly useful in regular patterns like memories, and much less in random logic designs where features can be completely irregular.”). Semiconductor fabrication involves patterning, and patterning periodic structures is much more difficult than a consistent pattern due to, for example, pattern distortion. Thus, again, the use of dummy structures was the norm to reduce fabrication issues.

104. Third, dummy channels provide structure support, which is important during the gate line replacement process (because that process forms voids where the sacrificial gates were, necessitating support members to prevent the stack from collapsing). This was well known in the art. It was known that to perform this gate replacement process, “support pillars” were necessary. Ex. 1018 (U.S. Pat. 8,945,996), 5:64-6:2, 7:19-23; Ex. 1019 (U.S. Pat. 10,115,632), 30:14-27; *see also id.*, 15:3-22 (structures 20 are dummy channel structures). I note that it was well known to include dummy support members that extend through the entire stack or

partially through the stack. Ex. 1015 (Kai), Fig. 6A (support members 20), 16:28-38. For example, the dummy channels may be on the edge of the array or in the staircase region.

105. Kai, for example, discloses forming active and dummy channels, which provide structural support. Ex. 1015 (Kai), 9:23-26 (defining “support opening” as “a structure in which a support structure (such as a support pillar structure) that mechanically supports other elements is subsequently formed”), 9:45-48 (“support openings 19” extend through stack), 10:20-27 (forming channels in support openings). Kai refers to the dummy channels as “support pillar 20” and active channels as “memory stack structured.” *Id.*, 16:28-38; Fig. 15A, 25:58-63 (dummy support channels (20) have no connection to the upper level, whereas the active channel structures (55) include contacts (88)).

106. Park provides another similar example of forming active and dummy, supporting channels. Ex. 1016 (Park), 6:19-26, 7:45-51.

107. Kim provides another similar example of forming active and dummy, supporting channels. Note dummy channel structures can be made at the same time as active channels, and if the dummy channels have all the same materials as the active channels, this saves process times. Ex. 1017 (U.S. Pat. Pub. 2018/0308559) [0047] (“The stack structure ST may be penetrated with a plurality of dummy holes DH on the connection region CTR,” “DS may physically support,” and listing same

materials as channels), [0071] (“The channel holes CH and the dummy holes DH may be formed at the same time.”), [0072] (same time), Fig. 13 (DH through stack on edge).

108. Fourth, as I note above, dummy channels can be made by the same process and at the same time as the active channels. Ex. 1015 (Kai), 10:20-27. The dummy channels, however, typically will not include interconnects to upper-elements, because the structures do not store data. Thus, dummy channels do not consume space above the structures, but still function as support members (and have the processing benefits that I describe above).

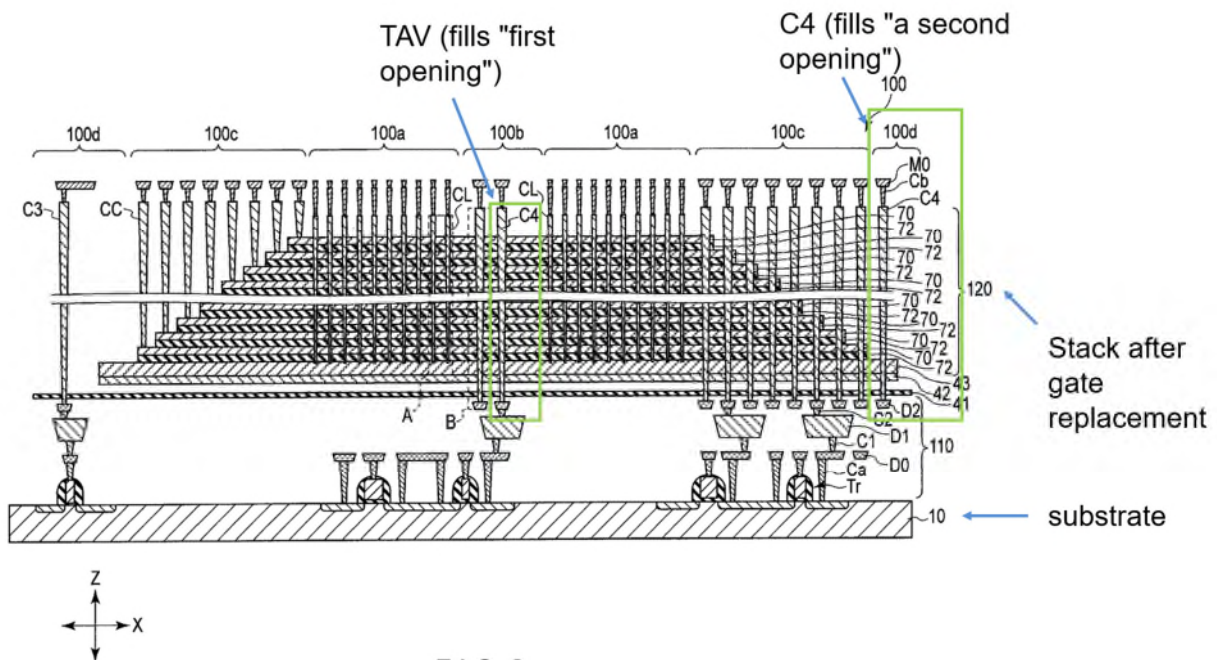
109. Finally, employing dummy structures would have been routine and a POSITA would have had a high expectation of success in doing so. First, Nakajima already discloses forming channel structures. Simply not connecting a channel structure to upper-level interconnects, such that it is an active channel, forms a dummy channel. The materials in the active and the dummy channels can be exactly the same. Also, I describe above that the addition of dummy channel structures actually reduces processing issues, such as defective bits and simplifies patterning. And again, these were commonplace and textbook material for decades.

3. Claim 3:

[3] “The method of claim 1, wherein forming the first opening comprises simultaneously etching the first opening through the stack and a second opening outside of the stack.”

110. As I describe below, Nakajima discloses, or renders obvious, this limitation.

111. As my analysis in claim [1.C] demonstrates, Nakajima discloses forming holes H1 through the stack for its TACs (C4). Nakajima discloses, however, both C4 structures though the array and that extend through the insulating fill over the staircase. Shown below, one C4 is completely outside the stack:



Ex. 1005, Fig. 2.

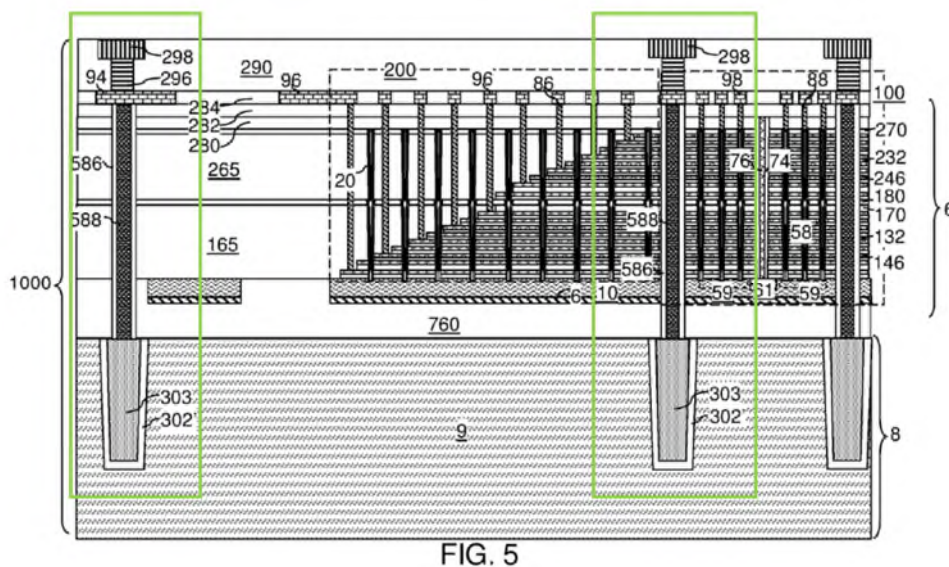
112. It would have been understood that Nakajima forms the holes for these two C4 structures at the same time. As I describe below, it was the norm to form all instances of a contact type at the same time. This is consistent with Nakajima's disclosure, because Nakajima discloses only one step for creating the H1 holes for the C4 structures. Ex. 1005, 7:37-43. Likewise, Nakajima only discloses one set of steps for forming the C4 contacts. *Id.*, 7:5-8:11.

113. In my opinion, it would also be obvious to form the two above C4 holes at the same time. Importantly, it would significantly reduce processing time. Even simply etching the holes requires multiple steps, e.g., forming a mask, etching the hole, etching out the bottom, potential clean steps, etc. Repeating this process for two different holes requires repeating the entire process twice. Also, all the structural elements of the C4s are the same (e.g., spacer and conductive core), so using a single set of processing steps to make all C4s would be straightforward, i.e., simply defining the location of the holes in, for example, masks and performing the same processing steps. Again, it would make little sense to unnecessarily repeat these processing steps.

114. Forming both at the same time would have been routine and highly predictable. First, as the above figure illustrates, Nakajima's process is already able to etch the C4 holes in different regions of the memory device, e.g., in the array region with a full stack, in the staircase region in which a portion of the stack exists,

and in the peripheral where there is no memory stack. I also note that Nakajima discloses etching contact CC partially through the stack (a staircase contact) and C3 (which do not travel through the stack) at the same time. Ex. 1005, 17:33-45. Such etches, e.g., RIE, were well known to achieve these results, and were commonplace. *E.g.*, Ex. 1023 (Tessariol), [0037] (“dummy-structure openings 56 and via openings 54 are formed at the same time (i.e., simultaneously)”), Fig. 9 (extending through different number of stack layers).

115. Mushiga demonstrates forming through-array contacts (588), including the cavities, insulating spacers, and conductive cores, at the same time in various portions of the memory device was routine and well understood:



Ex. 1010 (Mushiga), Fig. 5, 10:31-58.

4. Claim 4:

[4] The method of claim 3, wherein forming the TAC comprises depositing the conductor layer in the first opening to form the TAC and in the second opening to form a peripheral contact.”

116. Nakajima discloses this limitation.

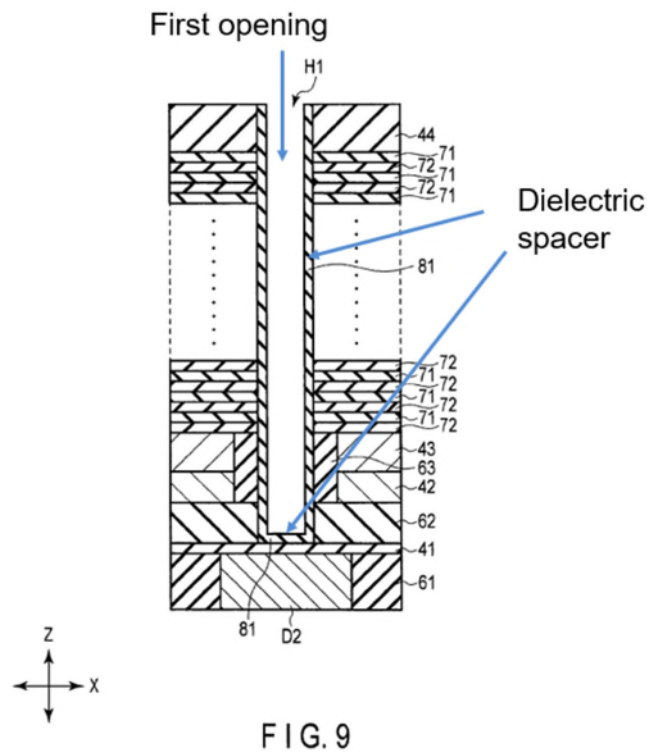
117. As I describe in my claim [3] analysis, Nakajima discloses a C4 outside the memory stack, i.e., a peripheral contact. The '254 Patent likewise refers to a contact outside of the array, i.e., on the peripheral of the array, as a peripheral contact. Ex. 1001, 10:2 (peripheral contact 148), Fig. 1. The claim [1.E] analysis demonstrates that Nakajima discloses depositing a conductor layer in these openings, i.e., to form a TAC (for the C4 in the stack) and a peripheral contact (for the C4 outside the stack). By definition, a contact has a conductive layer.

5. Claim 5:

“[5.PRE] The method of claim 1, wherein forming the spacer on the sidewall of the first opening comprises:

[5.A] depositing a dielectric layer on the sidewall and a bottom surface of the first opening; and”

118. Nakajima discloses these limitations: “silicon oxide layer 81 is conformally formed along the bottom and the side surface of the hole H1.” Ex. 1005, 7:44-49. A natural result of forming a conformal silicon oxide layer in the hole, like shown below, is the formation of the silicon oxide on the bottom as well, due to the deposition that flows from the void at the top of the hole.



Id., Fig. 9.

[5.B] “removing part of the dielectric layer that is deposited on the bottom surface of the first opening.”

119. Nakajima discloses this limitation: “Next, as shown in FIG. 10, a portion of the silicon oxide layer 81 that is located at the bottom of the hole H1 is removed by, for example, RIE using a mask layer not shown in the drawing, so that the silicon nitride layer 41 is exposed.” Ex. 1005, 7:50-53. Again, because the natural result of the deposition to form the spacer is the silicon oxide at the bottom of the hole, it was necessary to remove this portion, because the contact must ultimately contact another conductive element. The Nakajima contacts ultimately couple devices above and below the stack.

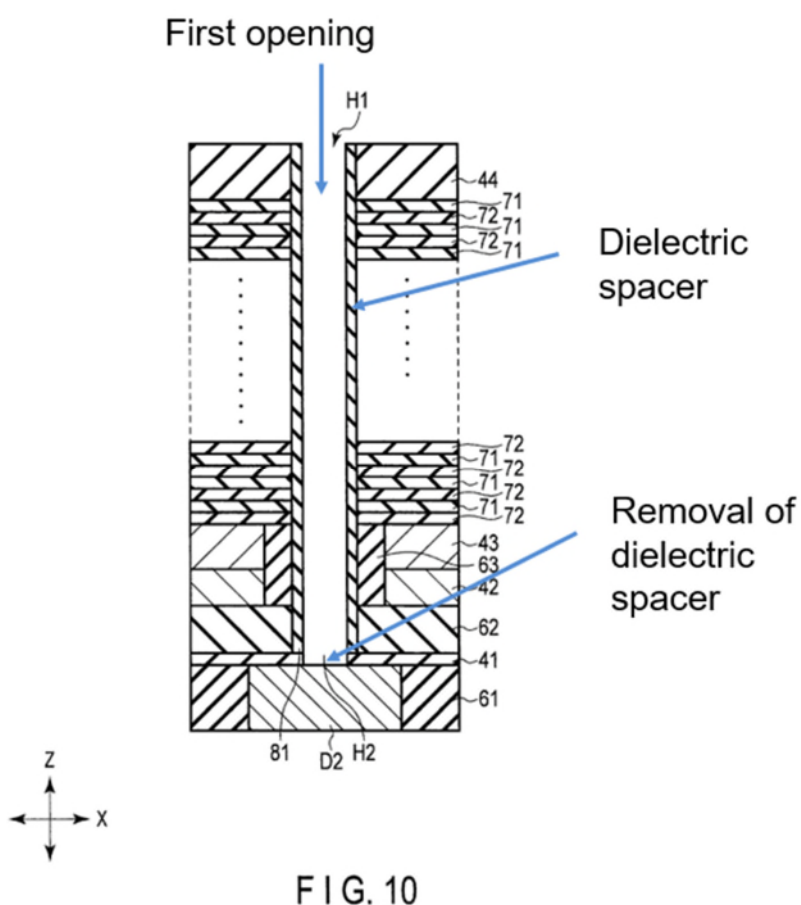


FIG. 10

Ex. 1005, Fig. 10.

6. Claim 6:

[6] “The method of claim 5, wherein the deposition of the dielectric layer comprises atomic layer deposition (ALD), and the removal of the part of the dielectric layer comprises anisotropic etching on the bottom surface of the first opening.”

120. Nakajima renders this limitation obvious in view of the knowledge of a POSITA. I address both atomic layer deposition (ALD) and anisotropic etching separately below.

ALD

121. Nakajima discloses depositing the oxide liner (“silicon oxide layer 81”) “conformally” (see my analysis under claim [1.D]). ALD was very well known for decades. In the last few decades before the filing of the ’254 Patent, in particular, it became important for thin layers of high-K layers (including in the memory industry). For the specific application of spacers, e.g., a silicon oxide spacer, it was well known. Ex. 1009 (Toyama), [0226] (backside trench 79), [0313] (moat trenches 579); Ex. 1024 (U.S. Pat. 9,620,514), 35:51-61 (forming “dielectric spacer” by first forming “silicon oxide layer” via “ALD”); Ex. 1023 (Tessariol), [0063] (ALD), [0038] (conductive vias 58).

122. A POSITA would have been motivated to employ ALD with a high expectation of success for several reasons. First, given that Nakajima expressly requires a conformal deposition, a POSITA would have immediately understood ALD as an ideal deposition technique. Conformal deposition has always been a key benefit of ALD. Ex. 1025 (Hwang), 12 (“better conformality over three-dimensional (3D) structures”) 13 (“unprecedented conformality over the 3D structures”). Second, ALD was well understood for this specific application, as I describe above. Thus, specific process steps for such spacers were known and readily available. Third, ALD was highly predictable. Again, ALD was textbook material. *Id.*; Ex.

1009 (Toyama), [0226], [0313]; Ex. 1023 (Tessariol), [0063], [0038]. Known ALD deposition steps were readily available for this application.

Anisotropic Etching

123. Nakajima's RIE etch that removes the bottom portion of the dielectric (see [5.B]) is anisotropic etching, because it is directional: "Next, as shown in FIG. 10, a portion of the silicon oxide layer 81 that is located at the bottom of the hole H1 is removed by, for example, RIE using a mask layer not shown in the drawing, so that the silicon nitride layer 41 is exposed." Ex. 1005, 7:50-53. The resulting sidewalls are vertical. Such RIE etches that are anisotropic were well known. Ex. 1026 (U.S. Pat. 10,515,799), 6:63-65 ("For example, channel hole 120 can be formed by anisotropic reactive ion etching (RIE)."); Ex. 1027 (U.S. Pat. 9,570,460), 11:55-58 ("The at least one memory film 7, 9, 11 and cover layer 410 may be etched using RIE or another suitable anisotropic wet or dry etching method to form the opening 417."). Anisotropic etching aims to remove material in a specific direction and that is precisely what Nakajima's RIE etch does.

124. I also note that it was well known that to form a material, including a dielectric liner, on only the sidewall of a hole, the typical approach involves a deposition and then an etch—such as an anisotropic etch—to remove the deposition on the bottom portion. Ex. 1028 (U.S. Pat. 9,728,546), 34:62-35:3 ("The dielectric liners 141 can be formed, for example, by formation of a dielectric material layer

including a first dielectric material, and by a subsequent anisotropic etch (such as a reactive ion etch) that removes horizontal portions of the dielectric material layer to form dielectric spacers 141”), 17:41-46 (“Each first semiconductor channel portion 601 can be formed on inner sidewalls of each memory film 50 by deposition of a semiconductor material layer and a subsequent anisotropic etch of the semiconductor material layer.”). It goes without saying that removing the bottom portion is necessary for the Nakajima C4 contacts, because a subsequent conductive core must connect to an underlying element, thereby providing an electrical coupling of a device above the array and a device below the array.

7. Claim 7:

[7.PRE] “The method of claim 1, wherein forming the spacer on the sidewall of the first opening comprises: [7.A] “forming a plurality of shallow recesses by removing parts of the sacrificial layers abutting the sidewall of the first opening;”

125. I address this limitation under what appears to be PO’s incorrect interpretation of the limitation and the correct interpretation.

126. The ’254 Patent discloses an etch that intentionally forms recesses in the sacrificial layers. Ex. 1001, 13:47-61, Fig. 3D. It appears in alleging infringement in the district court case, however, PO interprets this claim to include largely undetectable and unintentional alleged recesses. Ex. 1029 (Ex. A-2, YMTC’s Contentions), 30. In typical etches through a stack with silicon oxide layers and silicon nitride layers (usually the composition of the sacrificial gates), the

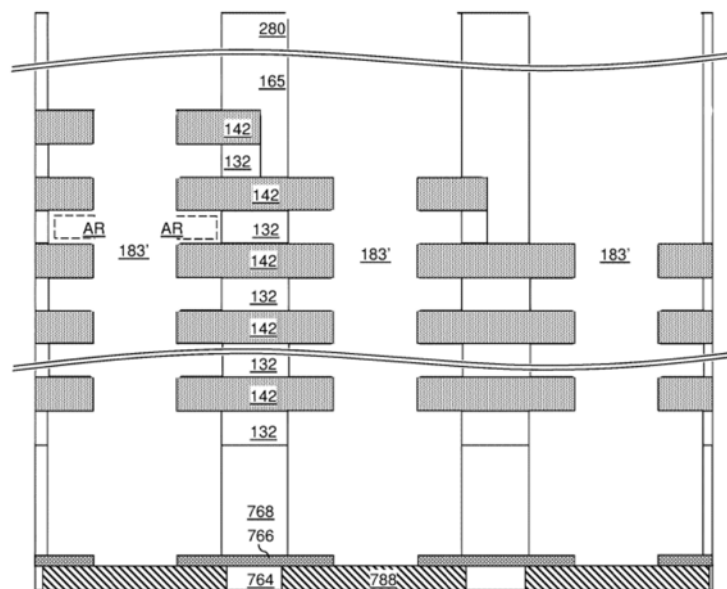
result will be recesses in either the silicon oxide or silicon nitride layers due to what is known as etch selectivity. In simple terms, an etch involves using a chemical, which may in a wet or dry form, to remove material. That chemical, however, can favor a particular type of material, and more aggressively remove that material. For a stack of silicon oxide and silicon nitride layers, prior art etches would typically favor one of these material types. Ex. 1030 (U.S. Pat. 11,075,084), 2:59-67 (In “3D NAND memory, it is important to have an etching gas which can etch both SiO₂ and SiN layers (or both SiO₂ and p-Si layers) without selectivity. In another words, ***it is a challenge to find an etch gas that has similar high etch rates of SiO₂ and SiN in terms of getting a smooth sidewall*** of high aspect ratio holes in 3D NAND memory.”). Thus, prior art etches would naturally create very small lateral recesses, which may be in the silicon nitride sacrificial layers depending on the etch type. *Id.*, 2:59-67.

PO’s Incorrect Claim Interpretation

127. Recall that Nakajima discloses etching through a silicon nitride and silicon oxide stack (see claim [1.A], [1.C]). And recall that typical prior art etches that effectively create a hole through that stack result in very small lateral recesses in either the dielectric spacers or sacrificial layers. Ex. 1030 (U.S. Pat. 11,075,084), 2:59-67. Thus, it would have been obvious that small unintentional recesses would naturally result, because this was known as a natural result of these prior art etches.

The Correct Claim Interpretation

128. Creating intentional lateral recesses in a hole for a contact, however, was also known. For example, Cui (U.S. Pat. 10,304,852, Ex. 1031) discloses contacts 183 that travel through the staircase and through the entire array. Ex. 1031 (Cui), Fig. 14A, 25:51-53 (e.g., 183 contact on right of region 200); *see also* Ex. 1015 (Kai), 11:9-34 (“laterally recessed”). Cui discloses two types of these holes. First, Cui depicts an embodiment in which the sidewalls of this contact are straight (“cylindrical via cavity”). Ex. 1031 (Cui), Fig. 15A, 25:63-26:22. Second, Cui depicts an alternative embodiment with large recesses in the conductor layers (“ribbed via cavity”). *Id.*, Fig. 16A, 26:23-33. In other words, both alternative options were known.



Id., Fig. 16A.

129. The ribbed via cavity in Cui creates additional space. In effect, the spacer, or liner, is longer now, because it travels into and out of the lateral recesses. The '254 Patent describes this same purpose of the lateral recesses. Ex. 1001, 13:48-61. Cui refers to these additional regions as “rib regions.” Ex. 1031 (Cui), 26:23-34. The dielectric material, i.e., the spacer, will additionally fill these rib regions.

130. Implementing the rib regions provide two fundamental options. First, the rib regions can be made in the sacrificial gates. Second, the rib regions can be made in the conductive layers. Both result in the same additional space. It is only a matter of selecting one of two options. Etching these regions in each layer type was known. Ex. 1031 (Cui), Fig. 16A, 26:23-33 (recesses in conductive layers); Ex. 1015 (Kai), 11:9-34 (recesses in sacrificial gates).

131. A POSITA would have had a high expectation of success in forming the rib regions. Again, etch chemistries that naturally create small lateral recesses were known. Further, isotropic and selective etches were well known, and selecting an etch chemistry to a certain selectivity was well known. *E.g.*, Ex. 1031 (Cui), 26:33-45; Ex. 1015 (Kai), 11:9-34 (recesses in sacrificial gates).

[7.B] “depositing a dielectric layer filling in the shallow recesses and on the sidewall and a bottom surface of the first opening; and”

132. Nakajima renders this limitation obvious. Nakajima discloses forming conformal dielectric spacer in the hole, and the conformal spacer will fill the shallow recesses because it is conformal. See Claim [5.PRE-5.B].

[7.C] “removing part of the dielectric layer that is deposited on the bottom surface of the first opening.”

133. Nakajima renders this limitation obvious in view of the knowledge of a POSITA. As I explain in my [7.PRE-B] analysis, it would have been obvious to form a conformal liner in the hole with shallow recesses. Again, such a conformal process, like Nakajima’s, typically results in the silicon oxide at the bottom of the hole. Thus, Nakajima discloses removing the bottom portion of the spacer, ultimately enabling a connection to an underlying device (or interconnects to that device). See Claim [5.C].

8. Claim 8:

[8] “The method of claim 7, wherein the removal of the part of the dielectric layer comprises isotropic etching on the sidewall and the bottom surface of the first opening.”

134. Nakajima renders this limitation obvious in view of the knowledge of a POSITA.

135. I first note that the ’254 Patent describes using an isotropic etch because the dielectric material on the bottom will be thicker than on the sidewalls. This allows for an isotropic etch. An isotropic etch is a non-directional etch. Ex. 1001,

14:1-19. This was well known. For example, Mushiga (U.S. Pat. No. 10,354,980, Ex. 1010) describes depositing a liner (586) such that the liner is thicker at the bottom (at the interface of the substrate) and then performing an isotropic etch because of this fact to remove the bottom dielectric. Ex. 1010 (Mushiga), 10:38-42, 12:30-53. That the bottom liner is thicker is what allows for the isotropic etch. This is advantageous because directional etching is not necessary given the thicker bottom oxide. Anisotropic etch relies on physical bombardment of ions accelerated by electric field. As such, it can cause damage, and it roughens the surface. Isotropic etch does not have such issues. A POSITA would have had a high expectation of success, because isotropic etches were textbook materials. As I describe above, such etches were well known for this exact application.

9. Claim 9:

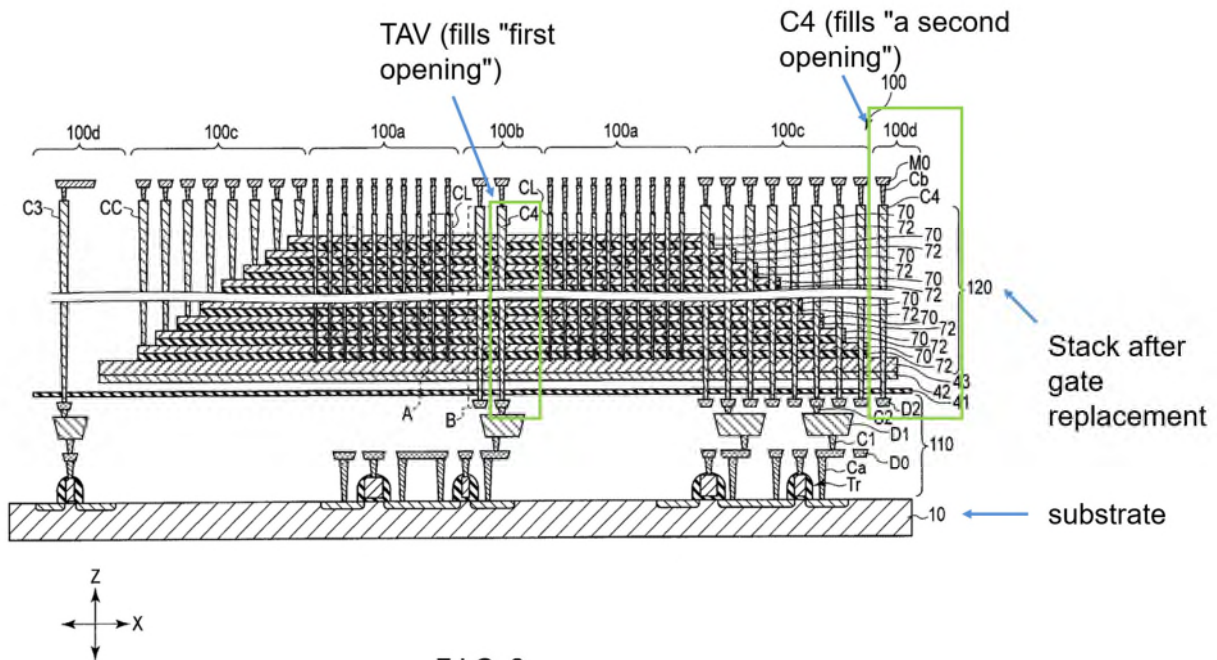
[9.PRE] “The method of claim 1, wherein forming the first opening comprises:

[9.A] “simultaneously etching the first opening through the stack, a second opening outside of the stack, and a third opening through the stack,”

136. Nakajima renders obvious these limitations in view of the knowledge of a POSITA.

137. First, as I explain above with respect to claim [3], Nakajima would have been understood to disclose etching the holes for the C4s at the same time, including the first hole all the way through the stack and another hole outside the stack, for the

peripheral contact, which maps here to “a second opening.” These two holes are shown below:



Ex. 1005, Fig. 2.

138. Second, the claim [2] analysis demonstrates that it would have been obvious to further etch dummy holes. A dummy hole corresponds to a “third hole.” As I describe with respect to claim [3], these dummy structures may be in the array, the edge of the array, etc., and thus through the stack.

139. For the same reasons that I explain in claim [3], it would have been obvious to etch all these holes at the same time. Again, etching a hole is not one step, e.g., one first creates the masking layers. Thus, unnecessary repeating that process unnecessarily increases the fabrication time. Fabrication time is an

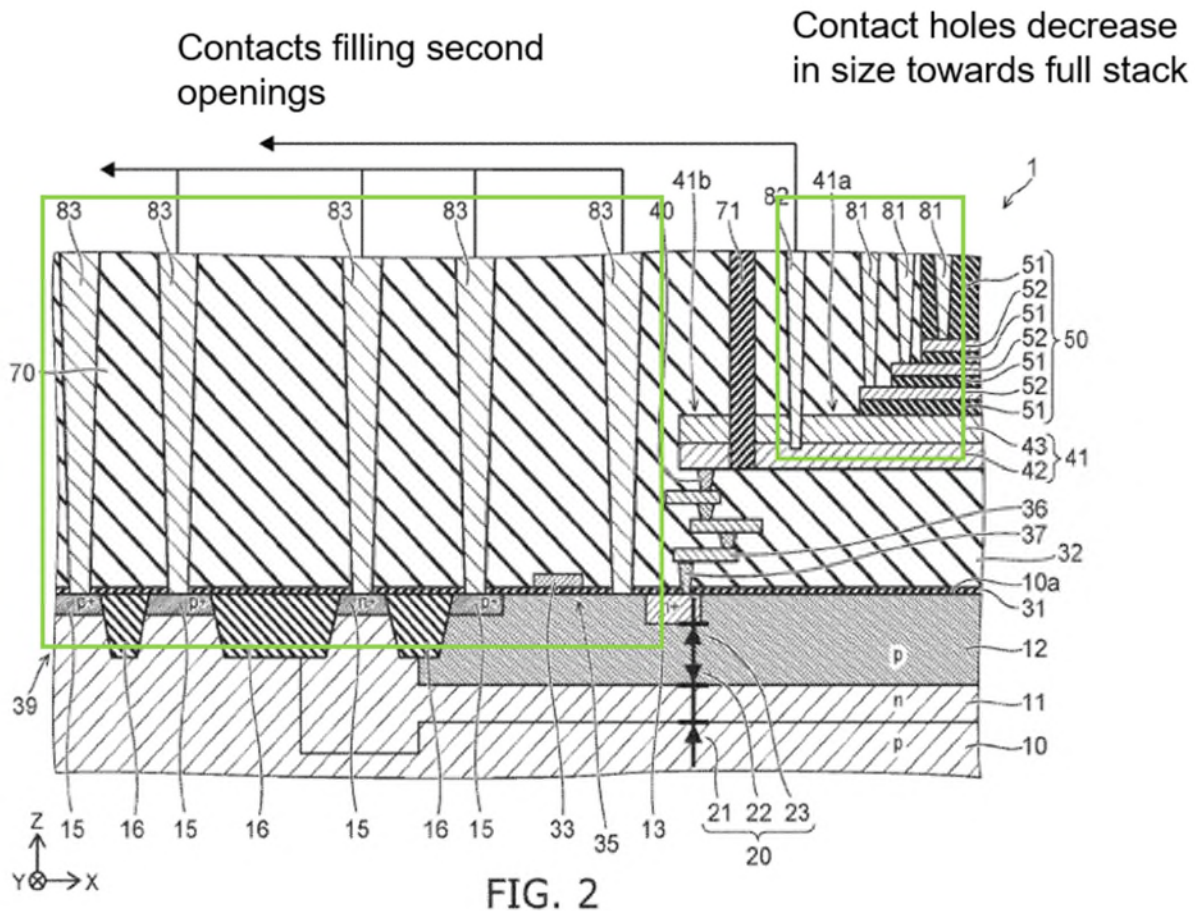
important factor in the cost of fabricating chips, and semiconductor manufacturers aim to reduce that time. A POSITA would have immediately thought to form different holes for contacts at the same time in view of these considerations. I also demonstrate in that analysis that the ability to create holes at the same time, even if through different portions of the stack (or not the stack at all) was well known.

[9.B] “wherein a lateral dimension of the third opening is smaller than lateral dimensions of the first and second openings.”

140. Nakajima renders this limitation obvious in view of the knowledge of a POSITA.

141. This limitation relates to the relative lateral dimensions, e.g., diameter, of the holes. As I will explain, this limitation is obvious, because the third openings are for dummy structures (and support structures with very small diameters were commonplace and function effectively as support members), the second openings are in the peripheral (which allow for large contacts), and the first openings are in the array (and the contacts are larger than the dummy structures, but smaller than the array contacts).

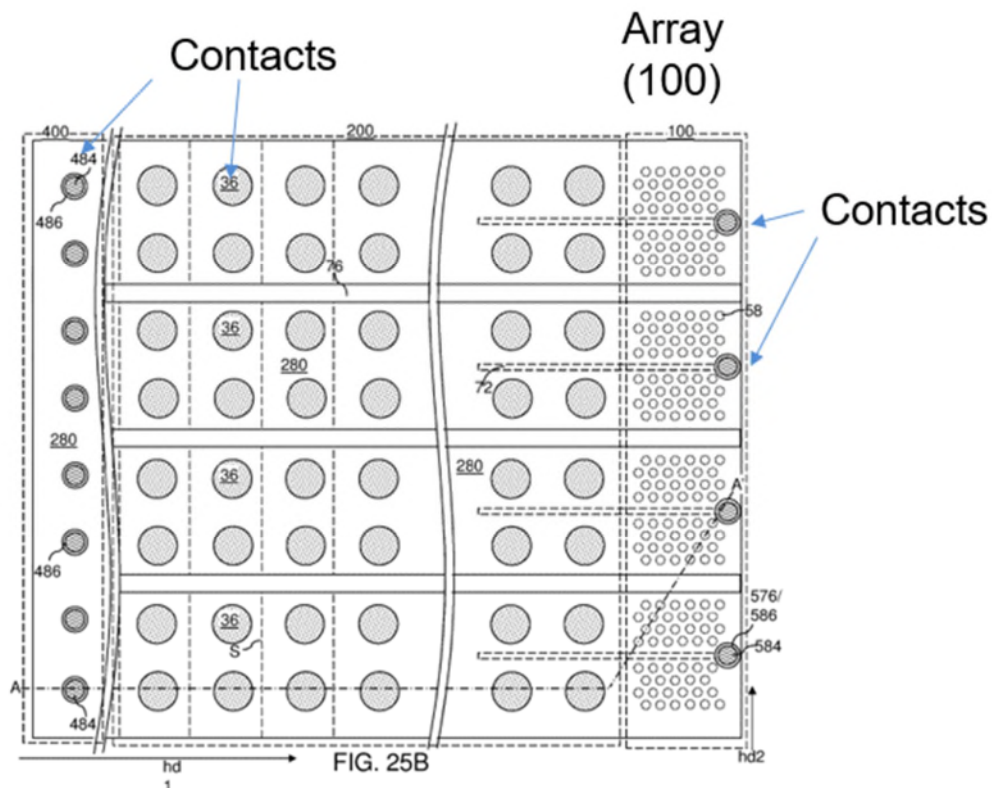
142. The lateral dimensions of via structures typically get smaller towards the array, because the array is the densest portion of the memory. The array region, for example, contains millions or billions of channel structures. A representative view of this is shown below:



Ex. 1006 (Fujiki), Fig. 2. Thus, it would have been obvious that the second hole, which is outside of the array in the peripheral, may have the largest lateral dimension, consistent with Fujiki's Figure 2. Again, the peripheral is less dense, and the processing does not have to be as precise. In the array portion, given the density, more issues persist, such as creating inadvertent short circuits, support issues, etc. I will note that Figure 1 of Nakajima depicts C4s with a represent box that with the boxes have the same size. But this is clearly not drawn to scale, as there are many millions or billions of channel structures (CL) in the array region. And in any event,

it was well known that larger contacts may exist in the peripheral, providing for example, a lower resistance.

143. As to the third hole, it would have been obvious that the third hole will have the smallest lateral dimensions. As I explain in the claim [9.A] analysis, the third hole is a dummy hole, e.g., a dummy channel hole. As I describe in my claim [2] analysis, such structures provide a support function. Channel holes are miniscule in size relative to contacts. For example, below is a top-down view showing channel structures in region 100 versus various contacts:



Ex. 1031, (Cui), Fig. 25B. Also note the height difference in Figure 2 above. The contacts 83 are longer, and as a natural result of etches that taper (as shown in Figure

2), the lateral width of the top is naturally wider. Note while obviously not to scale, the difference in size of these elements, namely, the channel holes (and channels) and various contact would have been understood to represent the well-known difference in relative size of the many small channels versus the fewer and larger contacts.

10. Claim 10:

[10.PRE] “The method of claim 9, wherein forming the spacer on the sidewall of the first opening comprises: [10.A] “depositing a dielectric layer (i) fully filling in the third opening to form a dummy channel structure and (ii) partially filling in the first opening and the second opening; and”

144. Nakajima in view of the knowledge of a POSITA renders this limitation obvious.

145. First, my analysis of claim [1.D] demonstrates that Nakajima discloses depositing a dielectric liner on the first opening and second opening (C4s), i.e., partially filling those holes. This is to form the spacer, which is necessary to isolate those contacts. Note that the C4 that goes though the edge travels through certain layers, e.g., layer 43, and the spacer isolates that contact from those layers.

146. Second, one way to form a support pillar from a dummy hole was to completely fill it with an oxide, here the insulating liner. This creates a support pillar. A common support pillar was a solid dielectric, e.g., oxide, pillar. Ex. 1032 (U.S. Pat. 9,793,139), 15:21-36 (“dielectric support pillar 7P”). The oxide fill results in a solid oxide pillar that supports the memory stack.

[10.B] “removing parts of the dielectric layer that are deposited on a bottom surface of the first opening and on a bottom surface of the second opening.”

147. Nakajima renders this limitation obvious in view of the knowledge of a POSITA.

148. As I explain my analysis for claim [5.B], Nakajima discloses removing the bottom portion, because this enables the electrical coupling between devices above and below the stack. Again, this was necessary to do for all contacts, because Nakajima’s deposition of the liner creates oxide on the bottom.

11. Claim 11:

[11.PRE] “A method for forming a three-dimensional (3D) memory device, comprising:”

149. This limitation is identical to [1.PRE] and Nakajima discloses it for the same reasons.

[11.A] “forming a stack comprising a plurality of dielectric/sacrificial layer pairs on a substrate;”

150. This limitation is identical to [1.A] and Nakajima discloses it for the same reasons.

[11.B] “forming a channel structure extending vertically through the stack;”

151. This limitation is identical to [1.B] and Nakajima discloses it, or renders it obvious, for the same reasons.

[11.C] “forming a dummy channel structure extending vertically through the stack;”

152. Nakajima renders obvious forming a dummy channel structure that extends vertically through the stack for the reasons set forth in [2].

[11.D] “simultaneously etching a first opening through the stack and a second opening outside of the stack;”

153. This limitation is present in [3], and Nakajima discloses it, or renders it obvious, for the same reasons.

[11.E] “simultaneously forming a first spacer on a sidewall of the first opening and a second spacer on a sidewall of the second opening;”

154. The claims [3]-[4] analysis demonstrates that Nakajima discloses, or renders obvious, forming the C4s at the same time, and thus forming the spacers in the first and second holes at the same time.

[11.F] “depositing a conductor layer (i) filling in the first opening to form a through array contact (TAC) and (ii) filling in the second opening to form a peripheral contact; and”

155. This limitation is substantively the same as claim [4] (but recites “depositing” instead of “filling”), and Nakajima discloses it, or renders it obvious, for the same reasons.

[11.G] “after forming the TAC and peripheral contact, forming a slit extending vertically through the stack.”

156. This limitation is substantively the same as [1.F] in view of forming the TAC and peripheral contact at the same time, and Nakajima discloses it for the same reasons.

12. Claim 12:

[12.PRE] “The method of claim 11, wherein forming the first spacer on the sidewall of the first opening comprises:

[12.A] “depositing a dielectric layer on the sidewall and a bottom surface of the first opening; and”

[12.B] “removing part of the dielectric layer that is deposited on the bottom surface of the first opening.”

157. These limitations are substantially the same as [5.PRE-B], and Nakajima discloses them for the same reasons.

13. Claim 13:

[13] “The method of claim 12, wherein the deposition of the dielectric layer comprises atomic layer deposition (ALD), and the removal of the part of the dielectric layer comprises anisotropic etching on the bottom surface of the first opening.”

158. This limitation is identical to [6], and Nakajima renders it obvious for the same reasons.

14. Claim 14:

[14.PRE]-[14.C]

159. These limitations are substantively the same as claim [7.PRE-7C], and Nakajima renders them obvious for the same reasons.

15. Claim 15:

[15] “The method of claim 14, wherein the removal of the part of the dielectric layer comprises isotropic etching on the sidewall and the bottom surface of the first opening.”

160. This limitation is identical to claim [8], and Nakajima renders it obvious for the same reasons.

16. Claim 17:

[17] “The method of claim 11, wherein the dielectric layers in the dielectric/sacrificial layer pairs comprise silicon oxide, the sacrificial layers in the dielectric/sacrificial layer pairs comprise silicon nitride, and the first and second spacers comprise silicon oxide.”

161. Nakajima discloses this limitation. Ex. 1005, 7:26-36 (“sacrifice layers 71 are silicon nitride layers, and the insulation layers 44, 62, 63, and 72 are silicon oxide layers”), 7:44-49 (“silicon oxide layer 81 is conformally formed along the bottom and the side surface of the hole H1”).

17. Claim 18:

[18.PRE] “A method for forming a three-dimensional (3D) memory device, comprising:”

162. This limitation is identical to claim [1.PRE], and Nakajima discloses it for the same reasons.

[18.A] “forming a stack comprising a plurality of dielectric/sacrificial layer pairs on a substrate;”

163. This limitation is identical to claim [1.A], and Nakajima renders it obvious for the same reasons.

[18.B] “forming a channel structure extending vertically through the stack;”

164. This limitation is identical to claim [1.B], and Nakajima renders it obvious for the same reasons.

[18.C] “simultaneously etching a first opening through the stack, a second opening outside of the stack, and a third opening through the stack, wherein a lateral dimension of the third opening is smaller than lateral dimensions of the first and second openings;”

165. This limitation is identical to claim [9.A-B], and Nakajima renders it obvious for the same reasons.

[18.D] “depositing a dielectric layer (i) fully filling in the third opening to form a dummy channel structure and (ii) partially filling in the first opening and the second opening;”

166. This limitation is identical to claim [10.A], and Nakajima renders it obvious for the same reasons.

[18.E] “removing parts of the dielectric layer that are deposited on a bottom surface of the first opening and on a bottom surface of the second opening;”

167. This limitation is identical to claim [10.B], and Nakajima renders it obvious for the same reasons.

[18.F] “depositing a conductor layer (i) filling in the first opening to form a through array contact (TAC) and (ii) filling in the second opening to form a peripheral contact; and”

168. This limitation is substantively the same as claim [4], and Nakajima discloses it obvious for the same reasons.

[18.G] “after forming the TAC and peripheral contact, forming a slit extending vertically through the stack.”

169. This limitation is substantively the same as claim [1.F], and Nakajima discloses it obvious for the same reasons. This claim also refers to forming the slit after the peripheral contact, but as shown above, it would have been obvious to form both contacts at the same time, so my analysis in claim [1.F] equally applies.

18. Claim 20:

[20] “The method of claim 18, further comprising prior to etching the first, second, and third openings, forming a staircase structure at one side of the stack.”

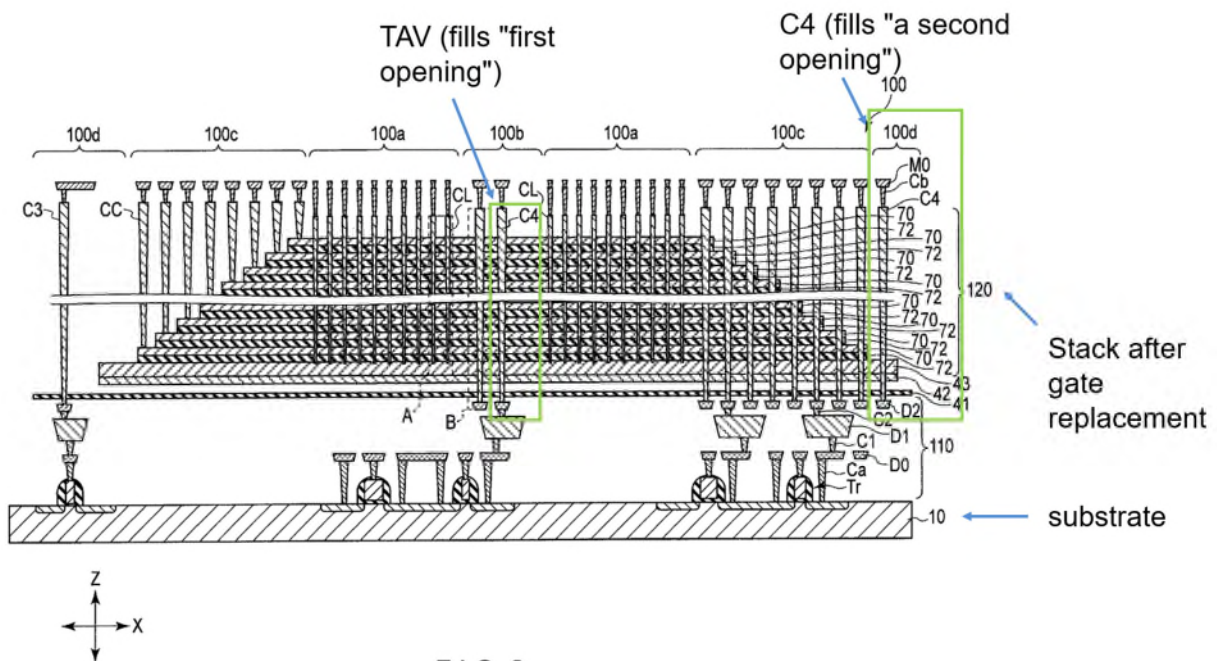
170. Nakajima would have been understood to disclose, and alternatively render obvious, this limitation.

171. A POSITA reading Nakajima’s fabrication of the C4 structure would have understood Nakajima to disclose this limitation. There, after forming the C4 structures, Nakajima describes performing the gate line replacement process. This involves replacing the sacrificial gates with conductive gates, e.g., with tungsten gates. Ex. 1005, 7:5-8:34. A POSITA would have immediately understood the staircase already exists. Consistent with how staircases are made, Nakajima describes forming a staircase that etches the sacrificial gates and oxide layers. *Id.*, 16:49-55. This is a repeating process that basically trims that portion of the stack into the staircase. Thus, when the staircase is made, it is before the C4 manufacturing steps begin (because those steps flow immediately into the gate replacement process).

172. In addition, attempting to form the staircase region after gate replacement would be problematic. This would require etching large amounts of, for example, tungsten (the typical conductive gates after gate replacement) from the stack. Etching the stack of oxide and silicon nitride layers, in comparison, is much simpler. Indeed, the sacrificial material is selectable, and considerations such as

forming the staircase and etching out the sacrificial material are made when selecting that material.

173. I also note that the peripheral contact extends through a conductive layer that is on the staircase structure:



Ex. 1005, Fig. 2. The “second opening” is through an insulator structure that is deposited over the staircase after the staircase is made. Finally, I note that the standard construction process is building the stack, the staircase, and then the other elements of the memory device. Ex. 1015 (Kai), Figs. 1-6.

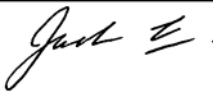
C. Secondary Considerations of Non-Obviousness

174. Based on my review of the '254 Patent's file history, I note that no secondary considerations of non-obviousness were identified in connection with the

Petition for *Inter Partes* Review of U.S. Patent No. 10,879,254
Declaration of Dr. Jack C. Lee

patent's claims. Nor am I otherwise aware of any evidence of commercial success, skepticism, failure of others, industry praise, unexpected results, or the like relating to the '254 Patent. Instead, as discussed above, it is my opinion that the subject matter embraced by the challenged claims was known in and obvious over the prior art.

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willfully false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1101 of Title 18 of the United States Code.

Date:	<u>October 11, 2024</u>
Location:	<u>Shanghai, China</u>
Signature:	<u></u>
	DR. JACK C. LEE