Filed on behalf of: Yangtze Memory Technologies Company, Ltd.

Entered: February 21, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

Case IPR2025-00034
Patent 10,879,254

DECLARATION OF STEPHEN CAMPBELL
IN SUPPORT OF
PATENT OWNER'S PRELIMINARY RESPONSE

YMTC
Exhibit 2007
Micron v. YMTC
IPR2025-00034
Ex. 2007

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I. Introduction and Qualifications

1. I have been retained by Yangtze Memory Technologies Company, Ltd. ("YMTC" or "Petitioner") to provide my opinion concerning the validity of U.S. Patent No. 10,879,254 (Ex. 1001).

2. I received my Bachelor's degree in Physics from the University of St. Thomas (St. Paul, Minnesota) in 1975, and my M.S. and Ph.D. in Physics from Northwestern University (Evanston, Illinois) in 1978 and 1981, respectively. I then joined Sperry, now called Unisys, in 1981 as a CMOS process development engineer. In 1982, I was assigned the lead engineer for the 1.2 μm technology process development effort. In 1984 I was promoted to head of silicon research for the company. This involved a wide variety of process technologies for submicron CMOS.

3. In 1986, I joined the University of Minnesota as an Assistant Professor in the Electrical Engineering Department. My research at the University involved semiconductor processing, materials, and device structures. I raised more than $100M in various grants and successful submissions to companies and industry consortiums such as the Semiconductor Research Association, as well as State and US government agencies including DARPA and the National Science Foundation. The first ten years of my career at the University concentrated on the development of rapid thermal annealing for 200

mm wafers, particle control in CVD systems, and the development of high uniformity rapid wafer annealing systems. The next ten years were dedicated to the invention and development of high permittivity (aka high-k) films for use as gate insulators. This is necessary to allow the development of deeply scaled CMOS devices. This technology has been widely adopted for nanoscale CMOS devices. In the last fifteen years at the University, my work involved the development of low-cost tandem photovoltaics and micro electromechanical systems (MEMS). The latter included a chronic deep brain sense/stimulation system and very high-speed mechanical switches. Finally, I developed processes for the fabrication of novel 2D materials such as black arsenic, and fabricated transistors using these materials. I retired from the University in 2021.

4. A brief summary of my work at the University would include:

- Approximately 200 publications
- The leading textbook on semiconductor technology. Currently in its fourth edition, Fabrication Engineering at the Micro and Nanoscale (Oxford 1996, 2000, 2008, 2013) is the dominant text on the topic.
- Honors from outside the University such as being named a Presidential Young Investigator by the National Science

Foundation and a Life Fellow by the Institute of Electrical and Electronic Engineers (IEEE).

- Honors within the University including outstanding service and outstanding teaching.
- As the Director of the University's Nanofabrication Center, I increased lab usage from 30 to more than 300 users, enabling millions of dollars research awards annually by Minnesota faculty, and leading to the construction of a new $80M building with an expansive cleanroom facility.

5. Since retiring from the University, I have consulted with semiconductor companies including patent litigation.

6. Additional information regarding my education, technical experience and publications, including a list of the U.S. patents of which I am an inventor/coinventor, is included in my *Curriculum Vitae*, which I understand is attached at Exhibit 2006.

II. Summary Of Materials Reviewed And Considered

7. All of the opinions contained in this Declaration are based on the documents I reviewed and my knowledge and professional judgment. In forming the opinions expressed in this Declaration, while drawing on my experience in the field of semiconductor fabrication, I reviewed the following documents:

Ex.	Description
1001	United States Patent No. 10,879,256 ("the '254 patent")
1002	File History for the '254 patent ("'254 FH")
1003	Declaration of Jack C. Lee
1004	Curriculum Vitae of Jack C. Lee
1005	U.S. Patent 10,777,501 to Nakajima et al. ("Nakajima")
1010	U.S. Patent 10,354,980 to Mushiga et al. ("Mushiga")
1015	U.S. Patent 10,290,643 to Kai et al. ("Kai")
1016	U.S. Patent 9,859,297 to Park et al. ("Park")
1017	U.S. Patent Appl. Publ. 2018/0308559 to Kim et al. ("Kim")
1023	U.S. Patent Appl. Publ. 2019/0081061 to Tessariol et al. ("Tessariol")
1031	U.S. Patent 10,304,852 to Cui et al. ("Cui")

8. My opinions are additionally guided by my appreciation of how a person of ordinary skill in the art would have understood the claims of the '254 patent at the time of the invention, which I have been asked to assume is August 21, 2018.

III. Understanding of Legal Standards

9. I am not an attorney, and in this Declaration, I do not opine on matters of law. For the purposes of this Declaration, I have been informed about certain aspects of the law that are relevant to my analysis and opinions. My understanding of these principles is set forth below.

10. I have been informed by Counsel that the validity analysis is a two-step process. First, the patent claims are construed to ascertain their proper scope. Second, the construed claims are compared to the identified prior art to determine if the claims are valid over the prior art.

A. Claim construction

11. I have been informed by Counsel that the claims of a patent define the limits of the patentee's exclusive rights. I have been informed by Counsel that to determine the scope of the claimed invention, courts typically construe claim terms, the meaning of which the parties may dispute. I have been informed by Counsel that claim terms should generally be given their ordinary and customary meaning as understood by one of ordinary skill in the art at the time of filing of the patent application, after reading the patent and its prosecution history. I also have been informed by Counsel that a basic tenet of claim construction presumes that different words in a claim have different meanings, unless there is evidence to the contrary.

12. I have been informed by Counsel that claims must be construed in light of, and consistent with, the intrinsic evidence. In this context, I have been informed by Counsel that intrinsic evidence includes the claims themselves, the written disclosure in the specification, and the patent's prosecution history, including prior art that was considered by the United States Patent and

Trademark Office ("USPTO"). I have been informed by Counsel that the specification is always highly relevant to the claim construction analysis and often is the single best guide to the meaning of a disputed term. I have been informed by Counsel that extrinsic evidence may also be considered when construing claims and may include, for example, technical dictionaries, technical publications and books, treatises, and expert testimony.

B. Obviousness

13. I have been informed by Counsel that patent claims can be deemed invalid if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the pertinent art. While such conclusions are often based on more than one piece of prior art, only one is required. It is not sufficient that a collection of prior art references merely recites the various elements of a challenged patent claim. Rather, as I have been informed by Counsel, the prior art must present the elements in a manner that is consistent with their arrangement or use in the challenged claims. I have been informed by Counsel that obviousness cannot be based on the hindsight combination of components selectively culled from the prior art.

14. I have been informed by Counsel that a person having ordinary skill in the art (i.e., a POSITA) is a hypothetical person who is presumed to have

known the relevant art at the time the invention was made. I have been informed by Counsel that the condition "at the time the invention was made" is imposed to rule out impermissible hindsight. I also have been informed by Counsel that an expert is to analyze the prior art from the perspective of a person of ordinary skill in the art at the time the invention was made, and not simply to provide his/her own personal conclusions.

15. I also have been informed by Counsel that an obviousness determination includes several factual inquiries, including (1) determining the scope and content of the prior art; (2) ascertaining the differences between the claimed invention and the prior art; (3) resolving the level of ordinary skill in the pertinent art; and (4) taking into consideration any objective indicia of nonobviousness.

16. I have been informed by Counsel that obviousness must be determined as of the date of the invention (i.e., the effective filing date or priority date of the patent). Thus, in considering the reason or motivation to combine references, it is essential to avoid using hindsight. For example, the problem examined when considering obviousness is the general problem that confronted the inventor before the invention was made, not the specific problem solved by the invention. Defining the problem in terms of its solution reveals improper hindsight in the selection of the prior art relevant to obviousness. Further, an

overly narrow statement of the problem can represent a form of hindsight, because often the inventive contribution lies in defining the problem in a new revelatory way. Similarly, an assertion that a person of ordinary skill could combine the references, rather than that they would have been motivated to do so, is an impermissible form of hindsight. Moreover, knowledge of a problem and motivation to solve it are entirely different from motivation to combine particular references to reach the particular claimed invention.

17. I have been informed by Counsel that a motivation to solve a problem (or issue) is not the same as a motivation to have combined references. I have been informed by Counsel that whether a skilled artisan would be motivated to make a combination includes whether he/she would select particular references in order to combine their elements.

18. I have been informed by Counsel that the analysis of the motivation to combine should be explicit. Additionally, it must include articulated reasoning with rational underpinnings to support the conclusion of obviousness. Providing a full explanation of the motivation to combine the references and the reasonable expectation of success is a necessary component of the obviousness inquiry, as inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known. However, conclusory statements fail to

adequately explain why a person of ordinary skill would have a motivation to combine the potential prior art references.

19. I have been informed by Counsel that common sense, common wisdom, and common knowledge may be used to support a motivation to combine, so long as the use of common sense in the analysis is explained with sufficient reasoning. But, common sense can only be used to supply a limitation missing from the prior art where the technology is unusually simple and straightforward.

20. I also have been informed by Counsel that evidence suggesting reasons to combine cannot be viewed apart from evidence suggesting reasons not to combine. In analyzing motivation, both advantages and disadvantages must be considered. Teaching away, for example, is a statement in the prior art that either (i) discourages one from following the path of the claimed invention, or (ii) encourages one to follow a path that diverges from the path of the claimed invention. The concept of teaching away bears directly on whether there was a reason to combine prior art. Known disadvantages in prior art technology or devices which would naturally discourage a search for new inventions may also be taken into account in determining obviousness.

IV. Level of Ordinary Skill in the Art

21. Dr. Lee defines a person of ordinary skill in the art ("POSITA") as a person having "a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (*e.g.*, researching, designing, or teaching) NAND flash memory devices, or an equivalent level of skill, knowledge, and experience (*e.g.*, an advanced degree may replace some of the professional experience)." Ex. 1003 ¶ 36.

22. For the purposes of this declaration, I have not been asked to provide an opinion on the level of ordinary skill in the art. In view of my educational background and work experience, I surpass Dr. Lee's definition of a POSITA, and did so before August 21, 2018. Regardless of the precise definition of a POSITA, Ground 1 of the Petition does not show the challenged claims obvious. I reserve the right to opine as to an alternative level of a POSITA in other proceedings or if the Board institutes review in this proceeding.

V. Overview of the '254 patent

23. The '254 patent recognized that 3D memory devices require contacts that go vertically through the memory stack called "through array contacts" or "TACs" for "providing vertical interconnects between the stacked memory array device and peripheral device (e.g., for power bus and metal routing)." '254 patent, 4:55-59. In the past, these TACs were formed within a "dielectric stack

region within a memory stack," also referred to as a "barrier structure." *Id.*, 4:59-62. The drawbacks of a "barrier structure" is that "the regions enclosed by the barrier structures take up large area in the core array region where memory strings can be formed." *Id.* at 4:59-65. TACs within a barrier structure "also have a negative impact on the resistance of word lines." *Id.*, 4:59-65. "Moreover, the existing fabrication processes for forming the barrier structures become more challenging for the next generation 3D memory devices" which "have less process margin." *Id.*, 4:66-5:2.

24. The '254 patent discloses a novel "3D memory device having TACs not enclosed by barrier structures, which resolves the above-noted issues associated with the barrier structures." *Id.*, 5:3-6. The '254 patent explains that "by removing the barrier structures, the areas for TACs can be reduced while keeping their functions, thereby increasing memory cell density and decreasing process cost." *Id.*, 5:6-9. In addition, "[m]ore process margin"—i.e., room for error—"may be obtained due to the elimination of etching and alignment steps for making the barrier structures." *Id.*, 5:11-15. To "further simply the fabrication flow and reduce process cost," the '254 patent teaches that the non-barrier structure TACs can be "formed in the same fabrication process(es) for making other structures" such as "peripheral contacts" outside of the memory stack. *Id.*, 5:15-20.

25. Figure 1, reproduced below, illustrates a cross-section of an embodiment of a "memory stack 104" and a "staircase structure" 142. *Id.*, 8:61-63. As shown below, the memory device 100 includes a TAC 136 (yellow) that extends vertically through the stack to carry electrical signals to/from the memory device 100. *Id.*, 8:28-39. Unlike the prior art, TAC 136 is not "enclosed by barrier structures." *Id.*, 5:3-20. This allows the TACs to be "formed in the same fabrication process(es) for making other structures," including those ***outside*** the memory array such as "peripheral contact 148" (green). *Id.*, 5:3-20; 12:24-45. In addition, "dummy channel structures 146" are "disposed in the outer region 118 of memory stack 104 as shown in Fig. 1" to "provide mechanical support to the memory array structures, e.g., memory stack 104." *Id.*, 9:39-49.

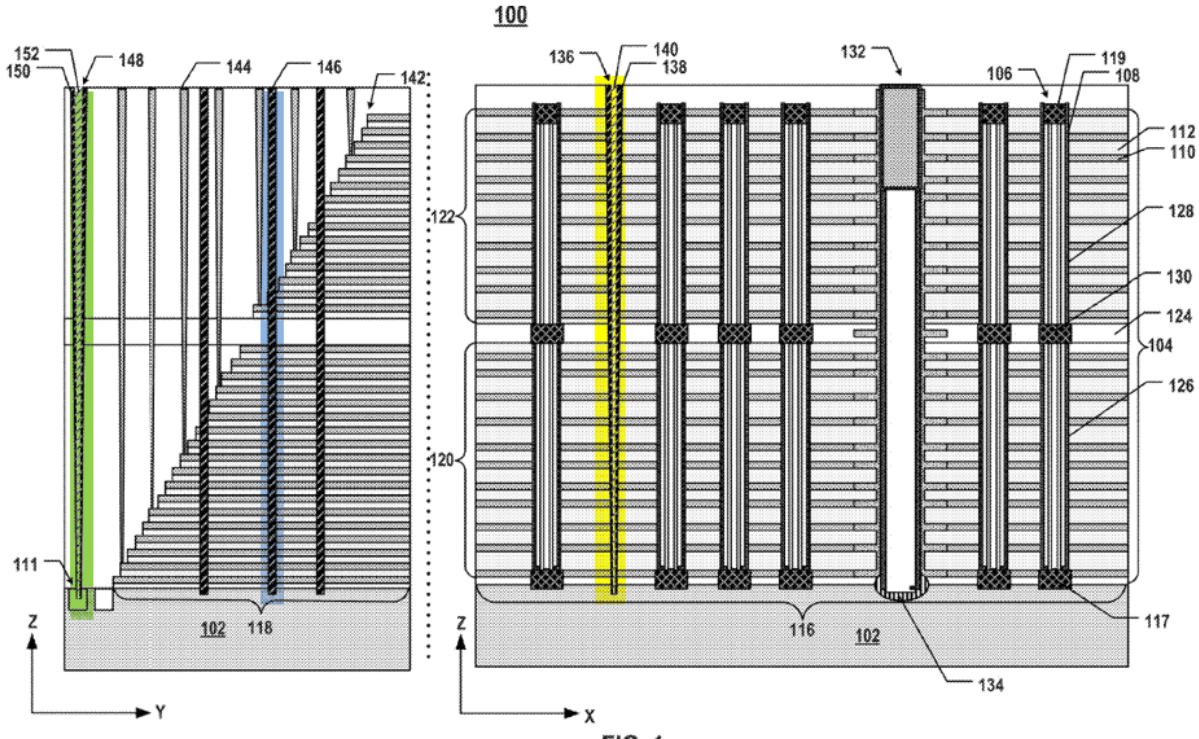


FIG. 1

26. The '254 patent discloses additional details about forming the claimed TACs not enclosed by a "barrier structure." Instead of forming the TACs in a "barrier structure" to isolate the TACs from other electrical components, the process for forming the TACs of the '254 patent start by forming openings in the memory stack itself for the TAC and then depositing "spacers" on the sidewalls of the openings. *Id.*, 12:64-67. Figure 7B, reproduced below, is a flowchart of an exemplary method for forming such a spacer for the first opening. *Id.*, 13:34-40. The method includes forming a plurality of shallow recesses by removing parts of the sacrificial layers the memory stack abutting the sidewall of the first opening. *Id.*, 13:36-40.

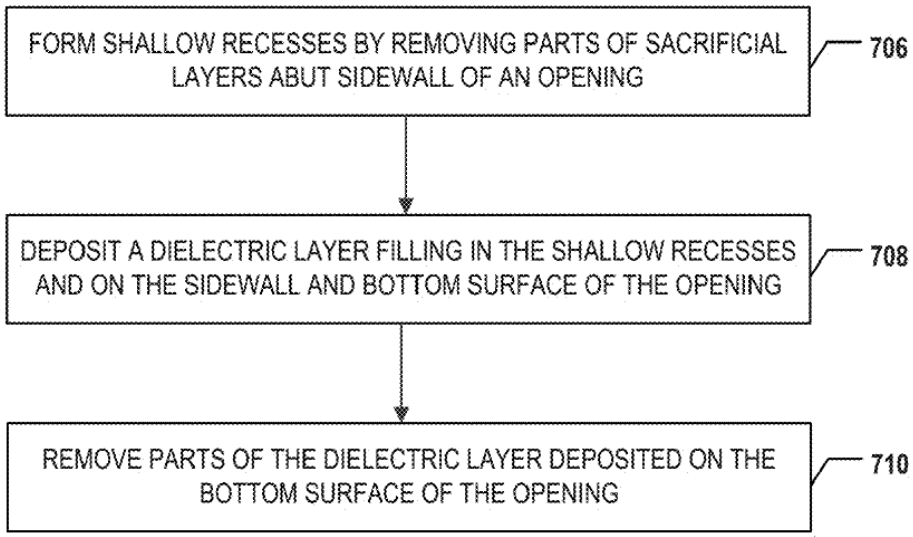


FIG. 7B

27. Exemplary recesses 312 are shown in Figure 3D, reproduced below. '254 patent 13:52-57. These recesses provide space for a thicker dielectric spacer deposition in step 708, resulting in improved electrical isolation, even without a barrier structure. '254 patent 13:59-61.

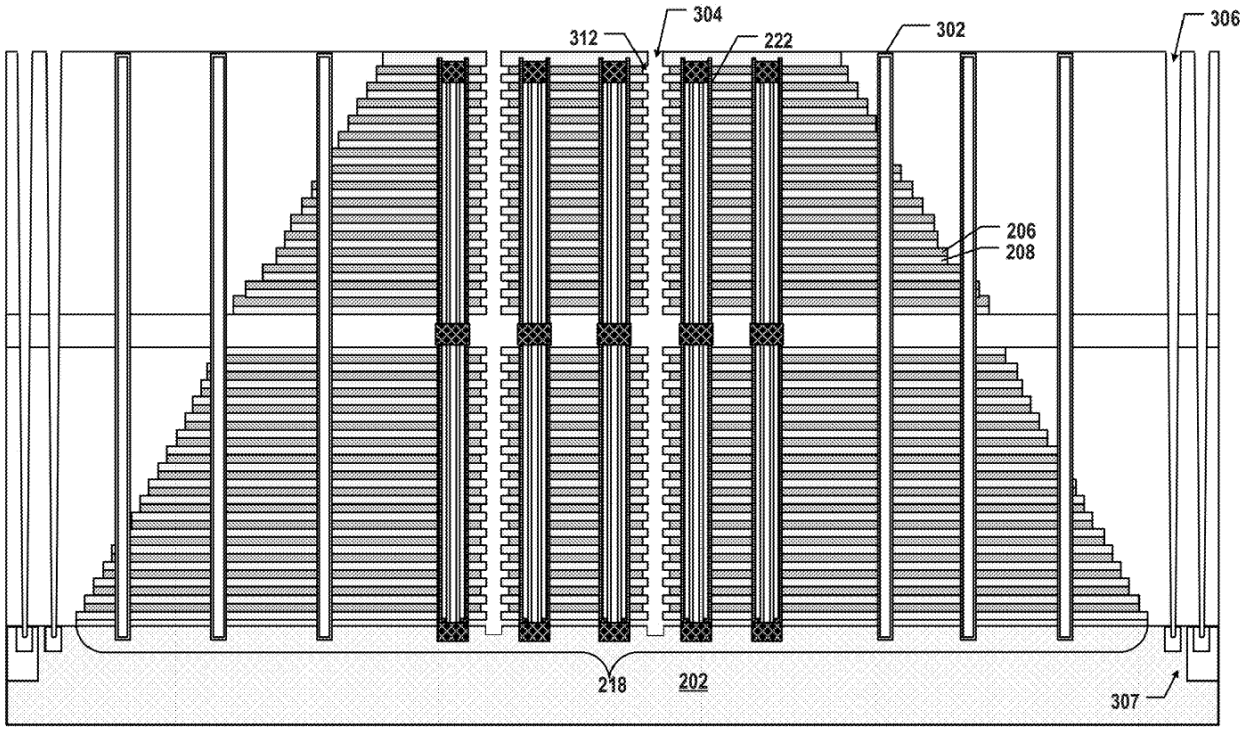


FIG. 3D

VI. A POSITA would not have found claims 2-4, 7-15, 17-18, and 20 obvious in view of Nakajima.

28. As a general matter, Dr. Lee relies on the knowledge of a POSITA to supply at least three features missing from Nakajima in relation to the challenged claims. In doing so, he relies on several patent documents from around the same time as the '254 patent. As I discuss further below, I do not agree that these documents supply the missing features, and none of the missing

features are simple. In fact, as I discuss more below, the field of 3D NAND memory manufacturing is not simple, as it pushes the limits of semiconductor fabrication in terms of size and complexity, and even seemingly small modifications can result in unforeseen problems.

A. Claims 2, 11-15, 17 ("dummy channel…through the stack")

29. Claim 2 recites "prior to forming the first opening, forming a dummy channel structure extending vertically through the stack."

30. Dr. Lee opines that "it would have been understood and certainly obvious (a POSITA would have been motivated with a reasonable expectation of success) that Nakajima also forms dummy channels for several reasons." Ex. 1003 ¶ 101. However, in his subsequent discussion (¶¶ 102-109) he does not cite to any portion of Nakajima as disclosure of forming dummy channels. Instead he asserts that aspects of dummy channels were known to a POSITA (¶¶ 102-104) and disclosed in other patent literature (¶¶ 105-108).

31. The Petition also does not cite to any passage of Nakajima as disclosing formation of a dummy channel structure. Petition at 38-41. Rather, the Petition states that "[i]n view of the knowledge of a POSA, it would have been obvious to implement some of Nakajima's channels as dummy channels." Petition at 39.

32. Based on the above, I understand the Petition to be proposing a modification of Nakajima to "implement some of Nakajima's channels as dummy channels" based on the supposed "knowledge of a POSA." Petition at 39. As an initial matter, I note that forming a dummy channel structure is not unusually simple, and involves complex semiconductor manufacturing processes, including "wet etching, and/or dry etching, such as DRIE" and "thin film deposition processes, such as ALD, CVD, PVD." '254 patent, 12:7-23.

33. Dr. Lee annotates Figure 2 of Nakajima as shown below, highlighting Channels CL in region 110a in a purple box. *See also* Petition at 33 (same annotation). These are the channels "CL" of which the Petition proposes "some" to be implemented as "dummy channels." Petition at 39.

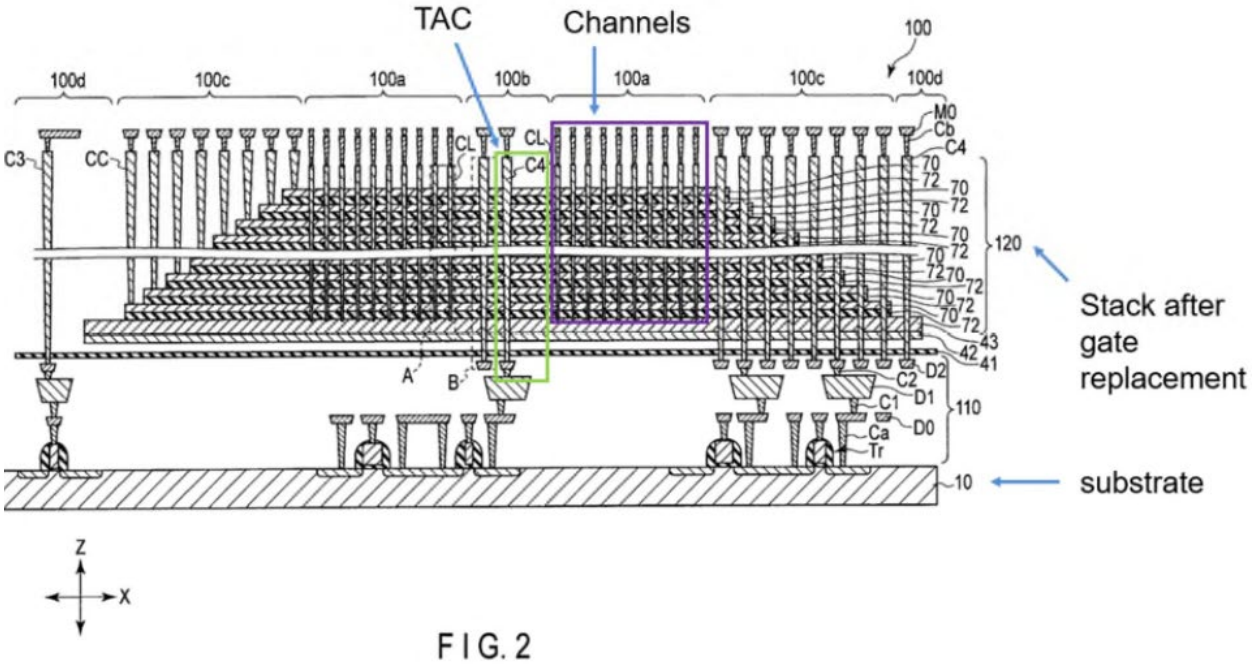


FIG. 2

34. These channels "CLs" (also called "pillar structures CL") are all in the "memory cell array areas 100a" and include functional structures, such as "a core layer 50, a semiconductor layer 20, and a memory layer 30." Nakajima, 5:16-21; *see* Fig. 4. The semiconductor layer 20 "functions as a channel." Nakajima 5:55-56. Together, the "semiconductor layer 20, the memory layer 30, and the conductive layer 70 constitute a memory cell MC." Nakajima 5:49-50. In other words, the channels CL include functional components of the memory cells, and have vital roles in the device. The Petition does not explain how Nakajima's system could function as intended (i.e., as NAND flash memory) if these functional channels were implemented them as dummy components that only provide structural, mechanical support. But even setting aside operability, replacing channels with dummy structures will significantly decrease the memory's storage capacity because channels are a part of every memory cell. A POSITA would have recognized that decreasing storage capacity is an undesirable result, which is not even offset by additional benefit in the proposed combination.

35. Dr. Lee asserts that "dummy channels provide structure support, which is important during the gate line replacement process (because that process forms voids where the sacrificial gates were, necessitating support members to prevent the stack from collapsing)." Ex. 1003 ¶ 104. But Dr. Lee omits that

Nakajima discloses the pillar structures CL—which are not dummy structures—already provide this support. Specifically, Nakajima discloses that after "the sacrifice layers 71 are removed," the remaining "insulation layers 72 of the layer stack" are "***supported by physical joints with such pillar structures CL***, and thereby the ***gaps 73 between the insulation layers 72 are maintained***." Nakajima, 8:24-29. Thus, Nakajima has no need for dummy channels. And changing Nakajima's pillar structures CL to dummy channels would require additional processing steps because the CL pillar structures would now be formed with different structure than others. Notably, Dr. Lee asserts (relative to claim 3) that "it was the norm to form all instances of a contact type at the same time" (¶ 112) and doing so "would significantly reduce processing time" (¶ 113). But he does not address that making some pillar structures CL as dummy channels would require a separate process to deposit the different materials needed to form dummy channels (e.g., dielectric materials instead of semiconductor layer 20).

36. The Petition cites to three references—Kai, Kim, and Park—that purportedly "confirm[] the knowledge of a POSITA." Petition at 39. None of these references disclose dummy structures within the memory array, as the Petition and Dr. Lee propose, and thus none of them motivate implementing "some" of Nakajima's channels CLs as dummy structures. Nakajima, 2:54-55

(Nakajima's channel structures (CLs) are within the "memory cell array areas 100a").

37. For example, the Kai reference (Exhibit 1015) discloses "support pillars 20" (blue) in a "***contact region 300***" (yellow) that is "between the memory array region 100 and the peripheral device region 200." Kai, 6:2-5, Fig. 6A; *see also* Fig. 15A (showing "support pillars 20" only in the connection region).

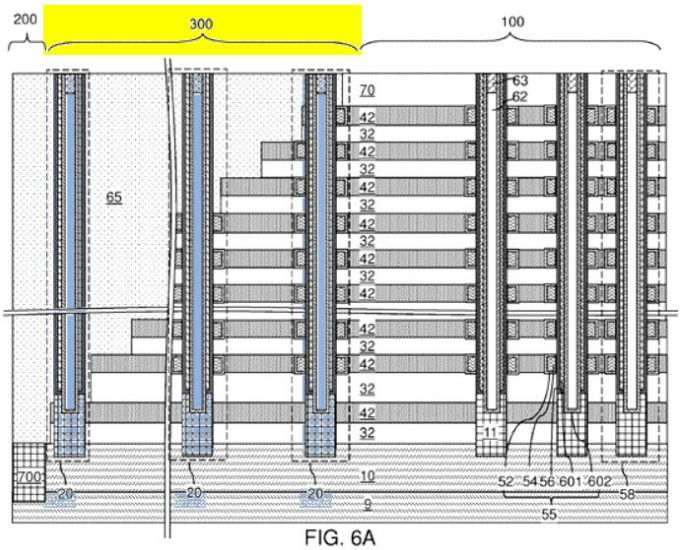


FIG. 6A

In contrast, the "memory array region 100" includes what the Petition calls "active channel structures" that "include contacts (88)" to the upper level, as shown in Figure 15A.

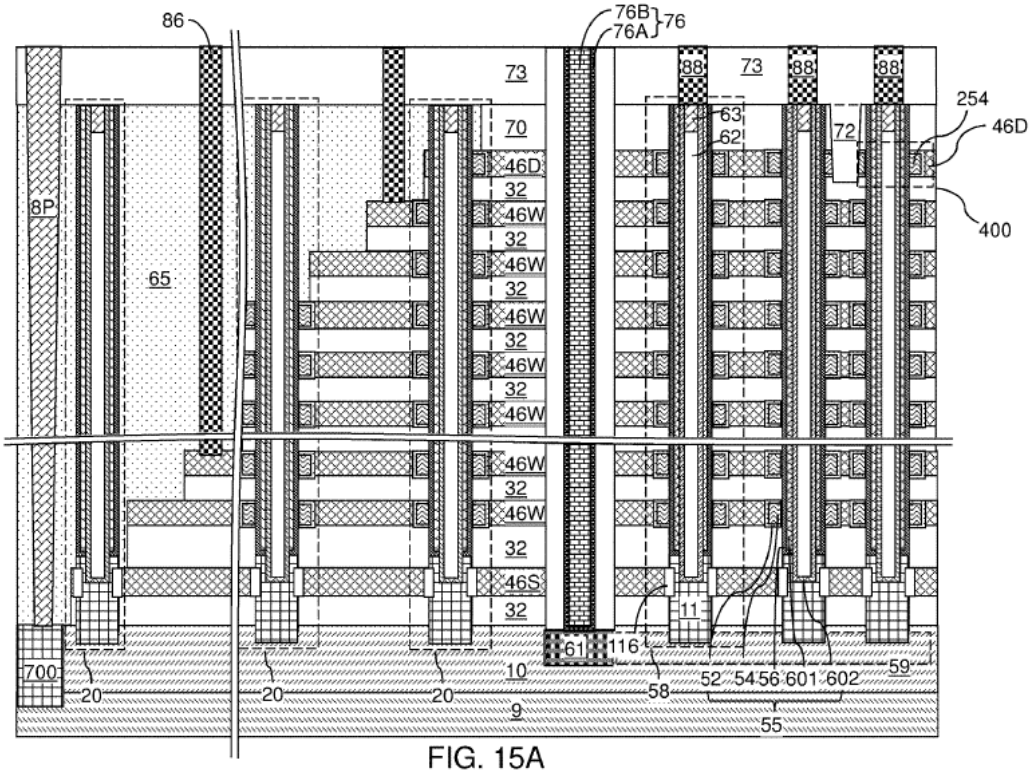
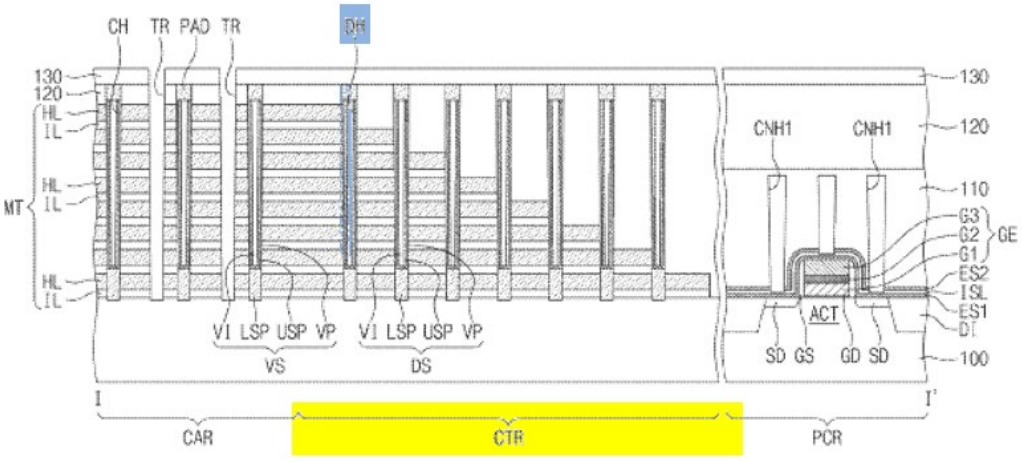


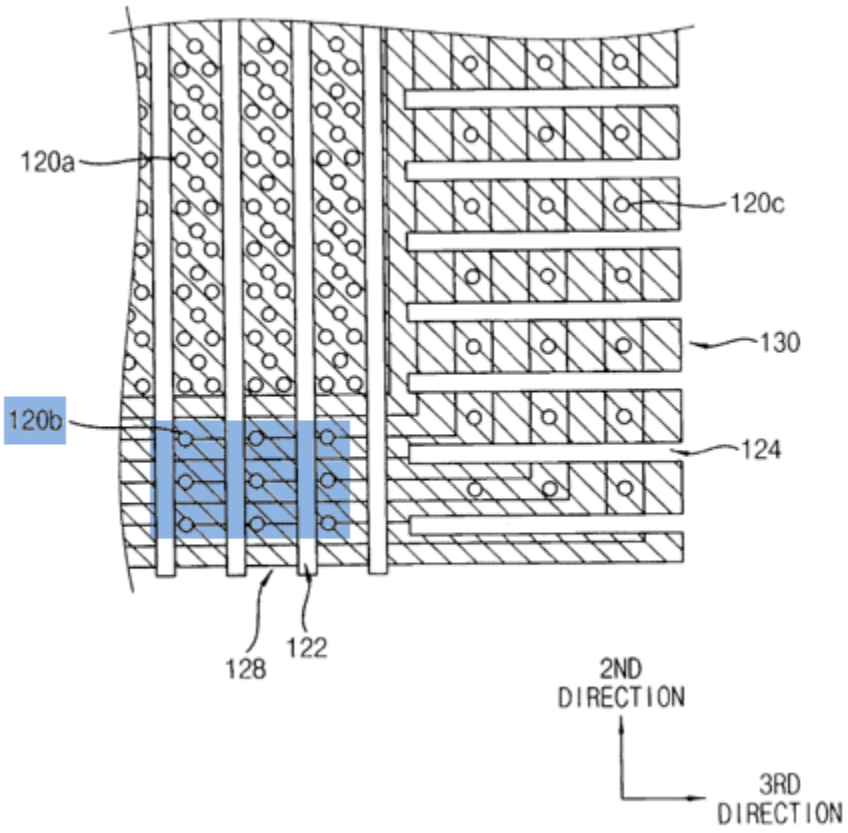
FIG. 15A

38. Similarly, the Kim reference (Exhibit 1017) discloses "dummy holes DH" (blue) in a "Connector Region CTR" (yellow) that is outside the "Cell Array Region (CAR)," i.e., the memory array. Kim, Figure 13 (below), [0047]; *see* Petition at 39 (citing Kim [0047]) ("The stack structure ST may be penetrated with a plurality of dummy holes DH ***on the connection region STR***"); *see also* Kim [0070] ("***On the connection region CTR***, a plurality of dummy holes DH may be formed.").

FIG. 13



39. For its part, Park (Exhibit 1016), discloses separate "cell and dummy regions." Park, Abstract. Park discloses "second channel structure 120b" that are "disposed on the wiring region"—not the "main cell region" with channel structures 120a—and "may not be provided as the portion of the memory cell." *Id.*, 7:38-44. Park's Figure 8, annotated below, shows that the "second channel structure 120b" (shown in blue) are dummy channels in an area separate from the "first channel structure 120a … disposed on the main cell region." *Id.*



40. To summarize, none of Kai, Kim, or Park, teach forming dummy channels in the memory array. Rather, at most each of these references teaches dummy structures in a separate area outside of the memory array, called "contact region" (Kai), "connector region CTR" (Kim), or "dummy regions" (Park). None of Kai, Kim, or Park would have motivated a POSITA to change Nakajima's "pillar structures CL" that are ***in the "memory cell array area 100a"*** into dummy structures—especially because, as discussed above, Nakajima's pillar structures CL already provide the structural support that the Petition asserts is provided by the dummy structures, and modifying structures within the memory cell array would require (1) additional processes to form the different pillar structure and

(2) removing functional channels from the device (or further additional structures to compensate for the loss of functional channels).

41. The Petition asserts other supposed benefits to forming Nakajima's channels CLs as dummy channels. I disagree that they would have motivated a POSITA to make the proposed modification. As I mentioned above, changing the pillar structures in region 100a to dummy structures would remove the channel functionality of the pillars, which would require some additional modifications to the structure to correct for (which the Petition does not address). It would also make the fabrication process more complicated and reduce capacity, as I mentioned above.

42. The Petition also asserts that "adding the additional dummy structures would result in reducing the likelihood of defective bits on the edge of the memory cell regions because the addition of the additional rows extends the memory cell pattern for those respective columns into the dummy region." Petition at 40. It is not clear what the Petition means by "addition of the additional rows" in this sentence. Further, Nakajima does not include a dummy region. Nevertheless, this does not motivate implementing Nakajima's functional channels CL as dummy structures, for similar reasons that Kai, Kim, and Park don't. Additionally, to the extent Dr. Lee discusses employing dummy channels "at the edge of the array" to provide support to mitigate against abnormalities, I

disagree. *See* Ex. 1003 ¶ 102. Specifically, the edge of the array in Nakajima does not need such support, as it employs through-array contacts (TACs)—not dummy channels—in staircase region 100c that provide structure support at the edge of the array. This is shown in Figure 2 of Nakajima, annotated below.

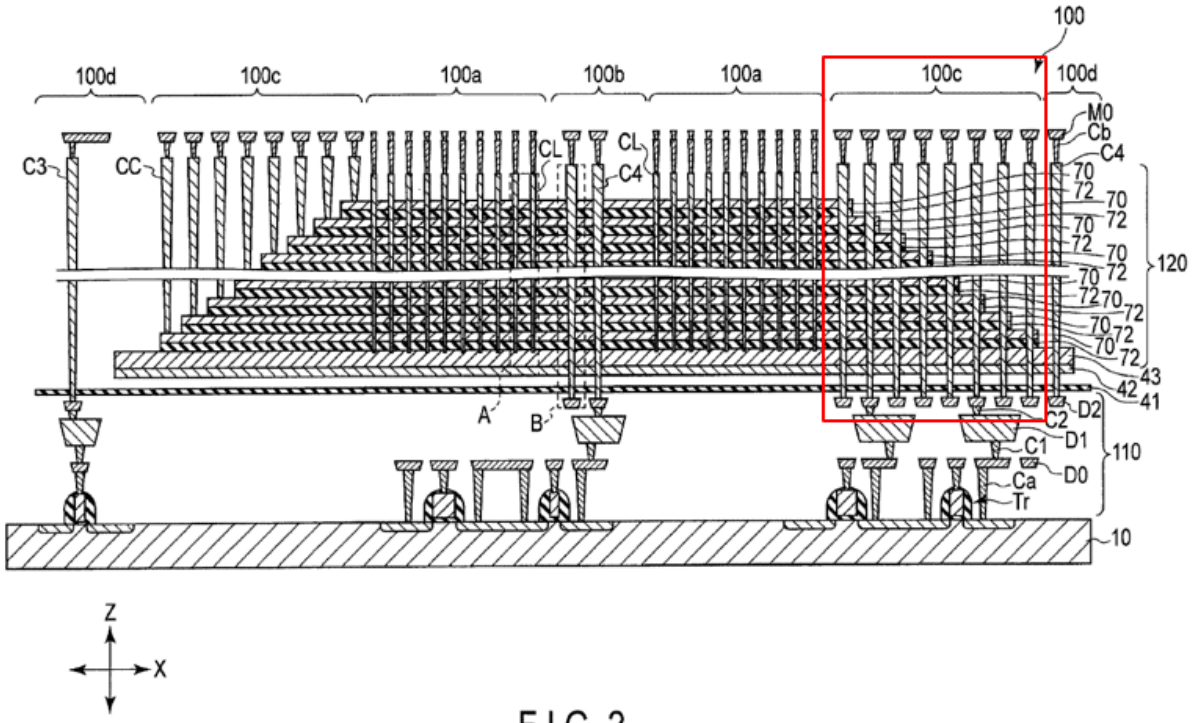


FIG. 2

43. Although I focused on claim 2 above, these opinions also apply to claim 11 for the same reasons as claim 2, because claim 11 similarly recites "forming a dummy channel structure extending vertically through the stack." Claims 12-15 and 17 depend from claim 11.

B. Claims 3-4, 9-10, 18, 20 ("simultaneously etching" a "first opening through the stack" and a "second opening outside of the stack")

44. Claim 3 recites "wherein forming the first opening comprises simultaneously etching the first opening through the stack and a second opening outside of the stack." The claimed "stack" refers to "a plurality of dielectric/sacrificial layer pairs on a substrate" as inherited from claim 1.

45. Dr. Lee asserts that "Nakajima discloses forming holes H1 through the stack for its TAVs (C4)" and that "one C4 is completely outside the stack." Ex. 1003 ¶ 111. Dr. Lee annotates Figure 2 (reproduced below) to show this C4 "outside the stack" and maps it as filling "a second opening." *Id.*

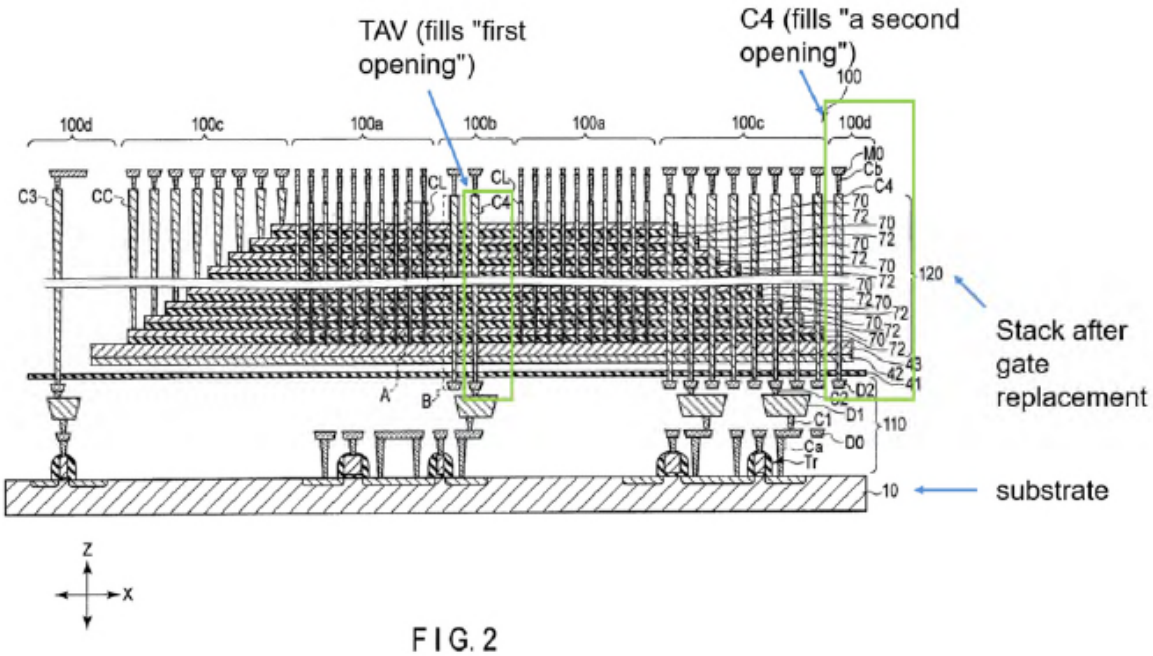


FIG. 2

46. Dr. Lee seems to assume that because this C4 in region 100d is outside the stack, and it must have filled and *opening* that was formed outside the

stack. That is incorrect. In column 7, Nakajima discloses "[a] process of manufacturing the contact C4." Nakajima 7:8-9. Here, Nakajima explicitly teaches that the H1 holes (which Dr. Lee agrees are used to form C4 structures) are "formed in…the layer stack 120, as shown in FIG. 8." Nakajima, 7:37-39. For example, "[t]he hole H1 penetrates the insulation layers 44, 62, and 63, *and the layer stack 120*, to reach the silicon nitride layer 41." Nakajima 7:41-43. Nakajima's Figure 8 is reproduced below with annotations, showing hole H1 penetrating the stack, which comprises alternating layers of insulation layer 72 and sacrifice layer 71. Nakajima 7:28-31 ("[A]lternately stacking the insulation layer 72 and the sacrifice layer 71 is repeated, so that the layer stack 120…is formed.").

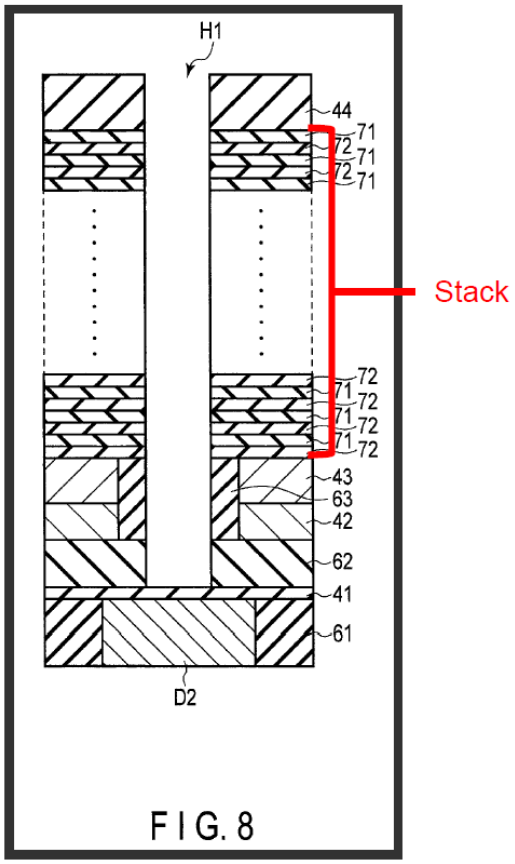


FIG. 8

47. Dr. Lee identifies the same structure as the claimed stack. Ex. 1003 ¶ 79 ("Nakajima discloses forming a stack ('layer stack' 120) comprising a plurality of dielectric ('silicon oxide layers' 72)/sacrificial layer ('sacrifice layers 71')…."). Dr. Lee further annotated Figure 7 (before the hole is formed) as including the stack.

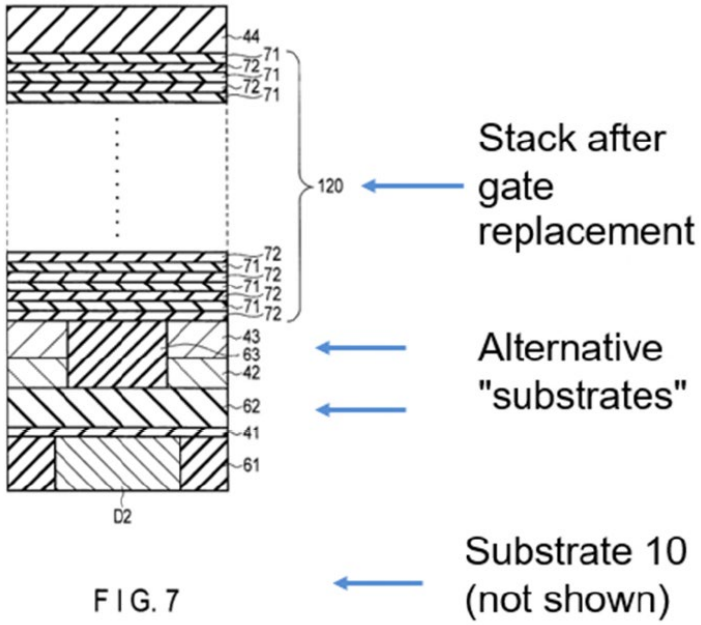


FIG. 7

48. Nakajima does not disclose or suggest forming hole H1 outside the stack, let alone forming an opening outside the stack simultaneously with an opening through the stack. Figure 2 is no exception. As Dr. Lee states, "Nakajima only discloses one set of steps for forming the C4 contacts" (Ex. 1003 ¶ 112 (citing Nakajima 7:5-8:11) and that set of steps requires forming a hole through the stack. The fact that a C4 structure may exist outside the stack in the final structure (as shown in Figure 2) does not teach that the hole H1 formed for the structure was etched outside the stack. Dr. Lee ignores that a C4 structure formed through the stack (as explicitly taught by Nakajima) may end up outside the stack in the final structure (e.g., Figure 2) if the portions of the stack are removed after holes H1 are etched through the stack.

49. Further, Dr. Lee does not address the fact that applying a single etching process at the same time on two different materials would result in different etch rates, and thus different-sized holes H1. Nakajima never suggests that to be the case for the H1 holes, and Dr. Lee does not address it. Instead, Dr. Lee points to contacts CC/C3 as evidence that holes could be etched simultaneously within the stack and outside the stack—asserting that contact CC is formed "partially through the stack" at the same time as contacts C3 "which do not travel through the stack." Ex. 1003 ¶ 114. But as shown below, CC is not illustrated as being "through the stack," and unlike the C4, the holes for CC are explicitly formed *after* the staircase region. Nakajima 17:38-41 (holes for CC reach terrace in staircase region), 16:49-52 (staircase formed before holes for CC).

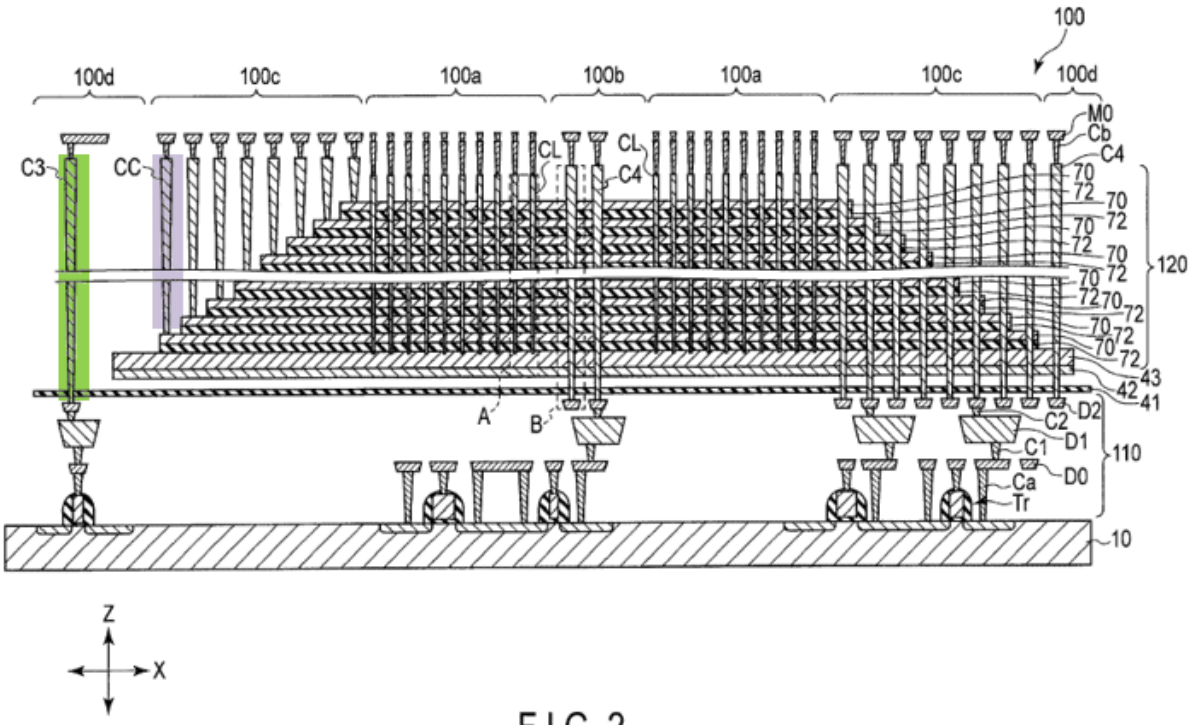


FIG. 2

50. Further, the comparison of CC and C3 demonstrate that such holes reach different depths because of the different materials they penetrate. Nakajima 17:38-43 (holes for CC stop at terrace, whereas holes for C3 reach interconnect D2). In contrast to this discussion of CC and C3, Nakajima never hints that any hole H1 for C4 contacts is formed outside the stack, and explicitly teaches the opposite. Additionally, the identical depths for the C4 contacts (Figure 2) further teaches a POSITA that the holes were etched through the same material—i.e., through the stack. Penetrating the stack by etching holes H1 while simultaneously penetrating a different material (such as silicon oxide layer 65) outside the stack

to the *same* depth using the *same* process is unlikely to have been successful and is not something Nakajima suggests.

51. Dr. Lee cites Tessariol (Exhibit 1023) as teaching simultaneous etching of openings through different numbers of layers of the stack, it's clear from the passage Dr. Lee cites that both sets of openings are formed *through* the stack unlike the claimed first and second openings of claim 3. Ex. 1003 ¶ 114 (citing Tessariol [0037] and Figure 9). For example, Dr. Lee cites to openings 56 and 54 as being formed at the same time and characterizes Figure 9 as showing these holes extending through "stack layers."

52. Finally, Dr. Lee asserts that Mushiga (Exhibit 1010) demonstrates that forming "forming through-array contacts…at the same time in various portions of the memory device was routine and well understood." Ex. 1003 ¶ 115 (citing Mushiga Fig. 5, 10:31-58). But Mushiga never describes the cavities for these contacts as being formed simultaneously through and outside of the stack. *See* Mushiga 10:31-58. The most Mushiga discloses about the topic of timing is that the "cavities can be formed before or after formation of the electrically conductive layers (146, 246)." Mushiga 10:49-57. But this does not require or suggest forming the cavities at the same time through the different materials that the two cavities penetrate. *See* Mushiga, Fig. 5, 10:31-38. Nor does it provide any motivation to a POSITA to modify Nakajima's explicit disclosure of forming its

holes H1 for contacts C4 through the stack, especially in light of the complexities of making such extensive modifications as discussed above.

53. Although the above discussion focused on claim 3, it also applies to claims 4, 9-10, 18, and 20. Specifically, claim 9 similarly recites "simultaneously etching the first opening through the stack, a second opening outside of the stack, and a third opening through the stack." Claim 10 depends from claim 9. Claim 18 also recites "simultaneously etching a first opening through the stack, a second opening outside of the stack, and a third opening through the stack." Claim 20 depends from claim 18; claim 4 depends from claim 3; and claim 10 depends from claim 9.

C. Claims 7-8, 14-15 ("forming a plurality of shallow recesses by removing parts of the sacrificial layers abutting the sidewall of the first opening")

54. Claim 7 recites "forming a plurality of shallow recesses by removing parts of the sacrificial layers abutting the sidewall of the first opening." Notably, "the first opening" in claim 7 is the opening through which the "through array contact (TAC)" is formed in independent claim 1.

55. Dr. Lee discusses claim 7 under two interpretations: first, an interpretation that "include[s] largely undetectable and unintentional recesses" (Ex. 1003 ¶¶ 126-127); and second, an interpretation that requires "[c]reating

intentional lateral recesses." Ex. 1003 ¶ 128. In my opinion, neither interpretation is rendered obvious based on Nakajima.

56. First, Dr. Lee cites Exhibit 1030 for support that "typical prior art etches that effectively create a hole through the stack result in very small lateral recesses in either the dielectric spacers or sacrificial layers." Ex. 1003 ¶ 127. The cited passage of 1030 says no such thing. Rather, the passage describes "a lack of etching a plurality of alternating layers of SiO and SiN layers in a 3D NAND application using a nontraditional hydrofluorocarbon etching gas." Ex. 1030 2:56-58. "Although there are numbers of prior arts for SiO2 etching with high selectivity to SiN, for certain applications, it is important to have an etching gas which can etch both SiO2 and SiN layers…without selectivity." Ex. 1030 2:59-63. "In another word, it is a challenge to find an etch gas that has similar high etch rates of SiO2 and SiN in terms of getting a smooth sidewall of high aspect ratio holes in 3D NAND memory." Ex. 1030 2:63-67. This passage describes that it is important to have an etching gas without selectivity (which etches the layers evenly) and the patent itself purports to provide a solution. As Exhibit 1030 further explains, its proposed solution mitigates against sidewall bowing or barreling as depicted in Figure 1d, below. Ex. 1030 18:38-63. Exhibit 1030 further describes bowing as undesirable, and does not motivate or inform a

POSITA that such a pattern would be formed in Nakajima. Ex. 1030 18:42-44. Nor does it suggest forming a plurality of shallow recesses.

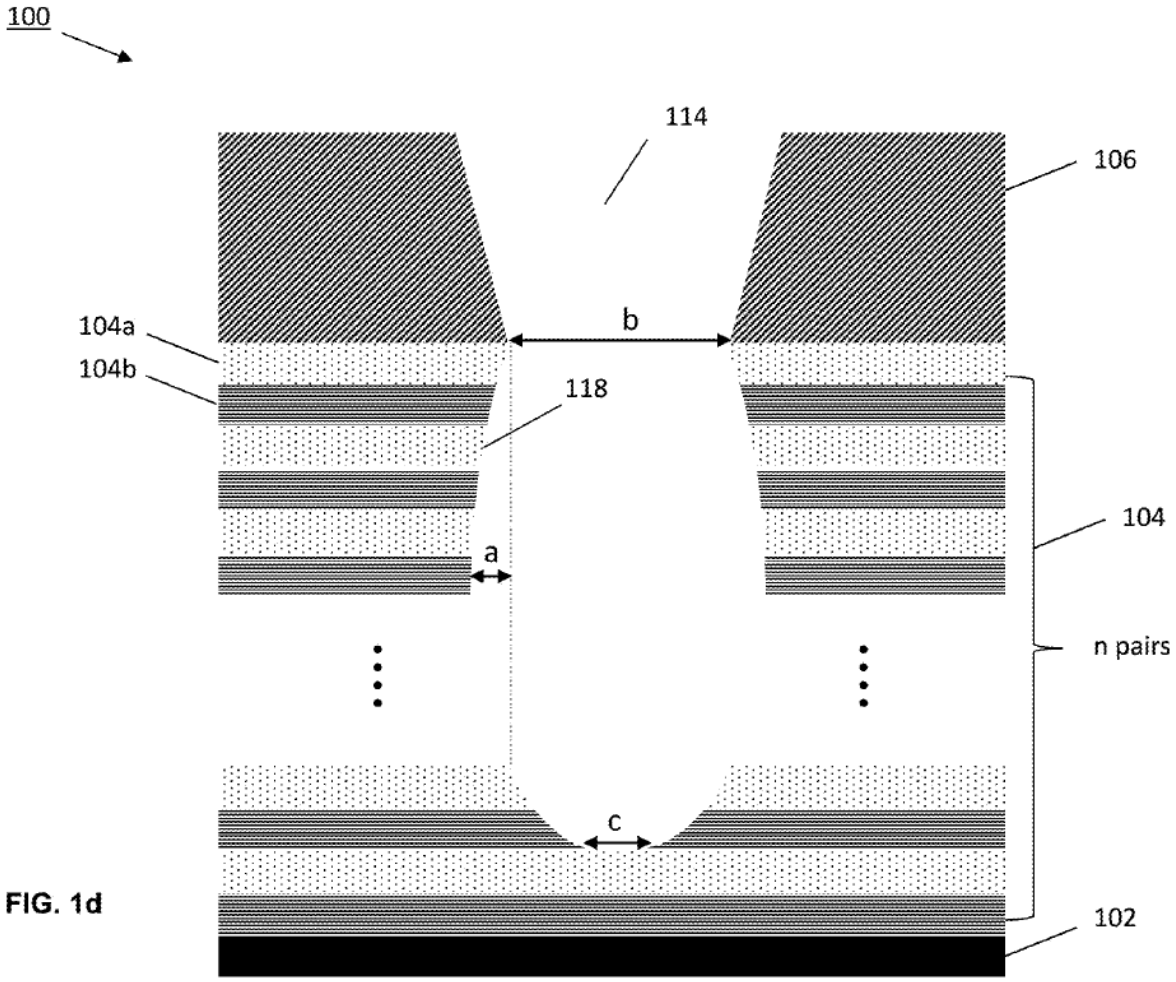


FIG. 1d

Ex. 1030 Fig. 1d

57. Second, with respect to what Dr. Lee asserts to be the "correct" claim interpretation, Dr. Lee asserts that intentional lateral recesses in a hole "for a contact" was also known. Ex. 1003 ¶¶ 128-131. For support, Dr. Lee relies on Cui (Ex. 1031) and Kai (Ex. 1015). However, neither Cui nor Kai disclose or

suggest forming shallow recesses by removing parts of the *sacrificial layers* abutting the sidewall of an opening for a "through array contact (TAC)" as required by claim 7. And doing so is not unusually simple or particularly straightforward. Forming recesses in sacrificial layers is highly technical and complex, and requires, among other things, that "the lateral dimension of shallow recess" be "controlled by the etching rate and/or etching time." '254 patent, 13:48-61.

58. Cui, for example, discloses forming ribbed cavities by removing portions of *insulating* layers, leaving the sacrificial layers intact. Cui 26:23-25 ("[A]n isotropic etch process can be performed to laterally recess the ***insulating layers*** (132, 232) with respect to the spacer material layers such as the first and second sacrificial material layers (142, 242)."). The claims, however, require forming the "shallow recesses" by "removing parts of the ***sacrificial layers***"—not "insulating layers." In fact, as shown by Figure 16A (reproduced below), Cui's etching deliberately does ***not*** form recesses in the sacrificial layers 142 as required by the claims of the '254 patent. *Id.*; *see also* Cui Fig. 16A.

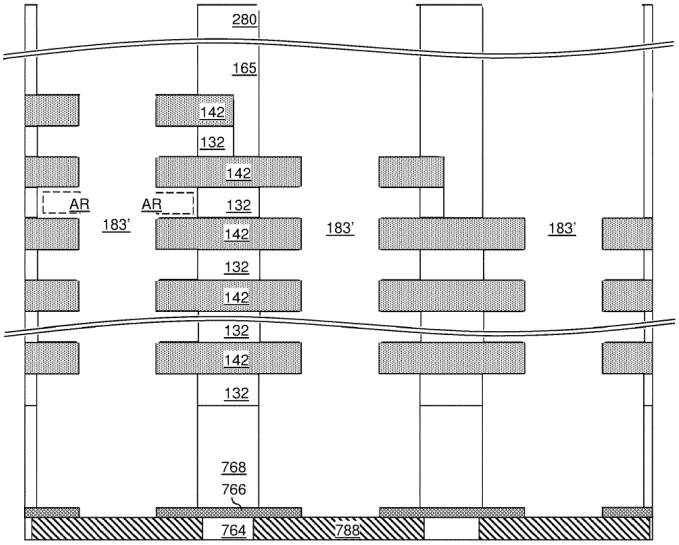


FIG. 16A

59. Dr. Lee asserts that forming recesses in "sacrificial gates" was "known" and cites to Kai for support. Ex. 1003 ¶ 130 (citing Kai 11:9-34). But Kai says nothing about forming recesses in the sacrificial layers of an alternating stack of dielectric and sacrificial layers for openings associated with a TAC as claimed.

60. Although the above discussion is framed in view of claim 7, it applies equally to claims 8, 14, and 15. Claim 8 depends from claim 7. Claim 14 similarly recites "forming a plurality of shallow recesses by removing parts of the sacrificial layers abutting the sidewall of the first opening." Claim 15 depends from claim 14.

VII. CONCLUSION

All statements made herein of my own knowledge are true, and all statements made on information and belief are believed to be true. Further, I am aware that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001. I declare under penalty of perjury that the foregoing is true and correct.

Executed on February 21, 2025, in Arden Hills, Minnesota.

Stephen Campbell

Stephen Campbell