

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

IPR2025-00034
Patent 10,879,254 B2

Before JO-ANNE M. KOKOSKI, KIMBERLY McGRAW, and
MICHAEL T. CYGAN, *Administrative Patent Judges*.

CYGAN, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. *Background and Summary*

Micron Technology, Inc. (“Petitioner”) filed a Petition requesting an *inter partes* review of claims 1–15, 17, 18, and 20 of U.S. Patent No. 10,879,254 B2 (Ex. 1001, “the ’254 patent”). Paper 1 (“Pet.”). The Petition is supported by a Declaration from Dr. Jack C. Lee. Ex. 1003 (“Lee Declaration”). Yangtze Memory Technologies Company, Ltd. (“Patent Owner”) filed a Preliminary Response to the Petition. Paper 10 (“Prelim. Resp.”). The Preliminary Response is supported by a Declaration by Dr. Stephen Campbell. Ex. 2007. On February 21, 2025, Patent Owner filed a Statutory Disclaimer of claims 1, 5, and 6. Ex. 2005.

Petitioner has acknowledged the existence of a second petition challenging the same claims of the ’254 patent, and ranked that second petition lower than the one filed in this proceeding. Paper 6. Patent Owner argues that instituting trial on both petitions is not warranted. Paper 11. Because this proceeding addresses the higher-ranked petition, we need not here decide the issue of whether a second petition is warranted.

We have authority to determine whether to institute an *inter partes* review. *See* 35 U.S.C. § 314; 37 C.F.R. § 42.4(a). The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted “unless . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” Institution of *inter partes* review, however, is discretionary. *See Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1367 (Fed. Cir. 2016) (“[T]he PTO is permitted, but never compelled, to institute an IPR proceeding.”). For the reasons discussed below, we determine that Petitioner establishes a reasonable likelihood of

prevailing with respect to the unpatentability of at least one claim of the '254 patent. We also determine that the arguments and evidence of record do not support discretionary denial of the Petition under 35 U.S.C. § 314(a). Accordingly, we institute an *inter partes* review of claims 2–4, 7–15, 17, 18, and 20 of the '254 patent.

B. Patent Owner's Disclaimer of Claims 1, 5, and 6

As indicated above, Patent Owner filed a statutory disclaimer of claims 1, 5, and 6 of the '254 patent. *See* Ex. 2005. In view of Patent Owner's statutory disclaimer, we treat claims 1, 5, and 6 as having never been part of the '254 patent. *See Vectra Fitness, Inc. v. TNWK Corp.*, 162 F.3d 1379, 1383 (Fed. Cir. 1998) ("This court has interpreted the term 'considered as part of the original patent' in [35 U.S.C.] § 253 to mean that the patent is treated as though the disclaimed claims never existed."). Because *inter partes* review cannot be instituted based on disclaimed claims, claims 1, 5, and 6 are outside the scope of this proceeding. 37 C.F.R. § 42.107(e) ("No *inter partes* review will be instituted based on disclaimed claims."); *General Elec. Co. v. United Techs. Corp.*, IPR2017-00491, Paper 9 (PTAB July 6, 2017) (precedential) (denying institution in view of a statutory disclaimer of all the challenged claims). Thus, we confine our analysis in this Decision to claims 2–4, 7–15, 17, 18, and 20, the challenged claims that have not been disclaimed.

C. Real Parties-in-Interest

Petitioner identifies itself and its subsidiaries, including Micron Consumer Products Group LLC, as real parties-in-interest. Pet. 5. Patent Owner identifies itself as the real party-in-interest. Paper 5, 1.

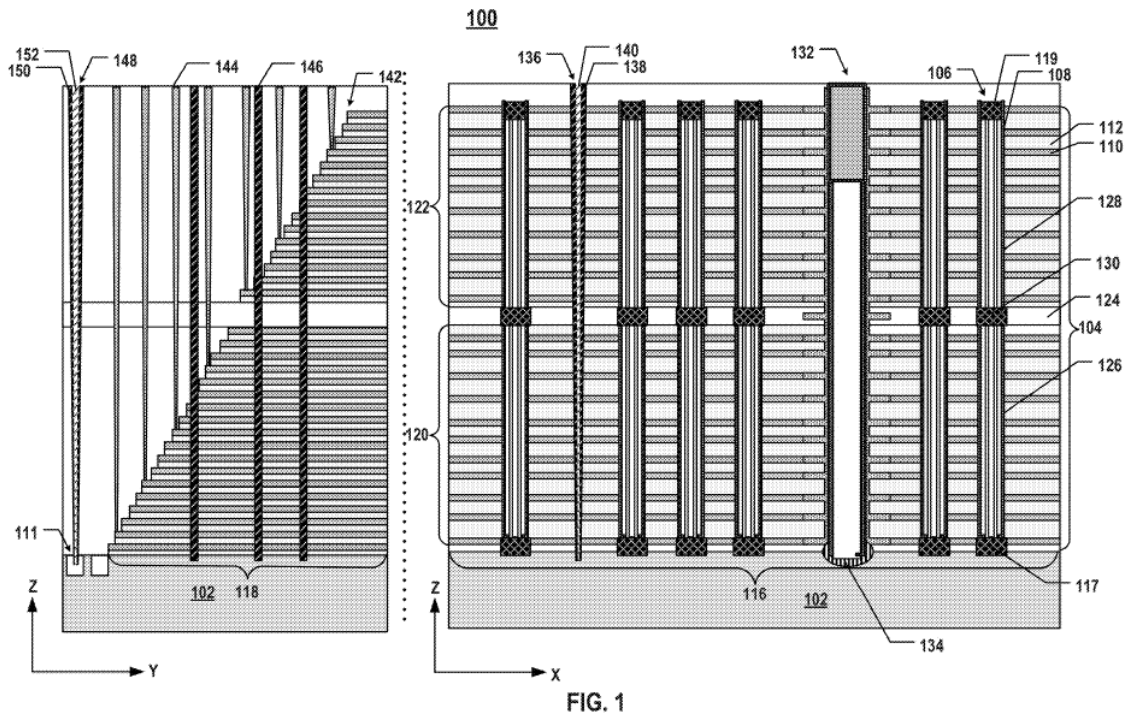
D. Related Matters

The parties represent that the '254 patent is involved in *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC*, Case No. 3:23-cv-05792-RFL (N.D. Cal., filed November 9, 2023). Paper 5, 1; Pet. 5. Petitioner also filed IPRs challenging each patent asserted in the district court case. Pet. 5–7.

E. The '254 Patent

The '254 patent is titled “Three-Dimensional Memory Devices Having Through Array Contacts and Methods for Forming Same.” Ex. 1001, code (54). The '254 patent issued on December 29, 2020, from Application No. 16/745,343, filed on January 17, 2020, and is a continuation of U.S. Application Number 16/149,103, filed on October 1, 2018, which in turn is a continuation of Application Number PCT/CN2018/101482, filed on August 21, 2018. *Id.* at codes (21), (22), (63).

The '254 patent relates to a staircase structure for a 3D memory device including a dielectric stack, including a plurality of dielectric/sacrificial layer pairs, having a channel structure extending vertically therethrough. *Id.* at code (57). A through-array contact is formed vertically in an opening in the dielectric stack, separated by a spacer from a sidewall of the opening. *Id.* Figure 1 of the '254 patent illustrates the structure:



Ex. 1001, Fig. 1. Figure 1 depicts memory device 100 having memory stack 104 including interleaved conductor layers 110 and dielectric layers 111, which include channel structure 108 filled with semiconductor, and through array contacts 136 having conductive material 140 and spacer 138. *Id.* at 5:20–8:60.

F. Illustrative Claim

Claims 1 (disclaimed), 11, and 18 are independent. Claim 2 is illustrative, and depends on claim 1, which recites as follows:¹

[1.PRE] A method for forming a three-dimensional (3D) memory device, comprising:

[1.A] forming a stack comprising a plurality of dielectric/sacrificial layer pairs on a substrate;

[1.B] forming a channel structure extending vertically through the stack;

¹ Bracketed organization added as per the Petition.

[1.C] forming a first opening extending vertically through the stack;

[1.D] forming a spacer on a sidewall of the first opening;

[1.E] forming a through array contact (TAC) extending vertically through the stack by depositing a conductor layer over the spacer in the first opening; and

[1.F] after forming the TAC, forming a slit extending vertically through the stack.

Claim 2 recites:

[2] The method of claim 1, further comprising prior to forming the first opening, forming a dummy channel structure extending vertically through the stack.

G. Evidence

Petitioner relies on the following patent document evidence.

Name	Patent Document	Exhibit
Nakajima et al. “Nakajima”	US 10,777,501 B2	1005

H. Prior Art and Asserted Grounds

Petitioner asserts that claims 2–4, 7–15, 17, 18, and 20 would have been unpatentable on the following ground:²

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
2–4, 7–15, 17, 18, 20	103 ³	Nakajima ⁴

² Although Petitioner challenged claims 1–15, 17–18, and 20, this proceeding does not include disclaimed claims 1, 5, and 6.

³ We apply AIA 35 U.S.C. § 103 to the '254 patent because it was filed after, and never claimed the benefit of an effective filing date before, March 16, 2013. Ex. 1001, codes (22), (63); Pet. 6.

⁴ Petitioner styles this ground as also being based on “the knowledge of a POSITA [Person of Ordinary Skill In The Art].” However, an *inter*

II. DISCRETION UNDER 35 U.S.C. § 314(a)

Patent Owner argues that the Board should exercise its discretion to deny institution under 35 U.S.C. § 314(a) based on the factors set forth in *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 6 (PTAB Mar. 20, 2020) (precedential). Prelim. Resp. 29. We address each of these factors in turn. In assessing one of these factors (the sixth *Fintiv* factor), we address the strength of the merits of the Petition. *Infra* § III. We determine that these factors, taken as a whole, do not support exercising our discretion to deny the Petition.

Fintiv factor 1 asks whether the court has granted a stay, or evidence exists that one may be granted if a proceeding is instituted. *Fintiv*, Paper 11 at 6–7. Petitioner asserts that factor 1 is neutral. Pet. 10. Patent Owner contends that factor 1 favors denial because, although an opposed motion to stay has been filed in the parallel litigation, it is unlikely to be granted. Prelim. Resp. 31. However, subsequent to filing its Preliminary Response, Patent Owner notified the Board that the parallel court proceeding has been stayed pending the outcome of the *inter partes* review. Paper 13, 1. The granting of a stay pending *inter partes* review “has weighed strongly against exercising discretion to deny institution.” *Snap, Inc. v. SRK Technology LLC*, IPR2020-00820, Paper 15 at 9 (P.T.A.B. October 16, 2019) (precedential). The stay of the parallel proceeding results in factor 1 weighing strongly against exercising discretion to deny institution.

partes review may be requested “only on the basis of prior art consisting of patents or printed publications,” although it may “rely on evidence beyond prior art documents.” 35 U.S.C. § 311(b); *Qualcomm Inc. v. Apple, Inc.*, 24 F.4th 1367, 1374–75 (Fed. Cir. 2022) (stating that the “basis of a ground” must be “contained in a document that is a prior art patent or prior art printed publication.”). Patent Owner does not raise a § 311(b) challenge.

Fintiv factor 2 looks to the proximity of the court’s trial date to the Board’s projected statutory deadline to issue a final written decision. *Fintiv*, Paper 11 at 9. “If the court’s trial date is at or around the same time as the projected statutory deadline . . . the decision whether to institute will likely implicate other factors.” *Id.* Conversely, “[i]f the court’s trial date is earlier than the projected statutory deadline,” this has generally weighed “in favor of exercising authority to deny institution.” *Id.*

Patent Owner argues that this factor is neutral because trial in the parallel litigation (June 15, 2026) was set to begin less than one month after the projected statutory deadline for a Final Written Decision in this proceeding (on or around May 21, 2026). Prelim. Resp. 32–33. Petitioner asserts that this factor weighs strongly against exercising discretion to deny institution because IPR proceedings would be completed before the scheduled trial date and that on average, it takes 48.9 months to reach trial in the Northern District of California. Pet. 10. However, the parallel court litigation has been stayed pending the outcome of the *inter partes* review, providing weight under Factor 2 against exercising discretion to deny institution. *Snap, Inc.*, Paper 15 at 9. Based on these facts, we determine that factor 2 weighs against exercising discretion to deny institution.

Fintiv factor 3 looks to the investment in the parallel proceeding by the court and the parties at the time of institution. *Fintiv*, Paper 11 at 9. For example, “if at the time of the institution decision, the district court has issued substantive orders related to the patent at issue in the petition, this fact favors denial.” *Id.* at 9–10. Conversely, if “the district court has not issued orders related to the patent at issue in the petition, this fact weighs against exercising discretion to deny institution.” *Id.* at 10.

Patent Owner lists numerous efforts that the parties have already expended, including exchange and response to interrogatories and requests for production, source code discovery, and narrowing of infringement claims. Prelim. Resp. 33–34. Petitioner points only to those activities that were performed prior to the filing of the Petition. Pet. 10. Petitioner further asserts that expeditious filing of the Petition, approximately three months after being served with the relevant complaint, weighs strongly in favor of institution. *Id.* at 10–11.

The parties have expended a non-trivial level of effort in the district court proceeding, exchanging invalidity contentions and completing claim construction briefing. *See, e.g.*, Prelim. Resp. 33–34 (stating the parties have produced over 113,000 pages of documents, have conducted many weeks of code review, and have performed extensive analysis of infringement, validity, and damages issues related to narrowing the number of asserted claims to 70). Weighing against exercising discretion to deny institution is Petitioner’s filing of the Petition within three months of the complaint. *See Fintiv*, Paper 11 at 11–12; *Sotera*, Paper 12 at 17. Furthermore, *Fintiv* factor 3 is related to *Fintiv* factors 1 and 2, and because the “investment” factor is related to the “trial date” factor, the stay of the district court proceeding weighs against exercising discretion to deny institution. *See Fintiv*, Paper 11 at 10 (“This investment factor is related to the trial date factor, in that more work completed by the parties and court in the parallel proceeding tends to support the arguments that the parallel proceeding is more advanced, a stay may be less likely, and instituting would lead to duplicative costs.”). On balance, we discern that these facts weigh slightly against exercising discretion to deny institution.

Fintiv factor 4 looks to the overlap between issues raised in the petition and in the parallel proceeding. *Fintiv*, Paper 11 at 12.

In the Petition, Petitioner asserts that overlap is eliminated by its stipulation “that it will not advance in District Court on any ground asserted in this Petition.” Pet. 11 (citing *Sand Revolution v. Continental Intermodal Group - Trucking LLC*, IPR2019-01393, Paper 24 at 11–12 (PTAB June 16, 2020) (informative)). Patent Owner argues that such a stipulation “runs the risk of significant overlap both in consideration of the same evidence and arguments framed as ‘different grounds’ than the Petition.” Prelim. Resp. 35. Should the parallel court proceedings remain stayed pending the issuance of a final written decision in this *inter partes* review, Petitioner may not assert in the parallel proceeding that any claim challenged in the *inter partes* review is invalid on “any ground that the petitioner raised or reasonably could have raised during that inter partes review.” 35 U.S.C. § 315(e)(2). This potential estoppel further reduces, but does not eliminate, the risk of significant overlap between the assertions in the Petition and those that may be raised in the parallel litigation. This minimized risk of overlap alleviates concerns of inefficiency and the possibility of conflicting decisions. *Fintiv*, Paper 11 at 12. We determine that this factor weighs against exercising discretion to deny institution.

Fintiv factor 5 asks whether the Petitioner and the defendant in the parallel proceeding are the same party. *Fintiv*, Paper 11 at 13–14. Both parties confirm that this is the case. Pet. 11; Prelim. Resp. 36. In consideration of the fact that the parallel District Court proceeding is stayed, and that the potential 315(e)(2) estoppel reduces potential overlap between the invalidity contentions and the Petition challenges, we regard the consideration of the fifth *Fintiv* factor as neutral or, at most, weighing

slightly in favor of exercising discretion to deny institution. *Snap, Inc.*, Paper 15 at 16.

Fintiv factor 6 looks to whether other circumstances exist that impact the Board’s exercise of discretion, including the merits. *Fintiv*, Paper 11 at 14–15. For example, if the merits “seem particularly strong on the preliminary record, this fact has favored institution,” whereas “if the merits of the grounds raised in the petition are a closer call, then that fact has favored denying institution when other factors favoring denial are present.” *Id.*

The parties disagree on the strength of the merits of the Petition. Pet. 11–12; Prelim. Resp. 36–37. As detailed below, we determine that the Petitioner meets its burden for institution only for claims 3, 4, 9, 10, 18, and 20, and not for claims 2, 7, 8, 11–15, and 17. *Infra* § III. As noted, the merits are not particularly strong. *Id.*

We further consider the relative number of claims and grounds for which institution is supported, which is an additional circumstance to be considered when deciding whether to institute *inter partes* review. *See Chevron Oronite Co v. Infineum USA*, IPR2018-00923, Paper 9 at 10–11 (PTAB Nov. 7, 2018) (informative) (determining that instituting a trial with respect to twenty claims where a reasonable likelihood of prevailing was only shown with respect to two claims was “not an efficient use of the Board’s time and resources”); *Deeper, UAB v. Vexilar, Inc.*, IPR2018-01310, Paper 7 at 42–43 (PTAB Jan. 24, 2019) (informative) (determining that instituting a trial with respect to twenty-three claims where a reasonable likelihood of prevailing was only shown with respect to two claims was not an efficient use of the Board’s time and resources). Here, Petitioner’s case is sufficient against six claims and insufficient against nine claims within its

single ground of obviousness. Although the relative number of insufficiently addressed claims is not nearly as high as in *Chevron Oronite* or *Deeper*, and insufficient to deny institution on that basis alone, it is not minimal either.

Therefore, considering the strength of the merits and relative number of meritorious assertions and claims addressed by those meritorious assertions, factor 6 weighs in favor of discretionary denial.

We consider factors 1–6 and determine that together, they indicate that we should not apply our discretion to deny institution. Factor 1 (parallel litigation stayed) weighs strongly against exercising our discretion to deny institution. Factor 2 (stayed trial date for parallel proceeding close to Final Written Decision date) also weighs against exercising our discretion to deny institution. Factor 3 (some effort expended in the parallel proceeding, which is stayed, and Petition filed expeditiously) weighs slightly against exercising our discretion to deny institution. Factor 4 (potential of overlap minimized by stay) weighs against exercising our discretion to deny institution. Factor 5 (same parties) is neutral, or at most, weighs slightly in favor of exercising discretion to deny institution. Factor 6 (insufficient showing for nine of fifteen challenged claims) weighs towards exercising our discretion to deny institution. On these facts, we decline to exercise our discretion to deny institution.

III. ANALYSIS OF THE MERITS

A. *Legal Standards*

A claim is unpatentable under 35 U.S.C. § 103 if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious before the effective filing date

of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains.” 35 U.S.C. § 103; *see also KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of non-obviousness.⁵ *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

Petitioner asserts that a person of ordinary skill in the art (“POSITA”) at the critical time “would have had a bachelor of science degree in electrical engineering or a similar discipline, along with 2–3 years of professional experience working with (e.g., researching, designing, or teaching) monolithic 3D structures and NAND flash memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience).” Pet. 25 (citing Ex. 1003 ¶¶ 34–38). Petitioner further asserts that a POSITA “would have been aware of and generally knowledgeable about 3D NAND’s structure, how it is manufactured, and its component parts.” *Id.* Patent Owner does not provide any such assessment in its Preliminary Response. Prelim. Resp. 8. For purposes of this Decision, we adopt Petitioner’s proposed level of ordinary skill, as it appears to be consistent with the specification of the ’254 patent and the prior art of record.

⁵ Neither party presents evidence or arguments regarding objective evidence of non-obviousness. Pet. 66; Prelim. Resp.

C. Claim Construction

Neither party proposes any express claim construction. Pet. 35 (stating claims should receive their “plain and ordinary meaning”); Prelim. Resp. 8 (stating that Petitioner’s challenges fail “under any reasonable construction”). In an *inter partes* review, we construe a patent claim “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. [§] 282(b).” 37 C.F.R. § 42.100(b). Under this standard, the words of a claim generally are given their “ordinary and customary meaning,” which is the meaning the term would have to a person of ordinary skill at the time of the invention, in the context of the entire patent including the specification. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc).

We determine no terms require express construction for purposes of this Decision.

D. Obviousness over Nakajima

Petitioner asserts that claims 2–4, 7–15, 17, 18, and 20 are unpatentable under 35 U.S.C. § 103 as obvious over Nakajima in view of the knowledge of a person of ordinary skill in the art. Pet. 28–66. Patent Owner argues against this assertion. Prelim. Resp. 9–30.

1. Nakajima

Nakajima is titled “Semiconductor Device and Method of Manufacturing the Same.” Ex. 1005, code (54). Nakajima relates to a semiconductor device that includes a substrate, an interconnect layer, a layer stack, and a first silicon nitride layer. *Id.* at code (57).

2. Claims 2, 11–15, and 17

We begin our analysis of Petitioner’s obviousness contentions with Petitioner’s assertions as to claim 2, which depends from disclaimed claim 1.

With respect to the limitations of claim 1, incorporated into claim 2 through its dependency thereon, Petitioner points to teachings of Nakajima. Pet. 28–38.

Petitioner asserts that claim 2, which recites “prior to forming the first opening, forming a dummy channel structure extending vertically through the stack,” is taught by Nakajima in view of the knowledge of the prior art. Pet. 38–41. Petitioner asserts that Nakajima discloses forming a channel structure extending vertically through the stack prior to forming the first opening, but not that any of such channels are dummy channels. *See* Pet. 32 (citing Ex. 1005, 8:24–33), 39; Ex. 1003 ¶ 86; Prelim. Resp. 9.

Instead, Petitioner asserts that in view of the knowledge of a person having ordinary skill in the art, “it would have been obvious to implement some of Nakajima’s channels as dummy channels.” Pet. 39 (citing Ex. 1003 ¶ 104). Petitioner points to three references, Kai,⁶ Park,⁷ and Kim,⁸ for teaching active and dummy channels for providing physical support. *Id.* Petitioner asserts that such support is necessary for performing the gate replacement process of Nakajima. *Id.* at 40 (citing Ex. 1018 (U.S. Pat. 8,945,996 B2)), 29–30 (citing Nakajima’s Figures 2, 7 as showing gate replacement), 32 (stating, “Nakajima describes that the channel pillars support the structure during the gate replacement process”)).

Patent Owner argues that Petitioner does not provide a sufficient reason to modify Nakajima to convert some of its channels to dummy channels. Prelim. Resp. 10–11. Patent Owner argues that a “POSITA would not be motivated to modify Nakajima as proposed because the

⁶ U.S. Patent 10,290,643 B1 (Ex. 1015).

⁷ U.S. Patent 9,859,297 B2 (Ex. 1016).

⁸ U.S. Pat. Publ. 2018/0308559 A1 (Ex. 1017).

modification provides no benefits, decreases the memory's storage capacity, and adds complexity to the manufacturing process.” *Id.* at 11.

Petitioner provides multiple reasons why a person having ordinary skill in the art would have been motivated to employ dummy channels, which we address in light of Patent Owner's arguments. Pet. 40–41; Prelim. Resp. 12–17.

Petitioner asserts that dummy channels would provide additional support and be made at the same time and by the same process as the active channels, except that dummy channels typically will not include interconnects to upper elements. Pet. 40 (citing Ex. 1015 (Kai), 10:20–27; Ex. 1003 ¶ 108). Patent Owner argues that additional process steps would be needed to fill selected channels with dielectric instead of semiconductor layers. Prelim. Resp. 12 (citing Ex. 2007 ¶ 35). Patent Owner further argues that removing some interconnects in Nakajima to form dummy channels would reduce storage capacity by removing active channels. *Id.* (citing Ex. 2007 ¶ 34). Patent Owner further asserts that Petitioner admits that Nakajima's active channels already provide support, and has not shown that changing some to dummy channels would provide any additional support. *Id.* (citing Ex. 2007 ¶ 35)

We agree with Patent Owner that no advantage is clearly shown by replacing some of Nakajima's active channels with dummy channels. Although Petitioner asserts that adding dummy channels would provide additional support, Petitioner's combination does not add new channels, but instead, “implement[s] some of Nakajima's channels as dummy channels.” Pet. 39. Because Petitioner admits that Nakajima's active channels provide support, and has not asserted that dummy channels are more supportive than active channels, the record does not support Petitioner's assertion that

replacing Nakajima's active channels with dummy channels would provide additional structural support. *See* Pet. 32 ("Nakajima describes that the channel pillars support the structure during the gate replacement process"); Ex. 1005, 8:24–29 (Nakajima's "pillar structures CL" support insulation layers 72). Thus, even if no additional process steps would be needed to form dummy channels (upon which the parties and their declarants differ), the record indicates that no structural advantage would be gained, and the memory storage capability would instead be reduced. To the extent that Petitioner's replacement or addition of dummy structures would result in additional structural support, Petitioner has not explained how any tradeoffs with reduced memory capability or additional processing would be viewed as desirable by a person having ordinary skill in the art. Consequently, the record does not support Petitioner's reason to combine dummy channels as known in the art with the teachings of Nakajima.

Nor are we persuaded by Petitioner's remaining assertions that dummy channels would reduce the likelihood of defective bits on the edge of the memory cell region and increase the uniformity of the feature pattern and thereby reduce processing issues. Pet. 40–41. Patent Owner argues that there is no teaching that additional rows of dummy structures on the edge of the memory cell region would extend the memory cell pattern in any of the documents presented by Petitioner as reflecting the knowledge of the prior art. Prelim. Resp. 17–18. Patent Owner further argues that Nakajima uses through-array contacts in its staircase region that provide structural support without the use of dummy structures, thereby negating any need for dummy channels to be added to prevent abnormalities due to insufficient support. *Id.* at 18 n.3 (citing Ex. 2007 ¶ 42).

We agree with Patent Owner that Petitioner insufficiently supports these assertions. Petitioner does not explain how the additional dummy structures would be placed at “the edge of the memory cell region” to extend the memory cell pattern in such a manner as to “result in an overall more uniform feature pattern.” Pet. 40–41 (citing Ex. 1003 ¶¶ 102–103; Ex. 1020, 8:47–53; Ex. 1021, 2:20–43). At best, Petitioner shows that “it is common to refrain from using the cells at the array edge,” which are “sometimes referred to as dummy cells,” due to “processing variations.” Ex. 1020, 8:47–53.⁹ Nor does Petitioner show that such placement is known in the prior art such that it would be implemented in Nakajima without further explanation. Dr. Lee notes that such a dummy region at the edge of the array is “later sacrificed in processing,” which would undercut Petitioner’s other rationale that such dummy channels would provide additional support. Ex. 1003 ¶ 102 (citing Ex. 1021, 2:20–43). Petitioner’s reasons for edge placement of additional dummy “cells” or a dummy “region” thereby differ from its reasons for replacement of Nakajima’s active channels with dummy channels, and would appear to be separate combinations resulting in distinct structures with potentially opposing advantages.

Petitioner’s showing is also undercut by its reliance solely on the knowledge of a person having ordinary skill in the art for teaching dummy channels. Patent Owner argues that such reliance is improper to teach a limitation missing from the supplied prior art unless “the missing limitation in question [is] *unusually simple* and the technology *particularly*

⁹ Petitioner’s reference to Ex. 1022, which discusses advantages of quadrupole illumination for photolithography, lacks an explanation of its connection to the channels at issue in the claimed invention, and therefore does not meaningfully support Petitioner’s obviousness assertion. Pet. 41.

straightforward.” Prelim. Resp. 9–10 (citing *Motorola Mobility LLC v. Largan Precision Co.*, IPR2024-00688, Paper 7 at 29 (PTAB Oct. 28, 2024); *DSS Tech. Mgmt. v. Apple*, 885 F.3d 1367, 1374 (Fed. Cir. 2018)). Patent Owner points to “complex semiconductor manufacturing processes” involved in forming a dummy channel, including “wet etching, and/or dry etching, such as DRIE,” and “thin film deposition processes, such as ALD, CVD, PVD.” *Id.* at 10 (citing Ex. 2007 ¶ 32; Ex. 1001, 12:7–23). Patent Owner adds that additional process steps, not addressed by Kai, Kim, or Park, would be needed to “change [Nakajima’s] functional channels within a memory array into dummy channels.” Prelim. Resp. 13. We agree with Patent Owner that the lack of record support for Petitioner’s reliance on the knowledge of a person having ordinary skill in the art undermines Petitioner’s obviousness showing.

We determine that Petitioner has not shown a reasonable likelihood of success of proving its obviousness assertions for claim 2 because of insufficiently explained and inadequately supported reasons to combine the knowledge in the art with Nakajima to teach or suggest claim 2’s “dummy channel” limitation. The deficiencies in Petitioner’s showing extend to claim 11, which recites a “dummy channel” limitation, and its dependent claims 12–15 and 17. Ex. 1001, 21:35–22:19, 22:22–26. Consequently, Petitioner has not shown it is likely to succeed on its obviousness challenges to claims 2, 11–15, and 17.

3. *Claims 3, 4, 9, 10, 18, and 20*

We turn to Petitioner’s assertions as to claim 3, which depends from claim 1. Claim 3 further recites, “wherein forming the first opening comprises simultaneously etching the first opening through the stack and a

second opening outside of the stack.” With respect to the limitations of claim 1, incorporated into its dependent claim 3, Petitioner points to teachings of Nakajima. Pet. 41–43. Petitioner asserts that Nakajima teaches forming holes through its stack for its TAVs (C4), and that one C4 structure is outside of the stack. *Id.* at 41. Petitioner asserts that Nakajima would be understood as forming both holes simultaneously because Nakajima discloses only one set of steps for creating the H1 holes and one set of steps for forming the C4 contacts. *Id.* at 42 (citing Ex. 1005, 7:37–43, 5:8–11).

Patent Owner argues that Nakajima teaches that all H1 holes for the C4 structures are etched through the stack, not outside the stack, at the time of etching. Prelim. Resp. 19–20 (citing Ex. 2007 ¶¶ 46–48; Ex. 1005, 7:37–39, 7:41–43, 7:28–31). Patent Owner argues that the hole for the C4 structure outside the stack in Nakajima’s Figure 2 may result from removal of portions of the stack after holes are etched through the stack. *Id.* at 21. Consequently, although Figure 2 shows holes both in and outside the stack, both holes may have been simultaneously etched while both were inside the stack, contrary to the requirements of claim 3. *Id.* at 21–22. (citing Ex. 2007 ¶ 48; Ex. 1005, 7:37–39, 7:41–43).

We agree with Patent Owner that Petitioner has not shown that Nakajima’s disclosure of a single step of creating H1 holes would be understood as resulting from simultaneous etching of a hole through the stack and a hole outside the stack. Petitioner requires us to assume that the step of etching H1 holes is performed when the structure has both stack and non-stack areas for hole etching; i.e., when the structure appears as in Figure 2 of Nakajima. Pet. 41–42, 28 (stack comprised of dielectric/sacrificial layers on a substrate). However, Patent Owner provides an alternative process in which all holes are simultaneously etched in a stack, and the non-

stack areas are later created. In such an alternative, holes would be present in non-stack areas (through later removal of stack portions), but would not be etched in a non-stack area (having no dielectric sacrificial layers) at the same time as holes would be etched in a stack area. Petitioner points to Nakajima's description that hole H1 is formed in "the layer stack 120"; i.e., not outside the stack. Prelim. Resp. 19 (citing Ex 1005, 7:37–39, 7:41–43). We determine that Petitioner does not demonstrate that a person having ordinary skill in the art would understand that Nakajima creates holes resulting from simultaneous etching of a hole through the stack and a hole outside the stack. Consequently, Petitioner does not show that Nakajima describes simultaneous etching of a hole through the stack and a hole outside the stack.

Alternately, Petitioner asserts that it would have been obvious to form both holes simultaneously to reduce processing time in a routine and highly predictable manner. Pet. 42 (citing Ex. 1003 ¶ 113; Ex. 1023 (U.S. Pat. Publ. 2019/0081061) ¶ 37; Ex. 1010 (U.S. Patent 10,354,980 B1), Fig. 5, 10:31–58).

Patent Owner argues that use of a single set of processing steps to create holes is more consistent with forming all holes in the stack first and etching the stack later. Prelim. Resp. 22 (citing Ex. 2007 ¶¶ 49–50). Patent Owner argues that simultaneously etching interior and exterior holes would result in the C4 structure having different depths, contrary to Nakajima's Figure 2. *Id.* (citing Ex. 2007 ¶ 50; Ex. 1005, 7:37–39, 7:41–43)). Patent Owner further argues that the missing "simultaneously" limitation is neither unusually simple nor involves particularly straightforward technology such that the general knowledge of the prior art can supply a missing limitation. Prelim. Resp. 24–25 (noting that neither of the references cited in support of

simultaneous etching relate to holes both inside and outside of the stack) (citing Ex. 2007 ¶¶ 51–52).

Petitioner shows significant support for its assertions. For example, Dr. Lee states that Nakajima describes simultaneous etching of other stack and non-stack components. Ex. 1003 ¶ 114 (citing Ex. 1005, 17:33–45). Dr. Lee states that “it was the norm to form all instances of a contact type at the same time.” *Id.* ¶ 112. Dr. Lee further points to evidence in the art of simultaneous etching of dummy and via openings through different numbers of layers of the stack, and of simultaneous etching of various vertical channels in various portions of a memory device. *Id.* ¶¶ 114–115. Such evidence tends to contradict Dr. Campbell’s testimony that simultaneous etching could not be performed due to different resulting etch depths. Ex. 2007 ¶ 50. Although Dr. Campbell raises questions as to whether the cited art would be understood as disclosing simultaneous etching through the stack and outside the stack, Dr. Lee’s uncontested advantage of reducing processing time by simultaneous etching supports Petitioner’s reason to alter Nakajima.

Consequently, Petitioner has shown a reason to combine that is sufficient for institution on claim 3. We invite the parties to address, at trial, whether the prior art shows that simultaneous etching of stack and non-stack areas would be unusually simple and particularly straightforward such that Petitioner’s reliance on the general knowledge in the art is warranted.

Claims 4, 9, 10, 18, and 20 each contain a limitation requiring simultaneous etching of openings through and outside of the stack, and are not argued separately from claim 3. Ex. 1001, 20:56–59, 21:17–34, 22:27–49; 22:52–54; Prelim. Resp. 18–19. We have reviewed Petitioner’s remaining assertions for claims 3, 4, 9, 10, 18, and 20, and determine that

Petitioner has shown a reasonable likelihood that these claims would have been obvious over the prior art.

4. *Claims 7, 8, 14, and 15*

We turn to Petitioner's assertions as to claim 7, which depends from claim 1. With respect to the limitations of claim 1, incorporated into claim 7 through its dependency thereon, Petitioner points to teachings of Nakajima. Pet. 49–53. Claim 7 further recites,

wherein forming the spacer on the sidewall of the first opening comprises:

forming a plurality of shallow recesses by removing parts of the sacrificial layers abutting the sidewall of the first opening;

depositing a dielectric layer filling in the shallow recesses and on the sidewall and a bottom surface of the first opening; and

removing part of the dielectric layer that is deposited on the bottom surface of the first opening.

Ex. 1001, 21:4–13 (emphasis added). Patent Owner disputes Nakajima's teaching of the recited "shallow recesses." Prelim. Resp. 25–30.

Petitioner asserts that Nakajima teaches such shallow recesses either (1) inherently, as a result of typical prior art etches, or (2) obviously in view of a person of ordinary skill's knowledge that an option for a through-array channel is to have a ribbed shape with recesses in one of the stack layers. Pet. 49–52.

a) *Recesses resulting from hole etching*

Petitioner asserts that typical prior art etches for creating holes in a stack "were also known to result in lateral recesses in either the dielectric spacers or sacrificial layers." Pet. 50 (citing Ex. 1030 (U.S. Pat. 11,075,084)). Petitioner asserts that shallow recesses are formed unintentionally during etching because "it is a challenge to find an etch gas .

. . in terms of getting a smooth sidewall of high aspect ratio holes in 3D NAND memory.” *Id.* at 49–50 (citing Ex. 1030, 2:59–67).

Patent Owner argues that Petitioner’s evidence does not support its conclusion. Prelim. Resp. 27. Patent Owner argues that a POSITA would have understood that finding an etching gas without selectivity (to achieve a smooth sidewall) was a challenge, “[b]ut that does not mean POSITAs would therefore be motivated to use gases with selectivity that would result in unintentional recesses.” *Id.* We agree with Patent Owner that because Petitioner’s evidence indicates that a smooth sidewall can be obtained with the proper etch gas, Petitioner has not shown that a non-smooth sidewall would have been understood by a person having ordinary skill in the art as the result of etching in Nakajima.

b) Recesses from formation of ribbed cavity

Petitioner additionally asserts that it was known in the art to create large recesses in conductor layers to form a ribbed via cavity. Pet. 50–51 (citing Ex. 1031 (“Cui”), Fig. 16A, 26:23–33). Petitioner further asserts that such a ribbed via cavity is advantageous because it creates additional area for the dielectric material. *Id.* at 51 (citing Ex. 1003 ¶ 129). Petitioner further asserts that such rib regions are known to be formed in either the conductive layer or the sacrificial gates, each providing the same benefit. *Id.* at 51–52 (citing Ex. 1015 (“Kai”), 11:9–34, Ex. 1003 ¶ 130).

Patent Owner first argues against Petitioner’s reliance on common knowledge to supply the missing “shallow recesses” claim limitation where Petitioner has not shown that the limitation is “unusually simple” or the “technology particularly straightforward.” Prelim. Resp. 27–28. Patent Owner argues that forming shallow recesses is a highly technical and complex process dependent on the lateral dimension of the shallow recess

and the etching rate and/or etching time. *Id.* (citing Ex. 2007 ¶ 58).

However, we credit Dr. Lee’s uncontested testimony that such shallow recesses may result from using certain etchants, as discussed *supra*.

Although we agree with Patent Owner that such recesses may be considered undesirable, that they may result from etch gas selection tends to show they are unusually simple and result from particularly straightforward etch technology. We have determined that one having ordinary skill in the art would be “generally knowledgeable about 3D NAND’s structure[and] how it is manufactured.” *Supra* § III(B). Therefore, we disagree with Patent Owner that Petitioner may not rely on the general knowledge in the art to teach “shallow recesses.” However, to show that shallow recesses would have been obvious to form in a memory device as taught by Nakajima, Petitioner must still show that a person having ordinary skill in the art would have had reason to do so.

Patent Owner argues that Petitioner’s citation to Cui to show the well-known nature of shallow recesses fails to show the obviousness of shallow recesses because Cui creates “*large recesses*,” not shallow recesses. Prelim. Resp. 28–29 (citing Pet. 51; Ex. 1031, Fig. 16A, 26:23–33). Further, Patent Owner argues that Cui creates recesses by removing portions of the insulating layers, not, as claimed, by removing portions of the sacrificial layers. *Id.* at 29 (citing Ex. 1031, 26:23–25). Patent Owner points out that Cui does not create recesses in the sacrificial layer. *Id.* (citing Ex. 1031, Fig. 16A). Patent Owner argues that to the extent that Kai teaches creating recesses in sacrificial gates, Petitioner has not shown that a person having ordinary skill in the art would implement such recesses as shallow recesses in Nakajima by removing parts of Nakajima’s sacrificial layers. *Id.* at 30 (citing Ex. 1015 (“Kai”)).

We agree with Patent Owner that Petitioner’s asserted combination would result in “large recesses,” not the claimed shallow recesses. We note that Kai, in the portion cited by Petitioner, teaches forming lateral recesses in the sidewalls of sacrificial material layers 42, in which the lateral recess distance is in a range from 20 nm to 120 nm. Ex. 1015, Fig. 5C, 11:9–34. However, Petitioner does not assert that such ranges are part of its combination, that they result in “shallow” recesses per claim 7, or that they would result in the “rib regions” that Petitioner asserts to be the advantage exhibited by Cui’s large recesses.

Patent Owner further argues that Petitioner has not shown sufficient motivation for a person having ordinary skill in the art to remove sacrificial material to form shallow recesses in Nakajima. Prelim. Resp. 30. Patent Owner argues that the provided motivation, because it “serves the same purpose as the ’254 Patent,” is purely derived from hindsight. *Id.* (citing Pet. 51).

We agree with Patent Owner. Petitioner merely states that such recesses “create[] additional area for the dielectric material.” Pet. 51 (citing Ex. 1003 ¶ 129). Neither Petitioner nor Dr. Lee explain why this additional area is advantageous, only that it creates a longer spacer, which is the same purpose of the lateral recesses in the ’254 patent. Ex. 1003 ¶¶ 129–130. Thus, Petitioner presents no particular advantage to the combination except through reference to the ’254 patent. But a reason to combine should not be obtained solely from the challenged patent. *KSR*, 550 U.S. at 421 (“A factfinder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon ex post reasoning.”); *Metalcraft of Mayville, Inc. v. Toro Co.*, 848 F.3d 1358, 1367 (Fed. Cir. 2017) (“[W]e cannot allow hindsight bias to be the thread that stitches

together prior art patches into something that is the claimed invention.”). Petitioner’s improper reliance on the ’254 patent for a reason to alter Nakajima’s teachings is undermined by its admission that the ’254 patent “provides virtually no explanation on creating these known rib regions.” Pet. 52.

Consequently, Petitioner has not shown a reasonable likelihood that it would prevail on its obviousness assertions for claim 7 because it has not presented a satisfactory reason to combine the teachings of Nakajima with the knowledge of person of ordinary skill in the art. Petitioner’s assertions as to claims 8, 14, and 15 rely on the same assertions as for claim 7, and are likewise insufficient. Thus, Petitioner has not shown a reasonable likelihood that it would prevail on its obviousness assertions for claims 7, 8, 14, and 15.

IV. CONCLUSION

Based on the arguments in the Petition and the Preliminary Response, and the evidence of record, we determine that Petitioner establishes a reasonable likelihood that it will prevail on its challenge to at least one claim of the ’254 patent. We also determine that the arguments and evidence of record do not support discretionary denial of the Petition under 35 U.S.C. § 314(a). Our determination at this stage of the proceeding is based on the evidentiary record currently before us. This decision to institute trial is not a final decision as to patentability of any claim for which an *inter partes* review has been instituted. Our final decision will be based on the full record developed during trial.

Accordingly, we institute an *inter partes* review of all the challenged, non-disclaimed claims on all the challenged grounds; i.e.:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
2–4, 7–15, 17, 18, 20	103	Nakajima

V. ORDER

For the foregoing reasons, it is:

ORDERED that an *inter partes* review is instituted with respect to all of the grounds asserted in the Petition with respect to the non-disclaimed challenged claims; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which shall commence on the entry date of this Decision.

IPR2025-00034
Patent 10,879,254 B2

For PETITIONER:

Jeremy Jason Lang
Thomas James
Jared Bobrow
ORRICK, HERRINGTON & SUTCLIFFE LLP
jlang@orrick.com
tjames@orrick.com
jbobrow@orrick.com

For PATENT OWNER:

Inge A. Osman
Brenda L. Danek
Steven W. Peters
Amit Makker
LATHAM & WATKINS LLP
inge.osman@lw.com
brenda.danek@lw.com
steven.peters@lw.com
amit.makker@lw.com