

SEMICONDUCTOR ENGINEERING

Select Language

f

t

in

Home > Test, Measurement & Analytics > 3D NAND Metrology Challenges Growing

TEST, MEASUREMENT & ANALYTICS

3D NAND Metrology Challenges Growing

f

Rising costs and gaps in equipment emerge as technology scales; new tools under development.

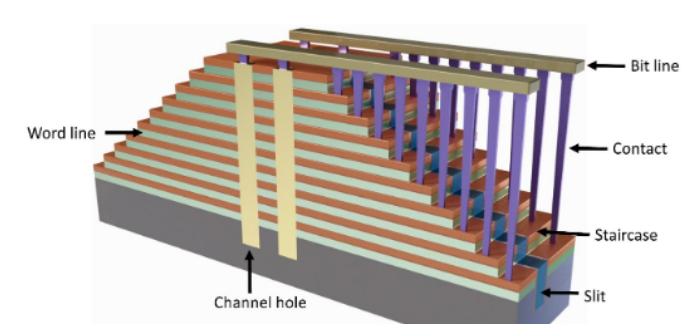
APRIL 9TH, 2019 - BY: MARK LAPEDUS

3D NAND vendors face several challenges to scale their devices to the next level, but one manufacturing technology stands out as much more difficult at each turn—metrology.

[Metrology](#), the art of measuring and characterizing structures, is used to pinpoint problems and ensure yields for all chip types. In the case of 3D NAND, the metrology tools are becoming more expensive at each iteration and the gaps are growing. Metrology is different than inspection, which inspects and finds defects in chips. Many chips require both optical and e-beam inspection systems.

This is not so clear-cut for metrology in 3D NAND. It's relatively straightforward to measure today's planar NAND, which is more or less a two-dimensional structure. [3D NAND](#), the successor to planar NAND, is a different story. Unlike planar NAND, 3D NAND resembles a three-dimensional vertical skyscraper in which horizontal layers of memory cells are stacked and then connected using tiny vertical channels. Both planar and 3D NAND are used for storage applications, such as smartphones and solid-state storage drives (SSDs).

3D NAND is quantified by the number of layers stacked in a device. As more layers are added, the bit density increases. Today, 3D NAND suppliers are ramping up 96-layer devices, while 128-layer products are in R&D. Vendors also are working on chips with 500 or more layers.



TECHNICAL PAPERS

Machine Learning Based Prediction: Health Behavior On BP

OCTOBER 12, 2018 BY TECHNICAL PAPER LINK

Autonomous Vehicle Navigation In Rural Environments Without Detailed Prior Maps (MIT)

MAY 15, 2018 BY TECHNICAL PAPER LINK

Silicon CMOS Architecture For A Spin-Based Quantum Computer

JANUARY 24, 2018 BY TECHNICAL PAPER LINK

Making High-Capacity Data Caches More Efficient

OCTOBER 24, 2017 BY TECHNICAL PAPER LINK

How Neural Networks Think (MIT)

OCTOBER 18, 2017 BY TECHNICAL PAPER LINK

Knowledge Centers

Entities, people and technologies explored

LEARN MORE

RELATED ARTICLES

Fundamental Shifts In 2018

This will go down as a good year for the semiconductor industry, where new markets and innovation were both necessary and rewarded.

BY BRIAN BAILEY

In-Memory Computing Challenges Come Into Focus

Researchers digging into ways

Overall site

Search

SPONSORS

KLA

ADVANTEST

NATIONAL INSTRUMENTS

DELTA

OPTIMAL+

PDF/SOLUTIONS

Mentor

A Siemens Business

NEWSLETTER SIGNUP

Email:

Interests:

☐ System-Level Design

☐ Low Power-High Performance

☐ Manufacturing, Packaging & Materials

☐ Test, Measurement & Analytics

☐ IoT, Security & Automotive

Subscribe

POPULAR TAGS

2.5D

3D-IC

7NM

10NM

AI

ANSYS

APPLE

APPLIED MATERIALS

ARM

ARTERIS

ATRENTA

AUTOMOTIVE

BUSINESS

CADENCE

EDA

EMULATION

ESILICON

EUV

FINFETS

GLOBALFOUNDRIES

IBM

IMEC

INTEL

IOT

IP

LAM RESEARCH

MACHINE LEARNING

MEMORY

MENTOR

MENTOR GRAPHICS

MIT

MOORE'S LAW

NVIDIA

NXP

QUALCOMM

RAMBUS

SAMSUNG

SECURITY

SEMI

SIEMENS

SOFTWARE

SONICS

SYNOPSYS

TSMC

VERIFICATION

RECENT COMMENTS

■ Brian Bailey on Target: 50% Reduction In Memory Power

■ 10957 reader on Single Vs. Multi-Patterning EUV

YMTC
Exhibit 2011
Micron v. YMTC
IPR2025-00034
Ex. 2011-001

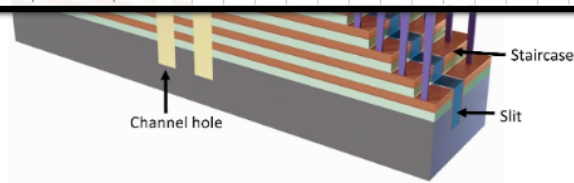


Figure 1: 3D NAND structure showing high-aspect ratio (HAR) features such as the channel hole. Source: KLA

With that in mind, 3D NAND presents some challenges for the metrology equipment in the fab. "While metrology is required for process control of planar NAND structures, the measurements are not as difficult relative to the challenges faced with high-aspect ratio 3D NAND," said Scott Hoover, principal yield consultant with [KLA](#). "The change from 2D to 3D integration introduces new metrology challenges, including very high-aspect ratio structures, wafer stress driven bow and vertical gate dimension control."

The big challenge is to characterize the inner portions of a 3D NAND device, which consists of complex materials, multiple layers and tiny channel holes. Then, as you add more layers, the metrology challenges increase "due to a higher number of 3D gate stacks and multi NAND string stacks," said Jeongdong Choe, an analyst at TechInsights.

All told, metrology is becoming more challenging and expensive in 3D NAND scaling. Compounding the challenges is that no single metrology system can handle all requirements. 3D NAND requires an assortment of metrology tool types, such as electron microscopes, optical systems and X-ray. Even then, there are some metrology gaps.

2D to 3D NAND

The NAND market is undergoing a turbulent period. In 2018, the market fell into an oversupply mode, while product prices tumbled throughout the year.

The NAND downturn has extended into 2019 amid weak server and smartphone demand. For a 128Gbit device, contract prices fell 10.8% in the first quarter of 2019, compared to the previous period, according to KeyBanc. In the first quarter, prices were down 56% year-over-year.

On the bright side, the downward pressure on NAND prices allows OEMs to sell high-density SSDs at lower prices. "NAND-based SSDs originally were targeted for more of the high end," said Gill Lee, managing director of memory technology at [Applied Materials](#). "Now it's a big part of notebook computers. SSDs also are targeting even the low-end of storage. So the market for NAND is not only going up, it's also covering a big part of the hard disk-drive market."

NAND has been undergoing a challenging technology transition. Planar NAND was the mainstream technology for years, and today vendors are selling planar NAND at the 15nm/14nm regime. But that's where it runs out of steam. To continue increasing density, the industry is moving to 3D NAND, which stacks the memory cells in the vertical direction. The latest 3D NAND devices have 96 layers. Intel, Micron, Samsung, SK Hynix and the Toshiba-Western Digital duo are working on 3D NAND with 128 layers and above.

In-Memory Computing Challenges Come Into Focus

Researchers digging into ways around the von Neumann bottleneck.

BY KATHERINE DERBYSHIRE

Engineering Talent Shortage Now Top Risk Factor

New market opportunities and global competitiveness are limited by qualified people.

BY MARK LAPEDUS

Making Chip Packaging Simpler

The promise of advanced packaging is being able to integrate heterogeneous chips, but a lot of work is needed to make that happen.

BY ED SPERLING AND MARK LAPEDUS

Finding Defects In Chips With Machine Learning

Better algorithms and more data could bolster adoption, particularly at advanced nodes.

BY MARK LAPEDUS

China's Foundry Biz Takes Big Leap Forward

30 facilities planned, including 10/7nm processes, but trade war and economic factors could slow progress.

BY MARK LAPEDUS

What's The Right Path For Scaling?

New architectures, packaging approaches gain ground as costs increase, but shrinking features continues to play a role.

BY MARK LAPEDUS

Mostly Upbeat Outlook For Chips

2019 will be a year of change for the semiconductor industry as new fields drive technological advancements.

BY BRIAN BAILEY

- Brian Bailey on Target: 50% Reduction In Memory Power
- 10957 reader on Single Vs. Multi-Patterning EUV
- C. Hodson on Target: 50% Reduction In Memory Power
- Gil Russell on 3D NAND Metrology Challenges Growing
- neil on Target: 50% Reduction In Memory Power
- Computational Storage Dude on In-Memory Computing Challenges Come Into Focus
- Mark LaPeduc on 3D NAND Metrology Challenges Growing
- Peter manoj on 3D NAND Metrology Challenges Growing
- David Stoddard on Silicon CMOS Architecture For A Spin-based Quantum Computer
- Jacob Monberg on Making high-capacity data caches more efficient
- John Evans on The 7nm Pileup
- Nick T on Mathematic Model Helps Predict Markets That Will Drive Semiconductor Growth
- Enchuan on Single Vs. Multi-Patterning EUV
- Suresh Kumar K Regonda on Finding Defects In Chips With Machine Learning
- Chandra on Machine Learning Meets IC Design
- Sally, displaced and re-engineered self on Engineering Talent Shortage Now Top Risk Factor
- Subodh Taigor on The Case For Antifuse OTP NVM For Secure & Reliable SoCs
- Wolfgang Roethig on IC Test: Doing It At The Right Place At The Right Time
- Katherine Derbyshire on EUV Arrives, But More Issues Ahead
- K. Goldberg on EUV Arrives, But More Issues Ahead
- jeffl on Making Chip Packaging Simpler
- Tejinder Singh on EUV Arrives, But More Issues Ahead
- Guest on EUV Arrives, But More Issues Ahead
- Riko R on A Different Kind Of Material World
- semi probes on The Mighty Sensor In The Fab
- Tony on Engineering Talent Shortage Now Top Risk Factor
- Pete Clarke on The Growing Challenge Of Thermal Guard-Banding
- ..

3D NAND devices have 96 layers. Intel, Micron, Samsung, SK Hynix and the Toshiba-Western Digital duo are working on 3D NAND with 128 layers and above.

Vendors are taking different approaches here. In a 96-layer device, some are stacking all 96 layers in the same die. Others are stacking two 48-layer devices or decks on top of each other. This is called string or tier stacking.

Making 3D NAND is different from planar NAND. In 2D NAND, the idea is to shrink the cell size using 193nm lithography and multiple patterning. Lithography is still used for 3D NAND, but it isn't the most critical step. For 3D NAND, the idea is to go vertical, and so the challenges shift from lithography to deposition and etch.

Metrology challenges

The metrology challenges are also different. In planar NAND, vendors take top-down images and other measurements of the device, which locates the defects and other issues. In 3D NAND, the films, layers and channels reside inside the device. The defects also are buried in the structure.

Many metrology tools can't penetrate the structure and look inside the device. X-ray tools can penetrate the structure, but they are only used in select apps. So, metrology is more difficult for 3D NAND. Yet, the industry uses the same metrology tool types for both planar NAND and 3D NAND. These include CD-SEMs, optical CD (OCD) tools, overlay systems, TEMs and X-ray.

A [critical-dimension scanning electron microscope](#) (CD-SEM) takes top-down images of a structure. Meanwhile, a transmission electron microscope (TEM) transmits a beam through a structure to measure a sample. X-ray metrology involves different tool types.

One OCD tool type is called an ellipsometer. Used in the industry for years, the ellipsometer utilizes polarized light to characterize structures.

Meanwhile, making 3D NAND is a complex process. First, using a deposition tool, a system deposits a layer of material on a substrate, followed by another layer on top. The process is repeated several times until a device has the desired number of layers.

The stack requires thin-film measurements to ensure it meets spec. For this, vendors use an ellipsometer and/or a reflectometer to make thin-film measurements. Reflectometry uses light to measure films. The decision to use an ellipsometer or a reflectometer depends on the material types.

Ellipsometry is a non-destructive technique that doesn't measure the actual device or film. Instead, it uses a model-based approach to characterize structures. An ellipsometer system consists of a light source, polarization generator, analyzer and detector. In operation, light is transmitted through a polarizer, which then hits a sample in two planes at an angle.

Then, the reflected light enters into an analyzer, which is converted into a signal. From there, the data is crunched in a system, which provides thin-film measurements.

- Tony on Engineering Talent Shortage Now Top Risk Factor
- Pete Clarke on The Growing Challenge Of Thermal Guard-Banding
- Henry on More Lithography/Mask Challenges (part 1)
- Scott Jewler on Finding Defects In Chips With Machine Learning
- Mark LaPedus on Finding Defects In Chips With Machine Learning
- Carl Zweben on Shedding Pounds In Automotive Electronics
- John Eastwood on Making Autonomous Vehicles Safer
- Scott Jewler on Finding Defects In Chips With Machine Learning
- Navathej on Power Aware Intent And Structural Verification Of Low-Power Designs
- Guest on Defect Detection Strategies and Process Partitioning for SE EUV Patterning
- David J Leary on Chip Aging Accelerates
- nikilla on CMOS Image Sensors (CIS): Past, Present & Future
- Vojislav on In-Memory Computing Challenges Come Into Focus
- Brendan on Engineering Talent Shortage Now Top Risk Factor
- WILSON PARDI JUNIOR on Engineering Talent Shortage Now Top Risk Factor
- Ludo Vandenberg on Lithography Challenges For Fan-out
- Jeff on The Paradox Of Automotive Electronics
- Allen Rasafar on Transistor Options Beyond 3nm
- Allen Rasafar on Week In Review: Manufacturing, Test
- Ed on Engineering Talent Shortage Now Top Risk Factor
- Mark LaPedus on Embedded Phase-Change Memory Emerges
- SStones on Engineering Talent Shortage Now Top Risk Factor
- Américo Dias on Engineering Talent Shortage Now Top Risk Factor
- Kati on Dodging The Next Generation Of Car Thieves
- Santosh K Kurinec on Engineering Talent Shortage Now Top Risk Factor
- Link on Engineering Talent Shortage Now Top Risk Factor
- Andrew D Reynolds on Engineering Talent Shortage Now Top Risk Factor
- P. Miguel Santos on Engineering Talent Shortage Now Top Risk Factor
- CH on Ultra-Scale Data Technology

Then, the reflected light enters into an analyzer, which is converted into a signal. From there, the data is crunched in a system, which provides thin-film measurements.

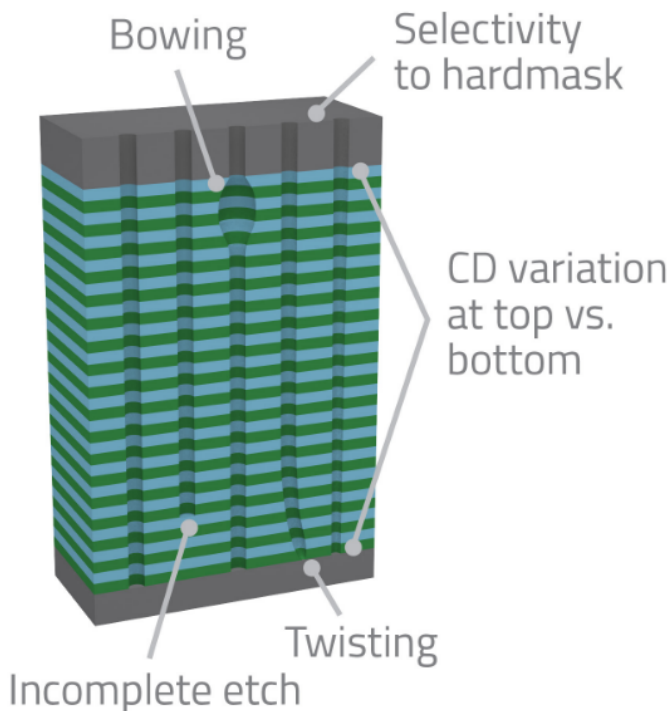
Generally, the thin-film measurement steps are relatively straightforward for today's 3D NAND. "As the stack continues to scale toward 128 layers, current technologies in metrology are capable and proven in R&D," said Kevin Heidrich, senior vice president of corporate development at Nanometrics. "As device manufacturers move to 256 layers and beyond, new improvements in the system are being developed to deal with very thick film effects and a lot of light absorption."

Following the stack deposition process, the device undergoes the high-aspect ratio (HAR) etch step. This is the most difficult step in 3D NAND, where an etch tool drills tiny circular holes or channels from the top of the device stack to the bottom substrate. A device may have 2.5 million tiny channels in the same chip. Each channel must be parallel and uniform.

"High-aspect ratio etch continues to be the most critical and difficult step in the entire flow," said Yang Pan, corporate vice president of advanced technology development at [Lam Research](#). "At 96 layers and above, not only does the memory hole module get more challenging, but other structures such as slits also become critically difficult with layer stacking."

This is also the most challenging metrology step. The goal is to obtain the "channel hole profiles" of the device. This involves a range of measurements, such as the top and bottom CDs of the holes.

The difficult part is to measure the uniformities and profiles inside the individual holes. At times, some channel holes are not uniform and may have a bowing effect. The challenge is to determine where the variations are located and to make the measurements.



Engineering Talent Shortage Now Top Risk Factor

- P. Miguel Santos on Engineering Talent Shortage Now Top Risk Factor
- CH on Using Sensor Data To Improve Yield And Uptime
- David Silva on A Brief History of Test
- Priya Mukundhan on Lithography Challenges For Fan-out
- Mohammed Abdelwahid on The Paradox Of Automotive Electronics
- Katherine Derbyshire on What's For Dinner?
- dick freebird on Why Analog Designs Fail
- Mike K on The Paradox Of Automotive Electronics
- Liz on The Paradox Of Automotive Electronics
- Lloyd Condra on Reliability Becomes The Top Concern In Automotive
- Marc-David Levenson on Lithography Challenges For Fan-out
- Craig Hillman on Reliability Becomes The Top Concern In Automotive
- Gil Russell on In-Memory Computing Challenges Come Into Focus
- Rafael Varela Della Giustina on Reliability Becomes The Top Concern In Automotive
- Gil Russell on What's For Dinner?
- realjij on The Paradox Of Automotive Electronics
- AC on Issues In Designing 5G Beamforming Antennas
- Mike on The Paradox Of Automotive Electronics
- Hau Lam (TSSI) on ATE Lab To Fab
- Ayush Gupta on Cutting The Cord: How Edge Intelligence Is Enabling The IoT To Go Where Cloud Can't
- Brian Grenon on Manufacturing Bits: Feb. 11
- belal iqbal on In-Memory Computing Challenges Come Into Focus
- Dean Phillips on Why Fabs Worry About Tool Parts
- Eugene Barash on Unsticking Moore's Law
- David Chapman on In-Memory Computing Challenges Come Into Focus
- Allen Rasafar on Manufacturing Bits: Feb. 5
- Brian Bailey on Bugs That Kill
- Moshe Frankel on Unsticking

Twisting Incomplete etch

Fig. 2: Channel etch challenges in 3D NAND. Source: Lam Research.

"New process control challenges are expected, including 3D shape and symmetry of both channel hole etch and the word line cut. Vertical stack dimensional control, including gate length and 3D film conformity control, are required," KLA's Hoover said. "Finally, with increasing stack height and the move to multi-deck structures, coupled with extreme wafer-level bow and in-die stress induced distortion, deck-to-deck channel hole alignment will be challenging."

For the channel holes, 3D NAND vendors want a tool that can measure the CDs inside a channel hole at each layer. So for a 96-layer device, vendors want to measure the CDs at 96 layers. The problem is that no such tool exists, so 3D NAND vendors must use the existing tool types. OCD is the most common technique, while TEMs, etch-back SEM and X-ray are also options.

For the channel hole profile apps, the industry uses an OCD-based system called a spectroscopic ellipsometer, which is an ellipsometer with a broadband light source. This tool is used in conjunction with a measurement technique called scatterometry.

The spectroscopic ellipsometer doesn't measure the actual structure, but rather it uses a model-based approach. In this process, you first develop a device with certain parameters. Then, you build a physical model of the device. A complex process might require multiple models.

You put a sample structure of the device in the ellipsometer and the light hits the target. The scattering light is measured at various polarizations, and then you compare the experimental results to the model.

Using a mathematical concept called regression analysis, you obtain the results. "The best way to explain the OCD mathematical signal processing aspect is that we combine the known interaction of light when it gets absorbed by different materials in the sample and the known behavior of light when it hits a repeating pattern of geometric features to construct some theoretical spectra. We can think of the theoretical spectra as a series of individual dots in a graph. We try to 'force' all of these dots to some minimum fitting error so that they coincide with the continuous line formed by the acquired spectra," explained Padraig Timoney, a principal engineer of metrology at [GlobalFoundries](#).

Scatterometry is widely used for leading-edge logic. This technique also works for the difficult channel hole profile metrology steps in 3D NAND. "We still focus on ellipsometry and reflectometry for the structure measurements and apply a high-fidelity OCD model to the measured spectral data or use complex machine learning," Nanometrics' Heidrich said. "Not only do we extract detailed profiles of the etch process with many critical dimensions through the stack, but we also determine tilt and other complex profile changes. With tier stacking, layer-to-layer channel hole registration also becomes a challenge. Much like super-lattice deposition, the thick nature of the films and high absorption will drive new

Focus

- Allen Rasafar on Manufacturing Bits: Feb. 5
- Brian Bailey on Bugs That Kill
- Moshe Frankel on Unsticking Moore's Law
- Humera Ahsanullah on And The Winners Are... 10 Formal Solutions To Einstein's Riddle
- guest on Variation's Long, Twisty Tail Worsens At 7/5nm
- Ghazi on What Happened To Aftermarket Car Audio?
- Allen Rasafar on Manufacturing Bits: Jan. 29
- Doc on Dirty Data: Is the Sensor Malfunctioning?
- Jerry on Fearless chip and fab tool forecasts
- Guest on Embedded Phase-Change Memory Emerges
- Xprmntl on What's Next For AI, Quantum Chips
- Pavan Bathla on Cutting The Cord: How Edge Intelligence Is Enabling The IoT To Go Where Cloud Can't
- Dr. James Ignizio on Variation's Long Tentacles
- Venkat on New BEOL/MOL Breakthroughs?
- David Estrada on Manufacturing Bits: Jan. 22
- Yair on Mostly Upbeat Outlook For Chips
- Stephen Su on Cutting The Cord: How Edge Intelligence Is Enabling The IoT To Go Where Cloud Can't
- Kevin Cameron on Taming Concurrency
- Allen Rasafar on Week In Review: Manufacturing, Test
- Bilim on Taming Concurrency
- David Rayer on RISC-V Pros And Cons
- Roy Stahl on Making IP Friendlier
- Katherine Derbyshire on Quantum Issues And Progress
- TONYD on Making Autonomous Vehicles Safer
- civil engineering on Anti-Drone Tech Emerges With Drone Growth
- Miller on Next-Gen Memory Ramping Up
- Ronald Niederhagen on Quantum Issues And Progress
- Kirstie Parker on Quantum Issues And Progress
- Tanj Bennett on People Vs. Self-Driving Cars
- Allen H Rasafar on What's the Right Path For Scaling?

many critical dimensions through the stack, but we also determine tilt and other complex profile changes. With tier stacking, layer-to-layer channel hole registration also becomes a challenge. Much like super-lattice deposition, the thick nature of the films and high absorption will drive new hardware systems.”

With OCD, the measurement times are fast, but is also takes time to build the models. Complex devices require more time-consuming models.

Besides OCD, the industry uses other techniques for the channel hole profile step, such as TEMs or SEM etch-back. These tools are used in R&D, but they can also be utilized in production.

The TEM enables users to measure the actual structure, but this is a destructive technique. A user must cut the wafer and examine the cross-section of the structure using a TEM.

Still, TEMs provide valuable data. “You can characterize the entire HAR channel shape using a cross-sectional TEM. If the lamella is thin enough—typically less than 30nm—you can see the individual layers in the TEM image. This allows you to characterize not only etch hole shapes, but also the uniformity of the oxide and nitride deposition processes,” said Larry Dworkin, director of product marketing at Thermo Fisher. “An alternative TEM technique is planar view sample preparation. This style of TEM looks at one ‘slice’ along the channel hole. Planar view TEM images of 3D NAND samples enable high-resolution characterization of the etch and deposition profiles for a specific layer.”

In another approach, Thermo Fisher has developed an etch-back technique using a SEM and a focused ion beam (FIB) tool. Like the TEM, the FIB/SEM approach is slow and destructive.

In an example of this approach, a 64-layer 3D NAND sample is delayered or milled layer by layer using a gas-enhanced FIB. Then, high-resolution SEM images are recorded at layer 6, 22, and 44. “SEM images can be acquired, and hole shapes characterized at specific layers, enabling within-wafer and wafer-to-wafer process control using statistical methods,” Dworkin said.

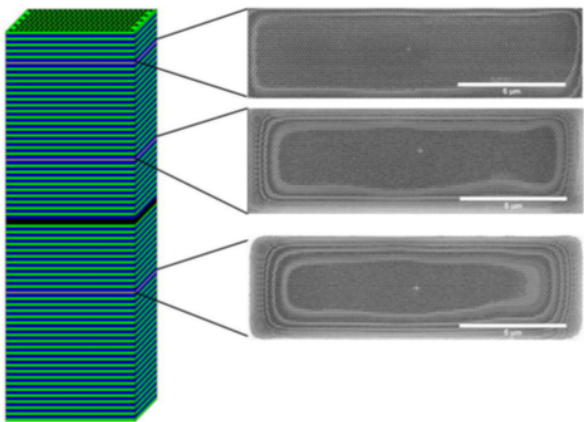


Figure 3: (L) 3D representation of the cell stack indicating in purple where images were acquired; (R) Representative SEM endpoint images of a surface upon which metrology is performed after top-

- And Progress
- Tanj Bennett on People Vs. Self-Driving Cars
 - Allen H Rasafar on What's the Right Path For Scaling?
 - Tanj Bennett on Why Chips Die
 - Tanj Bennett on Patently Absurd
 - Mark Sitkowski on Executive Insight: Wally Rhines
 - Tanj Bennett on Bridges Vs. Interposers
 - Ethan Krauss on System Bits: Nov. 27
 - Yovav Yahav-Amir on ATE Lab To Fab
 - Kevin Cameron on Making IP Friendlier
 - Thomas Barrett on It's All About The Data
 - Sergio Marchese on Using Software Approaches In Hardware Verification
 - Mark C on Fundamental Shifts In 2018
 - Farzad on Designing For Ultra-Low-Power IoT Devices
 - Karl Stevens on What Makes A Good AI Accelerator
 - Karl Stevens on Beyond The RISC-V ISA

Figure 3: (L) 3D representation of the cell stack indicating in purple where images were acquired; (R) Representative SEM endpoint images of a surface upon which metrology is performed after top-down PFIB processing. Source: Thermo Fisher

Meanwhile, following the HAR etch process, a gate is formed using various materials. To measure the composition of materials, the industry uses X-ray photoelectron spectroscopy (XPS). Then, the peripheral logic must be connected to the control gates. To measure the structure, chipmakers uses atomic force microscopy (AFM), which uses a tiny probe to enable measurements.

What's next?

As 3D NAND vendors move to 128-layer devices and beyond, the existing metrology tools will be pushed to the limits. "Many metrology methods from planar NAND will still play a role in process control for 3D NAND, but these techniques are not sufficient to fully monitor the etch and CVD performance of the high-aspect ratio structures like the channel hole," KLA's Hoover said. "The need for inline measurements of 3D shape and tilt for process monitoring will require a non-destructive technique. The move beyond 128 layers will bring additional wafer shape requirements to handle high wafer bow and increased deck-deck overlay requirements."

So new metrology tools are required, especially for HAR channel hole profiles. "OCD itself is a good one, but not a perfect one. For example, non-destructive X-ray plus OCD/SEM will be a 100% perfect metrology tool," TechInsights' Choe said.

The industry is exploring new tool types. In R&D, for example, the National Institute of Standards and Technology (NIST) and others have been developing a technology called small angle X-ray scatterometry (CD-SAXS). The X-rays used in CD-SAXS have a wavelength less than 0.1nm, according to NIST.

CD-SAXS is a non-destructive technique. In operation, X-rays hit a sample and the scattered electrons are captured and the data is crunched.

CD-SAXS has some challenges, namely cost. The throughputs are slow for leading-edge logic devices, so it might be better suited for memory.

"3D NAND is an ideal structure to measure with CD-SAXS. The X-ray scattering strength depends on the square of the height of a structure, so very tall structures (such as 3D NAND and DRAM) scatter hundreds to thousands of times stronger than finFETs. This improves the throughput enough to make CD-SAXS measurements of the overall shape of 3D NAND channel holes very interesting," said Joseph Kline, a materials engineer at NIST. "Also, since the transmission of CD-SAXS goes through the entire wafer, there are no penetration problems with measuring tall structures. This does introduce the complication that any buried layers in the stack will also contribute to the CD-SAXS signal and must be incorporated into the scattering models."

CD-SAXS won't solve all problems for 3D NAND. It's also unclear if OCD can do the entire job for future devices. So, it will take a range of tools to do the job.

the scattering models.

CD-SAXS won't solve all problems for 3D NAND. It's also unclear if OCD can do the entire job for future devices. So, it will take a range of tools to do the job.

Still, the metrology community must continue to innovate. In the future, 3D NAND vendors plan to develop devices with 500 layers and perhaps beyond, meaning the metrology and other fab tool sectors must keep pace. That won't be easy in a competitive and cyclical business environment.

Related Stories

- [3D NAND Flash Wars Begin](#)
- [Fab Equipment Challenges For 2019](#)



TAGS:

3D NAND

AFM

APPLIED MATERIALS

ATOMIC FORCE MICROSCOPY

CD-SAXS

CD-SEM

ELLIPSO METER

ELLIPSO METRY

FIB/SEM

FLASH

GLOBALFOUNDRIES

HAR

HIGH ASPECT RATIO ETCH

INTEL

KLA-TENCOR

LAM RESEARCH

MEMORY

METROLOGY

MICRON

NAND

NANOMETRICS

NIST

OCD

OPTICAL CD

OVERLAY SYSTEMS

REFLECTOMETRY

SAMSUNG

SCATTEROMETRY

SEMICONDUCTORS

SK HYNIX

SSD

STACK DEPOSITION

STEREOSCOPIC ELLIPSO METER

TECHINSIGHTS

TEM

THERMO FISHER

THIN-FILM MEASUREMENTS

TIER STACKING

TOSHIBA-WESTERN DIGITAL

X-RAY

X-RAY PHOTOELECTRON SPECTROSCOPY

XPS

Mark LaPedus

(all posts)

Mark LaPedus is Executive Editor for manufacturing at Semiconductor Engineering.

3 comments

Peter Manoj Says:

April 9, 2019 at 6:01 pm

Good article but was expecting views from memory companies .

Reply

Mark LaPedus Says:

April 10, 2019 at 11:03 am

Hi Peter. Good point. I will do that next time around. FYI. Many memory and logic companies keep their fabrication techniques secret. They don't want to tip their competitors and give them an advantage. For example, Samsung and others will discuss the NAND parts, but they won't talk how they are made. It's a proprietary. Believe me, I've asked them. However, for this article, I made some basic assumptions. Many 3D NAND companies use the same process steps. The general fab techniques are known.

proprietary. Believe me, I've asked them. However, for this article, I made some basic assumptions. Many 3D NAND companies use the same process steps. The general fab techniques are known.

Reply



Gil Russell Says:

April 11, 2019 at 6:57 pm

Great article Mark. Thanks for the hard work of putting this together.

Will you be able to include Fab Cycle times in a future report? Very touch subject but it would be a very well read article.

-Gil Russell, Webfeet Research

Reply

Leave a Reply

Comment

Name*

(Note: This name will be displayed publicly)

Email*

(This will not be displayed publicly)

Post Comment

Multi-Layer Processing Boosts In...

Geoff Tate

Finding The Source Of EUV Stocha...

Katherine Derbyshire

SEMICONDUCTORENGINEERING

ABOUT

About us
Contact us
Advertising on SemiEng
Newsletter Sign Up

NAVIGATION

Homepage
Special Reports
System-Level Design
Low Power High Perf

CONNECT WITH US

Facebook
Twitter @semiEngineering
LinkedIn
YouTube

Gil Russell Says:

April 11, 2019 at 6:57 pm

Great article Mark. Thanks for the hard work of putting this together.

Will you be able to include Fab Cycle times in a future report?
Very touch subject but it would be a very well read article.

-Gil Russell, Webfeet Research

Reply

Leave a Reply

Comment

Name*

(Note: This name will be displayed publicly)

Email*

(This will not be displayed publicly)

Post Comment

Document title:	Semiconductor Engineering 3D NAND Metrology Challenges Growing -
Capture URL:	https://web.archive.org/web/20190415095018/https://semiengineering.com/3d-nand-metrology-challenges-growing/
Page loaded at (UTC):	Fri, 15 Aug 2025 17:43:05 GMT
Capture timestamp (UTC):	Fri, 15 Aug 2025 17:47:07 GMT
Capture tool:	10.59.0
Collection server IP:	54.145.42.72
Browser engine:	Mozilla/5.0 (X11; Linux x86_64) AppleWebKit/537.36 (KHTML, like Gecko) Chrome/138.0.7204.97 Safari/537.36
Operating system:	Linux (Node 22.17.0)
PDF length:	11
Capture ID:	wP3zeD1UfKjabAcyCRypAj
Display Name:	dani.green