

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner
v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2025-00191
U.S. Patent No. 11,581,322
Issue Date: February 14, 2023

Title: THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH
ARRAY CONTACTS AND METHODS FOR FORMING THE SAME

**DECLARATION OF DR. JACK C. LEE IN SUPPORT OF
PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 11,581,322**

YMTC
Exhibit 2013
Micron v. YMTC
IPR2025-00034
Ex. 2013-001

**Micron Ex. 1003, p. 1
Micron v. YMTC
IPR2025-00191**

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I, Dr. Jack C. Lee, declare as follows:

I. INTRODUCTION

1. I have been retained by Micron Technology, Inc. (“Micron”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office (“PTO”). I am not an employee of Micron or any affiliate or subsidiary of Micron.

2. I have been asked to consider whether certain references disclose or teach the features recited in Claims 1-20 of U.S. Patent No. 11,581,322, which I refer to herein as the ’322 Patent.

3. My opinions and the bases for my opinions are set forth below.

4. I am being compensated at my standard consulting rate of \$680 per hour for my time. My compensation is based solely on the amount of time that I devote to activity related to this case and is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other financial interest in this proceeding.

II. BACKGROUND AND EXPERT QUALIFICATIONS

5. My *curriculum vitae* (“CV”) is attached hereto as Ex. 1004 and provides an accurate identification of my background, experience, and qualifications as an expert in electronics and NAND memory technology.

e.g., dummy and active vias, was well known. *E.g.*, Ex. 1036 (Tessariol), [0037] (“dummy-structure openings 56 and via openings 54 are formed at the same time (i.e., simultaneously)”), Fig. 9. Implementing different hole sizes requires using specific etch chemistries to account for the different sizes. *E.g.*, Ex. 1035 (Wolf Vol. 2), 33. In short, creating the contacts of the same size, using the same process steps, simplifies the process and shortens fabrication time.

[6.D] “a diameter of the dummy channel structure is smaller than each of a diameter of the TAC and a diameter of the peripheral contact.”

163. As I describe below, Nishikawa in view of the knowledge of a POSITA renders this limitation obvious.

164. My analysis under Claim [3.A] demonstrates that it would have been obvious to form dummy channel structures using the same process to form active channels. As the below explains, the dummy channels have a much smaller diameter than the TACs and peripheral contacts.

165. The array contains millions or billions of channel structures and is the densest area. The driving force in manufacturing memory is to create as dense as an array as possible for two reasons. First, memory capacity is obvious a key element of a memory. Second, the denser the array, the less silicon is necessary to create a given memory size. As density increases, the memory design becomes more cost effective. Thus, a large focus of design efforts for memory revolves around

fabricating a dense array. As Ground 2 demonstrates, for example, the desire for a dense array with high-aspect ratio memory holes led to the multi-deck design. This desire for a dense array was textbook material well before the filing of the '322 Patent. *E.g.*, Ex. 1010 (Micheloni), 211-215. The dummy channel holes will generally have the same size as active channel holes to maintain a uniform pattern and reduce the edge effect issues. I discuss this in greater detail in my analysis under Claim 3. One point of employing dummy channels is to produce a repeating, uniform pattern, where the array edges include the dummy channels. The premise of these benefits is using the same size of dummy and active channels. Further, as I describe under Claim 3, the dummy and active memory holes are made using the same process. Thus, a single process makes a uniform, repeating pattern of these dummy and active holes, all of which will be the same size.

166. The below figure illustrates a top-down view representing contacts and channels:

C. Ground 2: Nishikawa in View of Lu and the Knowledge of a POSITA Render Obvious Claims 4-5, 11-12, and 17-18

1. Motivation to Combine

203. As I explain in detail below, a POSITA would have been motivated to combine Nishikawa with Lu's teachings of multi-deck 3D memory stacks with a reasonable expectation of success for several reasons.

204. A multi-deck memory stack refers to forming a first stack of alternating dielectric layers and conductive (or sacrificial) layers, then forming a second stack of the same layers thereon, and potentially forming additional stacks thereon. Typically, as I describe below, additional processing is done on a stack before forming another stack thereon. In short, a deck can be thought of a conventional memory stack.

205. The design of multi-deck structures was the result of challenges in etching high aspect ratio channel holes. Recall that memory designs typically attempt to achieve a very dense memory array. In 3D NAND, this requires a memory with many layers and forming high-aspect ratio holes through that stack. These high-aspect holes became a limiting factor to memory density. Ex. 1010 (Michelsoni), 211-215.

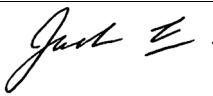
206. A multi-deck structure significantly aids in forming high-aspect ratio holes. As I explain below, in simple terms, a two-deck stack reduces the taper of the etch by a factor of two, effectively narrowing the width of the top of the memory

that the TAC is circular has no impact on the expectation of success, because circular TACs through multi-deck structures were commonplace. *See* §VI.

F. Secondary Considerations of Non-Obviousness

243. Based on my review of the '322 Patent's file history, I note that no secondary considerations of non-obviousness were identified in connection with the patent's claims. Nor am I otherwise aware of any evidence of commercial success, skepticism, failure of others, industry praise, unexpected results, or the like relating to the '322 Patent. Instead, as discussed above, it is my opinion that the subject matter embraced by the challenged claims was known in and obvious over the prior art.

244. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willfully false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1101 of Title 18 of the United States Code.

Date: December 2, 2024
Location: Austin TX
Signature: 
DR. JACK C. LEE