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Creating Higher Density 3D NAND Structures

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Identify the manufacturing issues associated with increased 3D NAND density to make the best tradeoffs and avoid structural collapse.

FEBRUARY 21ST, 2019 - BY: TIMOTHY YANG

3D NAND flash memory has enabled a new generation of non-volatile solid-state storage useful in nearly every electronic device imaginable. 3D NAND can achieve data densities exceeding those of 2D NAND structures, even when fabricated on later generation technology nodes. The methods used to increase storage capacity come with potentially significant tradeoffs in memory storage, structural stability, and electrical characteristics. This post will discuss the manufacturing challenges of 3D NAND structures, as well as techniques to advance the data density of 3D NAND devices, studied in our recent work.

3D NAND devices and their operating principles

3D NAND devices consist of three major components: channel areas where data is stored, which orthogonally pierce an alternating stack of conductors and insulating layers; a "staircase" to access each word line of the aforementioned layers; and slit trenches to isolate the channels connected to bit lines. A cutaway of a 3D NAND stack is shown below (left), alongside a schematic (right):

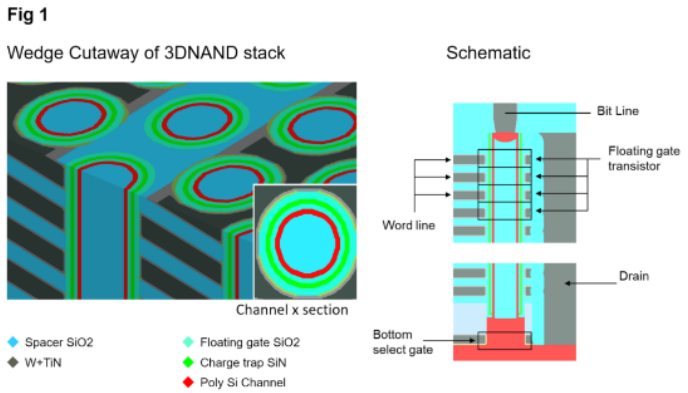

Figure 1: Wedge Cutaway and Schematic – 3D NAND Device

Charge trap type 3D NAND structures like the one shown above use an alternating stack of W and SiO2 with a vertical cylindrical channel that perforates the entire stack. Data is written or erased when a voltage is

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Figure 1: Wedge Cutaway and Schematic – 3D NAND Device

Charge trap type 3D NAND structures like the one shown above use an alternating stack of W and SiO2 with a vertical cylindrical channel that perforates the entire stack. Data is written or erased when a voltage is applied to a word line, and the electrons tunnel from the channel to the SiN charge trap layer.

The storage capacity challenge

While storage capacity is most easily increased by adding more layers to the stack, significant challenges arise as the stack gains height. The usable area for the channel is reduced, as shown below:

Fig. 2

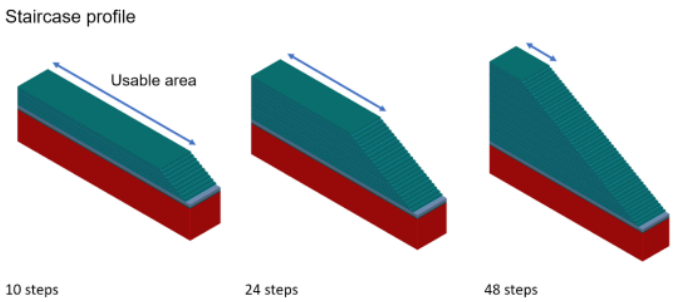

Figure 2: Staircase Span of 3D NAND stack. Adding layers to increase storage density requires additional staircase steps to access each layer. With each additional step, the usable channel area (indicated by the blue arrow) is reduced, since the volume underneath the staircase is unusable.

As the height of the "staircase" grows larger, the usable space decreases. An additional challenge is posed by the removal, in certain types of 3D NAND, of sacrificial layers in between the "steps" of the staircase. These layers are removed by wet etching to create room for an atomic layer deposition later in the fabrication process; thus, a large staircase means much longer, isolated layers suspended in thin air—and the possibility of structural collapse:

Fig. 3

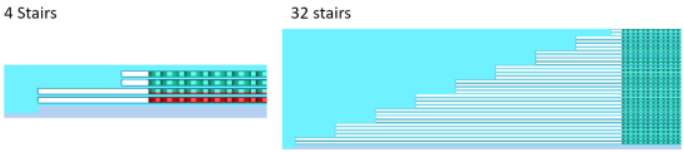

Figure 3: SiN sacrificial layer issues. Removal of SiN is required to create the ONON stack 3D structure in a 3D NAND. The left diagram displays a 20~30 nm thick SiO2 layer bridged over a 500 nm distance. With larger staircases (see right diagram), the oxide layer spans a greater dimension and there is a danger of layer collapse.

Partitioning the steps allows the insertion of more word line contact vias into the step structure and leads to a more compact staircase without this danger [2]. However, since all channels must be electrically separated, the number of accessible channels depends on the minimum wire pitch that can fit inside the channel pitch (if each channel has its own wire). With the fabrication techniques available right now (late 2018 / early 2019), this limits the number to about four channels.

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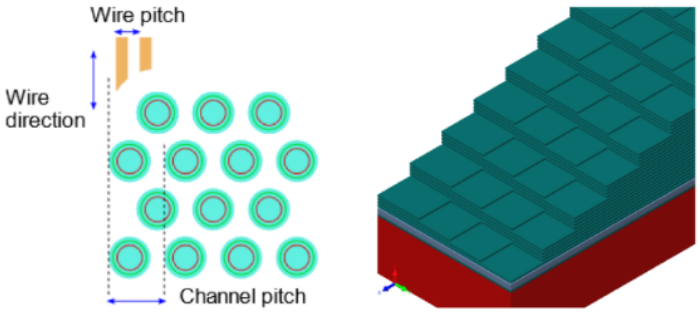


Figure 4: Tiered Staircase Structure. Left diagram: Using fabrication techniques available at the time of this writing (2018), this limits the channel area to about 4 channels. Right diagram: A more extreme example, where 4 steps are tiered into the structure.

However, a wider stack—desirable for the lower number of slits it requires—may contain more than four channels, which then need to be separated into periodic groups. Groups of channels may be separated by using an etch process to perforate a subset of the layers, effectively using several layers of floating gates as a selector transistor:

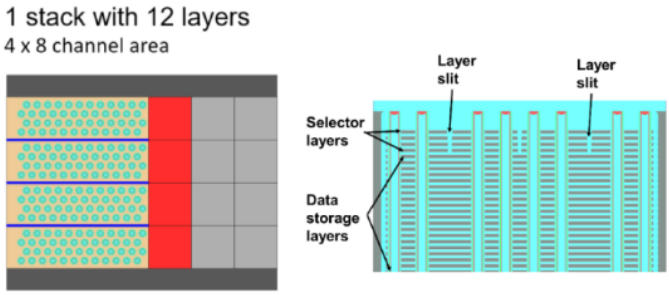
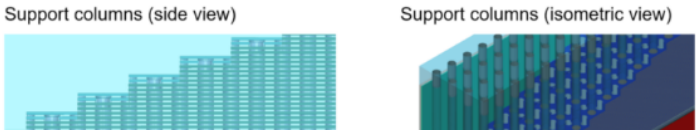


Figure 5: The left diagram shows the most extreme case of consolidating 4 stacks together in a 12-layer configuration using a 4-tier staircase. The right diagram shows channel and Bit Line Contacts.

Analyzing the effect of support columns

The complexity of the manufacturing processes involved in creating 3D NAND make it difficult to understand all of the tradeoffs in storage capacity, stability, and changes in other properties resulting from more layers in the stack, step partitioning, or layer perforation. A virtual process model, shown below, simulates the proposed fabrication steps. SEMulator3D was used to test the outcome of added support columns and different dimensions of contact vias. The added columns, whose holes are etched and then filled with SiO2, support the structure during the removal of the sacrificial material between the staircase layers:



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are etched and then filled with SiO2, support the structure during the removal of the sacrificial material between the staircase layers:

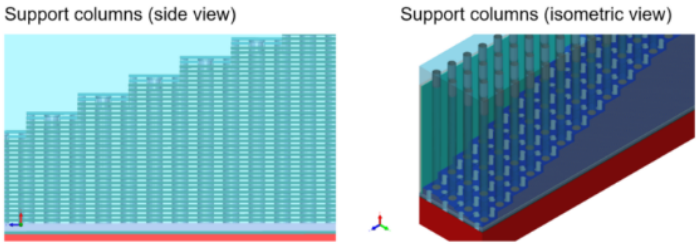

Figure 6: 3D NAND Support Structures. Side and isometric view showing the support structures. The right diagram has SiO2 sections colored white for clarity. The SiO2 columns perforate the staircase structure all the way to the substrate.

Electrical analyses performed on the Semulator3D model study an isolated a word line layer and simulate the effect of column size on resistance, as well as word line capacitance (in the right-hand plot, hole diameter refers to column width):

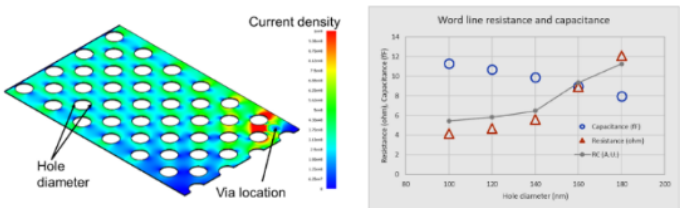

Figure 7: Modeled Resistance and Capacitance Values. Left: Isolated word line layer for electrical measurements. Right: Capacitance and resistance are plotted.

Enlarging support columns provides improved structural stability but increases word line resistance and uses additional space. Therefore, it appears to be beneficial to minimize the size and number of support columns as much as the structurally integrity of the device will allow.

Conclusion

This study demonstrates a real-life process model of a tiered, 3D NAND staircase structure and the virtual fabrication used to improve understanding of the tradeoffs in using support columns to enhance the structural stability of high density storage structures. To learn more about 3D NAND technology and methods to improve the data density of these devices, please download the detailed white paper.

References:

[1] "On the go with SONOS" IEEE Circuits and Devices Magazine (Volume: 16, Issue: 4, Jul 2000)

[2] "Apparatuses including stair-step structures and methods of forming the same" US Patent US20120306089A1

[3] "A novel double-density single gate vertical channel (SGVC) 3D NAND" 2015 IEEE International Electron Devices Meeting (IEDM)

[4] "3D NAND Flash Based on Planar Cells" Computers, Vol 6, 28 (2017)

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