Entegris

Considerations for Improving 3D NAND Performance, Reliability, and Yield

White paper

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INTRODUCTION

NAND flash technology has provided the world with nonvolatile memory capability for many years. Its uses have grown from flash drives to applications in laptops, smartphones, tablets, and solid-state devices now used in cloud storage operations. Over time, its structures have changed to meet growing needs for storage capacity, scale, and reliability demands, but the technology has proven its worth by delivering increased performance and lower power consumption with the promise of a lower cost per bit than previous solid-state memory technologies.

Initially, increased memory density and the corresponding cost reduction resulted from NAND flash memory manufacturers use of multiple patterning techniques to achieve progressively smaller dimensions. Unfortunately, 2D/planar NAND flash memory reached its scaling limit at the 15 nm node. This forced manufacturers to adopt a revolutionary approach of stacking gate-all-around NAND cell layers to achieve new performance targets. This was the dawn of today's 3D NAND structures, which represent a fundamental shift in the approach to scaling. Instead of scaling horizontally on a two-dimensional plane, this technology introduced vertical scaling, or growth in a third dimension, see Figures 1a and 1b. The promise of 3D NAND is higher density and a lower cost per bit.

2D NAND
String Plan View

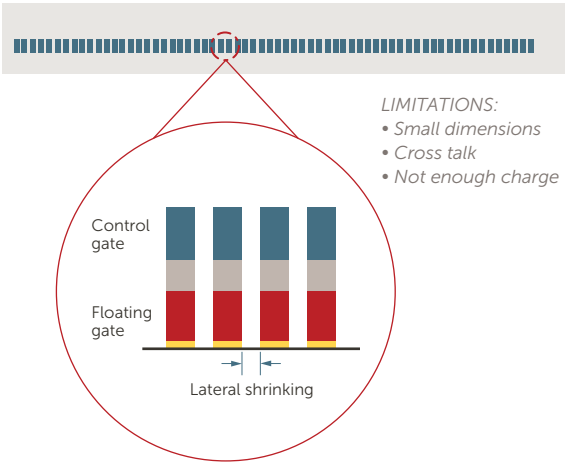


Figure 1a.

3D NAND
Vertical String Cross Section

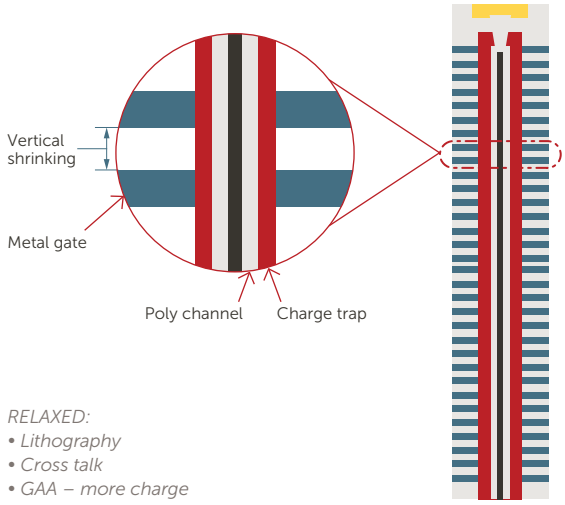


Figure 1b.

Figures 1a and 1b. The 3D NAND design stacks memory cells vertically in multiple layers to address 2D NAND scaling challenges, and to enable higher densities at lower cost per bit.

With all its promising advantages, however, the process complexity and capital intensity of 3D NAND manufacturing add to the challenges fabs are facing in terms of process control, yield, and economics.[1] With heavy investments, manufacturing processes for 24-layer, 32-layer, and 48-layer 3D NAND were developed in the hope of realizing competitive cost-per-bit. By many accounts, 64-layer and higher 3D NAND structures appear to be where the highest potential for cost savings occurs.

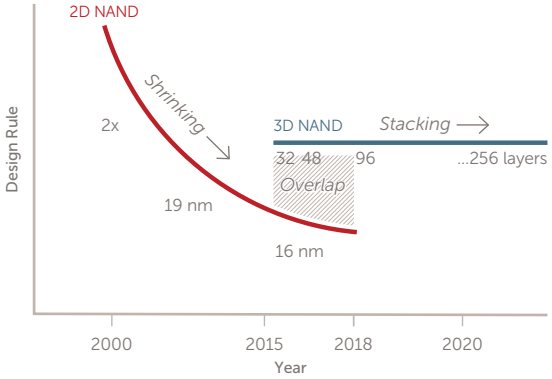


Figure 2. By stacking memory cells, 3D NAND architecture does not depend on lateral scaling to increase memory density.

Early applications of 3D NAND technology began in 2007, led by both Toshiba (bit cost scalable, BICS) and Samsung (vertical-NAND or V-NAND). Micron/Intel and SK Hynix swiftly followed, and YMTC China is the newcomer. These are the major players in the manufacturing of 3D NAND devices. The first high-volume manufacturing of 3D NAND was achieved by Samsung in 2013, and recently it has been accelerating production. By the end of 2017, it was estimated that the proportion of Samsung's 3D NAND flash production exceeded 70% of its total NAND flash production. In Q4 of that year, it exceeded 80% for the quarter.[2]

Even as 3D NAND races toward maturity and becomes a mainstream technology, chipmakers know there is still more to achieve to meet worldwide consumer and business data demands at lower costs, given the extreme complexities involved. It seems evident that the entire semiconductor industry, from chipmakers to equipment manufacturers to material suppliers, needs to work together to achieve the next step: greater manufacturing yield of higher-performing 3D NAND flash memory at lower cost. As with previous technologies, focusing on process efficiencies, materials innovations, and contamination control will optimize manufacturing processes, resulting in better performance, increased yield, and reduced costs. This paper looks at a few key areas that are worthy of addressing now, particularly etch and deposition challenges and contamination issues.

OPTIMIZE HIGH-ASPECT-RATIO ETCHING THROUGH MATERIALS DEVELOPMENT

In planar NAND technology, scaling is driven mostly by lithography. In scaling 3D NAND, extreme precision and process repeatability is required to create complex 3D structures with very high-aspect-ratio (HAR) features. Therefore, achieving success with 3D NAND requires innovative patterning solutions that minimize variability.[1]

Precision in etching extreme HAR features is critical for optimizing channel holes and trenches for cell access, as well as its unique staircase structure architecture, which connects the cells to the surrounding CMOS circuitry for reading, writing, and erasing data.

To date, amorphous carbon is the hard mask material typically used for HAR etching. This material is reaching its limits as the channel hole aspect ratio increases. There are several possible approaches under development to increase the selectivity of amorphous carbon including doping the amorphous carbon or adding other hard mask materials.

Latest information on the dimensions suggest the vertical pitch is around 100 nm and the stack thickness is around 5 µm, corresponding to an aspect ratio of around 50:1. To make matters worse, since the cell stack comprises stacked pairs of silicon nitride (Si_3N_4) at the cell level and silicon dioxide (SiO_2) to isolate cells, it is extremely difficult for dry etch engineers to achieve a continuous and straight profile while maintaining high enough selectivity to the amorphous carbon hard mask to reach the bottom of the structure. This is an area where engineers should look for significant material modifications, a material change, or even a new material, to help overcome these challenges.

Additionally, as multilayer stack heights increase, so does the difficulty in achieving consistent etch and deposition profiles at the top and the bottom of the memory array. For example, given a ratio of ~50:1, the selective removal of Si_3N_4 in the memory stack becomes a wet-etch challenge. The difficulty is removing the Si_3N_4 consistently at the top and bottom of the stack and across the wafer, without etching any of the SiO_2. Below 96 layers, this task is performed using hot phosphoric acid (~160°C); however, at 96 layers and above, a specially formulated wet etch chemistry is needed to improve process margin.

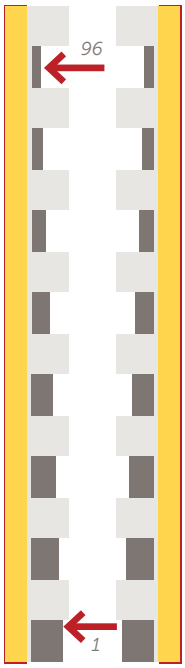


Figure 3: Selective Si_3N_4 removal relative to SiO_2. This is an important step in the fabrication of the cell stack, and the specifications must be met top and bottom alike.

Using a wet-strip process to remove hard mask material is potentially another example of a process where a formulated chemistry may be required to achieve specifications. The extreme processes required for HAR etching necessitate hard masks that are increasingly resistant to etching. Such masks are also more resistant to post-etch removal.

While dry etch tool and process innovations are required, the HAR features called for by 3D NAND, the hard mask, and subsequent materials-driven steps will also require development measures to bring stability, repeatability, and optimization to critical etch processes.

ELIMINATE THE SLOWDOWN

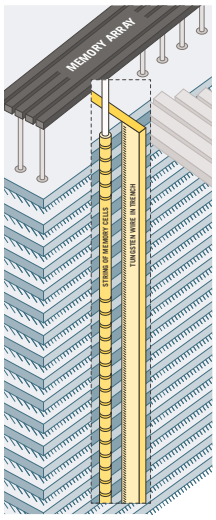


Figure 4: As the silicon channel gets longer, increasing the mobility of the electrons is critical.

With 3D NAND, as the stack gets taller, the silicon channel gets longer, and the speed of the device becomes limited by the mobility of electrons in the channel and the increased lengths they must travel. Manufacturers will be able to compensate for this slowdown by increasing the mobility of the electrons in the silicon channel with the help of dopant species in the conductive silicon channel. Germanium doping is one known method for improving electron mobility and is currently in development for 3D NAND processing. The requirement is to achieve uniform doping along an HAR silicon channel approximately 50 nm in diameter and several microns deep. Suppliers are working to find a more efficient means of providing germanium dopants for this application. A promising approach may be to replace the current practice of supplying germane diluted in hydrogen with a process that uses pure germane. The objective is to look for the best option to maximize the conductivity of the channel and preserve the operational speed of the device.

As previously stated, the purpose of the stair structure in 3D NAND is to provide access to cells at the bottom of the NAND stack thereby allowing the deposition of tungsten (W) to form the word-lines that allow access to the cell control gates from the outside peripheral circuitry. There is one step for every layer of cells, and as more cells are stacked, the staircase gets longer. Increasingly long lengths of conductor are needed to run the length of the staircase (top to bottom, on the order of 10 µm), which in turn introduces signal delays that affect device speed. It may be necessary to apply alternative conductors to tungsten, such as cobalt, ruthenium, or molybdenum, which have lower resistivity at thin dimensions to maintain overall device performance. Development work has started for precursors that can achieve atomic layer deposition (ALD) under these extreme HAR conditions and produce uniform films at the top and bottom of the cell stack. To avoid extreme aspect ratio processing-related challenges, some 3D NAND manufacturers are working on string stacking, a process by which multiple 96-layer structures are fabricated one over the other. This approach will alleviate increasing aspect ratio issues for etch and deposition, but, even with the string-stacked option, the staircase will increase in length, and there is still the need to not over-etch the W word-line. This is where formulated chemistry can be beneficial.

ESTABLISH DEFECT CONTROLS EARLY IN THE SUPPLY CHAIN

Process purity and defect controls are critical in 3D NAND processes. Tolerances for defects at larger chip sizes and in traditional NAND flash cell development were greater than they are at smaller sizes and in complex structures. In fact, as the number of transistors increases in a 3D stack, one defect could block more than one cell and affect the performance of the entire device. Consequently, all potential contamination areas must be identified and proper steps taken to avoid defects stemming from sources like etch chambers, material impurities, inadequate chemical filtration, wafer carrier devices, and photoresist bubble formation.

In extreme HAR plasma etch steps, internal etch chamber parts are exposed to long, high-powered, and high-temperature processing and subject to erosion and particle shedding. Traditionally, for protection from the aggressive plasma, etch chamber parts were spray-coated in a layer of yttrium oxide (Y_2O_3). Such a layer, shown in Figure 5, is extremely rough to the eye of a microelectronics engineer. This roughness results in significant shedding of small particles and contaminants. A higher-quality Y_2O_3 layer deposited by techniques like physical vapor deposition (PVD) or plasma-enhanced chemical vapor deposition is required. The higher density and smoother surface of this layer results in fewer wafer defects.

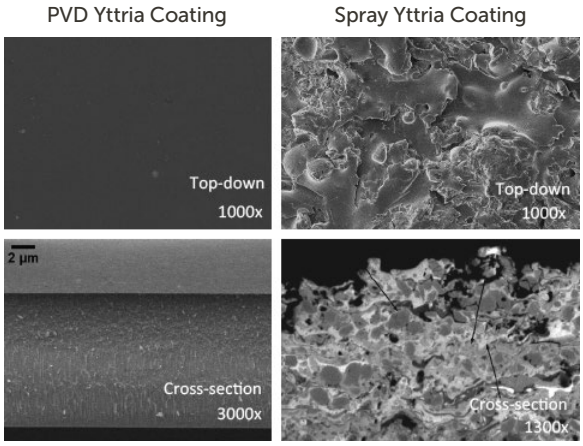


Figure 5. PVD silicon surface compared to plasma sprayed surface.

The same is true for ALD process. Recently, the demand for increasingly robust coating trials has extended to ALD chamber and tool parts. Since ALD processes deposit the cell layers whose job it is to manage charge, they are highly sensitive to any source of metallic contamination. Any surface that comes into contact with the precursor is a potential source of contamination. The delivery system, pipe, valves, and gauges. have internal parts that may require protection from contamination by coating techniques.

Parts coating is a highly tailored process. In some cases, PVD is sufficient, while ALD processing is used for parts requiring extreme step coverage. This greater attention to the quality of etch and deposition chamber parts, although initially driven by 3D NAND specifications, is increasingly demanded from high-end logic integrated device manufacturers (IDMs).

As with shrinking geometries in general, every generation of 3D NAND is becoming more sensitive to contamination. Material purity is critical, because defects have a greater impact on device performance. Purity control demands more attention.

Moreover, managing contamination in memory cell construction is critical to achieve optimum wafer yield and reliability. This begins with the chemicals that come into direct contact with every wafer. This is why chip manufacturers continue to pressure chemical suppliers to deliver a higher level of purity. Increasing chemical purity is the first step in enabling process cleanliness and improving device yield in the manufacturing process. It is critical then, to work with suppliers that are capable of high-volume manufacture scale-up, including advanced quality control measures, clean packaging, and logistics (e.g., including temperature control).

Considering the vast number of channel holes (>2 billion per chip) and the stack thickness of advanced 3D NAND devices, the volume of by-products generated during the etching step becomes more significant with each technology generation. Additionally, since the process steps are long, a batch of wafers typically spends extended time in some form of microenvironment, such as a front-opening unified pod (FOUP). Under these circumstances, by-products can be absorbed onto the inside FOUP surfaces and can be transferred to the wafer during queue time, causing defects. To prevent by-product re-adsorption within the micro-environment, an innovative solution was developed using polycarbonate FOUPs coated on the inside with a barrier material. This enables byproducts to be pumped away more efficiently, resulting in fewer defects.

For deep etch structures, very thick layers of higher-viscosity photoresist (~1000 cps) are needed to define the amorphous carbon hard mask layers. This level of viscosity can cause microbubble formation during resist dispense that translates to defects during subsequent patterning. Bubble formation on the wafer is not critical in larger dimension technology fabs; however, 3D NAND processes are more sensitive to lithographic defects because the dimensions are smaller (e.g., channel diameter is ~50 nm). Minimizing the bubbles requires a novel way to pump high-viscosity photoresist.

To that end, pumping systems have been developed and are being deployed for filtration, bubble removal, and dispense of high-viscosity photoresist. An important feature of these systems is a two-stage pump with the filter located between the pumps. During idle, the photoresist passes through the filter into the second stage, allowing discharge without limiting flow or releasing bubbles. Ideally, this pump will have network connectivity whereby an integrated flowmeter can upload the dispense volume to the fab parameter monitor system.

An alternative approach to reduce the likelihood of bubble formation is the bag-in-a-bottle concept. A clean bag, which is in a bottle, holds the clean photoresist. The space between the bottle and bag is pressurized to effectively squeeze the photoresist out to the tool. Eliminating the contact between the photoresist and the bottle material can help avoid contamination issues, and eliminating the air headspace above the resist in the bottle reduces the entrainment of trapped bubbles in the material.

In all, current and ongoing advances in contamination control are critical to achieving the process-purity levels required to help enable increased layers and dimension shrinkage for advanced chip development. To maximize the purity potential, the entire semiconductor ecosystem must work together to identify potential contamination sources and develop suitable solutions.

SUMMARY

As process shrinking reached the scaling limit in 2D planar NAND flash memory, and technology advanced to stacking NAND cell layers in 3D, a new set of process challenges related to stacking rather than shrinking emerged. Addressing these challenges is leading to innovations in:

- Extreme HAR etching, including all the peripheral innovations of hard mask and byproduct management
- Addressing needs in advanced contamination control to reduce defects
- Boosting electron mobility and conductivity to address slowdown issues
- Solutions to precisely construct memory cells in extreme geometries

Closer collaborations between integrated device manufacturers, original equipment manufacturers, and materials makers/contamination experts across the supply chain will allow process innovations that continue to enable 3D NAND into the foreseeable future. With vertical cell stacking architecture clearly moving toward 128, 256, and perhaps beyond, the industry will achieve higher-performing, more reliable devices with greater capacity and lower cost per bit.

ENTEGRIS SOLUTIONS FOR IMPROVING 3D NAND PERFORMANCE, RELIABILITY, AND YIELD

Entegris is a global leader in developing advanced materials, materials handling, and contamination control solutions for leading-edge semiconductor manufacturing. They understand the unique challenges of 3D NAND design and manufacturing and not only work with you to develop and optimize specially formulated chemistries for your etch and clean processes, they focus on understanding your operations and potential sources of contamination to develop solutions that ensure the integrity of your process. From liquid, solid, and gas chemistries to safe and efficient chemical delivery systems to advanced filtration technology and specialty coatings, their passion for purity feeds their desire to help you address the challenges affecting all aspects of the flash memory product chain, from design to supply to material handling, manufacturing, and delivery.

ABOUT ENTEGRIS

Entegris is a leading specialty materials provider for the microelectronics industry and other high-tech industries. Entegris is ISO 9001 certified and has manufacturing, customer service and/or research facilities in the United States, China, France, Germany, Israel, Japan, Malaysia, Singapore, South Korea, and Taiwan. Additional information can be found at www.entegris.com.

References

[1] Overcoming Challenges in 3D NAND Volume Manufacturing, Solid State Technology website: http://electroiq.com/blog/2017/07/overcoming-challenges-in-3d-nand-volume-manufacturing/

[2] Signaling End of Flat NAND Flash Era, Business Korea website: http://www.businesskorea.co.kr/english/news/ict/20216-signaling-end-flat-nand-flash-era-percentage-3d-nand-flash-production-exceeds-80

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