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Covering Everything about Memory Chips

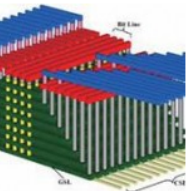
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3D NAND: How do You Access the Control Gates?

Published November 15, 2013 | By [Jim Handy](#)

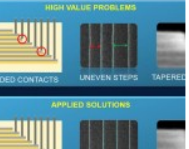


One of the thornier problems in making 3D NAND is the job of connecting the peripheral logic (the row decoders) to all of those control gates that are on layers buried somewhere within the bit array. Remember that the control gates are the conductive sheets of polysilicon or tantalum nitride at various depths in the chip.

The problem boils down to this: You can't run connections from each layer up or down the side of the chip to get to the CMOS circuits below. Instead you have to create a terrace structure to expose and connect to each layer.

These connections are made by etching a stair-step pattern into the layers and sinking vias down to connect with each level. This is illustrated in this post's first graphic showing Samsung's TCAT 3D NAND.

Stairsteps are difficult to manufacture, so The Memory Guy will explain this process in some depth in this post. After all, no chip today uses a stair-step etch, so it's a totally new process that had to be developed for 3D NAND. This etching must be precisely controlled because each via must align precisely with its polysilicon layer, and this is a huge challenge. Applied Materials shows this in this post's second graphic. (Click on any graphic to enlarge it. Right-click to open the larger version in a new window so you can "Alt-Tab" toggle back and forth from the text to the figure.)

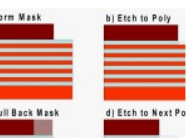


In the top left side we see stairsteps that are improperly connected to their vias. In the top circled connection the via only halfway connects to the step since steps were etched with an uneven widths. This is explained by the top middle photo. If steps are uneven, then the vias' connections to the wordlines will have inconsistent resistance, leading to unreliable performance. The photo at the right shows a tapered edge on a step, which leads to the problem depicted in the lower red circle on the top-left drawing. Here the via may or may not actually connect to the wordline, leading to the prospective failure of an entire flash block. The lower three frames of this graphic show the ideal: Steps are evenly etched and profiles are straight, leading to reliable connections.

One fortunate thing about the etch process is that layers can be specifically etched. Through various means, like etch chemistry and the color of the radiated light, the etcher can tell whether it is etching one material or the other, and can be stopped as soon as it reaches a new material. In the BiCS case a stairstep must stop etching when it reaches the polysilicon wordline plane; for TCAT etching would be stopped once it reaches a tantalum nitride plane. Either way, the process can be stopped at each layer very precisely.

Now, we could etch a portion of the stairstep, then perform a lithography step, then etch another, and so on, but this would create a ballooning number of lithography steps. While a typical NAND flash today might require about 35 mask steps, a 64-layer stairstep would require 64 mask steps in addition to the 20 or more mask steps used to build the underlying CMOS control logic, the connector at the bottom of the two-stack "U", and the columns themselves. For this reason a lithographic approach would be prohibitively expensive. (Keep in mind that the whole point of moving to a new process is to reduce costs.)

Instead, a process was developed in which lithography is used once to pattern a mask, and that mask is repeatedly used and etched to create the stairstep pattern. The third graphic shows how:



First the mask is photographically patterned and etched to create a hole the width of a single step (Step a in the graphic), and the first poly layer is etched (Step b). I have used a faded color to show what was just etched away. In Step c, the hard mask is etched sideways (which I have been told is very controllable) the width of a single step. This is called a "pull-back" and has been put into production for other processes, so it is a well-understood approach. Again layers are etched to the start of a new polysilicon layer (Step d), but the part that has already been etched goes down another layer, while the newly-exposed portion etches down to the first poly layer.

This process is repeated according to the number of layers there are. In the case of Samsung's 2013 V-NAND, with its 24 layers, this step would ideally be repeated 23 times. Existing production-volume semiconductor processes use a pull-back no more than once. Controlling 23 pull-backs can be problematic if it is not well controlled, since errors can accumulate. Today manufacturers will perform this process only 6-12 times before using a second photolithography step to create a new mask. As confidence grows, the number of pull-backs per lithography step will increase, with the ultimate goal of forming all of the stairsteps using only one lithography cycle.

Finally, a very thick silicon dioxide layer is deposited on top of the entire staircase, another pattern is lithographically created for the vias, and trenches are etched down to the polysilicon layer. The etch is controlled to remove only the silicon dioxide, so each trench stops when the polysilicon is reached.

The vias are then filled with conductive material (tungsten or polysilicon) to bring the control gate connections or wordlines to the top of the chip where it can be routed to other vias that connect them back down to the CMOS logic on the substrate that drives the array.

The stairstep etch is yet another very difficult and new process that must be managed to successfully mass produce 3D NAND. The vias must land precisely on their designated stairstep and not on any others, or the wordlines will be shorted to each other. If the via doesn't make a solid connection with a poly layer its resistance may prevent that entire wordline from working properly. This means that the mask pull-back must align precisely with the litho pattern of the connecting vias. You can imagine what a challenge this is!

What is striking is that the process of getting to the wordlines rivals the complexity of making the vertical bit strings themselves. Clearly 3D NAND involves a broad range of challenges, and it will take a significant effort to move from a planar process to 3D.

[Coventor](#) has shared a video of the process of making 3D NAND that details the stairstep process. This animation can be accessed from [another post on The Memory Guy](#). Have a look and you will be amazed at its complexity!

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Jim Handy Objective Analysis
Memory Market Research +1
(408) 356-2549 jim.handy
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This post is a part of a series called ***What is 3D NAND? Why do we need it? How do they make it?*** that was published in weekly segments during the fourth quarter of 2013 on [The Memory Guy](#) blog. The different sections are listed below, with a hot link to each section.

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